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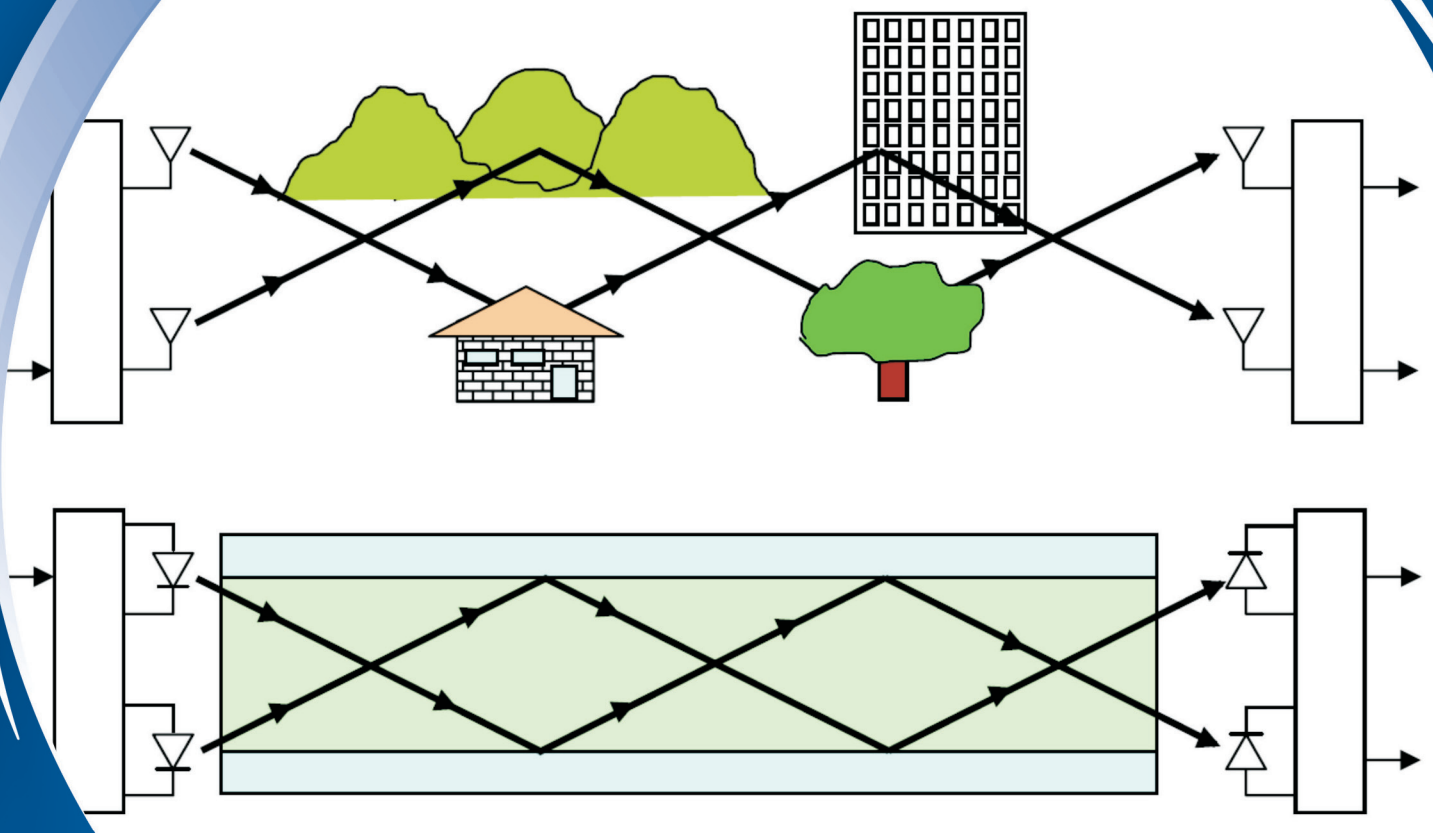

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Research challenges in optical communications towards 2020 and beyond

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Abstract: This paper presents an overview of future research activities in the field of optical telecommunications. The year 2020 is considered a milestone, when the capacity of optical communication links via a single optical fiber will reach the physical limitation called the "fiber wall". It is expected that advances in systems with a standard, single-mode, optical fiber, which enables increasingly higher transmission capacities due to accelerated scientific research, will reach the point where the capacity of the optical link via a single optical fiber will no longer grow. Due to this collision with the "fiber wall", research efforts to develop future solutions are all the more necessary. This article provides an overview of the fields in which the future development of optical communications will give the most focus. In the field of optical devices and components, the development goes in the direction of integrated optics and new optical fibers. In order to achieve the objectives, the new communication techniques comprise coherent communications, multidimensional modulation formats and multiplexing techniques, as well as the use of digital signal processing. Modern optical networks extend from the high-performance fiber optic connections in the backbone to broadband access in user's home, in the future their architecture will enable an adaptability to wavelength, bandwidth and modulation format. The main aim of the development towards 2020 and beyond is to build optical communication systems that will enable the transfer of large amounts of data with the minimum power consumption using the simplest and cheapest equipment.

Keywords: optical devices, optical fiber, optical networks, optical communication

Raziskovalni izzivi optičnih komunikacij do in preko leta 2020

Izvleček: Članek predstavlja pregled bodočih raziskovalnih aktivnosti na področju optičnih telekomunikacij. Leto 2020 se pojmuje kot mejnik, ko bo predvidoma zmogljivost optične komunikacijske zveze po enem optičnem vlaknu dosegla fizično omejitev imenovano »vlakenski zid«. Pričakuje se da bodo raziskave v sistemih s standardnim enorodovnim optičnim vlaknom, pri katerih se poskuša doseči vedno višje prenosne zmogljivosti, prišle do položaja, ko zmogljivost optične zveze po enem optičnem vlaknu ne bo več napredovala. Zaradi trčenja v »vlakenski zid«, so raziskovalni napori v bodoče rešitve toliko bolj potrebni. V članku je narejen pregled področij na kareta se bo razvoj optičnih komunikacij najbolj osredotočil. Na področju optičnih naprav in elementov gre razvoj v smeri integrirane optike in razvoja novih optičnih vlaken. Z namenom doseganja svojih ciljev nove komunikacijske tehnike vključujejo koherentne komunikacije, večdimenzionalne modulacijske formate in tehnike multipleksiranja ter s pridom uporabljajo digitalno obdelavo signalov. Sodobna optična omrežja se raztezajo od visoko zmogljivih optičnih povezav v hrbtenici do širokopasovnega dostopa v uporabnikovem domu. Njihova arhitektura pa bo v bodoče omogočala prilagodljivost na valovno dolžino, pasovno širino in modulacijski format. Cilj razvoja do in preko leta 2020 je izdelati optične komunikacijske sisteme, ki bodo omogočili prenos velike količine podatkov z najmanjšo porabo moči s pomočjo najenostavnejše in najcenejše opreme.

Ključne besede: optične naprave, optično vlakno, optična omrežja, optične komunikacije

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1 Introduction

Optical communications have been continuously developing over the past four decades and today they represent a mature industry [1]. New applications and services that require more and more data, and users who expect the instant and correct delivery of such data, without having to wait and experiencing errors, require increasingly sophisticated optical communication systems. Users are mainly interested in the speed

and the quality of the services, which provide them with a good user experience [2]. In this context, it is necessary to bear in mind that underneath a user's requirements there are many communication levels. Operators of telecommunications networks should ensure the smooth operation of their systems, which face the challenges of a constant increase in data traffic that must be transferred as fast as possible and with the least possible delay. They are, however, constrained by the costs associated with building (capital expenditures – Capex) and operating (operational expenditure – Opex) a telecommunications network. From the upcoming systems telecommunications operators expect a better ratio between transmission capacity and costs.

The capacity of the optical communication link is subject to the equipment available and its electronics, the communications channel and the type of transmission signal. All three elements are equally important for the correct and immediate delivery of telecommunications data, and therefore future researches will also be focused on these main areas: new optical devices, improved communication techniques and new architectures for optical networks (as shown in Figure 1). It is in these areas of optical communications that the most innovative solutions and development achievements can be expected in the future. There are many studies based on new modulation methods and new models for data transmission, which can also handle non-linear and randomly changing optical communication channels, whereby the objective is to provide higher bit rates and better signal or service quality. For these reasons, research in the field of signal issues, questions related to the transmission channel and electronics in the receiver and transmitter are closely inter-related and interdependent.

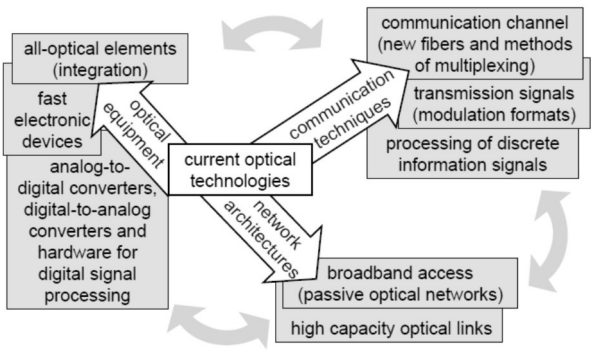

Figure 1: Three directions of development in optical communications.

Ever more powerful optical links, which are able to transmit more and more data over increasing distances, are the results of previous research. These optical links are now adapted to the use of a standard, single-mode, optical fiber, which has been a well-established transmission medium for a long time [1]. If future research achievements with the same time increment will shift the capacity boundaries of optical communication links by single-mode optical fiber [3], it is expected that by around 2020 the physical limit will be reached when the capacity of an optical line via a single optical fiber will no longer progress. The exact time of the emergence of the point of capacity constraint for a single mode fiber, called the "fiber wall" is difficult to predict. At present, research is needed, which will focus on new solutions in the field of optical backbone networks [4]. Once the "fiber wall" is achieved, it will be too late for this kind of research, because service providers will not be able to afford the subsequent installation of a parallel network in order to increase capacity. The installation of a parallel network is linked to Capex and Opex, which increase almost linearly with increasing capacity.

2 Optical devices

In the field of optical communication devices, developments are in the direction of integrated optics known as Planar Lightwave Circuits (PLCs) or Photonic Integrated Circuits (PICs). Integration has become an important tool in the effort to reduce the production costs of optical devices, increase the functionality of telecommunications networks and, ultimately, limiting the impact on the environment in relation to the amount of carbon-footprint emissions resulting from the use of electricity.

The development of optical circuits suggests that cheaper monolithic solutions will replace the current hybrid solutions [5]. The current technology of hybrid integrated circuits in a single enclosure combines various integrated circuits or discrete components that, connected together, perform certain optical and electrical functions. Future, monolithic integrated circuits will be a combination of passive and active circuit elements in a single optical chip. The aim of modern research is the integration of light sources (lasers), transmitters, modulators and signal processing elements (and vice versa; detectors, demodulators and receivers) on a single semiconductor substrate. Special attention will continue to be given to optical receivers as, based on the entire telecommunications connection, the signals in the receiver are the weakest and therefore this requires careful treatment.

The developments in the field of optical devices also includes the now familiar Micro-Electro-Mechanical Systems (MEMS) [6], Free-Space Optics (FSO), discrete optics, photonic crystals, ring resonators, gratings and plasmonic circuits and devices.

In relation to the development of new devices, the research will not focus only on III-V semiconductors (such as indium phosphide - InP) [7] but also on devices based on silicon, which is the so-called area of Silicon Photonics [8], and its family of oxides and nitrides. Silicon is more abundant, cheaper and more effective than III-V semiconductors. The latest developments in the field of integration are the integration of silicon waveguides with silicon nitride waveguides, or organic materials, the integration of waveguides of lithium niobate (LiNbO3) with silicon waveguides and the integration of liquid crystals with silicon waveguides. In the future these and other integrations will also be an important part of research in the field of optical materials and technologies.

The fact is that optical integrated circuits are much more expensive than the existing electronic integrated circuits; therefore, for many years the signal processing has been transferred from the optical domain to the domain of electronics. Electronics is also much more effective than optics, because it uses Digital Signal Processing (DSP). In the past decade, DSP became much more effective than analogue signal processing, which is still in use when we are working in the optical domain. Because there are no new technologies on the horizon that would enable the cheaper processing of optical signals, integration will retain an important role in combining the fields of optics and electronics in the years to come. According to the new system requirements, it is expected that the new generation of optoelectronic devices and integrated optics will be adaptable to the wavelength, bandwidth and modulation format [9]. Future research will also focus on the development of entirely new all-optical devices, which will have less consumption than the current opto-electronic solutions.

3 Communication techniques

The aim of the further development of optical communications is thus to extend the reach as well as increase the transmission capacity of optical links. Currently, the use of coherent optical systems is very interesting and very important. This idea emerged in the early 1980s and then "disappeared" due to the invention of optical amplifiers [1]. Now, a new need for the use of coherent systems has emerged that can come to life in reality with the use of new optical devices. The great advantage offered by coherent systems is the possibility of performing electronic equalization of the optical channel. Coherent optical systems can operate at very low levels of the received signal and very high bit rates, which range into the sphere of Tbit/s [10]. Interestingly, coherent optics uses techniques that are commonly used in radio systems, such as multi-level modulation formats (Differential Phase Shift Keying (DPSK), Quadrature Phase Shift Keying (QPSK) and various forms of Quadrature Amplitude Modulation (QAM)) and techniques with more orthogonal carriers known as Orthogonal Frequency-Division Multiplexing (OFDM). In order to correctly work a coherent system has to measure the complete received electric field (amplitude, phase and polarization) and use this information to electronically equalize chromatic, polarization and even modal dispersion.

More than two decades ago Wavelength Division Multiplexing (WDM) technology began to enforce itself on the backbone optical networks. In all the previous years, an increase in the transmission capacity of WDM technology went in the direction of increasing the number of channels, the used bandwidth and bit rate for each channel and reducing the channel spacing. All four methods of development have now reached a high level of engineering perfection. Modern, spectrally efficient systems have a large number of channels (sometimes over a hundred), which extend beyond the Conventional (C), Long (L) and even Short (S) wavelength bands, wherein in each of the channels the traffic can run with a bit rate of 40 Gbit/s and more. In accordance with the ITU-T standardization the downward trend of channel spacing has led to the current use in the distribution network of 12.5 GHz. The new network elements are adapting to the flexible grid of the optical spectrum.

While increasing the spectral efficiency of WDM systems by reducing the spacing between individual WDM channels, the development goes in two largely equivalent directions. In this way, complex procedures for shaping the spectrum are used, based on the orthogonality between the different WDM channels, either in the time domain or in the frequency domain. As an alternative to coherent OFDM transmission the system is known as the Nyquist WDM (Ny-WDM). In the case of Ny-WDM, the subcarriers are spectrally shaped so that their bandwidth is close to, or equal to, the Nyquist border for the emergence of inter-symbol interference and crosstalk between the channels [11]. In this context, to separate closely spaced WDM channels, highly selective optical filters are no longer used; instead, advanced Digital Signal Processing (DSP) [12] and Digital-to-Analogue Converters (DAC) are employed, which enables the precise formulation of the spectrum for each channel [13].

The use of high bit rates and long fiber ranges by WDM technology and erbium-doped fiber amplifiers (EDFA) triggered some previously insignificant restrictive phenomena. Among them, it is necessary to draw

attention to Polarization Mode Dispersion (PMD) and the nonlinearity of the optical fiber. The increased importance of PMD gave rise to many research studies, based on addressing the weaknesses and limitations as a result of the PDM as well as Chromatic Dispersion by means of digital signal processing. As shown in Figure 2, the transfer of the optical fiber, on the one hand limits the low signal-to-noise ratio, and on the other, a too high nonlinearity is becoming noticeable at large distances and high optical powers. The transfer can be improved by reducing the attenuation and non-linearity in an optical fiber, wherein Large-Aeff Pure-Silica Core Fiber (LA-PSCF) optical fibers are essential as they introduce the lowest attenuation (up to 0.161 dB/km) and two times smaller non-linearities known in a standard single-mode fiber.

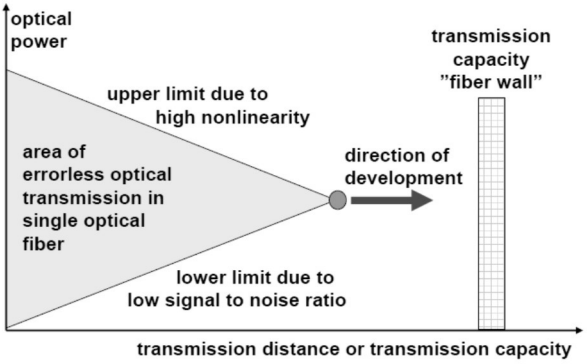

Figure 2: Transmission limits for optical fiber communications.

For radio communications the originally developed techniques are also used in the case where a so-called multimode fiber transmits a smaller number of modes, which forms the optical Multiple-Input Multiple-Output (MIMO) system [14]. As shown in Figure 3, while in radio communications the MIMO is reached with a larger number of transmission and reception antennas, in optical communications, multipath in multi-mode optical fiber is utilized. The generic dispersion in the fiber acts as a multipath in the space.

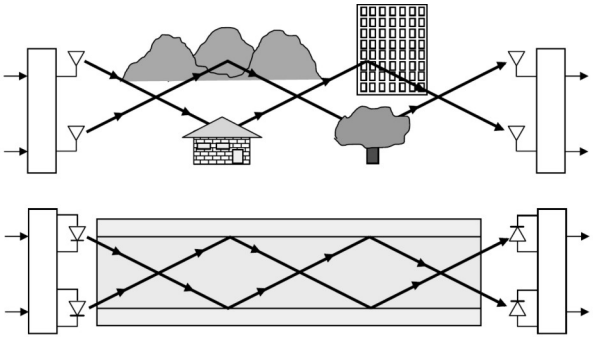

Figure 3: Radio and optical multipath.

In addition to the established multiplexing techniques, which can increase transmission capacities at the expense of the multi-dimensionality of the frequency, space or polarization, in recent years the exploitation of Orbital Angular Momentum (OAM) of electromagnetic waves presents itself as a new dimension of multiplexing in optical communications. In this context the orthogonality of the so-called vortex modes or modes with a phase singularity are exploited, which carry different orbital angular momentum [15]. Some researchers do not consider the use of OAM as a new technique of multiplexing, but as spatial multiplexing, which includes the MIMO. The similarity between optical MIMO and OAM is, in optical communications, seen in the fact that both of them exploit more modes for data transmission. They differ in the way of distributing the data between modes. The main difference between radio MIMO and optical MIMO is noticeable in the way of reception or the design of the receiver. Radio MIMO techniques require digital signal processing at the receiver side, with which individual data streams are distinguished by a knowledge of the transmission channel characteristics. Before and during the communication, the characteristics of the transmission channel are determined by a learning sequence, which is known to the receiving side. Neither digital processing nor a knowledge of the channel are not required for multiplexing with OAM, because to distinguish between the signals only spatial filtering is needed with this technique. In the case of radio technology, the difference is all the more apparent than in optical communications, because in OAM a direct sight between the transmitter and the receiver is desired, in MIMO the key requirement is a strongly emphasized multipath and thus Rayleigh statistics of fading.

For the transmission of multiplexing using the OAM via the optical fiber, a single-mode fiber is fundamentally inappropriate, since it does not allow the enlargement of more than one mode. Potentially, the single-mode fiber could be used at shorter wavelengths, where it acts as a few-mode fiber, or it would be necessary to use a fiber with an appropriately larger core diameter. If vortex modes spread along the normal multi-mode fiber, they make undesired coupling due to the frequency degeneration and birefringence caused by the bends and technological irregularities in the fiber. The ability to manage the vortex modes can be improved by using new types of fibers. For example, a vortex fiber [16] solves the problem of degeneration and enables the management, especially, of the lower modes (Figure 4). The air-core fiber is currently seen as the best solution for the management of higher modes.

Figure 4: Single-mode fiber (SMF), multi-mode fiber (MMF), few-mode fiber (FMF), vortex fiber, hollow-core photonic band-gap fiber (HC-PBGF).

Transmission systems up to the point are based on single-mode (single-core) optical fiber, but current technology is approaching the limit of the capacity of single-mode fibers in the C and L bands. By approaching the theoretical capacity limits of optical fiber [17] in inter-metropolitan connections, we will soon witness the use of a technology that seemed impossible five years ago. The example of such technology is Space-Division Multiplexing (SDM) in multi-core fibers (Figure 5) [18], which is the most realistic step to Pbit/s links [19], which are located behind the "fiber wall". In the past few years we have been witnessing a 10x increase in capacity of optical transmission by using spatial multiplexing. The development of new multi-core fibers will further increase system performance. Future research projects will deal with merging few-core fibers with each other and with a single-core fiber and with the development of transmitters, receivers and amplifiers for few-core fiber connections. Finally, few-core systems will also require commutations between the cores and the individual channels and bit streams within the SDM system, which will also be the focus of future research efforts.

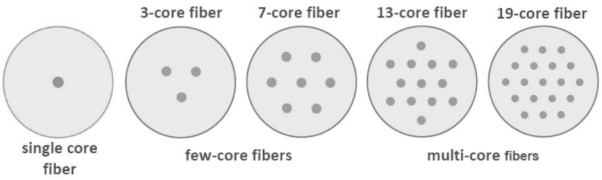

Figure 5: Single-core fiber (SCF), few-core fibers (FCF), multi-core fibers (MCF).

4 Optical networks

Research and development in the field of optical networks move towards mass broadband access in the vicinity of the end user and in the direction of high-performance optical connections between cities. The current three-segment network, comprising access, metropolitan and core networks, will in the future be substituted by a two-segment network that will include a combined metropolitan-access network and a core network.

Around the world, as well as in Slovenia, there is a lot of interest in managing the fiber all the way to user's home - Fiber to the Home (FTTH) [20]. A lot of development work has been invested in network architectures that enable high bit rates and the long reach of fiber from the central office to the user's home. In the background of new services there is the need for FTTH that will enable transmission speeds of up to several Gbit/s. The entire telecommunications sector also strives to meet the requirements for bandwidth in access networks for the required price of mass economy. For this purpose a number of new passive optical network architectures have been developed. For many years, Passive Optical Network (PON), based on the technology of classification using Time Division Multiplex (TDM), has been known. In the process of increasing the speed from 2.5 Gbit/s to 10 Gbit/s TDM-PON still benefits from technical improvements. The wavelength remodulation optical access network schemes are promising technique to reduce the crosstalk from downstream signal [21]. It should be noted that researches in the field of PON systems with a wavelength selectivity (WDM-PON) have been less frequent in last few years, as the requirement for building, or at least upgrading, the optical network presents operators with an unwelcome obstacle. TWDM-PON (Time Wavelength Division Multiplexing PON) and even coherent PON are becoming more noticeable.

Today, optical systems provide the backbone for the transmission of large amounts of data generated online, while using a packet, which is cheaper and more effective than any other type of transmission. The development is still in progress towards finding better and more expansive optical systems with high bandwidth, where the aim is to develop optical transmission systems that are suitable for the high-speed networking of continents, major cities and data centers. In this context, many researches focus on Software Defined Networks (SDN) [22], which will enable a transformation of the network without significant operator interference and in accordance with the demand for data transmission. SDN combine the optical network devices and the software that controls them. Programmable network interfaces enable a flexible optical network, which will have a new functionality such as dynamic control and virtualization. The optical physical level thereby obtains a certain degree of network intelligence, which will enable increased efficacy and the expansion of services. However, this also means more complexity in network operations, and therefore numerous studies in this area will be needed to optimize the algorithms of the design of optical networks [23] as well as the dynamic allocation of bandwidth [24]. Maybe this will allow the deletion of, or at least softening of, the boundaries between

telecommunications operators and content providers, which demand greater flexibility.

A significant proportion of all the optical connections are now also used to connect the data centers and within high-performance computers, because the compactness and capacity of optical communication has become indispensable to the design of large data-handling systems [25].

Data-center networks form a powerful backbone infrastructure for many existing internet service providers as well as the emerging providers of cloud computing. Many services, such as e-mail, on-line banking, software for business environments are happening in large data centers. The emerging cloud-computing model also encourages more and more innovation in the construction of extensive and efficient data centers. In typical data-center networks there are tens of thousands of servers that are connected to each other and are faced with technical challenges, such as high power consumption and the complexity of control in the transition to ever higher bit rates. It is from this perspective that optical communications represent a huge potential.

Finally, we must not forget that new systems are created that directly integrate optical and wireless technologies, and which are in the future expected to exceed the limitations faced by current traditional wireless and fiber systems. An example is Radio-over-Fiber (RoF), wherein different "wireless" radio or even mm-wave signals are transmitted via fiber to a remote antenna or in the interiors of buildings [26]. In the case of a practical network with a large number of cellular end stations and very few central stations RoF transmission has a substantial advantage over current data transfer. In addition, RoF systems with a stabilized optical path and a constant signal delay in an optical fiber over long distances allow redundant and precise synchronization [27] also to telecommunications networks.

Another example of optical and wireless technologies are optical wireless links [28], where a new generation of light-emitting diodes are used for the illumination and data transmission at home or in the office environment. If optical wireless link is done by using ordinary visible light emitting source, which is used for illumination, we talk about Visible Light Communication (VLC) [29]. VCL systems can be done as single color modulation or by using RGB-type light emitting source where simple WDM is implemented. We expect that low-cost, simple and high-speed VCL approaches will open door to various applications [30].

5 Conclusion

This article presents the major research challenges in optical communication technology towards 2020 and beyond. Like in the past, optical communications are expected to be promoted in order to develop their unparalleled speed in the future. Optical communications will also continue to be subject to continuous development and sophistication that will apparently overcome new boundaries. In fact, the competition for higher speeds, higher quality and enormous capacity continues to dictate an extensive development in the field of optical communications. In this respect, multi-level modulations, polarization multiplexing, coherent detection and digital processing have an important position as they give support to each other and complement each other. It may be that the introduction of a flexible network grid with WDM brought about a revolution in the field of the management of telecommunications traffic. The present, well-established scheme of General Multiprotocol Label Switching (GMPLS) will be replaced by the Software Defined Networking (SDN) of telecommunication traffic. This will ensure the easier implementation of programmable transponders, increase network flexibility and simplify its management.

A glimpse into the future shows that a standard single-mode fiber will be withdrawn after three decades of successful application to a new type of optical fiber, like multimode optical fiber, which was abandoned in practice in the past. Future research efforts in the field of optical backbone networks will be aimed at tackling the problem of "fiber wall", with two trends from the field of spatial multiplexing in sight. Scientific research will focus on systems with multi-mode fiber, which allows optical MIMO transmission or few-core or even multi-core fibers. In the case of the proper management of cross-talk between individual cores, even a hybrid solution can be expected.

In the past the very successful WDM technology required 10 years from first laboratory experiments to an implementation in practice. It is difficult to predict how much time will be needed for spatial multiplexing to become commercialized. Before a certain technology is applied in practice, it is necessary to make scientific discoveries and laboratory tests to engineering solutions and standardization harmonizations. Physical feasibility is not the only relevant factor for today's telecommunications operators, they are primarily looking for economic viability. An exponential increase in data traffic it is not easy to meet with a linear increase in the costs for building and operating the network, which gives a particularly difficult task to researchers in the field of optical communications.

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Development of Testing Method for Smart Substations with Prosumers

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Abstract: The paper presents a concept of design and realization of a new testing method for distribution substations which form a microgrid with prosumers. The distribution substation acts as a service provider for distributed resource units in a microgrid and can be used for bidirectional energy exchange between prosumers, such as electric vehicles, battery pack energy storage devices and utility networks. Use of distribution substations equipped with energy storing and bidirectional energy exchange capability enable peak load shaving and demand response, which will reduce the need for new investments into building new power sources or electric power grids to meet peak demand. While the state of the art in the field analyses mainly different theoretical microgrid topologies and integration of unidirectional distributed energy resources, focus in this paper is on practical issues regarding bidirectional energy exchange, which can provide solutions to microgrid manufacturing enterprises. Protection and control functions of the low voltage part of the distribution substation must be tested prior to exploitation. The new testing method for substations includes both computer simulations and practical verifications for automated energy exchange. Simulation results can be used to define and optimize parameters for protection and control functions before constructing a real microgrid. Functions of an experimental microgrid application were simulated with MATLAB, which showed that several prosumers can be served simultaneously and effectively utilized for peak shaving of utility network loads. The results of the simulations were used to develop sample control algorithms and program modules for the substation controller of the experimental microgrid prototype.

Keywords: bidirectional power flow, electric vehicles, microgrids, smart substation, substation testing methods

Razvoj testnih metod za pametne postaje s proizvajalci-porabniki

Izvleček: Članek predstavlja koncept načrtovanja in realizacije novih testnih metod za distribucijske postaje, ki oblikujejo mikro omrežje s proizvajalci-porabniki. Distribucijske postaje nastopajo kot ponudniki storitve za distribuirane enote virov v mikro omrežju in so lahko uporabljene za dvosmerni pretok energije med proizvajalci-porabniki, kot so električna vozila, hranilne enote in omrežja. Uporaba distribucijskih postaj s hranilniki energije omogoča rezanje vrhov porabe in odzivnost porabe, kar zmanjšuje potrebo po novih investicijah v nove proizvodne kapacitete, ki bi pokrivale vrhno porabo. Medtem ko se trenutne analize osredotočajo na različna teoretična mikro omrežja z enosmernim pretokom energije, ta članek opisuje praktične vidike dvosmernega pretoka energije in nudi rešitve proizvajalcem mikro omrežij. Pred uporabo distribucijskih postaj je potrebno testirati zaščite in kontrolne funkcije. Nove testne metode vključujejo računalniške simulacije in praktična preverjanja avtomatiziranega prenosa energije. Simulacijski rezultati so lahko uporabljeni za načrtovanje in optimizacijo zaščit in kontrolnih funkcij realnih mikro omrežij. Funkcije poskusnega omrežja so bile simulirane v MATLABu. Rezultati so pokazali, da se lahko oskrbuje več proizvajalcev-porabnikov hkrati, ki učinkovito omogočajo rezanje vrhov porabe energije. Rezultati so bili uporabljeni za razvoj kontrolnih algoritmov in programskih modulov za kontrolo postaj prototipnega mikro omrežja.

Ključne besede: dvosmerni pretok energije, električna vozila, mikro omrežja, pametne postaje, testne metode

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1 Introduction

Smart Grids and microgrids have attracted much attention due to the increasing awareness of energy conservation and environmental problems. Use of different prosumers (e.g. modern electric vehicles) and their effective integration into electric power grids depends on the technologies applied around distribution substations. The concept of a prosumer has two common meanings: a union of words of a producer with a con-

sumer or a professional consumer [1]. "Producing consumer" type of a prosumer either generates energy or consumes energy. A "professional consumer" is a well-educated, skilled consumer who commonly makes smart purchasing or selling decisions using additional information [1], [2]. Integration of prosumers to electric power grids is beneficial both to utility networks and prosumers. Prosumers can consume or generate electric energy and improve reliability of electric power supply (e.g. peak shaving, frequency regulation, voltage sags) by integrating renewable energy resources to electric power grids more efficiently. Prosumers can earn additional money with selling ancillary services to utility networks.

In energy trading, the role of distribution substations will increase when different types of prosumers are connected to their output bays. In this paper, mainly electric vehicles (EV) with Li-Ion batteries or battery energy storage unit (BESU) applications are considered as prosumers. EVs with vehicle-to-grid (V2G) capability can be charged or discharged through substations. Other types of prosumers that could be connected with distribution substations are generators (e.g. photovoltaic), energy storage units (e.g. supercapacitors, electrolyser, flywheel) or different subsystems (e.g. other bidirectional distribution substations, microgrids or smart homes).

The aim of this paper is to develop a new testing method for the next generation distribution substations (smart substations), which includes optimization of requirement validation algorithms and testing scenarios (defined according to the rules of testing functions), and selecting proper parameter values for protection and control functions. The method can be applied in the construction of new distribution substations (existing substations are typically designed for given purpose and do not have reserve space to expand to include energy storage).

The developed method will be used in the construction of an experimental microgrid prototype. For transparency, example control topologies for the substation controller are presented.

The paper is divided into ten main parts. Parts 2 and 3 describe the state of the art of smart substations and the proposed topology for smart distribution substation. Part 4 describes the state of the art of substation testing methodology. Part 5 introduces the new approach to substation development methodology. The substation organization and control architecture are firstly described and simulated according to the requirements, then saved for reuse in a repository. The results are practically verified during the experiments, using the experimental microgrid, and production cycle of the smart substation, and finally accepted by prosumers. General functional requirements and parameters are defined for distribution substations with prosumers (BESU and EV). Part 6 discusses the principles of the development and testing of control algorithms for the central controller of the distribution substation. Part 7 describes simulation of the control functions for bidirectional energy exchange between Li-Ion prosumers and the utility network with MATLAB Simulink. Parts eight and nine discuss the principles of testing novel distribution substations and the data required during the tests from prosumers. Finally, future studies and conclusions are presented.

2 State of the art of smart substations

Several papers have addressed microgrid (distributed resource island systems according to IEEE 1547.4) architectures [3]-[8], V2G architectures [9], [10] and bidirectional converter topologies [11], [12]. However, research papers regarding testing of microgrids or presenting technical analysis about control functions for automated bidirectional energy exchange between distribution substations and several prosumers are scarce. Several papers have addressed the concept of virtual power plants (VPP) [13], [14], but no technical analyses show how the concept could be realized in real applications.

Some reports address the testing of distributed resource units [15], PV [16] or V2G [17] applications and energy storage systems [18], [19], but not regarding prosumers in general.

Some companies are using the term "smart substation" [20] to describe substations, which only monitor and transmit data to a microcontroller or outside server. These types of substations include no devices e.g. for suppressing harmonics [21] or providing uninterruptible power supply.

Today's smart substations are either in the planning or in the prototype phase. Few projects can be found in field testing [22], [23].

It can be concluded that distribution substations for integrating prosumers to electric power grids are still in the development phase. IEEE 1547 standard presents mandatory requirements [24] for interconnection itself and testing. IEEE 1547 standard is not a design handbook or application guide. Thus, it is necessary to solve how to construct next generation distribution substations and how to test these substations.

3 Topology of distribution substation for integrating prosumers with utility network

Transformer substations are part of the electric power system concentrated in a given place to transmit electric energy, distribute power and step up or down the voltage. Substations for medium voltage grids (typically 6-24 kV) transform 3-phase medium voltage to 3-phase AC low voltage (typically 400 V AC).

State of the art distribution substations do not include bidirectional energy exchange capability between prosumers, LV side consumers and utility network. Next generation distribution substations could control electric power quality in a local area, maximize benefits for prosumers and owners of microgrids, integrate several prosumers to electric power grids (e.g. large EV parking lots).

An example of a distribution substation topology for microgrids is presented in Fig. 1.

The substation consists of a MV switchgear, a transformer and a low voltage (LV) switchgear (with switches, smart meters, contactors and power converters). The substation allows bidirectional energy exchange between all the prosumers and consumers that are connected with the integrated AC & DC bus, and transfer energy to the utility network. Prosumers are connected either to behind AC/DC power converter with a common DC bus or to a common AC bus. For every prosumer in the common DC bus separate protection and switching apparatuses are available at the DC side.

The BESU in the substation is connected with the common DC bus. The DC bus voltage can float in the specified voltage range to increase the efficiency of energy conversion. For example, the BESU can support fast charging of EVs, provide backup energy and power capability for a utility network power outage. As the number of renewable energy sources is increasing in the grid (e.g. wind and solar energy), the balancing of excess generation sources and load demands can be controlled through the substation. This enables stabilization of the grid AC voltage and frequency [23].

The presented distribution substation topology is beneficial mainly to the future owners of a microgrid (e.g. manufacturing enterprises) for controlling energy storage and usage inside the microgrid. The master controller of the substation can be adjusted (e.g. scheduling, trading, optimization) according to the needs of the future owners of the microgrid.

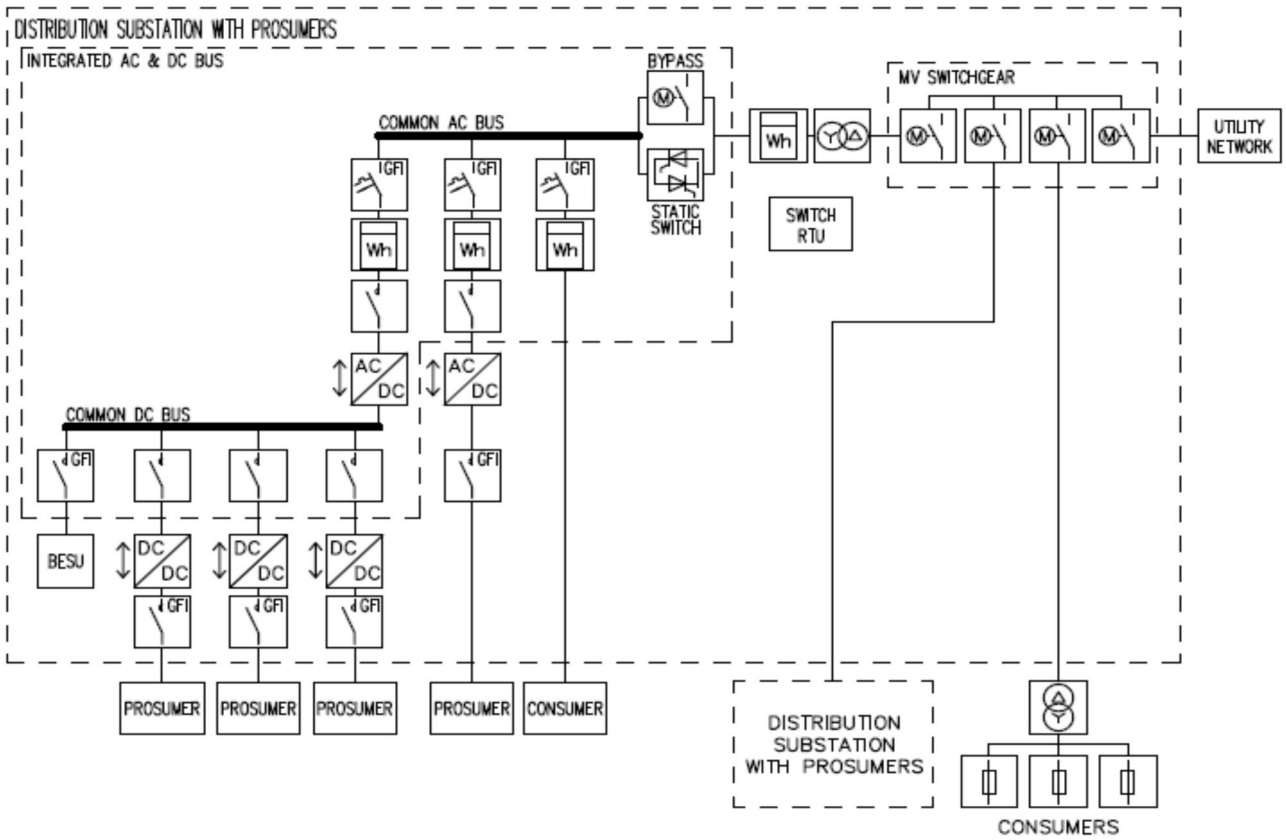

Figure 1: Topology of a distribution substation with an integrated AC & DC bus and prosumers for microgrid applications.

4 State of the art of substation testing methodology

Ordinary substation testing is divided into factory routine tests and field tests [25]. Factory routine tests are divided into visual tests, mechanical tests and electrical tests.

During visual factory tests, a general check is carried out to ensure the hardware is in accordance with project documentation, there exist no errors of assembly and all labels are correct. Also the absence of leakages will be checked.

The tightness of all electrical and mechanical connections will be checked during factory tests.

Electrical factory tests include: installation correctness (topology), wire insulation resistance and tests of protection and switching apparatus. Transformer parameters will also be checked [25]. A very important part is to test the substation under nominal current and voltage (separately).-

Substation field tests are is similar to factory tests. During mechanical field tests, only the connections installed on site will be tested. Electrical field tests measure the insulation resistance of only those cables which are installed on site. Protection systems and switchgear will also be tested on site. The testing methodology details will vary in different countries and legislative areas. [26], [25], [27].

The information structure (testing requirements, testing methods, test cases, functional descriptions and other detailed views as source texts of control programs) of an ordinary substation can be represented using a requirements definition software e.g. Axiom (Fig. 2).. The collected information is used as reference during optimization, validation, and verification processes.

The software allows parallel use of requirements information, simulation and verification data enable faster validation of microgrid projects.

Independent certification of specified and tested microgrid modules, such as energy storage systems, can reduce installation time at customer site from weeks to hours, since certification transforms energy storage from a nascent technology into a safe plug-and-play appliance. After the integration of the system (substation, prosumers and utility), main use cases need to be tested. The verification process commonly demands rigorous testing and evaluation and is a time consuming and costly process.

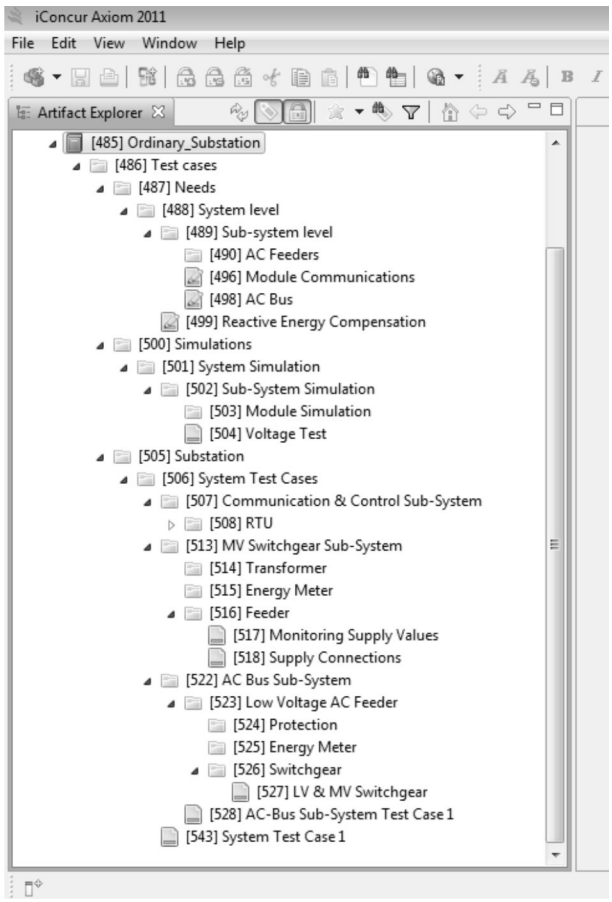

Figure 2: Screenshot of testing requirements for ordinary distribution substation.

5 New approach to substation development methodology

The substation testing methods, which were described in the previous part of this paper, are included in the construction of a new methodology. The new methodology is based on a software development methodology (X-model) and is visually represented in Fig. 3. During software testing, it is useful also to follow IEEE standard 829-2008 recommendations. The Requirements box (including e.g. application software functional requirements, substation user requirements, use cases etc.) is visualized in the left-upper part of Fig. 3. Documentation and repositoring is visualized in the left-lower part of Fig. 3. Prototype construction is visualized in the right-lower part of Fig. 3. Producing is visualized in the right-upper part of Fig. 3.

Next chapters of the paper introduce some control aspects of the smart substation and their testing methods.

Functional requirements and parameters for distribution substations with prosumers are described in different standards (e.g. IEEE 1547.1 and VDE-AR-N 4105 [28]).

IEEE 1547.1 standard describes test procedures for equipment interconnecting distributed resources (e.g. prosumers) with electric power systems. In addition, the German standard VDE-AR-N 4105 provides for the improved network integration of decentralized power generation (in particular, inverter-based generators).

During normal operation, the magnitude of the voltage change caused by the generating prosumers must in any connection point not exceed a value of 3 % compared to the voltage, when the generating prosumers were not connected. Voltage change of 3 % in the connection or disconnection with the distribution substation should not occur more frequently than once every 10 minutes.

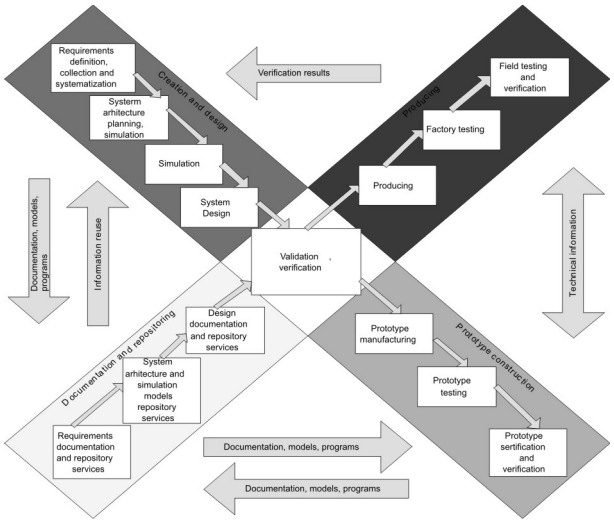

Figure 3: Substation testing methods in the developed methodology.

VDE-AR-N 4105 specifies the disconnection of inverters connected to the LV network due to grid side disturbances [29]. When the voltage variation (undervoltage, overvoltage) exceeds the limits $80\%U_n<U_{pcc}<110\%U_n$, disconnection is necessary within 100 ms. In case the upper limit is exceeded, according to EN 50160, inverters must shut down. If the frequency limits $47.5Hz<f_n<51.5Hz$ are exceeded, the inverters must disconnect in 100 ms. The inverters are allowed to reconnect after a fault, when the following conditions are satisfied: $85\%U_n<U_{pcc}<110\%U_n$, $47.5Hz<f<50.05Hz$, minimum delay of 5 s. The specific behaviour of the inverters and controlled rectifiers under a grid faults is very important, since it is desired that the system avoids disconnection as much as possible.

Frequency variation is a common problem which affects power systems. To avoid unbalanced conditions, distribution substations serving prosumers must be capable of adjusting power production by means of frequency regulation. Generating substations with the capacity over 100 kW have to reduce their real power in steps of at most 10 % of the max. active power [29]. Generating bays have to reduce their power output with a gradient of 40 % Hz, when a 50.2 Hz frequency limit is surpassed. The output power is allowed to increase again when the frequency is below 50.05 Hz. Outside the frequency limits, the bays have to disconnect from the grid. Controllable substations have to reduce the power output to the target value within a maximum period of time of 1 minute. If the set point is not reached in the mentioned time period, the generating prosumers must be disconnected.

6 Testing of control algorithms for the central controller of the distribution substation

The Remote Terminal Unit (RTU) acts as a central controller in the substation and also as the master in a microgrid. Each prosumer might include its own control unit handled as a slave device that serves the purpose of controlling prosumer related lower level tasks. The RTU operates the substation in general, while the functionality of safe and fast fault response is handled by protection apparatus (fuses, circuit breakers etc.). The purpose of the powerful RTU is to read the status and operational parameters of microgrid prosumers, to send control values and configuration information to the slave devices, to control bidirectional energy exchange between prosumers and the utility network (control of prosumer and utility bays), and to perform the following functions: scheduling, electricity trading (with electricity retailer), grid constraints observer (retrieve information from distribution system operator) and interface provider to EV owners (e.g. departure time, energy prices). In regard to the topology (e.g. integrated AC & DC bus) chosen, each bay for a prosumer might include its own slave controller or the central RTU could control all prosumer bays itself.

Communication between intelligent electronic devices (IEDs) of the next generation substation, including RTU and prosumers, should be realized with the IEC 61850 protocol [1] as much as applicable. The IEC 61850 protocol uses Ethernet as the basic communication technology, currently at a speed of 100 MBit/s. Different protection and control functions should be scattered between substation devices in order to speed up data flow between the devices [30].

Control algorithms for the RTU have to be tested prior to the exploitation of the distribution substations. This requires verification of the protection and control algorithms both in the simulation and laboratory environment, and then in factory testing.

Before any energy exchange in either direction can be executed, the communication side must be tested with data retrieval and sending. If the communication link is available and safe, data is being polled by RTU from the prosumer. For example, for EVs it is required to monitor the battery current and temperature in order to protect the prosumer during charge and discharge, thus it is necessary to gather the following data about the battery of the prosumer: state of charge (SOC), state of health (SOH), battery pack open circuit voltage, measured temperature values and nominal values of various BMS predefined parameters (rated capacity, maximum and minimum values of battery pack voltage, SOC levels, current and temperature).

To provide the best service to the prosumer (e.g. owner of the EV), the RTU needs data about the maximum possible time period the prosumer could stay connected to the microgrid, minimum SOC level required before departure and an agreement from the prosumer to allow partial discharge of the battery, which would be compensated according to the agreement with the service provider. This information can either be received remotely by the RTU or partially entered using a user interface (human to machine interface (HMI) panel, smartphone application etc.).

After testing the communication, protection functions have to be tested in order to evaluate and determine whether it is safe to proceed or not. This requires the presence of the main supply for testing. The algorithm for the RTU contains many protective functions:

- AC side protection functions are mainly realized by intelligent bay controllers (e.g. modern smart meters), ensuring that voltage and frequency are in the determined range and current values do not exceed defined maximum values. Digital input data from smart meters for the RTU:
  - automatic or manual mode of charge,
  - AC side circuit breaker closed,
  - positions of AC side contactors,
  - positions of the isolation monitoring devices
  - power related quantity values,
  - faults.
- DC side protection functions realized by the RTU for each bay ensure that DC side primary and auxiliary voltage values are in the determined range, current values do not exceed maximum values. Digital input data:
  - positions of DC side circuit breakers and contactors,
  - positions of isolation monitoring devices,
  - EV connector locking.
- General protection functions realized by the RTU ensure that parameter values of prosumers' BMSs and power converters are in the determined range, active monitoring of AC and DC side protection inputs, emergency stop pushbuttons not activated, connection termination not required by EV owners.

It must be verified that all data is being collected and logged by the RTU in order to generate operation and error reports.

If any of the criteria set by the protection functions is not met, the charge or discharge of prosumers must not be allowed and should be interrupted (soft stop) if a fault occurs during a process. All critical protection functions are carried out redundantly, independent of the RTU, and will be triggered automatically (hard stop) when fault conditions occur.

When the general protection functions have been tested, the RTU processing side can be tested. When no error conditions are present, the RTU must calculate the process values using polled and user defined data. Data used from processing must activate the AC/DC and DC/DC power converters in the predefined sequence and parameters values are to be downloaded to the power converters. Contactors behind DC/DC converters (at DC bus side) allow the switching of DC voltage to prosumers when DC/DC converters are ready in the buck mode. Contactors before DC/DC converters allow the switching of DC voltage to the common DC bus when DC/DC converters are ready in the boost mode. The position and status data of prosumer bay devices are transferred to the RTU for signalling purposes, for example, which substation bays are currently online and exchanging energy with prosumers (offline bays are reported in error reports).

If it has been verified that protection functions and operation of power converters run according to the control algorithm in RTU, predefined control algorithms for the system can be tested. The tests are based on typical use cases.

6.1 Charge

Figure 4 presents an example of an action flow chart for a prosumer charging use case (operation) [31]. Table 1 specifies the abbreviations and parameters used in Figs. 4 and 5. The command for charging is initiated by the prosumer (EV or BESU user). Some EVs need to

follow the CHAdeMO protocol [32]. For EVs, the charging start signal is sent to the EV. If protection functions are fulfilled, AC contactors for AC/DC converters positioned in front of the common DC bus are closed. AC/DC converters will receive target output voltages and power values from the RTU and will be set to rectifier mode. DC/DC converters are operating in the buck or boost mode. The DC/DC converters will receive target secondary side output voltage and power values from the RTU. If the common DC bus voltage is in range by the AC/DC converter, contactors on the primary side of the DC/DC converters are closed. When the DC/DC converter output voltage is in range, the BESU's BMS is set to the charge mode. For EVs, the connector is locked and the isolation test is performed, also contactors of the secondary side of DC/DC converters are closed. At the beginning of the charging process the SOC level of prosumers will determine whether the charge is performed with a slow current value, constant maximum current value or with constant voltage. The choice of the charging mode will be adjusted in accordance with the battery SOC value. For EVs charging is stopped at the zero current signals or timeout from the EV side. Depending on the location of fault detection, fault events will immediately open the adjacent switching apparatus.

6.2 Discharge

Figure 5 presents an example of an action flow chart for a discharging use case (operation) [31]. The command for discharge initiates the function for the selection of a prosumer type (EV or BESU user). For EVs the connector is locked and the isolation test performed. Contactors of the secondary side of the DC/DC converters are closed, the DC/DC converters receive a target for the primary side output voltage and power values from the RTU. When the output voltages of DC/DC converters are in range, the contactors of the primary side of the DC/DC converter are closed. Active power is transferred to the common DC bus. AC contactors for AC/DC converters (that are installed before the common DC bus) are closed if energy flow is directed from DC bus to AC bus side.

AC/DC converters will be set to the inverter mode and the RTU determines the target output power value for the AC/DC converter. The AC/DC converter synchronizes with the common AC bus voltage and power is transferred to the common AC bus. The time of discharge of prosumers (EV, BESU) depends on the quantity of resources acquired from the substation to perform its service providing. Discharging of prosumers is stopped when the depth of discharge, maximum discharge current or temperature is exceeded or the SOC value drops below the value defined in the manufacturer specifications [33]. Switching apparatuses are opened and operation of power converters stopped according to the determined sequences (determined stop or fault detection).

Table 1: Abbreviations and parameters in figs. 4 and 5

START	program cycle start
Check. Comm	communication check function
Status.Comm	communication status data object
Status.Comm.Err	communication error status
Poll	function to poll data from the prosumer
Data	RTU internal database for process values
Protection	function for carrying out protection functions
Calculate Process Values	function for calculating process values
Data.Prot.AC_B_err	AC bus error data object
Data.Prot.DC_B_err	DC bus error data object
Data.Pros.Chrg	prosumer charge command data object
Data.Pros.DsChrg	prosumer discharge command data object
Wake BESU	BESU wakeup function
Sleeping P-conv. to stand-by	function for setting power converters currently in sleep mode to stand-by
Close AC contactor	AC contactor closing function
Write process data to conv.	function for writing process data to converters
Write DC/DC conv. val	function for writing DC/DC converter process values
Write AC/DC conv. val	function for writing AC/DC converter process values
Set AC/DC conv. To Rectifier m.	function for setting the AC/DC converter to operate in the rectifier mode
Set AC/DC conv. to Inverter m.	function for setting the AC/DC converter to operate in the inverter mode
Set DC/DC conv. to Buck m.	function for setting the DC/DC converter to operate in the buck mode
Set DC/DC conv. Boost m.	function for setting the DC/DC converter to operate in the boost mode
Data.Pros.DC_ PBus_U_OK	DC prosumer primary bus voltage status data object
Close DC/DC conv. prim. Cont.	function for closing the DC/DC converter primary side contactor

Data.Pros.DC_ SBus_U_OK	DC prosumer secondary bus voltage status data object
Data.Pros.DC/ DC_Rdy	prosumers DC/DC converter ready state status data object
Data.Pros.Cap_DisCh	prosumers DC/DC converters capacitors need for discharge status data object
Data.Proc.Synch_OK	AC/DC converter AC output in synchronization with the AC bus status data object
Close DC/DC conv. sec. cont.	function for closing the secondary contactor of the DC/DC converter
Open DC/DC contactors	function for opening the primary and secondary contactors of the DC/DC converter
D.chrg DC/DC conv. cap	function for discharging the DC/DC converter capacitors
Close AC/DC Conv. AC cont.	function for closing the AC contactor of the AC/DC converter
END	end of program cycle

7 Simulation of bidirectional energy exchange between prosumers and utility network

Before microgrid system integration tests, (typical) use cases are to be simulated (visualized in left part of Fig. 3). This is done before prototype, factory and field tests, which are carried out using real hardware (visualized in right part of Fig. 3). Computer simulations provide a first testing environment for different control algorithms, allow optimization of energetic parameter values and a selection of devices for protection and control functions. Figure 1 shows a distribution substation topology that is similar to the topology simulated using the MATLAB Simulink model (Fig. 6) [31]. The model consists of 24 kV utility network supply through an MV switchgear, a 250 kVA voltage transformer 24/0.4 kV and an LV switchgear, which interconnects consumers and prosumers. The LV switchgear is divided into a common AC bus and a common DC bus. In this paper the BESU, (including Li-Ion battery pack with the nominal voltage of 460 V DC) is considered as prosumer in the MATLAB Simulink model. Other prosumers are connected with the common DC bus through bidirectional DC/DC power converters DCDC1-DCDC3 (double-leg full bridge DC/DC power converter topology with galvanic isolation). Contactors are included in the bays before and after the bidirectional DC/DC power converters. The common DC bus is supplied through

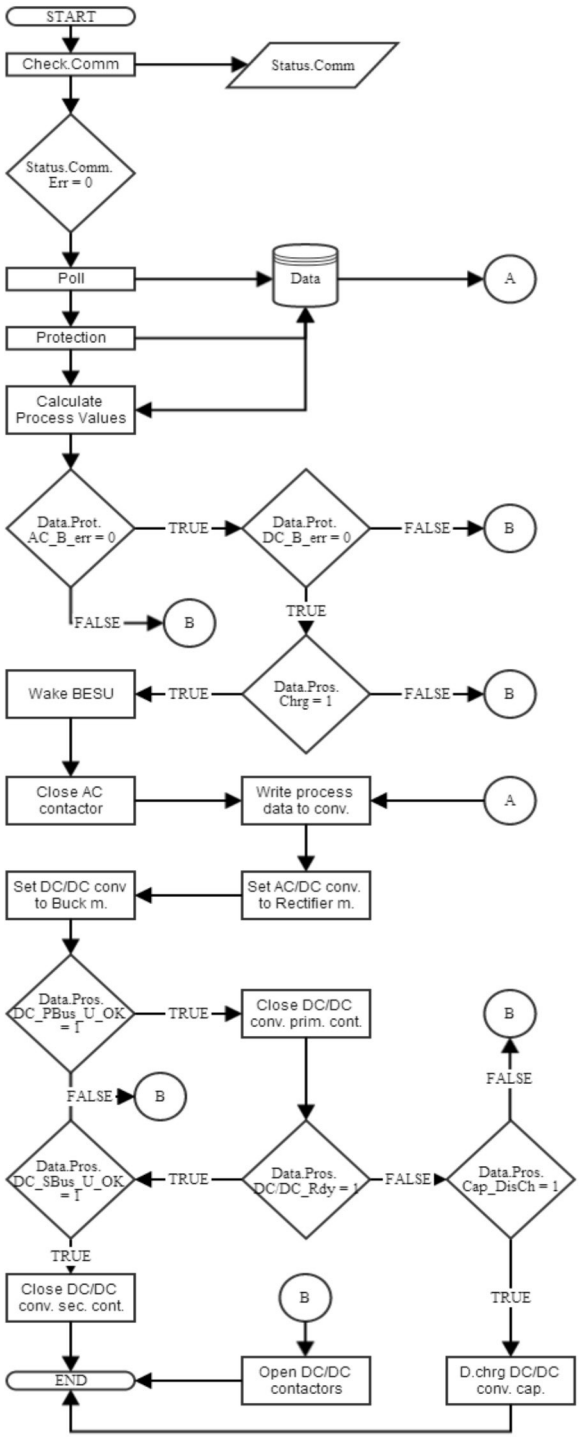

Figure 4: Action flow chart for the prosumer charging operation.

a 100 kVA bidirectional AC/DC power converter ACDC1 (three-level neutral point clamped voltage sourced converter). The common DC bus voltage can be adjusted up to 800 V DC. Consumers consuming 100 kVA to 200 kVA are connected with the common AC bus.

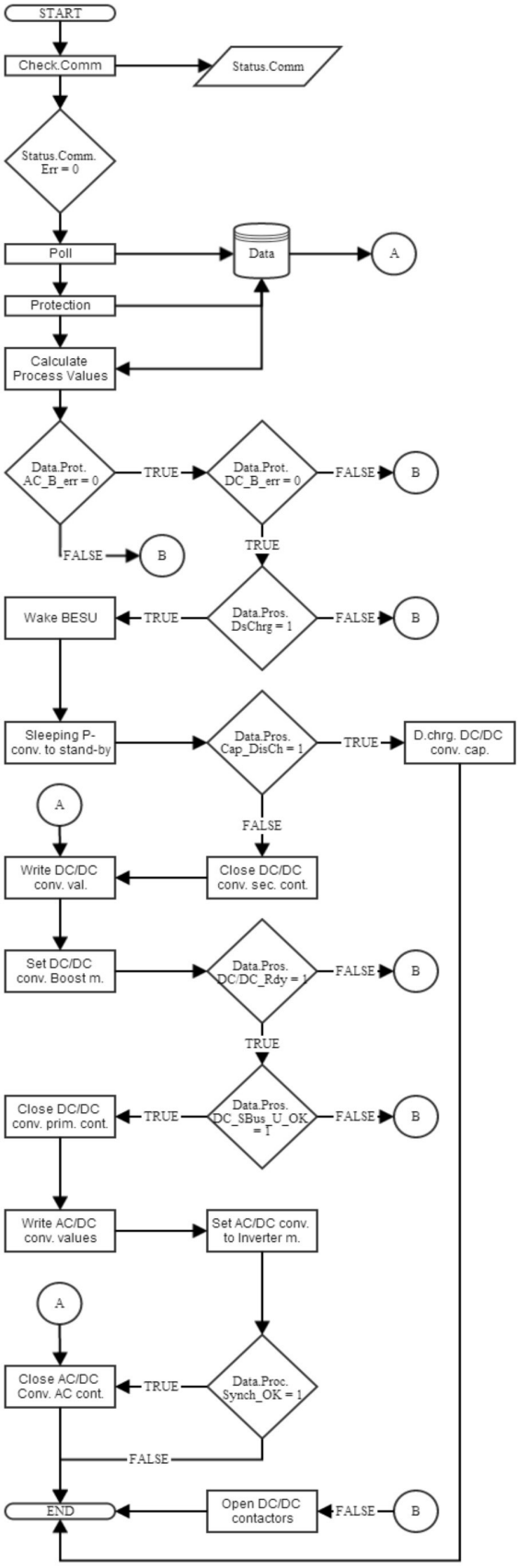

Figure 5: Action flow chart for the prosumer discharging operation.

The purpose of the MATLAB Simulink model is not to simulate a particular bidirectional AC/DC or DC/DC power converter, but rather to evaluate control functions (scripts) for bidirectional energy exchange and power distribution between the prosumers and the utility network. The simulated, tested (using the experimental prototype in laboratory) and verified control algorithms describing the control functions will be downloaded to a substation controller during the production of such a smart substation.

Some important systems integration tests can be carried out out much faster if user requirements, data models (systematized by developers) and the data values collected during simulations, laboratory experiments and factory tests are available also during site tests. Parallel recording and using the requirement information, simulation and verification data enable faster validation and approval of a microgrid project.

Independent certification (described in part 4 and visualized in lower right part in Fig. 3) can significantly reduce installation time spent at customer site.

During simulations, firstly, the consumer stage of a single prosumer (PROSUMER1) is examined. The bidirectional AC/DC converter ACDC1 operates in the rectifier mode and supplies the common DC bus.

The bidirectional DC/DC power converter DCDC1 in the prosumer bay operates in the buck mode. The results from the simulated model are presented in [31]. The charging current is ramped up smoothly and maintained at constant current level with the rising of the internal voltage of the Li-Ion battery pack.

Secondly, the producer stage of prosumers is examined. All three prosumers (PROSUMER1-PROSUMER3) provide support to the common DC bus. The support is utilized, for example for the peak shaving of the 200 kW load of the consumers for the utility network. The target goal is to reduce the load of the consumers for the utility network to 100 kW. The bidirectional DC/DC power converters DCDC1-DCDC3 operate in parallel in boost mode. The bidirectional AC/DC power converter ACDC1 operates in inverter mode and supplies the common AC bus. The results from the simulated model are presented in [31].

The simulations also help to define value ranges of resistances of possible electrical circuits. Internal resistance R_i of generating/consuming prosumers can be calculated and later tested from the voltage drop/rise ΔU during energy exchange with a constant current I. Designed BESU energy density can be predetermined by simulations. Effective gravimetrical energy density

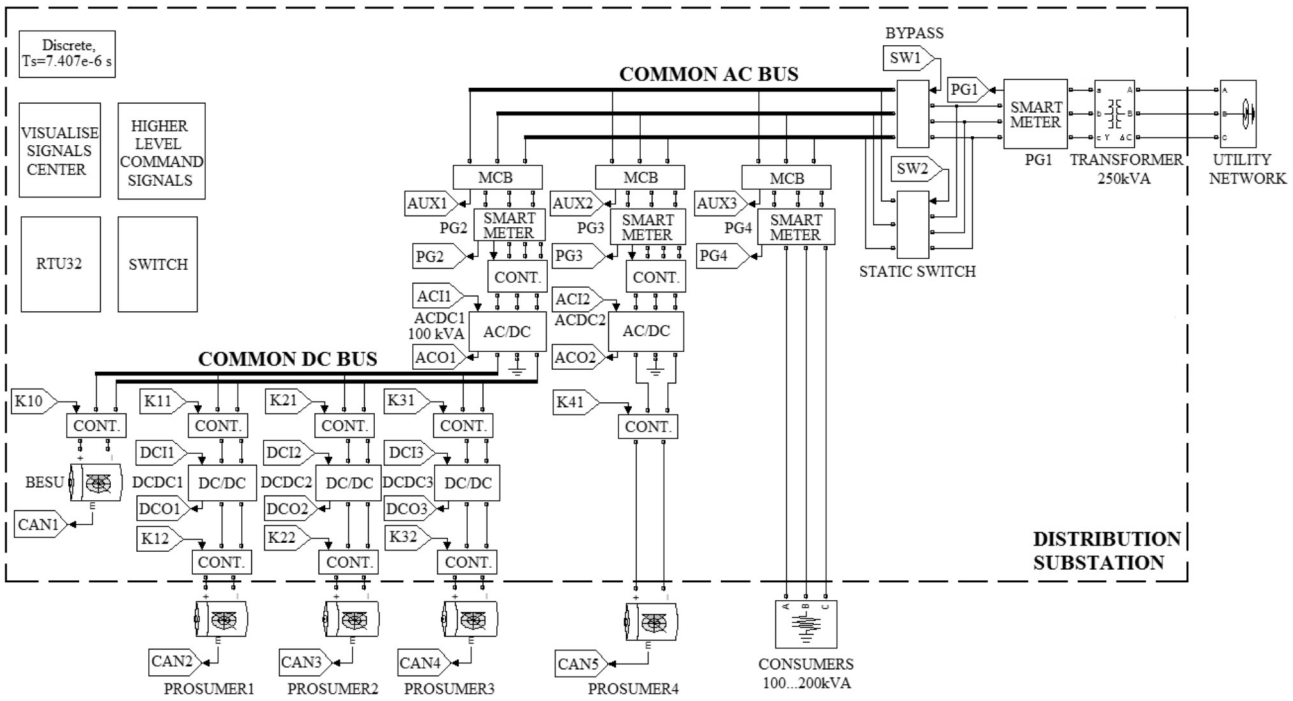

Figure 6: MATLAB Simulink model of a distribution substation with prosumers.

of modern lithium-ion batteries is about 100 to 265 Wh/kg.

Power density or the time rate of energy transfer is either measured gravimetrically (kW/kg) or volumetrically in kilowatt per litre (kW/l). Power density combines the energy density with the speed at which the energy can be delivered from one prosumer to the other or can be absorbed by a load. The actual speed is characterized by electric current.

The maximum power of an electric circuit is given by the formula $P_{max} = U^2/R_i$, where U is voltage applied and R_i, is the internal resistance of the circuit. The P_{max} specifies the power of a rectangular single maximum current peak of a given voltage. In reality the current peak is not rectangular caused by time constants and the voltage change is caused by the voltage drop. For supercapacitors the IEC 62391–2 standard therefore proposes a formula to calculate a more reality oriented effective power P_{eff} for power applications:

$$P_{eff} = \frac{1}{8} \times \frac{U^2}{R_i} \quad (1)$$

8 Test method for smart substations

Protection and control functions of smart substations have to be tested prior to exploitation. This includes running computer simulations, factory testing and onsite tests. Table 2 presents an example testing protocol for distribution substations that includes BESU and providing services for prosumers. For factory testing of the substation a variable voltage and frequency supply unit, load simulator and a test prosumers (e.g. EV and emulated PV plant that is based on programmable DC source) are required.

The testing method sequence begins with general routine tests for LV & MV switchgears, RTU and distribution substation. Settings and parameters need to be downloaded to devices and HMI.

Computer simulations verify the designed control algorithms and provide dynamic values (e.g. voltage and current values), which can be used for adjusting settings for protection and control devices. Differences between simplified computer simulations and practical test results should not exceed 10 %.

When the testing has been prepared, test supply unit can be connected and the behaviour of the system monitored.

Before connecting test loads, bays of the distribution substations must be prepared. This requires verification that protection functions run properly. Protection functions should be dependable (will operate when required), secure (will not operate when not required), selective (respond to events within their zones). Bay parameters have to be inserted and control of bays through RTU has to be verified. At the end of the prep-

aration of the bays the operation of power converters has to be tested.

After preparations and supply connection, test loads can be connected. Data retrieval and controllability of the prosumer's local controller (BMS) must be verified. Consumption and production stages (e.g. charging and discharging of the test EV) can be then tested for test prosumers and BESU.

IEEE 1547.1 type (design) tests are included in Table 2. The temperature stability test verifies that interconnection equipment maintains measurement accuracy of parameters over its specified temperature range. Abnormal voltage and frequency test verify that the system ceases to energize the area electric power system (EPS) in abnormal conditions. The synchronization test demonstrates that interconnection equipment will accurately and reliably synchronize to the area EPS. Interconnection integrity tests include verification for protection from electromagnetic interference (EMI), surge withstand performance and dielectric tests on the paralleling device. DC injection test verifies that the system complies with the DC current injection limit. Function tests include means to determine that the system ceases to energize the area EPS in unintentional island condition and loss of phase. Reconnect time test verifies the functionality of the reconnect timer in trip event. Harmonic tests measure individual current harmonics and total demand distortion (TDD).

IEEE 1547.1 production test verifies the operability of every unit of the interconnection equipment manufactured for customer use. Commissioning tests (onsite tests) are conducted after the interconnection system is installed and is ready for operation. Flicker tests are site dependent.

Onsite testing is vital prior to exploitation to verify that all the protection and control functions run properly. Specific functions like peak shaving, frequency droop control, reactive power compensation and intentional islanding can be monitored and test results protocolled. Time response to unintentional islanding should be 2 s according to IEEE 1547 requirement. During onsite testing the remote controllability of the distribution substation for the utility network can be verified. Some functions of the distribution substation have to be monitored over a longer period of time. These functions include ambient temperature tests to verify how much the prosumers and BESU can actually support in the production stage at different ambient temperatures (e.g. in winter and summer periods). The data can be used for accurate forecasting. The operations of data storing and scheduling functions must be verified.

Table 2: Testing protocol for distribution substation

No.	Description of test sequence	Status
	Factory tests	
1.	**Preparation for testing**	
1.1.	Routine tests for LV & MV switchgears and distribution substation	
1.2.	RTU testing (data retrieval, control of outputs)	
1.3.	Computer simulations for protection and control settings	
1.4.	Download of parameters and settings to power converters and smart meters	
1.5.	HMI set-up	
2.	**Connection of test sources and communications**	
2.1.	Supply connection	
2.2.	Monitoring of supply values (e.g. voltage, frequency)	
2.3.	Communication set-up and data flow	
3.	**Preparation of bays**	
3.1.	Protection ensured, interlocking of bays	
3.2.	Nominal, max. and min. values inserted for bays	
3.3.	RTU connection sequences (e.g. operation of contactors)	
3.4.	Activation of AC/DC and DC/DC power converters	
3.5.	Control response and data retrieval of AC/DC and DC/DC power converters	
4.	**Connection of test loads and BESU**	
4.1.	Data retrieval and controllability of prosumer controller (BMS)	
4.2.	Execution of example charging test sequence	
4.3.	Report from charging sequence (protection status, control functions, power quality)	
4.4.	Execution of example discharging test sequence	
4.5.	Report from discharging sequence (protection status, control functions, power quality, voltage rise, time responses)	
4.6.	DC input mismatch wiring test	
4.7.	First full charge of BESU	
4.8.	BESU functions testing (charge, discharge)	
5.	**IEEE 1547.1 type (design) factory tests**	
5.1.	Temperature stability	
5.2.	Responses to abnormal voltage	
5.3.	Responses to abnormal frequency	
5.4.	Synchronization in production stage	

5.5.	Interconnection integrity	
5.6.	DC injection	
5.7.	Unintentional islanding	
5.8.	Ceases to energize functionality and loss of phase (simulated fault sequences, emergency stop sequence)	
5.9.	Reconnect time and sequence	
5.10.	Harmonics	
6.	**Onsite (Field) testing of complete system behaviour**	
6.1.	Download of parameters and settings of the end user to devices	
6.2.	Peak shaving functional test	
6.3.	Frequency droop control in production stages	
6.4.	VAR management (reactive power compensation)	
6.5.	Power conditioning (PQ) and harmonic suppression	
6.6.	Intentional islanding and resynchronization	
6.7.	Power balancing in islanding mode	
6.8.	Blackstart management	
6.9.	Flicker test (site dependent)	
6.10.	Network communications (control from utility network)	
6.11.	Utility network supply accordance to EN 50160	
6.12.	Ventilation verification for heat extraction	
6.13.	Data storage (metering) and access through cloud applications	
6.14.	Scheduling tests	
6.15.	Ambient temperature tests (production stages of the prosumers and BESU)	
7.	**Conclusions**	
7.1.	Compliance with different international standards (EN 50160, IEC 61000, IEEE 1547.1 etc)	
7.2.	Remarks and limitations	
	Verification	

Table 3 presents an example of a generalized test report of the testing protocol for distribution substations. Different parameters have to be monitored and protocolled at consumption stage and production stage of the prosumers and also during different ancillary functions. The measurement values can be divided into three main categories: prosumer side, common DC bus side and utility network side.

Table 3: Test report with measured values

No.	Description of measurements	Value
	Field testing	
1.	**Prosumer DC side and BESU measurements both for consumption and production**	
1.1.	DC side voltage (start, end)	
1.2.	DC side current (max., average)	
1.3.	SOC values (start., end)	
1.4.	Active power (max., average)	
1.5.	Transferred energy (kWh)	
1.6.	Temperature of prosumer elements and DC/DC power converters (max., average)	
1.7.	Efficiency of DC/DC conversion	
1.8.	Specific energy (gravimetric mE, volumetric VE)	
1.9.	Specific power (gravimetric mP, volumetric VP)	
1.10.	Ambient temperature	
1.11.	Duration of full test and cycle times (e.g. constant current, constant voltage). Sampling rates.	
2.	**Common DC bus measurements during consumption or production of energy by prosumers**	
2.1.	Common DC bus voltage (max., min., average)	
2.2.	Common DC bus voltage unbalance (max., min., average)	
	Field testing	
2.3.	Common DC bus current (max., average)	
2.4.	Temperature of AC/DC power converters (max., average)	
2.5.	Efficiency of AC/DC conversion	
2.6.	Active power (max., average)	
2.7.	Transferred energy (kWh)	
3.	**Utility side measurements during consumption or production of energy by prosumers**	
3.1.	AC voltage (max., min., average, unbalance)	
3.2.	AC current (max., average)	
3.3.	AC frequency (max., min., average)	
3.4.	Active power, Reactive power, Apparent power (max., average)	
3.5.	Power factor (max., average)	
3.6.	Transferred energy (kWh)	
3.7.	Harmonic distortion (THDU, THDI, TDDI) with 1 to N activated prosumers at DC or AC side	
3.8.	Voltage flicker	
3.9.	Total efficiency of energy conversions	

3.10.	Duration times to load/production reduction: 25%, 50%, 75%	
3.11.	Inrush max. current and duration	
3.12.	Isolation monitoring and leakage currents	
4.	**Additional utility side measurements during production of energy by prosumers**	
4.1.	Max. continuous output power	
4.2.	DC current injection	
5.	**Functional test reports**	
5.1.	Clearing time to abnormal voltage (<U, >U)	
5.2.	Clearing time to abnormal frequency (<f, >f)	
5.3.	Clearing time unintentional islanding	
5.4.	Clearing time to simulated faults	
5.5.	Duration time for recovery (from abnormal area EPS values to nominal values)	
5.6.	Duration time for recovery (fault trip clearance)	
5.7.	Duration time to intentional islanding	
5.8.	Duration time to resynchronization	
5.9.	Duration time to blackstart	
5.10.	Duration time to peak shaving (target value, duration time and reference signal tracking error)	
5.11.	Ramp rate to active power production	
5.12.	Active power reduction gradient in frequency regulation	
5.13.	Duration time for VAR Management (target value, duration time, reference signal tracking error)	
5.14.	Duration time for harmonic suppression (target harmonic content, duration time and reference signal tracking error)	
5.15.	BESU roundtrip efficiency	
5.16.	BESU scheduling execution	
5.17.	Standby losses	

The key measured parameters in the test report are the efficiency values of the power converters, overall energy conversion efficiency and maximum continuous output power of the prosumers.

Other important parameters are the stress values for prosumers (current, temperature), power quality measurements at the utility network side (accordance to IEC 61000), clearing times and duration times of different IEEE 1547.1 determined functions and ancillary tasks. From the measured parameters energy density and power density values can be calculated for prosumers and BESU.

9 Configurable values for prosumers

While the main parameters of bays are defined in the designing phase, some of the bay parameters and ancillary services can be adjustable for the prosumers. Table 4 presents an example configurable value list for the bays of the distribution substation, which can be adjusted through HMI. These parameters include nominal, maximum and minimum values of different prosumer side parameters, price and scheduling options when to consume or produce (charge or discharge). Maximum values cannot exceed the limits of the selected devices. Minimum values, in most cases, are limited due to economic reasons or capabilities of the devices. Positions 1.1-1.7 in Table 4 can be inserted and simulated in the MATLAB simulation environment.

Functional settings include different ancillary tasks, threshold values, time delays, time synchronization, BESU side preferences, event/history logging and status reporting/reading. Time delays should provide ride-through for low/high voltage and frequency values.

Table 4: Configurable values for prosumers

No.	Description of values	Value
1.	Prosumer parameter values	
1.1.	Nominal/min/max voltage	
1.2.	Nominal/min/max current	
1.3.	Nominal/min/max charging power	
1.4.	Nominal/min/max discharging power	
1.5.	Maximum capacity (e.g. Ah)	
1.6.	Capability selection for bay: V2G	
1.7.	Maximum DOD (%)	
1.8.	Nominal/min/max temperature	
1.9.	Nominal/min/max prices for charging	
1.10.	Nominal/min/max prices for discharging	
1.11.	Scheduling preferences for prosumers	
2.	Functional settings	
2.1.	Peak shaving option activation	
2.2.	PQ preferences (VAR management or harmonic suppression)	
2.3.	Target cos φ	
2.4.	Individual harmonic compensation list	
2.5.	Load balancing activation	
2.6.	Non-islanding voltage and frequency range	
2.7.	Time delays for ride-through of abnormal conditions	
2.8.	Response times to abnormal conditions	
2.9.	Time synchronization	

2.10.	Scheduling preferences for BESU management	
2.11.	Event/history logging	
2.12.	Status reporting/reading	

10 Future studies

Tallinn University of Technology currently develops a smart substation development methodology and constructing an experimental microgrid that enables us to study energy flows and data communication. Parts of the smart substation development methodology that are not covered in this paper need future studies. The basic functions and operation modes (including protection algorithms) such as energy transmission from the power grid to the energy storing system, EV battery charging, balancing power loads and other functions have to be developed, tested and analysed. The simulated management and control algorithms have to be fine-tuned and will be transferred to the substation RTU (Fig. 7). Data will be collected for further analysis using an iConcur Axiom software. Primary goals are to analyse the quality of energy flow, energy efficiency and harmonic levels during EV charging through the microgrid, electromagnetic compatibility related issues and to improve and apply the testing methodology. The analysis will indicate needs for modifications to be made in the microgrid structure to optimize and improve the overall efficiency and power factor levels in the system to ensure the quality of electricity in accordance with international standards.

Figure 7: View of an experimental setup with RTU devices for microgrid experimentations.

Practical applications will show possible drawback areas in the communication between the devices, which will then have to be solved with different control algorithms. Future studies will focus on development of a prototype microgrid and on possibilities to transfer energy to the common AC bus or to the power grid with synchronization related issues. Results from microgrid experiments will be published in future papers. Advice and warnings of issues to be aware of for smooth and accurate testing will be provided.

11 Conclusions

This paper has reviewed a developed testing method for distribution substations which form a microgrid with prosumers. Topology of the substations has been presented with an integrated AC and DC bus. The topology enables providing simultaneously services to prosumers, consumers and utility network. It has been proven through simulations that an integrated AC and DC bus (Fig. 1) can be the main topology solution for integrating prosumers with different nominal voltages to electric power grids. Simulation results have verified that bidirectional energy exchange between the utility network and prosumers can be used for peak shaving of utility networks loads.

In microgrid applications a distribution substation can be viewed as an energy router and it is the function of the substation's main controller in the higher level to determine when to utilize prosumers for ancillary services.

This paper has presented a new testing protocol for distribution substations. The testing procedure includes running computer simulations, prototype tests (using laboratory tests for substation and microgrid integration), factory tests and onsite tests.

Before constructing a real life substation, a smaller stand has to be constructed and examined. An experimental microgrid is being constructed at Tallinn University of Technology. Experiments with the microgrid will give vital data about charging/discharging algorithms and communication between the devices. These studies will enable us to construct a larger real life substation capable of supplying power to several prosumers that will be part of a microgrid or even a viable module of Smart Grid solutions.

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A Compact 3.1–5 GHz RC Feedback Low-Noise Amplifier Employing a Gain Enhancement Technique

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Abstract: A low-noise amplifier (LNA) with main cascode amplifying stage utilizing a current-reuse transconductance-boosting technique is presented in this paper. This topology increases the effective transconductance, g_m, of the input transistor and prevents a large voltage drop across the load resistor, thus reducing power consumption. The feedback topology made of source follower connected in series with a parallel RC network improves input impedance matching at high frequencies, while a gate peaking inductor inside the feedback loop enhances the amplifier bandwidth. The proposed LNA is implemented in UMC 0.18 µm CMOS technology for a lower band of the ultra-wideband spectrum from 3.1 to 5 GHz. Measurements show a power gain (S_{21}) of 9.7±0.45 dB with the 3-dB band from 1.1 to 5.57 GHz. The input return loss (S_{11}) is below −10 dB from 1 to 5 GHz, while the output return loss (S_{22}) is less than −10 dB and the reverse isolation (S_{12}) is better than –25.5 dB across the whole measured bandwidth, 1–7 GHz. The input-referred 1-dB compression point (P_{1dB}) is −10.5 dBm at 3 GHz. The average noise figure (NF) obtained by post-layout simulations is 4.24 dB, with a minimum value of 4.05 dB at 4.92 GHz. By using only one inductor in the proposed design, the total chip area is greatly reduced to 0.913 mm^2. The LNA core area occupies 0.353 mm^2 and consumes 9.97 mW from a 1.8 V supply.

Keywords: CMOS technology, radio frequency integrated circuits (RFIC), ultra-wideband (UWB), low-noise amplifier (LNA), current-reuse technique, resistive-feedback technique

Kompakten 3.1–5 GHz RC povratni nizkošumni ojačevalnik s tehniko povečanja ojačenja

Izvleček: V članku je predstavljen nizkošumni ojačevalnik (LNA) z glavno kaskodno ojačevalno stopnjo s tehniko ponovne uporabe toka in povečanja transkonduktance. Uporabljena topologija povečuje efektivno transkonduktanco g_m vhodnega tranzistorja in preprečuje velike napetostne padce na bremenskem uporu, kar zmanjšuje porabo. Povratna topologija serijsko povezanega sledilnega vira s paralelnim RC omrežjem izboljšuje ujemanje vhodne impedance pri visokih frekvencah, pri čemer gladilna tuljava vrat v povratni zanki povečuje pasovno širino ojačevalnika. Predlagan LNA je izveden v UMC 0.18µm CMOS tehnologiji za spodnji del ultra širokega pasu spektra od 3.1 do 5 GHz. Meritve izkazujejo donos moči (S_{21}) 9.7±0.45 dB s pasovno širino 3-dB med 1.1 in 5.57 GHz. Povratne vhodne izgube (S_{11}) so pod -10 dB med 1 in 5 GHz, izhodne povratne izgube (S_{22}) so pod -10 dB, povratna izolativnost (S_{12}) boljša od -25.5 dB preko celotne pasovne širine 1-7 GHz. Vhodno naslovljena 1 dB točka kompresije (P_{1dB}) je -10.5 dBm pri 3 GHz. Povprečna slika šuma simulacije po postavitivi je 4.24 dB. Pri uporabi le ene tuljave se površina čipa močno zmanjša na 0.913 mm^2. Jedro LNA zaseda 0.353 mm^2 in porabi 9.97 mW pri 1.8 V napajanju.

Ključne besede: CMOS tehnologija, radio frekvenčna integrirana vezja (RFIC), ultra širok pas (UWB), nizkošumni ojačevalnik (LNA), uporovna povratna tehnika

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1 Introduction

In 2002, the Federal Communication Commission (FCC) set up rules and regulations for ultra-wideband (UWB) technology and allocated 7.5 GHz of unlicensed spectrum (from 3.1 to 10.6 GHz) for commercial deployment [1]. An UWB signal is defined as any signal that occupies bandwidth greater than 500 MHz or whose fractional bandwidth exceeds 0.20, where fractional bandwidth is defined as the −10 dB bandwidth occupied by the signal divided by its center frequency.

There are two different UWB approaches: multi-band (MB) UWB technology and impulse radio (IR) UWB. The former uses frequency hopping with orthogonal frequency division multiplexing (OFDM), where the available bandwidth of 7.5 GHz is divided into 528 MHz subbands, while the latter uses a series of short duration impulses, typically on the nanoseconds scale, utilizing a very wide bandwidth in the frequency domain. In MB-OFDM four band groups are defined, such as group A (3.1–4.9 GHz), B (4.9–6 GHz), C (6–8.1 GHz), and D (8.1–10.6 GHz), while the IR-UWB can be subcategorized in Time-Hopping (TH) UWB and Direct-Sequence (DS) UWB. The band of DS-UWB is separated into two parts, low band (3.1–4.9 GHz) and high band (6.2–9.7 GHz) [2].

The applications of UWB technology cover two areas: high data rate transmissions over short distances and low data rate communications with ranging and localization capabilities. The high data rate mode of UWB is related to short range wireless personal area networks (WPANs), while in the low data rate mode, UWB systems allow a new range of applications, including medical, military, vehicular radar, and security systems [3]. Generally, UWB shows a number of advantages compared to conventional narrowband applications, such as good time domain resolution, immunity to multipath propagation and interference, and potentially low complexity and low cost [4].

The FCC did not specify the type of the signal and modulation scheme of the UWB signal, but only the spectrum mask that the signal needs to meet with the emission limit restrictions issued for each specific UWB application. Power levels set for wireless communications are very low, i.e. −41.3 dBm/MHz, which allows coexistence of UWB and other conventional narrowband systems. Due to these strict power emission rules for the transmitter and the additional transmission path losses, the received signal power is typically three orders of magnitude smaller than that of narrowband systems [5]. This makes UWB receiver front-end design very challenging, particularly the design of the UWB low-noise amplifier. Since the overall noise figure of the receiver is mainly determined by the NF and the gain of the LNA, a sufficient gain and a low noise figure within a defined bandwidth is obligatory. In addition, to reduce return losses, adequate input and output matching is needed. All these requirements have to be fulfilled with low power consumption and within a wide bandwidth. Furthermore, for an UWB LNA designed for OFDM systems good power linearity is required to suppress adjacent channel interference. In the UWB impulse radio systems with more complex forms of modulation, e.g. BPSK (Binary Phase Shift Keying), good phase linearity (i.e., small group delay variation) is required instead. The frequency component of the transmitted signal should experience the same delay amount to be recovered properly.

With increasing interest on commercial wideband integrated systems such as radars and wireless UWB and optical receivers, there is a demand for wideband complementary metal-oxide semiconductor (CMOS) amplifiers in the front-end section of such systems, since the CMOS process is more attractive and promising technology for high level of integration and system-on-chip (SOC) applications. CMOS devices offer the advantages of high f_T and f_{max} as well as superior linearity and lower voltage operation, due to lower threshold voltages (CMOS V_T vs. bipolar V_{BE}). Bipolar junction transistors (BJT) offer the advantages of noise performance and an improved transconductance. The 1/f noise due to carrier trapping-detrapping at interface states and thermal noise due to gate and channel resistances are both significantly higher in CMOS than in BJTs. To reduce noise, very large CMOS devices and large operating current are often required. While the ultimate selection is based on system specifications, the noted differences between performance and economics also need to be considered.

Often, the LNA's performance depends on on-chip inductors, which occupy a large area, making these topologies less attractive for low-cost application [6–8]. In this paper, an LNA with one main amplifying stage implemented in low cost UMC 0.18 μm CMOS technology is presented. Since inductors available in the used technology consume very large chip area, it was necessary to decrease their number. Only one peaking inductor inside the feedback loop is used in proposed design for enhancement of the amplifier's bandwidth. Furthermore, to overcome this technology constraint and to meet the requirements for LNA figures of merit (FoMs) some additional design techniques need to be used. To achieve wideband input impedance matching, the feedback network enhanced with a shunt capacitor. High gain in the whole operating band and low power consumption are obtained by merging resistive-feedback and current-reuse transconductance-

boosting technique. Section 2 presents basic UWB LNA topologies, Section 3 gives insight into the feedback technique and Section 4 explains the proposed circuit topology. Section 5 reports the measurement results along with the simulation data. Section 6 contains the conclusions based on the performance of the proposed LNA.

2 UWB LNA design techniques

There are several wideband amplifier architectures that can be used in CMOS technology.

The general block diagram of a distributed amplifier consists of transmission lines (realized using either coplanar waveguides or cascaded LC circuits) and gain stages distributed along them, that determine the overall gain of the amplifier. With this architecture impedance matching over a wide bandwidth can be achieved, but losses in the transmission lines limit the maximum gain. Moreover, it usually employs many spiral inductors that occupy a large chip area and consume considerable amounts of power, which makes them unsuitable for low power and low cost applications [6], [7].

The overall input reactance of the common-source amplifier with inductive source degeneration and extended with a multi section filter structure as input impedance matching circuit, is in resonance over the whole band. With this architecture low power consumption can be achieved, although noise performance will be degraded due to the LC network loss. In addition, a large silicon area is required, occupied by numerous integrated inductors [8].

The common-gate stage provides wideband input impedance matching with less design complexity and small area occupancy, for proper device size selection and bias current of the input transistor. However, the main disadvantage of this amplifier is a high noise figure as its relatively low transconductance value cannot provide low noise and high gain in the whole frequency range. To overcome this issue and discrepancy between input and noise matching, noise cancelling methods need to be used. Also, this type of amplifier is usually combined with an additional amplifying stage, which provides high-frequency gain and enhances the bandwidth [9].

Another area-saving solution is a common-source amplifier with resistive shunt-feedback technique [10]. With this approach wideband input impedance matching and flat gain can be obtained, though it is challenging to achieve very wide bandwidth with low NF. Moreover, due to strong dependence of voltage gain on the amplifying transistor's transconductance a large amount of current is required to achieve high gain. Therefore, to increase the transconductance and to reduce the power consumption a novel LNA circuit design needs to be proposed.

3 Theory of resistive-feedback LNA

The basic feedback topology, where the feedback resistor R_F, is implemented directly between the gate and drain of the input transistor, at low frequencies and under the impedance matched condition, exhibits a voltage gain of:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{R_L - g_{m1}R_L R_F}{R_L + R_F} \approx -\frac{R_F}{Z_{in}} \tag{1}$$

where R_L is the load resistor, g_{m1} is transconductance of the input transistor M_1, and Z_{in} is the input impedance of this circuit given by:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{R_L + R_F}{1 + g_{m1}R_L} \approx \frac{R_L + R_F}{g_{m1}R_L} = \frac{1}{g_{m1}}\left(1 + \frac{R_F}{R_L}\right) \tag{2}$$

For a common-source (CS) amplifier employing the feedback resistor connected through a source follower, the voltage gain at low frequencies under the impedance matched condition is:

$$A_v = \frac{v_{out}}{v_{in}} = -g_{m1}R_L \approx -\frac{R_F}{Z_{in}} \tag{3}$$

and the input impedance is given by:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1 + g_{m2}R_F}{g_{m2}\left(1 + g_{m1}R_L\right)} \approx \frac{1}{g_{m1}}\frac{R_F}{R_L} \tag{4}$$

where g_{m2} represents the source follower's transconductance.

By using A_v and Z_{in} approximate equations (1)–(4), for a voltage gain of 10 dB and input impedance matched to 50 Ω, the feedback resistor R_F in both cases is 158 Ω. If g_{m1} = 50 mS, it follows from (2) and (4) that R_L is 105 Ω and 63 Ω, respectively. By inserting a source follower in the feedback, the value of R_L is reduced by 40% compared to the topology without it. The reduction in R_L leads to a wider amplifier bandwidth, since a decrease

in load resistance shifts the main pole, determined by the RC time constant of the CS output node, to higher frequencies. An additional benefit of a smaller load resistor value is the decrease in voltage drop across R_L, which allows proper biasing of the amplifying transistor with high current demands.

4 UWB LNA circuit design

The schematic of the proposed UWB LNA is shown in Fig.1. The input stage consists of an amplifying stage based on a cascode configuration, which is enhanced with resistive feedback connected through a source follower, and current-reuse M_3–M_5 block. The output stage is realized as a simple source follower that provides a broadband output impedance of 50 Ω for measurement purposes.

Input impedance matching is obtained by using a shunt feedback circuit, composed of source follower and R_FC_F parallel network. By using the source follower in the feedback path, the value of resistor R_L is decreased, resulting in a smaller voltage drop across the load resistor and in an enhancement of frequency band. However, to achieve a high gain, the drain current of transistor M_1 should be large, which makes the voltage drop still significant. By adding transistor M_3 these two effects, R_L voltage drop and enhancement of the M_1 transconductance, are less coupled. In this way, the current through cascode transistor M_2 is only part of the current of transistor M_1 and the voltage drop across resistor R_L is reduced, thus improving the voltage headroom. The amount of current through transistor M_3 is controlled by the current mirror, formed by transistors M_4 and M_5. By connecting the gate of M_3 to that of M_1, the total transconductance of the input stage g_m is enhanced and is given as the sum of the transconductances of transistors M_1 (NMOS) and M_3 (PMOS). Consequently, the gain of the LNA increases. Additionally, by inserting the current-reuse stage, current through R_L decreases, thus the value of the resistor R_L could be increased, which leads to higher amplifier gain and reduced noise figure value, but smaller bandwidth.

For the basic feedback topology, the input impedance, given by (4), increases at high frequencies as the amplifier gain, $g_{m1}R_L$, drops due to parasitic capacitances. By adding a capacitor C_F in parallel with feedback resistor R_F, the feedback impedance at high frequencies is reduced, the input impedance remains constant with frequency change and the broadband impedance matching is improved.

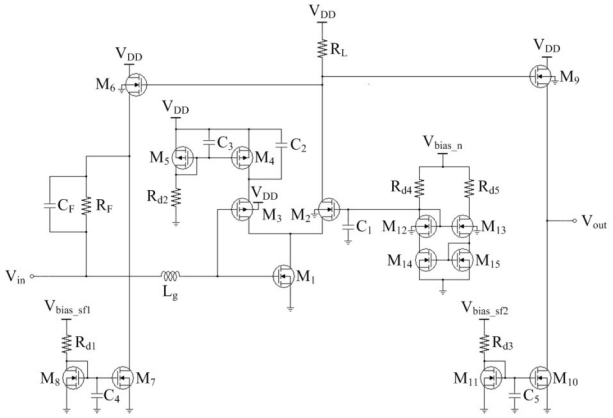


Figure 1: Proposed 3.1–5 GHz CMOS UWB LNA.

The total input node capacitance is approximately the sum of the capacitance C_F and the gate capacitances of transistors M_1 and M_3. Inductor L_g is connected to the gate of M_1 and M_3, as shown in Fig. 1, to resonate with these capacitances. Simulations show, that by increasing the inductance of L_g, gain peaking becomes more significant and the amplifier bandwidth enhances up to some value above which the bandwidth starts to decrease. The voltage signal at the gate of M_1 (M_3), and hence the transconductance, increases approaching the resonant frequency causing gain peaking. Additional increase in the gain value is obtained by adding a large value capacitor C_2 at the source of transistor M_3. With increasing frequency, the source impedance seen by transistor M_3 decreases. This results in a larger transconductance g_{m3} value and consequently a higher LNA gain.

Three simple bias circuits composed of resistors R_{dn} (n = 1, 2, 3) and transistors M_n (n = 4, 5, 7, 8, 10, 11) as current mirrors are used. To decrease the overall power consumption (P_D), the width of the bias transistors is a small fraction of that of the corresponding amplifying transistors. A bias circuit using a modified Wilson current mirror sets the bias level for transistor M_2, as shown in Fig. 1. Supply voltages V_{bias_sf1}, V_{bias_sf2}, and V_{bias_n} are driven externally to provide an additional degree of measurement freedom and ability to compensate for process and voltage variations. In a final design these voltages can be set to V_{DD}, which in turn decreases the number of pads and reduces chip area.

In further analysis, influences of cascode stage and output buffer stage are omitted for simplicity.

4.1 Bandwidth enhancement with inductor L_g

For the LNA employing the RC feedback network connected through a source follower, without inductor L_g at the gate of the input transistor M_1, the voltage gain of the amplifying stage is derived as:

$$A_{v1} \approx -\frac{(g_{m1}+g_{m3})R_L\left(1+j\omega\frac{C_{gs6}}{g_{m6}}\right)}{1+j\omega\frac{C_{gs6}}{g_{m6}}\left(1+\frac{R_L}{Z_F}\right)}\cdot\frac{1}{1+j\omega(C_{gs1}+C_{gs3})R_g} \tag{5}$$

where R_g is the gate resistance, and Z_F is the impedance determined by the capacitor C_F in parallel with the feedback resistor R_F, given by:

$$Z_F = \frac{R_F}{1+j\omega C_F R_F} \tag{6}$$

If the value of resistor R_F is of the same order as the value of resistor R_L, A_{v1} can be simplified as:

$$A_{v1} \approx -\frac{(g_{m1}+g_{m3})R_L}{1+j\omega(C_{gs1}+C_{gs3})R_g} = -(g_{m1}+g_{m3})R_L \tag{7}$$

After inductor L_g is placed inside the feedback loop, the first amplifying stage voltage gain can be approximated as:

$$A_{v1} \approx -\frac{(g_{m1}+g_{m3})R_L\left(1+j\omega\frac{C_{gs6}}{g_{m6}}\right)}{1+j\omega\frac{C_{gs6}}{g_{m6}}\left(1+\frac{R_L}{Z_F}\right)}\cdot$$

$$\cdot\frac{1}{1+j\omega(C_{gs1}+C_{gs3})R_g-\omega^2(C_{gs1}+C_{gs3})L_g} \tag{8}$$

and after simplifying:

$$A_{v1} \approx -\frac{(g_{m1}+g_{m3})R_L}{(C_{gs1}+C_{gs3})L_g\left[\frac{1}{(C_{gs1}+C_{gs3})L_g}+j\omega\frac{R_g}{L_g}-\omega^2\right]} \tag{9}$$

It can be seen that by inserting inductor L_g at the gate of transistor M_1, the second-order circuit is obtained. From (9) follows that the frequency of the pair of complex-conjugate poles is ω_0: $1/\sqrt{L_g(C_{gs1}+C_{gs3})}$ and the Q-factor of a complex-conjugate pole pair is equal to:

$$Q = \sqrt{\frac{L_g}{R_g{}^2(C_{gs1}+C_{gs3})}} \tag{10}$$

It can be seen that with this inductor L_g addition potential bandwidth enhancement can be achieved. Fig. 2 shows the simulation results of the voltage gain for different values of the gate inductor L_g. For an increasing value of inductor L_g, the bandwidth of the amplifier is improved. However, based on the expression for bandwidth in terms of Q-factor and resonant frequency, $BW=\omega_0/Q$, exceeding a certain value of the inductance, the peaking becomes severe and the bandwidth starts to degrade.

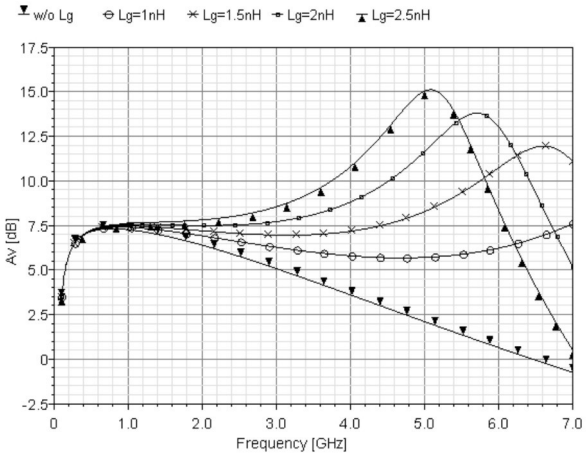


Figure 2: Simulation results of the voltage gain for different L_g values.

For the proposed design the optimum inductance value of L_g is found to be 2.3 nH. With this value the LNA covers the frequency band from 3.1 to 5 GHz with 1.82 dB variation in S_{21} parameter.

4.2 Influence of capacitor C_F on impedance matching

The input impedance of the proposed LNA is given by:

$$Z_{in} = \frac{Z_F+\frac{1+j\omega C_{gs6}R_L}{g_{m6}+j\omega C_{gs6}}}{1+|A_{v1}|} \,||\, \frac{1-\omega^2(C_{gs1}+C_{gs3})L_g}{j\omega(C_{gs1}+C_{gs3})} \tag{11}$$

where C_{gs6} and g_{m6} are the gate-source capacitance and the transconductance of the source-follower transistor M_6, respectively. The real and imaginary parts of the input impedance are examined, as shown in Figs. 3 and 4.

From Figs. 3 and 4 it can be seen that the input impedance is determined by two equivalent subcircuits. At low frequencies the parallel resonant circuit with resonant frequency around 4 GHz shows the dominant effect on overall LNA impedance. Below this frequency the parallel RLC circuit has inductive and beyond it capacitive character, as shown in Fig. 4. From the expression for the output impedance of the source follower, given by

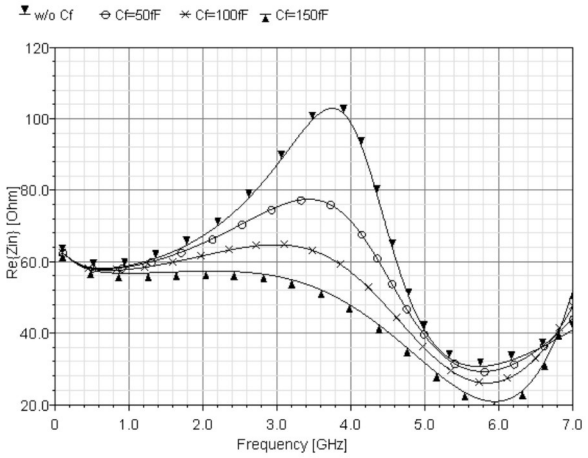


Figure 3: Simulation results of the real part of the input impedance for different C_F values.

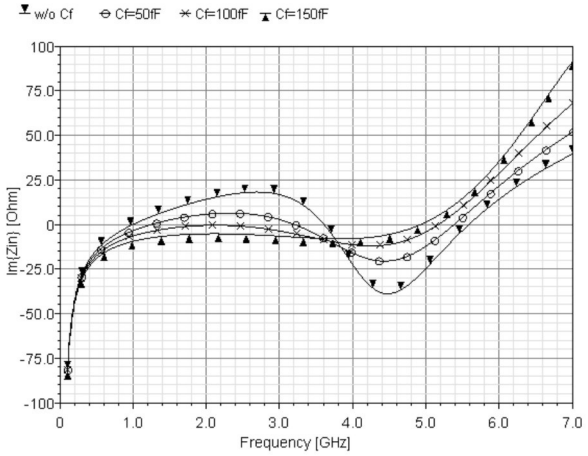


Figure 4: Simulation results of the imaginary part of the input impedance for different C_F values.

$$Z_{out} = \frac{1 + j\omega R_L C_{gs6}}{g_{m6} + j\omega C_{gs6}} \tag{12}$$

it can be observed that by increasing the frequency, for $1/g_{m6} < R_L$, the impedance of the source follower shows inductive behavior. Based on the method presented in [11], this impedance can be represented as a parallel LR_1 circuit connected in series with a resistor R_2. The component values can be obtained as:

$$L = \frac{j\omega C_{gs6}}{g_{m6}}\left(R_L - \frac{1}{g_{m6}}\right) \tag{13}$$

$$R_1 = R_L - \frac{1}{g_{m6}} \tag{14}$$

$$R_2 = \frac{1}{g_{m6}} \tag{15}$$

This inductance forms a parallel resonant circuit together with the input capacitances C_{gs1} and C_{gs3}. By adding capacitor C_F in parallel to feedback resistor R_F, the real component of the feedback impedance is reduced, given by (6), and comes closer to ideal 50 Ω, as shown in Fig. 3. In addition based on (11) the capacitive effect is increased by A_{v1}, which decreases the imaginary part closer to zero and, therefore, improve input impedance matching. Consequently, the parameter S_{11} is improved, as shown in Fig. 5.

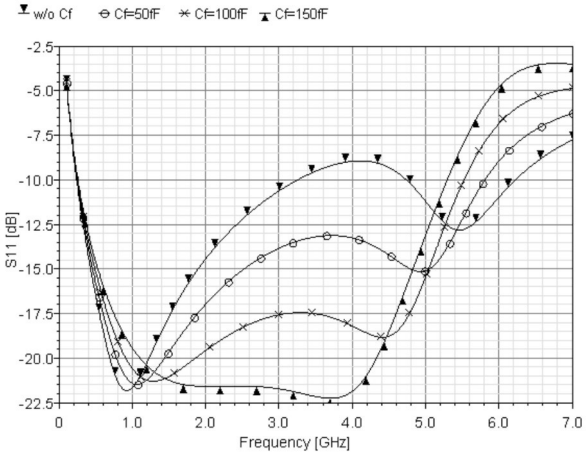


Figure 5: Simulation results of the S_{11} parameter for different C_F values.

At high frequencies the influence of the serial resonant circuit, formed by inductor L_g and input capacitances of transistors M_1 and M_3, can be seen with resonant frequency at 6 GHz given by:

$$\omega_0 = \frac{1}{\sqrt{L_g\left(C_{gs1} + C_{gs3}\right)}} \tag{16}$$

The influence of capacitor C_F can be seen from Figs. 3 and 4, as a reduction of the input impedance real part. As before, capacitor C_F decreases the feedback impedance for increasing frequency. The imaginary part of the input impedance will start to increase with frequency as a result of inductive behaviour.

4.3 Noise analysis

At high frequencies the noise is white, but at low frequencies the power spectral density is inversely proportional to the frequency.

For transistors in the proposed LNA, it was found that the flicker noise (1/f) corner frequency is around 10 MHz, which is in accordance with the data given in Process Design Kit (PDK) for 0.18 µm CMOS technology. From simulation it was found that 1/f noise of the LNA

is mainly contributed by the input amplifying NMOS transistor M_1 (14.55 %), with the W_1 = 105 µm.

The noise factors of the most important thermal noise sources of the LNA, under input impedance matched condition and not considering a gain boosting stage, are derived as:

$$F_{RL} \approx \frac{1}{g_{m1}{}^2 R_L R_S} \tag{17}$$

$$F_{RF} \approx \frac{R_F}{g_{m1}{}^2 R_L{}^2 R_S} \tag{18}$$

$$F_{M1} \approx \frac{1}{g_{m1} R_S} \frac{\gamma_1}{\alpha_1} \tag{19}$$

$$F_{M6} \approx \frac{1}{g_{m6} R_S} \left(\frac{1}{g_{m1} R_L} \right)^2 \frac{\gamma_6}{\alpha_6} \tag{20}$$

where F_{RL}, F_{RF}, F_{M1}, and F_{M6} stand for the noise factors due to thermal noises of the load resistor R_L, the feedback resistor R_F, the amplifying transistor M_1, and the source follower transistor M_8, respectively. R_S is the input source resistance, γ is the MOSFET's thermal noise coefficient, and parameter α describes g_m/g_{d0} ratio, where g_{d0} is the drain-source conductance at zero V_{DS}. The total noise factor of the LNA is given as:

$$F = 1 + F_{RL} + F_{RF} + F_{M1} + F_{M6} \tag{21}$$

In the final LNA design, transistor M_3 is added to enhance transconductance of input transistor M_1, so lower value of noise factor can be achieved, as can be seen from (17)–(20). Consequently, a lower current flows through resistor R_L providing some additional increase of R_L for the same voltage headroom, but a smaller bandwidth. During the design procedure trade-offs among power consumption, BW, input impedance matching and NF are performed.

5 Measurement and simulation results

The proposed LNA circuit was designed and implemented in UMC 0.18 µm twin-well CMOS technology with supply voltage V_{DD} = 1.8 V.

Simulations were obtained by using Cadence Design System with Spectre device models for all components. Post-layout simulations were performed using Assura, Cadence parasitic extractions tool. Transistor models are realized as multi-finger structures with 0.18 µm fixed gate length. The information about transistor widths is presented is Table 1, while values of passive components used in the circuit are given in Table 2. The bulks of all NMOS/PMOS transistors are connected to adequate reference voltages (GND in case of NMOS, and V_{DD} in case of PMOS transistors), as shown in Fig. 1.

Table 1: Transistors widths (W), L = 0.18 µm.

Devices	$M_{1,4,9}$ [µm]	$M_{3,6}$ [µm]	$M_{2,10}$ [µm]	M_{15} [µm]	M_5 [µm]	$M_{7,8,11-14}$ [µm]
Design values	21 × 5	13 × 5	11 × 5	9 × 5	7 × 5	5 × 5

Table 2: Values of passive circuit components.

Devices	R_F [Ω]	R_L,R_{d4} [Ω]	$Rd_{1,3}$ [Ω]	R_{d2} [kΩ]	R_{d5} [Ω]	L_g [nH]	C_1 [pF]	$C_{2,3}$ [pF]	$C_{4,5}$ [pF]	C_F [fF]
Design values	219.8	136.6	719.7	3	317.7	2.3	4.9	4	2	119.9

A die microphotograph of the proposed LNA circuit is shown in Fig. 6. Using only one inductor in the LNA design, the chip area is greatly reduced and measures 1.251×0.729 mm^2. The active area, which excludes the pads, is approximately 0.919×0.384 mm^2.

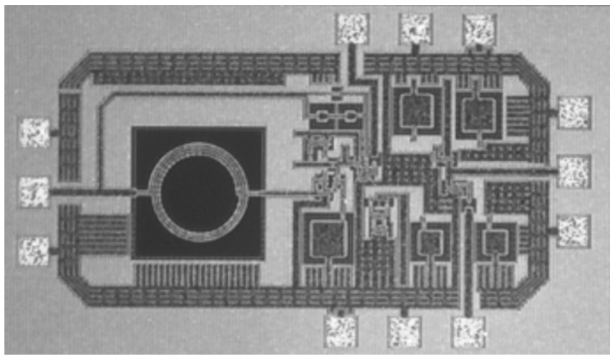
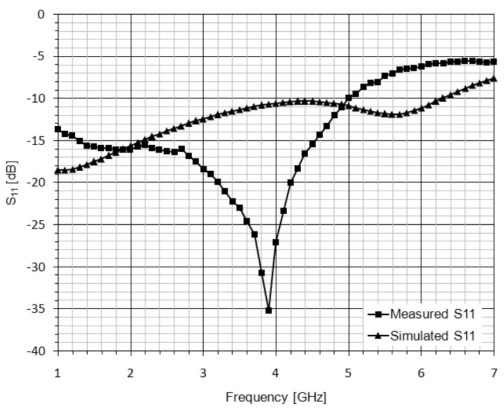


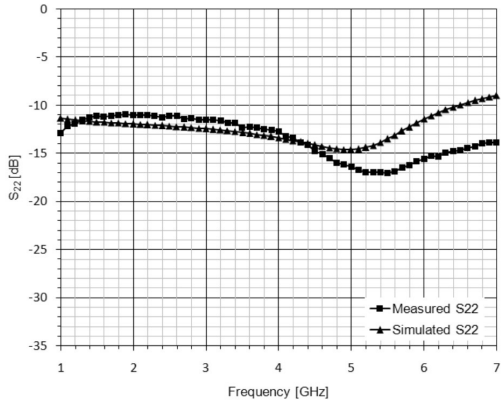
Figure 6: Die microphotograph of the designed LNA.

On-wafer probing under a 1.8 V supply voltage was performed to characterize the circuit performance of the LNA. The S-parameters were measured by using a Rohde & Schwarz ZVM Vector Network Analyzer. Fig. 7 shows the measured S_{11}, S_{22}, S_{21}, and S_{12} parameters along with the simulation results. The measured input return loss (S_{11}) is better than –10 dB for the frequency range from 1 to 5 GHz. The discrepancy between simulation and test results is mainly attributed to the additional parasitic effects. Over the entire frequency band of interest (3.1–5 GHz), the measured output return loss (S_{22}) and the measured isolation (S_{12}) remain below –11.52 dB and –36.07 dB, respectively. Fig. 7(c) shows the measured power gain (S_{21}) versus frequency. The LNA achieves a high S_{21} of 9.7±0.45 dB over the 3.1–5 GHz band, and a 3-dB bandwidth from 1.11 to 5.57 GHz.

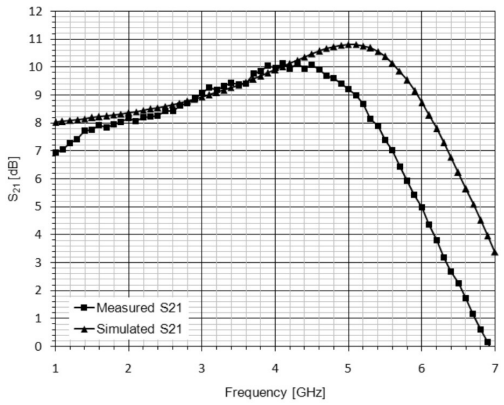
(a)



(b)



(c)



(d)

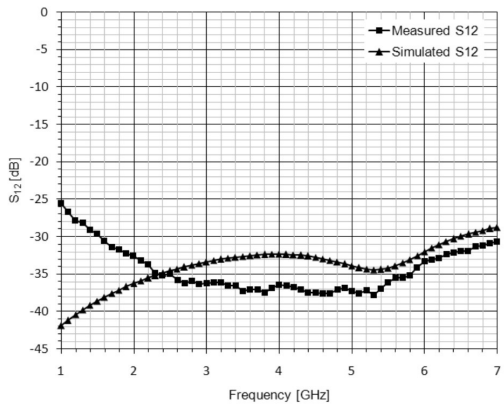


Figure 7: Measurement and simulation results: (a) S_{11} parameter, (b) S_{22} parameter, (c) S_{21} parameter, (d) S_{12} parameter.

The post-layout simulation result for the noise figure (*NF*) is shown in Fig. 8. It can be seen that the parameter value varies from 4.42 dB at 3.1 GHz to 4.06 dB at 5 GHz, with a minimum of 4.05 dB at 4.92 GHz.

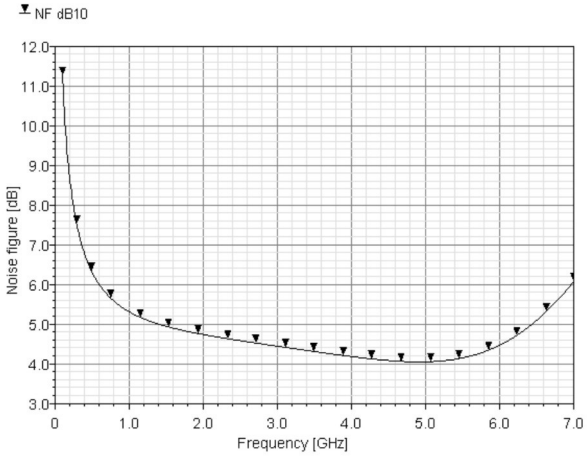


Figure 8: Post-layout simulation results: Noise figure (*NF*).

The linearity of the proposed LNA was characterized measuring the 1-dB compression point using a Rohde& Schwarz Spectrum Analyzer FSP 30. An Hewlett Packard Network Analyzer 8753E, was used as an input source for varying the input power from –35 to 0 dBm. Due to its limitation in the frequency range, the linearity was measured only at 3 GHz. Measurements were performed for five LNA samples, and the results range from –9.5 to –11.5 dBm. Average result is plotted in Fig. 9.

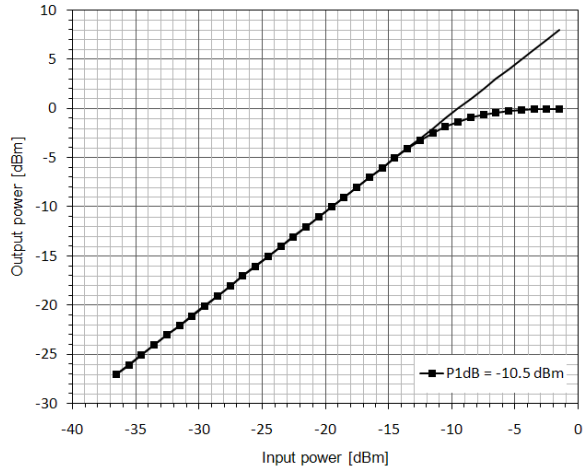


Figure 9: Measured results: 1-dB compression point.

The use of source-follower as LNA output stage leads to amplifier linearity degradation. The additional source follower in the feedback circuit further decreases 1-dB compression point. Despite this, proposed LNA meets the linearity requirements for the UWB amplifier design and shows better linearity performance than other re-

ported amplifiers designed in 0.18 µm technologies, which in addition use more complex circuit designs and increase costs.

A common measure for phase linearity is the group delay, defined as the derivation of the transfer function S_{21} phase. The measured maximum group delay variation of the proposed LNA is ±34.59 ps across the 3.1–5 GHz band. By definition, a group delay variation of less than ±10 % of the bit period over the specified bandwidth is required to limit the generation of data dependent jitter [12]. This corresponds to maximum possible bit period of 345.9 s, i.e. bit rate up to 2.89 Gb/s. Thus, proposed LNA shows good phase linearity.

The stability of the LNA is determined by the Rollett stability factor K and the auxiliary stability factor B_1. Minimum values of K and B_1 are 3.66 and 0.94, respectively, hence unconditional stability requirements, given by $K > 1$ and $B_1 > 0$ [13], are satisfied. In addition, the geometric stability factors of an amplifier are calculated. The µ (Mu) and µ' (Mu-prime) factors are so called load stability factor and source stability factor, respectively. A two port network is unconditionally stable if $\mu > 1$ or $\mu' > 1$ [14], which means that with any load presented to the input or to the output of the device, the circuit will not become unstable. Furthermore, it can be said that larger values of µ and µ' imply greater stability. The stability factors of the proposed UWB LNA are calculated for all frequencies where the device is able to provide a gain larger that unity. The measured results are shown in Fig. 10. It can be noticed, that LNA circuit is stable for all frequencies, up to 10 GHz.

The current consumption of the LNA was measured with a Keithley 2000 Multimeter. The LNA's total core current is 5.54 mA. Taking the currents drawn by the bias circuits and the output buffer into consideration, the LNA dissipates a total of 28.54 mW from a 1.8 V supply.

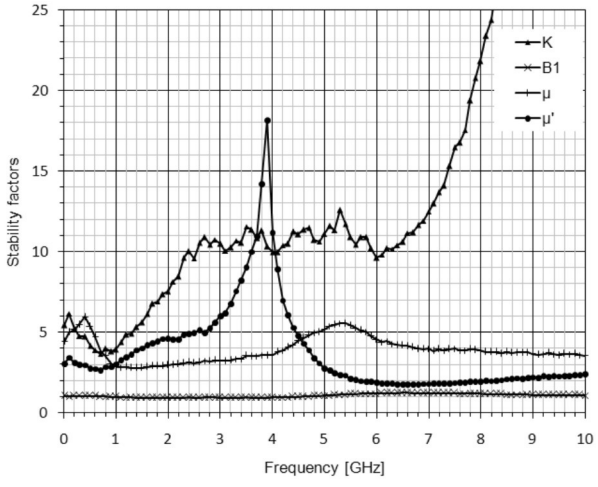


Figure 10: Measured results: Stability factors.

To provide a certain level of controllability, separated pins are added in the design for supply voltages V_{bias_sf1}, V_{bias_sf2}, and V_{bias_n}. By decreasing these voltages (they are nominally set to 1.8 V), S-parameters and noise figure characteristics are affected. Post-layout simulation results are shown in Figs. 11–13.

By changing the voltage V_{bias_sf1} from 1.8 to 1 V, the gate-source voltage of transistor M_7, V_{gs7}, and consequently the gate-source voltage of transistor M_1, V_{gs1}, is increased. A higher V_{gs1} voltage results in a larger transconductance value g_{m1} and leads to S_{21} increase. Additionally, due to higher output resistance the low-frequency gain increases and peaking is less pronounced. According to the (4), input impedance value decreases and diverges from 50 Ω, which leads to a higher parameter S_{11} value. Furthermore, voltage V_{bias_sf1} variations result in minor S_{22} change and slight increase of *NF*. Decrease in voltage V_{bias_n} value influences transistor M_2 biasing point, thus decreasing the overall gain of the amplifier up to 1dB. As a result, input impedance value, given by (11), increases and S_{11} parameter degrades. The voltage V_{bias_sf2} variations affect output impedance matching. For V_{bias_sf2} = 1 V, the output resistances of transistors M_9 and M_{10} increase. As a result, the LNA's output impedance changes, which leads to S_{22}, and consequently, S_{21} decrease.

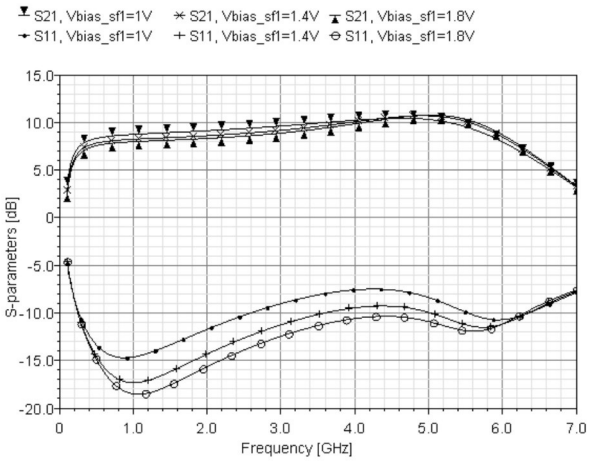


Figure 11: Post-layout simulation results: Simulated S_{11} and S_{21} when varying V_{bias_sf1} in the range from 1 to 1.8 V, with 0.4 V step.

Table 3 summarizes the measurement results of the proposed LNA compared to the FoMs of the recently published works. The design presented in this paper shows low variation of gain and noise in the 3.1–5 GHz band. As the main drawback of selected low cost 0.18 µm technology are inductors, that occupy a large area, by reducing their number to one, the chip area is greatly reduced and comparable to the area occupied by other designs, implemented in different 0.18 µm technolo-

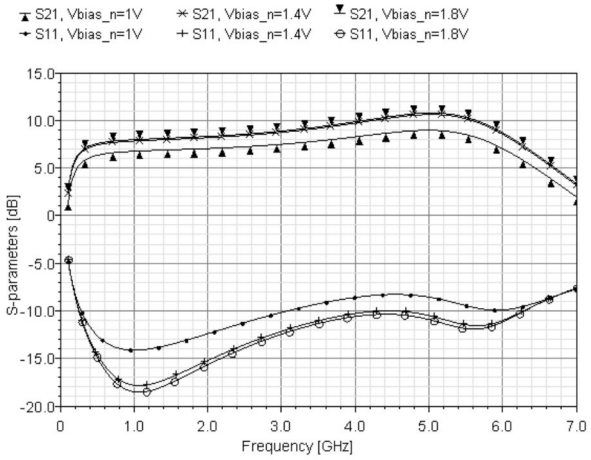


Figure 12: Post-layout simulation results: Simulated S_{11} and S_{21} when varying V_{bias_n} in the range from 1 to 1.8 V, with 0.4 V step.

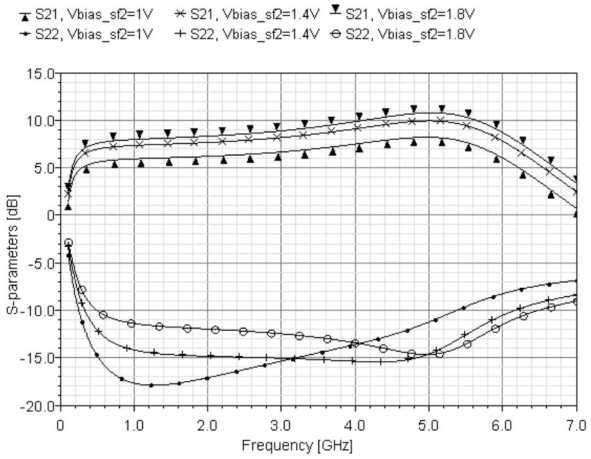


Figure 13: Post-layout simulation results: Simulated S_{22} and S_{21} when varying V_{bias_sf2} in the range from 1 to 1.8 V, with 0.4 V step.

gies. For example, the LNA topologies presented in [15] and [16] use four inductors, in [17] and [18] three, and in [19] five. Consequently, the small number of inductors in LNA design reduces the degrees of freedom, so additional techniques need to be used to meet requirements for all LNA FoMs. From Table 3 follows that parameters achieved in the presented paper are comparable to the results given by other authors, making the proposed architecture suitable for UWB wireless applications.

6 Conclusion

The proposed LNA is designed for lower UWB band from 3.1 to 5 GHz. By utilizing only one inductor placed inside the feedback loop, a compact layout design in low cost UMC 0.18 µm CMOS technology is presented. Therefore, proposed design is comparable with the other reported designs implemented in different technologies. To meet other LNA requirements different techniques are used. The amplifier employs the feedback resistor connected through a source follower, which leads to a wider operating frequency range and improved voltage headroom of the amplifier. In addition, the drain current of the cascode transistor is reduced by adding the PMOS transistor to form a current-reuse topology with the amplifying transistor. Consequently, the effective transconductance is enhanced, leading to high gain values. By adding feedback capacitor in parallel to feedback resistor, the input impedance is kept constant with frequency and wideband input impedance matching is obtained. The simulation and measurement results show low gain and noise variations in the band of interest, from 3.1 to 5 GHz, while satisfying the input and the output matching conditions and the power consumption requirements. Good power and phase linearity performances make the proposed LNA suitable for both OFDM and UWB impulse radio system applications.

Acknowledgments

This work was supported in part by the Ministry of Education, Science and Technological Development, Republic of Serbia (the project contract numbers III-43008 and TR-32016).

Table 3: Performance comparison of LNAs implemented in 0.18 µm technologies.

Ref.	BW [GHz]	S_{21} [dB]	S_{11} [dB]	S_{22} [dB]	NF [dB]	P_{1dB} [dBm]	P_D [mA@V]	Die area [mm^2]
/15/	3–5	12.7±0.4	<–13	<–10	3.2–5.5	–11.7	9.6*@ 1.8	0.7
/16/	3–4.8	13.5±1.5	<–10	/	3.5–6.8	–18	3.7*@ 0.9–1.8	0.76
/17/	3–7	10±1.5	<–11	<–11	3.5–4	/	5 @ 1.8	0.59
/18/	0.6–6.2	10.1±1.5	<–21	<–22	5.3–5.8	–13	5.6 @ 1.5	0.8
/19/	2–6	12.5±0.5	<–10	/	3–3.7	/	8.3 @ 1.8	0.98
This work	3.1–5	9.7±0.4	<–10	<–11	4–4.4**	–9.5	5.5*@ 1.8	0.91

*LNA core **simulated

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Printed Circular Patch Wideband Antenna for Wireless Communication

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Abstract: This letter presents a new wideband, printed, microstrip-fed, circular patch antenna for multifunctional wireless communication applications. The commercially available CST Microwave Studio software package, which is based on finite difference time-domain (FDTD) analyses, has been adopted in this study. The experimentally determined impedance bandwidths are 2.2 GHz (1.75 GHz to 4 GHz) and 750 MHz (4.15GHz to 4.90 GHz), which cover the GSM-1800, GSM-1900, UMTS, Bluetooth (2400-2800) MHz, WLAN (2400-2485) MHz, WiMAX (2500-2690) MHz and WiMAX (3400-3600) MHz frequency bands. The experimental measurements taken using the proposed antenna are in good agreement with the computational results.

Keywords: Antenna, circular patch, wideband, wireless communication.

Tiskana krožna krpičasta širokopasovna antena za brezvrvične zveze

Izvleček: Članek opisuje novo širokopasovno tiskano mikro trakasto krpično krožno anteno za večfunkcijsko brezžično komunikacijo. Za potrebe študije je bilo predelano komercialno programsko orodje CST Microwave Studio, ki temelji na metodi končnih razlik v časovnem prostoru. Eksperimentalno določene impedančne pasovne širine so 2.2 GHz (od 1.75 GHz do 4 GHz) in 750 MHz (od 4.15GHz do 4.90 GHz), ki pokrivajo frekvenčne pasove GSM-1800, GSM-1900, UMTS, Bluetooth (2400-2800) MHz, WLAN (2400-2485) MHz, WiMAX (2500-2690) MHz in WiMAX (3400-3600) MHz. Eksperimentalni rezultati so v dobrem ujemanju s simulacijami.

Ključne besede: Antena, krožna krpičasta antena, široki pas, brezžična povezava

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1 Introduction

In recent years, microstrip-fed circular patch antennas have become popular in antenna researcher because of their numerous benefits such as cost effectiveness, wideband abilities, simple fabrication and improved performance. Moreover, Improvements in wireless communications have introduced tremendous demands in the antenna technology. .It's withal the paved the way for extensive utilization of mobile phones in modern society resulting in mounting concerns circumventing its inimical radiation [1-3]. Furthermore, this type of antenna satisfies the challenges of connectivity with both mobile and fixed devices with greater user experience and also overcomes the limitation of narrow impedance and axial ratio bandwidth.

Researchers have analysed various types of circular antennas for different operating frequencies [4-7]. Various techniques, such as the annular ring microstrip patch antenna using a prolonged ear [8], have been used to obtain the desired operating frequency. Moreover, to achieve wideband abilities, a number of additional techniques were studied. For example, a dual rectangular wire loop configuration above an infinite ground plane was designed in [9]; an L-probe patch antenna was proposed in [10]; a magneto-dielectric resonator antenna was proposed in [11] and electromagnetically coupled, two-layer substrate was used in [12].

Furthermore, by adding one or more parasitic elements, a wide bandwidth of up to 40% axial-ratio bandwidth was achieved in [13]. A fan-shaped, parasitic patch with

an annular-ring patch antenna was investigated in [14], where a bandwidth of 2.3% was achieved, and the effect of parasitic elements was investigated in [15-18].

A number of studies have been conducted on slot antennas as well [19-24], where CP antennas have achieved 4% to 25% axial-ratio bandwidths.

In this article, a new wideband, circular polarized, printed monopole antenna is proposed that can be operated in the GSM, UMTS, WLAN and WiMAX frequency bands with improved gains. The concept of adding a parasitic element and cutting slot are investigated and compared. The experimental results of the antenna exhibit continuous wide bands from 1.75 GHz to 4 GHz and from 4.15 GHz to 4.9 GHz.

2 Antenna geometry

The geometries of the proposed and fabricated antenna prototype are shown in Fig. 1 and Fig. 2, respectively. The length of the printed circuit board is Lg = 50 mm and the width is Wg = 62.9 mm. The antenna consists of two main parts: the circular patch with parasitic elements and the defected ground. The radius of the circular radiator is 12.5 mm. The width and length of the feed line are Wf and Lf, respectively, which has an input impedance of 50 Ω. A parasitic element is attached to the patch to change the surface current's path. The dimensions of the proposed antenna are shown in Table I.

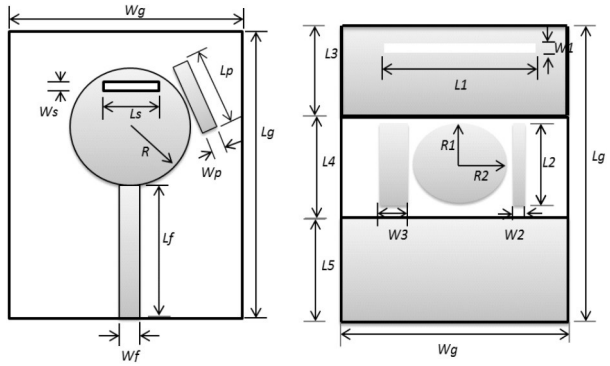
Table. 1: The proposed antenna specifications (in mm).

Parameters	Values (mm)	Parameters	Values (mm)
Wg	50.00	**L1**	28
Lg	62.9	**L2**	15
Lf	25.5	**W1**	1.06
Wf	2.89	**W2**	6.5
R	12.5	**L3**	15
Ls	12.3	**L4**	21.4
Ws	1.06	**R1**	10
Lp	14.5	**R2**	11
Wp	2.00		

3 Parametric studies

3.1 Effect of parasitic elements and slots

The best performances of the proposed antenna are obtained by adding different types of parasitic elements and cutting slots. Parasitic elements and cutting slots are added to change the current flow and attain better radiation profiles. The proposed antenna has been designed using optimally sized parasitic elements. Initially, analyses were performed with one conventional, circular patch microstrip monopole antenna. Several steps were subsequently followed. In the first step, a 15 mm × 3 mm copper element was added to the ground plane, which resulted in a smaller reflection coefficient. In the second step, a 15 mm × 6.5 mm copper element and an ellipse were added to the ground plane together with first element and analysed. In the third step, the 15 mm × 50 mm copper elements were added in the upper side of the ground plane, which resulted in improved results relative to the previous step. In the fourth step, a slot was cut from the upper portion of the ground. In the fifth step, a parasitic element was added to the patch, which resulted in improved results. Finally, a slot was cut from the patch, which resulted in



(a) (b)

Figure 1: Design layout of the proposed antenna: (a) Top View and (b) Bottom view.

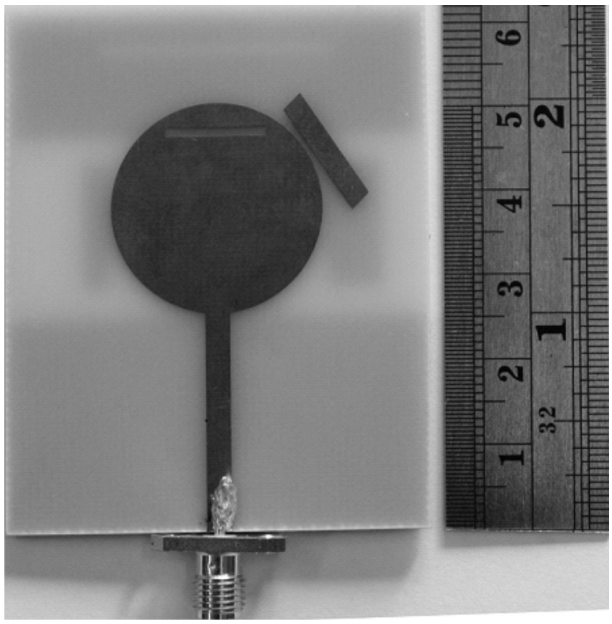


Figure 2: Photograph of the fabricated proposed antenna.

the desired results. The reflection coefficient values of the different slots are compared in Fig. 3.

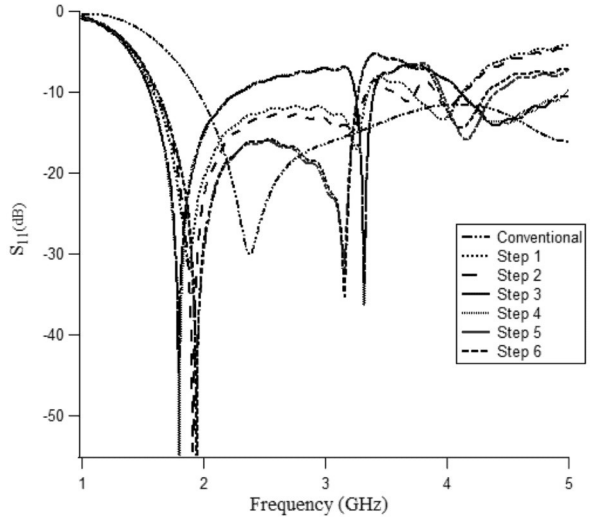


Figure 3: Effect on the reflection coefficient from adding parasitic elements and slotting.

3.2 Substrate Height

Fig. 4 shows the simulation result of the reflection coefficient of the proposed antenna for FR4 substrate thicknesses of 0.254 mm, 0.500 mm, 1 mm and 1.6 mm. From Fig. 4, it is clearly observed that the best performance of the proposed antenna was found using a thickness of 1.6 mm. Because the thicker substrate increases the radiated power and improve impedance bandwidth.

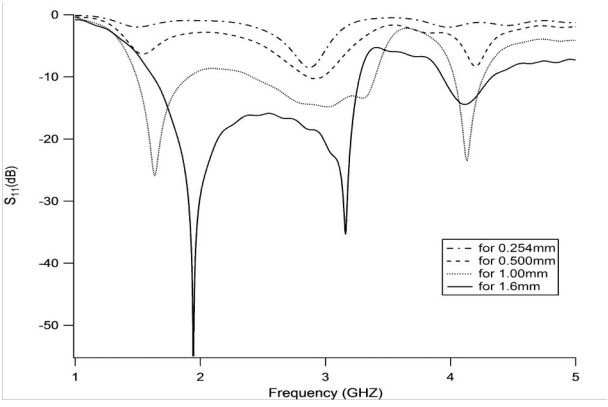


Figure 4: Reflection coefficient for different values of substrate thickness.

3.3 Different Substrates

The reflection coefficients of the antenna using different types of substrate materials are shown in Fig. 5. From Fig. 5, we see that the substrate material is an important parameter for the antenna design. The different materials properties are shown in Table II.

Table. 2: Material properties of different materials

Substrate Name	Permittivity	Loss Tangent	Substrate thickness
RT 5880	2.2	0.0015	1.6
RT 5870	2.33	0.0012	1.6
RT 6010	10.2	0.002	1.6
FR4	4.6	0.02	1.6
Bio plastic	15	0.002	1.6

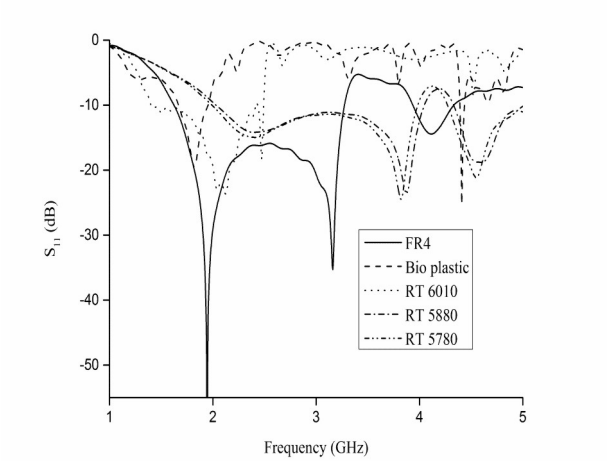


Figure 5: Reflection coefficient for different types of substrates.

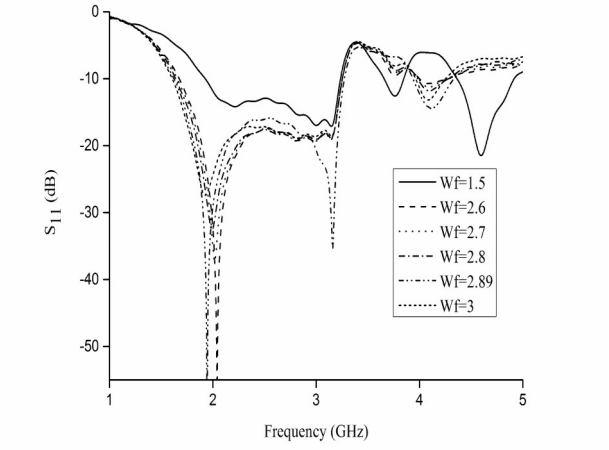


Figure 6: Reflection coefficient for different values of the feed line width

3.4 Feed Line Width

Fig. 6 shows the simulated reflection coefficient values of the proposed antenna for different feed line widths (Wf). The optimum value of Wf for the desired frequency band was determined to be 2.89 mm. which indicates that the input impedance matches smoothly at 2.89 mm feed line width.

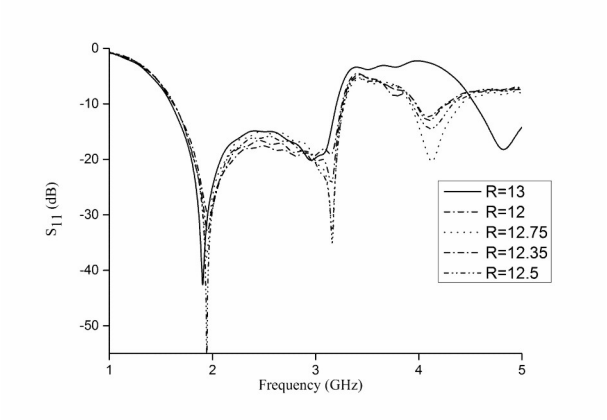


Figure 7: Reflection coefficient for different values of patch radius .

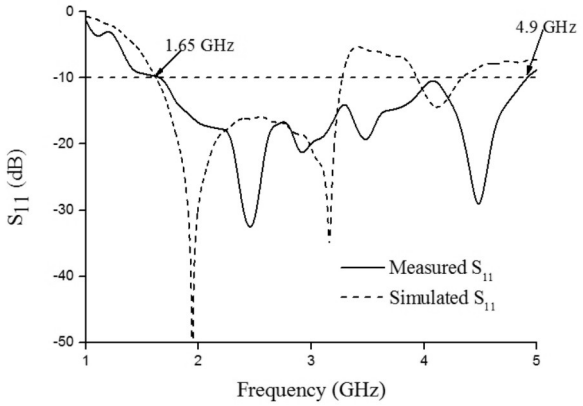


Figure 8: Simulated and measured reflection coefficient value of the proposed antenna.

3.5 Patch Radius

The optimized patch radius for the proposed antenna is 12.5 mm as seen in Fig. 7. The frequency band from 3.9 GHz to 4.5 GHz can be controlled by regulating the patch radius as seen in Fig. 7.

4 Results and discussions

The design and simulation of the proposed antenna have been performed using the commercially available CST Microwave Studio and High Frequency Structural Simulator (HFSS) software package. The prototype of the proposed antenna has been fabricated and measured. The reflection coefficient measurement has been performed using an Agilent TE8362C network analyzer. The simulated and the experimental reflection coefficients were compared as seen in Fig. 8. It is seen from Fig. 8 that the simulated peak resonant was achieved at 1.95 GHz and 3.16 GHz. Moreover, two wide bandwidths of 1.65 GHz and 550 MHz were seen from 1.62 GHZ to 4.45 GHz. In the experiment, two wide bandwidths of 2.2 GHz from 1.75 GHz to 4 GHz and 750 MHz from 4.15 GHz to 4.9 GHz were found. The surface current distribution was observed for different frequencies as seen in Fig. 9.

In addition, the simulated E-plane and H-plane radiation pattern at 1.8 GHz, 2.1 GHz, 2.4 GHz, 2.7 GHz, and 4.5 GHz are shown in Fig. 10. From Fig. 10, it is observed that the proposed antenna shows a directional radiation pattern for E-plane and H-plane radiation pattern. At higher frequency there are some distortion in the radiation pattern.The main reason of this distortion is the excitation of higher-order current mode.

The dimensions of the wideband wireless antenna to cover the GSM 1800, GSM 1900, GSM 2100, UMTS, Bluetooth (2400-2800 MHz), WLAN (2400-2485 MHz), WiMAX (2500-2690 MHz), and WiMAX (3400-3600 MHz) frequency bands are quiet larger. In [25], the authors achieved a wide bandwidth of 1.37 GHz from 1.04 to 2.41 GHz, and the antenna ground plane dimension was 300 mm × 300 mm. In [26], the authors presented a wideband, circularly polarized antenna; however, their antenna ground plane radius is larger than the proposed antenna, which is 150 mm. Conversely, the dimensions of the proposed antenna were 50 mm × 62.9 mm, which achieved a wide bandwidth of 2.2 GHz and 750 MHz from 1.75 GHz to 4 GHz and from 4.15 GHz to 4.9 GHz, respectively.

5 Conclusion

A simple, low-cost, wideband, circular patch microstrip-fed monopole antenna was presented. The presented antenna has a wide bandwidth of 2.2 GHz from 1.75 GHz to 4 GHz and 750 MHz from 4.15 GHz to 4.9 GHz, respectively. The proposed antenna can cover the GSM 1800, GSM 1900, UMTS, Bluetooth, WLAN and WiMAX frequency bands. In this study, it was observed that the proposed antenna can play an important role in current wireless communication systems.

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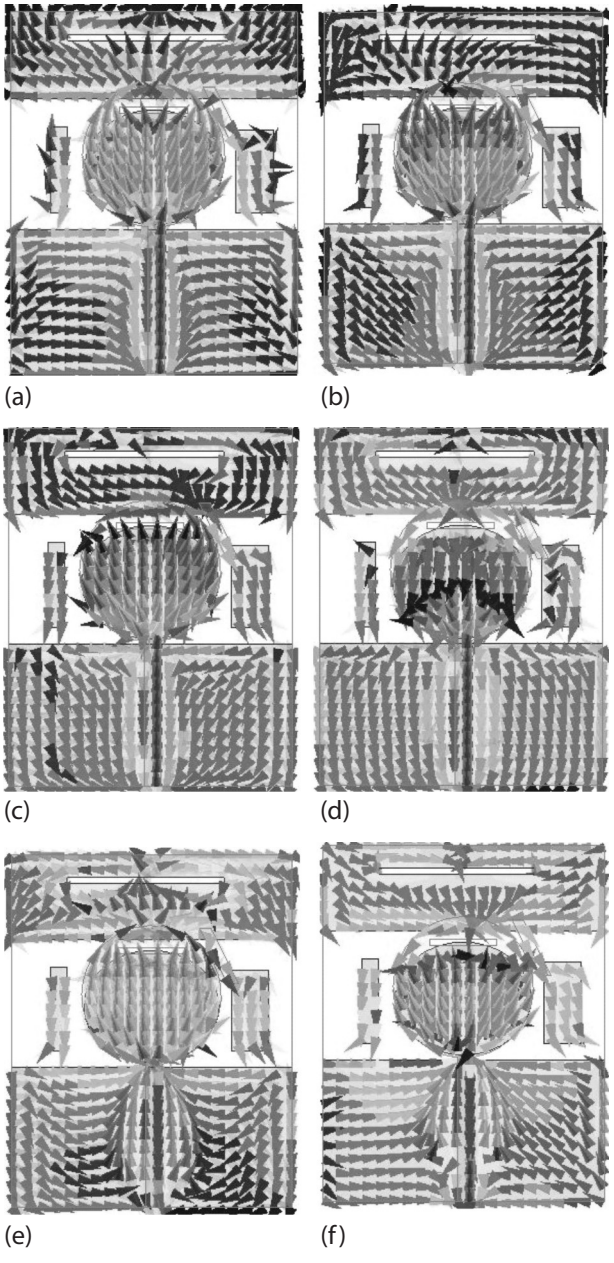

Figure 9: Simulated surface current at (a) 1.8 GHz, (b) 1.9 GHz, (c) 2.1 GHz, (d) 2.4 GHz, (e) 3.6 GHz and (f) 4.5 GHz

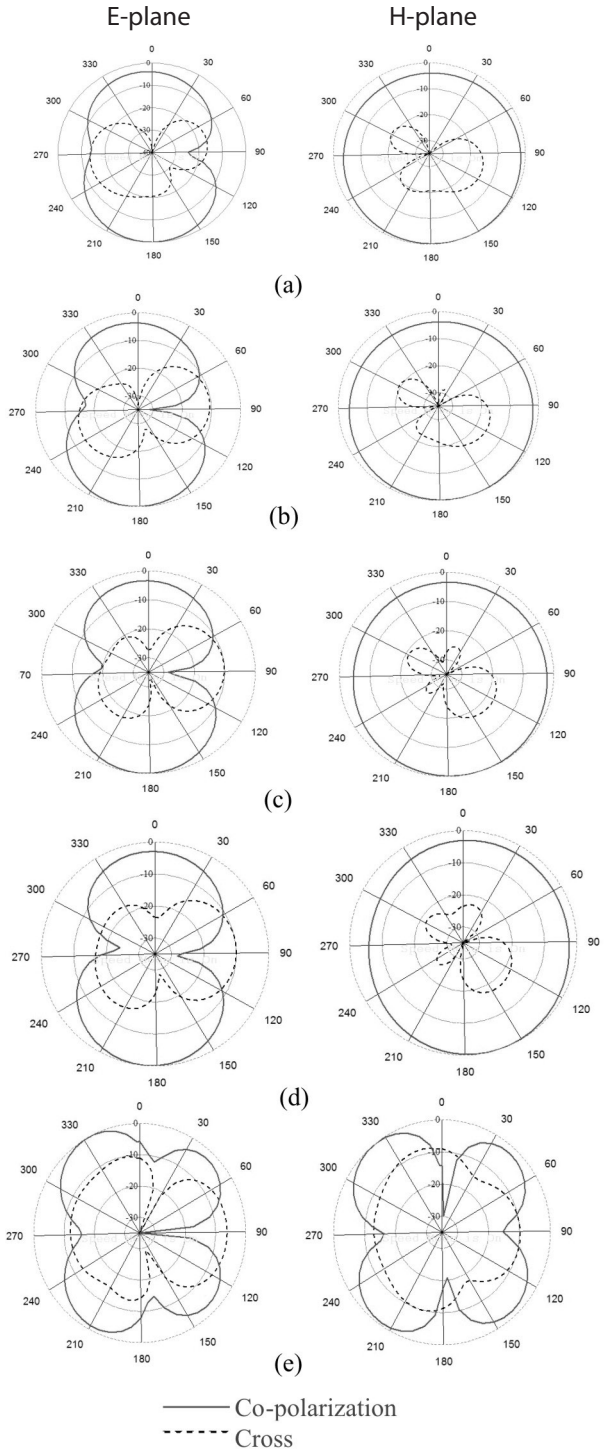

Figure 10: Radiation Pattern (a) at 1.8 GHz, (b) 2.1 GHz, (c) 2.4 GHz, (d) 2.7 GHz and (e) 4.5 GHz

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Design and Analysis of a New Double Negative Metamaterial

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Abstract: This paper presents a new double negative metamaterial unit cell structure which is designed on a Rogers RT 6010 substrate. The proposed structure exhibits resonant frequency within the C-band of microwave spectra and shows a negative permeability and permittivity at that resonant frequency. The commercially available simulation software CST Microwave Studio has been used to get the reflection and transmission parameters of the unit cell. The simulated result shows good conformity with the experimental result. In addition, an analysis has been done with the same design by replacing the substrate with popular FR-4 and then it behaves as a single negative metamaterial at the same frequency band.

Keywords: DNG, Metamaterials, SNG

Načrtovanje in analiza novega dvojno negativne meta material

Izvleček: Članek opisuje novo strukturo osnovne celice dvojno negativnega meta materiala, ki je načrtovana na Roger RT 6010 substratu. Predlagana struktura izkazuje resonančno frekvenco v C pasu mikrovalovnega spektra in izkazuje negativno permeabilnost in permitivnost pri resonančni frekvenci. Za določitev refleksijskih in transmisijskih parametrov je bil uporabljen komercialna programska oprema CST Microwave Studio. Simulacijski rezultati se dobro ujemajo s poskusi. Opravljena je bila tudi analiza strukture na popularnem FR-4 substratuu, kjer struktura deluje kot enojno negativen meta material v enakem frekvenčnem pasu.

Ključne besede: DNG, meta material, SNG

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1 Introduction

Metamaterials are artificially constructed materials which may exhibit some exotic electromagnetic property and not naturally found. It may exhibit negative value of permittivity and permeability simultaneously at a specific frequency range. Metamaterials with simultaneous negative permeability (ε) and permittivity (μ) are called double negative (DNG) metamaterials. Materials of this type of negative characteristics are also called left handed materials (LHM), negative-refractive index materials, and backward wave media. The metamaterials with either of the permittivity or permeability negative is called single negative metamaterial. In 1968, Victor Veselago first explained and theoretically showed that materials with simultaneous negative permeability (μ<0) and permittivity (ε<0) had some different properties as compared to ordinary materials that are found in nature [1] but until 1999 this topic was not much interesting to the researchers due to lack of available such natural materials. Although there are some materials that show the property of effective negative permittivity but materials with effective negative permeability was still a challenging issue. In 2000 Smith at et al. successfully showed a new artificial material of such double negative property (i.e both μ and ε are negative) where, Snell's law, Cherenkov radiation, Doppler Effect are inverted [2]. Due to these exotic electromagnetic properties of these materials, it can be used in many important applications like, antenna design, electromagnetic cloaking, SAR reduction etc [3-6]. There are varieties of metamaterial structures

have been proposed according to the applications like U-shape, V-shape, S-shape, Triangular etc. and very few of them are applicable for C-band microwave spectra [7-12]. In this paper we are introducing a new metamaterial unit cell structure that contains two split ring resonators with a metal stripe between them and shows resonant frequency in the C-band (4-8 GHz) [13] of microwave spectra and it also shows double negative properties (both permittivity and permeability are simultaneously negative) at that frequency.

2 Design of the Unit Cell

The design parameter and the schematic view of the proposed double negative unit cell structure are given in Fig. 1(a). The structure has been designed with two split ring resonators (SRR) of copper and a metal strip of copper between them with all of them having thickness of 0.035mm. Each ring has inner radius 3mm and outer radius 4mm and gap width of 1mm. In between the rings there is a metal strip of copper with a length of 14mm and width of 1.6mm. The gap between each ring and the metal is 0.33mm. The structure is printed over a square shaped Rogers RT 6010 substrate with dielectric constant of 10.2, dielectric loss-tangent of 0.002, side length and width of 30mm and thickness of 1.6 mm. The unit cell parameters are seen in the Table 1.

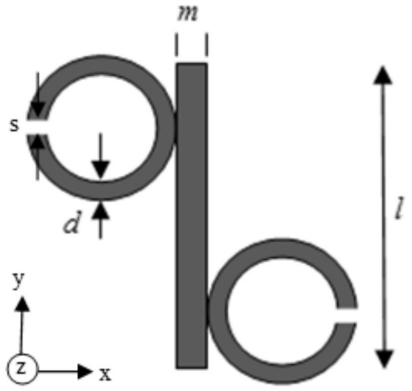
Afterwards for further investigation, the popular FR-4 Substrate has been replaced by the Rogers RT 6010 substrate of the proposed design structure which has dielectric constant of 4.5, dielectric loss-tangent of 0.002, side length and width of 30mm and thickness of 1.6 mm.

Table 1: Design specifications of the unit structure

Unit Cell Parameters	Value (mm)
d	1
l	14
m	1.6
s	1

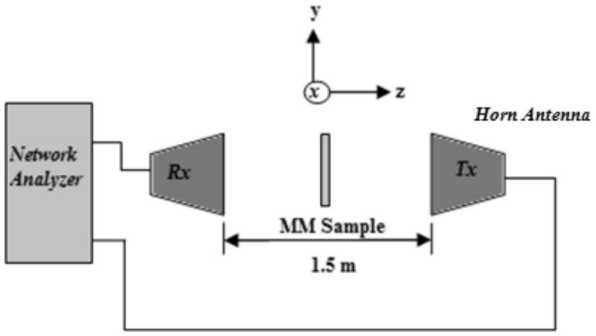
3 Methodology

The commercially available Simulation software CST Microwave Studio has been used to compute complex scattering parameters and also to monitor the resonance frequencies of the proposed unit cell structure. These parameters are used for the retrieval of effective permeability (μ) and permittivity (ε) for the proposed unit cell structure.



(a)

(b)



(c)

Figure 1: (a) The proposed unit cell structure (b) Fabricated metamaterial prototype for measurement on Rogers RT 6010 substrate material (c) Measurement setup (top view)

The structure has been placed between two waveguide ports of positive and negative of z- axis and excited by the transverse electromagnetic (TEM) wave. The perfect electric conductor (PEC) boundary has been defined in the x-plane and the perfect magnetic conductor (PMC) boundary has been defined in the y-plane. Frequency domain solver has been used for simulation. The normalized impedance has been set to 50 ohm. Simulation is done for the frequency range of 4-7 GHz.

However, further simulation is done after replacing the substrate with a FR-4 substrate and the same methodology has been used to get the values of S-Parameters and effective medium parameters.

A 160×160 mm^2 prototype of 4×4 unit cell is fabricated for measurement, as shown in Fig. 1(b). The prototype is then placed between two horn antennas which are 1.5m apart in the same plane. The measurement arrangement is being displayed in Fig. 1(c). An Agilent E8363D vector network analyzer is used to calculate the transmission co-efficient. For calibration purpose, measurement without metamaterial and with metamaterial is done.

There are many methods exist for effective parameter extraction of metamaterial like-TR Method, Lossy-Drude Method, Nicolson-Ross-Weir method etc. The effective medium parameters permeability and permittivity are extracted from the simulated complex S_{21} and S_{11} parameters using method mentioned in [14]. The simplified formulae have been given bellow,

$$V_1=S_{21}+S_{11} \quad (1)$$

$$V_2=S_{21}-S_{11} \quad (2)$$

$$\mu_r \approx \frac{2}{jk_0 d}\frac{1-V_2}{1+V_2} \quad (3)$$

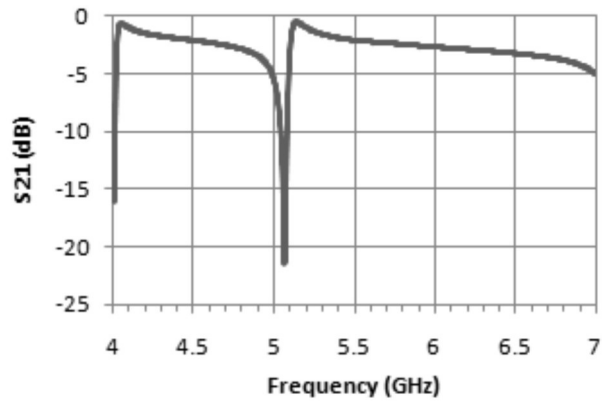
$$\varepsilon_r \approx \frac{2}{jk_0 d}\frac{1-V_1}{1+V_1} \quad (4)$$

$$\eta = \sqrt{\varepsilon_r \mu_r} \quad (5)$$

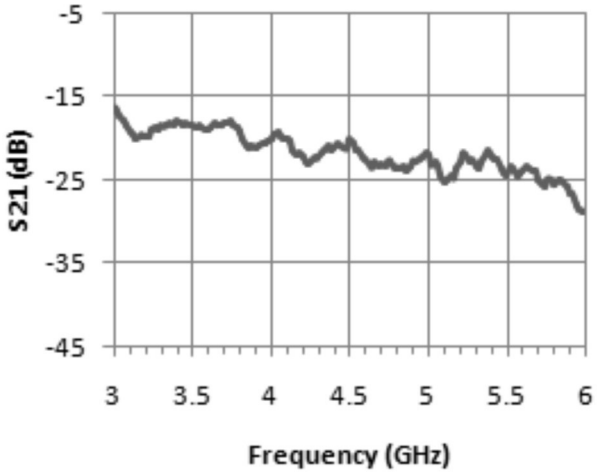
where, ε_r is the effective permittivity, μ_r is the effective permeability, 'd' is the thickness of the substrate, k_0 is the wave number and η is the refractive index.

4 Results and Discussion

The simulated result of transmission coefficient (S_{21}) for the proposed unit cell structure is given in Fig-2(a) and the experimental results for the unit cell are seen in Fig. 2(b) and 2(c). Here the simulated spectra of the transmission coefficient (S_{21}) shows the maximum resonance at 5.09 GHz which is in the range of C-band microwave spectra and the experimental result of the transmission coefficient that is seen in the Fig. 2(c), agrees well with the simulated result. Unlike the SRR rings the currents flows in the opposite direction of the two rings and these two opposite currents also create opposite currents in the two sides of the metal strip and Fig-3 shows the currents distribution at frequency 5.09 GHz in the unit cell structure.



(a)



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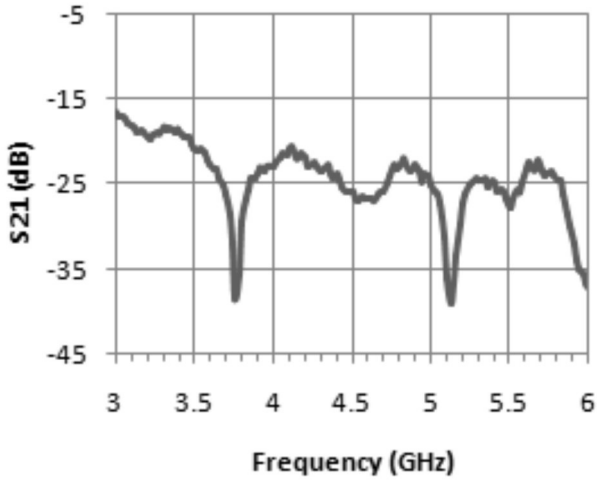


(c)

Figure 2: (a) Simulated transmission coefficient (S_{21}) in dB (b) Measured value of S_{21} in dB without metamaterial (c) Measured value of S_{21} in dB with metamaterial sample

The two metal rings are responsible for creating the inductance and by increasing the side length of the rings the inductance can be increased which leads to decrease the LC resonance frequency. On the other hand

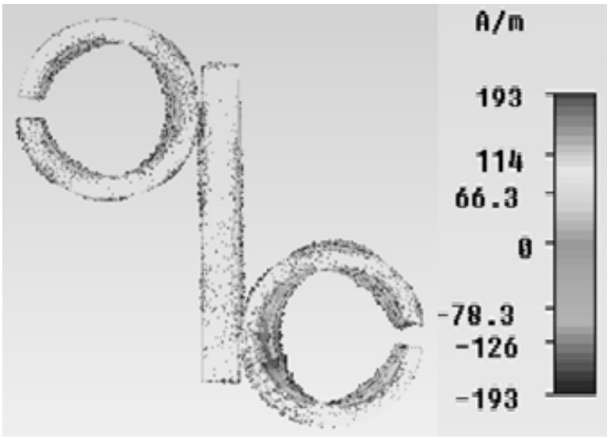
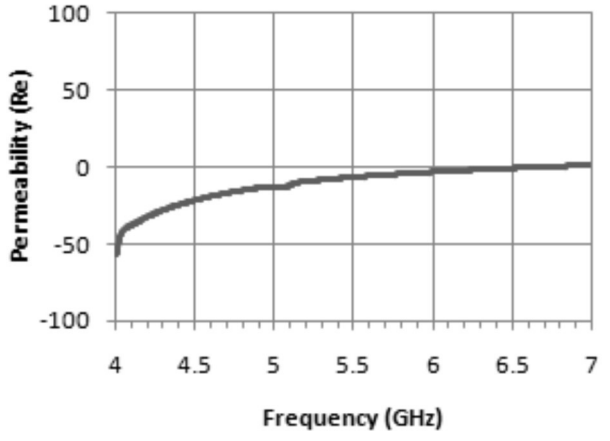


Figure 3: Current distribution in the unit cell structure

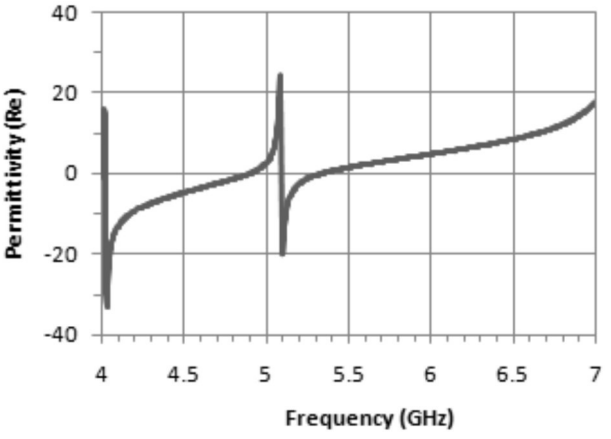
as the split of the rings are responsible for creating the capacitance for the design, by increasing the gap the capacitance can be reduced which leads to increase the LC resonant frequency.

These results are given in Fig-4(a) and Fig-4(b) where the effective permeability is shown in Fig-4(a) and effective permittivity is shown in Fig-4(b) against frequency. In Fig-4(a) and 4(b), we see that at the maximum point of resonance frequency of 5.09 GHz, the both curve of permeability and permittivity show negative value and they are ε= -13.93 (Real) and μ= -11.92 (Real) . So, the structure can be said a double negative (DNG) metamaterial. Normally a charge builds up in the gap of a split ring resonator and creates capacitance if it is kept in a changing magnetic field. At low frequency the current of the oscillator remain in phase of the driving field but in higher frequency the current starts lagging which produces negative permeability at that frequency.

The DNG material are also called negative refractive index materials, backward media, and left handed materials (LHM). In case of negative refractive index material, the light rays are refracted in the same side of its entrance. Actually in a double negative media the phase and the energy flow of the wave moves in the opposite direction which makes the wave to flow in the backward direction. Accordingly in Fig-5 the real part of refractive index curve is seen against the frequency where at frequency 5.09 GHz the refractive index is also negative and that is η= -19.09 . So, realization of negative permeability over that frequency bands may also be useful in long distance communication applications. The simulated result also depicts the double negative characteristics for the unit cell at the frequency of 4.03GHz which is in the range of S-band (2-4GHz) microwave spectra. However, the measured result has bit displaced from the simulated result in this case. This difference most likely happens because of fabrication error.



(a)



(b)

Figure 4: (a) Real value of effective permeability (μ) versus frequency (b) Real value of effective permittivity (ε) versus frequency

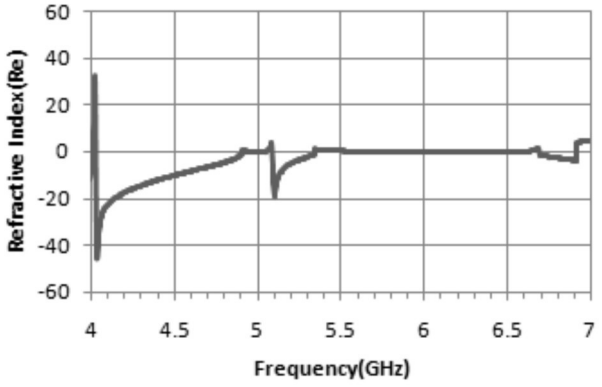
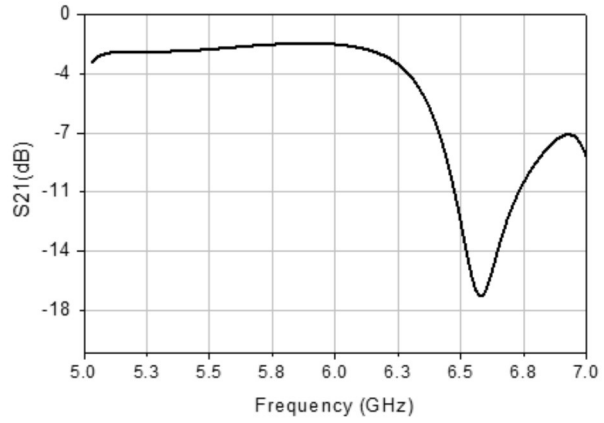


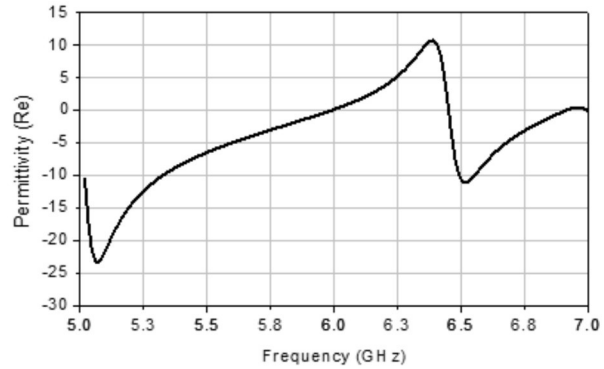
Figure-5: Real value of Refractive Index versus frequency.

After using the FR-4 substrate for the same design structure it is seen in Fig-6 (a), that the S-Parameter spectra has changed a bit. Previously we found that transmission spectra at 5.09 GHz for the design on Rogers RT 6010 substrate and we had sharp resonance below -25dB whereas for substrate FR-4 we have got

the resonance at the frequency of 6.65 GHz but this time the resonance is seen very close to -18dB. Actually this difference in the transmission coefficients of Fig. 2(a) and Fig. 6(a) has occurred due to the difference of dielectric constants in the two substrate materials, where the Rogers RT 6010 has dielectric constants of 12.2 and FR-4 has 4.2. The dielectric constant of a material depends on the material internal structure. When electromagnetic waves propagated through a material it's electric and magnetic fields oscillate as sinusoidal pattern and its velocity depends upon the electrical conductivity of the material which actually depends on the internal structure of the material. The relative speed of electrical signal that travel through the material varies according to the type of interaction with its internal structure and this variation caused the different results in the transmission characteristics. In Fig. 6(b), the frequency versus permittivity curve for FR-4 substrate depicts that permittivity is still negative and its real value is ε= -4.77 which was -1.03 for Rogers RT 6010 based design. However the Fig. 7(a) reveals that the permeability for the FR-4 substrate for the same design does not show negativity and the real value is μ= 8.33 which was previously -4.48 for Rogers RT 6010 substrate. So, now it is clear that the design based on FR-4 substrate does not show double negative characteristics and accordingly the real value of refractive index in Fig-7(b) reveals the positive value of η= 0.92. So, for FR-4 substrate the material can be characterized as single negative (SNG) metamaterial. The overall comparative results are presented in Table 2.

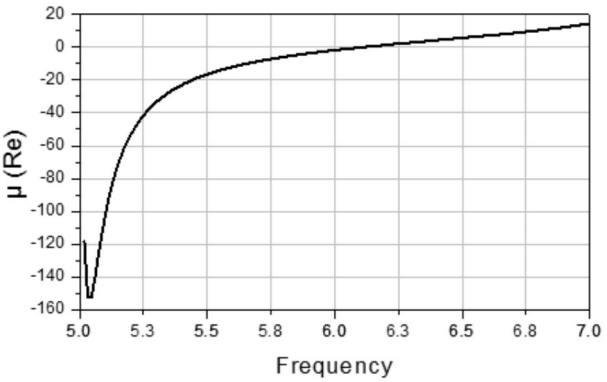


(a)

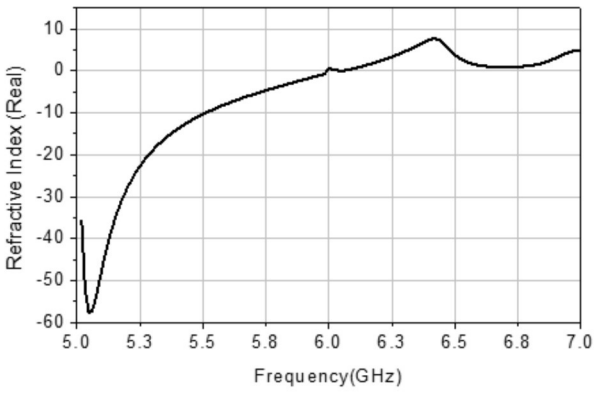


(b)

Figure 6: (a)Transmission coefficient for FR-4 substrate material (b) Real magnitude of permittivity (ε) for FR-4 substrate material



(a)



(b)

Figure 7: (a) Real magnitude of permeability (μ) for FR-4 substrate material (b) Real magnitude of refractive Index (η) for FR-4 substrate material

Table 2: Effective parameters comparisons for two popular substrate materials

Substrate	Dielectric Constant	Frequency (GHz)	Permittivity(ε)	Permeability(μ)	Refractive Index (η)	Metamaterial Type
Rogers RT 6010	10.2	5.09 GHz	-13.93	-11.92	-19.09	DNG
FR-4	4.2	6.65 GHz	-4.77	8.33	0.92	SNG

5 Conclusion

In this paper we have presented a new double negative metamaterial structure on Rogers RT 6010 that resonates at frequency in 5.09 GHz which is in the C-band of microwave spectra. We have then changed the substrate by popular FR-4 substrate and we have found the resonance at point of 6.65 GHz which is also in the C-band. However, it does not show double negative characteristics at 6.65GHz. C-band of microwave spectra specially used for long distance communication like, satellite communications. We have used two popular substrates to demonstrate its metamaterial characteristics and we have done comparative analyses between them. So, this structure can be used besides other metamaterials especially in the C-band metamaterial applications.

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CCM and DCM Analysis of Quasi-Z-Source Derived Push-Pull DC/DC Converter

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Abstract: This paper presents a steady state analysis of the operation modes of the quasi-Z-source (qZS) derived push-pull DC/DC converter topology. It was derived by the combination of the qZS network and coupled inductors. The output stage of the converter consists of a diode bridge rectifier and an LC-filter. This topology provides a wide regulation range of the input voltage and galvanic isolation. These features fit the requirements for the integration systems of renewable energy sources, such as PV panels, variable speed wind turbines, and fuel cells. A converter can operate in continuous (CCM) and discontinuous conduction mode (DCM). Switching period is divided into four and six intervals for CCM and DCM, respectively. Equivalent circuits and analytical expressions for each interval are presented. The DC gain factor for each mode is derived. To simplify our analysis, coupled inductors were substituted with a model that consists of an ideal transformer and magnetizing inductance. Leakage inductances are neglected because the coupling coefficient in this topology should be close to unity. In DCM the converter operation depends on the active duty cycle and the duty cycle of the zero current condition. Two solutions are possible for the DC gain factor in DCM. It is theoretically impossible to achieve the unity DC gain factor in DCM if the turns ratio of coupled inductors is equal to or more than one. The proposed topology was simulated with PSIM software in two operating points. Experimental verification proves our theoretical and simulation results.

Keywords: DC/DC converter, quasi-Z-source converter, galvanic isolation, renewable energy, steady state analysis.

Analiza CCM in DCM Push-Pull DC/DC pretvornika z impedančnim prilagodilnim vezjem

Izvleček: Članek opisuje statično analizo delujočih stanj push-pull DC/DC pretvornika z impedančnim prilagodilnim vezjem (qZS). Izveden je s kombinacijo qZS omrežja in sklopljenih tuljav. Izhodna stopnja pretvornika je sestavljeno iz diodnega usmerniškega mostiča in LC filtra. Topologija omogoča široko regulacijsko območje in galvansko ločitev. Lastnosti ustrezajo zahtevam integriranih sistemov obnovljivih virov energije, kot so PV moduli, vetrne turbine s spremenljivo hitrostjo in gorivne celice. Pretvornik lahko deluje v neprekinjenem (CCM) ali prekinjevalnem (DCM) prevodnem režimu. Perioda preklapljanja je razdeljena na štiri ali šest intervalov za CCM oziroma DCM. Predstavljeno je ekvivalentno vezje in analiza za vsak interval ločeno. Za vsak način je izračunano faktor DC ojačenja. Za poenostavljeno analizo so bili, za sklopljene tuljave, uporabljeni modeli z idealnim transformatorjem in magnetno induktivnostjo. Uhajalne induktivnosti so zaradi enotnosti koeficienta enotnosti v tej topologiji zanemarjene. Pri DCM je delovanje odvisno od aktivnega obratovalnega ciklusa in obratovalnega ciklusa pri ničelnem toku. Možni sta dve rešitvi za DC ojačenje pri DCM. Teoretično je nemogoče doseči enotno ojačenje pri DCM če je razmerje ovojev sklopljenih tuljav večje ali enako ena. Predlagana topologija je bila simulirana s programskim paketom PSIM v dveh točkah delovanja. Ekperimentalen preizkus potrjuje teorijo in rezultate simulacij.

Ključne besede: DC/DC pretvornik, impedančno prilagodilno vezje, galvanska ločitev, obnovljivi viri, statična analiza

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1 Introduction

Quasi-Z-source inverters (qZSIs) providing logical improvement of Z-source inverters were proposed in 2008 [1]. QZSIs extend the family of single stage buck-boost inverters. The concept of the QZSI provides improved reliability due to high EMI withstandability, wide input voltage regulation possibility, and continuous input

current. These features make the qZSI appropriate for the realization of renewable energy systems (PV panels, fuel cells, wind turbines, etc.) [2]-[5] and electric vehicle applications [6]. Output voltage of the renewable energy sources (RES) usually is by far lower than grid voltage. An intermediate DC/DC converter can be used for voltage stabilization when high step-up is needed for RES integration into the grid [7-9]. DC/DC qZSI-based converters have been widely used because of their good performance as voltage matching converters that interconnect the RES and the grid-tied inverter [10]-[12].

The recent push-pull converter derived from the quasi-z-source (qZS) concept is shown in Fig. 1 [13]. This topology has ample opportunities for DC gain regulation [14]. Continuous input current can be achieved in a wide range even for the discontinuous conduction mode (DCM) in branches. The converter contains small component count and only two active switches that lead to a simple control circuit. Topology derivation is based on the combination of two qZS networks implemented with two three-winding coupled inductors.

The converter utilizes two qZS networks: C_1, C_2, D_1, TR_1 and C_3, C_4, D_2, TR_2, as shown in Fig. 1. Three-winding coupled inductors TR_1 and TR_2 provide galvanic isolation and store energy in the form of equivalent magnetizing current (i.e. field in the core of the coupled inductors). Transistors T_1 and T_2 work interleaved. The turn-on state of the transistor corresponds to the shoot-through behavior of the qZS network. Capacitors of the qZS network transfer part of the stored energy to the coupled inductor and the output load during the equivalent shoot-through state. Voltage across the primary windings can be described similarly to that of the conventional qZS network. Current in the primary windings of the coupled inductors differs from the current in the conventional qZS network due to the energy transfer process in the coupled inductors. From the input side the converter looks like two independent branches. These branches are connected in series by means of secondary windings. Summarized voltage of the secondary windings $v_S(t)$ is applied to the diode bridge rectifier $D_3 \ldots D_6$. Rectified voltage feeds the output load with the rectified voltage through the LC-filter L_f, C_f. The frequency of the current ripple of the input current and the output inductor current is twice higher than the switching frequency of the transistors. Voltage regulation is achieved by the adjusting of the turn-on state (active) duty cycle of the transistor.

The aim of this article is to present an analytical description for possible operation modes of the qZS derived push-pull converter. Like most of step-up switching power converters, the investigated topology can operate in the continuous conduction mode (CCM) and DCM. In DCM the transistors and diodes of the qZS networks suffer from high voltage stress. DCM occurs at low DC gain and low input power. The DC gain characteristic depends strongly on the operation mode. This paper is based on our earlier preliminary version [15] and includes substantially revised theoretical analysis and additional experimental results, not presented there.

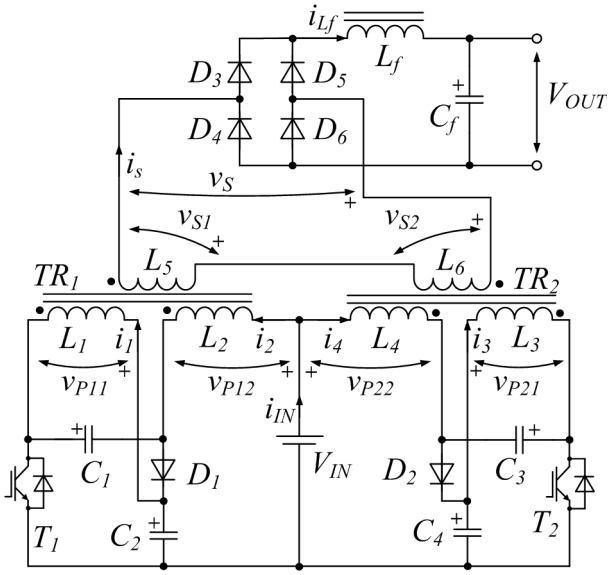


Figure 1: qZS-derived push-pull converter topology.

Several assumptions should be made for our further analysis. In this topology a coupled inductor should have the coupling coefficient close to unity. Primary windings should have an equal number of turns N_{12}. It means that in each qZS network voltages across the primary windings are equal: $v_{P11}(t) = v_{P12}(t)$, $v_{P21}(t) = v_{P22}(t)$. The secondary winding utilizes N_3 turns. The turns ratio $k = N_3/N_{12}$ defines the minimum achievable DC gain. Voltage across the secondary winding depends on the turns ratio and the voltage of the primary windings: $v_{S1}(t) = k \cdot v_{P11}(t)$, $v_{S2}(t) = -k \cdot v_{P21}(t)$, $v_{S1}(t) + v_{S2}(t) = v_S(t)$. In this case coupled inductors can be substituted with a simplified model that consists of the magnetizing inductance L_M reflected to one of the windings and an ideal transformer with N_{12}:N_3 primary to secondary turns ratio. Also, in any mode currents in the primary windings of each coupled inductor are equal: $i_1(t) = i_2(t)$, $i_3(t) = i_4(t)$. Let us assume that the voltage ripple of all capacitors in the converter is well below the corresponding average voltage. These assumptions and the symmetry of branches result in equal average voltages across the capacitors: $V_{C1} = V_{C3}$, $V_{C2} = V_{C4}$. Let us assume that the current of the filter inductor $i_{Lf}(t)$ is continuous in any mode. None of the losses are considered in this article. It means that the input power P and the output power are equal: $I_{OUT} = I_{Lf} = P/V_{OUT}$. The lower case letter of the voltage and the current corresponds to an instantane-

ous value, and the upper case letter or angle brackets correspond to an averaged (or constant in some cases) value. The input power is represented as *P*. For the symmetry operation of the branches, each of them should operate at half of the rated power: $I_4 = I_2 = P/(2 \cdot V_{IN})$.

2 Circuit Steady-State Analysis in CCM

Current and voltage waveforms for an idealized converter in CCM are shown in Fig. 2. The figure shows that the switching period of the converter *T* can be divided into four time intervals: two equal active intervals during which only one of the transistors is turned on (i.e. active states with the time duration t_A each) and two inactive intervals when both transistors are not conducting (i.e. zero state, t_0 each):

$$\frac{t_A}{T} + \frac{t_0}{T} = D_A + D_0 = 0.5. \tag{1}$$

where D_A is the duty cycle of an active state and D_0 is the duty cycle of a zero state. It is clear from (1) that $D_A < 0.5$ and $D_0 < 0.5$. In CCM, as well as in DCM, the current $i_{Lf}(t)$ has a double switching frequency ripple. Also, in both modes $i_{Lf}(t)$ always rises during active states and falls during a zero state.

Figure 3a shows the equivalent circuit of the converter for the time interval *t1-t2* when the transistor T_1 is turned on, diode D_1 is blocked and D_2 is conducting. Equations (2)-(6) describe the behavior of the converter during this time interval.

$$v_{C1}(t) = v_{C2}(t) - V_{IN}, \tag{2}$$

$$v_{C2}(t) = v_{P11}(t) = L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - k \cdot i_{Lf}(t)\right), \tag{3}$$

$$v_{C3}(t) = -v_{P21}(t) = -L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) + k \cdot i_{Lf}(t)\right), \tag{4}$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \tag{5}$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C2}(t) + v_{C3}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) - 2 \cdot k \cdot i_{Lf}(t)\right). \tag{6}$$

where $v_{C1}(t)$, $v_{C2}(t)$, $v_{C3}(t)$, $v_{C4}(t)$ are the capacitor voltages, $v_{S1}(t)$ and $v_{S2}(t)$ are the voltages of the corresponding secondary windings of the transformer, $v_S(t)$ is the summarized voltage of the secondary winding applied to the rectifier, $i_1(t)$, $i_2(t)$, $i_3(t)$, $i_4(t)$ are the currents of the corresponding primary windings of the transformer, L_M is the magnetizing inductance of the coupled inductors, *k* is the turns ratio of the coupled inductors, and $i_{Lf}(t)$ is the current of the filter inductor L_f.

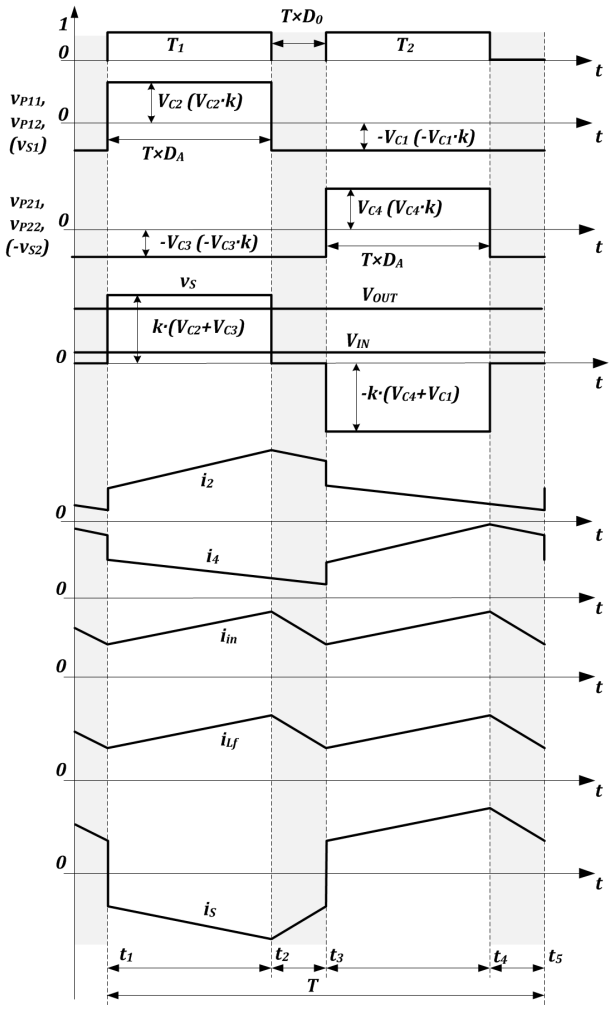


Figure 2: Generalized converter voltage and current waveforms during the operation in CCM.

During the interval t_2-t_3 both transistors are not conducting, diodes D_1 and D_2 are conducting. The equivalent circuit of the converter is depicted in Fig. 2b. Equations (7)-(11) describe the operation of the converter for that time interval. Summarized voltage of the secondary windings $v_S(t)$ is equal to zero if the voltage ripple of the qZS capacitors is negligible.

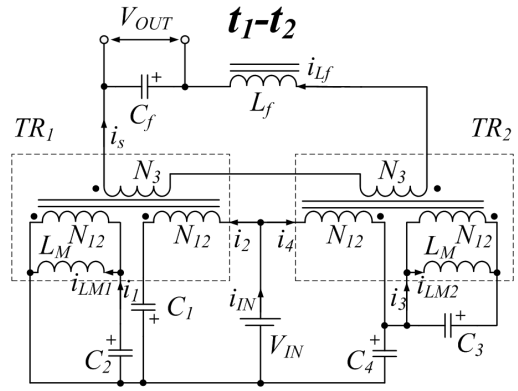
$$v_{C1}(t) = -v_{P11}(t) = -L_M \cdot \frac{di_{LM1}(t)}{dt} \\ = -L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - k \cdot i_{Lf}(t)\right), \tag{7}$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \tag{8}$$

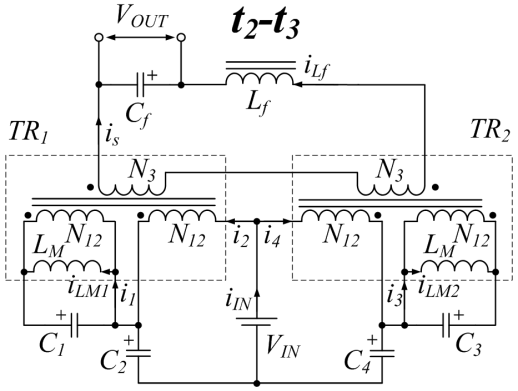
$$v_{C3}(t) = -v_{P21}(t) = -L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) + k \cdot i_{Lf}(t)\right), \tag{9}$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \tag{10}$$

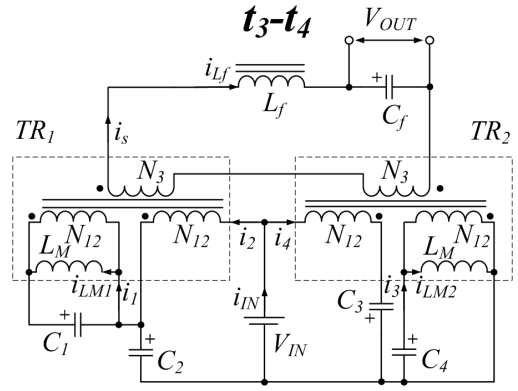
(a)



(b)



(c)



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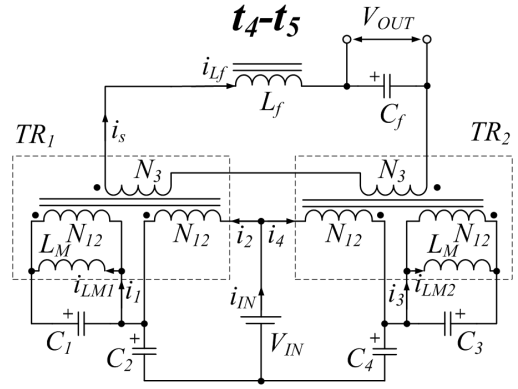

Figure 3: Equivalent circuits of the investigated converter in CCM.

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C3}(t) - v_{C1}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) - 2 \cdot k \cdot i_{Lf}(t)\right) \approx 0. \quad (11)$$

Figure 2c depicts the equivalent circuit of the converter for the time interval t_3-t_4 when the transistor T_2 is turned on, the diode D_2 is reverse based and D_1 is conducting. Equations (12)-(16) define the operation of the converter during the time interval t_3-t_4:

$$v_{C1}(t) = -v_{P11}(t) = -L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) + k \cdot i_{Lf}(t)\right), \quad (12)$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \quad (13)$$

$$v_{C3}(t) = v_{C4}(t) - V_{IN}, \quad (14)$$

$$v_{C4}(t) = v_{P21}(t) = L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) - k \cdot i_{Lf}(t)\right), \quad (15)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(-v_{C1}(t) - v_{C4}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) - 2 \cdot k \cdot i_{Lf}(t)\right). \quad (16)$$

During the interval t_4-t_5 both transistors are switched off, diode D_1 and diode D_2 are conducting. The equivalent circuit for the fourth interval is shown in Fig. 2b. Equations (17)-(21) define the behavior of the converter for the time interval t_4-t_5. Summarized voltage of the secondary windings $v_S(t)$ is equal to zero if the voltage ripple of the qZS capacitors is negligible. The fourth interval differs from the second in the direction of the current $i_{Lf}(t)$ via the secondary windings, i.e. $i_S(t)$ has an opposite sign.

$$v_{C1}(t) = -v_{P11}(t) = -L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) + k \cdot i_{Lf}(t)\right), \quad (17)$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \quad (18)$$

$$v_{C3}(t) = -v_{P21}(t) = -L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) - k \cdot i_{Lf}(t)\right), \quad (19)$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \quad (20)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C3}(t) - v_{C1}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) + 2 \cdot k \cdot i_{Lf}(t)\right) \approx 0. \quad (21)$$

At the time moments t_1, t_3 and t_5 currents in the primary windings change by step:

$$\Delta i_2(t_1) = -\Delta i_4(t_1) = k \cdot i_{Lf}(t_1),$$

$$\Delta i_4(t_3) = -\Delta i_2(t_3) = k \cdot i_{Lf}(t_3),$$

$$\Delta i_2(t_5) = -\Delta i_4(t_5) = k \cdot i_{Lf}(t_5).$$

This step change could be explained by the change of the direction of the current $i_S(t)$. Also, these steps are equal because $i_{Lf}(t_1) = i_{Lf}(t_3) = i_{Lf}(t_5)$. These steps are not reflected in the input current because the steps of currents $i_2(t)$ and $i_4(t)$ compensate each other.

According to the voltage-second balance principle, the average voltage across the primary winding of the coupled inductor over one switching period equals zero. That can be used for the calculation of the average voltage across the qZS capacitors:

$$V_{P11} = \langle v_{P11}(t) \rangle = \frac{1}{T}\int_0^T v_{P11}(t)dt = 0, \tag{22}$$

$$V_{P21} = \langle v_{P21}(t) \rangle = \frac{1}{T}\int_0^T v_{P21}(t)dt = 0. \tag{23}$$

In order to solve Eqs. (22) and (23) we need to assume that the voltage across the capacitors is close to the average value over the switching period:

$$v_{C1}(t) \approx \langle v_{C1}(t) \rangle = V_{C1}, \tag{24}$$

$$v_{C2}(t) \approx \langle v_{C2}(t) \rangle = V_{C2}, \tag{25}$$

$$v_{C3}(t) \approx \langle v_{C3}(t) \rangle = V_{C3}, \tag{26}$$

$$v_{C4}(t) \approx \langle v_{C4}(t) \rangle = V_{C4}. \tag{27}$$

The following expressions are right for all the intervals according to Eqs. (24)-(27) and (2)-(21):

$$V_{C2} = V_{IN} + V_{C1}, \tag{28}$$

$$V_{C4} = V_{IN} + V_{C3}. \tag{29}$$

$$V_{C1} = V_{C3}, \tag{30}$$

$$V_{C2} = V_{C4}. \tag{31}$$

From Eqs. (22)-(31) it is easy to find expressions for the capacitor voltages:

$$V_{P11} = V_{C2} \cdot D_A - V_{C1} \cdot (1 - D_A) =$$
$$= D_A \cdot (V_{IN} + V_{C1}) - V_{C1} \cdot (1 - D_A) = 0,$$

$$V_{C1} = V_{C3} = \frac{D_A}{1 - 2 \cdot D_A} V_{IN}, \tag{32}$$

$$V_{C2} = V_{C4} = \frac{1 - D_A}{1 - 2 \cdot D_A} V_{IN}. \tag{33}$$

Using Eqs. (1)-(33) and considering all the abovementioned assumptions, the summarized voltage of the secondary windings of the coupled inductors could be analytically expressed for each time interval:
Time interval t_1-t_2:

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot (V_{C2} + V_{C3}). \tag{34}$$

Time interval t_3-t_4:

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = -k \cdot (V_{C1} + V_{C4}). \tag{35}$$

Time intervals t_2-t_3 and t_4-t_5:

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot (V_{C3} - V_{C1}) = 0. \tag{36}$$

In CCM the output voltage of the converter can be expressed as

$$V_{OUT} = \frac{1}{T}\int_0^T |v_{S1}(t) + v_{S2}(t)| \cdot dt =$$
$$= k \cdot \frac{2}{T}\int_0^{T \cdot D_A} (V_{C3} + V_{C2}) \cdot dt = \frac{N_3}{N_{12}} \cdot \frac{2 \cdot D_A}{1 - 2 \cdot D_A} \cdot V_{IN}. \tag{37}$$

The resulting DC voltage gain of the proposed DC/DC converter is

$$G = k \cdot \frac{2 \cdot D_A}{1 - 2 \cdot D_A}. \tag{38}$$

In Fig. 4 the DC voltage gain of the converter (38) is depicted as a function of an active state duty cycle for different turns ratios of the coupled inductors. As is seen, a very wide regulation range of the DC voltage gain could be achieved for the lossless system. Also, high step-up can be reached using coupled inductors with a high turns ratio. In real systems the DC voltage gain of the step-up converter usually is seriously influenced by the losses in the components, especially in semiconductors.

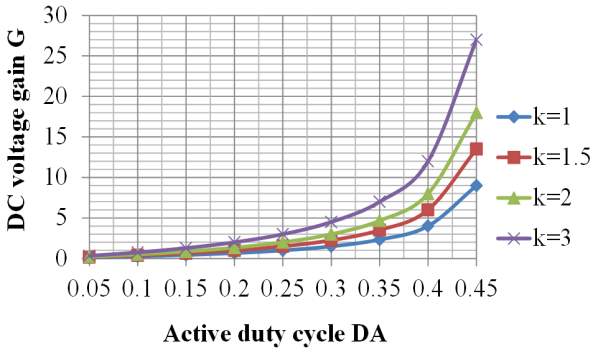

Figure 4: DC voltage gain G as a function of the active state duty cycle D_A for the proposed DC/DC converter operated in CCM.

3 Circuit Steady-State Analysis in DCM

In general, the converter operation mode is considered as DCM when the input current falls to zero. However, in the investigated topology, DCM will be considered as a mode when the current in the primary winding of the coupled inductor drops to zero. In DCM the input current can still remain continuous. Typical waveforms

for DCM are shown in Fig. 5. Two additional equivalent circuits that are needed for the analysis of DCM are shown in Figs. 6a and 6b. These figures correspond to the time intervals t'_1-t_2 and t'_3-t_4, respectively. During other time intervals converter operation is the same as for CCM. If the duty cycle of the DCM state γ less than the D_0 converter operation is almost similar to CCM.

Figure 6a shows the equivalent circuit of the converter during the time interval t'_1-t_2 when the transistor T_1 is turned on, diode D_1 is reverse based, and diode D_2 is not conducting. This mode is possible only if $\gamma > D_0$. Voltage is applied to the diode D_2: $v_{D2}(t) = v_{C3}(t) + \alpha$, where $\alpha = v_{P21}(t)$. Voltage α is constant during this time interval. Equations (39)-(43) describe the operation of the converter during this time interval when $i_3(t) = i_4(t) = 0$.

$$v_{C1}(t) = v_{C2}(t) - V_{IN}, \quad (39)$$

$$v_{C2}(t) = v_{P11}(t) = L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - k \cdot i_{Lf}(t)\right), \quad (40)$$

$$v_{P21}(t) = v_{P22}(t) = \alpha = k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt}, \quad (41)$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \quad (42)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C2}(t)\right) - k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt} = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - 2 \cdot k \cdot i_{Lf}(t)\right) \approx V_{C2} - \alpha. \quad (43)$$

Figure 6b shows the equivalent circuit of the converter for the time interval t'_3-t_4 when the transistor T_2 is conducting, the diode D_1 is not conducting, and the diode D_2 is reverse based. Voltage is applied to the diode D_1: $v_{D1}(t) = v_{C3}(t) + \alpha$, where $\alpha = v_{P11}(t)$. Equations (44)-(48) describe the behavior of the converter over this time interval considering that $i_1(t) = i_2(t) = 0$.

$$v_{P11}(t) = v_{P12}(t) = \alpha = k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt}, \quad (44)$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \quad (45)$$

$$v_{C3}(t) = v_{C4}(t) - V_{IN}, \quad (46)$$

$$v_{C4}(t) = v_{P22}(t) = L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) - k \cdot i_{Lf}(t)\right), \quad (47)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(-v_{C4}(t)\right) + k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt} = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(-i_3(t) - i_4(t) + 2 \cdot k \cdot i_{Lf}(t)\right) \approx -V_{C4} + \alpha. \quad (48)$$

3.1 DCM mode 1

If the duty cycle of the DCM state is less than the duty cycle of the zero state ($0 < \gamma < D_0$), the operation of the converter will remain unchanged. In this case the behavior of the converter could be described by Eqs. (2)-(6).

3.2 DCM mode 2

In case the duty cycle of the DCM state lies in the range $D_0 < \gamma < 0.5$, the average voltage of the qZS capacitors and the DC voltage gain of the converter should be recalculated. It can be done using Fig. 5, taking into account (22)-(31), and assuming that α is equal to zero in order to simplify the calculations:

$$V_{P11} = V_{C2} \cdot D_A - V_{C1} \cdot (1 - D_A - \gamma + D_0) = \\ = D_A \cdot (V_{IN} + V_{C1}) - V_{C1} \cdot (1.5 - \gamma - 2 \cdot D_A) = 0,$$

$$V_{C1} = V_{C3} = \frac{2 \cdot D_A}{3 - 2 \cdot \gamma - 6 \cdot D_A} V_{IN}, \quad (49)$$

$$V_{C2} = V_{C4} = \frac{3 - 2 \cdot \gamma - 4 \cdot D_A}{3 - 2 \cdot \gamma - 6 \cdot D_A} V_{IN}. \quad (50)$$

The output voltage of the converter operated in DCM when $D_0 < \gamma < 0.5$ can be expressed as

$$V_{OUT} = \frac{1}{T}\int_0^T \left|v_{S1}(t) + v_{S2}(t)\right| \cdot dt \approx \\ \approx k \cdot \frac{2}{T}\left(\int_0^{T \cdot (0.5-\gamma)} (V_{C2} + V_{C3}) \cdot dt + \int_{T \cdot (0.5-\gamma)}^{T \cdot D_A} V_{C2} \cdot dt\right) = \\ = \frac{N_3}{N_{12}} \cdot \frac{8 \cdot D_A \cdot (1 - \gamma - D_A)}{3 - 2 \cdot \gamma - 6 \cdot D_A} \cdot V_{IN}. \quad (51)$$

The resulting DC voltage gain of the proposed DC/DC converter is

$$G = k \cdot \frac{8 \cdot D_A \cdot (1 - \gamma - D_A)}{3 - 2 \cdot \gamma - 6 \cdot D_A}. \quad (52)$$

In the DCM, when $\gamma = 0.5$ each branch consumes current only during $T/2$. In this case, time t_1 equals t'_1, and time t_3 equals t'_3. The input current of the converter is in the boundary conduction mode and reaches zero twice per switching period at the time moments t_1 and t_3. Current steps occur due to the change of the sign of the current $i_S(t)$ at the same time moments.

The condition $\gamma > 0.5$ is theoretically possible when the converter needs to operate at very low input power compared to the rated power value. This mode corresponds to the discontinuous input current. It should be avoided because of high overvoltage across the power semiconductor components. This mode could be avoided practically due to the losses in the converter. Also, renewable energy systems usually require high step-up at low power, or do not require ultra-light-load operation. On the other hand, in this mode the converter needs enormous inductance at the output filter

to satisfy the assumption about the continuous inductor current.

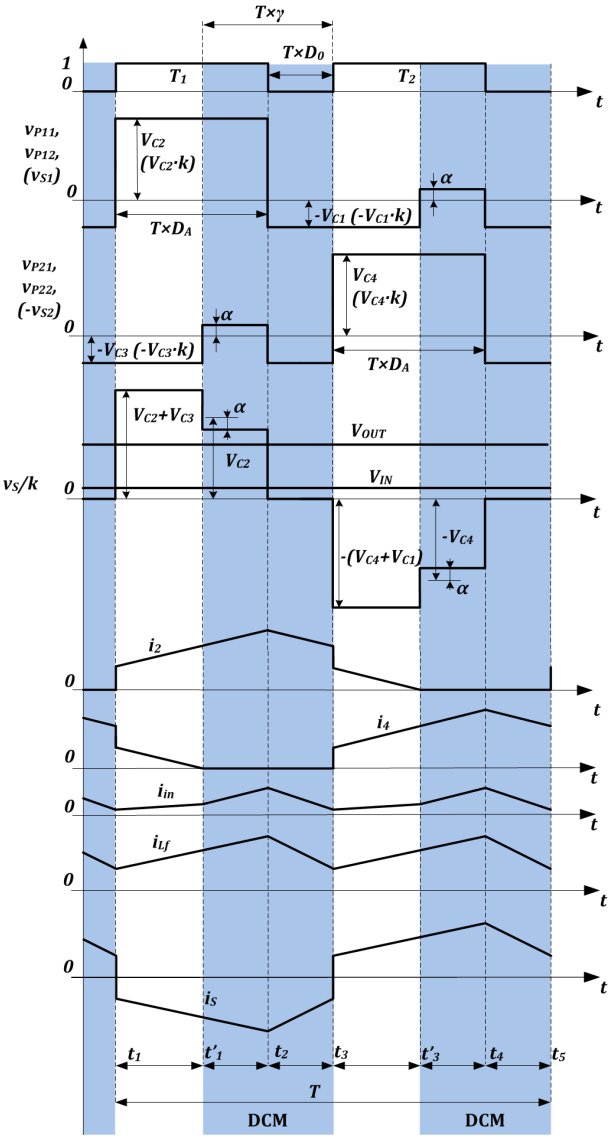

Figure 5: Generalized converter voltage and current waveforms during the operation in DCM.

4 Experimental Verification

Theoretical assumptions were verified by means of modeling. The model was rated for the power of 600 W in compliance with the topology shown in Fig. 1. Component values and given modeling conditions are listed in Table I. Simulation results are shown in Figs. 8 and 10. In the first case, the model of the converter operates in CCM (input voltage of 70 V and D_A = 0.43), while in the second modeling, the converter operates in DCM (input voltage of 250 V and D_A = 0.25).

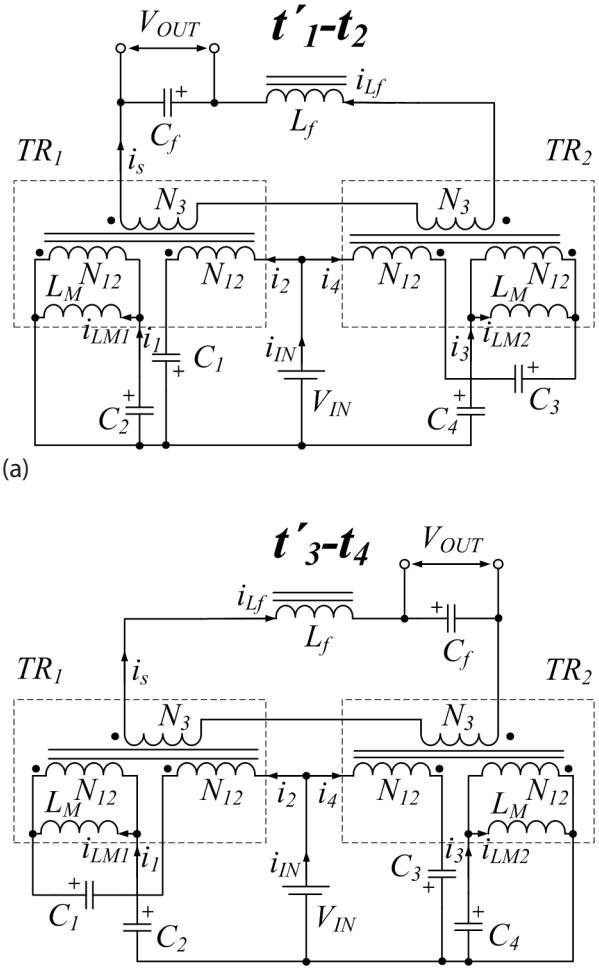

Figure 6: Additional equivalent circuits of the investigated converter for DCM.

Theoretical and simulation results were verified using a 600 W laboratory prototype, which is shown in Fig. 7. It was assembled in compliance with schematics in Fig. 1. Experimental waveforms including the input voltage are presented in Figs. 9 and 11. In the case of 70 V at the input, the converter operates in CCM. For CCM, experimental results are in good agreement with the theoretical assumption. On the other hand, when the input voltage equals 250 V, and the converter operates in DCM, the parasitic parameters in the experimental prototype cause major oscillations. Distinctions between the experimental and simulated waveforms are considerable.

Figure 12 shows experimentally measured curve of active state duty cycle D_A versus input voltage and DC voltage gain for constant output voltage 400 V and output power 600 W. CCM is achieved for input voltage below 150 V DC. Converter operates in DCM when input voltage is higher than 150 V DC. Measured curve has higher non-linearity in DCM, as it was expected.

Table 1: Operating Parameters and Passive Component Values of the Converter

Main operating parameters	Value
Minimal input voltage VIN, min	70 V
Maximal input voltage VIN, max	250 V
Desired output voltage VOUT	400 V
Nominal power P	600 W
Switching frequency fsw=1/T	100 kHz
Turns ratio of the isolation transformers N3:N12	1:1
Passive component values	
Capacitance value of the capacitors C1...C4	60 µF
Magnetizing inductance of the isolation transformers LM	1 mH
Inductance of the filter inductor Lf	1 mH
Capacitance of the filter capacitor Cf	220 µF

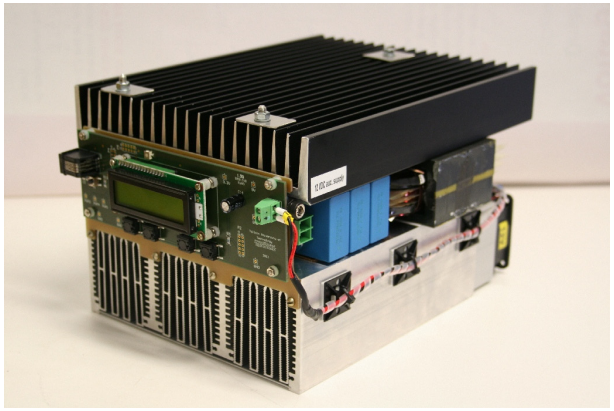

Figure 7: Converter prototype used for experimental verification.

5 Conclusions

The paper has presented a steady state analysis of the operation of the qZS derived push-pull DC/DC converter in the continuous and discontinuous conduction mode. The mathematical analysis provides a general solution for waveforms and values of voltage and current in the passive components. Some differences between the theoretical results and the simulation and experimental results are related to an idealized model (losses in components, leakage inductance are neglected). The converter reveals that the behavior in DCM is complicated. The DCM state duty cycle appears when half of the current ripple through the primary winding, defined by the magnetizing inductance, surpasses an average primary winding current defined by the load power. This mode of operation could occur at the gain factors closer to unity. This topology is a good solution

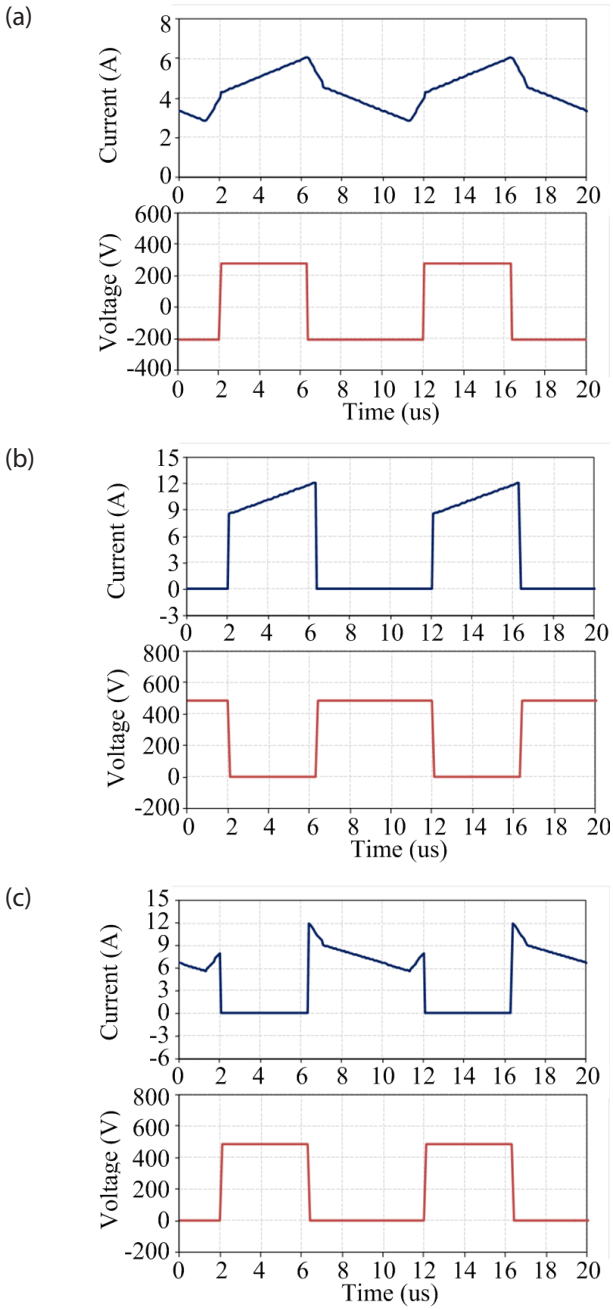

Figure 8: CCM simulated waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 70 V

for the integration of a variable voltage variable speed small wind turbine. In this case the converter operates with a lower gain at a higher power. This condition combined with the features of the converter could ensure operation in CCM in a wide range of power

The mathematical analysis was verified by means of the simulation software and the experimental prototype. As shown, the results are in good agreement with the theoretical predictions.

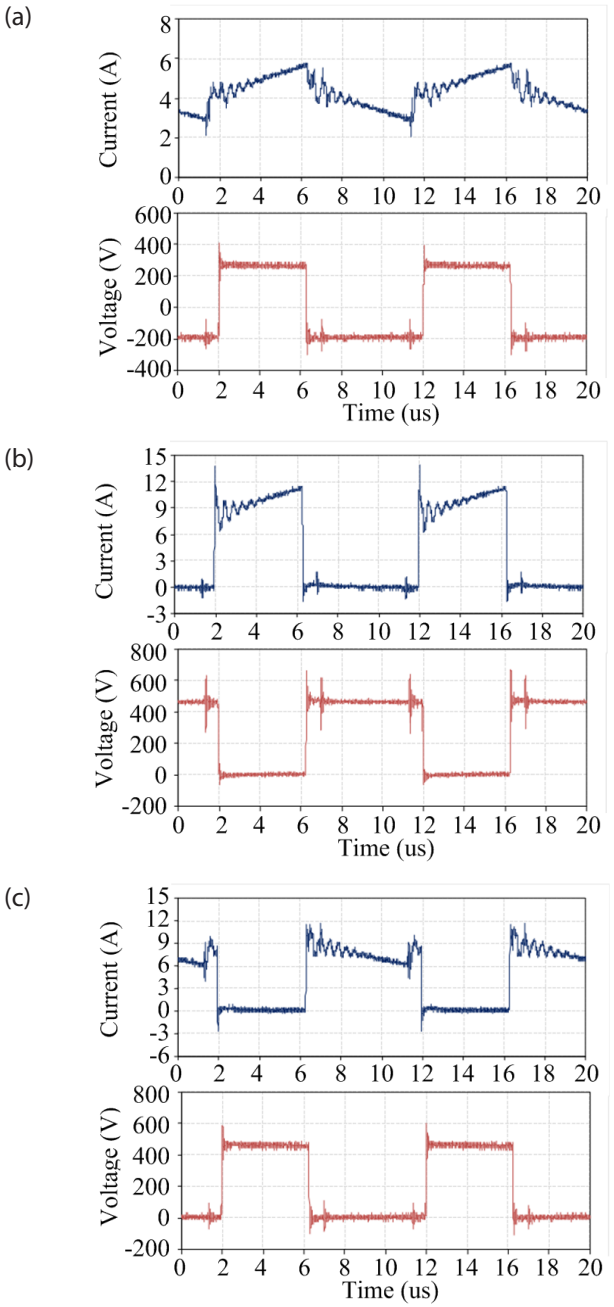

Figure 9: CCM experimental waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 70 V.

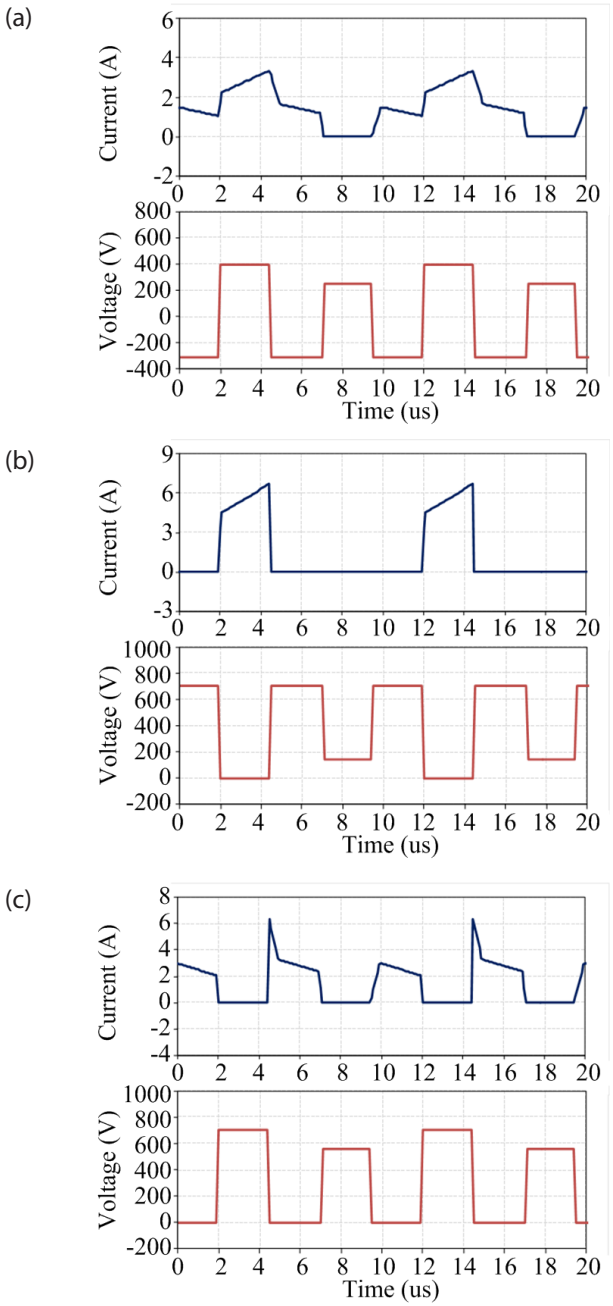

Figure 10: DCM simulated waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 250 V.

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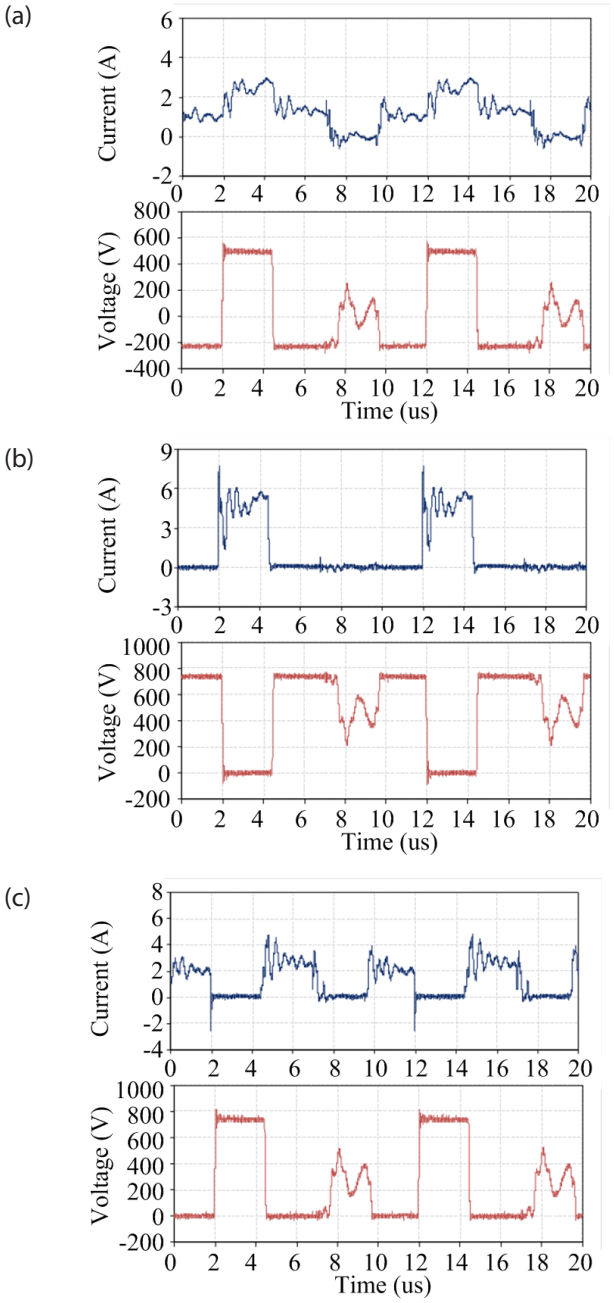

Figure 11: DCM experimental waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 250 V.

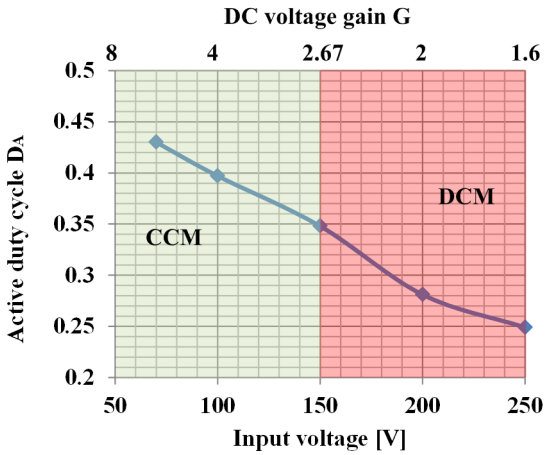

Figure 12: Experimentally measured active state duty cycle D_A versus input voltage and DC voltage gain.

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Sneak path current equivalent circuits and reading margin analysis of complementary resistive switches based 3D stacking crossbar memories

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Abstract: Sneak path currents of resistive memories is an important issue. They increase with increasing memory size and should be minimized for a usable resistive memory. The complementary resistive cells have been suggested as an alternative to one-cell resistive memories to decrease leakage currents. In literature, multilayer resistive memory topologies have also been inspected to minimize leakage currents. Recently, feasibility of 3D resistive RAMs is also inspected. However, to the best of our knowledge, no one has given equivalent leakage circuit models for complementary resistive switches based 3D resistive RAMs yet. In this study, equivalent leakage circuit models for different layers of a 3D resistive RAM with complementary resistive cells have been given and their leakage resistance and reading margins are compared to that of one layer crossbar memory. Some interesting and crucial results are obtained. Alternative complementary resistive switches based 3D resistive RAM topologies with insulating layer(s) for minimized leakage currents are suggested.

Keywords: Complementary Resistive Switches, 3D Multilayer Resistive RAM, Crossbar Memory, Sneak Path Currents.

Nadomestna električna vezja za analizo kvarnih tokov in analiza bralne meje pri komplementarnih uporovnih stikalih na osnovi 3-D večplastnih križnih pomnilnikov

Izvleček: Velik problem uporovnih pomnilnikov predstavljajo kvarni tokovi, ki se, z večanjem pomnilnika, povečujejo. Za zmanjševanje uhajalnih kvarnih tokov so, kot alternativa enoceličnim uporovnim pomnilnikom, predlagane komplementarne uporovne celice. Nadalje lahko v literaturi, za zmanjševanje uhajalnih tokov, zasledimo večplastne uporovne pomnilniške topologije. Trenutno se raziskuje tudi 3D uporovne pomnilnike. Glede na naše znanje, trenutno nihče še ni uspel podati ekvivalentnega vezja za 3D uporovne pomnilnike na osnovi komplementarnih uporovnih stikal. V tem delu je podano ekvivalentno vezje kvarnih uhajalnih tokov za različne plasti 3D uporovnega pomnilnika s komplementarnimi uporovnimi celicami in primerjava uhajalne upornosti ter bralne meje tega koncepta in enoslojnega križnega pomnilnika. Dobljeni so bili zanimivi in odločilni rezultati. Za minimiziranje uhajalnih tokov so predlagani alternativni 3D uporovni pomnilniki s komplementarnimi uporovnimi stikali in izolacijskimi plastmi.

Ključne besede: komplementarna uporovna stikala, 3D večplastni uporovni pomnilniki, križni pomnilniki, kvarni tokovi

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1 Introduction

Resistive switch memories are also memristive devices and they are under consideration for non-traditional memory applications [1 – 3]. Resistive switch memories may help to speed up the booting of computers, reducing their energy consumption and open the way for high density memories. Optimization and minimization of their leakage current and power consumption has emerged as an exciting new research area [4, 5]. Complementary resistive switching (CRS) memories have been suggested to minimize leakage currents in [6, 7]. Multilayer resistive memories are suggested so that the decreased number of cells in the selected layer results in less leakage current. 3D multilayer crossbar array memories are also suggested to maximize memory density [8 – 12]. Previously, 3D multilayer crossbar array memories with CRS cells are considered and their leakage is examined using simulations [10, 11, 13]. However, to the best of our knowledge, no equivalent circuit model for their leakage paths does exist in the literature yet. In this study, for the first time in literature, leakage equivalent circuits of a CRS based 3D Resistive RAM (CB-3D-ReRAM) have been given and leakage resistances and reading margin of one layer and CB-3D-ReRAM leakage currents are compared using the equivalent circuits.

The paper is arranged as follows. In the second section, a CRS cell is briefly explained. In the third section, equivalent leakage circuit of one layer CRS based quadratic memory is given. In the fourth section, the CB-3D-ReRAM is briefly explained and its equivalent circuits for reading a cell at the bottom, the top and middle layers are given. In the fifth section, comparison of leakage resistance and reading margin for different layers of CB-3D-ReRAM to that of a one layer quadratic memory are given using the ratio of the maximum CRS resistance to the minimum CRS resistance when both memories have the same size. In the sixth section, alternative CB-3D-ReRAM topologies with insulating layers are suggested to minimize leakage currents. The paper is finished with conclusion section.

2 Complementary Resistive Switches

Anti-series connected resistive switches are called complementary resistive switches and used to minimize leakage currents in crossbar arrays. A detailed explanation for CRS topology can be found in [6]. The CRS cell model in [6] is also used within this study and redrawn in Figure 1. A resistive switch can be made of a solid electrolyte sandwiched between copper and platinum electrodes as shown in Figure 1.a. The lower resistive switch consists of the copper contact, the bottom solid electrolyte and the bottom platinum contact. The upper resistive switch consists of the upper platinum contact, the upper solid electrolyte and the copper contact. When the CRS is exited by an AC voltage, its zero-crossing hysteresis loop is shown in Figure 1.b.

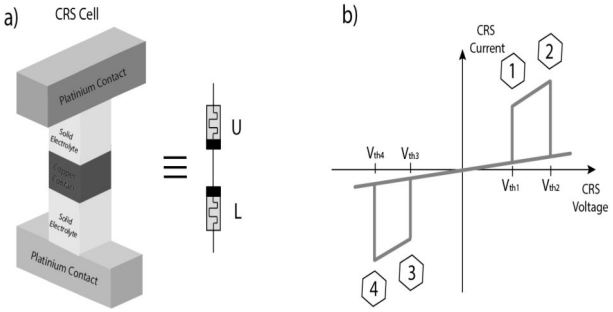

Figure 1: a) The CRS, which is made of the anti - series connected memristive elements or resistive switches U and L, b) Idealized zero crossing current - voltage hysteresis loop of the CRS cell.

If a resistive switch or a memristive element has a high resistance, it is in high resistance state (HRS) and, if it has a low resistance, it is in low resistance state (LRS). When the resistive switch U is in HRS and the resistive switch L is in LRS, the CRS state is logic 0. If the resistive switch U is in LRS and the resistive switch L is in HRS, the CRS state is logic 1. R_{ON} and R_{OFF} are the maximum and the minimum CRS resistances respectively. They are given as

$$R_{OFF} = R_{HRS} + R_{LRS} \tag{1}$$

And

$$R_{ON} = R_{LRS} + R_{LRS} \tag{2}$$

Where
R_{HRS} is the maximum resistance of a CRS switch (either U or L).
R_{LRS} is the minimum resistance of a CRS switch (either U or L).

The maximum CRS resistance, R_{OFF}, is a little higher than R_{HRS} and almost equal to R_{HRS} because of the high ratio between R_{HRS} and R_{LRS}. In [6], it has been shown that, under its threshold voltage, a CRS cell behaves as if a linear resistor with a resistance value of R_{OFF}. When a voltage whose magnitude less than the threshold voltage V_{th1} is applied and it draws a low current and does not switch its state as shown in Figure 1.b.

Reading a CRS cell of logic 1 destroys the cell state and it should be rewritten again [6]. However, the states of the CRS cells in sneak path are not destroyed. Using the CRS model, reading margin and leakage resistance of a

one layer quadratic memory and a CB-3D-ReRAM will be inspected in the next section and the fourth section respectively.

3 The equivalent leakage circuit of a CRS based of one-layer quadratic memory

A CRS based one layer NxN quadratic crossbar memory is shown in Figures 2 and 3. Its equivalent leakage circuit, given in [11,13], is shown in Figure 4. In Figure 4, R_{sel} is the selected cell resistance, R_{pu} is the pull-up resistor, and R_{leak} is the equivalent leakage resistance of one layer crossbar memory. The row number of the memory is designated as N and is equal to the column number of the memory. Equivalent leakage resistance decreases with increasing memory size (N^2) and it is given as

$$R_{Leak} = \frac{(2N-1).R_{OFF}}{(N-1)^2} \tag{3}$$

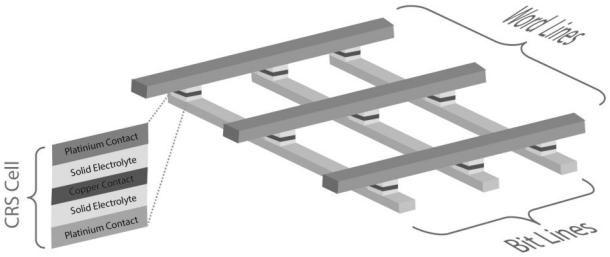

Figure 2: One layer quadratic memory with CRS.

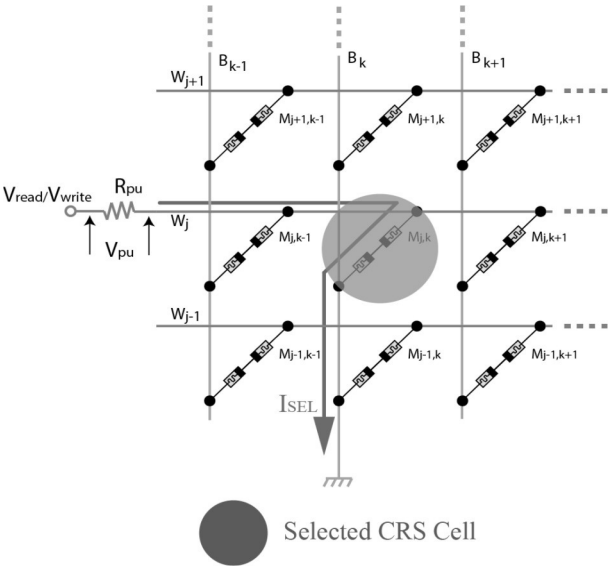

Figure 3: Reading a cell of a CRS based one layer quadratic memory. The reading voltage is applied to the row, W_j, and the column, B_k.

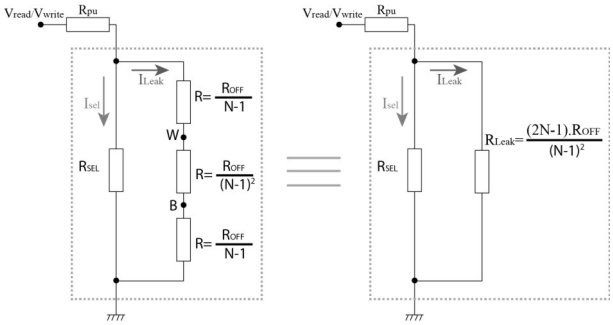

Figure 4: Equivalent circuit of a CRS crossbar array [11,13].

4 A CRS based 3D resistive RAM and its equivalent leakage circuits for different layers

A CB-3D-ReRAM structure is shown in Figure 5. It has L layers. It has either common rows or common columns between adjacent layers. Neighboring layers are constructed in an inverted manner. If only one cell at a layer is read at a time, that the top and the bottom layers shown in Figure 6 must have the same leakage because of symmetry. The equivalent circuit of an L layer CB-3D-ReRAM for reading/writing a cell which is at either the top or the bottom layers is shown in Figure 6. Its leakage resistance is found as

$$R_{Leak} = \frac{(3N-1).R_{OFF}}{(N-1).(2N-1)} \tag{4}$$

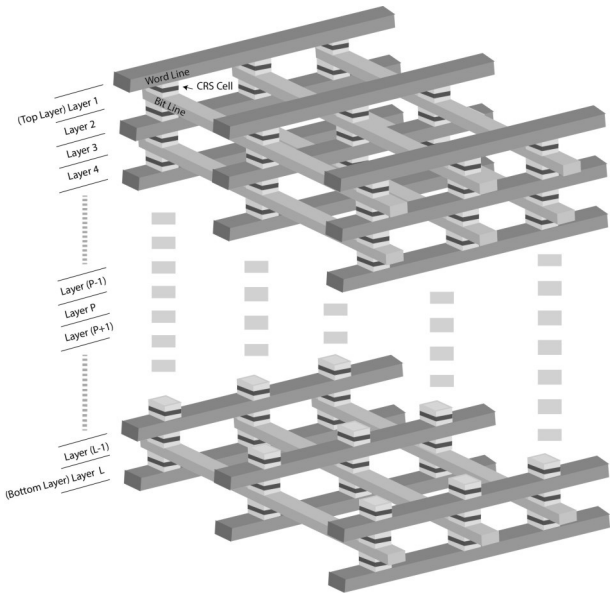

Figure 5: A CB-3D-ReRAM structure.

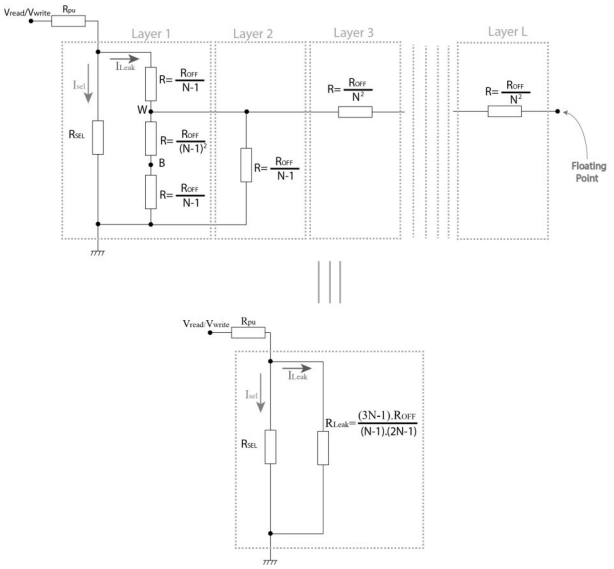

Figure 6: Equivalent circuit of the CB-3D-ReRAM with L layers when a cell at the top or the bottom layer is read / written.

It can be said that the reason of increasing number of layers not increasing sneak-path currents so much is the rest of unselected rows and columns have floating potentials and behave as equipotential surfaces.

If a cell at a middle layer of the CB-3D-ReRAM is read ($2 \le P < L$), its equivalent leakage circuit is shown in Figure 7. Its leakage resistance is found as

$$R_{Leak} = \frac{R_{OFF}}{(N-1)} \tag{5}$$

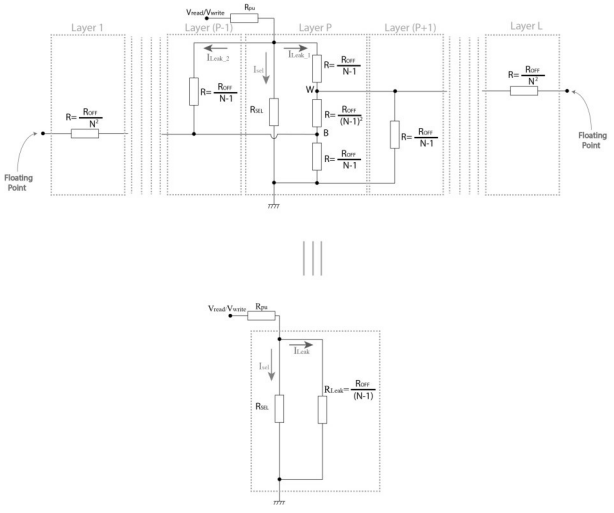

Figure 7: Equivalent circuit of the CB-3D-ReRAM when a cell at layer P, is read. For a middle layer: $2 \le P < L$.

5 Comparison of leakage resistance and reading margin for different layers of the CB-3D-ReRAM to that of one layer quadratic memory

Equivalent leakage circuits of the different layers of the CB-3D-ReRAM are given in the previous section. The equivalent leakage resistances of one layer quadratic memory, the top, the bottom and the middle layers of the CB-3D-ReRAM are calculated and then normalized by the maximum CRS resistance. The normalized leakage resistances are shown in Figure 8. One layer quadratic memory has highest leakage resistance (the least leakage current). The middle layer of CB-3D-ReRAM has the lowest leakage resistance (the worst leakage current). The leakage resistance of the top layer of the CB-3D-ReRAM is same as that of the bottom layer. It is higher than that of a middle layer of the CB-3D-ReRAM and less than that of one layer quadratic memory. If N>>1, Eq. (3) can be approximated as

$$R_{Leak} \cong \frac{2R_{OFF}}{N} \tag{6}$$

If N>>1, Eq. (4) can be assumed as equal to

$$R_{Leak} \cong \frac{3R_{OFF}}{2N} \tag{7}$$

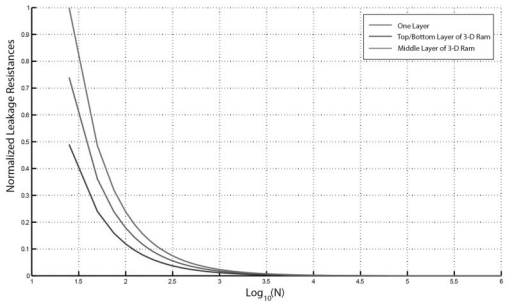

Figure 8: Leakage resistances normalized by the maximum CRS resistance.

If N>>1, Eq. (7) is only 25% less than the leakage resistance of one layer quadratic memory with CRS of the same size. V_{pu}, which is the voltage across the pull-up resistor R_{pu}, can be found as

$$V_{pu} = \frac{R_{pu}}{R_{pu} + R_{leak} // R_{sel}} V_{read} \tag{8}$$

In this study, the pull-up resistor is chosen to be equal to R_{ON} and the reading margin is defined as

$$\Delta V = \frac{V_{min} - V_{max}}{V_{read}} \quad (9)$$

Where
V_{min} is the voltage across the pull-up resistor R_{pu} when the cell has minimum resistance.
V_{max} is the voltage across the pull-up resistor R_{pu} when the cell has maximum resistance.
V_{read} is the reading voltage.

Reading margins of an NxN one layer quadratic memory and the top/the bottom layer and a middle layer of an NxN CB-3D-ReRAM are calculated shown in Figure 9. The ratio of the maximum CRS resistance to the minimum CRS resistance, R_{OFF}/R_{ON} is used as a parameter for all the drawings to show that both the reading margin and the leakage resistance go up when R_{OFF}/R_{ON} increases. For the same size, one layer quadratic memory has the highest (the best) reading margin, the reading margin of a middle layer of the CB-3D-ReRAM has the worst reading margin, the reading margin of the top layer of the CB-3D-ReRAM is same as that of the bottom layer of the CB-3D-ReRAM and it is higher than that of a middle layer and less than that of one layer quadratic memory. After all, if the same memory size is divided into layers, the CB-3D-ReRAM becomes advantageous. As an example, the memory size is chosen to be 4 Mbit for both the CB-3D-ReRAM and one layer quadratic memory. The layer numbers of the CB-3D-ReRAM can be chosen to be 4, 16, and 64. As a function of the layer numbers, the reading margins are shown in Figure 10. The leakage resistances normalized by the maximum top layer leakage resistance are shown in Figure 11. Increasing the layer number results in a less leakage current for the CB-3D-ReRAM than that for one layer quadratic memory or a higher leakage resistance than that for quadratic memory for the same memory size as shown in Figure 11, the CB-3D-ReRAM shows a better performance for the same memory size but it is difficult to construct. On the other hand, it would increase both reading margin and leakage resistance, it is not practical to make the layer number higher than necessary considering manufacturing difficulties and cost issues. Accordingly, for the same memory size, it could be preferable to choose the number of layers of the CB-3D-ReRAM is 4 instead of 16 or 64.

6 Alternative CB - 3D - ReRAM Topology Suggestions

Based on the findings of the last sections, alternative CB-3D-ReRAM topologies with insulating layer(s) can be suggested considering that insulating layers are going to less expensive in the future. Since the top and the bottom layers have higher equivalent leakage resistance than the middle layers with only one cell selected for reading, the number of the middle layers must be minimized for less leakage current during

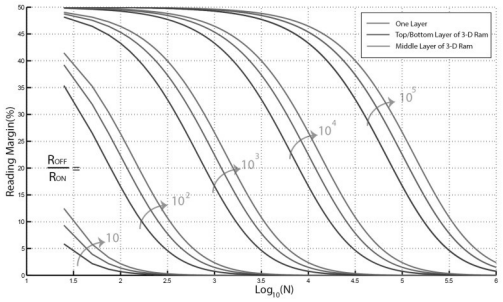

Figure 9: Reading margins of the top or the bottom layer of the CB-3D-ReRAM, a middle layer of the CB-3D-ReRAM, and a one layer quadratic memory.

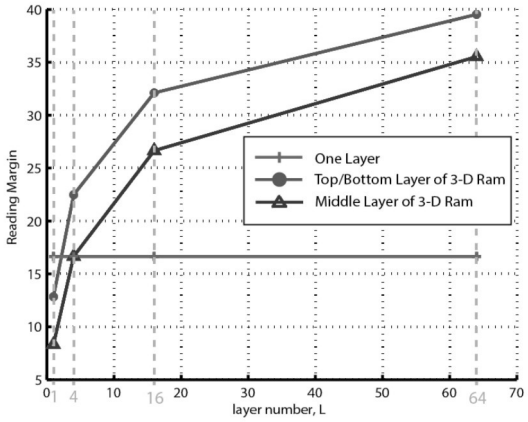

Figure 10: Reading margins of the CB-3D-ReRAM layers and one layer quadratic memory for the memory size,N^2,= 4 Mbit and R_{OFF}/R_{ON}=1000.

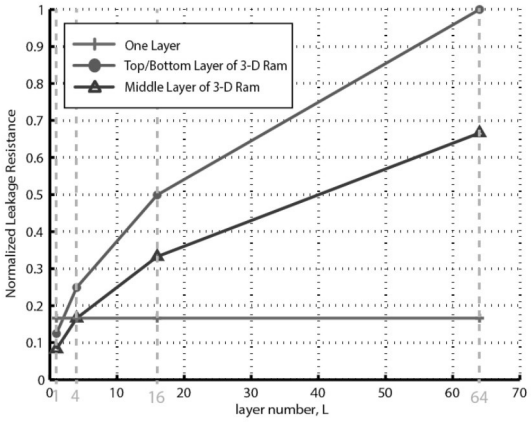

Figure 11: Normalized leakage resistances of the CB-3D-ReRAM layers and one layer quadratic memory when the memory size, N^2, = 4 Mbit and R_{OFF}/R_{ON}=1000.

operation. The suggested new topologies are shown in Figures 12–14. The 3D RAM topology seen in Figure 12 is obtained placing one insulating layer after every other two layers, there is one insulating layer between two layers. As a result, it has the lowest leakage during its operation since it does not have any middle layers. Still, it needs insulating layers whose number are almost half of the crossbar layers and it might be the most expensive to produce among the topologies shown in Figures 12–14.

The 3D RAM topology seen in Figure 13 is obtained placing one insulating layer after every other three layers, there is one insulating layer between three layers. For it has only one middle layer, its leakage current increases if the middle layer is read or written. Otherwise, its leakage is same as that of the topology given in Figure 12. If the topology is used, it has less insulating layers than that of the one in Figure 12 for a high number of crossbar layers. However, it has a higher leakage current with a probability of 1/3. The 3D RAM topology seen in Figure 14 is obtained placing one insulating layer after every other four layers, there is one insulating layer between four layers. Since it has only two middle layers, its leakage current increases if the middle layers are read or written. Otherwise, its leakage current is same as that of the topology given in Figure 12. If the topology is used, it has the least insulating layer among the ones given in Figures 12–14 for a high number of crossbar layers. Yet, it has a higher leakage current with a probability of 1/2.

If the technique to make insulating layers become easier and less expensive, the results of the analyses done in this study can be used to develop new CB-3D-ReRAM topologies with less leakage current and higher reading margin.

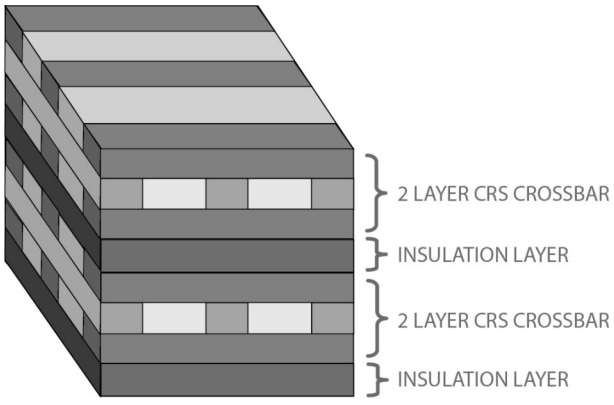

Figure 12: An alternative topology obtained placing one insulating layer after every other two layers, there is one insulating layer between two layers.

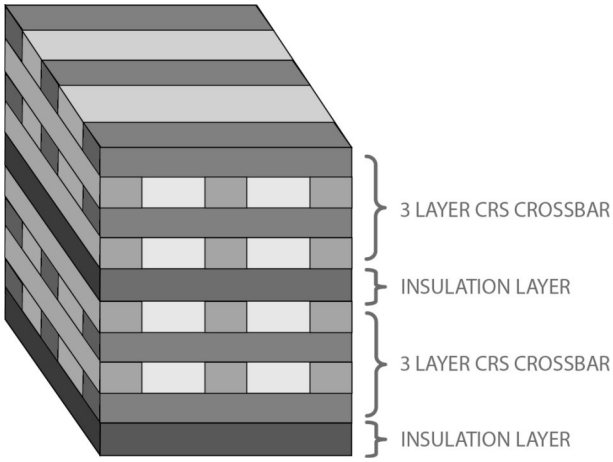

Figure 13: An alternative topology obtained placing one insulating layer after every other three layers, there is one insulating layer between three layers.

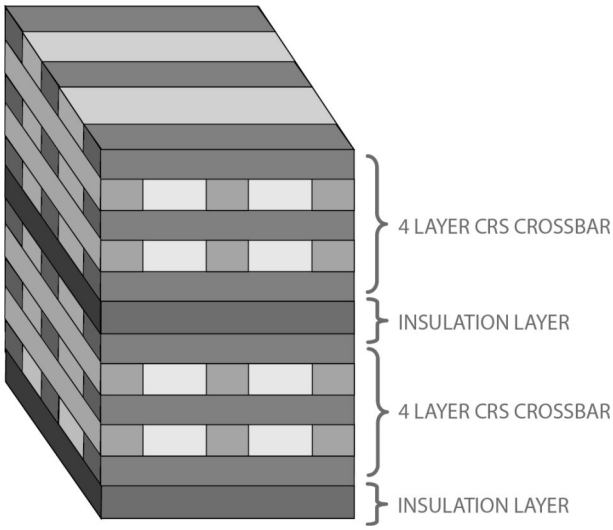

Figure 14: An alternative topology obtained placing one insulating layer after every other four layers, there is one insulating layer between four layers.

7 Conclusion

Leakage resistances of different layers of a CB-3D-ReRAM are examined using the equivalent circuits. It has been found that reading a cell at the top or the bottom layers of the CB-3D-ReRAM results in less leakage current than reading a cell at middle layers of the CB-3D-ReRAM. Leakage currents are same for all middle layers of the CB-3D-ReRAM. Leakage current of an NxN one layer quadratic memory is less than that of an L layer NxN CB-3D-ReRAM. However, the L layer memory array has less leakage current than a one layer quadratic memory for the same memory size when the layer number is more than or equal to four. Results show that the CB-3D-ReRAM for the same memory size and using

just a few layers is a promising candidate for the future memories.

Alternative CB-3D-ReRAM topologies with insulating layers are also suggested to minimize leakage currents during operation and they have less leakage current than the CB-3D-ReRAM examined at first. Besides, if the technique to make the insulating layers becomes cheaper, perhaps, the alternative topologies given in this paper can be used in the future CB-3D-ReRAMs.

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A New FGMOS FDCCII and Filter Applications

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Abstract: In this work, a new floating gate MOS (FGMOS) fully differential difference current conveyor (FDCCII) is presented. Employing FGMOS transistors two important advantages are introduced compared to conventional CMOS structure; firstly the input stage of the circuit providing the arithmetic calculations gets simpler, secondly the linearity range increases due to the properties of FGMOS differential amplifier. Furthermore, the versatility of the proposed FGMOS FDCCII is demonstrated on a filter circuit example. Both the FGMOS FDCCII circuit and proposed filter circuit are simulated with SPICE simulation program by using 0.35μm technology parameters. Simulation results show that the proposed building block can be used for the design of filters with high linearly properties.

Keywords: FGMOS, FDCCII, Biquad Filter, Analog Integrated Circuits

Nove možnosti uporabe FGMOS FCCII in filtrov

Izvleček: V članku je predstavljen nov diferencialni MOS ojačevalnik s plavajočimi vrati (FGMOS). V primerjavi s klasično CMOS strukturo ima FGMOS dve prednosti: enostavnejša vhodna stopnja aritmetičnih izračunov in izboljšana linearnost zaradi lastnosti FGMOS ojačevalnika. Vsestranskost predlaganega FGMOS FDCCII vezja je predstavljena na primeru filtra. FGMOS FDCCII in vezje filtra sta simulirana v SPICE okolju v 0.35μm tehnologijo. Simulacije nakazujejo, da je predlagana struktura uporabna za načrtovanje filtrov z visoko linearnostjo.

Ključne besede: FGMOS, FDCCII, biquad filter, analogna integrirana vezja

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1 Introduction

Designing circuits suitable for differential signals leads to have more versatile applications. There are lots of filter topologies in electronics literature employing the extensions of second generation current conveyor like differential difference current conveyor (DDCC) [1-2], differential voltage current conveyor (DVCC) [3-4], inverting current conveyor (ICCII) [5], current controlled conveyor (CCCII) [6-7] and dual-X current conveyor (DXCCII) [8].

Current conveyors are one of the most useful building blocks in analog design. Many efficient applications can be designed with success using CCII as basic component. Anyway, second generation current conveyors, as they have been proposed, show some drawbacks. For example, only one of the input terminals presents a high impedance level. This can be a problem if differential signals have to be handled. To overcome this, a solution using more CCIIs has been proposed [9].

A different approach can be that to implement more complicated basic blocks, one of which will be presented in this paper.

Fully differential difference current conveyor (FDCCII) may be considered as the most versatile building block that can be designed starting from the basic CCII. In fact, its topology can be thought as the "natural differential evolution" of the CCII idea. FDCCII circuit block combines the advantages and versatility of DDCC and DXCCII together. It has arithmetic signal processing capability of DDCC and gives opportunity to design filters with electronically tunable characteristics by utilizing two X terminals that is similar to DXCCII.

FGMOS structures are also known as multi-input MOS and their multi input advantages make it simpler to realize an arithmetic signal processing circuit. The FGMOS drain current is proportional to the square of the weighted sum of the input signals. In the last few years,

FGMOS transistors have found many applications in electronic programming [10], Op-amp offset compensation [11], D/A and A/D converters [12], inverters and amplifiers [13], voltage attenuators [14], current mirrors [15] and low voltage analog circuits [15]. Recently, an increased number of publications on the use of the FGMOS in analog computational circuits have been reported voltage squarers and multipliers [16-19].

In this paper, a new FGMOS FDCCII is proposed to obtain flexibility in analog IC design. By using FGMOS transistors the input stage of the circuit providing the arithmetic calculations gets simpler, also the linearity range increases due to the properties of FGMOS differential amplifier. The proposed FGMOS FDCCII is used in a filter circuit to demonstrate the versatility of the FDCCII block. Both the FGMOS FDCCII circuit and proposed filter circuit are simulated with SPICE simulation program by using 0.35um technology parameters. Simulation results show that the proposed circuit building block can be used to design filters with linearly tunable characteristics.

Rest of the paper is organized as follows. In Section II, the basic structure of the FGMOS transistor is described. The principle of operation of the FGMOS FDCCII and simulation results of the proposed circuit are presented in Section III and Section IV, respectively. Proposed filter circuit, as an application example, is shown in section V followed by conclusion in section VI.

2 The FGMOS transistor

Floating gate (FG) MOSFETs are being utilized in a number of new and exciting analog applications [17-20]. These devices are available in standard CMOS technology because they are being widely used in digital circuits. Thus floating gate devices are now finding wider applications by analog researchers. As a result, the floating gate devices are not only used for memories but are also being used as circuit elements. FGMOS transistors are used as analog memory elements, as part of capacitive biased circuits, and as adaptive circuit elements [20].

An FGMOS can be fabricated by electrically isolating the gate of a standard MOS transistor, so that there are no resistive connections to its gate. A number of secondary gates or inputs are then deposited above the floating gate (FG) and electrically isolated from it. These inputs are only capacitively connected to the FG, since the FG is completely surrounded by highly resistive material. So, in terms of its DC operating point, the FG is a floating node [20]. The equivalent schematic for an n-input n-channel FGMOS transistor is given in Figure 1.

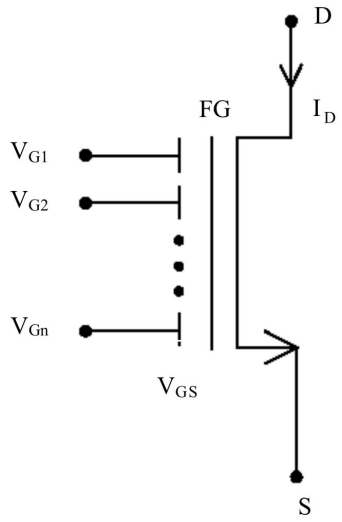


Figure 1: n-input n-channel FGMOS transistor

3 FGMOS FDCCII

Starting from the first and second generation current conveyors, many types of new topologies have been designed during the past years. FDCCII is one of the most versatile circuit blocks which presents flexibility in analog circuit design with its arithmetic signal processing capability and gives opportunity to electronically tunable characteristics in application examples.

3.1 FDCCII Circuit Building Block

FDCCII is characterized by four high-impedance input terminals (Y_1, Y_2, Y_3 and Y_4), two low-impedance node (X_1 and X_2) and four high-impedance output nodes (Z_1, Z_2, $Z_{1'}$ and $Z_{2'}$). Its block scheme and matrix characteristics are summarized below.

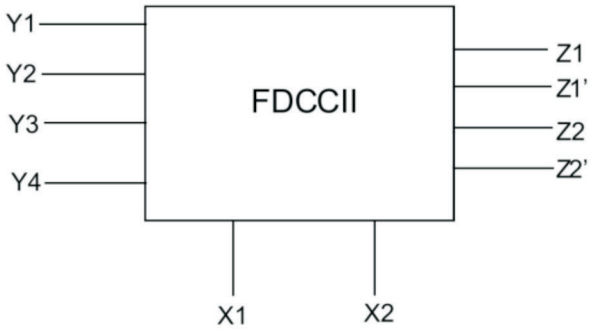


Figure 2: FDCCII block representation

$$\begin{bmatrix} V_{X1} \\ V_{X2} \\ I_{Y1,2,3,4} \\ I_{Z1,Z1'} \\ I_{Z2,Z2'} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \pm 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & \pm 1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{X1} \\ I_{X2} \end{bmatrix} \quad (1)$$

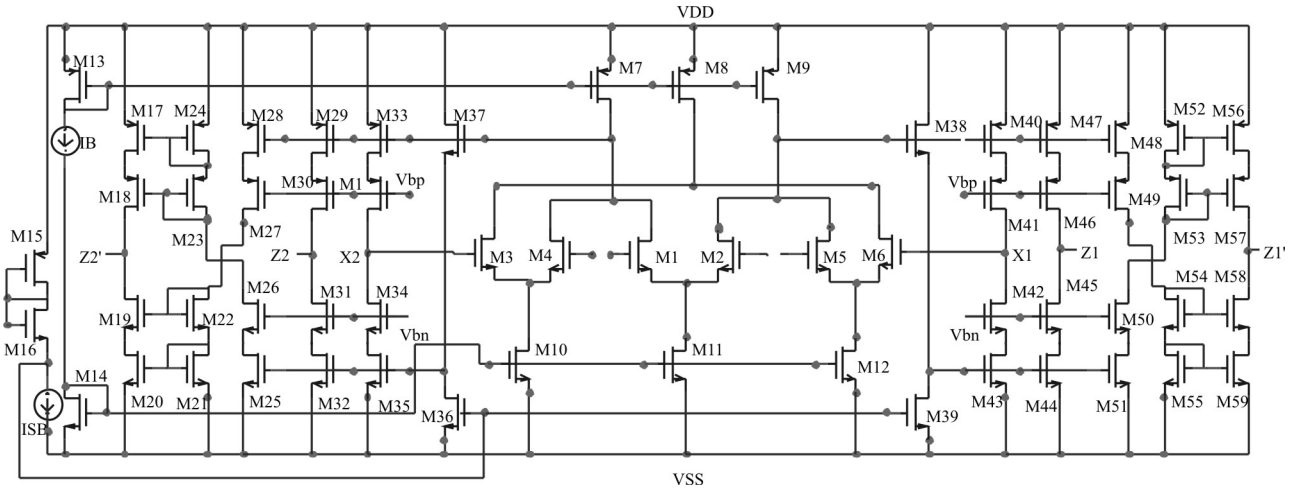
3.2 FGMOS FDCCII

Fig. 3a shows the CMOS FDCCII circuit while Fig. 3b shows the proposed floating gate fully differential difference current conveyor circuit employing FGMOS differential pairs instead of conventional MOS pairs to improve the circuit behavior. CMOS FDCCII circuit given in [21] employs three differential pairs in order to get the relationship of $V_{X1} = V_{Y1} - V_{Y2} + V_{Y3}$ and $V_{X2} = - V_{Y1} + V_{Y2} - V_{Y4}$. In FGMOS FDCCII circuit given in Fig. 3 only two FGMOS differential pairs are used to get both $V_{X1} = V_{Y1} - V_{Y2} + V_{Y3}$ and $V_{X2} = - V_{Y1} + V_{Y2} - V_{Y4}$. It is clearly seen that by using FGMOS transistors both the input stage of the circuit providing the arithmetic calculations gets simpler also the linearity range increases due to the properties of FGMOS differential amplifier [20]. In addition to these, new Y nodes can be added to FGMOS FDCCII circuit without any new transistors by only increasing the inputs of FGMOS transistors already used in differential pairs. This also reveals the flexibility of using FGMOS transistors in circuit blocks employing arithmetic calculations.

FGMOS transistors in differential pairs have three inputs which are applied through equal sized capacitors, Ci. The input signals of V_{Y1}, V_{Y2}, V_{Y3} and the control voltage V_C are applied to one of the floating gates in the differential pairs. Since the voltage at the gate is less than the input voltage the differential pair transistors can work in saturation even when large signals are applied. This leads to increase the input dynamic swing.

Determining parameters of voltage and current conveying properties are the slopes of related transistors and it is achieved easily by choosing matched transistors.

Impedance values of X, Y, Z nodes of the FGMOS FDCCII circuit can be seen as small at X node because of feedback and high at Z nodes because of the drain nodes of related transistors.



Figre 3a: CMOS FDCCII circuit

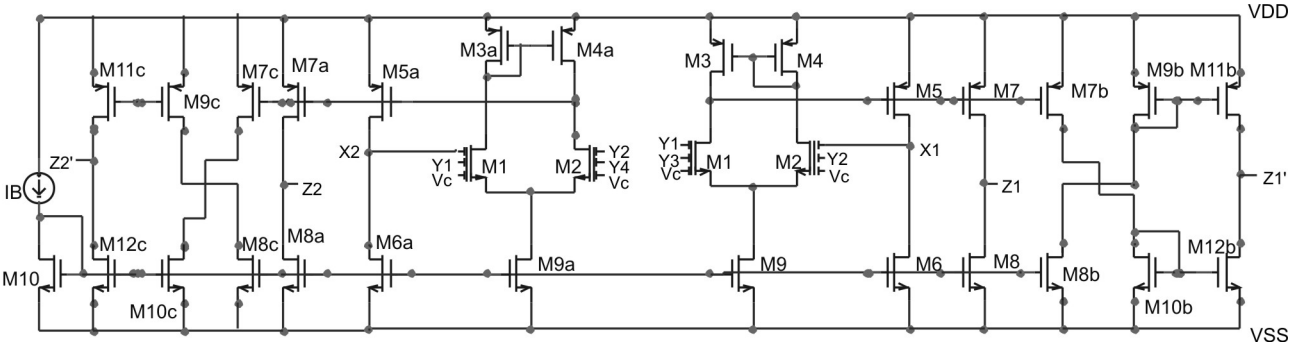


Figure 3b: FGMOS FDCCII circuit

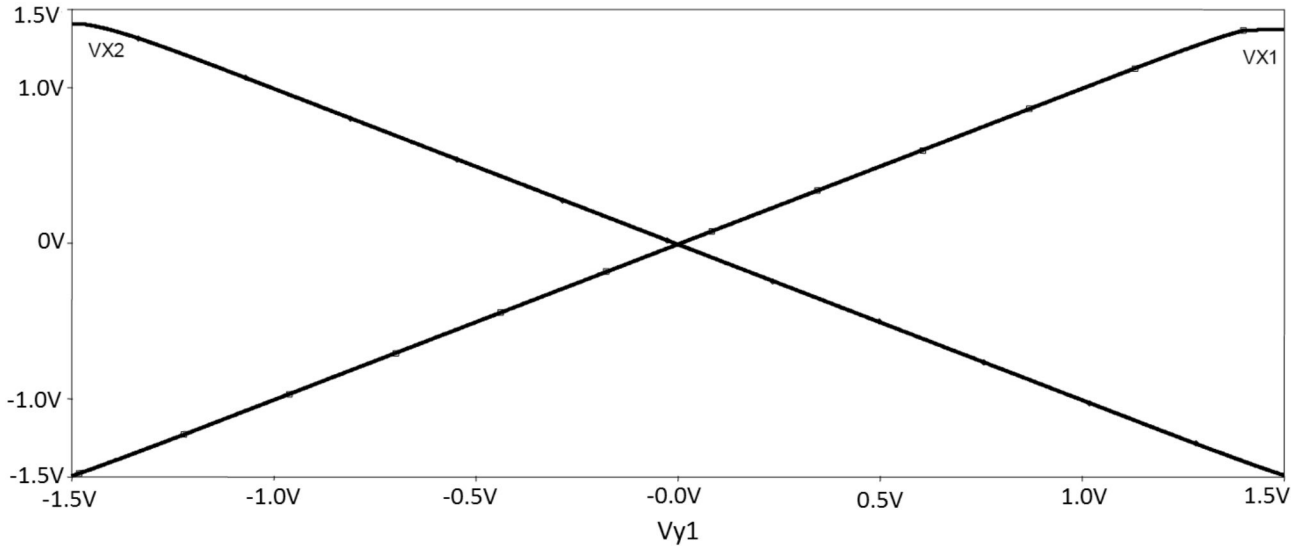


Figure 4: FGMOS FDCCII DC voltage transfer characteristics (V_{X1}-V_{Y1} and V_{X2}-V_{Y1})

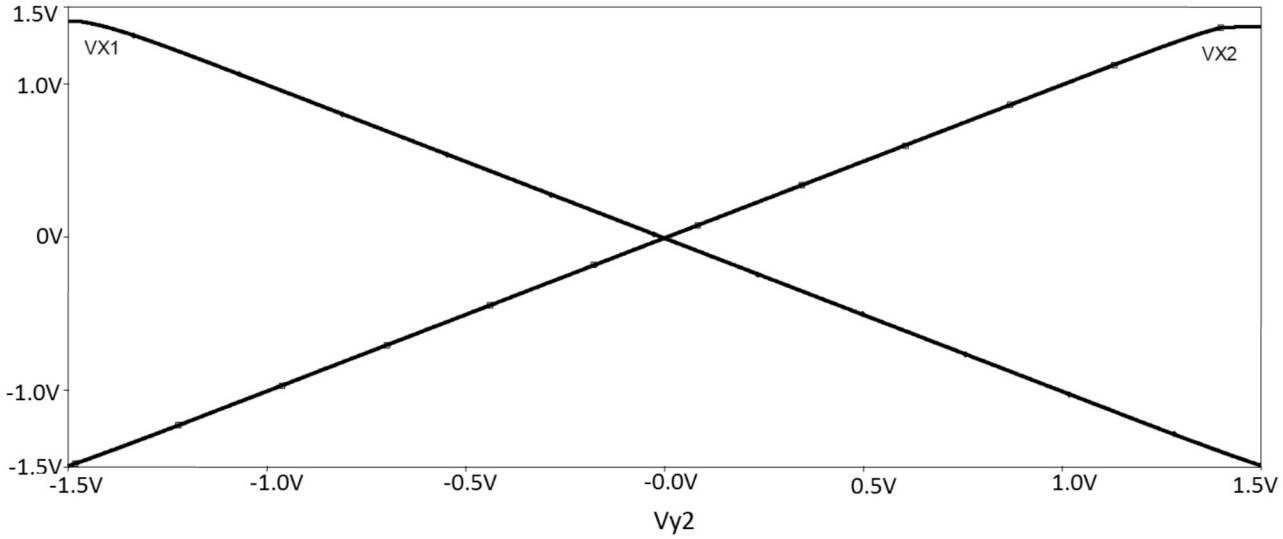


Figure 5: FGMOS FDCCII DC voltage transfer characteristics (V_{X1}-V_{Y2} and V_{X2}-V_{Y2})

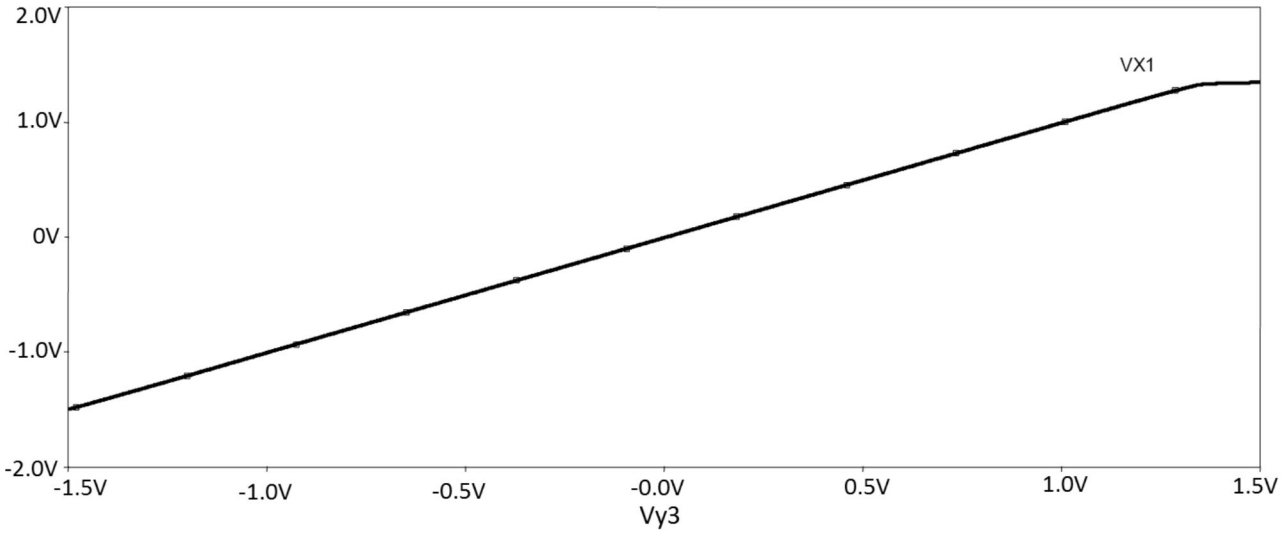


Figure 6: FGMOS FDCCII DC voltage transfer characteristics (V_{X1}-V_{Y3})

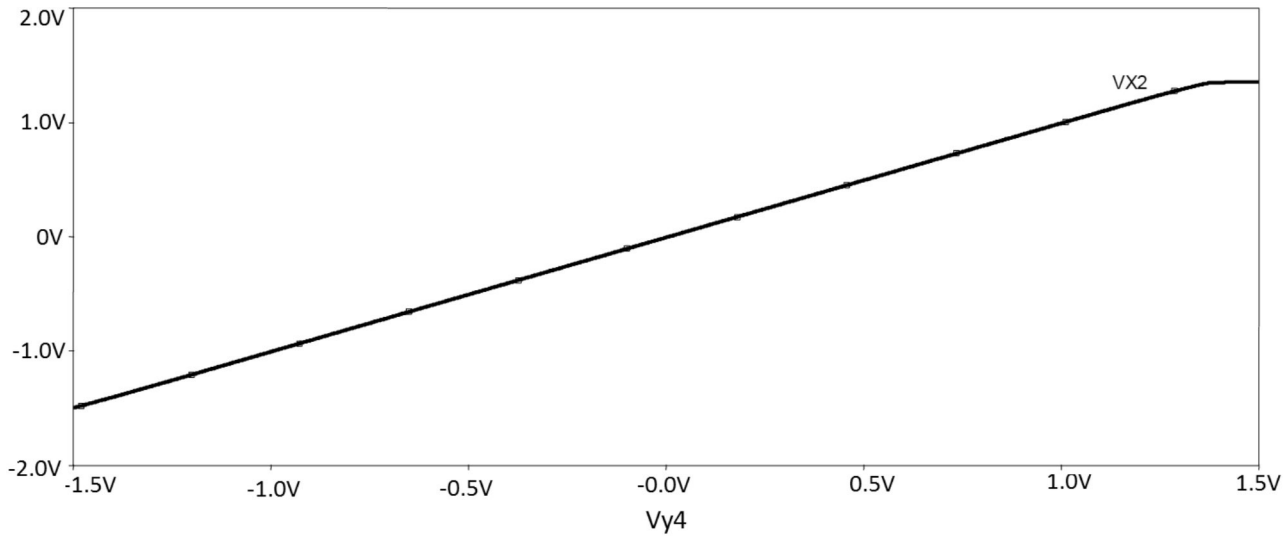


Figure 7: FGMOS FDCCII DC voltage transfer characteristics (V_{X2}-V_{Y4})

4 Simulation results

The proposed circuit of Fig. 3 is simulated with SPICE by using 0.35µm TSMC technology parameters. The supply voltages are ±1.5V, V_C is set to V_{DD} and bias current I_B = 10µA. The input capacitor values are taken C_i= 16,25fF while the C_{FGD} and C_{FGS} values are calculated as 0.2fF and 1.63fF, respectively. The dimension for n-type transistors is W / L = 0.7µm / 0.7µm and for p-type transistors is W / L = 1.4µm / 0.7µm.

Fig. 4, Fig. 5, Fig. 6 and Fig. 7 show the DC voltage transfer characteristics of the proposed circuit with respect to $V_{Y1, Y2, Y3, Y4}$ input DC voltages. DC voltage $V_{Y1, Y2, Y3, Y4}$ is swept between -1.5V and 1.5V while the DC voltage $V_{X1, X2}$ is plotted.

In Fig. 5, Fig. 6 and Fig. 7 while V_{Yi} is -1.5V, VX1 and VX2 take -1.49V and 1.4V, respectively. While V_{Yi} is 1.5V, V_{X1} and V_{X2} take 1.4V and -1.49V, respectively. As it is seen from these values, input swing is almost equal to the supply voltages.

Fig. 8 shows the DC voltage transfer characteristics of the proposed FGMOS circuit and the CMOS circuit [21] together. V_{X1} is plotted for both circuits. As it is seen from the figure, input swing is increased by using FGMOS transistors.

Fig. 9 and Fig. 10 show the DC current transfer characteristics of the proposed circuit with respect to I_B bias current. DC bias current I_B is swept between -10µA and 10µA while the DC output currents $I_{Z1,Z1',Z2,Z2'}$ are plotted.

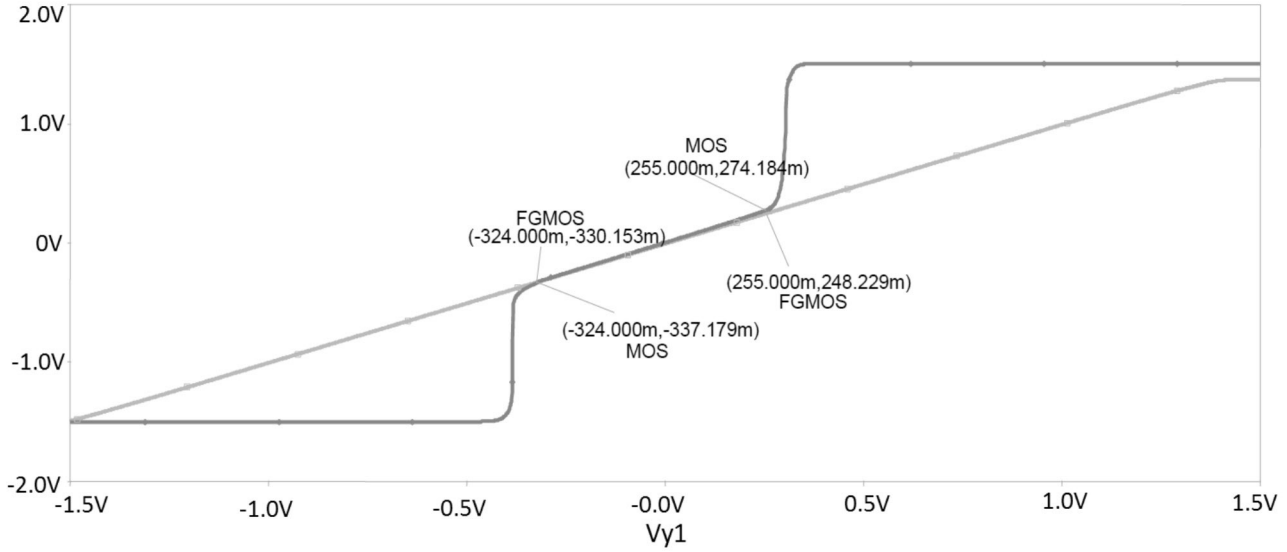


Figure 8: DC voltage transfer characteristics of the proposed FGMOS circuit and CMOS circuit

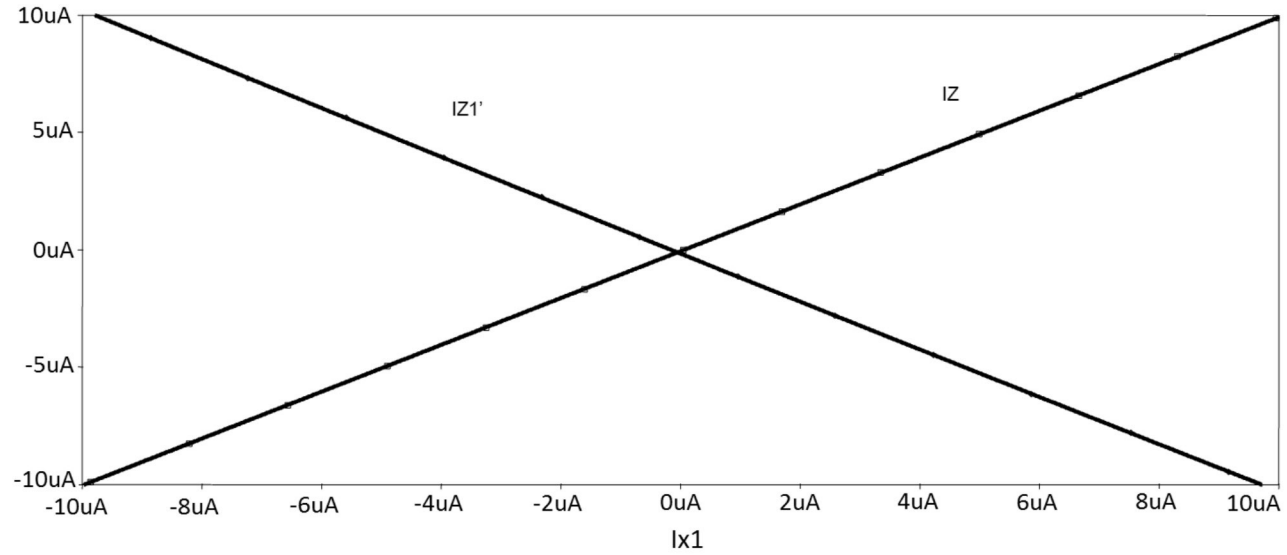


Figure 9: FGMOS FDCCII DC current transfer characteristics

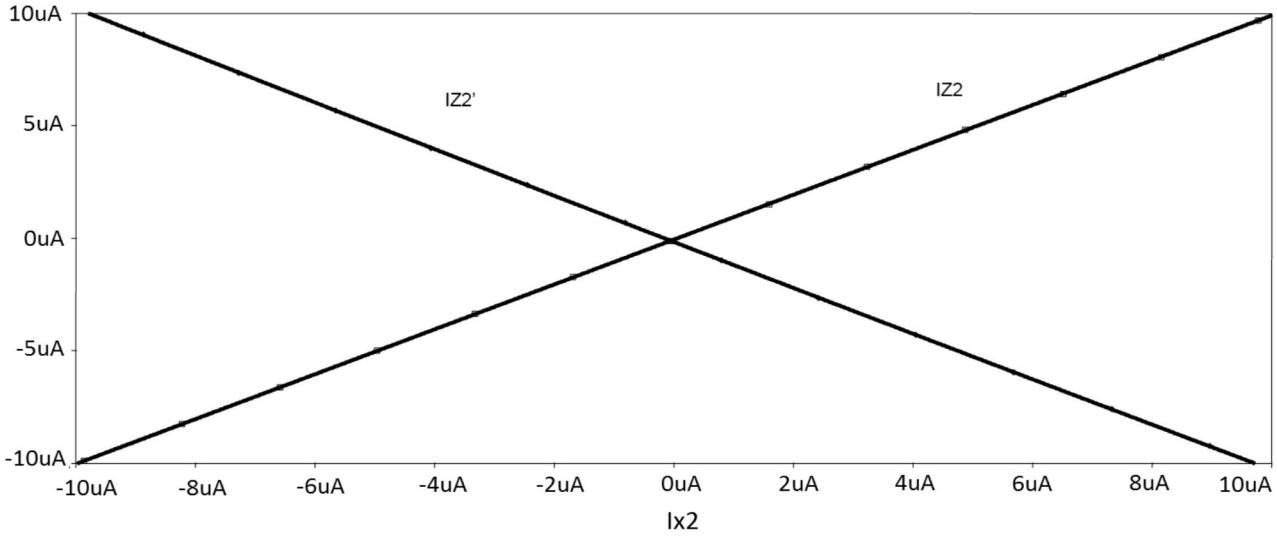


Figure 10: FGMOS FDCCII DC current transfer characteristic

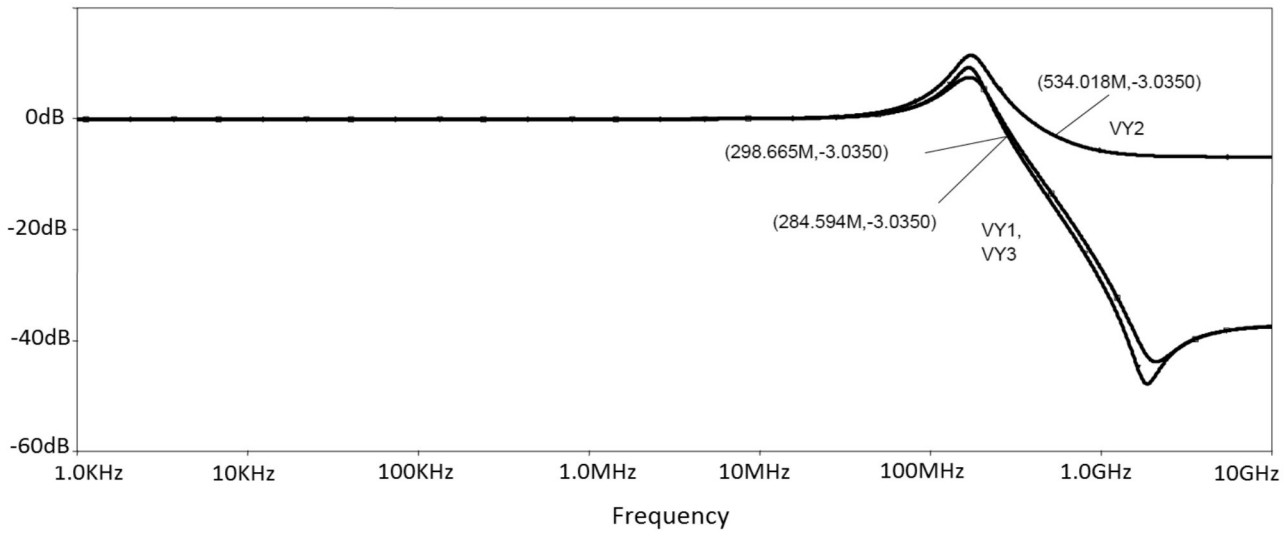


Figure 11: FGMOS FDCCII AC voltage transfer characteristics (V_{X1}-$V_{Y1, Y2, Y3}$)

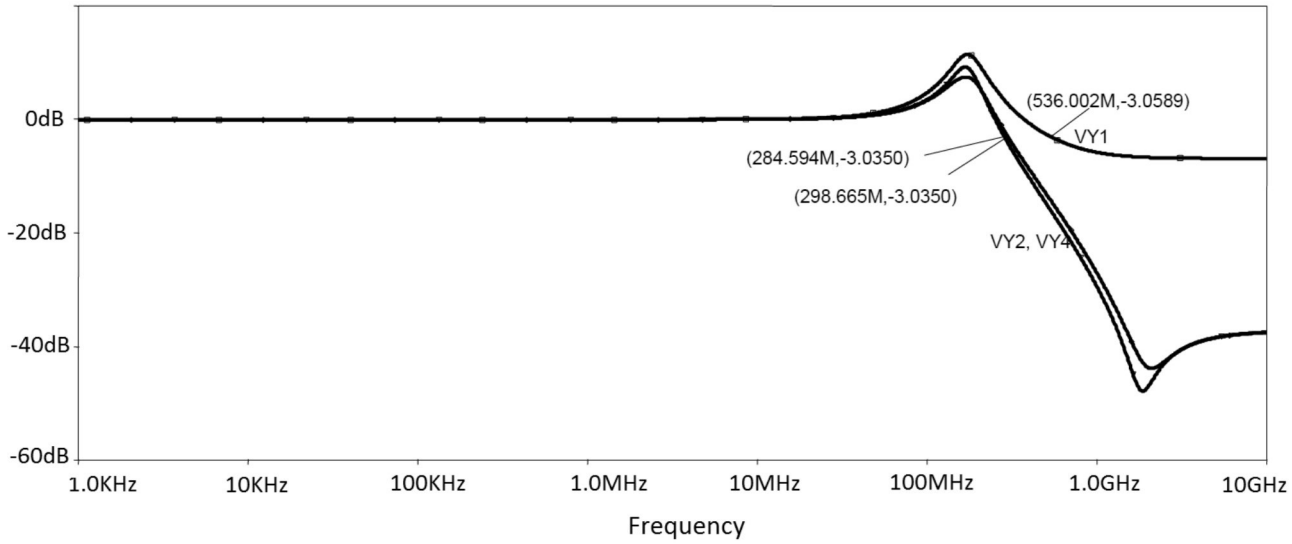


Figure 12: FGMOS FDCCII AC voltage transfer characteristics (V_{X2}-$V_{Y1, Y2, Y4}$)

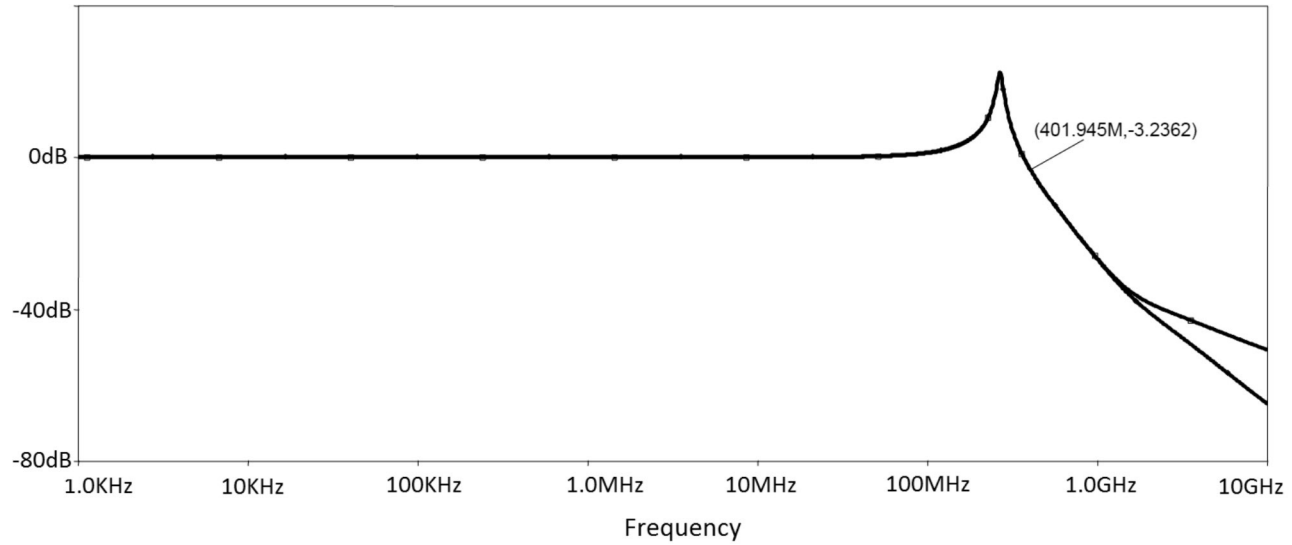


Figure 13: FGMOS FDCCII AC current transfer characteristics

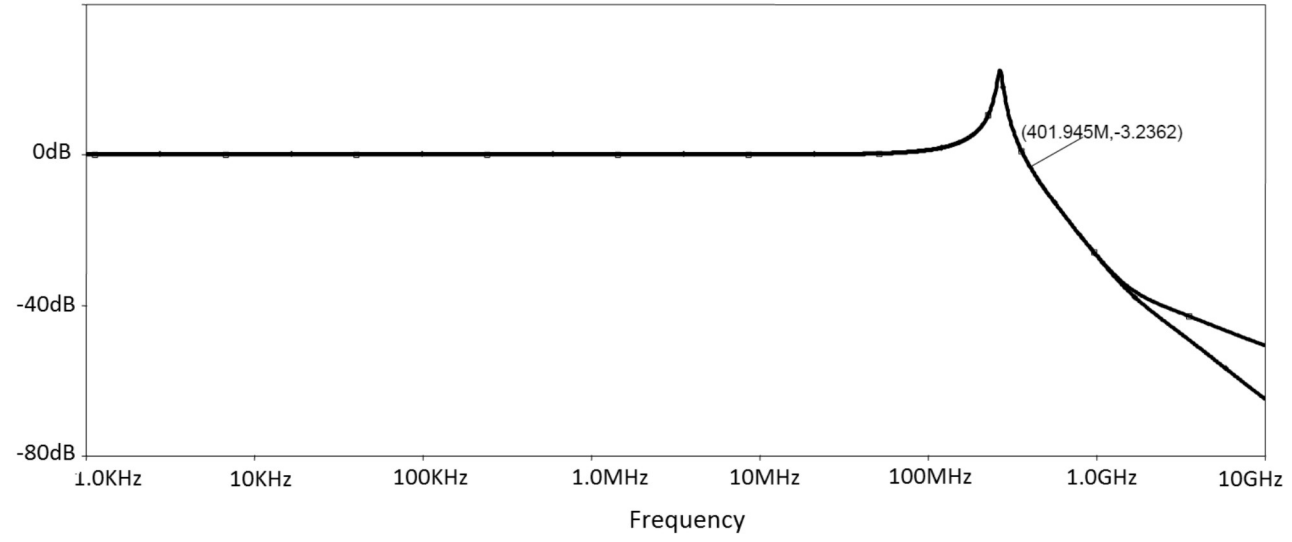


Figure 14: FGMOS FDCCII AC current transfer characteristics

Fig. 11 and Fig. 12 show the AC voltage transfer characteristics of the proposed circuit with respect to $V_{X1, X2}$ and $V_{Y1, Y2, Y3, Y4}$.

Fig. 13 and Fig. 14 show the AC current transfer characteristics of the proposed circuit with respect to $I_{X1, X2}$ and $I_{Z1, Z2, Z1', Z2'}$.

Impedance values of X1, X2, Y1, Y2, Y3 and Z nodes have been also determined as 1.46kΩ, 1.78kΩ, 1.43TΩ, 1.36TΩ, 1.43TΩ and 1.57MΩ, respectively. We considered V_{X1} (output) against V_{Y1}(input) at 10 MHz for THD (Total Harmonic Distortions) analysis. Fig.15 shows the THD variation of the proposed FGMOS circuit and the conventional CMOS circuit together during the input voltage swing of V_{Y1} change between 1mV and 400mV which is common input voltage gap for FGMOS and CMOS circuits.

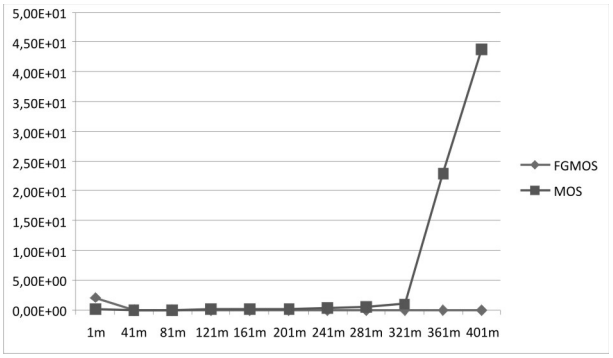


Figure 15: Total harmonic distortion (THD) values of the proposed FGMOS FDCCII and MOS FDCCII

5 Proposed filter as application example

In this section, current-mode and voltage mode two biquad filters have been presented. First proposed circuit is current-mode a biquad filter with single-input and three-outputs, which can simultaneously realize current mode low-pass, band-pass and high-pass filter responses employing all grounded passive components. The second proposed is voltag- mode biquad filter with three-inputs single-output, which can realize current mode low-pass, band-pass, high-pass, band-stop and all-pass filter responses employing single FDCCII.

The proposed current-mode filter is shown in Fig.16. Routine analysis of these circuits, which single-input three-output yields the following current-mode filter transfer functions:

$$\frac{I_{BP1}}{I_{IN}} = \frac{C_2 G_1 s}{G_1 G_2 + C_2 G_1 s + C_1 C_2 s^2} \quad (2)$$

$$\frac{I_{BP2}}{I_{IN}} = \frac{C_2 G_1 s}{G_1 G_2 + C_2 G_1 s + C_1 C_2 s^2} \quad (3)$$

$$\frac{I_{HP}}{I_{IN}} = \frac{C_1 C_2 s^2}{G_1 G_2 + C_2 G_1 s + C_1 C_2 s^2} \quad (4)$$

$$\frac{I_{LP}}{I_{IN}} = \frac{G_1 G_2}{G_1 G_2 + C_2 G_1 s + C_1 C_2 s^2} \quad (5)$$

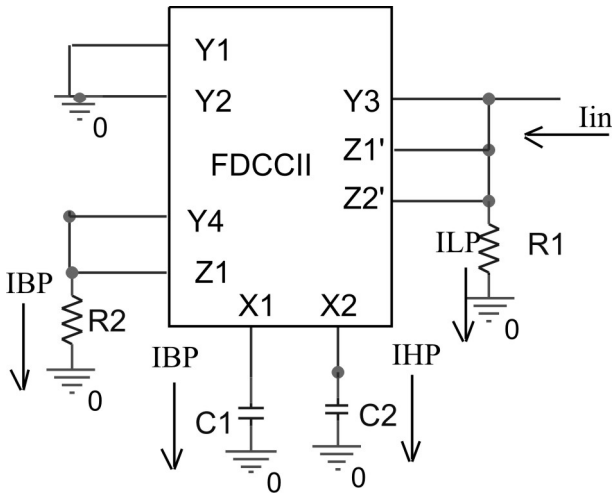


Figure 16: The proposed current-mode biquad filter employing FDCCII.

The resonance angular frequency ω_0 and the quality factor Q are given by

$$\omega_0 = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \quad (6)$$

$$Q = \sqrt{\frac{G_1 C_1}{G_2 C_2}} \quad (7)$$

The passive sensitivities of Q and ω_0 are given as follows,

$$S_{G_1}^{Q} = -S_{G_2}^{Q} = S_{C_1}^{Q} = -S_{C_2}^{Q} = \frac{1}{2} \quad (8)$$

$$S_{G_1}^{\omega_0} = S_{G_2}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = \frac{1}{2} \quad (9)$$

The second filter circuit can be used three-input single-output voltage-mode filter is shown in Fig. 17. Circuit analysis yields the following for the output voltage can be expressed as

$$V_O = \frac{G_1 G_2 V_1 - C_2 G_2 s V_2 + C_1 C_2 s^2 V_3}{G_1 G_2 + C_2 G_2 s + C_1 C_2 s^2} \quad (10)$$

Depending on the status of the input voltages V_1, V_2, and V_3, numerous filter functions are obtained. Special-

ization of the numerator yields the following voltage-mode filter transfer functions for the circuits.

(i) LP: $V_1 = V_{in}$ and $V_2 = V_3 = 0$,
(ii) BP: $V_2 = V_{in}$ and $V_1 = V_3 = 0$,
(iii) HP: $V_3 = V_{in}$ and $V_1 = V_2 = 0$,
(iv) BS: $V_1 = V_3 = V_{in}$, and $V_2 = 0$,
(v) AP: $V_1 = V_2 = V_3 = V_{in}$,

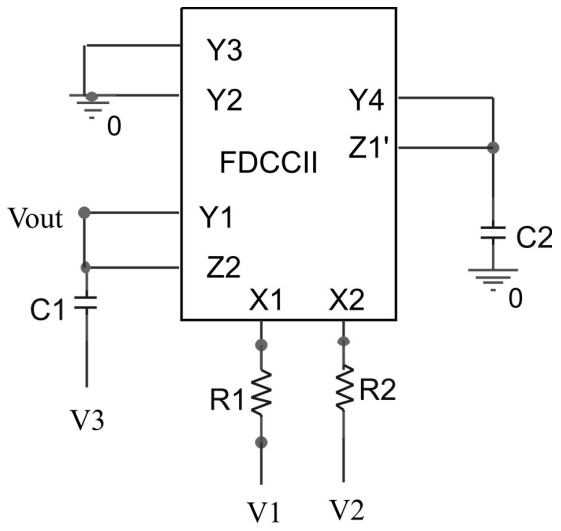


Figure 17: The proposed current-mode biquad filter employing FDCCII.

The resonance angular frequency ω_0 and the quality factor Q are given by

$$\omega_0 = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \quad (11)$$

$$Q = \sqrt{\frac{G_1 C_1}{G_2 C_2}} \quad (12)$$

The passive sensitivities of Q and ω_0 are given as follows,

$$S_{G_1}^{Q} = -S_{G_2}^{Q} = S_{C_1}^{Q} = -S_{C_2}^{Q} = \frac{1}{2} \quad (13)$$

$$S_{G_1}^{\omega_0} = S_{G_2}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = \frac{1}{2} \quad (14)$$

The current-mode biquad in Fig. 16 was designed for f_0 = 10 MHz by choosing $R_1 = R_2$ = 75kΩ, C_1 =0.3pF and C_2=0.15pF. Simulated response of high-pass, band-pass and low-pass filters topology shown in Fig. 18. For voltage mode filter in Fig. 17 has been design to provide high-pass, band-bass, low-pass, band-stop and all-pass responses with f_0 = 9.73 MHz. The passive component values are chosen as $R_1 = R_2$ = 75kΩ, C_1 =0.3pF and C_2=0.15pF. In Fig. 19 shows the simulated frequency responses for the high-pass, band-pass, low-pass, all-pass and band-stop configurations. As can be seen, there are a good agreement between theory and simulations.

Time domain analysis result is given in Fig. 20 for peak-to-peak 20 μA, 10 MHz sine wave input for current

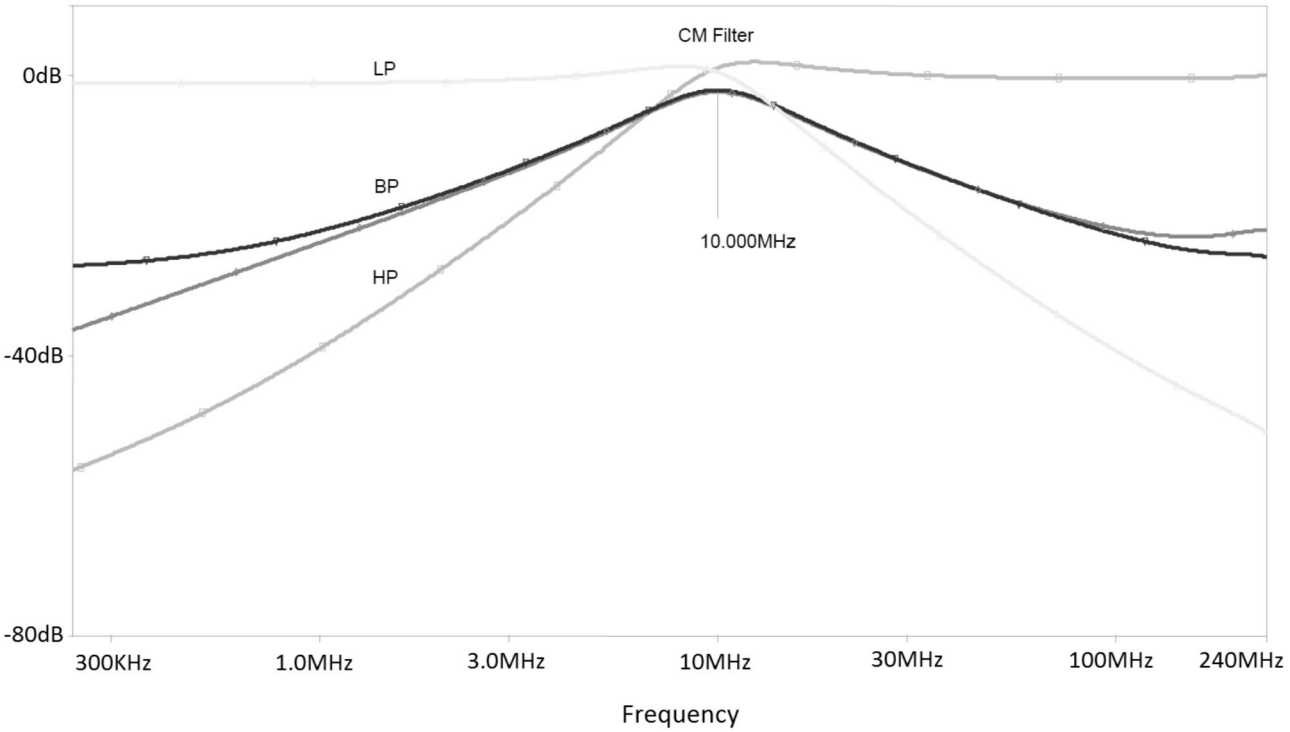


Figure 18: The simulated results of the gain–frequency responses of proposed curret-mode biquad filter

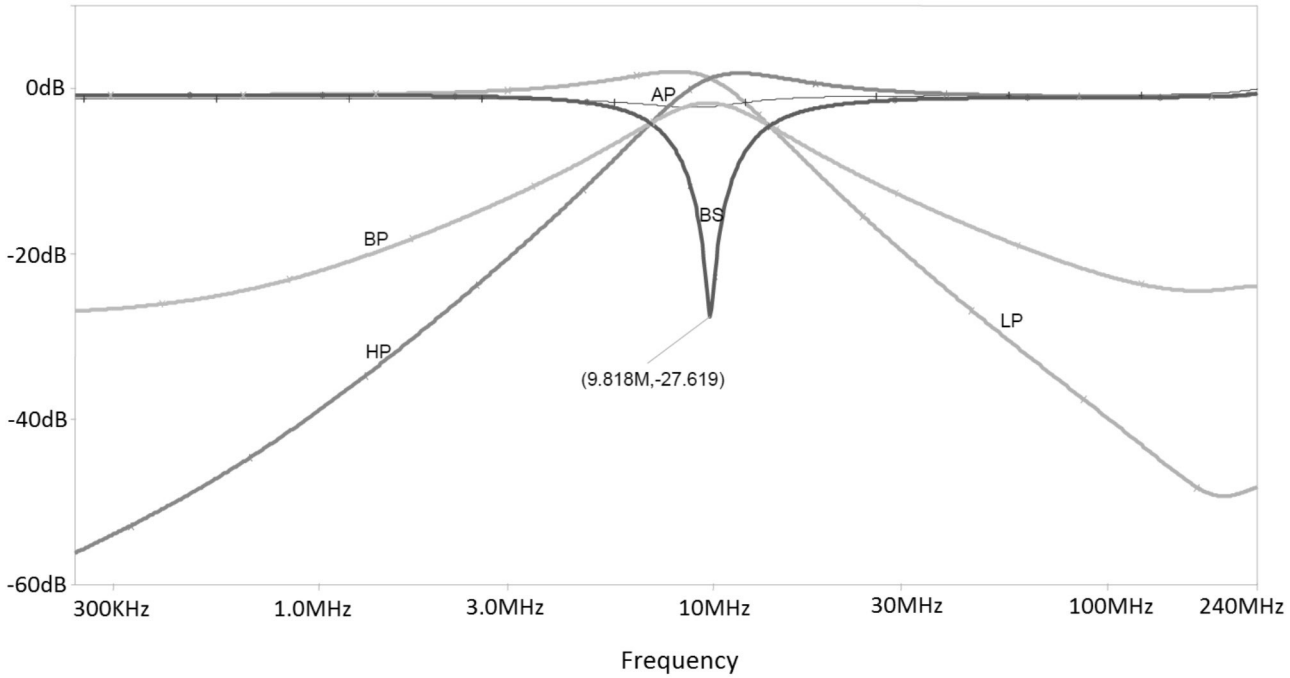


Figure 19: The simulated results of the gain–frequency responses of proposed voltage-mode biquad filter

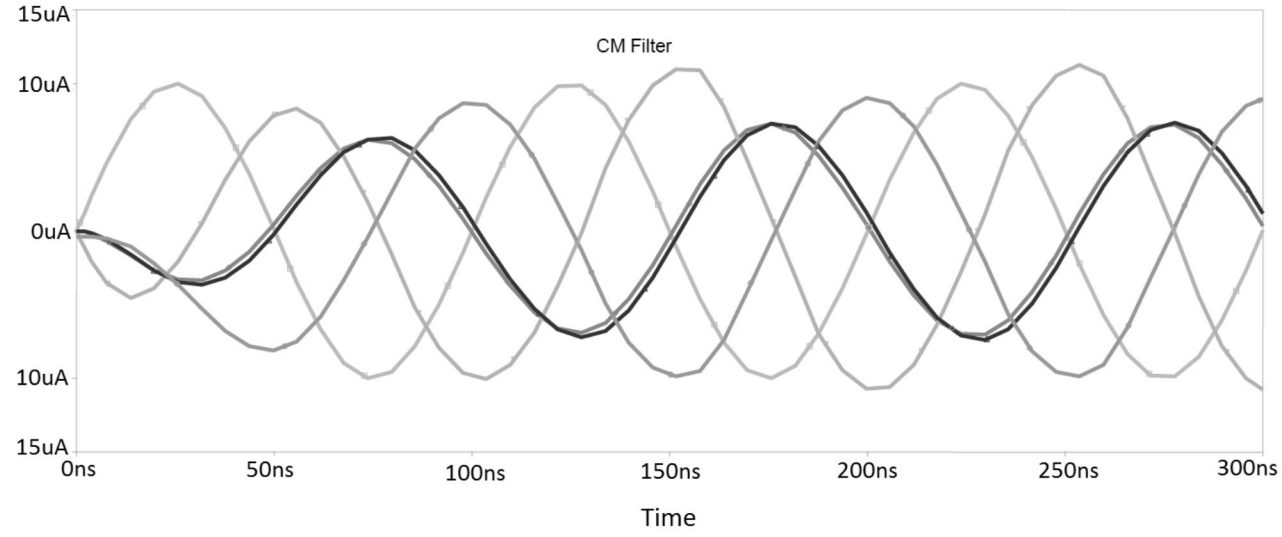


Figure 20: Time domain response of curret-mode filter

mode low-pass, band-pass and high-pass filters configuration for the circuit in Fig. 16. Time domain analysis result is given in Fig.21 for peak-to-peak 2V, sine wave at 9.73MHz input for voltage-mode low-pass filter. The large signal behavior of the circuit was tested by investigating the low-pass response on the input signal amplitude.

Fig. 22 shows the frequency response of curent-mode band-pass filter at 0°C, 25°C, 50°C and 100°C. As it is seen from the graphic frequency response of the filter almost does not change with respect to the temperature.

6 Conclusion

A new FGMOS FDCCII has been designed and simulated. By using FGMOS transistors both the input stage of the circuit providing the arithmetic calculations gets simpler also the linearity range increases due to the properties of FGMOS differential amplifier. The proposed FGMOS FDCCII is used in a tunable filter circuit in order to show the versatility of the FDCCII block. We can conclude that proposed FGMOS FDCCII structure provides the circuit designer further possibilites of realizing active circuits by reducing the number of transistors and extending the linearity range.

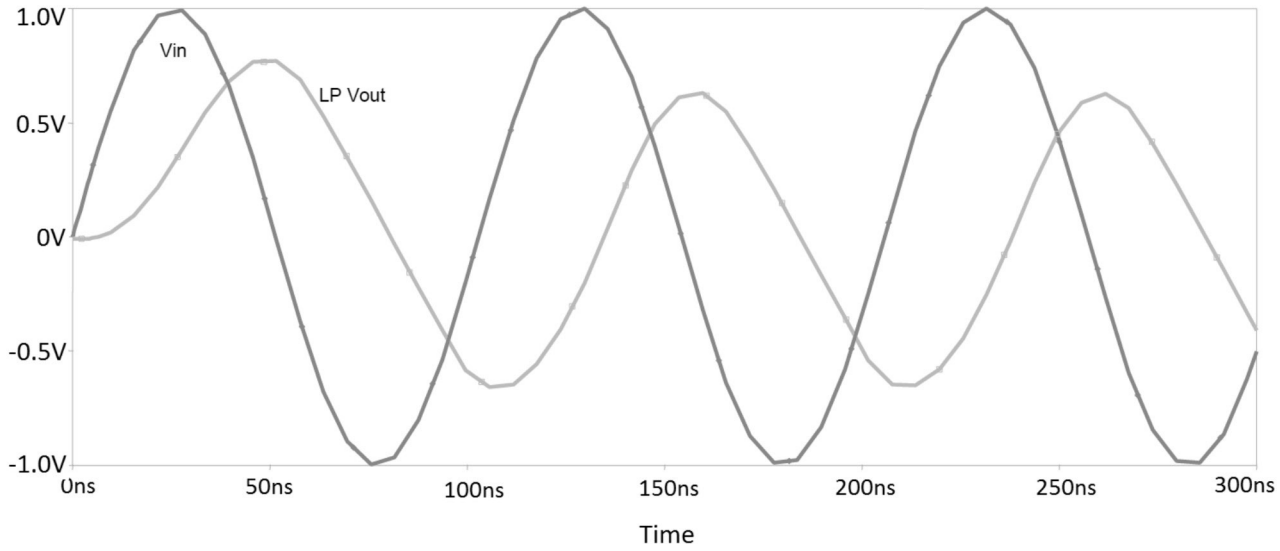


Figure 21: Time domain response of voltage-mode low-pass filter

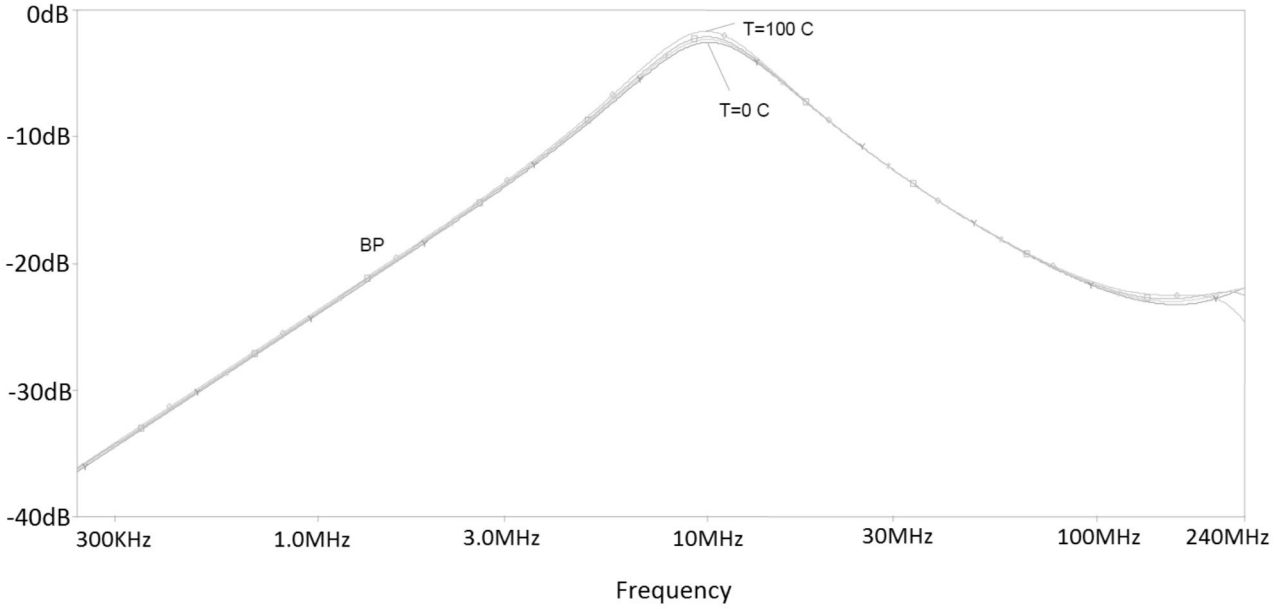


Figure 22: Frequency response of curent-mode band-pass filter at 0°C, 25°C, 50°C and 100°C

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