UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 1 ◦ 1995

Strokovno društvo za mikroelektroniko elektronske sestavne dele in materiale

Časopis za mikroelektroniko, elektronske sestavne dele in materiale
Časopis za mikroelektroniku, elektronske sastavne dijelove i materijale
Journal of Microelectronics, Electronic Components and Materials

INFORMACIJE MIDEM, LETNIK 25, ŠT. 1(73), LJUBLJANA, marec 1995

INFORMACIJE MIDEM 1 ° 1995

INFORMACIJE MIDEM	LETNIK 25, ŠT. 1(73), LJUBLJANA,	MAREC 1995
INFORMACIJE MIDEM	GODINA 25, BR. 1(73), LJUBLJANA,	MART 1995
INFORMACIJE MIDEM	VOLUME 25, NO. 1(73), LJUBLJANA,	MARCH 1995

Izdaja trimesečno (marec, junij, september, december) Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale.
Izdaja tromjesečno (mart, jun, septembar, decembar) Stručno društvo za mikroelektroniku, elektronske sastavne dijelove i materiale.
Published quarterly (march, june, september, december) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Naslov uredništva
Adresa redakcije
Headquarters
Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 61000 Ljubljana, Slovenija
(0)61 - 316 886

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Scientific Council for Technical Sciences of Slovene Ministry of Science and Technology has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials.
Publishing of the Journal is financed by Slovene Ministry of Science and Technology and by Society sponsors.

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Grafična priprava in tisk
Grafička priprema i štampa
Printed by
BIRO M, Ljubljana

Naklada
Tiraž
Circulation
1000 izvodov
1000 primjeraka
1000 issues

UDK621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 25(1995)1, Ljubljana

VSEBINA CONTENT

Slovenska mikroelektronika kot del svetovne mikroelektronike

Mikroelektronika v širšem pomenu besede je strateška industrija, ne le zaradi uporabe v vojaški industriji, ampak tudi iz makroekonomskega stališča, oz. v poslovnem smislu dologoročnega preživetja posameznih firm in dežel. Lep zgled za slednje so vzhodnoazijske države: Tajwan, Hongkong, Koreja, sledi jim že Kitajska, ki so v zadnjem desetletju z ustrezno poslovno-tehnološko strategijo svojih vlad, pripeljale svojo elektroniko in mikroelektroniko skoraj ob bok velikim.

Mikroelektronika hrani elektronsko industrijo, katera danes ponuja največ dodane vrednosti v svojih izdelkih. Leta 2000 bo svetovna polprevodniška industrija ustvarila za 200 bilionov US$ izdelkov, ki jih bo elektronska industrija uporabila za izdelavo sistemov v vrednosti 300 trilionov US$, in bo takrat najmočnejša industrijska veja v svetovnem merilu.

Mikroelektronika ne pomeni več samo posamezne komponente, ki jo je potrebno izdelati, ampak je že srce elektronskega sistema, saj se dodana vrednost celotnega sistema že počasi seli na stran mikroelektronike.

V zadnjih treh letih ponovno doživljamo rast trga polprevodniških komponent približno za 29% letno. Katere so tiste veje elektronike, ki vzdržujejo tako rast?

Poleg industrije osebnih računalnikov, ki nezadržno golta mikroprocesorje, spominska vezja in multimedijsko elektroniko (zvočne in video kartice, CD ROM naprave ipd.), telekomunikacijska industrija rabi vse več vezij za navadne in mobilne telefone ter vezja za DSP (Digital Signal Processing). Avtomobili počasi postajajo računalniki na kolesih, opremljeni z desetinami senzorjev in integrirano elektroniko za obdelavo meritev in nadzor vozila.

Še nekateri trendi so neizogibni: gostota vezij in hkrati njihova računska moč se podvojita vsakih 18 mesecev, pri čemer cena na enoto računske moči nezadržno pada. To omogoča prodor cenene elektronike ter s tem informacij v vsak konec našega planeta in povzroča trajne tehnološke in socialne spremebe družb, institucij ter prerazporeditev bogastva v globalnem merilu.

Podoba razvitega sveta se tako hitro spreminja, da nekatere firme že spoznavajo, da so njihove vzhodnoazijske hčere predaleč in predrage, če hočejo dovolj hitro reagirati na zahteve trga, zato ponovno počasi koncentrirajo vse svoje dejavnosti na enem mestu, kar pomeni izgradnjo novih kapacitet v domačih državah (ZDA, Evropa).

In kje smo mi?

Poleg nekaterih redkih svetlih izjem, se zdi, da naša elektronska industrija plava nekje na obrobju svetovnega dogajanja in šele išče področja, na katerih bi lahko odškrtnila velikim zajetnejši tržni delež.

Ravno tako Slovenija ne premore mikroelektronike v širšem pomenu besede, ki bi izdatneje hranila elektronsko industrijo. Resda imamo močne razvojno-raziskovalne skupine na IJS, Fakulteti za elektrotehniko in računalništvo, IEVT, in v nekaterih firmah, ki lahko v danem trenutku brez sramu Evropi in svetu pokažejo svoje dosežke. Le slovenska mikroelektronska industrija se zdi nekoliko podhranjena in prepuščena nekemu toku, ki jo neusmiljeno premetava iz ene v drugo kritično situacijo tako, da se komaj vzdržuje, o razvoju, investicijah in novih programih pa le občasno razmišlja.

Kako lahko spremenimo situacijo? Ali sploh potrebujemo močno elektronsko industrijo? Ali bomo to industrijo hranili z domačo mikroelektroniko, ali pa bomo večino dodane vrednosti elektronskega sistema kupovali v bodoče zunaj? Ali smo sposobni številne izume, dobre ideje, prototipe in uspešne maloserijske izdelke spremeniti v dobičkonosne industrijske izdelke z vgrajenim domačim znanjem?

Evropa se zaveda in priznava, da marsikatera vlada še ni spoznala pomembnosti pomoči in gojitve mikroelektronike v domačih logih, s čimer bi omogočila rast, konkurenčnost in osvajanje novih programov in izdelkov elektronike. Kaj lahko rečemo za našo?

Iztok Šorli

PHOTONIC TECHNOLOGIES AND DEVICES FOR MULTI-WAVELENGTH NETWORK APPLICATIONS[1]

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Keywords: photonic technologies, broadband services, telecommunication networks, optical networks, MWTN - MultiWavelength Transport Networks, wavelength multiplexing, optical overlay, optoelectronic integrated devices, transport capability of networks, layered networks, optical integrated devices, $LiNbO_3$ acousto-optic tunable filters, optical waveguides, spatial switches, practical examples, space switch matrices, semiconductor optical amplifiers

Abstract: Fast and quick growth of potential need for broadband services which may be offered by public network operators to business and residential users cannot be easily satisfied by a simple evolution of current electronic technology. In principle, photonic technology is ready to offer a huge increase in the overall transport capability of present networks, by using both the wavelength multiplexing principle and the optical overlay concept. A practical exploitation of these principles still needs a large amount of theoretical modelling and experimental work, along the guidelines which have been carried out within the RACE project "MultiWavelength Transport Network", where an optical network test bed has been fully implemented by using state of the art optoelectronic integrated devices. Results of this work will be presented here, with special attention to those aspects which need further improvement, and where different solutions may offer better alternatives.

Fotonske tehnologije in elementi za uporabo v večvalovnih komunikacijskih mrežah

Ključne besede: tehnologije fotonske, servisi širokopasovni, omrežja telekomunikacijska, omrežja optična, MWTN omrežja transportna večvalovnodolžinska, multipleksiranje valovnodolžinsko, prekrivanje optično, naprave optoelektronske integrirane, zmogljivost omrežij transportna, omrežja slojevita, naprave optične integrirane, $LiNbO_3$ filtri akusto-optični uglašljivi, valovodi optični, stikala prostorska, primeri praktični, matrike komutacijske prostorske, ojačevalniki optični polprevodniški

Povzetek: Današnja standardna elektronska tehnologija ne more več slediti hitri rasti potencialnih potreb za uslugami, ki jih upravniki javnih komunikacijskih omrežij ponujajo poslovnim in osebnim uporabnikom. V principu pa je fotonska tehnologija že pripravljena ponuditi ogromno povečanje gostote prenosa podatkov preko obstoječih mrež z uporabo načela valovnega multipleksiranja in optičnega prekrivanja. Pred praktično uporabo teh načel bo še vedno potrebno opraviti veliko teoretičnega modeliranja in eksperimentalnega dela v skladu z navodili, ki so zastavljena v sklopu RACE projekta " Večvalovne komunikacijske mreže ", kjer je bila tudi izdelana testna optična komunikacijska mreža s pomočjo najmodernejših optoelektronskih integriranih komponent. Rezultate tega dela bomo predstavili v tem prispevku, kritično bomo poudarili stvari, ki jih je potrebno še izboljšati, oz. kjer drugačne rešitve ponujajo boljše alternative.

1. Fundamentals of optical networks

The large transmission bandwidth associated with single mode optical fibers has been the basic factor for allowing the development of SONET (Synchronous Optical Network, in USA and Japan), and SDH (Synchronous Digital Hierarchy, in Europe) transmission standard. As a consequence, it has been possible in recent years to promote a world wide set of uniform criteria for defining:

- the *synchronous multiplexing technique*, which allows the transport of signals with different bit rates, services and transmission formats;
- a very flexible and powerful control technique for network management, bit error rate monitoring, network maintenance and provisioning, by using the section and path overheads bits in the SDH data stream;

1 Following two papers already published in MIDEM in 1994 on photonic devices, this last contribution is dedicated to medium term system and network applications aspects, which have been studied and developed mostly within the RACE II Project MWTN.

– the definition of a world standard for the SDH transmission equipment, from the STM1 (155 Mbit/s) hierarchy, which allows the full compatibility of equipment from different suppliers, to be used in the same transmission link.

These standards are still implementing a traditional concept, where electronic coding is used for all control and routing purposes, and optical technology is only applied for transport functions.

Looking to the introduction of broad band services (B-ISDN), a large increase in the network transport capacity is foreseen. A long term evolution strategy should be defined which shall allow a full use of the available fibre infrastructure transport bandwidth, and in particular by studying a more flexible and powerful network node structure, able to use photonic options, in addition to electronic functions, to increase the data throughput and traffic handling capability.

Recent advances in photonic device technology offer many opportunities to increase the transport network capacity; among them, EDFA are the key devices able to expand both the network geographical size and optical transparency, and to recover the optical losses which may be intrinsic to the use optical functionalities in the network node operation./1/

Racc. ITU G.803 defines a "layered model" of the transport network /2/, and classifies the nodes in *local exchanges*, directly connected to the users, and *transit exchanges*, without direct connections. This scheme may be extended by defining a new "optical layer" constituted by optical nodes (Optical Cross-Connect) and fibres interconnecting them. This layer will be overimposed on the "electrical layer", in which we find, for instance, the DXCs (Digital Cross-Connects).

In the new layer, signals will be carried transparently without dependence on the transmission format; on these signals main "optical transport functions" will be exerted:

i. assignment of wavelength to different signals by means of suitable tunable and/or switched sources
ii. selection of signals by means of fixed or tunable optical filters

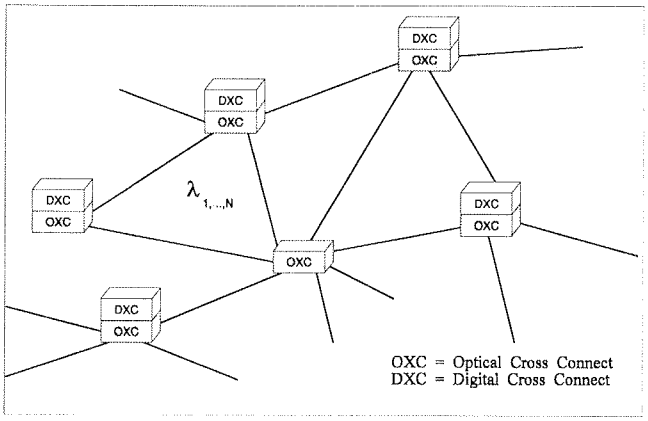

Fig. 1: "Layered" network: OXCs placed upon DXCs

iii. channels routing by means of spatial optical switching
iv. wavelength conversion
v. amplification by means of doped fibres or semiconductor amplifiers

Fig.1 shows the general scheme for a "layered" network.

A new and important feature is given by the capability of accessing the optical bandwidth to process signals by using the minimum number of optical-to-electrical-to-optical conversions.

On the basis of number of functions that will be exerted directly in the optical layer it will be possible to define a 'transparency degree" for the network, for instance with respect to the modulation scheme, data format and transmission speed.

Technology growth will allow the implementation of the "All-Optical Networks" /2/, in which, as a matter of fact, photonic devices will largely replace the electronic ones.

The introduction of such an optical layer in the telecommunication networks calls for the development of high performance, low cost components in order to make the optical transmission and routing functions cost effective with respect to more traditional solutions.

Some general considerations may be applied to the different applications.

In the range of data rates of 155÷622 Mbit/s, electronic equipment have been very well assessed: the ADMs (Add-Drop Multiplexers) and the DXCs (Digital Cross Connects), thanks to very large scale digital integrated circuits, can perform multi/demultiplexing, routing and switching in the electrical domain in a very efficient way.

At higher speed (2.5 Gbit/s, 10 Gbit/s, ...), quite essential for the B-ISDN, the realisation of very large ADMs and DXCs meets increasing feasibility problems in terms of physical dimensions, power consumption and costs.

On the contrary, at increasing bit rates, the implementation of optical routing functions becomes more convenient, depending on the high reliability of optical links and on the availability of a "new dimension", the "wavelength domain", in which performing network functions such as channel multi/demultiplexing and routing.

Let us consider optical filter devices, as an example, to select optical channels: the higher is the bit rate, the higher is the channel spectral width and, consequently, the easier is the technical feasibility of the optical filter.

2. Multi-wavelength transport networks: the MWTN project

The network proposed by the RACE Project R2028-MWTN (Multi Wavelength Transport Network) can be considered as a very good application of all the aforementioned concepts /3/.

Fig. 2 shows the OXC (Optical Cross Connect) node.

For each of the input or output fibres, the system carries 4 optical carriers (channels) spaced by 4 nm (1548, 1552, 1556, 1560 nm); each channel can then be substituted by a comb of 4 closely spaced optical carriers (0.1 nm), in order to further increase the overall capacity. In the "optical layer" channels can be transmitted, routed and amplified without any optoelectronic conversion.

A closer look at the OXC structure shows that optical amplifiers are located immediately at the input and at the output ports: they compensate for the path losses (a typical span of 50 km between two adjacent nodes is considered) and for the attenuation experienced by signals that have been filtered and spatially switched inside the node.

Optical multi-channel transmitters and receivers perform a suitable interface with the "electrical layer" (DXCs) and allow the drop/insert functions for channels relevant to the considered node; higher bit rates of the SDH hierarchy have been adopted: 622 Mbit/s and 2.488 Gbit/s.

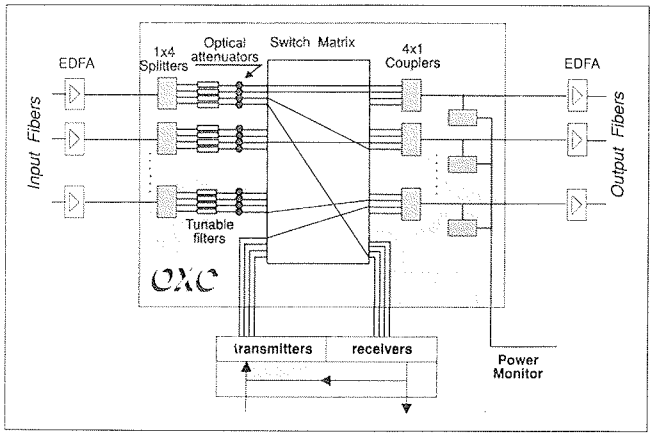

Fig. 2: OXC node proposed by the MWTN Project

3. Why optical integrated devices ?

Optical and optoelectronic integrated devices only can make cost effective the concepts related to a "layered network": they are essential to keep low the power consumption and the physical dimensions of the hardware.

Moreover, optical integration minimizes the number of optical interfaces between different devices: actually, fibre/device coupling introduces the more severe constraints in terms of attenuation and is the more costly step in the packaging process.

NxN waveguide spatial optical matrices, for instance, may be realized by interconnecting simple 2x2 switches in a specific multistage structure; monolithic integration is the only way to implement an efficient interconnection of the elementary bricks of the device.

The integration level of optical functions, both on semiconductor and on electro-optical materials, is very low if compared to that of electronic circuits. This is due to the larger dimensions of elementary component blocks and to a lower maturity of the photonic technology. Optoelectronic circuits are, anyhow, very valuable because transmission, more than logic, functions can be easily integrated. Another characteristic is related to the difficulty to obtain good yields and good performances because requirements for components such as sources, detectors, modulators, amplifiers, filters, couplers and switches are typically very stringent. In the following a brief review of more common integrated functions is given together with some implementation example.

4. Integration of optical functions

As far concerns laser sources, recently available DFB lasers are suitable for operation at 2,5 Gbit/s, with relatively low (0,1 nm) dynamic spectral broadening (chirp).

Moreover, the combined effect of chirp by the laser source and chromatic dispersion is often responsible of a bandwidth limitation; in this case, the useful bandwidth can be increased by using an external light modulator. Commercially available $LiNbO_3$ electro-optical modulators have 10 Gbit/s bit rate modulation capability, with almost negligible chirping, but require quite high driving voltages, which are not easily obtained at high bit-rate. Therefore it looks very promising the development of a monolithic integrated structure made by a laser coupled to a semiconductor electroabsorption modulator, which already shows high modulation rate, in excess of 10 Gbit/s, and low driving voltage (<5 Volt)./4/

Tunable sources are a critical component in multi-wavelength networks, where the wavelength of many optical carriers need to be quickly selected and switched in a tuning range several nm wide. Distributed Bragg Reflector (DBR) devices with multielectrode configuration are suitable to cope with the wavelength tuning requirement /5, 6/. The realization of DBR devices still remain a difficult technology development task, particularly in terms of yield, grating uniformity and layer thickness control. More sophisticated structures have been proposed to allow a wider tuning range, by using multiple DBR devices, integrated on a single substrate, with contiguous tunable ranges ($\Delta\lambda$ = 21 nm, /7/), Y shaped lasers ($\Delta\lambda$ = 50 nm, /8/), laser DBR with a non uniform grating period ($\Delta\lambda$ = 50 nm, /9/).

Semiconductor optical amplifiers, are ideal candidates to be combined in integrated monolithic devices to obtain a large variety of optical functions (splitting, combiners, filters and switches), with compensation of the relevant insertion losses. Optical non linear effects, as gain saturation and four-wave-mixing for instance, may be used to obtain high level functions; among them, wavelength conversion is a key feature for routing of optical channels through an OXC node.

Optical filters, in particular for high density WDM systems, are critical devices which must fulfil several tight

specifications: high selectivity, low insertion losses, wide range tunability and low cost. An interesting example of a filter based on a diffraction grating will be described in the following paragraph. Normal DFB or DBR lasers, operating under laser threshold as a selective amplifiers, may be used as active filters, with optical bandwidth between 1 and 10 GHz. Multielectrode configurations allow a tuning range of the order of 2 nm with a relatively flat output level /10/. These filters are tunable with switching times of a few nsec.

Acousto-optical filters /11/ are based on channel waveguides realized on $LiNbO_3$; the operating principle is shown in Fig. 3: the optical input signal (with TE polarization state) is coupled to the acoustic wave, and its polarization state is converted to TM, which is transmitted through the TM polarizer at the output of the filter. Without the coupling with the acoustic wave, the optical wave is blocked by the output polarizer. The optical transmission characteristic of the filter is controlled by the frequency of the RF signal, which generates the acoustic wave. The central frequency of the RF signal is about 175 MHz for frequencies around 1552 nm, and 10 mW of RF power are needed to achieve a good acousto-optic coupling. The optical selectivity of the filter is of the order of 1 nm and a tuning range of a few tens of nanometers may be achieved by changing the RF signal central frequency. Simultaneous tuning on different wavelengths can be obtained by using different RF excitation frequencies. Switching speed for acousto-optic filters is of the order of several microseconds.

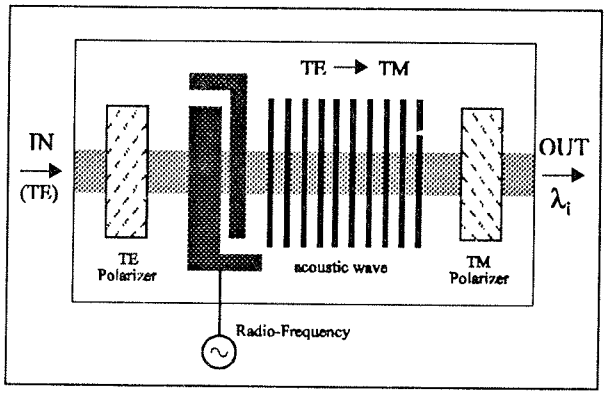

Fig. 3: $LiNbO_3$ acousto-optic tunable filters

Key components for the implementation of optical cross-connects are the space switching matrices, which may be realized starting with monolithic 2 x 2 elementary blocks. For this elementary unit, several design configuration (Fig. 4) have been already tested: a) the directional coupler, b) the Mach-Zehnder interferometer, c) the X junction, d) the optical gates.

In the first three devices, coupling or interference conditions are controlled by suitable voltages applied to the controlling electrodes; without bias, the optical signal coupled to the input port is transferred to the normal, or so called "bar", output port, while by applying the control voltage the signal is switched to the other "cross" output port. The fourth structure is based on semiconductor optical amplifiers which may be switched by current injection from a high absorbing state to a transparent state; therefore the optical path where the amplifier is located can be opened or closed by the control current, and any connection between input and output ports can be implemented. An added advantage of using optical amplifier is that optical gain may compensate the overall switch insertion losses.

The first three configuration, which make use of the dependence of the index of refraction from the electric field, may be realized on $LiNbO_3$, or semiconductor substrates. Recent experiments have shown the possibility to use, to the same purpose, a thermorefractive effect; therefore, Silica on Silicon or ion-exchanged-glass materials may be used as waveguide substrates. The semiconductor material, of the Multi-Quantum-Well heterostructure type, have the highest electro-optical coefficient, and are suitable for realization of very small elementary devices, which may lead to matrices with large number of stages.

The fourth structure can be realised only by semiconductor material.

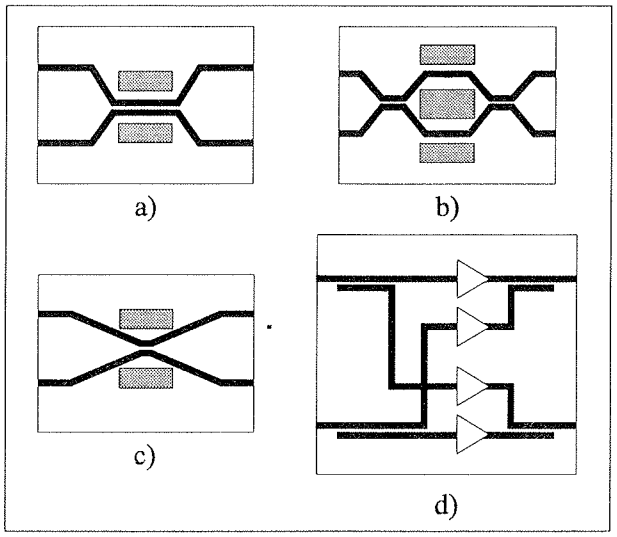

Fig. 4: Optical waveguide spatial switches with dimensions 2 x 2

Characteristic parameters of these devices are the insertion losses, operating voltages (currents), temperature stability, ageing, extinction ratio, switching time and noise.

Integration of optical and electrical functions on a single substrate is a further step toward the so called Opto Electronic Integrated Circuits (OEIC). Simple OEIC devices are for instance a laser with an integrated driver or a photodetector with integrated preamplifier; arrays of such simple OEIC have been implemented for multichannel operations, as for instance by the RACE 1027 Project /12/, where an array of 8 integrated detectors and

preamplifiers has been realized on InP substrate, as an example of monolithic OEIC with several tens of elementary optical and electrical devices.

An important point to be noted here is that OEIC development is particularly useful in view of their capability to offer high speed performances, allowed by the very short electrical connections, reduced stray capacitances and other parasitic effects.

5. Practical example of integrated optic devices

Main manufacturing technologies for integrated optic devices should include Lithium Niobate, InP based heterostructure materials and Silica on Silicon.

Lithium Niobate technology is now relatively mature and a few devices are commercially available; among them high speed electro-optical light modulators, optical switching matrices and optical filters. Recent advances include the realization of active (Er doped) waveguides, which may allow the development of optical amplifiers and laser sources integrated in the $LiNbO_3$ substrate, to obtain a quite wide range of optical functionalities.

InP technology holds the most promising potentiality for a truly integrated optics approach, as it may allow monolithic integration of laser sources, modulators, photodetectors and semiconductor optical amplifiers, to achieve a high degree of integration with very complex functionalities. Most of these potentialities have been already tested with laboratory prototypes, and in fact two devices (a 4 x 4 space switch and a 4 channel tunable filter), realized for the optical cross-connect used in the MWTN experiment, will be described in detail in this paper. Process control and reproducibility to achieve reasonable yields still need a better assessment before the InP technology could be considered fully available for cost-effective industrial purposes.

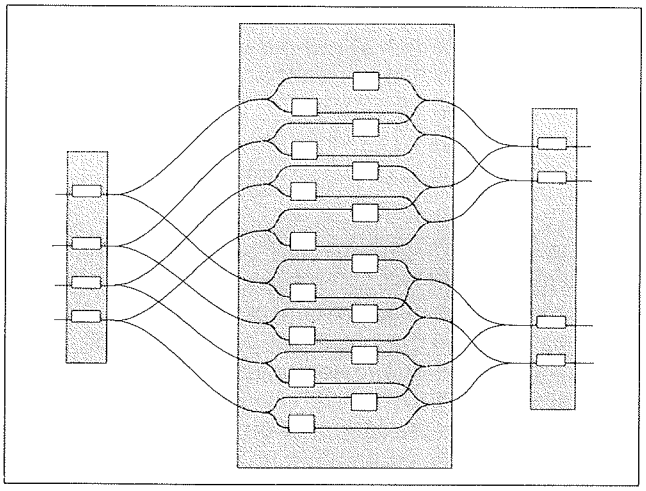

Fig. 5: 4 x 4 space switch matrix, based on semiconductor optical amplifiers

Silica on Silicon waveguide technology (which has been already described in this journal in detail, /14/) is suitable for a hybrid assembly opportunity, which may offer a good compromise between yields, complexity and cost, including the benefits of the mature and reliable Silicon process technology. A possible implementation of the optical cross-connect node for the MWTN experiment by using the SoS technology will be described.

5.1 InP 4 x 4 space switch, with active optical gates

The space switch matrix is the key functionality required for an optical cross-connect; the device described here, which is based on a single chip InP/InGaAsP integration of a passive waveguide optical routing network, 16 optical gates and 8 input/output semiconductor optical amplifiers (Fig. 5), may be considered a state of the art OEIC realization /15/, with characteristics well suited for an optical switch (low insertion losses, a few nsec reconfiguration set-up time, small (7 x 3 mm) dimensions).

The switching element in the matrix is a Y passive power splitter, followed by two semiconductor optical amplifiers; the optical signal path through the switch is controlled by the current injected into the matrix of optical amplifiers, which may be switched between off (absorbing) state and on (amplifying) state. The optical gain of the amplifiers can be used to compensate the splitting (3 dB) and excess loss of the splitters. The routing pattern through the full matrix implements a strictly non-blocking architecture. Further optical gain is provided by input and output buffer amplifiers, which allows compensation for fibre pig-tailing losses, bending losses and waveguide losses. The material growth process is based on a Metal Organic Vapour Phase Epitaxy, and the InGaAsP active material composition is chosen to operate around 1550 nm wavelength. Overall insertion losses (fiber to fiber) are less than 5 dB, and cross-talk extinction ratio better than 40 dB has been achieved. The device is somewhat sensitive to input light TE or TM polarization state, with differential losses between the two polarization states of the order of 6 - 12 dB. The level of current injection required to switch the gate amplifiers is of the order of 50 mA.

5.2 Multi-grating filters

Another device based on InP material technology is the multi-grating filter /16/, which allows the extraction of one or more selected wavelengths from a WDM signal. While still affected by relatively high losses and polarization sensitivity, these filters are easily controlled by current injection, with a good rejection factor and further monolithic integration capability. In Fig. 6 a scheme of a multi-grating filter is shown, designed for 4 channel selection, with wavelength at 1548, 1552, 1556, 1560 nm. The filter operation principle is based on a cascade of four DBR gratings, each one tuned to reflect one of the above wavelength, in such a way that, without bias, all optical channel are back reflected. To allow the transmission by the filter of one or more optical channels, the reflection band of the appropriate grating is shifted by current injection.

The structure of the multi-grating filter is based on a buried hetero-structure channel waveguide 0.2 μm thick and 1.3 μm wide, with intrinsic undoped InGaAsP active layer material, with 1,38 eV band gap energy at room temperature. The overall waveguide structure is identical to a laser structure with n and p doped InP cladding layers (Fig 6b). Gratings are etched 0.1 μm above the active layer with 60 nm thickness; each grating is 300 μm long, with 50 μm spacing between different gratings.

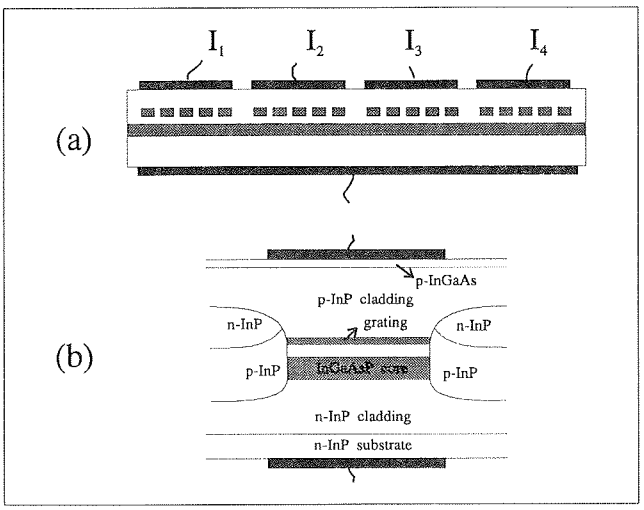

Fig. 6: Tunable multi-grating filter: a) side view, to show the electrical contacts structure, b) cross section view

Filter response has been measured by using the spontaneous emission from a fibre optical amplifier as a wideband light signal, with suitable polarizer to select TE or TM polarization state. Insertion losses (including pigtail losses of 6 dB for each chip facet) of the order of 25 dB have been measured for TE mode excitation, due to free carrier absorption and waveguide scattering losses. Transmission spectrum for the unbiased filter is shown in Fig. 7a, which shows a relatively flat response for the four gratings response. The transmission spectrum, with 2 mA current injected in the first grating electrode, is shown in Fig. 7b, and 2.6 nm shift in the transmission bandpass for the corresponding wavelength is clearly observed. With a TM polarized input light the effect is similar but the wavelength shift increase up to 4.5 nm with the same injection current. Therefore the input light need to be polarized to avoid cross-talk effects with the present device: an improved control of the polarization sensitivity of the structure is necessary, for instance by using a more symmetrical cross-section for the active waveguide, even if this may noticeably increase the complexity of the fabrication process.

The full cross-talk characteristic of the multi-grating filter, for a TE excitation, is shown in Tab. 1; the cross-talk is defined here as the ratio between the optical power transmitted by the active channel with respect to the

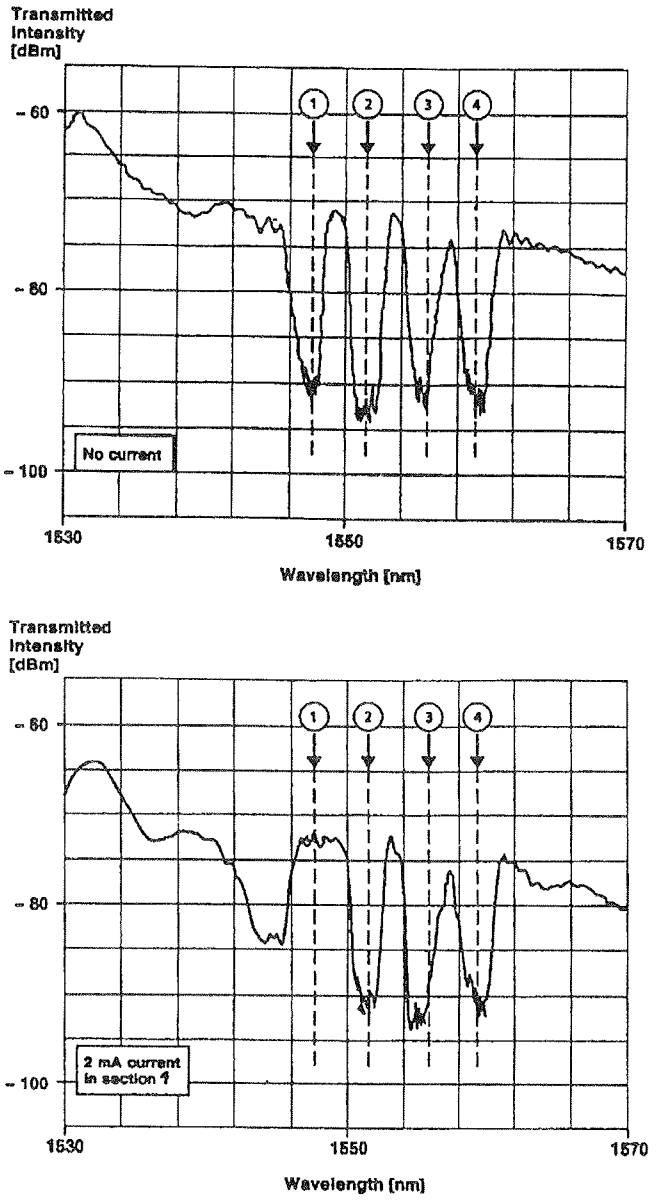

Fig. 7: Spectral emission from the Multi-grating filter. (Input light from the ASE emission by an EDFA) - a) without excitation b) with 2 mA current injected in the first section electrode

power transmitted through the blocking channels. A quite large spread has been found in the experimental values, ranging from a minimum of 9.4 dB up to 19.4 dB. Reasons for these discrepancies are still not well understood, but may be due to non uniform coupling of different gratings with the active waveguide, which can be improved by a better control of the fabrication process. Even taking into account present limits, which could be off set by an optimized structure design and by some improvement in the process technology, the optical notch filter described here is well suited for multi-wavelength systems applications, and is a good demonstration of the potential of the OEIC InP based technology.

Selected channel	Channel cross-talk			
dB	1	2	3	4
1	-	18.5	19.4	18.2
2	11.8	-	19.4	15.9
3	11.0	11.0	-	15.9
4	10.6	11.1	9.4	-

Tab. 1 - Channel cross-talk ratio, for different channels of the multi-grating filter

5.3 A perspective evaluation of the Silica on Silicon technology

We conclude the description of possible technology solutions to implement an optical 4 x 4 wavelength routing node by considering a full use of SoS devices. In this case, known data and technical characteristics of elementary SoS devices will be used for modelling a few relatively more complex optical circuits, taking into account present technology constraints (the 4" wafer size, as a limit for the optical circuit practical dimensions, for instance). The results should be taken only as a design feasibility indication, but they clearly demonstrate the intrinsic technology potential for very low cost, good performances and simple construction practices. The optical routing node structure is shown in Fig. 8; it consist of four main building blocks, each one of which can be realized on a 4" Silicon wafer, with overall dimensions of each device not larger than 60 x 60 mm. This is fully compatible with wafer process capability currently available, even if process yield for a wafer size device has not been evaluated so far.

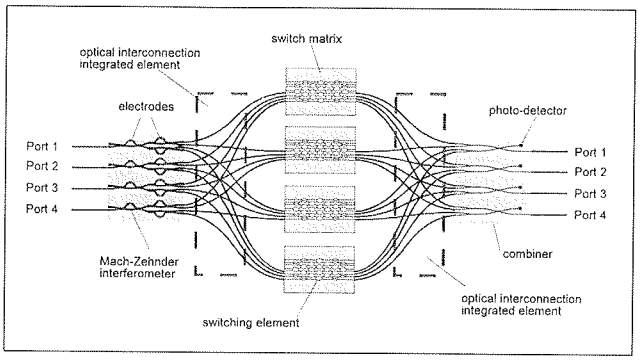

Fig. 8: Example of a 4 x 4 multi-wavelength routing node fully implemented with Silica on Silicon technology

Let us describe now each node building block in some detail starting from the input side:

4 channel WDM demultiplexer

The first device includes 4 identical WDM demultiplexers on a single substrate wafer; each demultiplexer is designed to separate the input multi-wavelength signal stream into four single wavelength output channel. A detailed description of the demultiplexer operation has been already reported in this Journal /ref. 14, pag. 155,156/; typical performances (already experimentally tested for a single device) are listed in Tab. 2.

insertion loss	2 dB
cross-talk attenuation	20 dB
spacing between adjacent channels	0.1 - 20 nm
temperature dependence	low
polarization dependence	low

Tab. 2 - Typical characteristics of a wavelength demultiplexer based on Silica on Silicon technology

Integrated interconnection element

As directly shown in fig. 8, the function of this element is simply to connect each wavelength channel output from the demultiplexers to the appropriate input of the switching matrices. Design constraints for such structure are related to the bending radius of the waveguides (which must be higher than 10 mm, to avoid attenuation) and the waveguides crossing angle (which should be not less than 15 degree, to avoid cross-talk). By using these simple design rules, the overall attenuation for each connection path, including fiber coupling loss, will be less than 1 db. This element is used twice in the optical node, as shown in fig. 8.

Optical switching matrices

The wavelength routing function is accomplished by four identical 4 x 4 optical space switches. Each space switch provides the routing of a single wavelength, by using a combination of balanced Mach-Zehnder interferometers, which can be switched between the "cross" and "bar" state by using the thermorefractive effect, induced by a small thin film heather deposited on one arm of the interferometer (for a more detailed description, see Ref. 14, pag. 157). The switching time which may be attained by the thermorefractive effect is of the order of a msec; therefore this type of space switch is suitable only for transport network applications, where low switching speed is generally adequate. Optical characteristics of the space switch are listed in Tab. 3.

insertion loss	3-4 dB
cross-talk attenuation	12-15 dB
modulation frequency	1 KHz
working principle	thermo-optical
control current	0-100 mA
temperature dependence	low
polarization dependence	low
optical bandwidth	>40 nm

Tab. 3 - Optical characteristics of a space switch based on Silica on Silicon technology

Optical combiner

The last building block for the node is an array of 4 x 2 optical combiners, where one of the output ports is used for output power control and monitoring. A small fraction of the light output is extracted from this channel waveguide by a 45 degree tilted mirror, directly etched into the waveguide, and coupled to a PIN monitor photodiode self aligned with respect to the mirror. Optical characteristic of this node output stage are listed in Tab. 4.

insertion loss	2 dB
intrinsic loss	6-7 dB
optical bandwidth	300 nm

Tab. 4 - Optical combiner typical characteristics.

ACKNOWLEDGEMENTS

The Authors wish to thank Dr. A. Fincato for his advice in writing the paragraph concerning the Silica on Silicon technology. Development of many components described in this paper has been in part financially supported by the E.C. RACE 2028 Project.

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Prispelo (Arrived): 27.03.95 ***Sprejeto (Accepted): 05.04.95***

RAZLAGA MOČNEGA KAPACITIVNEGA EFEKTA V NIN STRUKTURI IZ AMORFNEGA SILICIJA

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Ključne besede: a-Si silicij amorfni, NIN strukture polprevodnikov, SCLC prevajanje, efekt kapacitivni, frekvence nizke, admitanca diferencialna, kapacitativnost diferencialna, prevodnost ohmska

Povzetek: Pred kratkim je bil ugotovljen močan kapacitivni efekt pri nizkih frekvencah v amorfnih silicijevih NIN strukturah. Ta efekt, ki je odvisen od priključene enosmerne prednapetosti in od frekvence majhnih vzbujevalnih signalov, je razložen s pomočjo faznega premika, ki ga povzroča mehanizem zakasnjenega lovljenja in ponovne emisije elektronov na lokaliziranih stanjih v mobilnostni reži amorfnega silicija.

Explanation of Strong Capacitive Effect in Amorphous Silicon NIN Structure

Key words: a-Si, amorphous silicon, NIN semiconductor structures, SCLC conduction, capacitive effect, low frequencies, differential admittance, differential capacity, ohmic conductivity

Abstract: Steady-state and small-signal characteristics of various amorphous silicon NIN samples, differing in fabrication steps and having different I-layer thicknesses, were measured using HP 4140B pA meter and HP 4284 A 20Hz-1MHz LCR meter. DC current-voltage characteristics showed SCLC conduction mechanisms described in the literature. Small signal AC measurements showed a strong capacitive effect in all measured NIN devices. In the low frequency range the measured capacitance was up to few thousand times higher than the static capacitance $C_0=\varepsilon(S/L)$ and it decreased with the increasing frequency of AC signal. The capacitance increased strongly with the increasing DC bias voltage on NIN device. The parallel small signal conductance was also measured. It increased by increasing both, frequency and DC bias voltage.

The main physical effect causing the high capacitive effect of NIN diode at low frequencies is the delay of small signal trapped carrier concentration Δn_t following the injected free carrier concentration Δn. This delay is governed by electron capturing and emission mechanisms at localised states in the gap of a-Si. This delay is strongly influenced by density of states in the gap. It also depends on DC bias and the frequency of AC excitation. Small-signal trapped electron concentration can not follow high frequency free electron variations so that capacitance at high frequencies is low and depends mainly on stored electron concentration. In the low frequency range however, trapped carriers Δn_t follow free carriers Δn. Space-charge pertaining to carrier concentrations Δn and Δn_t are causing small-signal electric field, which is connected with terminal voltage ΔU (by integrating electric field ΔE over the I-layer thickness).

At low frequencies however, the variations of trapped carriers Δn_t predominate over free carriers Δn, influencing dominantly small signal electric field ΔE and terminal voltage ΔU on NIN device terminals.

A small-signal equivalent analytical model of NIN diode is developed which agrees well with experimental results. Using this model it is shown that an increasing frequency of signal excitation moves the energy region of gap states engaged in delaying action towards the conduction band resulting in strongly decreasing capacitive and increasing conductive effect of NIN device.

1. UVOD

Če bi bila plast polprevodnika med dvema prevodnima kontaktnima oblogama zelo slabo prevodna, bi bila med zunanjima priključkoma kapacitivnost $C_0 = \varepsilon(S/L)$, kjer je L razdalja med kontaktnima oblogama, S je površina oblog in ε je permeabilnost polprevodnika.

Ker pa je v I-plasti NIN zgradbe iz amorfnega silicija možno prevajanje z elektroni, se pri vsaki spremembi ΔU okoli enosmerne prednapetosti U pojavi pripadajoča sprememba injekcije elektronov na enem NI-spoju in ekstrakcije elektronov na drugem NI-spoju. Zaradi sprememb koncentracij injiciranih prostih elektronov in zaradi lovljenja ter reemisije elektronov na lokaliziranih stanjih v energijski reži se v I-plasti prerazporedi prostorski naboj. Če bi bila sprememba prostorskega naboja Δq zaradi sprememb koncentracij prostih in ujetih elektronov Δn in Δn_t trenutna, bi lahko kapacitivnost NIN strukture (tako kot kapacitivnost osiromašene plasti PN-spoja) izrazili z razmerjem $C = \Delta Q / \Delta U$, kjer pomeni ΔQ spremembo naboja v I-plasti zaradi majhne spremembe zunanje napetosti ΔU. Pri tem je za NIN strukturo iz a-Si značilno, da v ΔQ sodeluje predvsem ujeti naboj (saj je $n_t >> n$ in $\Delta n_t >> \Delta n$), ta pa je odvisen od porazdelitve gostote stanj v mobilnostni reži a-Si.

Pri predpostavki eksponencialnega poteka repa akceptorskih stanj v energijski reži pod prevodnim pasom in pri zanemaritvi difuzijskega toka je Rose ugotovil /1/, da bi se zaradi $\Delta n_t(\Delta U)$ kapacitivnost lahko povečala od C_0 največ na vrednost $2C_0$. Z analizo enosmernih lastnosti a-Si NIN zgradbe, pri kateri je zanemarjena difuzijska komponenta toka, se da dokazati približno odvisnost takšne kapacitivnosti od porazdelitve lokaliziranih stanj v reži. Analiza pokaže /2/, da z rastočo strmino repa stanj pod prevodnim pasom kapacitivnost upada od $2C_0$ (pri konstantni gostoti stanj v vsej reži) do C_0 (pri nenadni spremembi gostote stanj na robu prevodnega pasu).

Meritve diferencialne admitance NIN strukture pa so pokazale /3/, da je kapacitivnost lahko tudi nekaj 1000 krat večja od medelektrodne kapacitivnosti C_0. Merjena kapacitivnost je odvisna od izbrane mirovne delovne točke in od frekvence izmeničnega signala. Tudi izmerjena ohmska diferencialna prevodnost je močno odvisna od enosmerne delovne točke in od frekvence.

Glavni razlog za zelo povečani kapacitivni efekt je zakasnitev izmeničnega ujetega naboja Δn_t za injiciranim nabojem Δn, ki se pojavlja zaradi lovljenja elektronov v lokalizirana stanja ter njihove ponovne emisije v prevodni pas. Posledice tega so zakasnitve prostorskega naboja, električnega polja in potenciala za injiciranimi prostimi elektroni ter kompleksni karakter admitance NIN strukture.

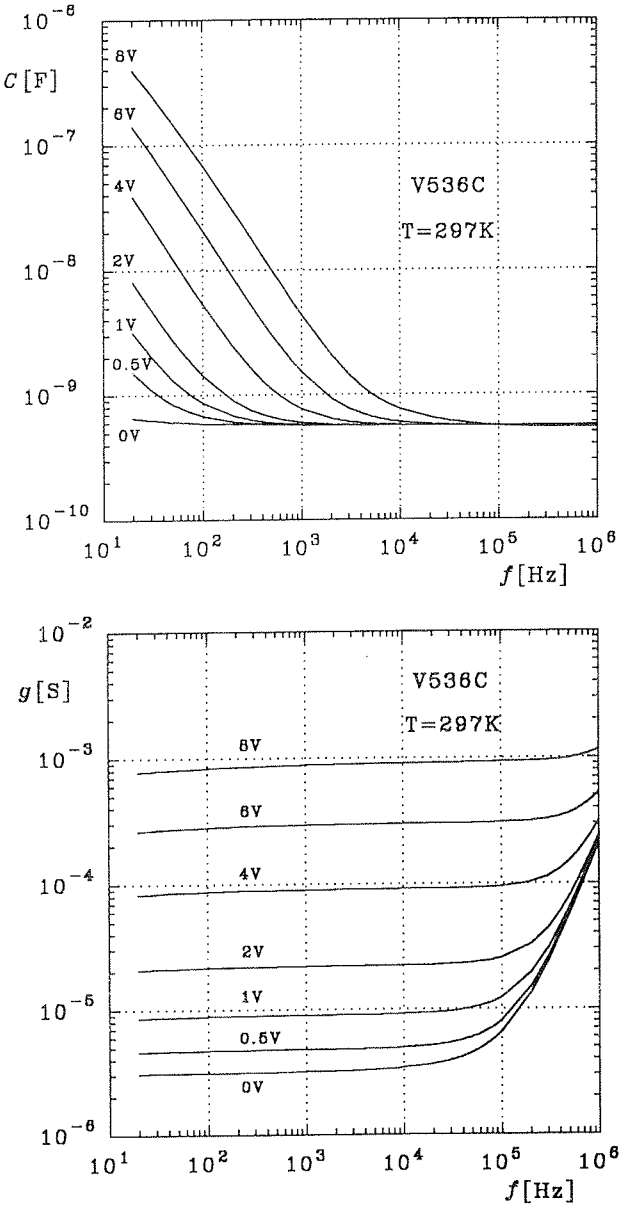
V članku je podana fizikalna slika delovanja NIN strukture pri vzbujanju z majhnimi izmeničnimi signali pri različnih enosmernih prednapetostih. Opisan je tudi zanimiv pojav, da pri višanju frekvence signalov pri konstantni enosmerni prednapetosti sodelujejo lokalizirana stanja v reži z energijami vedno bližjimi prevodnemu pasu. To pa ima za posledico, da se z rastočo frekvenco signalov zakasnitve ujetja in sproščanja elektronov zmanjšujejo. Kapacitivni efekt zato upada, diferencialna ohmska prevodnost pa narašča.

2. MERJENE KARAKTERISTIKE NIN STRUKTURE

Enosmerne karakteristike in kompleksne admitance treh različnih NIN struktur (razlike pri tehnološkem pro-cesu, razlike geometrijskih razsežnosti) so bile izmerjene s HP 4140B pikoampermetrom ter HP 4284A 20Hz-1MHz LCR metrom.

Izmerjene enosmerne tokovno-napetostne karakteristike so pokazale tipični potek SCLC prevajanja (tok omejen s prostorskim nabojem), ki je opisan v literaturi /4/. Električne lastnosti pri vzbujanju z majhnimi signali pa pokažejo, da lahko NIN strukturo nadomestimo z vzporedno vezavo ohmske prevodnosti in kapacitivnosti, ki pa sta obe odvisni od izbrane enosmerne delovne točke in od frekvence.

Slične admitance so bile izmerjene pri vseh NIN vzorcih. Kot primer kaže slika 1 poteke kapacitivnosti in prevodnosti za NIN strukturo z debelino I-plasti 1.25 μm ter s kontaktnimi površinami 0.06 cm^2.



Slika 1: Izmerjena diferencialna kapacitivnost in ohmska prevodnost NIN strukture v odvisnosti od enosmerne prednapetosti in od frekvence

Izmerjeni grafi kompleksne admitance NIN diode kažejo, da kapacitivnost te zgradbe upada od velike vrednosti pri nizkih frekvencah proti mnogo manjši kapacitivnosti pri visokih frekvencah, komponenta realne prevodnosti pa s frekvenco raste. Obe komponenti naraščata z rastočo enosmerno prednapetostjo na NIN strukturi.

3. OPIS FIZIKALNIH UČINKOV NA ADMITANCO NIN DIODE

Glavni vzrok za veliko kapacitivnost pri nizkih frekvencah izmeničnih signalov so zakasnitve ujetih elektronov pri reemisiji iz lokaliziranih stanj v energijski reži v pre-

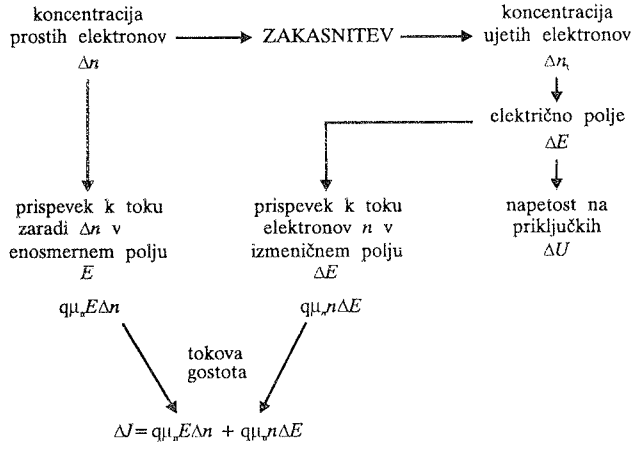
vodni pas. Pri visokih frekvencah so spremembe krmilnih izmeničnih signalov tako hitre, da jim elektroni, ki prehajajo med prevodnim pasom in lokaliziranimi nivoji, ne morejo več slediti. Zato teče elektronski tok le s premiki prostih elektronov v prevodnem pasu. Ker se pri teh premikih javljajo zakasnitve med toki in napetostmi, se kaže to kot kapacitivni učinek, ki pa je zaradi izredno kratkih zakasnitev mnogo manjši od tistega zaradi časovnih zakasnitev ujetih elektronov na lokaliziranih stanjih pri nizkih frekvencah.

Poleg visokofrekvenčne kapacitivnosti zaradi zakasnitev prostih elektronov pri prehodu preko I-plasti je prisotna seveda tudi kapacitivnost $C_0 = \varepsilon(S/L)$ zaradi poljskega toka $J = \varepsilon(dE/dt)$.

Nov in najbolj zanimiv je učinek izredno visoke kapacitivnosti pri nizkih frekvencah /3/. Fizikalno sliko te kapacitivnosti si najlaže predstavljamo, če izhajamo iz injekcije elektronov na enem NI-spoju ter ekstrakcije elektronov na drugem NI-spoju. Takšno delovanje nastane, ko je na NIN strukturo priključena enosmerna prednapetost.

Če enosmerni koncentraciji elektronov n v I-plasti dodamo še neko majhno harmonično komponento $\Delta n \exp(j\omega t)$, povzroča kompleksor presežka prostih elektronov Δn še zakasnjeni presežek ujetih elektronov Δn_t. Ta je v a-Si pri počasnih signalih po vrednosti mnogo večji od vrednosti Δn. Koncentracija Δn_t s svojim prostorskim nabojem povzroča izmenično električno poljsko jakost ΔE, ki je z integralom preko dolžine I-plasti povezana z majhnim izmeničnim signalom ΔU na zunanjih priključkih.

Če pri nizkih frekvencah predpostavimo, da so spremembe Δn_t v fazi z ΔE, te pa v fazi z ΔU, je izmenična komponenta majhnih signalov tokove gostote ΔJ povzročena s premikom enosmerne koncentracije prostih elektronov n zaradi izmeničnega polja ΔE ter s premikom izmenične komponente koncentracije elektronov Δn pod



Slika 2: Komponente izmenične tokove gostote v NIN strukturi

$$\frac{\Delta J}{J} = \frac{\Delta I}{I} = \frac{\Delta E}{E} + \frac{\Delta n}{n} = \frac{\Delta U(g + j\omega C)}{I} = \frac{\Delta U}{U}\frac{g + j\omega C}{G}$$

vplivom enosmernega električnega polja E, kot kaže shematično graf na sliki 2.

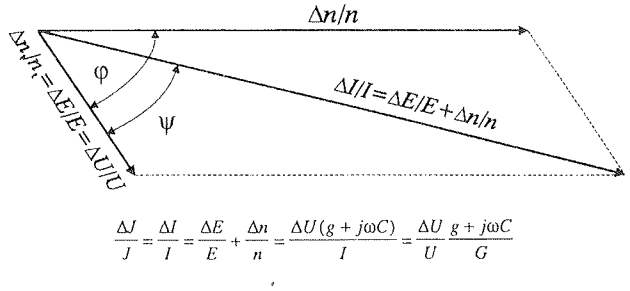
Če dalje upoštevamo, da teče v I-plasti električni tok, ki je omejen s prostorskim nabojem (SCLC delovanje), lahko opišemo tipično krajevno odvisnost električnega polja v I-plasti s parabolo

$$E(x) = E(L)(x/L)^m$$

Pri zanemaritvi vseh zakasnitev, razen tiste med Δn in Δn_t, se da z rešitvijo Poissonove enačbe ugotoviti, da so normirane komponente malih signalov ujetega naboja, električnega polja in napetosti na priključkih med seboj enake

$$\frac{\Delta n_t}{n_t} = \frac{\Delta E}{E} = \frac{\Delta U}{U}$$

Pri teh pogojih dobimo enostaven kazalčni diagram signalov na sliki 3. Zaradi zakasnitve φ med Δn in Δn_t se pojavi kompleksna admitanca $y = g + j\omega C$ s faznim kotom ψ med tokom ΔI in napetostjo ΔU.



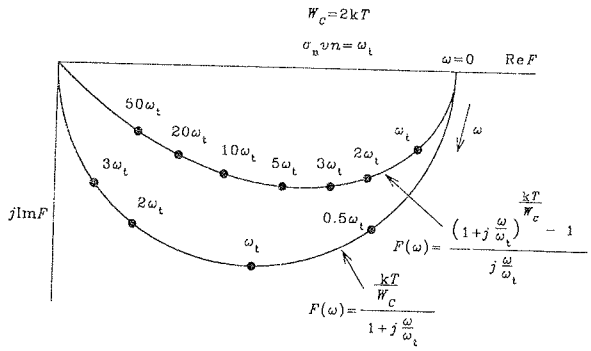
Slika 3: Kazalčni diagram izmeničnih signalov v NIN strukturi

Kapacitivni učinek je pri nizkih frekvencah skrit v zvezi med kompleksorjema Δn in Δn_t. To zvezo se da dobiti iz splošnih enačb za amorfni silicij pri vzbujanju z majhnimi signali /5/ preko integracije zasedenih stanj akceptorskega tipa v energijski reži med valenčnim in prevodnim pasom a-Si /2/

$$\Delta n_t = \int_{E_V}^{E_C} \Delta f_{tA} g_A dE = \Delta n \frac{n_t}{n} \frac{(1 + j\frac{\omega}{\sigma_n v n})^{\frac{kT}{w_c}} - 1}{j\frac{\omega}{\sigma_n v n}} = \Delta n \frac{n_t}{n} F(\omega)$$

kjer je σ_n prerez ujetja elektronov v nevtralnih akceptorskih stanjih, v je termična hitrost in w_c energijska konstanta pri eksponencialni porazdelitvi gostote akceptorskih stanj v reži a-Si. Frekvenčni potek funkcije $F(\omega)$, ki vsebuje zakasnitev med Δn in Δn_t, je pri tipičnih vrednostih snovnih konstant a-Si pri eni izmed izbranih delovnih točk prikazan na sliki 4. Ta potek je soroden poteku funkcije $kT/w_c(1+j\omega/\omega_t)$, ki opisuje tipično zvezo med napetostjo in tokom pri paralelni vezavi konstantne kapacitivnosti in upornosti. Prav odstopanje izračuna-

nega poteka F(ω) od tipične zakasnilne funkcije pa je razlog za upadanje kapacitivnosti ter naraščanje prevodnosti z rastočo frekvenco.



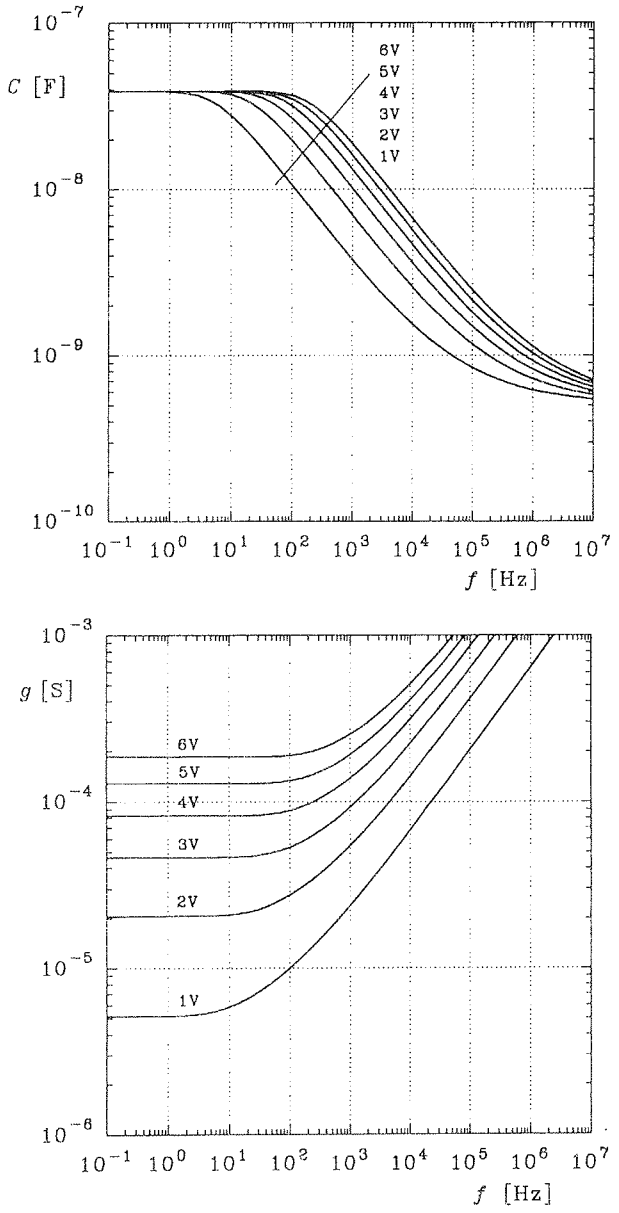
Slika 4: Potek frekvenčno odvisne zveze F(ω) med prostim in ujetim nabojem

Tudi v a-Si bi dobili zvezo med Δn in Δn_t preko člena $(1+j\omega/\omega_t)$, če bi pri vseh frekvencah elektroni iz prevodnega pasu izmenjavali mesta z istimi lokaliziranimi nivoji v energijski reži. Podrobnejša analiza pokaže, da sodelujejo pri izmeničnih signalih lokalizirani nivoji v okolici kvazifermijeve energije E_{Fn}. Z višanjem frekvence signalov se spreminja verjetnost zasedenost v reži. Pri višjih frekvencah so prispevki k Δn_t pri energijah, malo nižjih od E_{Fn} močneje slabljeni kot prispevki stanj pri energijah, nekoliko višjih od E_{Fn} (zasedenost se pri nižjih energijah v reži močneje zmanjšuje). To pomeni, da pri višjih frekvencah izmeničnih signalov sodelujejo s svojimi zakasnitvami vedno bolj plitva lokalizirana stanja, bližja prevodnemu pasu. Pri teh stanjih pa so hitrejše reemisije ujetih elektronov v prevodni pas, kar se navzven pokaže kot znižanje zakasnitve Δn_t za Δn in kot zmanjšanje kapacitivnega učinka.

Opisani premik sodelujočih lokaliziranih stanj pa ima za posledico tudi naraščanje realne prevodnosti z rastočo frekvenco krmilnega signala. Ko sodelujejo vedno plitvejša stanja, je zaostajanje Δn_t za Δn manjše, kot če bi bila udeležena vedno ista stanja okoli E_{Fn}. Hkrati pa absolutna vrednost Δn_t upada (oboje kaže tudi izračunani potek F(ω) na sliki 4). Temu pa ustrezajo manjše vrednosti električnega polja ΔE in napetosti ΔU. Zaradi tega je pri istem toku ΔI prevodnost $\Delta I/\Delta U$ bliže realni prevodnosti, ta pa z rastočo frekvenco raste.

Primer izračunanih potekov realne prevodnosti in kapacitivnosti NIN strukture pri različnih enosmernih prednapetostih v odvisnosti od frekvence kaže slika 5. Razmeroma dobro ujemanje izračunanih lastnosti po poenostavljeni analitični poti z izmerjenimi lastnostmi na sliki 1 vodi do sklepa, da opisana fizikalna dogajanja v NIN zgradbi primarno učinkujejo na frekvenčno in napetostno odvisnost nadomestne admitance pri vzbujanju z majhnimi signali.

Iz rezultatov prikazane obravnave lahko ugotovimo zelo važno potencialno uporabno lastnost, in sicer zelo visoko kapacitivnost NIN strukture pri nizkih frekvencah.



Slika 5: Analitična izračuna poteka kapacitivnosti in ohmske prevodnosti od enosmerne delovne točke in od frekvence

Primerno bi bilo raziskati poleg a-Si še druge snovi, ki imajo veliko gostoto lokaliziranih stanj, preko katerih ni možno neposredno prevajanje električnih nabojev, ki pa so sposobna loviti in sproščati z zakasnitvami velike količine vstopajočih električnih nabojev. To bi lahko vodilo k izdelavi kondenzatorjev, ki bi v področju nižjih frekvenc izkazovali veliko kapacitivnost v majhnem volumnu zgradbe.

4. ZAKLJUČEK

Podan je bil fizikalni opis dogajanj v NIN strukturi iz amorfnega silicija. Za visoko kapacitivnost pri nizkih frekvencah so odgovorna lokalizirana stanja v energijski reži polprevodnika, ki jih z zakasnitvami polnijo in praznijo prevodni elektroni. Zakasnjeni prostorski naboj uje-

tih elektronov povzroča zakasnjeno napetost na zunanjih priključkih in zato močan kapacitivni karakter NIN strukture.

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Prispelo(Arrived): 18.11.1994 ***Sprejeto(Accepted): 07.03.1995***

TRIPLE DIFFUSED BiCMOS TECHNOLOGY FOR ANALOG - DIGITAL ASICS

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Keywords: microelectronics, IC, integrated circuits, analog-digital circuits, CMOS devices, bipolar devices, bipolar devices, circuit design, device fabrication, complementary properties, vertical NPN bipolar transistors, vertical PNP bipolar transistors, lateral PNP bipolar transistors, BiCMOS circuits, triple diffused BiCMOS technology, MOS capacitors, active devices, passive devices

Abstract: Synergy of CMOS and bipolar performances has been for a long time a designer's dream. BiCMOS, a technology which enables making CMOS, bipolar and other passive devices on the same chip allows realisation of this dream. In particular, we have developed so called triple diffused BiCMOS technology suitable for analog-digital design of ASICs for medium power supply voltages of up to 15 V. Besides added flexibility, good price - performance ratio, this technology also allows a new qualitative step ahead with almost zero investment into new process equipment and clean room construction.

Trojnodifundirana BiCMOS tehnologija za izdelavo analogno-digitalnih integriranih vezij po naročilu

Ključne besede: mikroelektronika, IC vezja integrirana, vezja analogno digitalna, CMOS naprave, naprave bipolarne, transistorji bipolarni, snovanje vezij, izdelava naprav, lastnosti komplementarne, NPN transistorji bipolarni vertikalni, PNP transistorji bipolarni vertikalni, PNP transistorji bipolarni lateralni, BiCMOS vezja, BiCMOS tehnologija trojno difundirana, MOS kondenzatorji, naprave aktivne, naprave pasivne

Povzetek: Sinergija lastnosti, ki jih ponujata CMOS in bipolarna tehnologija je sen vsakega načrtovalca integriranih vezij. BiCMOS tehnologija, ki omogoča izdelavo CMOS, bipolarnih in drugih pasivnih elementov na enem čipu, pa je tista, ki lahko ta sen tudi uresniči. V prispevku opisujemo posebno, tki. trojno difundirano BiCMOS tehnologijo, ki smo jo razvili za potrebe načrtovanja analogno - digitalnih naročniških integriranih vezij z napajalno napetostjo do 15 V. Poleg dodane fleksibilnosti in zadovoljive cene na enoto funkcije, pa nam ta tehnologija omogoča kvalitativen korak naprej, skoraj brez investicije v novo procesno opremo in čiste prostore.

1. INTRODUCTION

Bipolar technology has been for long time the working horse of early days microelectronics. Being typical "analog" technology at the beginning, it has forced designers to thoroughly characterise and optimise many analog subcircuits. The emergence of MOS technology in early seventies and especially the invention of CMOS has revolutionarized microelectronics a great deal. After all bugs were taken care of, CMOS was easier to integrate, less complicated, cheaper per silicon area and had less power consumption. It was ideal for integration of digital functions which was later proved by many successful designs.

Depending on which design group somebody belonged to from the beginning, designers have actually through time divided themselves into fans of either "digital -MOS" or "analog - Bipolar" design approach. Late eighties have brought certain new waves of thinking among them. Having realised that modern telecommunication, automotive and industrial electronics started needing ASICs capable of integrating analog and digital functions, they have also started thinking how to realise all these functions on the same chip, or at least in the same electronics system.

To start with, at that time CMOS has already been a mature, low cost high yielding digital technology. However, some innovative design approaches like the discovery of SC (Switch-Capacitor) circuits, successful realisation of operational amplifiers in CMOS and some others have proved that CMOS can be also turned into attractive process to make analog-digital ASICs. As well, built in the CMOS technology is the possibility to make lateral and low performance vertical NPN or PNP bipolar transistors with no extra process steps or cost. This capability has been for long time used by designers if they really needed bipolar transistors besides MOS ones, /1/, /2/. So basically, CMOS already is a certain kind of "BiCMOS", a mixed Bipolar&CMOS technology which allows realisation of MOS and bipolar transistors on the same chip.
And here is where the whole story begins.

2. DO WE REALLY NEED BiCMOS ?

Since most of the analog-digital functions can be realised with CMOS, do we really need special BiCMOS technology?

Our answer is yes, since CMOS is after all limited to certain extent in making the best performance analog-

digital functions. We believe that only synergy of MOS and bipolar transistors within certain subcircuits where advantageous behaviour of each component is utilised can bring to the optimum price - performance ratio.

This has already been proven by others, /3/, and by our own design experience, /4/. We will better understand this if we take into consideration basic differences between MOS and bipolar transistor. These differences are briefly explained in this section, but the reader can find more information on this subject in references /3/, /5/ and /9/.

2.1 Comparison of MOS and Bipolar Transistors

2.1.1 Transconductance

Transconductance of a bipolar transistor is given by:

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{U_T} = \frac{qI_C}{kT} \qquad (1)$$

g_m : transconductance

I_C : collector current

V_{BE} : base to emitter voltage

U_T : thermal voltage given by $U_T = kT/q$

while transconductance of an MOS transistor in saturation is given by equation:

$$g_m = \sqrt{2k\frac{W}{L}I_{DS}} \qquad (2)$$

k : transconductance parameter

W, L : width and length of the transistor

I_{DS} : drain current

Comparing both equations we can quickly see that bipolar transistor outperforms MOS. Not only that the absolute value of the transconductance is much higher, see figure 1, but its value depends linearly on current, inversely on temperature and is geometry independent. In other words, minimal geometry bipolar transistor has same transconductance as large one at the same current level. To obtain same value of transconductance with MOS transistor it must be 50 to 700 times larger than its bipolar counterpart.

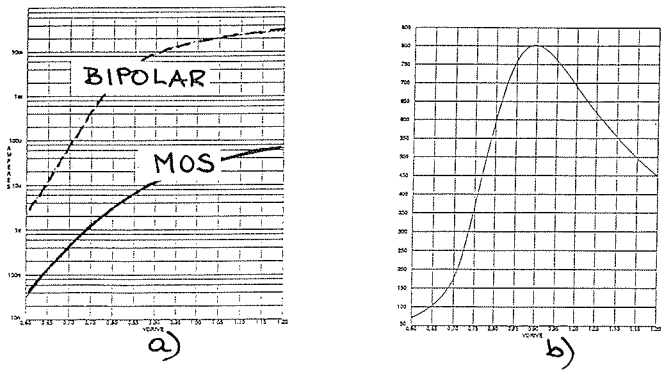

Fig. 1: Transconductance comparison between equal sized MOS and bipolar transistors at different current levels, a) transistor current as a function of V_{BE} (V_{GS}), b) BIP/MOS g_m ratio as a function of V_{BE} (V_{GS})

2.1.2 Open circuit voltage gain

Open circuit voltage gain of a bipolar transistor in common emitter configuration is given by:

$$a_0 = \frac{\partial V_{CE}}{\partial V_{BE}} = g_m r_0 = \frac{V_A}{U_T} \qquad (3)$$

V_{CE} :collector to emitter voltage

r_0 : output impedance

V_A : Early voltage

while open circuit voltage gain for an MOS transistor in saturation is given by:

$$a_0 = g_m r_0 = \frac{1}{\lambda I_{DS}}\sqrt{2k\frac{W}{L}I_{DS}} \qquad (4)$$

λ : channel length modulation parameter

Analog design requires high open circuit voltage gain values. We again see that bipolar transistor is not only better than MOS but its gain is again geometry independent. We can easily make bipolars with V_A above 50 V which gives us a_0 around 2000 while for MOS transistor to achieve this value at 1 mA current level, we must make W/L ratio around 10^5 !!

2.1.3 Temperature Effects

We can show that for two bipolar transistors with emitter area ratio N, their base to emitter voltage difference varies according to the equation :

$$\Delta V_{BE}(T) = \frac{kT}{q}\ln N \qquad (5)$$

N : emitter area ratio of two bipolar transistors

This equation predicts simple relationship among base - emitter voltage difference, absolute temperature and emitter area ratio of two neighbouring bipolar transistors. This is actually the basis for the design of temperature independent subcircuits and electronic temperature sensors.

On the contrary, V_{GS} of an MOS transistor is quite complicated function of temperature and its geometry which favours use of bipolar oriented design for temperature insensitive electronics.

2.1.4 Offset Voltage

It can be shown that the offset voltage of the bipolar differential stage can be written as:

$$V_{OS} = \frac{kT}{q}\left(-\frac{\Delta R}{R} - \frac{\Delta A_E}{A_E} - \frac{\Delta Q_B}{Q_B}\right) \quad (6)$$

V_{OS} : offset voltage

R : load resistance

A_E : emitter area

Q_B : Gummel base number given by

$$Q_B \equiv \int_{base} N(x)dx \quad (7)$$

Same expression for MOS transistor is:

$$V_{OS} = \Delta V_{TH} + \frac{V_{GS} - V_{TH}}{2}\left(-\frac{\Delta R}{R} - \frac{\Delta(W/L)}{W/L}\right) \quad (8)$$

V_{TH} : threshold voltage

Both expressions in parenthesis are caused by process and geometry short range variations. If we suppose that their value is about the same for both transistors, we see that the offset voltage of a bipolar differential stage is much lower since the value of kT/q factor (0.025 V at the room temperature) is also much lower than (V_{GS} - V_{TH})/2 of MOS transistor which is in the range of 0.25 V.

Typical offset voltage of bipolar differential stage is 1 mV while for MOS differential stage it is around 10 - 15 mV.

2.1.5 Noise

It would be out of the scope of this paper to discuss the noise aspects of both transistors in details. However, some general statements can be made. It has been widely accepted for a long time that bipolar transistors have lower noise than MOS especially since they exhibit low 1/f noise which is usually neglected, while for MOS transistors' 1/f noise is high. Lately, MOS designers have, using some inventive and careful design techniques, succeeded in bringing MOS circuit noise figures down to the levels comparable to bipolars. This was achieved at the expense of larger circuit area/silicon but at the same time such MOS stages have several times lower input currents than bipolar counterparts.

2.1.6 Power Consumption

In general, bipolar ICs are known to dissipate a lot of power while due to inherent working principles CMOS circuits assure zero power supply quiescent current at DC conditions.

2.1.7 Input Current

MOS transistors have almost infinite input impedance, since there is practically no current flow into MOS gates.

2.1.8 Ideal Switch

So far we have compared MOS and bipolar transistors as voltage controlled current sources. It is obvious that in the active region of operation bipolar transistor outperforms MOS.

However, bipolar transistor in saturation (very low values of V_{CE}) actually operates with forward polarised collector to base voltage. This region of operation is difficult to control. On the contrary, MOS transistor can be used either as voltage controlled resistor (linear region) or just as a switch; with gate voltage below threshold it is completely blocked, while condition $V_{GS} > V_{TH}$ assures conduction, figure 2.

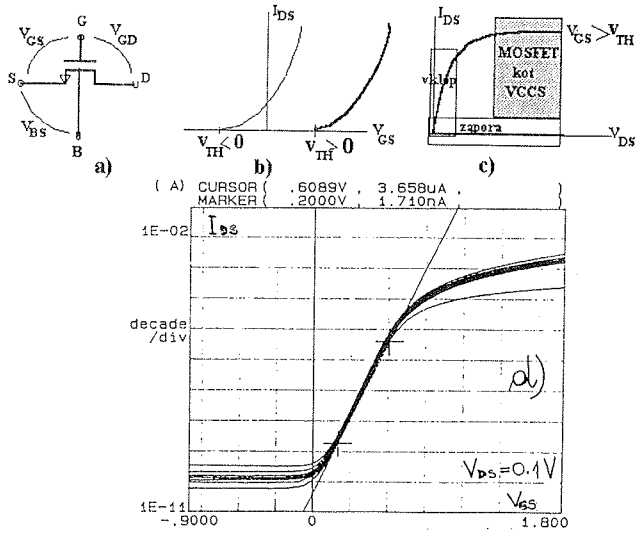

Fig. 2: MOS transistor and its regions of operation
a) electrical symbol
b) input characteristics
c) output characteristics
d) subthreshold characteristics

2.2 Synergy of Bipolar and MOS Technology

In table 1 advantages and disadvantages of bipolar and CMOS transistors are listed regarding their use in analog-digital design. BiCMOS option is added.

Ideally, it seems like BiCMOS technology could pick up only good sites of each technology. Only to start with, somebody could design certain full MOS or full bipolar subcircuits within one single chip. This is probably the easiest way to integrate MOS and BIP transistors but as mentioned previously synergy of MOS and BIP transistors on the cell level would be a new qualitative jump.

Although BiCMOS is more complex due to more process steps, it is also more robust and offers more flexibility to the designers.

But there is another aspect which makes BiCMOS technology so attractive. Introduction of BiCMOS practically does not require any investments into clean rooms or new equipment, only the process must be modified as a first step. It seems that by smartly transferring some designs originally fabricated using CMOS or BIP processes to BiCMOS their performance increases by as much as factor 2. This is definitely a strong argument for an ASIC manufacturer who is strongly involved in analog-digital design to start introducing this new technology in his technology portfolio.

Table 1: CMOS and BIPOLAR technology comparison

PARAMETER	CMOS	BIP	BiCMOS
High transconductance		0	0
High open circuit voltage gain		0	0
Simple temperature behaviour		0	0
Low offset voltage		0	0
Low noise	(1)	0	0
High speed	(2)	0	0
Low power consumption	0		CMOS part
Zero input current - high input impedance	0		CMOS part
Ideal switch	0		CMOS part
Good capacitive load driving capabilities		0	BIP part
Very small geometries (ULSI)	0	(3)	CMOS part
Mature high yielding technology	0		CMOS part

(1) CMOS noise improves with smart design techniques
(2) CMOS speed improves with smaller gate lengths
(3) minimum geometry MOS transistor is smaller than minimum geometry BIP transistor

3. BiCMOS TECHNOLOGY

3.1 Introduction

Three categories of BiCMOS ICs have emerged, / 6 /:
- low cost, medium speed 5 V digital
- high performance, higher cost 5 V digital
- analog - digital

The distinction among these are based on differences in the process flows used to produce them.

Low cost BiCMOS parts are fabricated with slightly modified, single well CMOS processes (only one or two masks are added to a baseline CMOS process).

High performance digital BiCMOS ICs are fabricated with twin well, CMOS based process flows that are significantly modified from the baseline CMOS process (three or four mask levels are typically added).

Analog - digital BiCMOS ICs are fabricated with processes designed to accommodate the larger voltage levels of analog applications (e.g. 10-30 V for low voltage analog circuits and more than 30 V for power applications). Analog digital processes must also permit the production of the resistors, capacitors and isolated PNP transistors needed in analog circuits in addition to allowing the fabrication of NPN bipolar and CMOS structures. Analog circuit requirements are such that they can still be met by devices built with less aggressive design rules than those needed in digital circuits.

3.2 Medium Voltage Analog-Digital BiCMOS

As mentioned earlier, the possibility to produce analog and digital functions on the same chip provides significant benefits to the manufacturer of ICs. For example, CMOS can be used to minimise DC power dissipation and provide high impedance FET inputs for certain operations. Bipolar devices can not only provide high current gain and extended bandwidth capabilities but they can also be used to minimise noise factors and provide good on chip voltage references.

The differences between analog-digital BiCMOS and 5 V digital BiCMOS processes stem primarily from the fact that analog functions generally operate over a much wider range of power supply voltages (higher than 10 V) and power dissipation levels. However, medium voltage analog-digital circuits require 10-15 V operating voltages in order to maintain high signal to noise ratios and to permit the use of cascading in analog design. Some CMOS speed performance must be traded off to gain reliable operation at the increased voltage levels, for example thicker gate oxides are needed to withstand higher gate voltages while due to this, MOS transistor transconductances are reduced.

For analog function circuit design, the most important device characteristics are those of NPN transistors. High gain is required to reduce input bias current into transistor and to prevent the loading of a previous stage. A value of 100 or more is usually satisfactory and f_T values above 2 GHz are welcome. The transistors must also have low R_C values (below 100 Ω) to allow high current operation, as well as high Early voltage (V_A) values (greater than 50 V), since, as noted in section 2.1.2, the intrinsic small signal voltage gain of an amplifier is proportional to V_A.

Isolated PNP transistors are also needed in some analog circuits. Although lateral PNP transistors are "free" devices, their speed performance is poor. So in certain cases vertical isolated PNP transistors must be built to satisfy above requirements.

The higher operating voltages also limit the minimum gate lengths of MOS devices to 2-3 μm in analog-digital BiCMOS to prevent premature breakdowns and short

channel effects. Furthermore, since analog designs often use both positive and negative supply voltages, isolated CMOS structures are desirable.

Thicker field oxides are also usually needed to provide field region threshold voltage values that exceed the maximum operating voltage. Likewise, the CMOS devices must be protected against hot carrier effects that arise as a result of exposure to higher supply voltages. Latchup is another concern due to high substrate currents common in many analog BiCMOS designs.

3.3 Triple Diffused BiCMOS Technology

Triple diffused (3D) BiCMOS technology has got its name according to the way that bipolar NPN or isolated PNP transistors are produced. In this case *all three* transistor regions: Emitter, Base and Collector are first successively doped, usually by ion implantation, and then separately *diffused* into silicon substrate to form corresponding areas.

The easiest way to realise such an approach is to start with "digital" high yielding n-well CMOS process to which certain process modules are added, /4/. Basic CMOS allows the formation of standard MOS structures which are well characterised while with new modules bipolar vertical NPN transistors, isolated vertical PNP transistors, double poly capacitors and high resistivity polysilicon resistors are made. This approach is depicted in figure 3.

Please, note that this modular approach allows easy tailoring of the technology to the specific needs of the design, as well as easy deletion or addition of the components in question.

3D BiCMOS as presented here has some advantages and some disadvantages regarding analog-digital design.

Advantages are the following:

- starting material is the same as for the established n-well digital CMOS which means that there is no need to buy expensive EPI wafers
- this process does not require formation of buried layers
- basic process flow is altered only as much as needed which assures high yield and built-in reliability
- there is no need to buy new generation of equipment: all new modules can be realised with the equipment which is already on the floor

Disadvantages are the following:

- bipolar transistors are not optimised regarding low collector resistance
- although simple to start with, 3D BiCMOS becomes complex with addition of new masks if we want to optimise several device parameters at a time
- BiCMOS built on wafers without EPI is more susceptible to latch up and less immune to noise

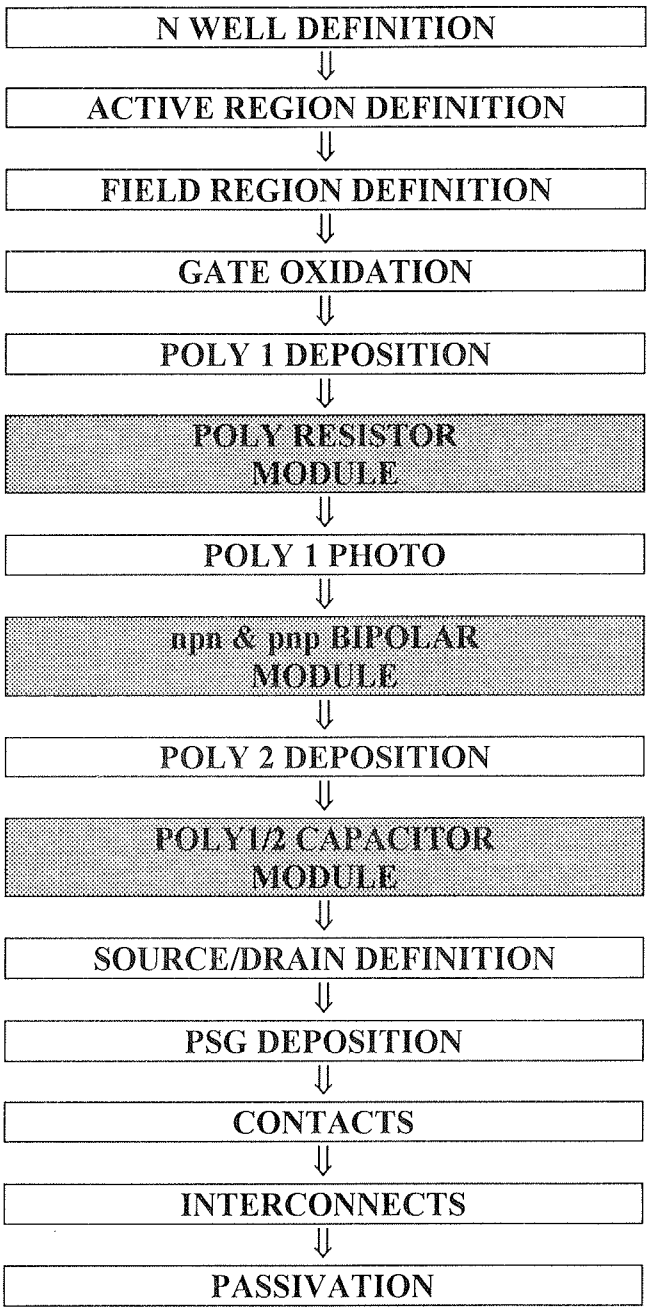

Fig. 3: Simplified flow chart of 3D BiCMOS process showing modules added to basic n-well CMOS in order to make vertical NPN and PNP bipolars, double poly capacitors and polysilicon resistors

In the next sections the overview of all active and passive components that can be built with 3D BiCMOS is presented.

3.3.1 MOS Transistors

The structure of NMOS and PMOS transistors is a basic one as can be seen in figure 4. N type polysilicon gate together with gate oxide and channel implant define threshold voltage which is one of the most important

transistor electrical parameters. Its typical value range is between 0.6 V and 1.0 V, figure 5. It is important to mention that PMOS transistor is of a buried channel type, since its surface is, due to boron channel implant, p type and conduction channel is actually formed below the surface.

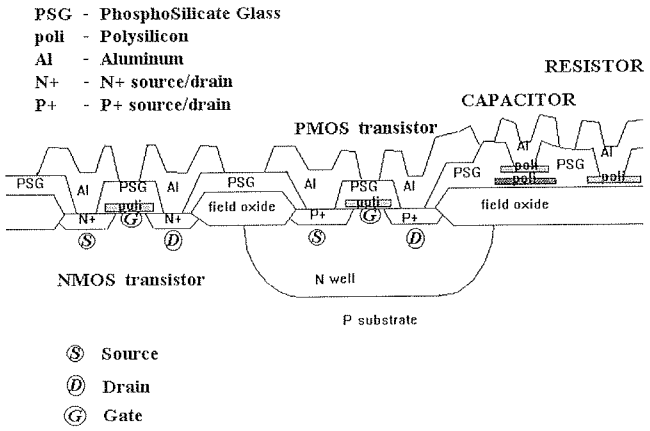

Fig. 4: Cross section of the basic CMOS process showing NMOS and PMOS transistors, double poly capacitors and polysilicon resistors

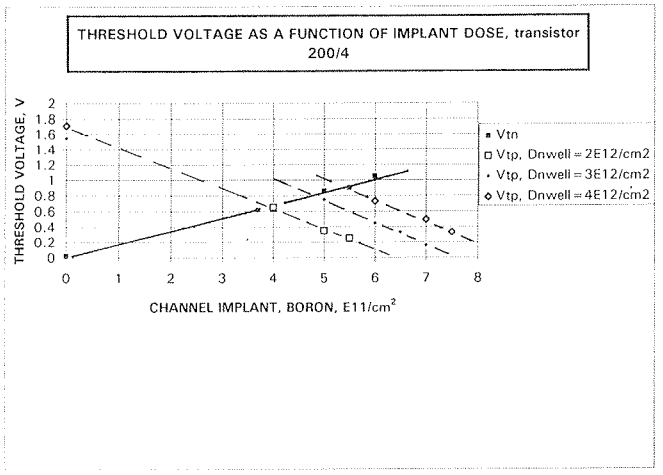

Fig. 5: NMOS and PMOS transistor thresholds as a function of n well and channel implant doses.

Concentration of the p substrate for NMOS and of the n well for PMOS transistors, defines their body factors which describe the behaviour of threshold voltage as a function of applied substrate bias. Due to higher n well concentration, compared to p substrate, PMOS transistors have higher body factor. Ideally, it should be as low as possible.

Another important transistor parameter is its transconductance which is given as :

$$g_m = \mu \cdot C_{OX} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{DS} \qquad (9)$$

μ : charge mobility

C_{OX} : gate capacitance per unit area

W_{eff} : effective channel width

L_{eff} : effective channel length

V_{DS} : drain to source voltage

Device designer would like to have as high transconductance as possible. This can obviously be achieved with high mobility, large gate oxide capacitance (thin gate oxide), wide and short channel and high applied voltage. Of course, all these parameters can not be altered deliberately. On one side, electron (hole) mobility decreases with increasing channel concentration, increasing gate voltage and finally with increasing lateral electric field which is defined as the ratio of applied voltage and effective channel length. Also, too thin gate oxide can cause reliability problems, while short channel effects can cause premature transistor breakdown and excessive leakage currents. Generally, we can say that maximum allowable substrate concentration is dictated by maximum allowable values of body factor and parasitic junction capacitances in the chip. On the other side, high substrate concentration allows higher transistor breakdowns and less pronounced short channel effects. The same is true for channel doping: its maximum value affects subthreshold swing and charge mobility while low values allow premature surface breakdown. To conclude: careful device design is needed which must take into account all these factors to bring all important transistor electrical parameters within the acceptable window for successful analog-digital design.

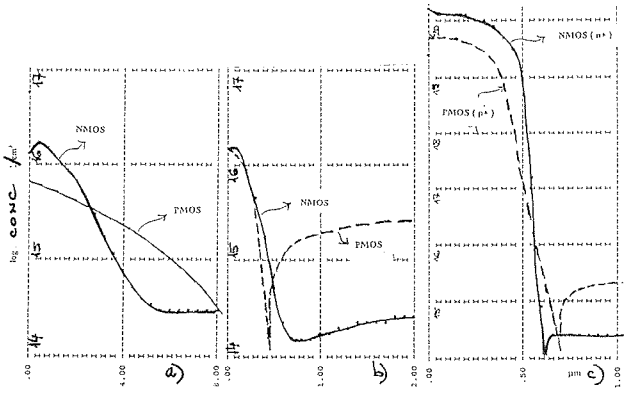

Fig. 6: Dopant profiles for different device regions, CMOS part of 3D BiCMOS
a) passive (field) region
b) active region, MOS transistor channel
c) active region, source/drain

In figure 6 simulated dopant profiles for different CMOS regions are depicted, while in table 2 some basic process and electrical parameters are presented.

Table 2: Typical process and CMOS device electrical parameters, 3D BiCMOS process

PARAMETER	unit	NMOS	PMOS
PROCESS PARAMETERS			
Gate oxide thickness	nm	70(50)	70(50)
Field oxide thickness	nm	1000	1000
Polysilicon thickness	nm	500	500
Junction depth, MOS source/drain	µm	0.54	0.64
Junction depth, n well	µm		9.5
ELECTRICAL PARAMETERS			
Power supply voltage, digital part	V	5	5
Power supply voltage, analog part	V	12	12
Field transistor threshold	V	>15	<-15
Active transistor threshold, 200/4	V	0.8	-0.8
Transconductance factor at V_{DS} = 0.1 V	$\mu A/V^2$	32	12
Body factor at V_{BS} = 5V	$\sqrt{V}$	0.23	0.76
Active transistor source - drain breakdown, BV_{DSS}	V	>15	<-15
Maximum carrier mobility	cm^2/Vs	696	260
Substrate concentration	$/cm^3$	3.2E14	3.8E15
Source/drain sheet resistivity	Ω/□	17	65
N well sheet resistivity	kΩ/□		4

All MOS discrete devices have been electrically characterised for their relevant parameters, their temperature dependence measured when necessary and their uniformity on the wafer evaluated. As an example, in figure 7 we show comparison of measured and calculated transistor characteristics using extracted SPICE parameters. Obviously, the match is satisfactory.

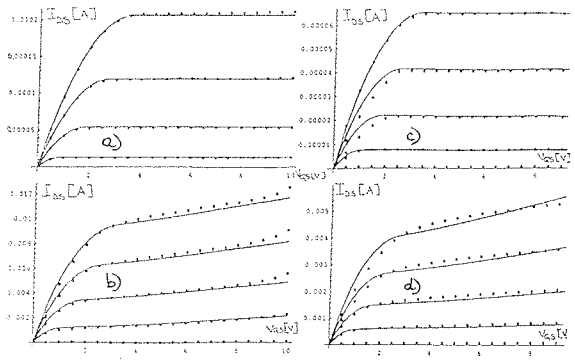

Fig. 7: Measured (points) and calculated (solid lines) transistor characteristics from SPICE
a) NMOS 100/100
b) NMOS 200/4
c) PMOS 100/100
d) PMOS 200/4

3.3.2 Composite Bipolar Transistor

Original n-well CMOS process allows formation of lateral isolated PNP and vertical PNP bipolar devices. However their performance is quite poor and usually they are used by designers as one composite device, where collector of the isolated PNP is tied to the wafer substrate which is at the same time collector for vertical PNP bipolar transistor, figure 8.

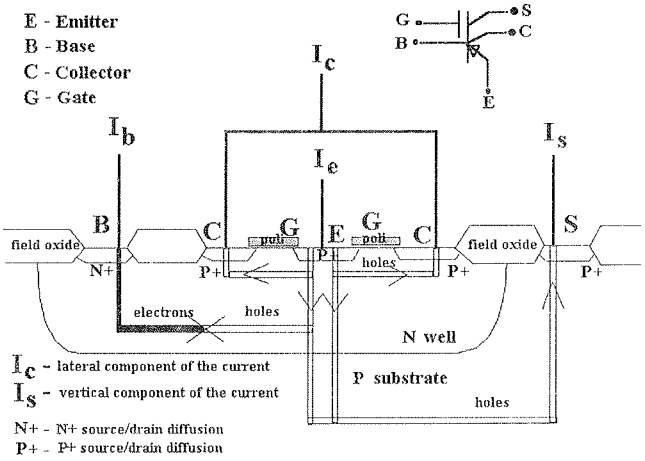

Fig. 8: Cross section and components of the current, composite PNP transistor

As can be seen from the figure 8, transistor base width is determined by difference in junction depths of its emitter and n-well in case of the vertical PNP device and by lateral distance between emitter and collector (two p+ source/drain diffusions) in case of the lateral PNP transistor. Please, note that in the particular transistor design shown in figure 8, polysilicon gate is used to define lateral E-C distance.

Transistor current components can be expressed as follows:

$$I_C = \alpha \cdot I_E \quad and \quad I_S = (1-\alpha) \cdot I_E \tag{10}$$

I_E : emitter current

$\alpha < 1$

I_S : substrate, collector current of the vertical PNP

Out of this we can define several transistor current gains as:

$$\beta_L = \frac{I_C}{I_B} \quad and \quad \beta_V = \frac{I_S}{I_B} \quad and \quad \beta_{tot} = \beta_L + \beta_V \tag{11}$$

β_L : lateral transistor common emitter current gain

β_V : vertical transistor common emitter current gain

β_{TOT} : composite transistor common emitter total current gain

Basically, designers could use each of the three transistors separately. In that case, their common emitter current gains are defined with equation 11. In case only isolated lateral PNP is needed, it should be optimised regarding lateral current component by increasing periphery to area ratio and by minimising vertical current component. The opposite is true for vertical PNP transistor.

In table 3 typical electrical parameters of the composite PNP bipolar transistor are given.

Table 3 : Typical electrical parameters for the composite PNP bipolar transistor, 3D BiCMOS process

PARAMETER	unit	value	comment
Emitter area	μm^2	8 x 8	changeable
Maximum common emitter current gain		150-200	process dependent
Collector series resistance	Ω	500-800	process dependent
Early voltage	V	<70	process dependent
BV_{EBO}	V	35-40	process dependent
BV_{CBO}	V	35-45	process dependent
BV_{CEO}	V	25-30	process dependent

Process parameters which affect composite PNP transistor electrical parameters and which can be changed during the process are:

- transistor lateral dimensions (polysilicon mask change)
- implant and well diffusion conditions for n-well definition
- implant and n+/p+ diffusion conditions for source/-drain definition

3.3.3 Vertical Isolated NPN Transistor

We need to introduce at least one new mask, one implant and one high temperature step to be able to make vertical isolated NPN transistor which would be suitable for analog design. After polysilicon resistor mask, the following steps should be added to the basic CMOS flow chart, figure 9:

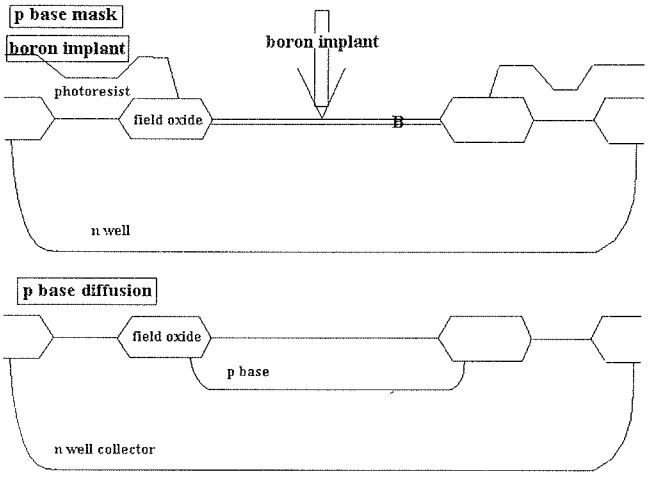

Fig. 9: Process steps needed to make collector and base of the vertical isolated NPN bipolar transistor, 3D BiCMOS process

- p base mask
- p base implant, boron, 100 keV, dose in the range 0.5 - 3E13/cm^2
- p base diffusion

In this case, transistor collector is defined with n-well mask, n-well implant and diffusion conditions, its base with the above described process steps, while emitter is defined with same process steps as NMOS transistor's source/drain.

Table 4: Vertical isolated NPN bipolar transistor electrical parameters as function of process parameters, 3D BiCMOS process, minimum size transistor

n well dose /cm^2	p base dose /cm^2	W_B simulated µm	β max	rc kΩ	BV_{EBO} V	BV_{CBO} V	BV_{CEO} V	V_A V
4.5E12	9E12	1.35	350	0.869	18	43	43	55
4.5E12	1.25E13	2.85	110	1.67	18	52	52	>60
4.5E12	2E13	3.2	60	1.73	15.5	68	68	>60
3E12	2E13	3.48	66	4	16.4	90	90	
2E12	2E13	3.76	65	16.6	16.4	105	105	
1E12	2E13	3.96	1	17.3	14	90	90	

Of course, transistor electrical characteristics are very sensitive to the process conditions used to make its active regions. This is well demonstrated in table 4, where basic isolated NPN transistor electrical parameters are shown together with some process data.

Immediately, we notice that high enough current gains (usually above 100 is required), figure 10, and suitable breakdown voltages can easily be achieved, while collector series resistances are very high, as expected. Also, Early voltages are well above the limits needed for analog design.

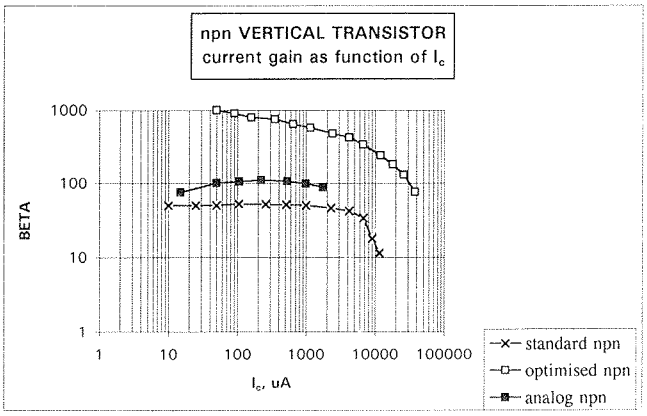

Fig. 10: Current gain as a function of collector current, vertical isolated NPN bipolar transistor, 3D BiCMOS process

High collector series resistance calls for some immediate corrective actions which will be described in the next section.

3.3.4 Collector Series Resistance Optimisation - NPN Vertical Bipolar Transistor

In figure 11, different contributions to collector series resistance are shown. Besides lateral contribution (r_{Cl}) due to collector current flowing below base, there is also vertical contribution due to current flowing into the surface contact (r_{Cv}). Ideally, both of them should be as low as possible.

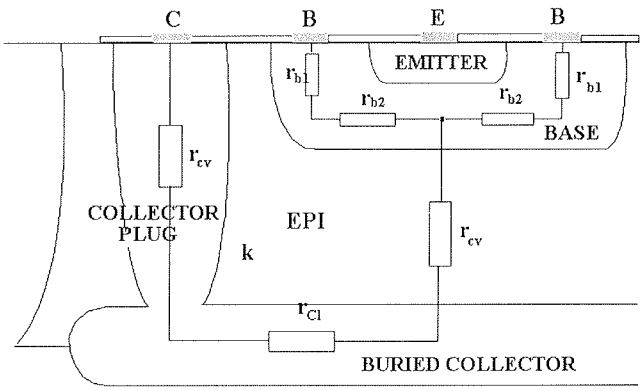

Fig. 11: Contributions to collector series resistance, vertical NPN bipolar transistor

There are two basic approaches for diminishing collector series resistance:

- process
- geometric

Process approaches usually require addition of one or more process steps (mask, implant, diffusion) while geometric approaches require change in device geometry. We will first describe some process and then one geometric approach to device collector series resistance optimisation.

Introduction of Extra Collector N-Well

In order to diminish lateral and vertical component of collector resistance, we must increase collector doping level. If we use the same well as for MOS devices we can not alter its concentration deliberately since we are limited by required active MOS devices performance, which would be affected by this change.

So, in order to be flexible enough, we must introduce new collector n-well which background concentration must be much higher than that of the device n-well. Of course, this requires at least one new mask and one phosphorous implant more while collector n-well diffusion can be done at the same time as device well diffusion.

In figure 12 we show the effect of extra collector well implant on collector resistance of vertical NPN bipolar transistor. Unfortunately, other device parameters are also changed. This can be seen in table 5. By increasing collector concentration we decrease its resistance and all transistor breakdown voltages, while current gain increases. Of course, for analog design there is an optimum set of process conditions which must be used to make suitable vertical NPN transistor. Taking this into account, we see that collector resistance reduction that can be achieved by this method is in the range of 50%.

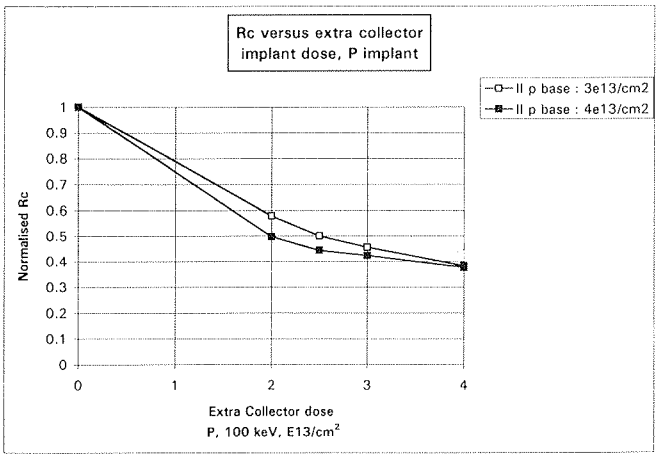

Fig. 12: Collector resistance relative change as a function of extra collector well implant dose, vertical isolated NPN bipolar transistor

Table 5: Effect of extra collector well implant on electrical parameters of vertical NPN bipolar transistor, 3D BiCMOS process, minimum size transistor

Collector well dose /cm^2	W_B simulated µm	β max	r_c normalized	BV_{EBO} V	BV_{EBO} V	BV_{EBO} V
3E12	3.9	55	1	16	95	51
2E13	2.1	120	0.58	19	25	18
2.5E13	1.9	158	0.5	21	21	15
3E13	1.7	293	0.46	21	20	13
4E13	1.3	780	0.38	28	18	11

Introduction of Collector Plug

We have seen that higher collector well doping affects whole transistor area and all of its electrical parameters. It would be ideal if we were able to increase collector doping only in its passive area, away from base. In fact, this can partially be achieved by additionally implanting only collector contacts as shown in figure 13. In this way only vertical part of collector series resistance would be affected. This implantation is performed prior to base diffusion and requires additional "plug" mask which is in effect reverse p base mask which allows implantation only in the transistor collector contact areas. Again, phosphorous is implanted and total emitter contact & plug profile is shown in figure 13b.

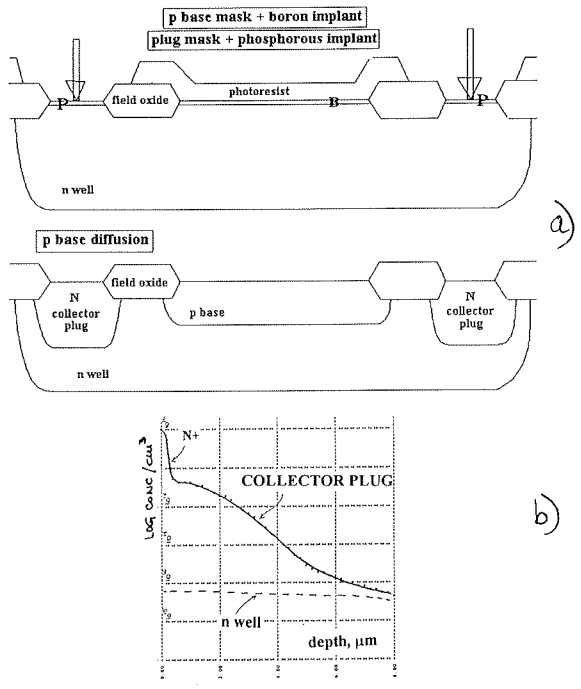

Fig. 13: a) Process steps needed to make collector plug of the vertical isolated NPN bipolar transistor, 3D BiCMOS process
b) Doping profile of the collector plug, SUPREM simulation

By introducing collector plug we expect to further decrease collector series resistance by 50%.

Buried Collector

The most effective way to lower only lateral component of collector series resistance is to increase collector doping level below base leaving enough space between base and buried collector not to affect BV_{CBO}, figure 11. This is usually achieved by first selectively implanting all collector areas in a chip with arsenic and then by growing silicon EPI layer over it. In the EPI layer all active devices are then built above their respective buried layers.

This approach requires EPI reactor in house or use of EPI deposition service in another company.

Although being the most effective, this approach is also the most expensive.

There exist some other techniques to make buried layers without need for subsequent EPI deposition. One of the most exotic ones is high energy ion implantation /10/. In this case phosphorous (arsenic) is implanted through suitable mask 1 to 3 µm deep into silicon to make high concentration buried layer below NPN transistor base. Again, this approach requires expensive equipment and is limited in the depth to which ions can be implanted.

Neither of the above two mentioned techniques for formation of buried layer were implemented into our 3D BiCMOS process.

Transistor Topology Optimisation

Standard vertical NPN transistor geometry is shown in figures 14a and 15a. Emitter is in the middle of the structure, completely surrounded by the base and col-

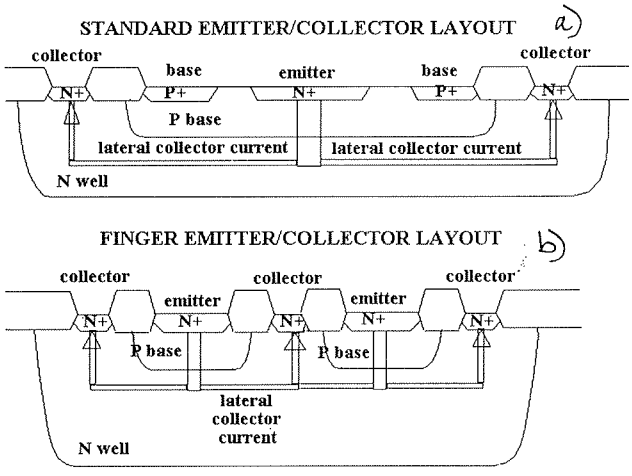

Fig. 14: Cross section of vertical NPN transistor
a) structure with emitter in the centre
b) structure with interdigitated emitter and collector

lector. Since collector current flows laterally below the base, lateral component of collector series resistance is directly proportional to the distance between emitter and collector contacts on the surface. In order to lower this resistance, we should make these two contacts as close to each other as possible. This is actually achieved by finger layout where emitter and collector are interdigitated, figures 14b and 15b.

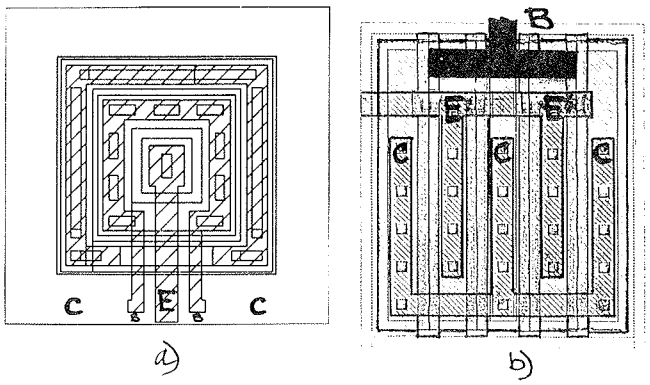

Fig. 15: Layout of vertical NPN transistor
a) standard layout with emitter in the middle
b) optimised layout, structure with interdigitated emitter and collector

Comparison of the current characteristics of two bipolar NPN transistors with approximately equal emitter areas shows pronounced improvement of collector series resistance of the finger structure compared to standard one, figure 16.

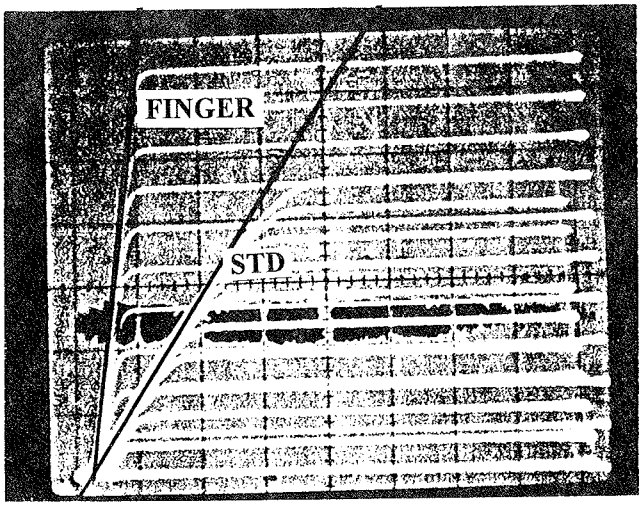

Fig. 16: Comparison of the current characteristics of two bipolar NPN transistors with approximately equal emitter areas,
$r_{C\ standard} / r_{C\ finger} \approx 4$.

Conclusion

In this section we have shown that we are able to make vertical isolated NPN bipolar transistor with the electrical parameters very suitable for analog applications.

We can easily obtain current gains well above 100, all breakdown voltages above 18 V and Early voltage in the range of 50-60 V. Due to its inherent structure, 3D vertical NPN transistor has high collector series resistance. However, with some improvements in the geometrical layout of the structure, with introduction of one to two new masks and ion implant steps we can lower this resistance by factor of 4-8, compared to standard - one added mask 3D BiCMOS NPN transistor. This means that by increasing 3D BiCMOS process complexity we are able to bring collector series resistance down to the values acceptable for analog design.

3.3.5 Vertical Isolated PNP Bipolar Transistor

The idea behind making another, this time isolated vertical PNP transistor (remember: vertical PNP already comes for free in original CMOS, but with wafer substrate as its collector) is to use p base of vertical NPN as the collector for isolated vertical PNP transistor. Of course, this can be achieved by adding another n base mask after p base diffusion and by implanting n base areas of PNP transistor with phosphorous. A short drive in cycle follows this implantation to allow phosphorous to diffuse deeper into the base. Cross section of vertical isolated PNP transistor together with its simulated profile is shown in figure 17.

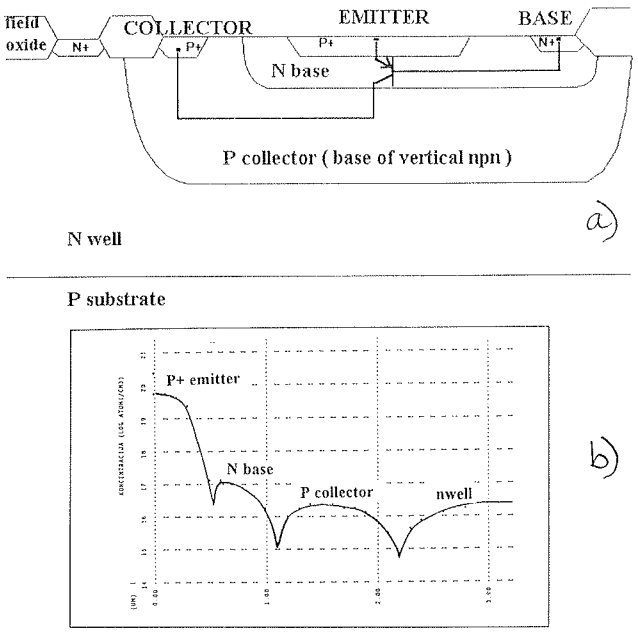

Fig. 17: Vertical isolated PNP bipolar transistor, 3D BiCMOS process
a) cross section
b) simulated SUPREM profile

Electrical characteristics of such a transistor are very attractive as shown in table 6. As well its current gain versus collector current is depicted in figure 18.

Table 6: Vertical isolated PNP bipolar transistor, basic electrical parameters, emitter area 20x20 μm², 3D BiCMOS process

W_B, simulated μm	β_{max}	BV_{EB0} V	BV_{CB0} V	BV_{CE0} V	V_A V
0.73	110	11.5	32	17	11

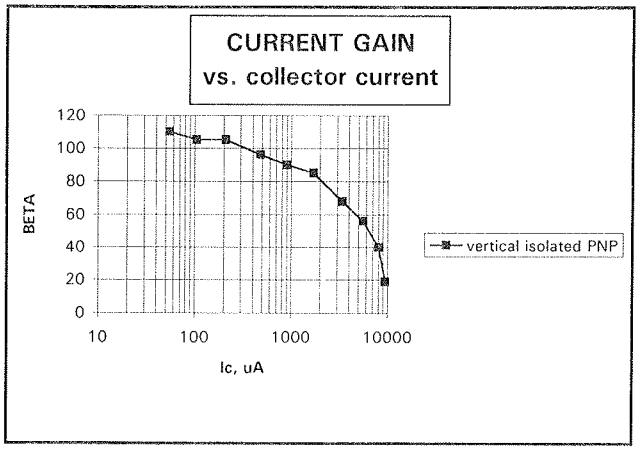

Fig. 18: Common emitter current gain as function of collector current, vertical isolated PNP bipolar transistor, 3D BiCMOS process

3.3.6 Integrated Diodes

Any of the several pn junctions made in 3D BiCMOS process can be used as a diode. They come for free although their leakage current, as well as capacitance are parasitic parameters, unless used on purpose. In table 7 we present an overview of all possible diodes encountered in our particular 3D BiCMOS process.

3.3.7 Integrated Capacitors

3D BiCMOS technology offers wide spectrum of diffused and MOS capacitors. In today's modern design of analog digital ASICs, the designers relatively seldom use dif-

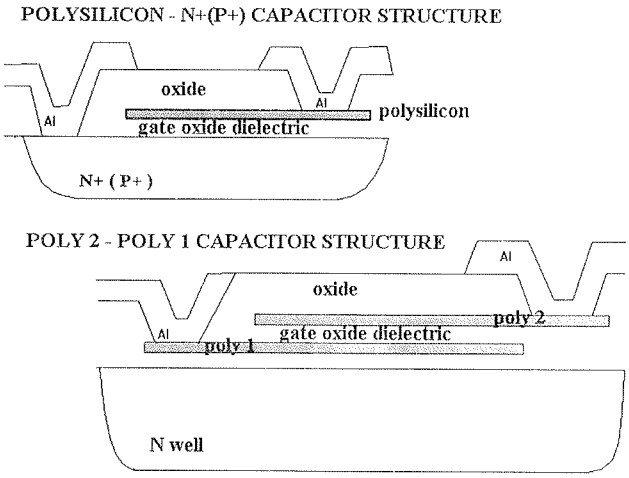

Fig. 19: Cross section of two possible capacitor structures, 3D BiCMOS process

Table 7: All possible diode structures in 3D BiCMOS process

DIODE TYPE	DIODE STRUCTURE	BV at 10 μA, V	COMMENT
n+ psub	n+: source/drain of NMOS psub: p substrate	>19	breakdown of n+ to p field
n+ pbase	n+:source/drain of NMOS pbase: base of a vertical NPN	10	
nbase psub	nbase: base of a vertical PNP psub: p substrate		
nbase pbase	nbase: base of a vertical PNP pbase: base of a vertical NPN	>30	affected by base doping
nwell psub	nwell: nwell for PMOS psub: p substrate	190	affected by substrate resistivity
p+ nwell	p+: source/drain of PMOS nwell: nwell for PMOS	-19	breakdown of p+ to n field
p+ nbase	p+: source/drain of PMOS nbase: base of a lateral PNP	-35	breakdown of p+ to n well
p+ nbase	p+: source/drain of PMOS nbase: base of a vertical PNP	-12	breakdown of p+ to n base of PNP
pbase nwell	pbase: base of a vertical NPN nwell: nwell for PMOS	-95	affected by nwell doping
n+ p+ ZENER	n+: source/drain of NMOS p+: source/drain of PMOS	5.3 - 5.6	lateral ZENER diode

fused capacitors due to their voltage dependent capacitance. MOS capacitors are more interesting since high capacitance per unit area and voltage independence can be easily achieved.

Two MOS capacitor structures are of great importance, as shown in figure 19: polysilicon to n+ (p+) capacitor and double poly capacitor.

In both cases we use silicon dioxide as the dielectric, grown during gate oxide step. Capacitance of such a structure is given with the expression:

$$C = \frac{\varepsilon \cdot \varepsilon_0}{d_{ox}} A \qquad (12)$$

ε : silicon dioxide dielectric constant (3.8)

dox : capacitor oxide thickness

A : capacitor area

Since oxide thickness is usually in the range of 50-90 nm, typical obtained capacitance is in the range of 0.37-0.67 fF/μm^2. In our particular case, this capacitance is 0.4± 0.02 fF/μm^2.

With both presented structures we can make capacitors which are voltage independent (less than 50 ppm/V), with low temperature coefficient of capacitance (below 30 ppm/°C), as well as achieved capacitance ratios are within 0.1%. However, double poly capacitor structure is the most popular one in analog digital design due to its low leakage current towards substrate.

Designers of analog circuits usually use so called "unity" capacitors with which very precise capacitance ratios can be achieved. These capacitors are usually square in geometry with absolute capacitance in the range of 1 pF. In such a case its dimensions would be 50 μm x 50 μm. Change in absolute capacitance is due to variation of capacitor area, dielectric thickness and its dielectric constant. Summing all these contributions we arrive to the capacitance relative accuracy value of ±6% within one lot. However, better results can be achieved for matching, as we will see later.

3.3.8 Integrated Resistors

General

3D BiCMOS process allows realisation of:

- diffused and
- thin film

resistors, table 8. Diffused resistors are defined usually by ion implantation and then by subsequent diffusion step. All implants used in the process like nwell, pbase, nbase, n+, and p+, already give resistors with sheet resistivity in the range 25-4000 Ω/□.

There are also two thin film resistors: polysilicon and aluminium. While aluminium has very low sheet resistivity (about 35 mΩ/□ for the thickness of 1 μm), polysilicon looks more promising since its resistivity can be changed by thickness and doping variation within very broad range.

In figure 20 the geometries of diffused and thin film resistors are compared. In both cases their resistance is defined by the equation:

$$R = \rho \cdot \frac{L}{d \cdot W} = R_{sh} \cdot \frac{L}{W}, \quad R_{sh} = \frac{\rho}{d} \qquad (13)$$

ρ : specific resistivity of the film or doped region

L : resistor length

W : resistor width

d : resistor thickness

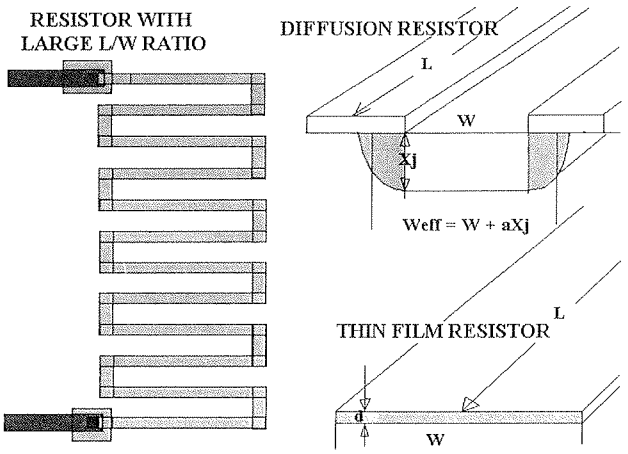

Fig. 20: Geometry and structure of diffused and thin film resistors, 3D BiCMOS process

Diffused resistor lateral dimensions are defined with active mask (for p+, n+, pbase or nbase resistor) or nwell mask (for nwell resistor). Polysilicon resistor lateral dimensions are defined only by poly mask and plasma etch step. Absolute mask dimension accuracy is in both cases similar while for diffused resistor we know that side dopant diffusion additionally affects its lateral dimensions especially in the case of deep well. In this case we must rewrite equation 13 as:

$$R = R_{sh} \cdot \frac{L}{W_{eff}} = R_{sh} \cdot \frac{L}{W + \alpha \cdot x_j}, \quad \alpha < 1 \qquad (14)$$

xj : junction depth, diffused resistor

Weff : effective resistor width

Even in the case of large L/W ratios relative accuracy achieved is in the range ±6 % for low R_{sh} and ±10% for high R_{sh} resistors within one wafer lot.

One big drawback of weakly doped diffused resistors (nwell, pbase, nbase) is their voltage dependent resistance. This happens because depletion layer width changes with voltage, inducing resistor geometry and consequently its resistance change.

Table 8: Overview of diffused and thin film resistors, 3D BiCMOS process

RESISTOR	Dopant	R_{sh} Ω/□	Relative accuracy, %	Temp. coeffic. Ω/□/°C
n+ diffusion	AS implantation	17	6-8	0.06
p+ diffusion	B implantation	65	6-8	0.08
n well	P implantation	3500	10-20	
n base	P implantation	≥800		
p base	B implantation	≥700		
n+ poly1 or poly2	P, gaseous source	25	5	0.02
n/p poly	P/B implantation	500-40000	5-15	-41 at 10kΩ/□

High Sheet Resistivity Polysilicon Resistors

Polysilicon resistors are suitable for analog design since their geometry and doping levels can be precisely controlled within wide value range without need to worry about resistance voltage dependency like in the case of diffused resistors. As well, they are not made in the substrate which means that parasitic leakage currents and parasitic capacitances are very low.

Figure 21 presents poly sheet resistivity variation with ion implant dose for polysilicon thickness of about 500 nm. We can clearly see that sheet resistivities in the range of 500-40000 Ω/□ can be achieved.

However, when designing polysilicon resistors, we must be aware that their sheet resistivity, uniformity on the wafer and resistance matching depend on the following parameters, /11/ :

- polysilicon thickness
- dopant type and implant dose
- polysilicon deposition parameters
- polysilicon thermal history during subsequent processing
- final low temperature anneal conditions during Aluminium alloy
- final passivation type

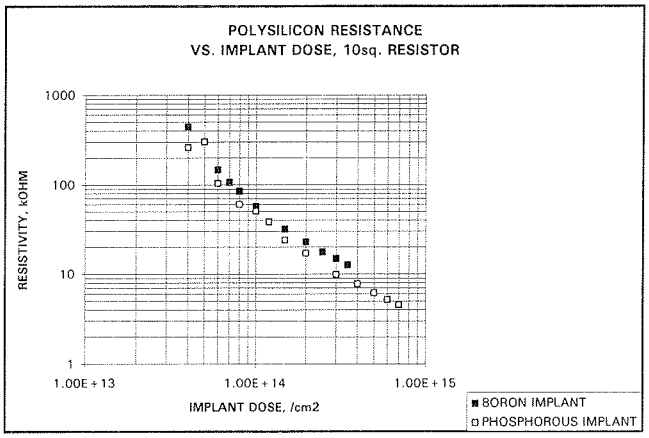

Fig. 21: Polysilicon resistance variation with ion implant dose, 3D BiCMOS process

As an illustration of above statements we show in the figure 22 polysilicon sheet resistivity change with time of anneal in hydrogen at 450°C. Hydrogen diffusion through polysilicon and its segregation on the surface of poly grains causes effective increase of free dopant concentration, consequently lowering polysilicon resistance. We see similar effect when depositing plasma silicon nitride passivation above poly resistors. It is well known that PECVD nitride contains up to 10% of free hydrogen which, during aluminium alloy, diffuses to polysilicon, causing similar resistance changes described previously.

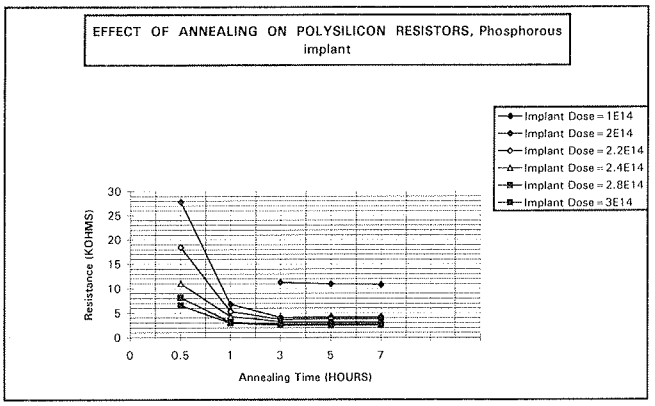

Fig. 22: Polysilicon resistance variation with anneal time in hydrogen at 450°C.

3.4 Matching of Active and Passive Devices

When talking about changes of dimensions and electrical parameters of active and passive devices in 3D BiCMOS process, we must differentiate between two basic ideas:

- global changes of parameters on a wafer or within a lot
- local changes within single chip, or difference of the same parameter between two neighbouring elements in the same chip; the degree to which we can make two devices equal locally, is cold matching

Today's design of precision analog ICs is based on devices' and their parameters' ratios rather than absolute values. This means that the precision of most analog operations within an IC is limited by poor device matching. That's why it is important to evaluate critical parameters' matching and find out reasons for mismatch.

In table 9 we bring an overview of typical values of dimensional and electrical parameters' matching for active and passive devices. Matching is defined as a difference in parameter value (absolute matching) divided with its average value (relative matching) for two neighbouring devices.

Table 9: Typical parameters' matching values, 3D BiCMOS process

PARAMETER	SYMBOL/ UNIT	TYPICAL VALUE	MATCHING max σ
MOS TRANSISTOR			
Threshold Voltage	V_{TH}, V	0.8	1%
Mobility (n)	μ_n, cm^2/Vs	700	≤1%
Mobility (p)	μ_p, cm^2/Vs	300	≤1%
Capacitance, Gate Oxide	C_{OX}, $fF/\mu m^2$	1.12	0.1%
Channel Length, Drawn	L, μm	1-5	0.1 μm
Channel Width, Drawn	W, μm	2-2000	0.1 μm
POLY2-POLY1 CAPACITOR			typical σ
Dielectric Constant	ε_{OX}	3.8	0.02%
Thickness, Gate Oxide	t_{OX}, nm	50	0.03%
Thickness, Poly1 Oxide	t_{OX}, nm	80	0.05%
Capacitor Length	L, μm	10-500	0.1 μm
Capacitor Width	W, μm	10-500	0.1 μm
DIFFERENT RESISTORS			
Diffused	R ,Ω/□	40	2%
Poly1, Difussed	R ,Ω/□	30	1%
Poly1, Implanted	R ,Ω/□	1000	1%
Resistor Length	L, μm	2-2000	0.1 μm
Resistor Width	W, μm	1-20	0.1 μm

Using above values, we can calculate matching of transconductance parameter for two neighbouring MOS transistors, as follows, /12/:

$$\frac{\sigma_k^2}{k^2} = \frac{\sigma_L^2}{L^2} + \frac{\sigma_W^2}{W^2} + \frac{\sigma_\mu^2}{\mu^2} + \frac{\sigma_C^2}{C^2} \qquad (15)$$

Taking for L = 3 μm and W = 6 μm, we get σ_k/k = 3.8 %. However, choosing larger transistors with L = 12 μm and W = 48 μm, matching goes down to about 1 %. Similarly, we can anticipate V_{TH} matching to 1 %, which gives us final MOS transistor current matching between 1-5 % !! Very important conclusion is that V_{TH}, k and I matching depend very much on transistor geometry. So, it is very important to use long and wide transistors for optimum matching.

We can draw similar conclusions for polysilicon resistors matching. Actually, we have measured matching of two neighbouring polysilicon resistors on couple of wafers made with 3D BiCMOS process. The results are shown in figure 23 for a wafer with average poly sheet resistivity of 5 kΩ/□ .

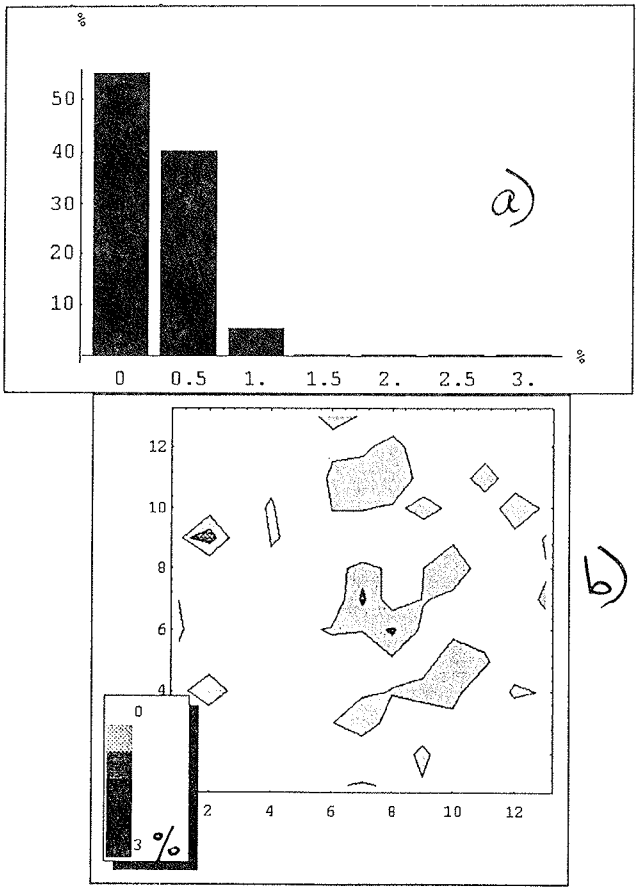

Fig. 23: Polysilicon sheet resistivity matching
a) histogram and
b) on wafer uniformity in %.
Two neighbouring polysilicon resistors with same dimensions, L = 200 μm, W = 20 μm.

Below 1% matching of resistors is typical for the average polysilicon sheet resistivity value of about 5 kΩ/□. Even better matching was observed for lower values of sheet resistivities (higher implant doses) and larger W/L ratios, as expected.

We did not directly evaluate double poly capacitance matching. However, indirect measurements of SC filter performance indicate matching to be in the range of 0.1 %.

4. CONCLUSION

We are able to join typically good CMOS technology performances as:

- low power consumption,
- almost infinite MOS transistor input impedance,
- low price per function,
- high yielding, mature digital technology,

with good bipolar transistor-technology performances like:

- large transconductance,
- low noise,
- low offset voltage,
- good driving capabilities of large capacitive loads,
- predictable temperature behaviour,

into **BiCMOS** - a new technology which offers better price-performance ratio, a lot of flexibility to the designers and a new step ahead with almost zero investment into new process equipment and clean room.

Out of several possible BiCMOS technologies, we have developed 3D BiCMOS suitable for making medium power supply voltage analog - digital ICs.

The idea behind our approach is to start with standard digital nwell CMOS technology to which certain process modules are added which allow realisation of additional:

- double poly capacitors
- high sheet resistivity polysilicon resistors
- vertical isolated NPN bipolar transistors
- vertical isolated PNP bipolar transistors

In order to allow optimisation of each of the above components for analog - digital design, several masking, implant and diffusion steps are added, thus increasing process performance and complexity. In table 10, we bring an overview of respective growing process complexity in terms of mask and process step numbers.

Table 10: Comparison of several 3D BiCMOS processes regarding process complexity

Process Steps	Digital CMOS	Analog-Digital CMOS with capacitors and poly resistors	Analog-Digital BiCMOS with simple NPN	Analog-Digital with optimised NPN	Analog-Digital BiCMOS with optimised NPN and isolated PNP
MASK LEVELS	8	10	11	13	14
PLASMA ETCHING STEPS	3	4	4	4	4
IMPLANT	5	7	8	10	11
DIFFUSION	16	17	18	18	19

Such an approach allows process tailoring to the designers' needs, as well as we believe that it is cost-performance competitive to the modern BiCMOS processes being developed for the specific product range of 10-15 V power supply analog - digital ASICs.

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Prispelo (Arrived): 07.03.95 ***Sprejeto (Accepted): 20.03.95***

ANALYSIS OF CONTACT LAYERS IN MINIATURE ELECTRICAL RELAYS WITH AUGER ELECTRON SPECTROSCOPY

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Keywords: electrical contacts, miniature relays, contact quality, cleaning of contacts surfaces, ion etching, sputter-etching processes, AES analysis, AES, Auger electron spectroscopy,surface composition of contacts, contact surface contamination, contact alloys, impurities of alloys, impurity detection

Abstract: The surface composition of miniature electrical relay contacts was investigated with Auger electron spectroscopy. Surprisingly, large amounts of contaminants (carbon, sulphur, oxygen, calcium), were detected in addition to gold, iron, nickel and cobalt, nominally composing the contact alloy. To improve the technology of relay contacts several phases of technological process were examined. Some models of explaining the behaviour of contaminating elements under various experimental conditions such as temperature, sputter-etching process etc are given.

Analiza kontaktnih površin miniaturnih relejev z Augerjevo elektronsko spektroskopijo

Ključne besede: kontakti električni, releji miniaturni, kakovost kontaktov, čisčenje povrsin kontaktov, jedkanje ionsko, procesi naprsevalno-jedkalni, AES analize, AES Auger spektroskopija elektronska, sestava povrsin kotaktov, zlitine kontaktne, nečistoče zlitin, detekcija nečistoč

Povzetek: S spektroskopijo Augerjevih elektronov smo studirali strukturo povrsine kontaktov miniaturnih električnih relejev. Poleg zlata, _eleza, niklja in kobalta, ki sestavljajo kontaktno zlitino, smo detektirali presenetljivo velike količine nečistoč: ogljika, _vepla, kisika in kalcija. Z namenom, da bi izboljsali tehnologijo relejskih kontaktov, smo raziskovali različne faze tehnoloskega postopka. Podajamo nekaj modelov, s katerimi razlagamo obnasanje elementov nečistoč pod različnimi eksperimentalnimi pogoji, kot so temperatura, proces ionskega jedkanja itd.

I. INTRODUCTION

Few data have appeared in the literature on the composition of the first few layers of any contact material. Therefore in our research in development of contacts we are interested in finding out the composition of these layers because they dictate the behaviour of contacts.

The Auger electron spectroscopy was chosen to establish the surface composition of contacts since it provides qualitative and semiquantitative information about elements in the upper three to five atomic layers. Only hydrogen and helium can not be detected /1-6/. The Auger peak to peak height, i.e. the distance between the positive and negative extreme of an Auger line in the dN/dE plot versus energy is in first approximation proportional to the element concentration /7/, though the sensitivity is not the same for all elements.

The contacting alloy was composed of gold, iron, nickel and cobalt, and of gold, iron and nickel either. Surprisingly large amounts of contaminants such as carbon, sulphur, oxygen, calcium, silicon and chlorine were detected. To find out the source of these contaminants the relay contacts in various phases in technological process were examined. The results helped us to improve the technology.

II. EXPERIMENTAL

Analyses were performed on the Auger system /2,5,6/ manufactured by Physical Electronics Industries, using a cylindrical mirror analyser with a coaxial electron gun. The diameter of the electron beam on the target was 0,3 mm. Both surface analysis (AES and sputter-etching) could be performed without moving the specimen.

All relay contacts were analysed after one million of operations at the contact current of 0,1 mA D.C. and at the contact voltage of 6V D.C.. First the relay contact surface was analised. Then the upper layers were removed by bombardment with argon ions (sputter-etching) at the ionic current of 0,5 μA per 3,6 mm^2 area, and fresh surfaces were reanalysed. This procedure was repeated until almost all impurities disappeared from the surface.

III. RESULTS AND DISCUSSION

Figure 1 shows Auger electrons spectrum of the surface from a contact whose initial contact resistance was smaller than 100 mohms, but after one million of operations it was increased to more than 100 mohms. Such contacts are not usable and therefore declared as "bad".

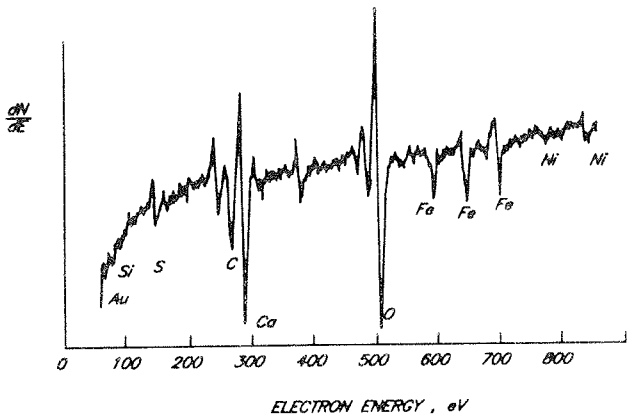

Fig. 1: *Auger electron spectrum of the contact surface having contact resistance of 100 mohm.*

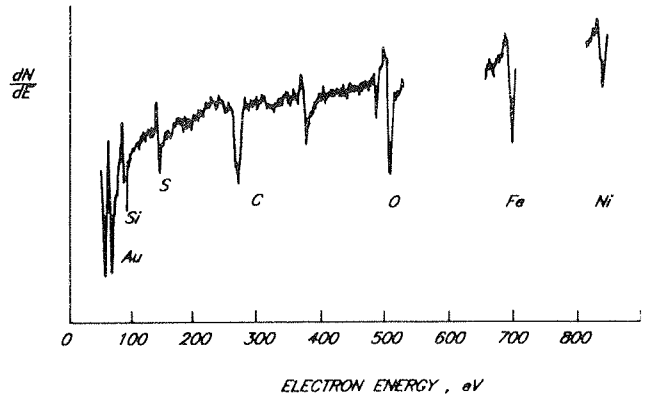

Fig. 2: *Auger electron spectrum of the contact surface having contact resistance of 90 mohms.*

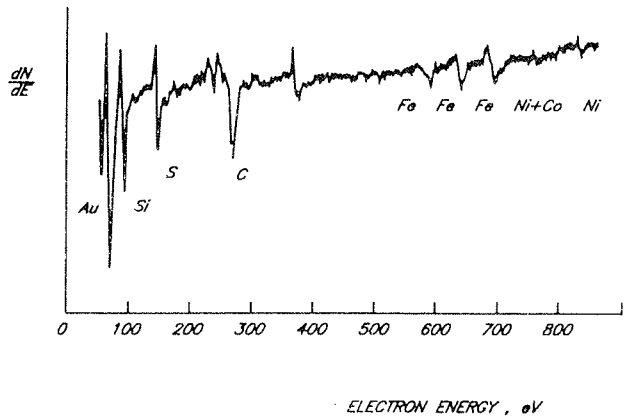

Fig. 3: *Auger electron spectrum of the contact surface having contact resistance of 90 mohms.*

Gold, the main element of the contact alloy with its characteristic peak at 69 eV is almost unnoticed. Iron at 703 eV and nickel at 848 eV are not observed well, either. However, large amounts of oxygen (at 510 eV), carbon (at 272 eV), sulphur (at 152 eV), and calcium (at

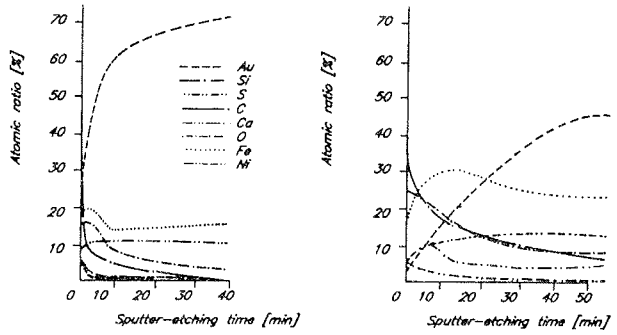

Fig. 4: *Composition profile of contact layers with the contact resistance of 90 mohms (1) and 100 mohms (2).*

290 eV) are observed, which certainly do not act favourably to the contact properties.

Figure 2 shows the spectrum of surface of a layer contact with the 90 mohm contact resistance after one million of operations, where carbon, sulphur and oxygen appear in relatively small quantities, while calcium does not appear at all. The same is valid also for Figure 3, which shows that there is practically no oxygen at all, while the gold peak is very strong.

The observed trends are even more pronounced when we compare the composition profile of contact layers of two relay contacts after one million operations (Fig.4).

The layer thickness is represented as sputter-etching time. The etching current was 0,5 μA per 3,6 mm^2. Concentration of elements was calculated according to:

$$C_x = \frac{I_x \cdot K_x}{I_x^{II}} \left(\sum_i \frac{I_i \cdot K_i}{I_i^{II}}\right)^{-1} \cdot 100 \quad (at\ \%)$$

where I_X is Auger peak to peak height of the measured element x.

I_X and K_X (scale factor) are obtained from the literature /5/.

Ii is the Apph. of the i-th element.

The formula was derived from the following two formulas:

$$C_x = \frac{I_x}{S_{x,Ag}} \left(\sum_i \frac{I_i}{S_{i,Ag}}\right)^{-1} \qquad S_{x,Ag} = \frac{I_x^H}{K_x \cdot I_{Ag}^H}$$

Calculating the concentration of sulphur it was taken into account that the gold peak at 150 eV was superimposed on sulphur peak at 152 eV. From the observed peak height the 1/34 of the 69 eV gold peak height was subtracted. We did this since in our experiment the ratio between the peak to peak height in the case of uncon-

taminated gold layers is 1:34 (at 150 eV and 69 eV). Comparing with the literature all the peak to peak heights of gold are approx in the same ratio to 69 eV peak height the one at 150 eV which is 1:17 /5/. We believe that the reason for this is that in the latter case there was some sulphur present as contaminant.

As it is evident from Fig.4, gold is more abundant both on the surface as well as in the internal atomic layers of a contact layer with "gold" contact properties. Carbon and oxygen are also found in smaller quantities. The amount of nickel is approximately equal in all studied samples,but the amount of iron varies to some extent. There is more iron on "bad" contacts. Calcium was found only on "bad" contacts. Small quantities of chlorine and silicon probably do not affect the contact quality.

Many factors which are out of our control influence the height of the signals of Auger electrons of individual elements. Therefore, it is possible that the absolute values of concentrations were somewhat faulty. The exact determination of concentration was not the aim of this work since we were mostly interested in the change of concentration of an element in question in different layers. About 50 contacts were analysed for the composition of contact layers. Even though the composition profiles were not always as pronounced as in the example just given, we found no "good" contact with greater amounts of oxygen, sulphur and calcium on its surface. It is similar for carbon, even it is permissible in greater concentrations. Furthermore it is not definitely established that the surface composition is the only parameter influencing the quality of contacts. Small dust particles and the geometry could also contribute to the enhancement of contact resistance even in the case of good contact composition (no impurities).

Thus, the alloyed golden layer is to some extent covered with impurities. This is unavoidable when working in the atmosphere. We were mainly interested in which technological phase greater amounts of impurities appear on the contact relays, so we might learn which of them must be changed or controlled with greater care.

The contact alloy was made by electroplating of gold on the iron, nickel, cobalt or iron and nickel base, followed by thermal treatment to achieve the diffusion process.

The possible source of calcium atoms is the running water which we use in the technological process.

Sulphur is, opposite to calcium, incorporated in the gold layers. Similar phenomenon was observed in the case when the carbon atoms were incorporated into gold layers /8/.

The composition profile of contact alloy according to Fig.4, shows the decrease of the sulphur concentration in the deeper layers. But after heating by electron bombardment (at T = 800°C, few seconds) the presence of sulphur at the surface increased drastically. This is in the agreement with the results presented by the other authors /9/. Regarding the changes noticed in the previous experiments, the amount of sulphur varied insignificantly by heating unplated contact relays.

The interpretation of this results is rather simple. At the beginning there was some concentration of sulphur present as contaminant bath, from the air pollution /10/ and from the gold plating bath. During the combined sputter-etching and AES analysis the present sulphur atoms were eliminated to the greater extent. After electron bombardment some sulphur atoms from the deeper layers migrated to the surface. As is mentioned above the presence of greater quantities of carbon atoms were also established. We believe that the main source of the carbon atoms is not the gold plating process as we use unbrightened acid cyanide bath. Carbon inclusions in similar electrolytes are known /8,11/, when iron, nickel, cobalt or indium are used as brighteners and are codeposited in the plated layers. In our case atmosphere is also source of carbon atoms /10/.

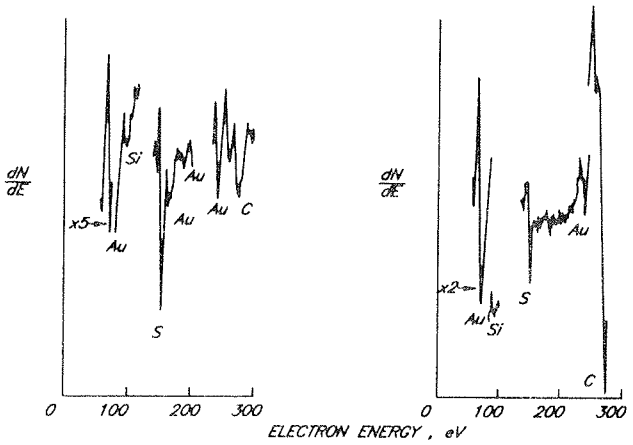

Fig. 5: Auger electron spectra of the surface of the contact relay before (1) and after (2) cleaning with Freon TF.

A noticeable increase of the concentration of carbon (Fig. 5) after cleaning the surface with Freon TF (CCl_2F-$CClF_2$) led us to concr similar method of cleaning with different organic solvents during the technological process is unsuitable. This is in accordance with the data referred in the earlier works /10

IV. CONCLUSION

- The analysis of contact surfaces of relay contacts indicated the appearance and the amount of unwanted elements.
- Comparing "bad" and "good" contacts the "good" ones showed greater concentration of gold on the surface as well as in deeper layers. The quality of the contacts depends on the concentration of contaminants such as carbon, sulphur, oxygen, and calcium. The higher the concentration the worse are the properties of the contacts.

- We were interested to find out the sources of the particular contaminants during the technological process. For sulphur it is the gold plating process. The sulphur atoms can not be removed from the surface since in our opinion they are incorporated in the contact alloy.
- Calcium atoms as contaminants originate from running water used in technological process for rinsing after electroplating.
- The sources for contamination of the surface with carbon atoms are the cleaning process with Freon TF, and probably also the relay capsule atmosphere. Unlike sulphur, carbon atoms are not incorporated in the contact layer and can be removed by heating to temperatures higher them 800° C.
- Cleaning with different organic solvents during the technological process is under question for same reason as mentioned above.
- The information like composition and concentration of particular elements at the surface and in the bulk of contacts are necessary for further development in the research and production of contacts. Auger electron spectroscopy is obviously an appropriate method for such investigations. Even more information about contacts could be obtained by using the Scanning Auger Microprobe, which makes possible the analysis of the contact spot with the diameter in the range 30-100 μm.

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Prispelo (Arrived): 30.01.95 ***Sprejeto (Accepted): 24.02.95***

INHOMOGENITY OF LASER-DRIVEN TECHNOLOGICAL PROCESSES
II. Material Related Inhomogenities

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Keywords: laser-driven technological processes, process inhomogenity, material surfaces, metal surfaces, laser beams, L-M-I, laser-material interactions, processing technology, inhomogeneous melting, dislocation disorder, premature melting, faceted melting, rotational cells

Abstract: Inhomogenity of laser-driven technological processes, caused by the surface inhomogenity is considered. Homogeneous laser beam interacting with the (metal) surface containing irregular grains, grain boundaries, dislocations, dislocation pile-ups, inclusions of the foreign atoms etc., causes the inhomogeneous melting. Of all the possible origins of inhomogeneous surface melting, only two were considered: dislocations and the premature melting associated with the stress-intensity contours (including the rotation cells on dislocation pile-ups), and the faceted melting of polycrystalline surfaces. The first origin of premature melting is associated with laser pulses on all time scales; the last one is associated with laser pulses shorter than 10 ns.

Inhomogenost laserski-iniciranih tehnoloških procesa
II. Inhomogenost vezana na materijal

Ključne besede: procesi tehnološki laserski, nehomogenost procesov, površine materialov, površine kovin, žarki laserski, L-M-I interakcije laser-material, tehnologija obdelave, topljenje nehomogeno, nered dislokacijski, topljenje prezgodnje, topljenje facetirano, celice rotacijske

Sažetak: Razmatra se nehomogenost laserski iniciranih tehnoloških procesa, izazvanom nehomogenošću površine materijala. Homogeni laserski snop u interakciji sa (metalnom) površinom koja sadrži nepravilna zona, granice zona, dislokacije i dislokacijske nakupine, inkluzije stranih atoma i sl., izaziva nehomogeno topljenje površine. Od svih mogućih uzroka nehomogenog površinskog topljenja razmatrana su samo dva: dislokacije i prerano topljenje povezano sa konfiguracijom linije stresa (uključujući i rotacijske ćelije formirane na dislokacijskim nakupinama), i facetirano topljenje, tj. selektivno topljenje samo nekih kristalnih ploha na polikristalnoj površini. Prvi uzrok preranog topljenja javlja se kod laserskih pulseva na svim vremenskim skalama, dok se drugi javlja samo kod laserskih pulseva kraćih od 10 ns.

INTRODUCTION

The inhomogenity is introduced into laser-material interaction (L-M) either by the inhomogeneous laser beam interacting with the homogeneous (ideal) surface (i), or by the homogeneous beam interacting with the inhomogeneous (real) surface (ii). The case (i) was studied in the ref. (1), while the case (ii) is the subject of this paper.

The greatest deal of inhomogeneous L-M interactions is caused by the "real systems" i.e. the surfaces with irregular grain microstructure, lattice deformations caused by the presence of defects like, impurities, dislocations of various kind, grain boundaries, continuous or discontinuous segregates in the composite surfaces etc., as schematically shown in Fig. 1.

Areal polycrystalline surface may be assumed a surface with inhomogeneous potential barrier distribution. Such a surface shows the inhomogeneous response on the homogeneous laser beam action. The most important consequence is that the surface exhibits a premature melting in a zones around defects, thus dividing the laser spot into separate basins of various dynamics. The contours of the molten basins are therefore, defined by the premature melting barrier T_{PM}, formed around every

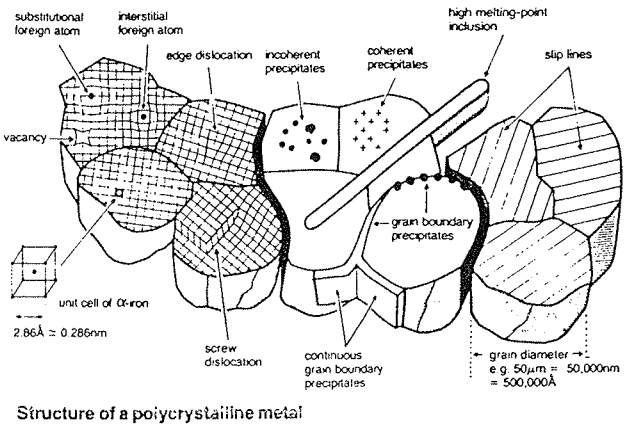

Fig. 1: Real surface of the polycrystalline metal sample. The surface is understood in a somewhat to has the thickness equal to the grain size.

particular defect. Thus, depending on the defect type and size a set of T_{PM} points will be established with characteristic that the largest defects cause the lowest T_{PM}. In other words, a homogeneous laser beam establishes the homogeneous temperature field T(x,y) on the

surface, while the surface defects establish distribution of the system transformation thresholds below T_M, which leads to local premature melting. In this way a similarity with the case (i) is established: namely, the surface shows a stochastic division into basins of solid (S) and the liquid (L) behaviour. Fig. 2. These basins are defined by the specific contours of premature melting, because the phase transition barrier is locally reduced.

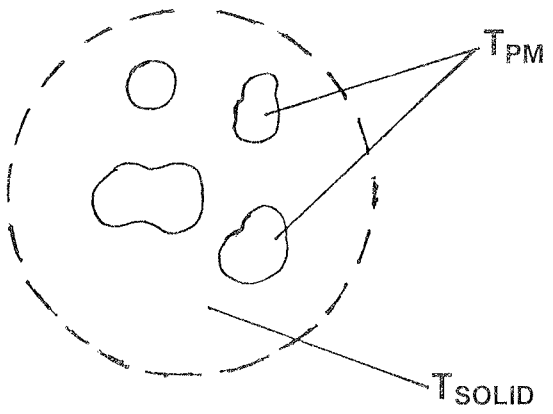

Fig. 2: Division of the laser spot into basins of the solid and the liquid response, by the contours of premature melting formed around defect places on the surface.

Since the surface defects define the point of premature melting, the surface consists of only two type of basins. The solid and the liquid one. (The basin showing vaporization has no connection to the surface defects).

Once, the basins of premature melting are established, one can introduce the pressure and temperature gradients ΔP and ΔT inside them. Introducing further their vertical and parallel components with prospect to the surface i.e. $\Delta T_{\parallel}$, $\Delta T_{\perp}$ and $\Delta T_{\perp}$, $\Delta P_{\parallel}$ and following ref. /1/, one can introduce representation of possible cases by the combination of $\Delta T_{\parallel,\perp}$ $\Delta P_{\parallel,\perp}$ gradient pairs meaning that all the physical effects discussed in ref. /1/ (for the S and L phases) are possible, in this case too.

A. GENERATION OF BASINS OF LOCAL SURFACE DYNAMICS BY SURFACE DISORDER

Dislocation Disorder:

Among all surface defects important for the inhomogeneous L-M interaction, dislocation have the most intriguing role.

Assuming a regular topological network on the ideal crystal surface, the introduction of any dislocation reflects as a local deformation of the network, i.e., as a topological disorder. An illustration of dislocation disorder is shown in Fig. 3.a,b. Fig. 3.a. represents the crystal surface with high (local) density of strongly interacting dislocations, while Fig. 3.b. shows the other kind of disorder for the similar case. Such a locally disordered surface may be corresponded with the surface of liquid, shown in Fig. 3.c. Ziman has mentioned that (in the topological sense) the liquid state can be assumed a crystal with very high number of dislocations, while the melting can be understood as a spontaneous formation of dislocations /2/.

It is well known that the elastic energy of the system connected with dislocation is proportional to the loga-

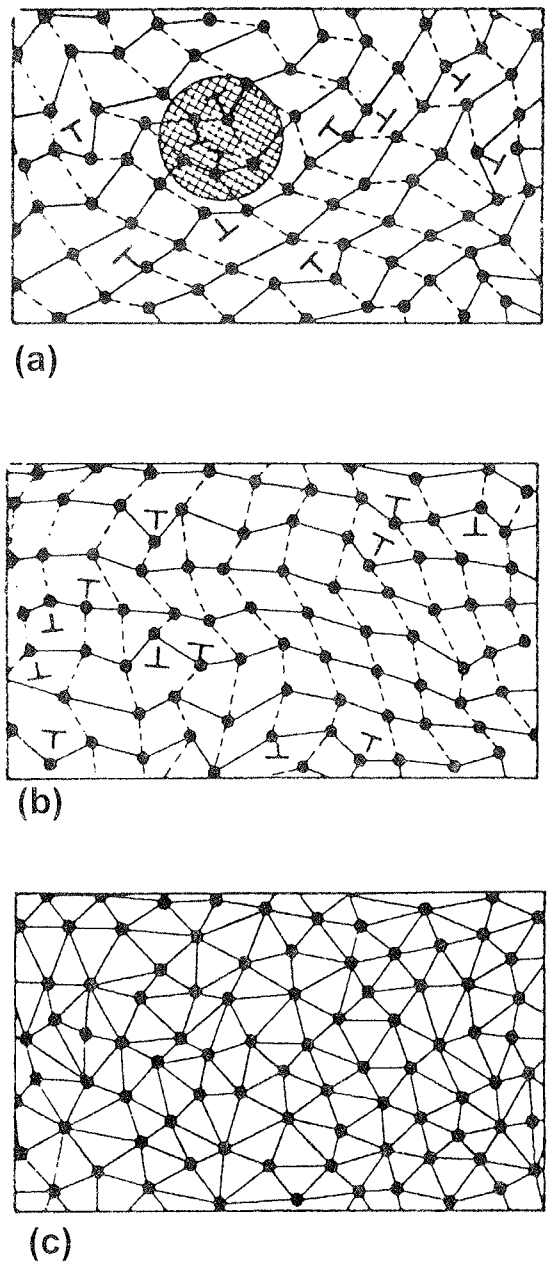

Fig. 3: Topological disorder of the crystal surface.
a) Corresponding to high density of strongly interacting dislocations.
b) Corresponding to another case of dislocation density.
c) Topological disorder of liquid.
From ref. 2.

rithm of the area taken by one dislocation. Consequently, this energy decreases as the dislocation density increases. However, this topological description has a sense only if dislocations are located at relatively large distances, so as to be easily identified /2/.

Local Density of Electronic States at the Core of Screw Dislocation

Corresponding picture to the topological one of dislocating disordered (defect) surface is the picture of local density of electronic states. Obviously, the topological lattice defect result in modified (defect) electron density of states with respect to the regular lattice, and therefore in the local forces, and in final result in different (lower) phase transition points. The best illustration is the level density of el. states calculated by Paidar for the screw dislocation in the BCC lattice. /3/

Local density of electronic states was studied taking into account a dislocation topology namely the screw dislocation with the Bargers vector (1/2) [111] in a b.c.c. lattice and using (only the s-orbits at each atomic site). For s-orbital the matrix elements of the Hamiltonian are completely determined by distances to the neighbouring atoms, and not depend on directions between them /3/. The effects of atomic disorder near a dislocation core were calculated on the hoping integrals, taking into account 30000 atoms in the topology of the screw dislocation.

The results of calculation showing local density of electronic states n(E) are given in Fig. 4. and clearly indicate

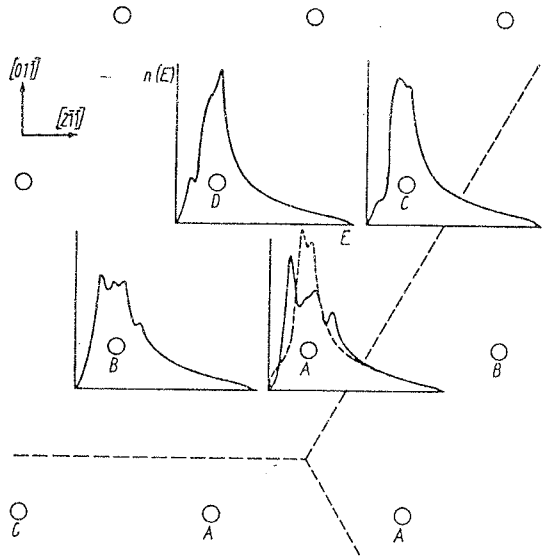

Fig. 4: Local density of electronic states for atoms in the screw dislocation core. For comparison, the local density of states for the perfect b.c.c. crystal is plotted by dashed line. The positions of atomic rows in the projection onto the (111) plane are marked by small circles. Three dashed lines radiating from dislocation centre (the projection of dislocation line), correspond to the half-planes [011] onto which the dislocation splits. From ref. 3.

the shift and the broadening of the bond as well as covering of its symmetry at the atoms close to the dislocation center. The difference in the total energy between an atom in the dislocation core and one in the perfect lattice due to shape variations of n(E) is negative /3/. Consequently, the zone around a screw dislocation is topologically defect, bounded less toughly and therefore the zone of premature melting.

Identification of the stress-intensity contours around 1,2 or more screw dislocations.

Different view of this problem is based on the stress-intensity lines associated with dislocations in the lattice. Various kinds of stress-intensity contours were found around 1,2 or more screw dislocations (in metals), which are in a strong interaction.

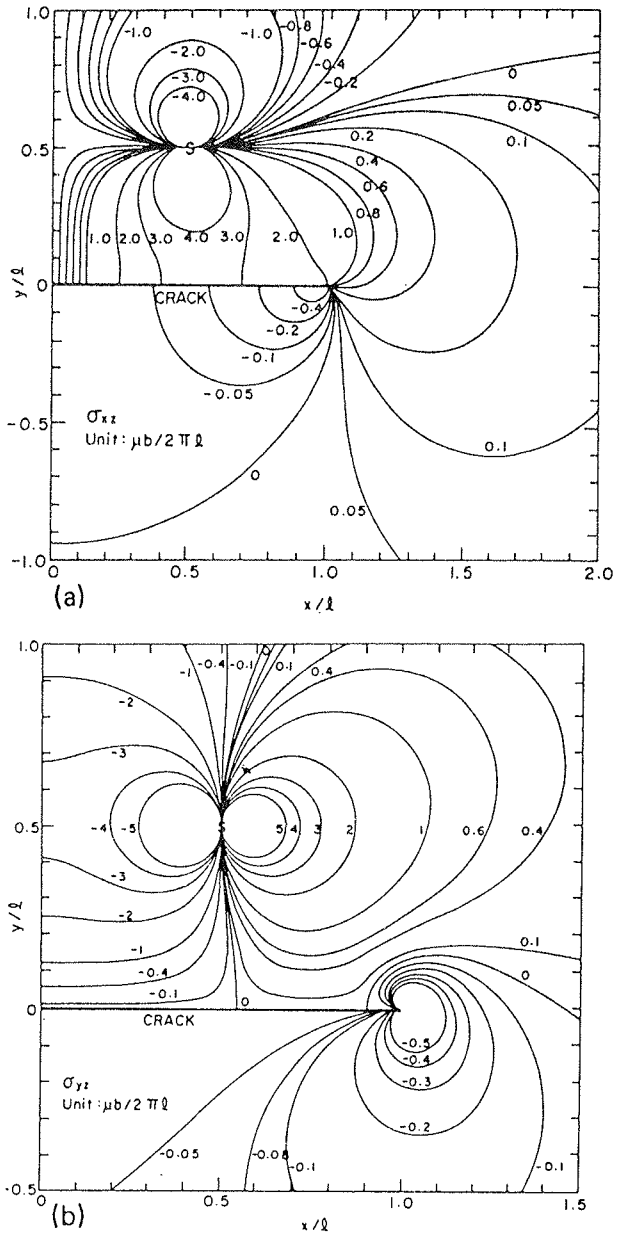

Fig. 5: Contours of stress components are induced by a **dislocation situated at (0.5l, 0.5l)**. *(a)* σ_{xz}, *(b)* σ_{yz}. *From ref. 4.*

The stress-intensity configuration modifies (decreases) a local surface forces and therefore reduces the melting point. This configuration plays a crucial role in the surface L-M interaction causing local melting and amorphization.

Very complex case of elastic interaction between general parallel screw dislocations and a surface crack was studied by Yung and Lee /4/. Assuming a complex situation of a defect surface i.e. such which contains crack(s) and the screw dislocations in the crack tip vicinity, they calculated the stress-intensity configuration in a few different topological situations calculating the stress field:

(i) induced by dislocations inside the crack

(ii) induced by lattice dislocations.

The contours of the stress components σ_{xz} and σ_{yz} (without the applied stress), for different crack size, ℓ, are given in Figs. 5.a,b. The stress-intensity contours at the crack tip are given in Fig. 6.

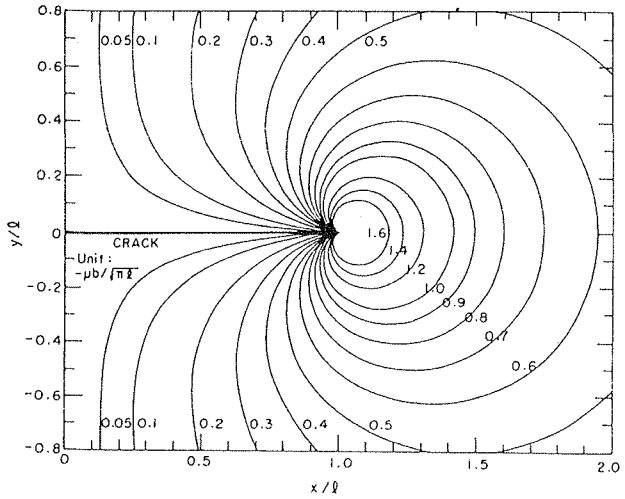

Fig. 6: Contour of the position of the dislocation to generate the same stress intensity factor (unit = $\mu b/\sqrt{\pi l}$) at the crack tip (μ = shear module, b = Burgers vector of screw dislocation). From ref. 4.

The contours of the stress-intensity factor (in the absence of applied stress), for different angles α and ϕ_0 are given in Fig. 7.a,b,c. [The angle α is the angle between the line connecting two antiparallel screw dislocations, and the base plate, while ϕ_0 is the angle between dislocations and the crack-line]. (See ref. 4.)

The contours of the stress-intensity factor determine the local surface topology which is a candidate for a premature melting in laser treatment.

Obviously, the envelope of the (premature) melting zone follows the stress-intensity lines. Since, their shape is strongly dependent on the number of interacting dislocations and their spatial location, one expects a number of shapes, usually appearing as isolated cells, some of which are rotational.

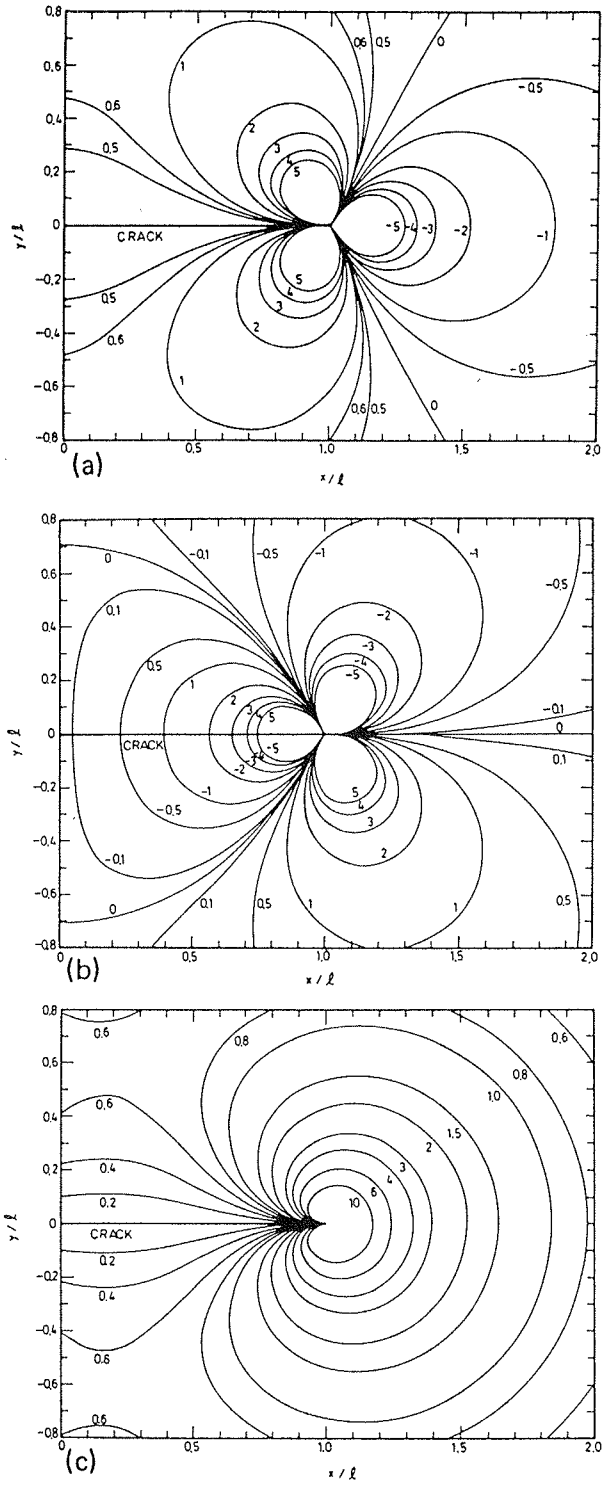

Fig. 7: Contour of the position of the dislocation dipole **to generate the same stress intensity factor** *(unit = $\mu ab/\sqrt{\pi l}$) at the crack tip. (a) α = 0. (b) $\alpha = \pi/2$. (c) $\alpha = \phi_0$. From ref. 4.*

Formation of rotational cells on dislocation pile-ups

It was recently shown that local premature melting is associated with the appearance of the surface rotational cells in shock-located crystalline metallic materials. The effect is of a general nature appearing in different kinds of shocks, and in this respect covers the specific field of laser-induced shocks.

The rotational cells are generated in crystalline metallic material (steel, Cu, A, and Ti based alloys). In shock-loaded metallic crystals the small regions are rotated relative to the neighbouring material. The disorientation of such rotated regions (rotation cells) ranges from units to dozen degrees. There are two types of RC-s: a) Crystallographic RC-s are spherical, b) At given boundaries the RC-s are imperfect, but close to spherical usually associated with crack (see the previous work of Yung and Lee).

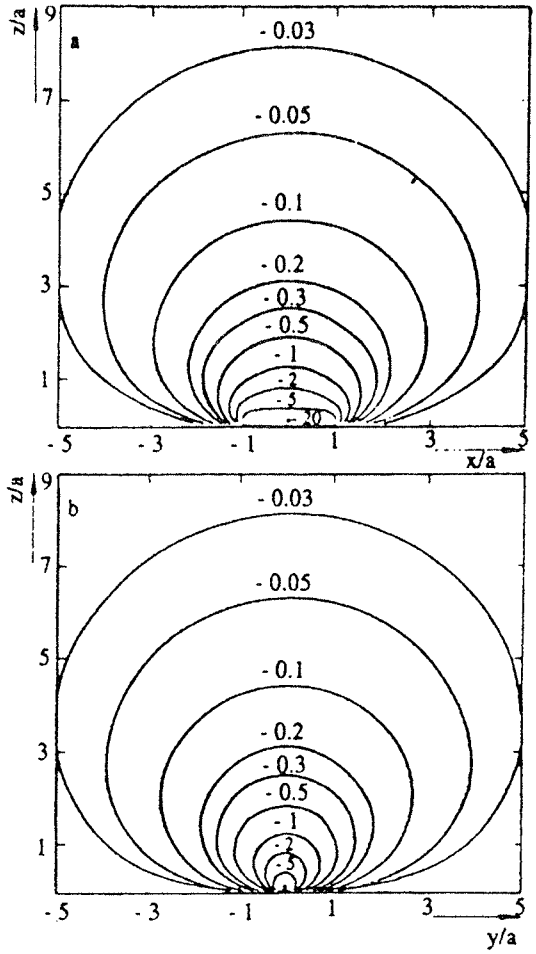

Fig. 8: *Maps of* **spatial distribution of the hydrostatic stress field** *induced by the* **π-shaped superdislocation loop** *with the edge* **segment length being** *2 a. Here we use value of G/6π (1+νB)/(1-νa) as unit for the hydrostatic stress field. (a)* **The section y=0. (b) The section x=0.** *From ref. 5. (G = shear module, ν = Poisson ratio, B = Bergers vector of large dislocation loop: B = Nb; a = dimension of a large dislocation loop.).*

The rotational cells range from one to many of them being quite disordered or ordered (organized) into chains, or some irregular formations (as we observed in laser generated shocks). An important feature of the RC-s is that they have a **resonant character** relative to the shock-load rate /5/. This effect assures within a certain (narrow) interval of shock-load-rate for each material. The physical model of the RC-s generation of Gutkin et al./5/ is based on dislocation loop pile-ups in shock loaded metallic crystals. For example, in iron and steel materials the shock wave of amplitude of ~13 GPa, a straight line of parallel rows of screw dislocations oriented along <111> directions inside grains is generated. Therefore, the ensemble of dislocation loops is introduced, and each edge screw of the dislocation loop move in the shock-wave front, while the screw-segments are immovable. The length of the screw segment increases parallel with the motion of the edge segments. This process leads to the formation of pile-ups consisting of the edge segments of the dislocation loop, when such segments are stopped by orbital (grain boundaries, particles, etc.) /5/. This process is the bases for the local appearance of the new properties, for example the local melting, which occurs near the head of a dislocation pile-up. Thus, the local amorphous phase is formed in the region near the dislocation pile-up head characterized by both high stress concentration and high latent energy density /5/.

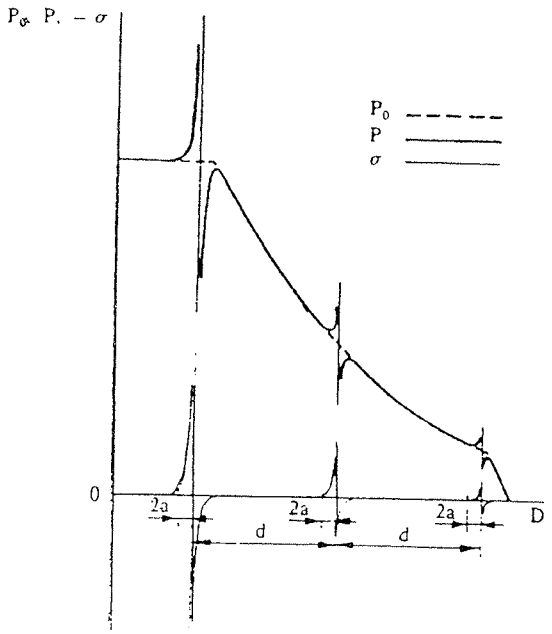

Fig. 9: **Local excitations of the shock-wave** *front* **near dislocation pile-up (schematically).** *Here the axis D intersects the head of the dislocation pile-ups and is oriented along the wave propagation direction. P denotes the mean pressure at the shock-wave front. P the effective local pressure. - σ the local pressure field induced by the dislocation loop pile-ups.* **2a the length of edge segments** *(which are perpendicular to axis D) of the dislocation loops being elements of the dislocation pile-ups.* **d the mean distance between the dislocation pile-ups.** *From ref. 5.*

The stress-field characteristics acting on the dislocation pile-up were determined for superdislocation lags consisting of N dislocations in the dislocation pipe-up. /5/

The components of the hydrostatic stress (compression) were calculated, and the result is graphically shown in Fig. 9. The effective dislocation of the elastic precursor (elastic component of the shock wave) E~10-100 ns while the time needed for the generation and 1 dislocation loop on the basis of Frank-Read mechanism is 0.5 ns, with shear stress to ~10^{-4} G (G = shear module). Thus, for the time $\tilde{t}$ (duration of elastic precursor), the pile-up consisting of 10-100 dislocation loops can be formed near the same origin The length of the pile-up is $\tilde{\ell}$ ~0.1-1 μm /5/.

Besides the compressive stress, the rotational momenta in local regions, are generated. There consequences are:

(i) a high concentration of interstational atoms within the shock-wave front, generated through anomalously high diffusion
(ii) capability of crystal-to-glass-to-crystal transformation induced by the shock
(iii) local rotations.

The resonance character of the process manifests by dependence of the process on the shock loading rate.

If the shock loading rate is small, $V<<V_{resonance}$ the intensity of the intensity of the shock more is sufficient for dislocation pile-up formation. If $V>>V_{res.}$, the shock

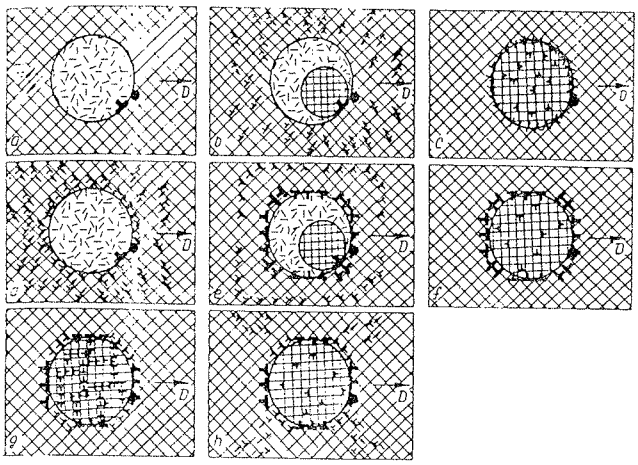

Fig. 10: Models of the formation of **crystallographic rotation cells(RCs) near dislocation pile-ups**. *(a) The* **formation of the crystallographic RC whose boundary contains the low-density ensemble of dislocations (case $V \geq V_{res.}$ abrupt front)**. *(d-g) Crystallization of the amorphous nucleus is followed by the formation of the crystallographic RC which contains the high-density dislocation ensemble (case $V \geq V_{res.}$ sloping front). (h) The same as (d-g), but dislocations "scatter" t the surrounding material (case $V \leq V_{res.}$ sloping front, short impulse). From ref. 5.*

more with a very abrupt front moves causing inhomogeneous amorphization (local, spherical amorphous zones). /5/

For $V<V_{res.}$ formation of chains was observed oriented along the shock more propagation direction. Formation of the individual rotation cells is show in Fig. 10. and formation of chains-of-rotational cells is shown in Fig. 11.

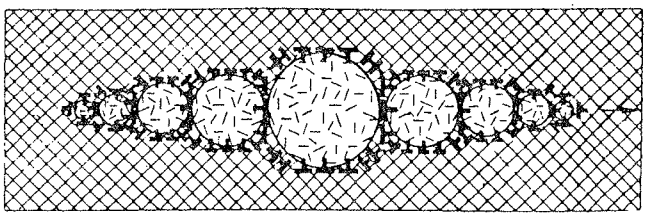

Fig. 11: Model for the formation of the chain of the **crystallographic rotation cells** *(case $V \leq V_{res.}$ sloping front,* **long impulse**). *From ref. 5.*

Dimensions of the RC-s in the chain decrease from center to the edges of the chain. Decrease of dimensions of RC-s to the left of the center occurs since interstational atom concentration decreases as the shock wave propagates through the region in which the formation of the RC-s occurs. Decrease of dimensions of RC-s to the right of the chain center occurs since only a small-density ensembles of dislocations have time to be formed at boundaries of amorphous nuclei /5/.

B. FACETED MELTING

The inhomogenity of L-M interaction a local premature melting may also appear though other reasons different from the (surface) dislocations. The polycrystalline surfaces, like those schematically shown in Fig. 1., [because of different potential on different crystallographic surfaces] may exhibit a premature melting at some surface facets and not on the others.

This effect is expected to occur in L-M interactions on the time scale below 10 ns; very fast cooling after pulse termination causes immediate freezing of the surface in which local melting stay frozen permanently. In all the other cases [i.e. for τ>10 ns time scale] a fast thermal diffusion and the heat conduction causes the melting also of the neighbour metal facets, with different crystallographic orientation, so that premature melting of only one specific facet is lost /6,7,8/.

Surface effects which are the consequence of crystal anisotropy i.e. crystal facet dependent, like for example surface faceting and melting. Surface faceting is a spontaneous decay of a crystal face into partions (facets) of other faces, (under laser pulse treatment).

The stability of surfaces is connected with the anisotropy of the surface free energy of crystals. The microscopic

mechanisms leading to surface faceting may be diverse, so long as they produce a dip in the specific surface free energy of a crystal, which generates the unstable region. Unstable vicinal surfaces facet and involve into hill-and-walley structures. Sharp edges are than present on the equilibrium crystal shape /6/. A phenomenon which is instead typical of high temperature is surface melting. It consists of preferential **thermal breakdown** of crystalline rigidity with onset of liquid-like mobility and diffusion near the surface. When present, this phenomenon leads to the formation of a stable "quasi-liquid-layer" which coats the crystal surface, and where thickness may diverge when the melting point T_m is approached from below. Surface melting has been shown to take place on a large variety of mell characterized surface faces. Generally speaking surface melting is common for weekly bounded crystals (Van der Vaals crystals), and for the poorly packed faces of any given crystal. On the contrary, the well packed surfaces of strongly bonded metals are more stable and less pure to surface melting which has been shown not to occur for Al(111), Au (111), Cu (111) etc. /6,7/

The high temperature faceting was studied by computer simulation for the vicinal surface close to Au(111). The results are shown in Fig. 12. Fig. 12.a. shows particle trajectories at low temperature for the surface configuration chosen, in this particular case a (423) vicinal with $\beta \cong 15.2°$; and reconstructed terraces. Bringing the surface in thermal equilibrium close to the bulk melting temperature, gives the result in Fig. 12.b. The steps have merged or collapsed together to form a liquid "drop" whose surface is slotted at an angle $\beta_C \sim 30°$ with respect to the (111) direction. /6,7/

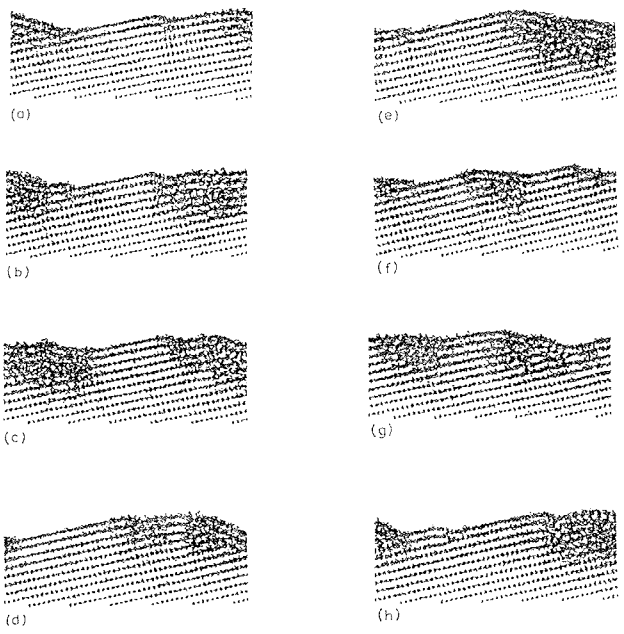

Fig. 12: Examples of fluctuations for the high-temperature faceting. The Au(534) surface is shown at T=0.99 T_m after: (a) 1.8, (b) 2.9, (c) 3.6, (d) 4.6, (e) 5.4, (f) 6.1, (g) 6.4, and (h) 7.1 ns. From ref. 6.

Among additional kinds of welting phenomena, there are prewetting (involving a jump in the thickness of the wetting layer) and incomplete wetting, where the thickness of the wetting layer saturates at some finite value. Thus, for example, the Pb(100), Ni(100) and Au(100) show only disorder at T_m, i.e. only the incomplete wetting. /6,7/

Molecular dynamics calculations for A(100) have shown a very interesting effect. While at 0,3 T_m and 0.74 T_m there is a little diffusion and the surface is in a solid phase, at 0.8 T_m and 0.99 T_m, a considerable amount of liquid diffusion exists but solid-like-islands are also present. Disorder is essentially restricted to the two topmost layers. /6,7/

CONCLUSION

Of all the possible material-related origins of inhomogenity in L-M-I, we addressed only two in this paper: dislocation disorder and the faceted melting. The first origin is associated with the laser pulses on all time scales, while the second one is associated with pulses shorter than 10 ns. Both of them couse premature melting as a local phenomena limited either to the largest stress-interesty contour (i) or to the size of the particular facet. They are the most interesting subject of intensive studies today. All the others, like local lattice distorsion because of Jan-Teller effect, chemical composition, etc. were not considered in this paper. Also, the effects caused by different light absorption in composite materials, or those containing inclusions of the foreign particles, were not the subject of this paper.

It was shown that the stress interesty contours around dislocations in the L-M interaction are the premature melting contours. Dislocation disorder of high degree usually leads to formation of dislocation pill-ups on the stress-intensity contour and to the rotational cells. Different kind of rotational cell organization on the surface (linear, irregular, etc.) was shown to appear depending on the surface stress field configuration.

In addition, the faceted crystal surface melting was discussed also. It was mentioned that (110) surfaces of fcc metals exhibit surface melting, i.e. complete wetting of the solid gas interface by the liquid at the ns and ps time scale. On the contrary, close-packed (111) surfaces of many fcc metals do not melt below T_m. The surface melting properties of (100) fcc surfaces, with on intermediate packing density between (110) and (111), are less known today.

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Prispelo (Arrived): 20.12.94 ***Sprejeto (Accepted): 31.01.95***

SNOVANJE DIGITALNIH VEZIJ Z OPISNIM JEZIKOM VHDL

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Ključne besede: jeziki računalniški, vezja digitalna, VHDL jezik, opis jezika, razvoj jezikov, omejitve pri snovanju, jeziki opisni, snovanje vezij digitalnih, strukture vezij, arhitektura vezij, obnašanje vezij, načrtovanje vezij

Povzetek: Članek predstavi standardizirani jezik VHDL za opis digitalnih vezij. V VHDL-u lahko opišemo obnašanje in/ali strukturo vezja. Tako obnašanje kot strukturo lahko predstavimo na različnih abstraktnih nivojih, od arhitekturnega nivoja do nivoja logike. Prvi koraki razvoja VHDL-a so bili narejeni v zgodnjih osemdesetih letih. Končna verzija predlaganega jezika, poznana kot VHDL Verzija 7.2, je bila pripravljena leta 1985 in leta 1987 sprejeta kot standard IEEE-1076. Glavne prednosti VHDL-a so: javna dostopnost, podpora različnih metodologij načrtovanja in načinov implementacije vezja, neodvisnost od tehnološkega procesa, možnost opisa na različnih abstraktnih nivojih, prenosljivost opisov, modularnost, ponovna uporabljivost in podpora vlade ZDA. Ker je VHDL standardiziran, je na voljo vedno več načrtovalskih orodij, ki uporabljajo za vhod opise vezij v VHDL-u. Zadnja standardizirana verzija jezika je IEEE-1076-1993. Trenutno se razvija razširitev VHDL-a za opis analognih vezij.

Digital Circuit Design with VHDL Description Language

Keywords: computer languages, digital circuits, VHDL language, language description, language development, design limitations, digital circuit design, circuit structure, circuit architecture, circuit behaviour, circuit planning

Abstract: This paper presents the standardised VHDL digital hardware description language. VHDL is a language for describing digital electronic systems. It arose out of the United States Government's Very High Speed Integrated Circuits (VHSIC) program, initiated in 1990. There was a need for standard language for describing the structure and function of integrated circuits (ICs). Hence the VHSIC Hardware Description Language (VHDL) was developed, and subsequently adopted as a standard by the Institute of Electrical and Electronic Engineers (IEEE).

VHDL is designed to fill a number of needs in the design process. Firstly, it allows description of the structure of a design, that is how it is decomposed into sub-design, and how those sub-designs are interconnected. Secondly, it allows the specification of the function of designs using familiar programming language constructs. Thirdly, as a result, it allows a design to be simulated before being manufactured, so that designers can quickly compare alternatives and test for correctness without the delay and expense of hardware prototyping.

A history of VHDL can be separated into three phases: the definition phase, the development phase and the deployment phase. In the definition phase the basic concepts and elements that form the character of the hardware description language were defined. At the same time the academic and industrial environments necessary for the eventual acceptance of VHDL as an industry standard were cultivated. The principal activity of the development phase has been the development of software to support the use of VHDL for electronic product design and documentation. After successful development the deployment phase began. In this phase VHDL can be widely used in industry, university education and research. The final version of the language, known as VHDL Version 7.2, was made available and standardised by IEEE as IEEE Standard 1076 in 1985 and 1987, respectively. In 1992 IEEE revised the standard. Some new features in signal assignment, new predefined operators, functions and attributes, and detailed specified timing model needed for the simulation cycle were added. These revisions were accepted as IEEE-1076-1993 standard.

Circuit description in VHDL can be behavioural and/or structural. Each kind of description covers different abstraction levels, from the architecture level down to the logic level. The full set of design representations that a VHDL can specify is described in the followig matrix.

Level	Behavioural domain	Structural domain
Architectural	Perforn1ance specifications	Logical connections of processors, memories, controllers, buses
Algorithmic	Procedural behaviour, manipulation of data structures	Data structures, procedural partitions
Functional	Concurrent operations, register transfer, state sequencing	Physical connections of functions, including arithmetic and logic units, multiplexers, and registers
Logic	Boolean equations	Physical connection of gates,latches

VHDL represents the full behavioural and structural domains. The behavioural domain describes what a circuit or device must do. The structural domain describes a component's logical layout: partitioning, decomposition (hierarchy), and interconectivity.

The main advantages of VHDL are: public availability, different design methodology and technology support, technology and process independence, wide range of descriptive capability, design exchange, modularity, design reuse and USA government support. A few years ago VHDL was used only in academic societies, but now powerful tools for making integrated circuits that use VHDL entry description are available. The advantage of VHDL in comparison to other hardware description languages is that VHDL is standardised by IEEE and it is in public availability.
Currently, VHDL analog extensions are under development.

1. Uvod

VHDL (VHSIC Hardware Description Language) je standardizirani jezik za opis digitalnih vezij /1,9/. Je rezultat programa VHSIC (Very High Speed Integrated Circuits), začetega leta 1980, katerega cilj je bil razvoj zelo hitrih integriranih vezij. V okviru tega programa se je pojavila potreba po standardnem jeziku za opis tako strukture kot tudi obnašanja integriranih vezij.

VHDL zapolnjuje številne potrebe v procesu načrtovanja vezij. Omogoča opis strukture vezja, v katerem se poda, iz katerih modulov je vezje zgrajeno in kako so ti moduli med seboj povezani. Omogoča tudi specifikacijo funkcije vezja na način, ki je podoben standardnim programskim jezikom. Opis vezja lahko simuliramo ter tako hitro primerjamo alternativne rešitve in testiramo pravilnost zasnove še pred izdelavo prototipa. Tako obnašanje kot strukturo lahko predstavimo na različnih abstraktnih nivojih, od arhitekturnega nivoja do nivoja logike.

Postavlja se vprašanje, ali je za predstavitev vezja primerneje uporabiti opisni jezik ali shematski opis. Nekateri načrtovalci menijo, da je shematski opis najprimernejši, vendar postanejo sheme nepregledne, ko vezje preseže nekaj 10000 logičnih vrat. Zato se vedno več načrtovalcev odloča za uporabo jezikov za opis vezij.

Članek najprej predstavi nastanek in razvoj jezika VHDL, njegove značilnosti in prednosti. V nadaljevanju so opisani glavni konstrukti jezika VHDL in primeri opisov obnašanja in strukture vezja. Sledi razprava o primernosti izbire jezika VHDL za načrtovanje digitalnih vezij. Na koncu so opisane še omejitve pri načrtovanju z jezikom VHDL ter njegov nadaljnji razvoj.

2. Razvoj jezika VHDL

Razvoj jezikov za opis vezij se je pričel v šestdesetih letih, ko so nastali prvi višji programski jeziki. Prvi jezik za opis vezij je bil CDL (Computer Design Language) /5/. CDL ima nekatere konstrukte programskih jezikov in objekte, ki so gradniki digitalnih vezij (registri, dekodirniki, stikala, urni signali, ...). Nekoliko kasneje je nastal jezik DDL (Digital System Design Language), ki že ima možnost opisa vezja na arhitekturnem nivoju in na nivoju Boolovih funkcij /5/. V sedemdesetih in osemdesetih letih je prišlo do poplave najrazličnejših jezikov za opis vezij. S tem je nastajala zmeda, saj jeziki med seboj niso bili združljivi.

Zgodovino jezika VHDL lahko razdelimo na tri faze: fazo definicije jezika, fazo razvoja in fazo uporabe /6/. Faza definicije jezika je potekala približno od leta 1980 do 1986. V njej so bili definirani osnovni koncepti in značilnosti jezika. Za začetke definiranja VHDL-a označujemo znanstveno delavnico *The Hardware Description Language Summer Study*, ki je bila junija 1981 v mestu Woods Hole v Massachusettsu /10/. Tam so izoblikovali priporočila za jezik, ki bi bil primeren za opis digitalnih sistemov. Na osnovi teh priporočil je prevzelo iniciativo obrambno ministrstvo ZDA in določilo program razvoja VHDL-a. Formalno se je delo na definiciji jezika pričelo poleti 1983, ko je obrambno ministrstvo ZDA vzpostavilo stik s podjetji Intermetrics, Texas Instruments in IBM. Ta podjetja so definirala osnovne konstrukte jezika. Njihovo delo je kulminiralo poleti leta 1985, ko je bila predstavljena definicija jezika VHDL Verzija 7.2.

Druga faza, faza razvoja jezika, sega približno od leta 1986 do 1993. Glavni dejavnosti v tej fazi sta standardizacija jezika in razvoj programskih orodij, ki uporabljajo za načrtovanje in dokumentiranje digitalnih vezij opis v VHDL-u. Po definiciji VHDL-a je njegovo standardizacijo pričel IEEE. V letu 1986 je IEEE sponzoriral več srečanj, kjer bi se definiral jezik za opis vezij. Osnova je bila definicija VHDL Verzija 7.2. Decembra 1987 je bil sprejet standard IEEE-1076, ki opisuje definicijo jezika VHDL.

Po definiciji in razvoju VHDL-a se prične faza njegove uporabe. Za pričetek uspešne uporabe morajo obstajati ustrezna programska orodja in interes načrtovalcev za uporabo. Javna last VHDL-a in standardiziranost so prispevali k temu, da se VHDL pričenja množično uporabljati.

3. Hierarhični opis vezja

Z VHDL-om lahko opisujemo vezje na različnih abstraktnih nivojih. Pri opisu zasnove digitalnega vezja imamo dve domeni: domeno obnašanja in domeno strukture. Z opisom obnašanja vezja definiramo, *kaj* vezje dela. Obnašanje opišemo s podatkovnimi strukturami in funkcijskimi preslikavami med vhodnimi in izhodnimi vrednostmi na priključkih vezja. Z opisom strukture vezja definiramo komponente vezja in njihove medsebojne povezave, torej kako vezje opravlja zahtevano funkcijo. Domeni opisa vezja in nivoji abstrakcije v VHDL-u so prikazani na sliki 1.

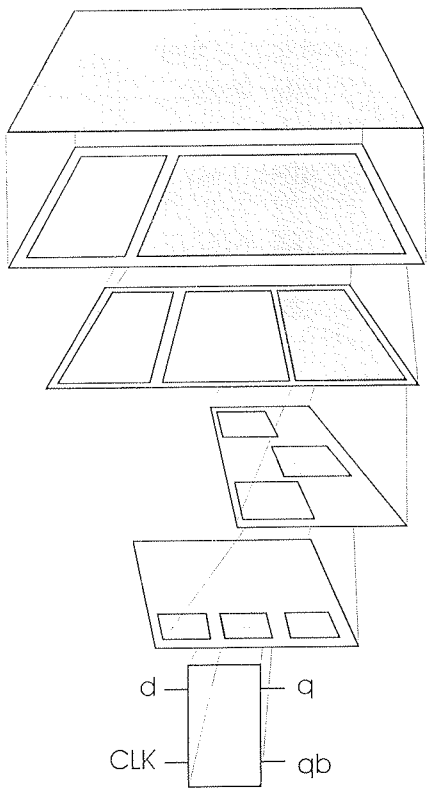
nivo	domena obnašanja	domena strukture
arhitektura	specifikacija zmogljivosti	logične povezave med procesorji, pomnilniki, krmilniki, vodili
algoritem	proceduralno obnašanje, manipulacije s podatkovnimi strukturami	podatkovne strukture, dekompozicija procedur
funkcije	sočasne operacije, prenosi med registri, prehajanje med stanji	fizične povezave med funkcionalnimi enotami (aritmetične in logične enote, multipleksorji in registri)
logika	Boolove enačbe	fizične povezave med logičnimi vrati in zadrževalniki

Slika 1: Domeni opisa vezja in nivoji abstrakcije v VHDL-u

Z opisom obnašanja na nivoju arhitekture specificiramo zmogljivosti celotnega digitalnega sistema, na nivoju algoritma opišemo proceduralno obnašanje in manipulacije nad podatkovnimi strukturami, na funkcionalnem nivoju sočasne operacije, prenose med registri in preha-

janje med stanji. Obnašanje na najnižjem nivoju, nivoju logike, opišemo z Boolovimi enačbami. Tudi strukturo vezja lahko opišemo na istih abstraktnih nivojih. Na nivoju arhitekture opišemo logične povezave med procesorji, pomnilniki, krmilniki, vodili in drugimi večjimi logičnimi enotami, ki predstavljajo neko zaključeno celoto. Na nivoju algoritma opišemo podatkovne strukture in dekomponiramo opise procedur. Na funkcionalnem nivoju opišemo fizične povezave med funkcijskimi enotami, kot so npr. aritmetične in logične enote, multipleksorji in registri. Strukturo na nivoju logike opišemo s fizičnimi povezavami med logičnimi vrati in zadrževalniki.

Možnost opisovanja vezja na različnih abstraktnih nivojih omogoča, da opis vezja hierarhično dekomponiramo. Vezje najprej opišemo na nivoju arhitekture. Takšen opis lahko hitro simuliramo in ugotovimo morebitne napake pri zasnovi vezja. Če vezje deluje po zahtevani specifikaciji, lahko posamezne enote vezja dekomponiramo in jih opišemo na nižjih nivojih. Dekompozicija pa ni nujno potrebna za vse enote vezja. Na nižjih nivojih lahko opišemo samo posamezne enote vezja, druge pa pustimo na višjem nivoju. Tako lahko imamo v opisu vezja različne nivoje abstrakcije.




```
signal CLK, q, qb, d : bit;
D_FF : block (CLK = '1')
    signal s : bit;
begin
    s <= guarded d;
    q <= s;
    qb <= not s;
end block D_FF;
```

Slika 2: Hierarhični pristop k načrtovanju vezja

Hierarhični pristop k načrtovanju vezja je ilustriran s primerom na sliki 2 /13/. S takšnim pristopom dobimo hierarhičen opis vezja, v katerem je na nivoju i opisana specifikacija komponente, na sosednjem nižjem nivoju i-1 pa implementacija komponente.

4. Glavni konstrukti jezika VHDL

Opis celotnega vezja ali njegovega dela je sestavljen iz:

- *osebka* in
- ene ali več *arhitektur.*

V osebku opišemo zunanji vmesnik vezja in deklaracije, ki se nanašajo na vse arhitekture, ki pripadajo temu osebku. Z arhitekturami opisujemo obnašanje ali strukturo vezja.

Splošni zapis osebka ima naslednjo obliko:

entity *identifikator* is
    deklaracije
begin
    stavki
end *identifikator*

V deklaracijah navedemo ime, način in podatkovni tip posameznega priključka vezja, po potrebi pa deklariramo še podatkovne tipe, podtipe, konstante, notranje signale, podprograme, ... Dovoljeni načini priključkov so vhodni, izhodni, vhodno-izhodni in vmesniški. Vmesniški način se uporablja za izhodne priključke pomnilniških elementov. VHDL pozna naslednje podatkovne tipe: skalarne (celoštevilčni, realni, naštevalni in fizični), sestavljene (zapis in polje), kazalčne in datotečne. Uporabnik lahko sam deklarira nove tipe in podtipe. Podtip je podmnožica elementov nekega tipa. Posebej uporaben podatkovni tip je polje, saj ga lahko uporabljamo za krajši in preglednejši prikaz vrednosti signalov na vodilih.

Stavki v deklaraciji osebka niso namenjeni opisu dinamičnega obnašanja komponente, ampak preverjanju zunanjega vmesnika komponente. Z njimi lahko npr. preverjamo, če sta oba vhoda pomnilniške celice SR na logični enici.

Deklaracije osebkov so obvezne, saj specificirajo *zunanji pogled* na vezje in nekatere skupne lastnosti več različnih opisov iste komponente vezja. Zunanji pogled pomeni, da opazujemo komponento kot *črno škatlo* in vidimo samo njene priključke.

Primer deklaracije osebka *vrata_XOR*:

```
entity vrata_XOR is
    port (
        In1, In2 : in Bit;
        Out1 : out Bit );
    constant Delay : Time := 5 ns;
end vrata_XOR;
```

V zgornji deklaraciji deklariramo osebek *vrata_XOR*, ki ima vhodna priključka *In1* in *In2* tipa Bit in izhodni priključek *Out1* tipa Bit. Poleg priključkov je v zgornjem primeru deklarirana še konstanta *Delay* tipa Time z vrednostjo 5 ns. To konstanto lahko uporabljamo v vseh opisih arhitektur *vrata_XOR*.

Splošni zapis arhitekture ima naslednjo obliko:

architecture *identifikator* **of** *ime_osebka* **is**
    deklaracije
begin
    stavki
end *identifikator*;

V glavi arhitekture deklariramo spremenljivke, konstante, signale in druge konstrukte, ki veljajo samo znotraj arhitekture. Notranji signali predstavljajo povezave med posameznimi elementi opisane arhitekture. Pri deklaraciji signalov moramo navesti tip podatka, ki ga prenašajo.

Za zgled si oglejmo primer deklaracij v arhitekturi *opis1* za vezje z imenom *vezje*:

```
architecture opis1 of vezje is
    variable temp1, temp2 : Bit;
    constant Delay : Time := 7 ns;
    signal select : Bit_vector (2 downto 0);
    signal input, output :
        Bit_vector (7 downto 0);
begin
    .
    .
    .
end opis1;
```

V deklaracijah smo navedli, da v arhitekturi nastopata spremenljivki *temp1* in *temp2* tipa Bit, konstanta *Delay* tipa Time z vrednostjo 7 ns, signal *select*, ki predstavlja polje treh bitov, ter signala *input* in *output*, ki predstavljata polje osmih bitov.

S stavki v telesu arhitekture opisujemo obnašanje ali strukturo vezja. V zgornjem primeru bi lahko arhitektura *opis1* pomenila ali opis obnašanja ali opis strukture vezja *vezje*. Če bi želeli, bi lahko vezje opisali še z alternativnimi arhitekturami za obnašanje in/ali strukturo.

4.1 Opis obnašanja vezja

Obnašanje vezja opišemo s funkcijsko odvisnostjo vrednosti na izhodnih priključkih od vrednosti na vhodnih priključkih vezja. Pri opisu se ne spuščamo v podrobnosti o tem, kako je vezje sestavljeno, ampak gledamo na posamezne module vezja kot na črne škatle in opišemo samo akcije, ki se dogajajo na izhodnih priključkih vezja.

Obnašanje vezja lahko opišemo na dva načina: na *sekvenčni* ali *sočasni* način /11/. Pri sekvenčnem načinu opišemo obnašanje vezja s procesi, pri sočasnem načinu pa s sočasnimi prireditvami izhodnih vrednosti.

Proces je opis obnašanja dela vezja, običajno neke logične enote, ki ga pri opisu nima smisla deliti v manjše enote. Proces se izvede, ko postane aktiven, aktiven pa postane, ko se izpolnijo določeni pogoji. Pogoji so lahko spremembe vhodnih signalov ali ustrezni časovni pogoji. Več procesov se lahko izvaja sočasno in neodvisno drug od drugega, če le izpolnjujejo pogoje za svojo aktivnost. S procesi prirejamo vrednosti signalom na izhodnih priključkih vezja. VHDL omogoča specifikacijo časovnih zakasnitev pri prirejanju izhodnih signalov. Kot pri programskih jezikih lahko tudi v VHDL-u uporabimo krmilne stavke, kot sta npr. stavka *if-then-else* in *case* ter zanki *loop* in *for*.

Za zgled opišimo obnašanje vrat *vrata_XOR* s procesom:

```
proces_XOR : process
begin
    if In1='0' and In2='0' then
        Out1 <='0' after Delay;
    elsif In1='1' and In2='1' then
        Out1 <='0' after Delay;
    elsif In1='X' or In2='X' then
        Out1 <='X' after Delay;
    else
        Out1 <='1' after Delay;
    end if;
    wait on In1, In2;
end process;
```

Če sta na obeh vhodih enaki logični vrednosti, '0' ali '1', bo izhodu prirejena vrednost '0'. Če je na katerem vhodu vrednost 'X' (nedoločena vrednost), vrednosti izhoda ni mogoče določiti (priredimo mu vrednost 'X'), v vseh drugih primerih pa je vrednost izhoda '1'. Vrednosti se izhodom priredijo po preteku zakasnitve *Delay*. Opis procesa je zaključen s stavkom **wait on**, ki pomeni, da se bo proces ponovno aktiviral šele, ko se bo spremenila vrednost vsaj enega od naštetih vhodov.

Pri sočasnem modeliranju obnašanja opišemo sočasne prireditve izhodnih vrednosti. V tem primeru ni nobenih pogojev, ki bi prožili določeno akcijo. Tudi pri sočasnem modeliranju obnašanja imamo podobne prireditvene in krmilne stavke kot pri sekvenčnem modeliranju.

Za zgled opišimo obnašanje vrat *vrata_XOR* še s sočasnimi prireditvami:

```
Out1 <=
    '0' after Delay when
        In1='0' and In2='0' else
```

```
    '0' after Delay when
        In1='1' and In2='1' else
    'X' after Delay when
        In1='X' or In2='X' else
    '1' after Delay;
```

Zgornji opis je funkcionalno ekvivalenten opisu obnašanja na sekvenčni način s procesom. Iz primera je razvidno, da je opis pri sočasnem modeliranju obnašanja krajši in tudi preglednejši.

Za konec si oglejmo še, kako bi v VHDL-u opisali obnašanje preprostega sekvenčnega vezja. Prikazana je definicija zunanjega vmesnika in opis obnašanja pomnilne celice T s procesom:

```
entity T_FF is
    port(CLK : Bit; T : Bit;
        QOut :buffer Bit);
end T_FF;

architecture obnasanje of T_FF is
    signal s : Bit;
begin
    proces_T : process(CLK)
    begin
        if not CLK'Stable and CLK='1' then
            s <=T xor s;
            QOut <=s;
        end if;
    end process;
end obnasanje;
```

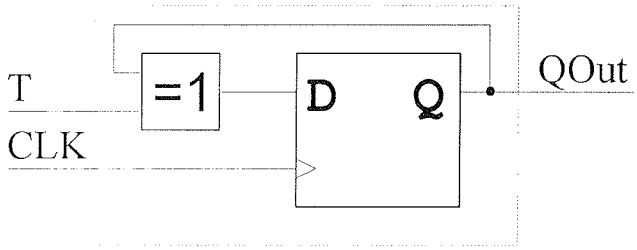
V opisanem primeru se proces aktivira ob vsakem prehodu ure CLK, signalu s pa se priredi nova vrednost le ob pozitivnem prehodu ure.

4.2 Opis strukture vezja

Strukturo vezja opišemo s komponentami vezja in njihovimi medsebojnimi povezavami. Iz strukture je razvidna notranja zgradba vezja.

Pri opisu strukture vezja je osnovni stavek stavek o deklaraciji in povezovanju komponent. Komponente so tisti osnovni gradniki vezja, ki jih ne razbijamo v bolj podrobne opise ali pa so podrobnejši opisi v ustreznih knjižnicah. Imena komponent in njihove zunanje vmesnike opišemo s stavki **component** med seboj pa jih povezujemo s stavki **portmap**.

V razdelku 4.1 smo že definirali zunanji vmesnik in opisali obnašanje pomnilniške celice T. Zdaj opišimo še njeno strukturo. Pomnilniško celico T lahko zgradimo npr. iz pomnilniške celice D in vrat XOR, kot je to prikazano na sliki 3.



Slika 3: Struktura pomnilniške celice T

Strukturo opisuje naslednja arhitektura:

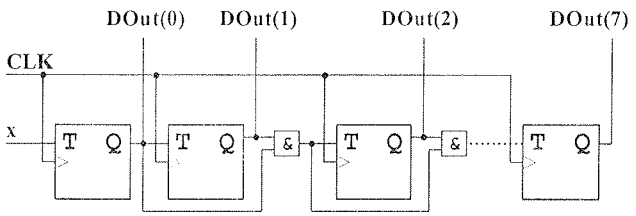
```
architecture struktura of T_FF is
    component vrata_XOR
        port (In1, In2 : Bit; Out1 : out Bit);
    end component;
    component D_FF
        port (CLK : Bit; D : Bit;
            Q : buffer Bit);
    end component;
    signal S1 : Bit;
begin
    vrata : vrata_XOR port map (
        In1 => T,
        In2 => QOut,
        Out1 => S1);
    FF : D_FF port map (
        CLK => CLK,
        D => S1,
        Q => QOut);
end struktura;
```

Stavek **architecture** pomeni, da opisujemo arhitekturo vezja. S prvim stavkom **component** smo deklarirali komponento, v našem primeru vrata *vrata_XOR* z vhodnima priključkoma *In1* in *In2* tipa Bit ter izhodnim priključkom *Out1* tipa Bit. Z drugim stavkom **component** je deklarirana še pomnilniška celica *D_FF*. S signalom S1 je predstavljena povezava med izhodom vrat in vhodom pomnilne celice. Povezave signalov s priključki komponente se opišejo s stavkom **port map**, ki mu sledijo pari

ime priključka komponente => ime signala.

Oznaki *vrata* in *FF* predstavljata simbolični imeni za komponenti *vrata_XOR* in *D_FF*.

Pri opisu strukture vezja imamo na voljo še dodatne stavke, ki nam olajšajo opis zahtevnejših vezij s *pravilnimi strukturami*. Pravilne strukture imenujemo tiste dele vezja, ki se v celotnem vezju večkrat ponovijo. To so lahko registri, večbitni števniki, ... Uporabnost stavkov, ki opisujejo pravilne strukture, je prikazana na primeru 8-bitnega števnika s slike 4:



Slika 4: 8-bitni števnik

```
entity stevnik is
    port (CLK : Bit; x : Bit;
        DOut : buffer
            Bit_vector (7 downto 0));
end stevnik;

architecture struktura of stevnik is
    component TFF
        port (CLK : Bit; T : Bit;
            Q : buffer Bit);
    end component;
    component And2
        port (I1, I2 : Bit; O1 : out Bit);
    end component;
    signal S : Bit_vector(7 downto 0) ;
    signal x : Bit := '1';
begin
    G1 : for I in 7 downto 0 generate
        G2 : if I=7 generate
            TFF_7 : TFF port map (
            CLK => CLK,
            T => S(I-1),
            Q => DOut(I));
        end generate;
        G3 : if I=0 generate
            TFF_0 : TFF port map (
            CLK => CLK,
            T => x,
            Q => DOut(I));
            S(I) <= DOut(I);
        end generate;
        G4 : if I>0 and I<7 generate
            And_1 : And2 port map (
            I1 => S(I-1),
            I2 => DOut(I),
            O1 => S(I));
            TFF_1 : TFF port map (
            CLK => CLK,
            T => S(I-1),
            Q => DOut(I));
        end generate;
    end generate;
end struktura;
```

Poleg prikazanih možnosti opisovanja strukture in obnašanja ima VHDL še številne druge konstrukte, kot so funkcije in procedure, bloki, knjižnice, pretvorba podatkov med različnimi tipi, itd.

5. Zakaj izbrati VHDL?

VHDL ima pred drugimi jeziki za opis vezij številne prednosti /9/:

- *Javna last:* VHDL je bil razvit s podporo vlade ZDA in je sedaj standard organizacije IEEE. Pri razvoju je imela vlada ZDA interes, da je VHDL v javni lasti in zanj ni potrebno plačevati licenc.

- *Podpora različnih metodologij načrtovanja in načinov implementacije vezja:* VHDL podpira več različnih metodologij načrtovanja (načrtovanje od zgoraj navzdol, načrtovanje od spodaj navzgor, uporaba knjižnic, ...) in različnih načinov implementacije (sinhrona vezja, asinhrona vezja, PLA, FPGA, ...). Opisni jezik VHDL je primeren za uporabo tako pri načrtovalnih orodjih, ki temeljijo na uporabi knjižnic, kot tudi pri orodjih za načrtovanje vezij ASIC.

- *Neodvisnost od tehnološkega procesa*: Opis vezja v VHDL-u je neodvisen od tehnološkega procesa izdelave integriranih vezij in zato nove tehnologije ne omejujejo njegove uporabe. Pri opisu ne navajamo, v kateri logični družini (npr. CMOS, NMOS, GaAs) bo vezje implementirano.

- *Opis na različnih abstraktnih nivojih*: VHDL omogoča opisovanje digitalnega vezja na različnih abstraktnih nivojih, od arhitekturnega nivoja do nivoja logičnih vrat. Ena od glavnih prednosti VHDL-a je možnost hkratnega opisa vezja na različnih nivojih.

- *Prenosljivost opisov*: Ker je VHDL standardiziran, je mogoče opise vezij v VHDL-u prenašati med različnimi sistemi in orodji, ki standard podpirajo.

- *Modularnost in ponovna uporabljivost*: VHDL je zasnovan podobno kot sodobni programski jeziki in omogoča dekompozicijo podatkovnih struktur in uporabo knjižnic z že izdelanimi komponentami vezja. Njegova modularnost dopušča skupinsko delo, kjer vsak načrtovalec razvija del vezja. Na koncu se opisi vseh načrtovalcev združijo v en sam opis.

- *Podpora vlade ZDA*: VHDL je nastal pod okriljem obrambnega ministrstva ZDA in zato morajo biti vsa integrirana vezja, ki so namenjena za potrebe vlade ZDA, opisana v VHDL-u. Posledica tega je, da se vedno več načrtovalcev odloča za VHDL in ne za kateri drugi jezik.

Ker VHDL ni edini jezik za opis vezij, se postavlja vprašanje, zakaj uporabljati VHDL in ne katerega drugega jezika. To vprašanje je bilo posebej očitno pred nekaj leti, ko na tržišču še ni bilo orodij, ki bi sprejemala opis vezja v VHDL-u in so ga uporabljali le v akademskih krogih. Vzrok za zakasnitev nastanka ustreznih orodij izhaja iz dejstva, da je VHDL standard za opisni jezik in ne za produkt katerega proizvajalca programskega orodja. Do nastanka VHDL-a je praviloma imel vsak proizvajalec programske opreme svoj opisni jezik, ki v večini primerov ni bil kompatibilen z drugimi. S povečevanjem ponudbe je na tržišču nastala zmeda, saj uporabnik ni vedel, za katero orodje in s tem opisni jezik naj se odloči. Tako se je pojavila potreba po standardizaciji in VHDL je bil sprejet kot standard IEEE-1076. Počasi so nastajala tudi programska orodja za VHDL, ki pa niso v celoti podpirala standarda. Iz standarda je bila izbrana samo določena podmnožica lastnosti. S tem je sicer bila možna njegova delna uporaba, vendar ni bil odpravljen eden od glavnih razlogov za njegov nastanek, to je prenosljivost opisov vezij med programsko opremo različnih proizvajalcev. Šele sedaj se na tržišču pojavljajo orodja, ki standard v celoti podpirajo.

Raziskava med 435 načrtovalci integriranih vezij v začetku leta 1992 je pokazala, da je tedaj 46% načrtovalcev uporabljalo opisni jezik Verilog in 39% VHDL /8/. Ista raziskava je pokazala, da kar 69% načrtovalcev namerava v prihodnosti uporabljati orodja na osnovi VHDL in 37% Verilog. To pa vsekakor pomeni, da bo v prihodnjih letih VHDL prevladal na tržišču.

6. Omejitve pri načrtovanju z jezikom VHDL

Čeprav ima opis vezja z jezikom VHDL številne prednosti pred drugimi načini opisa vezij, ima tudi nekatere slabosti in omejitve. Osnova jezika je bila postavljena s standardom IEEE-1076, ki pa je dokaj ohlapen in dopušča načrtovalcu, da jezik dograjuje s svojimi komponentami, funkcijami, procedurami in tipi podatkov. Takšni dodatki se običajno ne podajajo v samem opisu vezja, ampak so v knjižnicah. To pa pomeni, da se zmanjša prenosljivost opisov, saj morata imeti izvorno in ciljno orodje ekvivalentni knjižnici.

Druga slabost je ta, da lahko imajo opisi na različnih abstraktnih nivojih različno abstrakcijo podatkov. Primer za to je opis seštevalnika, kjer lahko obnašanje opišemo s stavkom

```
Z <= X + Y;
```

in pri tem sploh ne določimo števila bitov v sumandih, pri opisu strukture pa moramo imeti tudi to informacijo, ki je zelo pomembna pri uporabi orodij za avtomatsko sintezo vezja iz podanega obnašanja vezja. Pri reševanju tega problema so izdelovalci orodij izbrali dve poti. Prva je ta, da moramo pri opisu obnašanja uporabljati samo logične operatorje. S tem standard ni v celoti implementiran. Po drugem načinu se v takšnih primerih doda informacija o številu bitov, nad katerimi deluje operator, kot komentar. S tem se lahko izgubi prenosljivost, saj mora ustrezno orodje to informacijo znati uporabiti in je ne sme prezreti kot komentar.

Naslednji problem je časovno zaporedje prirejanja vrednosti signalom. Problem je razviden iz naslednjega primera:

```
P1 : process (x,y,w)
begin
    z <=x + y;
    q <=z + w;
end process P1;

P2 : process (x,y,w)
begin
    wait until clock'event and clock = '1';
    z <=x + y;
    wait until clock'event and clock = '1';
    q <=z + w;
end process P2;
```

V procesu P1 se izhodoma *z* in *q* priredi vrednost hkrati, v procesu P2 pa dobi *z* končno vrednost po prvem urnem impulzu, *q* pa šele po drugem urnem impulzu. Čeprav je končni rezultat v obeh primerih enak, pa proces P2 opisuje sekvenčno vezje, iz opisa procesa P1 pa lahko sklepamo, da gre za kombinacijsko vezje. Nekatera orodja imajo dodane *predprocesorje RTL (register-transfer level)*, ki iz opisa vezja razpoznajo, ali gre za opis sekvenčnega vezja, in nato v primerih, kot je zgornji, dodajo ustrezne pomnilniške elemente (registre in zadrževalnike) /12/.

Nekatera orodja ne dopuščajo specifikacije zakasnitve izhodne vrednosti s stavkom **after**. Vzrok za to omejitev je v dejstvu, da orodja za sintezo ne morejo zagotoviti, da se bo izhodna vrednost spremenila natanko po specificirani zakasnitvi.

7. Analogni VHDL

S sedaj veljavno definicijo VHDL-a je mogoče opisovati samo digitalna vezja. Želja načrtovalcev integriranih vezij pa je univerzalno orodje za načrtovanje tako digitalnih kot tudi analognih vezij in kombinacije obeh. Zaradi tega se v zadnjem času posveča precej pozornosti razširitvi jezika VHDL, ki bi omogočala opis analognih vezij in tudi nekaterih elektromehanskih sistemov. Takšna razširitev jezika bi nudila načrtovalcu enotno orodje za načrtovanje in opis kateregakoli električnega sistema. Z nadgradnjo VHDL-a se ukvarja več skupin, vendar njihovo delo ni skupno in je tako predstavljenih več različic analognega VHDL-a. Ena od njih je VHDL-A /7/. Značilnosti tega jezika so:

- enoten opis analogno-digitalnih in neelektričnih sistemov,
- močan jezik za modeliranje časa,
- popolna podpora hierarhičnemu načrtovanju,
- transparentna delitev na digitalni in analogni del sistema in
- možnost snovanja v frekvenčnem prostoru.

Odprta vprašanja, ki pri tej razširitvi še ostajajo, so:

- ni upoštevanja medsebojnega elektromagnetnega vpliva elementov,
- ne moremo modelirati ultravisokih frekvenc in mikrovalovnih sistemov in
- ne moremo modelirati in simulirati šuma.

8. Nadaljnji razvoj jezika

Nadaljnji razvoj jezika VHDL skuša odpraviti nekatere slabosti, ki so se pojavile v dosedanji praksi. Prvi korak je dopolnitev obstoječega standarda, ki poenoti oznake za logične nivoje. Pred tem je lahko vsak načrtovalec uporabljal nabor logičnih nivojev, ki mu je v danem problemu najbolj ustrezal. Tako je bila osnova dvonivojska logika (nivoja '0' in '1'), ki se je razširila v trinivojsko ('0', '1' in 'X'), štirinivojsko ('0', '1', 'X' in 'Z') in večnivojsko. To je onemogočalo združitev celotnega opisa vezja v primerih, kjer je del vezja opisan z eno logiko, del pa z drugo. Marca 1993 je bil postavljen standard IEEE-1164, ki za opise vezja definira devet logičnih nivojev ('U', 'X', '0', '1', 'Z', 'W', 'L', 'H' in '-') /2/. 'U' predstavlja neinicializirano stanje, 'X' neznano vrednost, '0' logično ničlo, '1' logično enico, 'Z' stanje visoke impedance, 'W' šibko nepoznano vrednost, 'L' šibko logično ničlo, 'H' šibko logično enico in '-' nepomembno vrednost.

Leta 1992, pet let po sprejemu prvega standarda, se je pričela revizija jezika. Dodana so bila nekatera dopolnila glede prirejanja vrednosti signalom in podrobneje obdelan časovni model opisa, ki je potreben za pravilno delovanje simulacijskega cikla. Dopolnila so bila sprejeta kot standard IEEE-1076-1993. Za ta standard se pogosto uporablja oznaka VHDL'93 ali VHDL'92 /3/.

Razvoj poteka tudi v smeri določitve standardnih knjižnic /4/. S tem bi se dejansko poenotili opisi vezij različnih načrtovalcev in tako postali resnično popolnoma prenosljivi med načrtovalskimi orodji različnih proizvajalcev.

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Prispelo (Arrived): 31.01.95 ***Sprejeto (Accepted): 06.02.95***

PRIKAZI DOGODKOV, DEJAVNOSTI ČLANOV MIDEM IN DRUGIH INSTITUCIJ

SISTEM CELOVITEGA OBVLADOVANJA KAKOVOSTI - TQM (Total Quality Management)

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Vpeljava sistema ISO 9000 in pridobitev certifikata po akreditirani tretji stranki je šele prvi korak na poti k zagotovitvi take ponudbe, ki bo vsestransko zagotovila zadovoljstvo tako kupca kot proizvajalca (in vseh členov verige), kar je predpogoj za sedanje in perspektivno pozitivno paslovanje. (Cena in kakovost izdelka še ne zadoščata za zadovoljstvo kupca.) ISO 9000 je torej potreben, ni pa tudi zadosten pogoj, za uspešno delovanje in trženje.

Poznano je, da ni dovolj, da je vpeljan in vzdrževan le sistem, ki omogoči ponovljivo izdelavo proizvodov brez napak - takšnih, kakršne pač nekdo zna delati. Proizvodi morajo povsem ustrezati potrebam kupcev (pa če tudi oni sami kdaj ne znajo povedati, kaj rabijo), pa tudi proizvajalčeve ambicije - ustvarjanje dobička - morajo biti zadovoljene. Zato je odločilno pomembno, da zna podjetje spoznati okolje in njegove zahteve ter trende in prisotno in porajajočo se konkurenco. Presoditi mora svojo ponudbo in svoje zmožnosti ponudbo pravočasno in v zadostni meri tako prilagoditi, da so dosežene zadostne in trajnejše konkurenčne prednosti in proizvodnja s profitom.

Za povsem nove proizvode pa je treba potrošnjo pogosto celo ustvariti. Poleg standardnih je na trgu vse več "appplication specific" elementov (izdelanih za specifično uporabo pri kupcu). Mnogi proizvajalci elementov so že zdavnaj spoznali, da je razvoj aplikacij in prodajni servis (svetovalne inženirske skupine na terenu), dobave JUST IN TIME in zadostna odzivnost za spremembe za uspešno trženje nujno potreben in spada k "ustrezni ponudbi". Izdelki in celoten servis morajo ustrezati potrebam kupca.

Kupci (zlasti srednji in manjši) ne želijo imeti stroškov z dragim preverjanjem kakovosti na vhodu. Raje izberejo zanesljivega dabavitelja, ki mu zaupajo. Dobavitelj pa izstavlja izjave o skladnosti svojih proizvodov deklariranim ali dogovorjenim (in seveda dokumentiranim) standardnim ali posebej dogovorjenim lastnostim ter s tem tudi prevzema odgovornost za vso nastala šodo.

Korak v to smer na področju proizvodnje elementov je gotovo sistem IECQ - IEC quality assessment system for electronic components (sistem ocenjene kakovosti s strani akreditirane tretje stranke - odobritev proizvajalca za posamezno skupino elementov - QA = skladnost z dogovorjenimi oz. z deklariranimi lastnostmi, oziroma odobritev sposobnosti proizvajalčevega proizvodnega procesa = CA ; Q=quality=kakovost), ki pa bazira na IEC in QC osnovnih, rodovnih, področnih in blank-detail standardih ter na odobrenih podrobnih standardih. Vpeljanost sistema ISO 9000 pa je predpogoj za pridobitev certifikata IECQ.

Da bi zagotovili kakovost ob najnižjih stroških (in s tem konkurenčnost) so prvi Japonci uvedli sistem CEOKA (Celovito obvladovanje kakovosti). V svetu se je iz njega izoblikoval pristop TQM (Total Quality Management = Celovito vodenje kakovosti) in še mnoge izpeljanke, med drugim MDQ (Market Driven Quality = Tržno vodena kakovost), ki ga zagovarja IBM, da si uredi svoje dobavitelje (ki pa morajo biti seveda urejeni v smislu TQM!) itd. Pri vseh sistemih gre za zavest, mativacijo in odgovornost za kakovost vseh udeležencev v poslovnem procesu.

Vsak od izpeljanih sistemov izhaja iz namena čim boljšega zadovoljevanja potreb kupcev.

Ni torej certifikat zadostni pogoj, da bo kupec pri nas kupil. Pri kupcu moramo blti dovolj poznani in dovolj prisotni in mu ponuditi blago v takšni izbiri, ki je zanj sprejemijiva in ga naredi konkurenčnejšega, slediti moramo razvoju njegovih potreb in biti z lastnim razvojem celo korak pred njim, da mu lahko nove zahteve takoj izpolnimo ali mu celo mi predlagarno zanj ugodnejše rešitve in smo pri tem boljši in cenejši od konkurence (in jo po možnosti ob sprejetju naše rešitve za daljši čas izključimo). Pri tem pa mora biti naš servis kvaliteten in ravno ob dogovorjenem času (JIT) in biti moramo odzivni na eventuelne zahtevane spremembe. Med kupcem in dobaviteljem se mora zgraditi zaupanje in veliko razumevanje - partnerski odnos v smislu dolgoročnega preživetja obeh (in profitnega poslovanja), ki je možno le ob stalnem prilagajanju drug drugemu in novim situacijam v okolju. Zahteve so vsak dan hujše. (Partnerski odnos ne more pomeniti lagodnosti, absolutne varnosti m popustljivosti. Pomeni upravičevanje zaupanja.). IBM postavlja v okviru svojega TQM sistema zahtevo "5 UP". V vsakem naslednjem obdobju se vse zahteve poostrijo 10x in to potrjevanje kratkih rokov in točnosti dobav, znižanje števila napak (cilj je 6σ oziroma 3.4 ppm) pri proizvodih in v logistiki, hitro reagiranje in vse večja odzivnost na željene spremembe.

Vsi partnerji (vsi dobavitelji in kupci v verigi) morajo torej uvesti in delovati v TQM.

Gre torej za spremembo vedenjskih vzorcev tako posameznikov, kot podjetja, gre za privzem nove kulture, nove politike in metodologij.

Tudi osnutki sprememb družine standardov ISO 9000 že predvidevajo spremembe v to smer, saj prehajajo iz Quality Assurance na Quality Management. (iz zagotavljanja na vodenje kakovosti).

Gre za stalno se ponavljajoč krog: opazovati potrebe kupca ter naših zmožnosti, analiza stanja in trendov, poiskanje izboljšav, preverjanje izboljšav in njihovo uvedbo v proizvodnjo, pa zopet opazovanje, ... Postati in ostati moramo najboljši dobavitelj.

Da bi bilo to v maksimalni meri možno, pa mora proizvajalec obvladovati celoten proces, imeti torej tudi odlično povezavo z dobavitelji in kupci ter imeti dovolj informacij znotraj podjetja. Osvojena mora biti filozofija Internega kupca (na naslednje delovno mesto ne sme priti neustrezen proizvod). Na ta način so stroški najnižji in verjetnost, da pride h kupcu defekten proizvod, najmanjša.

Obvladovani morajo biti vsi tehnični, ekonomski, administrativni in človeški faktorji (da se preprečijo kakršne koli neskladnosti, pomanjkljivosti,...). Obvladovan proces mora torej v vsakem trenutku zagotoviti kupcu proizvod, ki ga ta pričakuje.

Q management pomeni vse aktivnosti za postavitev in uresničitev Q ciljev, politike in strategije s tem da se izvrši:

- Q planiranje
- Q usmerjanje in vodenje
- zagotavljanje Q
- izboljšave lastnosti in Q izdelkov
- pri tem se upošteva zaščita okolja,... .
- usposabljanje za Q

Kako postopamo?

VODSTVO

- vodstva postavlja in objavlja politiko kakovosti (vse je usmerjeno na zadovoljevanje pričakovanj kupcev in s tem dolgoročno uspešno poslovanje in ustvarjanje dobička). Vodstvo ugotovi tržne potrebe in tiste, za katere ima dovolj virov (kadrovskih in finančnih - razvoj, ureditev proizvodnje,..) tudi realizira. (Delamo za kupca, ki ga ne želimo razočarati - izgubiti!)
- vodstvo uvaja kulturo kakovosti v podjetju in postavi skupne cilje podjetja (vsak posameznik pa mora biti osveščen in svoja prizadevanja podrediti temu skupnemu cilju) ter ustrezno priredi strukturo ter kadrovsko in izobraževalno politiko. Cilji morajo biti ambiciozni in vsako leto višji.
- vodstvo ustrezno izobrazi in motivira udeležence za kakovostna dela.
- vodstvo postavi plan kakovosti in merljive cilje - merila za ugotavljanje uspešnosti in merjenje napredka ter ugotavlja učinkovitost sistema. Zajeti so vsi deli procesa. Vodstvo zahteva stalne, načrtovane izboljšave na vseh področjih. Vodstvo pregleduje rezultate, pregleduje stroške kakovosti ter proži ukrepe za izboljšanje stanja in za znižanje vseh vrst stroškov.
- vodstvo postavi organizacijo in delegira pristojnosti in odgovornosti na ustrezne sodelavce, katerih vsak doprinese svoj del k uspehu celote. Odločanje mora biti prenešeno na dovolj nizke nivoje.
- vodstvo postavi tim kakovosti, ki vsklajena deluje in usmerja nastajanje kakovosti tako, da pregleduje rezultate, proži ukrepe za izboljšave na vseh področjih ter preverja njihovo realizacijo.

INFORMACIJSKI SISTEM

- Vsakdo mora vedeti, kaj se od njega pričakuje in biti mara seznanjem z rezultati svojega dela, da lahko ustrezno ukrepa. Zajemanje in obdelava podatkov o procesu naj je smiselno urejena (po možnosti avtomatsko).

PROCES

- nadzor je organski del poslovnega procesa, da se ugotavljajo in korigirajo ev. neskladnosti. Te naj se odkrijejo čim bolj zgodaj v procesu (takoj na mestu, kjer nastajajo), da bodo stroški izmetov čim nižji in da bo možno takoj ukrepati.
- analizirajo se reklamacije
- v vseh delih procesa postopamo tako, da do neskladnosti sploh ne pride - uporablja se SPC (Statistic process control - statistično obvladovanje procesa), da se ugotavlja dejansko stanje (in trendi) opazovanih karakteristik proizvodov napram postavljenim mejam in se lahko pravočasno korigira proces (še preden nam uide izven postavljenih mej). Analizirajo se rezultati in ugotavlja sposobnost (obvladovanje) delov in celotnega procesa
- Izdelek in proces je treba stalno izboljševati (sprememba materiala, dobaviteljev, našega poslovnega procesa, našega prodajnega in dobavnega servisa,...).

RAZVOJ

- v razvoju se vrši analiza napak (ugotavljanje vzrokov) in se zbirajo podatki o problemih in novih željah in zahtevah kupcev.
- stalno se zasleduje razvoj tehnologij v svetu, da bi tudi mi bolje in ceneje izdelovali ustrezne izdelke.
- že v fazi razvoja se mora nov proizvod tako oblikovati (postavitev in spoštovanje načrtovalskih pravil), da upošteva zmožnosti procesa ali se po potrebi predvidi možnost izboljšave procesa. (uporablja se tudi diagram vzrokov in posledic, FMEA, ... načrtovanje eksperimenta,...). Razvoj mora biti hiter in dokončan

(vsa potrebna - tudi kontrolna, nabavna, prodajna,... dokumentacija in postopki, ki omogočajo ponovljivost in nenastajanje napak, novi izdelki morajo biti atestirani).

KADRI, IZOBRAŽEVANJE, MOTIVACIJA

- v prizadevanju za kakovost sodelujejo (vplivajo) vsi zaposleni (saj se kakovost ustvarja, ne pa na koncu izfiltrira) - pojem internega kupca!
- uvedeno mora biti sistematsko izobraževanje vseh zaposlenih - vsakega svojim odgovornostim primerno in privzgajanje filozofije "Nič napak" (Zero-defect), 6σ, ppm, ...
- urejeno mora biti motiviranje za ustvarjanje kakovostne ponudbe in s tem zadovoljevanje kupcev.
- v podjetjih morajo delovati krožki kakovosti - vsi zaposleni iščejo in predlagajo rešitve problemov, vodje pa vzpodbujajo delovanje krožkov.

OPREMA

- da bi bilo podjetje konkurenčno, mora v svojem procesu uporabljati dovolj produktivno (procesu in količinam prilagojeno) in zanesljivo opremo, ki omogoča nastajanje zahtevanih lastnosti. Biti mora primerno vzdrževana, nadzorovana in zagotavljati mora "sposobnost procesa".

DELO S KUPCI IN DOBAVITELJI

- v skupnem delu je treba zagotovitii kakovost v celi verigi ob minimalnih stroških
- v tesnem sodelovanju med dobaviteljem in kupcem se je možno dogovoriti, kateri parametri so zares pomembni - kritični za proces, da ne bi po nepotrebnem drazili proizvodov in uporabnih izdelkov zvrščali v izmet.

PRILAGAJANJE PROGRAMA / PONUDBE V SLOVENSKIH INDUSTRIJSKIH PODJETJIH

Igor Pompe
Iskra IEZE Holding d.o.o., Ljubljana

Spremembe so nujno zlo, ki pa sposobnim omogoči, da prevzamejo posel manj sposobnim!

Preživi torej tisti, ki zna spremembe pravočasno predvideti in se pravočasno v zadostni meri prilagoditi - usposobiti za nove zahteve - razmere. To pa lahko stori le podjetje, ki si je zagotovilo vse potrebne resurse.

MNOGI NAŠI PROGRAMI SO V KRIZI !?

Kljub temu, da smo nekatere prihajajoče spremembe (večina prihaja počasi) znali opaziti in smo imeli ideje, kako se prilagoditi, *nismo izdelali dovolj uresničljivih projektov za njihovo realizacijo "do konca"* - do konkurenčno sposobne in na trgu priznane proizvodnje, ki zagotovi povrnitev vseh vložkov s primernimi obrestmi (za to pa je potreben dobro pripravljen strateški projekt, ki poleg ciljnih konkurenčnih prednosti preveri tudi vse potrebne resurse za proizvodno in trzno realizacijo in tudi rizike), ali pa *so nepričakovane spremembe v okolju onemogočile načrtovano realizacijo.* Takšnih političnih in trznih sprememb, kot jih je doživelo slovensko gospodarstvo v zadnjih štirih letih, ni mogel predvidevati nihče. (Poleg zmanjšanja potreb in dostopnosti na določene trge smo na nekdaj ugodnih trgih doživeli erozijo cen, poleg tega pa še doživeli izreden pritisk novih daljnovzhodnih proizvajalcev ter podcenjeno ponudbo vzhodnoevropskih ponudnikov in ciklično krizo v svetovnem gospodarstvu.) Inkubator, v katerem smo destletja živeli, se je naenkrat odprl. Naša, na videz cenejša, delovna sila pa je v resnici draga (obremenitve ob tolikšnem številu neproduktivnih prebivalcev, ki jih moramo preživeti) in z uporabo delovnih naprav, ki ne ustrezajo več sedanjemu času tudi premalo produktivna. Podjetja tudi niso bila sposobna na hitro izboljšati svojih prodajnih ekip.

Tako so mnogi dokončani razvojni projekti končali na polici in mnogi napori so ostali zgolj strošek. Kot ni vse zlato, kar se sveti, tudi ni za vsak poslovni subjekt vsaka, še tako blesteča, programska usmeritev tudi izvedljiva in koristna.

Poglejmo le nekaj izkušenj:

- **Elementi za površinsko montažo!**

Že v zgodnjih osemdesetih letih smo bili opozorjeni na "četrto elektronsko revolucijo" - tehnologijo površinske montaže elementov na tiskana vezja (SMT) in na zahtevo po neožičenih miniaturnih elementih za polaganje in spajkanje na tiskana vezja (SMD). Hitro smo razumeli ta velik izziv in hkrati veliko priložnost za uveljavitev, pridobitev novih kupcev in prehitenje številne konkurence. Podjetja - proizvajalci elementov v Sloveniji so kaj hitro razvila prve prototipe SMD elementov, saj so obvladala osnovne tehnologije za izdelavo elementov. Razvojne naloge so bile tudi podprte v podjetjih in s

strani Republiške raziskovalne skupnosti. Naloga in delo razvojnikov pa se je po takratnem pojmovanju žal zaključila pri izdelavi prototipa. Kot to velja za "klasične" standardne elemente, velja enako za SMD, da jih je možno konkurenčno proizvajati le v primerno velikih količinah in na ustrezni visoko avtomatizirani opremi. Potrošnja "novitete" pa je v svetu le počasi naraščala. Najresnejši proizvajalci so se nanjo kljub temu pravočasno pripravili (vlagali so v avtomatsko proizvodnjo, čeprav v prvih letih svojih vložkov niso mogli amortizirati). V Sloveniji za tako pripravo ni bilo ne dovolj nuje, ne dovolj sredstev. Celo programi, ki so že prešli začetne težave, so omagali. K temu so dodatno pripomogle zunanje razmere, kot je zamujanje Evrope v teh tehnologijah, selitev težišča porabe elementov v dežele jugovzhodne Azije, svetovna kriza v letih 91 do 93 in balkanska vojna.

Tako danes na tem (na področju elektronskih elementov najperspektivnejšem) področju ne pomenimo skoraj nič.

- **Mikroelektronika**

Sorodna, le še nekoliko dražja zgodba o neuspehu se je zgodila nekoliko prej na področju mikroelektronike. Tehniko smo v določeni fazi relativno dobro obvladali, nismo pa znali porabiti proizvedenega in zlasti nismo imeli moči v ta segment čedalje več vlagati. Poznano je, da vlaganja z miniaturizacijo eksponencialno naraščajo.

- **Podobnih primerov je še več.**

Kapital smo z vsako reformo bolj razdrobili. Posamezni deli nekdaj velikih podjetij, ki bi lahko poslovala kot koncerni in prevzemala tudi večja sistemska naročila za večje tuje kupce, so se povsem osamosvojili (small is beautyful) in vase zaprli. Vsaka enota služi drugemu kapitalu - drugim interesom. Trženje smo povsem razdrobili. Pretok znanja in drugih informacij smo ustavili in vse sinergije ubili. Vsaka organizacija opravlja sama vse funkcije, pa čeprav manj strokovno in manj ekonomično. Vsakdo kupuje izven hiše drugačno (včasih dvomljivo) novo znanje in storitve. Image na trgu smo porušili. Premalo učinkovite zunanjetrgovinske organizacije smo pustili odmreti ali se preusmeriti, namesto, da bi jih usposobili. Številne prednosti, ki smo jih nedvomno imeli vsaj pred vzhodnoevropskimi konkurenti, smo v veliki meri izgubili. Dopustili smo, da so nas zapustili nekateri sposobni kadri. Proizvodenj in prodajnih ekip za izdelke za specifične aplikacije nismo usposobili. V posodobitve nismo več vlagali.

Posledica

Le še na redkih izdelkih smo uspeli zadržati konkurenčnost pri globalni strategiji. Na področju standardnih izdelkov skoraj da nismo več konkurenčni.

Za trženje in razvoj application specific izdelkov nismo dovolj storili in zato nimamo dovolj naročil.

Mnoga podjetja smo prepustili v "last" in upravljanje Skladu, ki pa se ne spušča v resnične vzroke za neuspešno poslovanje in rešuje vse probleme na šablonski način - z zmanjševanjem zaposlenosti na počez (zdravljenje vseh bolezni s klistirom in ricinusom).

Dele podjetij s skrajno nizko ocenjeno dinamično vrednostjo prodajamo.

KAKŠNA PODJETJA SO V SLOVENIJI USPEŠNA ?

Če ne upoštevamo nekaterih novih, še majhnih zvezd in uporabimo podatke, objavljene v GV (št 4/95) in Managerju (julij/avgust 94) o najuspešnejših podjetjih oz. največjih izvoznikih, lahko zaključimo:

- največji dobiček imajo podjetja, ki delajo prvenstveno za domači trg izdelke, ki se običajno lokalno proizvajajo in trošijo (pivovarne, prehrambena industrija,....), ki prodajajo storitve in podjetja, ki imajo monopol (elektrogospodarstvo, komunalna podjetja, igralnice, ..), podjetja, ki imajo tuja sovlaganja in zagotovljen trg skozi mrežo tujega partnerja in uvozniki.

- Med največjimi izvozniki, med katerimi je veliko podjetij v solasti tujih uveljavljenih firm (Revoz, ETA Cerkno, Sava-Semperit, Danfos, Henkel-Zlatorog, MGA-Siemens, Iskra TEL,..), in tudi veliko domačih podjetij, ki z večine tesno sodelujejo s tujimi firmami kot komplementarni dobavitelji ali poddobavitelji sestavnih delov in izjemoma finalnih izdelkov z lastno blagovno znamko (Gorenje G.A., Domel, Kolektor, Unior, ETI-Izlake, Paloma, Elan, Krka, Lek, Elektronika Velenje in Iskrine firme Števci, Avtoelektrika, Kondenzatorji, Fotona, VCS in še več manjših), je le malo podjetij, ki izkazujejo primeren dobiček na vložena sredstva (Elan, Iskra Števci, ETA Cerkno, Paloma, Henkel-Zlatorog, Unior, Lek, Krka, Sava, ..). Mnogi pomembni izvozniki pa se bore za preživetje in se jim konkurenčna sposobnost iz leta v leto manjša.

- Uspešni so v večini primerov tisti, ki:
  - imajo dovolj velik domači trg za izdelke, ki se proizvajajo in trošijo lokalno
  - imajo postavljeno lastno prodajno mrežo ali dogovore za izkoriščanje obstoječe mreže partnerjev
  - imajo sodobne izdelke in obvladajo tehnologije (dovolj hitro sledijo spremembam)
  - imajo dovolj velike kapacitete in dovolj produktivne procese
  - izkoriščajo poceni surovine in/ali poceni delovno silo.

MOŽNI IZHODI IZ SITUACIJE:

- poizkusiti enote ponovno kapitalsko povezati zaradi izmenjave in boljšega in širšega izkoriščanja znanja in izkušenj, izkoristka sinergičnih učinkov, kapitala itd. ter tako ceneje in uspešnejše poslovati.

- V mreži povezanih podjetij poenotiti informacijski sistem, da bo možno brez nepotrebnih stroškov izkoriščati informacije in izmenjevati znanje. Vse funkcije v podjetjih medsebojno tesno povezati.
- Obstoječe konstrukcijske izkušnje in tehnologije ter obstoječo opremo
  - dopolniti in usposobiti za zagotavljanje konkurenčnosti že vpeljanih serijskih izdelkov (načrtovati zadostne konkurenčne prednosti, postaviti ciljne cene, dopolniti in ustvariti zadostne kapacitete, dovolj vlagati)
  - uporabiti za izdelavo specifičnih izdelkov po želji kupcev (in tej nalogi prilagoditi tudi svoj trżni nastop).
- Usposobiti obstoječe in pridobiti nove kadre ki,
  - bodo znali strateško planirati
  - bodo osvojili filozofijo TQM
  - bodo poznali potencialne nove aplikacije in znali predvideti nove zahteve kupcev
  - se bodo znali dovolj strokovno in uspešno pogovarjati s kupci in dobavitelji (jezik)
  - bodo znali razviti izdelke v skladu z zahtevami kupcev, z zmožnostmi opreme ter v okviru ciljnih stroškov (stalne izboljšave, uvajanje inovacij)
  - bodo znali poiskati oz. skonstruirati fleksibilno in dovolj produktivno opremo.

  Za to pa je treba kadre stalno dopolnilno izobrażevati (znanje poglobiti in razširiti) ter poskrbeti za zadosten pretok znanja. Kadre motivirati za trżni uspeh, za inovacije, za stalne izboljšave. Osnovna tehnična izobrażevanja dopolniti (tehnologija, ekonomika, jeziki, ..) .

  Pri zmanjševanju zaposlovanja bi morali biti bolj daljnovidni, da ne bi izgubili prav kadrov, ki naj bi bili sposobni realizirati inoviranje naše ponudbe. Nove ideje naj bodo vspodbujane, hkrati pa kritično presojane.
- Programe kritično trżno in dohodkovno analizirati, ugotoviti prave razloge za premajhen uspeh, sile koncentrirati na dohodkovno in perspektivno ugodnejše programe. Koncentrirati tudi marketinško dejavnost na ciljne odjemalce in trge. Ne pavšalno zmanjševati zaposlenosti. Kritična mesta je nujno kadrovsko okrepiti.
- Posebno pozornost posvetiti trżenju (lastno in pogodbeno). Usposobiti svoje trżnike in poiskati poslovne-kooperacijske partnerje - zaveznike za dopolnjevanje programa in uspešno trżenje (izkoriščanje že vpeljanih trżnih kanalov).
- S kupci vspostaviti partnerske odnose in z njimi skupaj razvijati nove izdelke.
- Poiskati poslovne partnerje za skupen razvoj.
- Prenesti del stroškov razvoja in proizvodnje na dobavitelje ter jih zavezati za kakovost.
- Ne le iskati partnerje za nakup naših kapacitet. V Slovenijo bi morali pritegniti investitorje, ki bodo tu odprli nove proizvodnje in tako ustvarili (v bližini) novo industrijsko potrošnjo.
  Tudi obstoječe vodilne firme bi morale generirati nove jedrne programe in s tem v Sloveniji generirati potrošnjo za podsestave in storitve.

Janez Štefanič - Manager leta 1994

LETOŠNJO NAGRADO "manager leta", ki jo vsako leto podeljuje društvo Manager, je prejel diplomirani inżenir elektronike **Janez Štefanič**, direktor družbe Iskra - industrije kondenzatorjev in opreme v Semiču. Na čelu omenjene tovarne je od leta 1991, potem ko je podjetje zaradi razpada jugoslovanskega trga zašlo v veliko krizo in je imelo 3,7 milijona mark izgube. Do danes mu je s pomočjo vodilne ekipe in seveda ob sodelovanju vsega kolektiva uspelo stanje sanirati, tako da że poslujejo z dobičkom. O dobrem vodenju oziroma o pravilni poslovni politiki ter dobrem delu vsega kolektiva pričajo tudi uspehi, doseżeni v zadnjem obdobju.

Tovarna kondenzatorjev in opreme Semič je povečala izvoz zunaj nekdanje Jugoslavije s 27 milijonov mark v letu 1991 v naslednjih dveh letih za dobrih 40 odstotkov; lani je tako izvoz znašal 38 milijonov mark. Letošnji načrt izvoza je ponovno višji za dobrih 20 odstotkov in bo po dosedanjih rezultatih sodeč znašal konec leta okrog 46 milijonov mark. Tako semiška Iskra dosega że več kot

80 odstotkov svoje realizacije na tujih trgih. Iz teh podatkov izhaja, da je bil dosežen pravi skokovit preobrat v trženju, ki ni le nadomestil nekdanje prodaje na jugoslovanskih trgih, ampak jo je tudi močno presegel.

Realizacija in izvoz semiške Iskre (v milijonih DEM)

Leto	bruto realizacija	izvoz	Slovenija
1991	43,0	27,016	
1992	42,0	36,06	
1993	46,0	39,0	7,0
1994 (poll.)	26,5	23,035	

Pred slovensko samostojnostjo je veliko slovenskih podjetij v svoje izdelke, ki so jih prodajala na jugoslovanske trge, vgrajevalo semiške kondenzatorje. Po ločitvi pa je na slovenskem trgu občutno padlo povpraševanje po kondenzatorjih iz Semiča, ker so se pač ti trgi zaprli.

Takšna odločna preusmeritev na tuje je terjala bistveno prestrukturiranje proizvodnje, predvsem pa je bilo treba dvigniti kakovost proizvodov in poslovanja nasploh, tako da je danes podjetje v sklepni fazi za pridobitev mednarodnega certifikata kakovosti ISO 9000.

Razen tega je Iskri v Semiču uspelo doseči občutno razdolžitev in zmanjšanje svojih obveznosti; sicer pa danes večji del posluje z lastnimi sredstvi. Hkrati z odločnim preobratom v trženju je semiška Iskra spet začela zaposlovati delavce. Tako so od lanskega oktobra dodatno zaposlili okrog 100 ljudi. Pri tem so plače v podjetju na ravni kolektivne pogodbe v branži, v kateri sicer semiška Iskra dosega 12 odstotkov prihodka dejavnosti proizvodnje električnih strojev.

V tem času je podjetje doseglo tudi številne izboljšave v tehnologiji, v korist boljšega počutja in delovnih razmer zaposlenih, tako da so škodljivi vplivi na okolje minimalni oziroma nižji, kot zahtevajo mednarodni standardi. In ne nazadnje je semiška tovarna kondenzatorjev in opreme s skoraj 1400 zaposlenimi zelo pomemben dejavnik za gospodarsko-socialni razvoj vse Bele krajine.

Portret nagrajenca

Janez Štefanič, direktor družbe Iskra Semič od leta 1991. Rojen 1946, diplomirani ing. elektronike, 23 let delovne dobe.

Dosedanje delo: Iskra Semič kot vodja laboratorija, vodja razvoja, član KPO za razvoj, direktor družbe.

Osnova za priznanje

Preusmeritev prodaje na tuji trg.
Prestrukturiranje proizvodnje.

Rezultati izboljšav

Izvoz v države zunaj nekdanje Jugoslavije se je povečal od 27 milijonov DEM (leta 1991) na 38 milijonov DEM (leta 1993) ali za 42 odstotkov.
Plan 1994 je 46 milijonov DEM. Izguba v letu 1990 je bila 3,7 milijona DEM.
Zaposlujejo nove delavce. V letu 1994 do maja 60 delavcev. Ob prenovi izboljšave v tehnologiji z vidika počutja zaposlenih in varovanja okolja.

Na teh naštetih uspehih torej temelji letošnja nagrada manager leta. A kakšne kvalitete mora imeti človek, da mu uspe takole "nasedlo barko", kot je bila semiška Iskra, v pičlih treh letih zakrpati, jo spraviti z jugočeri in uspešno zapluti v vode mednarodnega trga? Prvo, kar pade v oči, je zvestoba, v tem primeru semiški Iskri in torej Beli krajini. Lahko bi rekli, da Janez Štefanič ne pozna drugega kot semiško Iskro. Je rojen Belokranjec, kjer se je pred 48 leti rodil v od Semiča deset kilometrov oddaljenem Podzemlju. Leta 1970 je diplomiral na ljubljanski elektrotehniki, smer šibki tok, in bil čez dva dni že zaposlen v semiški Iskri.

"Pravzaprav sem že prej živel od naše Iskre, saj sem prejemal štipendijo že, ko sem od leta 1961 hodil na elektrotehniški oddelek srednje šole," pripoveduje, "in tako sem vseh 23 let delovne dobe in vse svoje delovne izkušnje dobil v tem kolektivu."

Tako je pravzaprav na lastni koži spoznal vse faze delovnega procesa, kakor je pač zorel in napredoval. Tako je med drugim bil vodja laboratorija, vodja razvoja in član kolegijsko-poslovodnega organa za razvojnotehnično področje. Ko se je leta 1991 kriza zaostrila, je bil predsednik upravnega odbora...

- Kako ste postali direktor?

ŠTEFANIČ: V začetku leta 1991 so se črni oblaki zaradi tranzicije in izgube jugoslovanskih trgov nad našo Iskro močno zgostili. Izguba je naraščala, bili smo nelikvidni, naročila so usihala, delavci pa so hoteli plačo, zato so grozile stavke, skratka položaj je bilo napet. Splošna zahteva je bila, da naj direktor naredi sanacijski program. Ni ga naredil, ker je takrat res bilo težko najti rešitev. Zato sem ga naredil jaz, ko so me imenovali za direktorja. . .

- Katere vaše lastnosti so bile odločilne, da ste v tako kritičnih trenutkih dobili mesto direktorja?

ŠTEFANIČ: Morda to, da so me ljudje v neposredni proizvodnji bolj poznali, saj sem dvajset let potoval skozi proizvodni proces...

Rezultati podjetja

Delež v dejavnosti: 12% prihodka dejavnosti proizvodnje električnih strojev.
Število zaposlenih: 1.388.
Skupaj viri sredstev: 47 milijonov DEM.
Obseg bruto dobička: 1992 - 47 tisoč DEM, 1993 - 60 tisoč DEM,
Skupaj prihodki: 1992 - 49 milijonov DEM, 1993 - 53 milijonov DEM, indeks 93/92 = 110%..
Prihodki od prodaje na drugih tujih trgih / skupaj prihodki: 1992 - 71%, 1993 - 72%, indeks 93/91 - 142
Bruto dobiček + odhodki za obresti / skupaj viri sredstev: 1992 - 4%, 1993 - 3%, indeks 93/92 - 82%
Obveznosti / skupaj viri sredstev: 1992 - 38%, 1993 - 36%, indeks 93/92 - 82%

Socialni vidik

Bolniška: 1993 - 8%, maj 1994 - 9,5%, fluktuacija 1993 - 7,3%
Delovnih invalidov: 2,7%
Plače na ravni kolektivne pogodbe in panoge (leta 1994). Vse emisije škodljivih snovi so pod dovoljenimi. Izboljšave tehnologije.

Prispevek predlaganca k izboljšavam

Odločilni za uspeh so strokovnost, sposobnost spodbujanja sodelavcev ter timsko delo.

• Ali prejšnji direktor ni bil vaše stroke?

ŠTEFANIČ: Ne, on je bil iz finančne stroke. Slabše se je spoznal na trg in na proizvod.

• Ali to pomeni, da je za uspešnega managerja pomembnejše, da je najprej doma v stroki, v kateri deluje njegovo podjetje, pa si potem komplementira znanje iz ekonomije?

ŠTEFANIČ: Jaz seveda ne bi podcenjeval nobenega znanja, ampak mislim, da managerji, ki obvladujejo proizvodnjo in aplikacijo, bolje uspevajo. Sicer pa poznam precej tehnikov, ki so pozneje postali managerji, in manj managerjev, ki so svoje znanje dopolnjevali s tehničnim. Sicer pa je za managerja potrebno kompleksno znanje. Tu sem pa seveda spada tudi tehnika, tehnologija in znanje o lastnih tehnoloških zmožnostih. Kar zadeva mojega predhodnika, pa je povsem logično, da se v takšnih kriznih trenutkih srd delavcev usmeri na tistega, ki je na vrhu, pa kdorkoli je to. Prejšnji direktor je pač bil žrtev tedanjih razmer.

• In kaj ste naredili najprej, ko ste prevzeli direktorsko funkcijo?

ŠTEFANIČ: V prvem hipu nič. Pač, najprej sem, če bi rekel po nogometno, umiril žogo. In to mi je uspelo. Potem, ali pa hkrati, sem ljudem predstavil realni položaj, ali nalil čistega vina, kot bi rekli po domače. Nato smo skupaj s sodelavci pripravili ukrepe. Predvsem smo se osredotočili na varčevanje in racionalizacijo, s čimer smo želeli zmanjšati stroške. Drugi ukrep je bilo zmanjšanje zalog, s čimer smo hoteli sprostiti finančne in prostorske zmogljivosti. Nadalje smo si prizadevali bolje organizirati proizvodnjo, torej bolje izkoristiti delovni čas, uvesti disciplino in končno, a ne nazadnje urediti plače. To je bil hkrati mobilizacijski moment, kjer je veljalo geslo: če bomo preživeli, bomo živeli bolje.

• Je bilo v tej sanaciji predvideno tudi odpuščanje delavcev?

ŠTEFANIČ: Odpuščanje ni bilo predvideno. Smo pa zahtevali od služb, da maksimalno iščejo možnosti za nove kupce, skratka, da bi se povečala proizvodnja. Seveda pa smo upoštevali tista dela, ki so pokrila stroške in dala vsaj minimalen dobiček. No, to nam je očitno uspelo, kajti za primer naj povem, da je bilo kar 150 naših fantov v teritorialni obrambi, kajti jaz sem direktorsko mesto prevzel tik pred agresijo na Slovenijo, aprila 1991, pa smo v tem času kljub temu povečali proizvodnjo.

• Je slovensko osvobajanje negativno vplivalo na vaše načrte za večji prodor na tuje trge?

ŠTEFANIČ: Po svoje je to celo pripomoglo k verodostojnosti naše poslovnosti v tujih očeh, čeprav se to morda sliši paradoksalno. Veste, proizvodnja kondenzatorjev je specifična po tem, da kupec ne more čez noč zamenjati kooperanta, saj se kooperant v pogodbah zaveže za natančno specificiran kondenzator v veliki seriji. Recimo za kondenzator, ki preprečuje radijske motnje v kakšnem električnem aparatu, za uporabo v gospodinjstvu itd. A ker je pri nas izbruhnila vojna, so naši kupci zahtevali, da odpremo v varni tujini skladišča, iz katerih bomo potem lahko vsaj tri mesece napajali njihovo proizvodnjo. Z velikimi napori in stroški nam je uspelo to zagotoviti, ampak to je potem naše kupce prepričalo, da smo resni partnerji.

• Torej so si tujci morali misliti, če v pogojih vojne lahko izpolnjujejo svoje obveznosti in proizvodnjo celo povečajo, potem so vsega upoštevanja vredni partnerji.

ŠTEFANIČ: No, morda je res to dodatni psihološki plus, ampak vedeti morate, da smo mi že od prej imeli v tujini renome, kajti naša Iskra je že iz šestdesetih let imela ateste za tuje trge, ker smo bili že v osnovi preveliki za jugoslovanski trg in smo se od vsega začetka orientirali na tuje trge. že dolgo poznamo zahteve zahodnih trgov, kakovost, nizke cene, spoštovanje rokov in poslovno moralo. Zato tudi 90 odstotkov repromaterialov uvozimo, da zadostimo vsem zahtevam tujega trga.

• Kaj pa je z nekdaj hudo razvpitim onesnaževanjem reke Krupe s tako imenovanim PCB iz vaše tovarne?

ŠTEFANIČ: Te strupene snovi smo sanirali že do leta 1985. A v tistem času so vse tovarne kondenzatorjev na svetu uporabljale isto tehnologijo. To je uporaba poliklo-riranih bifenilov kot impregnacijsko olje, ker ima to olje zelo dobre električne in kemične lastnosti. Če te proizvodnje ne bi bilo leta 1960, tudi semiške Iskre ne bi bilo. Z drugačnimi konstrukcijskimi rešitvami kondenzatorjev smo zdaj zamenjali to olje, pri čemer pa moram pripomniti, da v šestdesetih ali sedemdesetih letih ni bilo indikacij o škodljivosti PCB. Ko je svet to ugotovil, so proizvodnjo spremenili, kolikor se je dalo, s svetom pa tudi mi, res da nemara malce pozneje kot drugi.

• Kakšen je danes vaš proizvodni program?

ŠTEFANIČ: Izdelujemo tri velike skupine kondenzatorjev: za elektroniko, torej za najrazličnejše elektronske naprave, za odpravo radio-frekvenčnih motenj, recimo v električnih ročnih orodjih, aparatih za gospodinjstvo itd., in za energetske naprave, kot so naprave za kompenzacijo jalove energije. Naši proizvodi so lahko težki od grama pa do nekaj sto kg, in prav tako jih izdelujemo v serijah od nekaj deset do nekaj milijonov kosov. Sicer pa je tudi program pester: izdelujemo nekaj 10.000 različnih vrst kondenzatorjev. Hkrati ob tem imamo tudi močno proizvodnjo polizdelkov, od metaliziranja folij, izdelave plastičnih in aluminijskih ohišij, konfekcioniranja priključkov, do ogrodij, omar in lakirnice. Omeniti moram tudi to, da v naši tovarni naredimo kar 80 odstotkov opreme, potrebne za lastno proizvodnjo.

• Se te opreme ne da kupiti?

ŠTEFANIČ: Ne, tudi v svetu delajo tako. To je specifična oprema in je pravzaprav nekakšna tehnološka skrivnost. Če je ta oprema že naprodaj, je bodisi zastarela bodisi silno draga. Tako bomo letos samo z doma narejenimi stroji vložili v proizvodnjo okrog tri milijone mark. Sicer pa naša tovarna ponuja tudi storitve pri avtomatizaciji. Letos bomo tako iztržili milijon mark. To je dopolnilni program, ki je naša dolgoročna usmeritev, čeprav vemo, da bodo kondenzatorji še dolgo večinska proizvodnja v naši tovarni. Tudi tu imamo uspehe, saj smo za neko nemško firmo naredili strežne avtomate za neke avtomobilske dele in zdaj ti Nemci želijo podvojiti naročilo. Usmeritev v avtomatizacijo je tudi psihološkega pomena,saj si naši ljudje želijo razvoja prav v to smer in tako moramo balansirati med osnovno dejavnostjo, ki je

morda dolgočasna, in med razvojem avtomatike, ki si jo zaposleni želijo, da zadržimo ustrezne kadre.

- Ali ste takrat, ko je bila kriza, pomislili, da bi morda proizvodnjo polizdelkov prenesli na okoliške obrtniške kooperante, ki bi lahko bili vaši odvečni delavci?

ŠTEFANIČ: Ne, ker nas je bilo predvsem strah, ali bi bili na ta način sposobni hitrih fleksibilnih sprememb programa, razen tega pa mislim, da okolje ni sposobno zadostiti vsem tehnološkim zahtevam teh polizdelkov, saj gre največkrat za izredno natančne izdelke. Smo pa nemara edinstven proizvajalec kondenzatorjev na svetu, ki tako rekoč vse naredi doma.

- Ste torej z vašim sanacijskim programom povsem uspeli?

ŠTEFANIČ: V nekaterih točkah da, druge pa so se zaradi spremenjenih pogojev gospodarjenja spremenile. Recimo, če smo si zastavili desetodstotno zmanjšanje zalog, tega ni bilo več treba storiti pri povečani proizvodnji. No, cilji pa so ostali. Sicer pa je bila v okviru vladnega programa pri nas tudi znana revizijska hiša AT Kearney Inc. iz Združenih držav in njeni izsledki so pokazali, da smo na pravi poti, čeprav se z vsemi njihovimi zahtevami nismo strinjali. Tako so nam svetovali strateškega partnerja v tujini, ki bi za nas prevzel vse trženje. Tega smo se ustrašili, ker bi nazadnje postali od njega povsem odvisni. Predlagali so nam tudi, naj odpustimo 400 delavcev, da bi potem dosegli 40.000 mark letne dodatne vrednosti na zaposlenega. Mi bomo to poskusili s sedanjih 20.000 mark doseči z istim številom zaposlenih in do leta 2.000 doseči celo 60.000 mark letne dodane vrednosti na zaposlenega. Sicer pa delamo z dobičkom. Od leta 1990 nimamo izgube. Imamo sicer nekaj starih dolgov, smo pa nad vodo. Res da zaslužki niso veliki, je pa povprečna mesečna plača okrog 54.600 tolarjev, kar je v skladu s kolektivno pogodbo. In lani smo zaposlili sto novih delavcev. Izvozimo več kot osemdeset odstotkov izdelkov, in to v 34 držav, največ na zahtevne trge Južne Koreje, Nemčije, Tajvana, Hongkonga, Velike Britanije in Italije. V določenih branžah v nekaterih državah izpolnjujemo tudi do 30 odstotkov vseh potreb. Imamo pa težave z medvalutnimi razmerji, z nizko ceno dolarja in visoko ceno tolarja, v obeh primerih glede na marko.

- Katera načela so torej potrebna za uspeh?

ŠTEFANIČ: Imeti morate sposobno ekipo, ki je pripravljena sodelovati.

Članek je v celoti povzet iz revije MANAGER, oktober 1994

PREDSTAVLJAMO PODJETJE Z NASLOVNICE

SICO

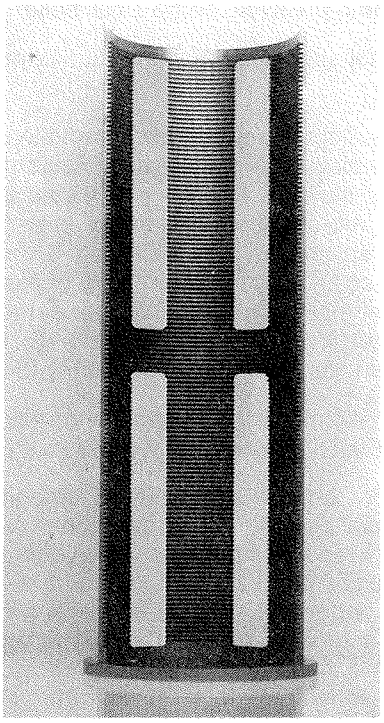
SICO Produktions- und HandelsgesmbH was established in the late eighties by the present president Walter Nadrag and his wife Sissy, in Bad Bleiberg in Austria.

Right from the start SICO specialized in the processing of materials used in the semiconductor industry, especially silicon and quartz glass.

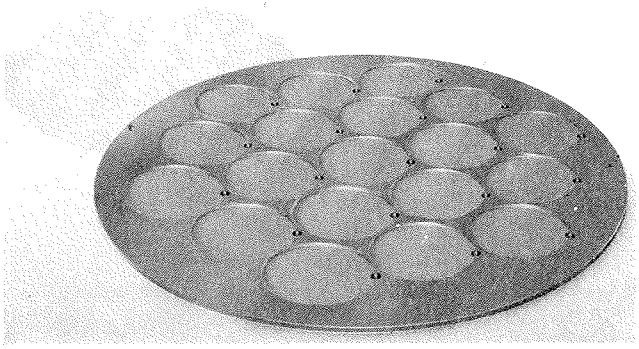
Silicon:

In 1992 SICO acquired a silicon producing company in the USA. The acquisition of this company, which was well known in the branch, enabled SICO not only to process and machine, but also to produce silicon,

SICO's rigid research and development program made great progress in the field of silicon processing. SICO is one of the market leaders in joining of silicon parts. This new, unrivaled technique gave SICO unlimited possibilities in the silicon processing field. Due to this new technique horizontal or vertical silicon boats can be produced **for any wafer dimension (even those for the next generation with 300 mm wafers)**. SICO is also one of the market leaders in pallet production with pallets up to 30 inches.



Picture of 8 inch boat



Picture of pallet 30 inch

Quartz glass:

Since the beginning of 1994 SICO also owns the largest synthetic quartz smelter in Europe, located in Jena, Germany. The quartz smelter, originally part of the Jena Glass Works, has an annual capacity of approx. 25 tons and can cover a quarter of the annual world wide production. Consequently SICO also produces its own quartz; synthetic as well as natural. Our quartz glass is available in the following qualities: synthetic - SP 1, SQ 0, SQ 1 and SQ-Ti natural - BQ 3, BQ 4 and BQ 5. Due to its excellent physical and chemical properties quartz glass is of great importance to modern science and technology. For years quartz glass has proven to be a suitable material especially for the semiconductor and optical industry and light sources production.

With the acquisition of the quartz smelter SICO joined the other market leaders. The reason being our high quality and one of the most chemically purest synthetic quartz glass.

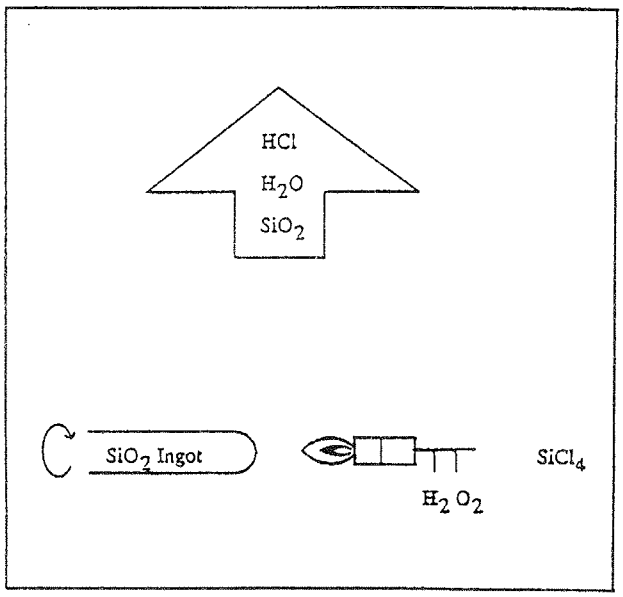
Chemical properties in regard to purity and average trace elements content (ppm):

Al	< 0,05
Na	< 0,10
Ca	< 0,40
Fe	< 0,10
Ti	< 0,08
Cu	< 0,05
Cr	< 0,01
Mn	< 0,01
Pb	< 0,02

Our Strategy

1. OUR AIM - QUALITY, SERVICE, IMMEDIATE DELIVERY

We continuously improve our traditional and high quality range of products.



Synthetic quartz glass production

2. CONSULTATION

None of your demands or wishes will pose a problem for us.

3. THE RESULTS - HIGH - TECH PRODUCTS OF TODAY AND TOMORROW

We want to create a basis that enables long-term cooperation with our customers so that we can sell products of technically high quality on the international market.

4. RESEARCH AND DEVELOPMENT

Our intensive cooperation with our customers can be the basis for permanent improvement and development of our common products. New markets and technological progress offer good prospects in connection with an innovative challenge.

Product range:
As already mentioned, our silicon processing allows us to offer custom made products and all standard products such as: plates, rings, rods,endcaps with and without gas inlets, boats, wafers, carriers, paddles and sleds.

Our well trained and experienced glass blowers and technicians in the quartz glass field can fulfill all customer wishes and offer a broad range of standard products such as: boats, tubes and rods (drawn without tools), plates, round discs, profile rods, substrates, maskblanks and glassblowing products.

Products made of technical sapphire and technical ceramic round off our range of products.

KONFERENCE, POSVETOVANJA, ...

PRVA SVETOVNA KONFERENCA O PRETVORBI SONČNE ENERGIJE V ELEKTRIČNO

Waikoloa, Havaji, 5.-9. december 1994

Naraščajoče zanimanje za izkoriščanje sončne energije v obliki neposredne pretvorbe v električno energijo in želja pa večji povezanosti raziskovalcev po svetu sta botrovala uresničitvi ideje o organizaciji prve svetovne konference z omenjenega področja. Kanferenco so po nekajletnih temeljitih pripravah, kot je večkrat ponovil predsednik konference J. Flood, organizirali ameriški, evropski in azijski Komiteji za sončno energijo. Potekala je od 5. do 9. decembra v kraju Waikoloa na največjem in najjužnejšem otoku v verigi Havajskih otokov.

Poleg znanstvenega programa je bil v sklopu konference organiziran tudi izobraževalni program in izredno bogata konferenčna razstava z več kot sedemdesetimi razstavljalci. Na znanstvenem delu kanference je bilo prisotnih skupno 963 udeležencev, od tega preko 200 iz Japonske in skoraj 280 iz Evrope. Na osmih aplikativnih in tehnoloških področjih(silicijeve celice in materiali, II-VI materiali in strukture, III-V materiali in večspojne celice, amorfni silicij, aplikacije na zemlji, sončne celice za vesolje, sistemi v vesolju in nacionalni programi) je bilo predstavljenih 650 prispevkov, med štiriinosemdesetimi s področja amorfnega silicija tudi dva prispevka sodelavcev Laboratorija za elektronske elemente Fakultete za elektrotehniko v Ljubljani, in sicer: 1. "Internal Opto-Electric Properties of p-i-n a-Si:H Solar Cells on Grooved TCO Texture" avtorjev J. Furlana, S. Amona, P. Popovića in F. Smoleta in 2. "Correlation Between TCO/p and p/i Heterojunction and Effect of n/TCO Heterojunction on a-Si:H Solar Cell Performance" avtorjev F. Smoleta, M. Topiča in J. Furlana.

Na področju silicijevih sončnih celic so raziskave usmerjene k nadaljnji optimalizaciji kontaktov, pasivizaciji površine z nizkotemperaturnimi postopki, zniževanju cene monokristalnih celic z visokim izkoristkom, izboljšanju lstnosti polikristalnega silicija, pasivizaciji defektov v strukturi in na kristalnih mejah z vodikom, in razvoju tankih kristalnih in polikristalnih sončnih celic. Že nekaj let je na področju raziskav silicijevih sončnih celic vodilna raziskovalna skupina prof. Greena na univerzi "New South Wales" v Avstraliji. Predstavili so najvišji izkoristek silicijevih celic doslej, in sicer 24,1%; po njihovih napovedih naj bi dolgoročneje tudi cenene celice za široko uporabo dosegle izkoristek nad 20%, že v nekaj letih pa nad 18%. Pri amorfnem siliciju povzroča še vedno največ težav stabilnost fotoelektričnih lastnosti, še naprej tečejo intenzivne raziskave tehnologij nanašanja enospojnih in tandemskih celic na različne substrate velikih površin, neučinkovite dopirane amorfne plasti se skuša nadamestiti z mikrokristalnimi dopiranimi plastmi, nadaljujejo se raziskave prehodov med posameznimi plastmi, še zlasti p-i prehoda pri enospojnih celicah in n+/p+ tunelskega spoja pri tandemskih celicah. Največji izkoristek celic iz amorfnega silicija 13,2% so dosegli v Centralnem raziskovalnem inštitutu na Japonskem. Japonci so že vsa leta vodilni na raziskavah amorfnega silicija. Med ostalimi tankoplastnimi celicami so raziskave

najobsežnejše na t.i. CIS oz. CIGS ($Cu(In,Ga)(S,Se)_2$) celicah. Usmerjene so predvsem v študij rasti plasti na substratih z različno vsebnostjo natrija, ki zelo pomembno vpliva na električne lastnosti CIS plasti. Pomembno vlogo igra tudi profiliranje prepovedanega pasu v absorberju ($Cu(In,Ga)(S,Se)_2$) in zveznost prehoda med absorberjem in oknom (CdS/ZnO). Na majhnih površinah je bil dosežen največji izkoristek 16%, na večjih površinah pa med 10 in 12%. Na raziskavah teh celic vodi skupina prof. Schock-a na Univerzi v Stutgartu.

Kljub do sedaj največjim dosežkom na področju kristalnih silicijevih sončnih celic, je bilo na konferenci razvidno, da bodo v perspektivi zanesljivo prevladale tankoplastne sončne celice.

Proizvodnja sončnih celic in modulov kot tudi število raznovrstnih aplikacij po vsem svatu vztrajno narašča. Po realističnih napovedih naj bi leta 2008 cena padla pod 3 ameriške dolarje, po bolj optimističnih pa celo pod 2 dolarja na wat maksimalne moči. Brez navajanja dokazov lahko prenesem ugotovitev, da bodo sončne celice v bodočnosti vedno pomembnejši vir električne energije.

Kraj konference zanesljivo ni bil izbran naključno. Ne samo narava in prekrasen ambient, predvsem izredno čisto ozračje je dajalo udeležencem dodatno motivacijo za še bolj delovno vzdušje.

Naslednja svetovna konferenca bo čez štiri leta na Dunaju, vmes pa se bo zvrstila vrsta celinskih konferenc; naslednja evropska bo že oktobra letos v Nici v Franciji.

Na koncu se želim zahvaliti Ministrstvu za znanost in tehnologijo za kritje stroškov potovanja in Laboratoriju za elektronske elemente za plačilo kotizacije in stroškov bivanja.

Dr. Franc Smole, dipl. ing.,
FER/LEE
Tržaška c. 25, Ljubljana

PRIKAZ MAGISTRSKIH DEL IN DOKTORATOV, LETO 1994

MAGISTRSKA DELA

Naslov naloge: **Analiza ravnotežnih stanj celičnih nevronskih mrež**

Avtor: **Iztok Fajfar**, dipl.ing., Ljubljana

Mentor: **prof. dr. Franc Bratkovič**

Univerza v Ljubljani, Fakulteta za elektrotehniko in računalništvo

Celične nevronske mreže (angl. Cellular Neural Networks, CNN) so nov razred analognih sistemov za obdelavo informacij. Zgrajene so iz velikega števila preprostih odsekoma linearnih gradnikov, ki jih imenujemo celice. Celice so razporejene v pravilno mrežo in le lokalno povezane, kar je primerna lastnost za VLSI gradnjo vezja. CNN obdelujejo podatke *paralelno in v realnem* času, rezultat obdelave pa dobimo v *binarni* obliki. Prav zaradi tega je moč CNN preprosto (brez uporabe A/D pretvornikov) povezati z digitalnim računalnikom, s čimer postanejo te mreže zmogljivi predprocesorji pri zahtevnih nalogah, kot je na primer razpoznavanje znakov.

Pri CNN ni obdelava podatkov pravzaprav nič drugega kot prehodni pojav od nekega začetnega stanja (vhodni podatek) do končnega stanja (izhodni podatek), ki je eno izmed stabilnih ravnotežnih stanj mreže. Ko se lotimo načrtovanja CNN, ki naj bi opravljala določeno nalogo, moramo, kot za vsak drug sistem, najprej spoznati njeno dinamično območje stabilnosti, s čimer si zagotovimo, da mreža ne bi zanihala ali postala kaotična. S problemom stabilnosti CNN se ukvarjajo mnogi raziskovalci širom sveta in čeprav je bilo objavljenih že precej uporabnih rezultatov, ostaja to še dokaj odprto področje.

Ko spoznamo v katerih območjih lahko gradimo CNN, smo v resnici šele na začetku poti. Razen za nekatere preproste mreže namreč ne obstajajo analitični postopki, na katere bi se inženir lahko oprl pri gradnji aplikacije, ki si jo je zamislil. Večino dela je zato prepuščena intuiciji ter izčrpnim računalniškim simulacijam.

Eden izmed uporabnih podatkov na poti do končnega izdelka je prav gotovo poznavanje vzorca stabilnih ravnotežnih stanj mreže. Ker so CNN odsekoma linearna vezja, bi ta stanja lahko poiskali preprosto tako, da bi reševali sistem linearnih enačb za vsako kombinacijo segmentov posebej, kar se hitro izkaže za neprimerno zaradi ogromnega števila takšnih kombinacij. Zaradi specifične zgradbe vezja tudi vse druge znane in v splošnem uspešne metode iskanja ravnotežnih stanj odpovedo.

Prav posebnosti zgradbe CNN (homogenost, simetrične nelinearnosti in lokalnost povezav) skupaj z upoštevanjem njihovih dinamičnih lastnosti - namesto samega reševanja sistemov enačb - so nam omogočile razviti metodo, ki učinkovito reši problem. Predlagana metoda iskanja vseh stabilnih ravnotežnih stanj celičnih nevronskih mrež temelji na novem teoremu o dinamiki mreže. Ta teorem nam omogoča, da poiščemo vsa stabilna stanja, ne da bi bilo treba pri tem rešiti en sam sistem linearnih enačb. Sama metoda je zgrajena iz dveh delov. Prvi del je preverjanje lege oglišč n-razsežnostne hiperkocke v prostoru stanj CNN glede na n hiperravnin, pri čemer vsaka celica prispeva svojo hiperravnino. Izmed oglišč, ki ležijo na pravih straneh določenih hiperravnin nato v drugem delu poiščemo s preprostim iskanjem po

binarnem drevesu tista, ki ustrezajo stabilnim ravnotežnim stanjem mreže.

Metodo smo programirali v jeziku C in jo preizkusili na nekaj praktičnih primerih, s čimer smo potrdili naša pričakovanja o njeni uspešnosti.

Naslov naloge: **Metodologija načrtovanja telekomunikacijskih sistemov z jezikom SDL**

Avtor: **Tomaž Hribar**, dipl.ing., Ljubljana

Mentor: **prof. dr. Franc Bratkovič**

Univerza v Ljubljani, Fakulteta za elektrotehniko in računalništvo

Z zelo hitrim razvojem digitalne tehnologije so se zelo hitro povečevale zmogljivosti materialne opreme. Množična uporaba digitalne tehnologije je močno znižala njeno ceno. Načrtovalci in proizvajalci takih sistemov so bili tako soočeni s problemi, katerih kompleksnost in število sta ponekod naraščala eksponencialno.

Tudi področje telekomunikacij pri tem ni bilo izjema. Kriza programske opreme, ki se je prva pojavila v računalništvu, se je pojavila tudi tu. Vzrokov za to krizo je bilo več. Dva izmed osnovnih sta bila slaba kakovost programske opreme in pomanjkanje usposobljenih programerjev. Na področju telekomunikacij je to še toliko bolj očitno, ker ti sistemi delujejo v realnem času. Zaradi tega so se močno povečali tako stroški razvoja kot tudi vzdrževanja sistemov, ki v posameznih primerih lahko dosežejo do 70% celotne cene produkta. Celotna cena produkta vsebuje tako ceno nabave, instalacije in vzdrževanja produkta. Poleg tega se je načrtovanje programske opreme smatralo bolj za umetnost kot pa inženirsko kategorijo, kjer vladajo določena pravila in principi. Ti problemi so postali posebej očitni pri prehodu z 8-bitne na 32-bitno tehnologijo. Večina teh problemov je izvirala iz prepričanja nekaterih, da je možno metode in tehnologijo, ki so jo uporabili na 8-bitnem področju, ustrezno "povečati" na potrebe načrtovanja 32-bitnih sistemov. Vendar je tako razmišljanje zelo podobno tistemu, da lahko nekdo, ki je naredil ducat friziranih mopedov, začne izdelovati dirkalne avtomobile formule 1. Dejstvo je, da majhni projekti zahtevajo le inženirsko delo, medtem ko vodenje velikih projektov zahteva multidisciplinami pristop, ki obsega tako planiranje projektov, ekonomiko, zagotavljanje ustreznih virov, načrtovalske metode in testne metode.

V nadaljevanju naloge se bomo ukvarjali v glavnem samo s principi načrtovanja programske opreme kompleksnih, srednjih in večjih sistemov (to so sistemi, ki obsegajo od 30 000 do 300 000 vrstic C izvorne kode) predvsem na področju telekomunikacij. Rešitev problemov, ki so bili našteti v prejšnjem odstavku, obsega tri področja:

- zaznavanje in odpravljanje napak v zgodnjih fazah življenjskega cikla
- zmanjševanje stroškov in časa vzdrževanja
- omogočanje enostavne komunikacije med kupcem in dobaviteljem.

Osnova temu, da lahko implementiramo zgornje rešitve so dobre specifikacije sistemov. Dobra specifikacija točno določa, kaj sistem mora delati in česa ne. Specifikacije morajo biti razumljive in enoumne, tako da kupec ve, kaj lahko od sistema pričakuje. Enoumne in dovolj formalno napisane specifikacije omogočajo tudi lažji prehod v fazo načrtovanja in zmanjšajo število napak, ki se prenesejo v fazo načrtovanja. S tem se zmanjšajo tako stroški razvoja kot vzdrževanja programske opreme. To je še posebej pomembno na področju telekomunikacij, kjer sistemi delujejo v zelo heterogenem okolju in so zaradi svoje dolge življenjske dobe podvrženi tehnološkim spremembam tako na področju programske kot aparaturne opreme.

Ena od možnih rešitev je uporaba "de facto" mednarodnega standarda za specifikacije in opis sistemov. SDL je tak jezik, ki ga je razvil in standardiziral v svojih priporočilih CCITT. Zaradi njegove relativno dolge in široke uporabe, različni proizvajalci ponujajo CASE orodja, ki olajšajo načrtovanje kompleksnih sistemov s pomočjo SDLa. Kljub temu je uvajanje SDLa v razvojni proces skupaj z uvajanjem ustrezne metode in povezava razvoja kompleksne programske opreme z ostalimi področji razvoja kot so dokumentacija, izobraževanje, testiranje in projektno planiranje kompleksen proces, ki se ga je potrebno pazljivo, premišljeno in sistematično lotiti.

Prvi del naloge obsega kratek opis problemov in razlogov, ki so pogojili nastanek in uvajanje SDLa v načrtovanje telekomunikacijskih sistemov. Opisan je tudi kratek pregled razvoja SDLa po posameznih študijskih obdobjih CCITTja. V drugem poglavju so na kratko predstavljeni osnovni koncepti SDLa (predvsem s stališča njihove uporabe pri načrtovanju sistemov ne pa formalne defnicije). Na koncu poglavja so opisane tudi razlike med SDLom, ki je bil defniran leta 1988 in zadnjo defnicijo SDLa iz leta 1992, ki je precej objektno naravnan. Podrobnejši opis SDLa brez objektnih razširitev se nahaja v /1, 2, 3, 13/. Tretje poglavje na kratko predstavi jezik MSC, ki omogoča dinamični opis odziva sistema. Četrto poglavje obsega opis različnih pristopov k strukturiranju sistemov in primere strukturiranja preprostih sistemov. V petem poglavju so opisani kriteriji za ocenjevanje posameznih metod in podrobneje sta opisani dve metodi: prva strukturirano in druga objektno orientirana. Poleg njiju sta na kratko predstavljeni še dve metodi. V šestem poglavju je opisana uporaba prvih dveh metod v posameznih (predvsem začetnih) fazah življenjskega cikla. V sedmem poglavju sta predstavljeni dve CASE orodji in kriteriji za njihovo izbiro na osnovi določitve lastnosti načrtovanih sistemov, poznavanju lastnosti SDLa in izbrane metode. V osmem poglavju so na kratko opisani vmesniki proti nekaterim področjem, ki so pomembna za uspešno načrtovanje programske opreme in uvajanje SDLa ter multidisciplinarnega pristopa v razvoj programske opreme.

Posamezna poglavja so opremljena s preprostimi in poenostavljenimi primeri, ki prikazujejo praktično uporabo v teh poglavjih opisanih principov.

Naslov naloge: **Modeliranje prehodnih pojavov v večplastnih strukturah iz amorfnega silicija**

Avtor: **Pavle Popović**, dipl.ing., Ljubljana

Mentor: **prof. dr. Jože Furlan**

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Z računalniškim modeliranjem struktur iz amorfnega silicija se v Laboratoriju za elektronske elemente že dolgo ukvarjamo. Marca leta 1989 je docent dr. Franc Smole zagovarjal doktorsko disertacijo z naslovom *Analiza amorfne silicijeve sončne celice z vključitvijo izboljšanega modela lokaliziranih stanj v mobilnostni reži.* V njej je predstavljen program ASPIN za analizo pin struktur iz amorfnega silicija v stacionarnem stanju. Odtlej je program doživel že veliko sprememb, predvsem je bil spet izboljšan model stanj, ki sedaj vključuje spoznanja o tem, da je gostota stanj odvisna od lege Fermijeve energije, razen tega pa je bil izboljšan tudi transportni model, ki sedaj omogoča obravnavo struktur s krajevno spremenljivimi snovnimi parametri.

Poleg tega je marca leta 1993 mag. Elvis Bassanese zagovarjal magistrsko delo z naslovom *Prehodni pojavi v amorfnem siliciju pri svetlobnem vzbujanju.* V tem delu obravnava prehodne pojave nosilcev naboja v homogenih strukturah iz amorfnega silicija. Prehodni pojavi so izračunani s pomočjo računalniškega programa. Kjer je bilo to mogoče, so s pomočjo dopustnih poenostavitev izpeljani tudi poenostavljeni analitični izrazi.

Z željo, da bi v enotni analizi zajela tako vplive krajevnih odvisnosti kot tudi vplive časovnih sprememb, sva z Elvisom Bassanesejem začela pisati nov računalniški program. Sistem enačb, ki vsebuje odvode tako po kraju kot po času, je za reševanje dosti bolj težaven kot sistema, ki ju iz njega dobimo tako, da postavimo odvode na kraj ali pa odvode na čas enake nič. Tega sva se zavedala že od vsega začetka, zato sva pri svojem delu neprestano iskala stikov z ostalimi sodelavci Laboratorija za elektronske elemente.

Program sva želela pisati v programskem jeziku C, ki je postal izjemno popularen za programiranje tako na osebnih kot tudi na večjih računalnikih, kjer so ga razvili. Zato nisva mogla enostavno začeti z nadgrajevanjem programa ASPIN, ki je napisan v Fortranu. Zato pa sva se pri razvoju najinega programa opirala na izkušnje in znanje doc. dr. Franca Smoleta. Pri iskanju krajevne diskretizacije nama tako ni bilo treba orati ledine, kot sva to morala početi pri časovni diskretizaciji.

Program, ki sva ga napisala, je predstavljen v pričujočem magistrskem delu. Program omogoča analizo prehodnih pojavov v večplastnih strukturah iz amorfnega silicija. Možna je samo analiza struktur, v katerih je ena dimenzija dosti krajša od drugih dveh, tako da lahko krajevne odvisnosti vzdolž drugih dveh dimenzij zanemarimo. Vzdolž tiste dimenzije, po kateri računamo, pa se lahko spreminjajo takorekoč vsi parametri, ki smo jih vključili v analizo.

Program smo preizkusili na različnih strukturah in z različnimi primeri vzbujanj. Izkazalo se je, da je napisani program primerno orodje za analizo prehodnih pojavov v večplastnih strukturah iz amorfnega silicija. Pri polnem upoštevanju odvisnosti od kraja izračuna prehodni pojav od začetka do vzpostavitve stacionarnega stanja, pri čemer je razpon na časovni osi lahko večji od deset dekad. Dva zgleda sta podana v petem poglavju.

V tem delu je numerična analiza prehodnih pojavov v amorfnem siliciju predstavljena širše. Nismo želeli našega programa samo opisati, ampak smo podali tudi teoretične temelje za reševanje sorodnih problemov. Zato smo začeli bolj splošno, kot je pri analizi polprevodniških elementov v navadi, z osnovnimi enačbami za analizo elektromagnetnih pojavov v materialih. V drugem poglavju smo te enačbe najprej poenostavili za analizo polprevodniških elementov na splošno, nato pa smo z uvedbo modelov za prostorsko gostoto naboja in transport nosilcev enačbe prilagodili za analizo amorfnega silicija. Obdelali smo tudi različne možnosti za formulacijo robnih pogojev, ki se uporabljajo v analizi polprevodniških elementov.

V tretjem poglavju smo obravnavali diskretizacijo dobljenega sistema parcialnih diferencialnih enačb. Obravnavali smo samo diferenčne metode. Obdelali smo krajevno in časovno diskretizacijo tako za sistem enačb kot za robne pogoje. Opisali smo vzroke, zaradi katerih je pri izboru obeh diskretizacij pri analizi polprevodniških elementov potrebna še posebna previdnost.

V četrtem poglavju smo obdelali metode za reševanje sistema algebraičnih enačb, ki ga dobimo po diskretizaciji sistema parcialnih diferencialnih enačb. Za metodo, ki smo jo uporabili v programu, smo podali tudi končne enačbe. Njihovi zapisi so dolgi in morda nekoliko nepregledni, vendar program računa prav po teh enačbah. Za odpravljanje težav so bistvenega pomena. V tem poglavju smo povedali tudi nekaj o izboru začetnih približkov pri iterativnem reševanju in o kriterijih za prenehanje iterativnega postopka.

V petem poglavju smo obravnavali dva zgleda izračunanih prehodnih pojavov. Izbrali smo vklop osvetlitve v pin strukturi in vklop napetosti v nin strukturi. Pri obeh zgledih smo poleg rezultatov izračuna podali tudi fizikalno sliko dogajanja med prehodnim pojavom.

V celotnem delu smo se držali ISO standardov (International Standardisation Organisation), priporočil Mednarodne elektrotehnične komisije (IEC - International Electrotechnical Commission) in SI sistema enot. Pomen uporabljenih oznak in simbolov je opisan tudi v Seznamu simbolov.

Enačbe smo številčili v vsakem poglavju od začetka. Na enačbe iz istega poglavja se sklicujemo z navedbo številke enačbe, na primer enačba (20), na enačbe iz drugih poglavij pa z navedbo števila, ki pomeni poglavje, ki mu za piko sledi številka enačbe, na primer enačba (3.15).

Naslov naloge: **BiCMOS tehnologija za izdelavo telekomunikacijskih integriranih vezij**

Avtor: **Iztok Šorli**, dipl.ing., Ljubljana

Mentor: **prof. dr. Lojze Trontelj**

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Telekomunikacije in mikroelektronika sta primer tesno povezanih "high - tech" panog, ki sta ena drugi vzpodbuda in gonilo. Tehnologija telekomunikacij, sprva popolnoma analogna, je doživela v prejšnjem in zlasti v tem desetletju transformacijo v analogno-digitalno tehnologijo.

Tudi mikroelektronika, ki je svoji dve glavni veji, bipolarno in MOS tehnologijo, pripeljala skoraj do popolnosti, se je spreminjala in sledila zahtevam posameznih področij telekomunikacij. Nastala je nova generacija mikroelektronske tehnologije, BiCMOS, ki zna elegantno integrirati veliko večino analogno-digitalnih funkcij, potrebnih telekomunikacijski tehnologiji.

Majhna poraba, velika hitrost, velik napetostni obseg delovanja, možnost realizacije fleksibilnih vhodno-izhodnih funkcij, visoka stopnja integracije, so le nekatere prednosti BiCMOS tehnologije pred predhodnicami.

Uvodni del magistrskega dela sem posvetil opisu zahtev, ki jim morajo zadostiti moderna telekomunikacijska integrirana vezja. Sledi opis delovanja gradnikov telekomunikacijskih integriranih vezij.

V tretjem poglavju obravnavam trojnodifundirano BiCMOS tehnologijo. Kot osnovo sem vzel CMOS tehnologijo, katera nam že nudi NMOS, PMOS ter lateralne pnp in vertikalne pnp substratne bipolarne tranzistorje. Z dodatkom nekaj fotolitografskih in visokotemperaturnih korakov ter ionskih implantacij izdelamo dodatne vertikalne izolirane npn in pnp bipolarne tranzistorje, poli1/poli2 kondenzatorje in polisilicijeve upore z visoko vrednostjo plastne upornosti.

Električne lastnosti naštetih osnovnih in dodanih integriranih gradnikov sem podrobneje prikazal v četrtem poglavju, medtem ko je peto poglavje posvečeno predvsem primerjavi MOS in bipolarnega tranzistorja s poudarkom na sinergiji njunih dobrih lastnosti pri načrtovanju analogno-digitalnih funkcij.

V zadnjem poglavju sem opisal pomen ujemanja dimenzijskih in električnih parametrov aktivnih in pasivnih integriranih gradnikov za analogno-digitalno načrtovanje.

Naslov naloge: **Modeliranje heterospojne PIN a-Si:H sončne celice**

Avtor: **Marko Topič**, dipl.ing., Ljubljana

Mentor: **prof. dr.Jože Furlan**

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V zadnjih 20-tih letih je na področju polprevodniških tehnologij vedno več zanimanja za amorfni silicij, še zlasti po občutnem izboljšanju električnih lastnosti, ki je bilo doseženo z vgradnjo atomarnega vodika v amorfni silicij (a-Si:H) med procesom nanašanja Si iz RF vzbujene plazme silana (SiH_4) na substrat. Atomarni vodik se veže na pretrgane (t.i. bingljajoče) vezi, ki jih je v amorfni strukturi zelo veliko, in s tem zmanjšuje koncentracijo defektov v a-Si:H. Koncentracija vodika običajno dosega 10 at.% koncentracije Si atomov.

Že sredi 70-tih let je bilo uspešno izvedeno dopiranje a-Si:H /1/ in s tem omogočeno izkoriščanje a-Si:H za različne tehnične aplikacije. Dandanes se polprevodniški elementi iz a-Si:H uporabljajo v fotokopirni tehniki, pri krmiljenju tekočih kristalov in CCD-jev (Charge Coupled Devices) velikih površin (uporaba tankoplastnih tranzistorjev TFT - Thin Film Transistors), na področju senzorjev X žarkov (uporaba senzorjev velikih površin) in kot najbolj obetajoče področje za a-Si:H, za tankoplastne sončne celice.

Odločilna prednost tega polprevodniškega materiala je, da je proces pridobivanja a-Si:H v primerjavi s pridobivanjem monokristalnih polprevodniških materialov zelo poceni, saj se nanaša iz plinastega stanja pri nizkih temperaturah (373 K - 650 K). Poleg tega se lahko nanaša na velike površine različnih geometrij (>1 m^2).

Fizikalne lastnosti, ki odlikujejo a-Si:H za uporabo pri sončnih celicah, so sledeče: zelo močna absorpcija v vidnem spektru svetlobe (10- do 20-krat večja v primerjavi z monokristalnim Si), visoka fotoprevodnost, nizka temna prevodnost, širok razpon optične reže (1 eV < E_{opt} < 3.6 eV, dosežena s pomočjo dodajanja Ge oz. C), možnost kreiranja heterospojev z nizko koncentracijo defektnih stanj na spoju in dobra mehanska trdnost.

Tehnološke prednosti, ki odlikujejo a-Si:H pri sončnih celicah, pa so: možnost nanašanja na velike površine različnih geometrij (s pomočjo plazemske CVD, ECR CVD, PE CVD...), nizka temperatura depozicije (373 K < Ts < 650 K), preprosta kontrola dopiranja preko kontrole pretoka dopirnih plinov, možnost nanašanja na cenene substrate (steklo, nerjaveča kovina, plastika), preprosta uporaba integrirnih tehnologij (heterospoji, tandemske celice), dobra ponovljivost...

Od prve sončne celice iz a-Si:H se je izkoristek z 1% dvignil močno proti teoretičnim mejam (15%), trenutni rekord izkoristka za enojno pin celico znaša 13.1% /2/. Optimizacija v najširšem smislu pomeni zmanjšanje cene na proizvedeni wat moči (cost per peak Watt), ki še vedno ni padla na nivo cene konvencionalnih virov. Optimizacija na nivoju izboljšave kvalitete sestavnih materialov sončne celice, optimizacija na nivoju enojne celice ali tandemske celice, optimizacija prehodov med različno dopiranimi plastmi, optimizacija kontaktnih spojev, optimizacija oz. zmanjšanje negativnih efektov, kot je npr. Staebler-Wronski efekt, so predmet številnih raziskav v tehnologiji izdelave a-Si:H sončnih celic ob podpori računalniških simulacij. V tekmi za čim večjim izkoristkom se vloga računalniškega modeliranja lastnosti a-Si:H in delovanja a-Si:H sončnih celic povečuje in lahko rečemo, da je računalniško modeliranje že postalo enako pomembno kot sama tehnologija.

Kljub intenzivnim teoretičnim in eksperimentalnim raziskavam z množico merilnih metod enoumno določena porazdelitev lokaliziranih stanj v a-Si:H še vedno ne obstaja. Ker pri večini analiz model stanj (DOS - Density of States) nastopa kot osnovni parameter, ki igra pri

realnosti rezultatov odločilno vlogo, bomo skušali v predloženem delu najprej podati izboljšani model stanj, ki smo ga uvedli v naš računalniški simulator ASPIN. Model stanj naj bi se čim bolj skladal tako z zanesljivimi eksperimentalnimi rezultati kot tudi z utemeljenimi teoretičnimi predvidevanji. Zato bo v 2. poglavju opisana narava in tvorba defektov v a-Si:H s termodinamskim pristopom, kot rezultat pa bo predstavljen "defect pool" model porazdelitve gostote defektnih stanj. Prikazana bo prilagoditev "defect pool" modela v računalniški simulator pin a-Si:H sončne celice. Podani bodo rezultati analize, kako "defect pool" model vpliva na lastnosti sončne celice v primerjavi s klasičnim pristopom porazdelitve gostote defektnih stanj. Dotaknili se bomo odprtih vprašanj v zvezi z "defect pool" modelom in na njih poskušali odgovoriti.

V 3. poglavju bodo izpeljane enačbe za modeliranje polprevodniških struktur s krajevno spremenljivimi snovnimi parametri, ki bodo v nadaljevanju prirejene za modeliranje enodimenzionalnih a-Si:H heterostruktur v stacionarnem stanju.

V 4. poglavju se bomo osredotočili na analizo heterospoja med prevodnim transparentnim oksidom (TCO - Transparent Conductive Oxide) in a-Si:H. Obravnavali bomo TCO/p(a-Si:C:H) heterospoj in TCO/n(a-Si:H) heterospoj za različne vrste TCO-jev. Podana bo analiza vpliva razlike izstopnih del in gostote defektnih stanj na spoju na notranje lastnosti in njihov vpliv na zunanje karakteristike steklo/TCO/p(a-Si:C:H)-i(a-Si:H)-n(a-Si:H)/TCO/kovina sončne celice.

Detajlne vidike magistrske naloge opisujejo sledeči prispevki z mednarodnih konferenc, ki se nahajajo v prilogi:

F. Smole, M. Topič, J. Furlan: *"Amorphous silicon solar cell computer model incorporating the effect of TCO/a-Si:* C:H *junction"*, Special Issue of Solar Energy Materials and Solar Cells, Elsevier Science Publisher, Amsterdam, v tisku (1993).

F. Smole, M. Topič: *"Effects of TCO/a-Si:* C:H *interface defect states* on p-i-n a-Si:H *solar cell performance"*, Material Research Society Symposium Proceedings, San Francisco, v tisku (1994).

F. Smole, M. Topič, J. Furlan: *"The influence of various defect states in TCO/a-Si:C:H interface on p-i-n a-Si:H solar cell performance"*, Proceeding of 12^{th} European Photovoltaic Science and Engineering Conference, Amsterdam, v tisku (1994).

V pričujočem delu sem za spremenljivke (ki jih ob prvem navajanju razložim, sicer pa so tudi navedene v Seznamu simbolov) uporabljal čim bolj standardne oznake. Kratice nekaterih angleških strokovnih izrazov so razložene ob prvi uporabi in v Seznamu kratic. Nekaterih strokovnih angleških izrazov nisem prevajal, saj slovenski jezik še nima udomačenih nadomestnih izrazov ali pa so preveč okorni. Zato so angleši izrazi navedeni v dvojnih narekovajih ("Total Yield" metoda) in so tudi v slovenskem strokovnem okolju tako poimenovani.

Naslov naloge: **Silicijevi detektorji ionizacije**

Avtor: **Danilo Vrtačnik**, dipl.ing., Ljubljana

Mentor: **prof. dr. Slavko Amon**

Univerza v Ljubljani, Fakulteta za elektrotehniko in računalništvo

Polprevodniški detektorji so se uporabljali v jedrski fiziki za energijske meritve že v začetku 60-tih let in v visokoenergijski fiziki (fiziki trdih delcev) približno deset let kasneje. Z razvojem planarne tehnologije so se odprle možnosti, da poleg energije vpadnega delca določimo tudi njegovo pozicijo.

V osnovi ločimo dva tipa detektorjev, ki uporabljata različni metodi, da dobimo prostorsko informacijo. Prvi uporablja zvezno odčitavanje z uporovno delitvijo naboja, drugi pa uporablja diskretno polje elementov (stripe). Prav silicijevi mikrostrip detektorji, izdelani v planarni tehnologiji, so postali najpogosteje uporabljeni elementi za eksperimente v visokoenergijski fiziki. Uporabljajo se kot aktivne tarče, kot detektorji za določitev žariščne točke ("vertex" detektorji), ali pa zgolj za prožen je dogodkov. "Vertex" detektor je običajno sestavljen iz več plasti mikrostrip detektorjev in se danes najpogosteje uporablja v t. i. "colliding beams experiments" (v eksperimentih, kjer trčita dva nabojno si nasprotna delca).

V 1. poglavju bodo opisane nekatere osnovne lastnosti polprevodniških materialov s poudarkom na polprevodniškem spoju. Povzeti in delno izpeljani bodo izrazi, ki bodo omogočili načrtovati in električno opisati detektor.

V 2. poglavju bodo proučena osnovna fizikalna dogajanja pri vpadu visokoenergijskega delca v snov in proučeni bodo najrazličnejši notranji in zunanji parametri, ki skupaj z elektroniko določajo lastnosti polprevodniškemu detektorju.

V 3. poglavju se bomo osredotočili na strukture najpogosteje uporabljenih pozicijsko občutljivih detektorjev, z natančnejšo proučitvijo obstoječih strukturnih in tehnoloških rešitev, ki bi bile primerne za naše razmere.

Na osnovi predhodnih študij in s pomočjo simulacijskih orodij bo v 4. poglavju načrtovana struktura in načrtani tehnološki postopki za izdelavo silicijevega mikrostrip detektorja. Element, ki smo ga poimenovali "ministrip" detektor, naj bi načrtovali v sodelovanju z Odsekom za eksperimentalno fiziko osnovnih delcev Inštituta "Jožef Stefan" za raziskovalno skupino CMS (Compact Muon Spectrometer) pri trkalniku LHC (Large Hadron Collider) iz CERN-a, Ženeva. Detektor naj bi se uporabljal znotraj eletromagnetnega (EM) kalorimetra za natančno določanje pozicije začetka EM plazu.

Naslov naloge: **Kompaktna mikrovalovna cev**

Avtor: **Andrej Pregelj**, dipl.ing.str., Ljubljana

Mentor: **red. prof. dr. Alojz Paulin**

Komentor: **red. prof. dr. Vitodrag Kumperščak**

Univerza v Mariboru, Tehniška fakulteta

Ideja je naslednja: stoječe elektromagnetno valovanje v mikrovalovnem votlem resonatorju lahko povzročimo in vzdržujemo tudi s pulzirajočim elektronskim curkom, ki prehaja skozenj. Pri tem se energija curka bolj ali manj zmanjša; iz stopnje oslabitve lahko določimo faktor kvalitete resonatorja Q. Pri določeni frekvenci pulzov je Q odvisen predvsem od oblike in velikosti votline. Predvidevamo, da bodo resonatorji popolnoma iste oblike imeli različen Q, ki bo odvisen samo od različnih materialov. V primeru uporabe superprevodnih (SP) resonatorjev bi se torej lahko iz različnih Q v odvisnosti od temperature dalo sklepati na njihove lastnosti pri visokih frekvencah, za kar je po našem poznavanju še zelo malo podatkov v literaturi.

Magistrsko delo podaja predlog konstrukcije za napravo, ki bi omogočala eksperimentiranje na zgoraj omenjeni način z mikrovalovnimi resonatorji iz različnih, tudi SP, materialov. Pri tem se srečamo z reševanjem več zahtevnih nalog:

- izbira frekvence (3 GHz) in njej ustrezne velikosti resonatorja,
- ohlajanje sedeža izmenljivih resonatorjev na zelo nizke temperature (okoli 4 K) za zagotavljanje pojava SP lastnosti,
- ustvarjanje vakuumskega okolja ($p < 10^{-5}$ mbar) za toplotno izolacijo in za omogočanje gibanja elektronov,
- študij možnosti izdelave resonatorjev iz klasičnih in iz visokotemperaturnih SP materialov.

DOKTORSKE DISERTACIJE

Naslov doktorske disertacije: **Razširitev simulacijskega modela unipolarnih tranzistorjev**

Avtor: mag. **Roman Opara**, dipl.ing., Ljubljana

Mentor: **prof. dr. Janez Trontelj**

Univerza v Ljubljani, Fakulteta za elektrotehniko in računalništvo

V prvem poglavju, z naslovom Spektralna analiza, podajamo kratek povzetek neparametrične analize digitalno vzorčenih signalov. Govorimo o običajnih orodjih in metodah pri spektralni analizi, s poudarkom na analizi naključnih signalov. Glede na naravo naključnih procesov so smiselne le statistične vrednosti, ki jih dobimo z metodo povprečenja spektra moči. Zaradi omejene dolžine vhodnega zaporedja vzorcev pri nizkofrekvenčnih meritvah nastane problem izgubljanja in ločljivosti spektra moči.

V okviru drugega poglavja dela Optimizacija analize signalov podajamo kriterij določanja dolžine vhodnega zaporedja vzorcev, selektivne meritve signalov in nivo šuma v vezjih. Zaradi lastnosti digitalno vzorčenih signalov smo za kvantitativno oceno določili uteži, pri tem pa izločili vpliv vzorčenja. Neparametrične analize signalov po osnovi Fourierjeve transformacije razširjamo na parametrično modeliranje naključnih procesov. Na podlagi nizkega števila vzorcev in časovne omejenosti analize z modelom AR naključnih procesov določamo kvaliteten spekter moči šuma v električnih vezjih.

V tretjem poglavju delo obravnava izvore in lastnosti šuma v električnih vezjih in gradnikih. Z analitičnim pristopom ter na podlagi meritev predstavljamo šumno karakteristiko splošnega električnega sistema. Glede na lastnosti šumnih izvorov identificiramo kritične parametre šumne karakteristike. S podrobno analizo diferencialnih struktur in Hallovega senzorja smo zgradili razširjene električne in šumne modele, primerne za simulacije.

Običajni simulacijski pristopi nam ne omogočajo simulacije ujemanja tranzistorja MOS, zato v četrtem poglavju dela razširjamo model le-tega, in sicer identificiramo kritične parametre ujemanja glede na dimenzije, orientacijo, oddaljenost parnih elementov ter delovne točke. Za verifikacijo identificiranih parametrov smo iz-delali testno strukturo v tehnologiji CMOS. Zgrajeni raz-širjeni model MOS optimizira časovni obseg simulacije in minimizira konvergenčne probleme pri simulacijah.

Naslov doktorske disertacije: **Precizno merjenje moči in energije z merilniki na osnovi Hallovega elementa**

Avtor: mag. **Miro Rozman**, dipl.ing., Ljubljana

Mentor: **prof. dr. Anton Jeglič**

Univerza v Ljubljani, Fakulteta za elektrotehniko in računalništvo

Primernost uporabe Hallovega elementa v preciznih merilnih sistemih za merjenje moči in energije je bila raziskana s pomočjo računalniške simulacije modela Hallovega elementa. Model je direktno prilagojen programskemu paketu za simulacijo elektronskih vezij SPICE, kar omogača analizo delovanja senzorja skupaj s spremljajočim vezjem. Tak pristop zagotavlja, da z analizo poleg dogajanja v Hallovem elementu in elektronskem vezju upoštevamo tudi medsebojni vpliv med obema.

Motilni vplivi, ki spremljajo Hallov pojav, v veliki meri otežkočajo enostavno uporabo, zato je pri zahtevnih sistemih potrebno vgraditi sistemske metode za zmanjšanje neželjenih pojavov. Za uspešno izvedbo te naloge so stranski pojavi vključeni v model, ki omogoča načrtovanje elektronskega vezja za izločitev stranskih vplivov s pomočjo simulacije. Simulacija celotnega sistema znatno olajša in poenostavi celoten postopek. Najvplivnejši stranski pojavi so: temperaturna odvisnost, preostala napetost, šum, nelinearnost upornosti, nelinearnost galvanskomagnetne pretvorbe in odvisnost upornosti aktivne plasti od magnetnega polja.

S pomočjo simulacije modela so bile razvite sistemske metode za izločitev preostalih napetosti, temperaturne kompenzacije, linearizacijo galvanskomagnetne pretvorbe in zadušitev raztrosa merilnih rezultatov. Učinkovitost teh metod je zagotovljena z združitvijo celotnega merilnega sistema v enem integriranem vezju. Tako je zagotovljena dobra povezava med Hallovim elementom in kompenzacijskimi elementi.

Veljavnost modela je potrjena z razvojem univerzalnega merilnika električne moči in energije, uporabnega za merjenje enosmernih in izmeničnih veličin. Pomen merilnika v metrološkem smislu je v tem, da pokriva široko frekvenčno področje pri visokih jakostih toka z enim samim merilnim območjem.

Ker statični števec porabe električne energije ni tako zanesljiv kot kiasični v mehanski izvedbi, je bil merilnik dopolnjen s sistemom za samopreverjanje pravilnosti delovanja med obratovanjem, kar omogoča hitro registracijo napake v sistemu. Na ta način se v veliki meri poveča zanesljivost merjenja v merilni mreži z velikim številom števcev v omrežju.

Z namenom, da se izkoristi nove tehnološke možnosti, je bil razvit izviren sistem preciznega merilnika moči in energije na osnovi Hallovega elementa s sistemom za samonastavitev prenosne funkcije. V sistemu so upoštevana vsa spoznanja zajeta v disertaciji in vključena v merilno elektroniko, prirejeno za izvedbo v tehnologiji analogno-digitalnih vezij z visoko stopnjo integracije.

Naslov doktorske disertacije: **Metodologija sinteze strukturirane električne topologije iz geometrijske podatkovne baze integriranega vezja**

Avtor: **mag. Janez Trontelj**, dipl.ing., Ljubljana

Mentor: **prof. dr. Dušan Raič**

Univerza v Ljubljani, Fakulteta za elektrotehniko in računalništvo

Izdelava integriranih vezij po naročilu (angl. full custom IC design) je še vedno zelo zamudno opravilo. Torej je potrebno razširiti nabor računalniških orodij, ki bi ta postopek poenostavila. Avtomatska sinteza strukturirane električne topologije iz razmestitve elementov za integrirano vezje (angl. layout) pomeni pomemben korak k avtomatizaciji postopka načrtovanja integriranih vezij. S pomočjo obratne poti lažje odkrijemo napake in parazitne pojave, ki smo jih nehote vnesli med načrtovanjem celic integriranega vezja. To je koristno zlasti pri načrtovanju kombiniranih, analogno-digitalnih integriranih vezij.

Znano je, da za risanje uporabnih električnih shem potrebujemo določeno spretnost, s katero pregledno nakažemo medsebojno odvisnost električnih simbolov. Z gledišča kombinatorike ta problem ni rešljiv v polinomskem času, vendar ga je mogoče zadovoljivo rešiti s pomočjo na novo razvitih postopkov, ki so predstavljeni v tem delu. Pri razvoju le teh, smo se naslonili na teorijo grafov, določene probleme pa je bilo potrebno reševati hevristično.

Razvili smo algoritme, s pomočjo katerih lahko avtomatsko izdelamo nehierarhično ali pa hierarhično električno shemo, ki se stilno v veliki meri približa ročno narisanim shemam. Kot podatkovna osnova nam torej služi razmestitev elementov za integrirano vezje, ki je podana v obliki standardnega opisnega jezika. Ta vsebuje opis fizikalnih lastnosti elementov ter podatke o njihovi medsebojni povezanosti brez kakršnih koli topoloških informacij. Na avtomatsko narisani električni shemi lahko prikažemo lastnosti elementov, kot sta na primer širina in dolžina kanala tranzistorja. Možno pa je tudi grafično prikazati parazitne upornosti in kapacitivnosti glede na vnaprej izbran prag.

Algoritme ter njihov opis smo razdelili na tri večje skupine. Te skupine sestavljajo algoritmi za hierarhično grupiranje simbolov, algoritmi za urejevanje in postavitev električnih simbolov na shemo ter algoritmi za povezovanje električnih simbolov. Vsi skupaj tvorijo povsem nov pristop k reševanju problema avtomatske sinteze električnih shem.

Naslov doktorske disertacije: **Oscilatorska diferencialna senzorska struktura**

Avtor: **mag. Vojko Matko**, dipl.inž.el.,

Mentor: **red. prof. dr. Dali Đonlagić**

Komentor: **doc. dr. Jože Koprivnikar**

Univerza v Mariboru, Tehniška fakulteta

V predlaganem delu je opisan poizkus uporabe diferencialne oscilatorske senzorske strukture v kapacitivnem senzorju. Raziskave so bile usmerjene v simulacijo, konstruiranje in analizo delovanja oscilatorske diferencialne strukture v kateri oscilatorja nihata zelo blizu skupaj ter v analizo uporabnosti kapacitivno odvisnih kristalov. Prav tako je analiziran pristop vzbujanja celotnega senzorja z naključnimi testnimi signali s korelacijsko dekonvolucijsko metodo, ki ima ob specialno izbranem testnem signalu ime tudi direktna digitalna metoda (DDM). Opisan je pristop kompenzacije temperaturnih in napetostnih vplivov; kakor tudi šumnih motilnih signalov. Prikazano je območje delovanja in ocena negotovosti senzorja brez in s testnim signalom.

Pri izvedbi kapacitivnega senzorja, za območje kapacitivnih sprememb pod 1 pF je prisoten problem izvora stabilnega nihanja, kompenzacije temperature, vpliva napajalne napetosti, šuma, A/D in D/A pretvorbe. Predlagana je rešitev s pulznoširinskim modulom, ki oblikuje pulznoširinsko modulirane tokovne impulze visoke frekvence. S temi impulzi polnimo in praznimo kondenzator v integrirnem členu. Pri kondenzatorju izkoristimo lastnost, da njegova napetost linearno narašča, če ga polnimo s konstantnim tokom. Ker vplivajo na polnjenje samo tokovni impulzi, ki razpolagajo z ustreznim tokom, šumni motilni signali ne vplivajo na polnjenje kondenzatorja. Prav tako pulznoširinski modul kompenzira temperaturni in napetostni vpliv preko modulacije. Korelacijska določitev izhodne merilne vrednosti zmanjša vplive kot so: vpliv A/D in D/A pretvorbe, "drift", "offset", šum, netočnosti toleranc elementov ter histerezo. Korelacijsko določanje merilne vrednosti je pomembno predvsem za določanje začetnih in končnih vrednosti. Ob ustrezni programski podpori sta predlagana dva načina delovanja (dinamično spremljanje meritev in korelacijsko določanje razlik).

23rd INTERNATIONAL CONFERENCE ON MICROELECTRONICS, MIEL'95
31st SYMPOSIUM ON DEVICES AND MATERIALS, SD'95
September 27.-29.1995, Terme ČATEŽ, SLOVENIA

Announcement and Call for Paper

ORGANIZER
MIDEM - Society for Microelectronics, Electronic Components and Materials,
Dunajska 10, 61000 Ljubljana, Slovenia

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GENERAL INFORMATION
MIEL-SD'95 is an international conference organized by MIDEM uniting two meetings with long tradition: 23rd International Conference on Microelectronics and 31st Symposium on Devices and Materials.

Both conferences are well known through the distinguished guest speakers. Several hundred scientists from all over the world took part in the MIEL-SD conference in the past. The goal of connection and building of friendship among the scientists and their companies remains the keystone of the organizer.

The conference will be held in **TERME ČATEŽ, Slovenia**, a picturesque tourist resort, **SEPTEMBER 27.-29.1995.**

ORIGINAL PAPERS IN THE FOLLOWING AREAS ARE SOLICITED:
- Novel monolithic and hybrid circuit processing techniques
- New device and circuit design
- Process and device modeling
- Semiconductor physics
- New electronic materials and applications
- Electronic materials science and technology
- Optoelectronics
- Photovoltaic devices
- Reliability and failure analysis
- Microelectronics education

Presentation of companies and laboratories working in the field of microelectronics and materials will be held after afternoon sessions.

INVITED PAPERS:
The following speakers will present introductory review papers before sessions:

1. Wolfgang PRYBIL, SIEMENS EZM, Villach, Austria:
   "Integrated Smart Power Circuits - Introduction, Design and Application"
2. Mark PLEŠKO, J. STEFAN INSTITUTE, Ljubljana, Slovenia:
   "The New Synchrotron Light Sources - Powerful Tools for Research and Production"
3. Gerhard HERZOG, TECHNISCHE UNIVERSITÄT, Graz, Austria:
   "Space Charges in Material Science"
4. Wilhelm KUSIAN*, J. Furlan, G. Conte, *SIEMENS AG Corporate R&D, München, Germany:
   "The pin/TCO/nip Solar Module"
5. Nihal SINNADURAI, MIDDLESEX UNIVERSITY, England:
   "Precision Thermal Profiling of Microelectronics Using Liquid Crystals"
6. Walter SMETANA, TECHNISCHE UNIVERSITÄT, Wien, Austria:
   "Aspects of Realization of Buried Capacitors in Thick Film Multilayer Circuits"

PREPARATION OF SUMMARY AND ABSTRACTS
A summary not longer than 60 lines in required for review. This summary must state clearly what new result have been obtained and what techniques have been used.

RECEIPT DEADLINE:
Deadline for receiving the summaries is **May 15th, 1995.**

PREPARATION OF THE PAPERS
The papers have to be prepared on maximum 6 **pages A4 format**, ready for reproduction in the Proceedings. Invited papers are not limited to 6 pages.

Further detailed information will be given to the authors of accepted papers by **June 1st**.

RECEIPT DEADLINE
Deadline for the manuscript of the paper is **September 1st**.

CONFERENCE PROCEEDINGS
Invited paper and accepted papers will be published in the conference proceedings distributed at the conference registration.

LANGUAGE
Official conference language is English.

REGISTRATION
The registration fee is US$ 300. Employees of the MIDEM Society sponsors have 20% discount, while MIDEM members have 30% discount. The fee includes Conference Proceedings and free access to all Conference events, including welcome cocktail party on September 27th and the Conference dinner on September 28th.

IMPORTANT DATES
Summary deadline: **May 15th**
Notification of acceptance: **June 1st**
Advanced Program: **August 1st**
Paper deadline: **September 1st**
Final conference program: at registration, **September 27th**

ACCOMMODATION
Hotel accommodation will be arranged at the conference site in hotel TERME. All details will be given in second announcement.
The conference site is about 100 km away from Ljubljana along the main road towards Zagreb, Croatia. The best way to reach Terme Čatež is to fly to Ljubljana airport and the to continue by car.

Program and organizing committee:
MIDEM, Dunajska 10, 61000 Ljubljana, SLOVENIA
Tel.: +386-61-312 898, fax: +386-61-319170
Mrs. Meta Limpel, M.Sc.

VESTI

Ustanovitev Odseka za računalniške sisteme

19. septembra 1994 je direktor Instituta "Jožef Stefan" doc. dr. Danilo Zavrtanik na osnovi 3. in 12. člena Statuta IJS ter v soglasju z Znanstvenim svetom Instituta izdal Sklep o ustanovitvi nove samostojne raziskovalne enote, to je Odseka za računalniške sisteme, z izločitvijo iz Odseka za računalništvo in informatiko (OE-4). Dejavnosti tega Odseka so arhitekturna sinteza vzporednih računalniških sistemov, načrtovanje, testiranje in diagnostika elektronskih vezij in sistemov ter podatkovni modeli in načrtovalski postopki v inženirskih okoljih. Do imenovanja vodje se za v. d. vodje Odseka za računalniške sisteme imenuje doc. dr. Franc Novak.

Odlomek iz NOVIC IJS

PRVI SLOVENSKI ŽAREK

Minister za znanost in tehnologijo, dr. Rado Bohinc, je lani z vodstvom sinhrotrona Elettra na Bazovici pri Trstu podpisal listine o sodelovanju. Pred kratkim pa sta Institut "JoŽef Stefan" obiskala generalni direktor sinhrotrona dr. Giuseppe Viani in znanstveni direktor prof. dr. Renzo Rosei, ki sta povedala, da je mednarodni programski komite odobril načrte za slovensko Žarkovno linijo.

Marca lani je bilo ustanovljeno neformalno združenje institucij in oseb, ki želijo opravljati poskuse na tržaškem sinhrotronu. Najprej je bilo treba dokazati dejanske potrebe Slovenije po raziskavah s sinhrotronsko svetlobo. Odziv je presegel vsa pričakovanja. Več kot 100 raziskovalcev iz desetih slovenskih raziskovalnih ustanov je pripravilo 35 predlogov za raziskave, več kot 20 slovenskih podjetij pa je pisno izjavilo, da bi radi uporabljali slovenske žarkovne linije, ter podprlo projekt gradnje.

Na podlagi teh predlogov in koncepta za žarkovno linijo, ki ga je pripravil dr. Iztok Arčon, je bila pripravljena znanstvena utemeljitev, nato pa so se ga lotili mednarodni recenzenti, saj to zahteva družba Sinhrotrone Trieste za vsako žarkovno linijo, ki naj bi jo postavili v Elettri.

Posebnosti slovenske linije

Običajno so žarkovne linije specializirane za eno samo merilno tehniko, slovenska žarkovna linija pa je načrtovana večnamesko: s sipanjem rentgenskih žarkov je mogoče določati strukturo snovi in površin, absorbcijska spektroskopija omogoča selektivni študij lokalne okolice posameznih elementov v snovi in njihove kemijske vezave, fluorescentna spektroskopija omogoča merjenje zelo majhnih koncentracij elementov v snovi, fotoelektronska spektroskopija pa daje informacije o elektronski zgradbi materialov.

Pri tem je bistveni kriterij kvaliteta možnih raziskav in ne, ali ima interesent na voljo denar. Na decembrski seji programskega odbora so člani soglasno sprejeli znanstveno utemeljitev slovenske žaskovne linije in s tem je bila uspešno opravljena stroga mednarodna recenzija.

Naslednji cilj je zagotoviti denar za gradnjo linije, ki naj bi stala okrog 2 milijona mark. Ker je to vrhunski projekt in je poleg tega predmet sodelovanja med Italijo in Slovenijo, se obetajo možnosti za financiranje iz posebnih mednarodnih virov, seveda pa bo pri tem morala finančno sodelovati tudi Slovenija.

Dnevnik, 30.01.1995

LEMA

LIGA-Experiment for Multiple Application

The development of the LIGA process (lithography, electroforming and moulding) is being carried out at Forschungszentrum Karlsruhe (the former Nuclear Research Center) since the early 1980s. The LIGA process allows the manufacturing of microscale structures in a wide variety of materials (metals, plastics, ceramics). A high aspect ratio (height / minimal lateral dimension) of the microstructures can be attained. Structures with details in submicrometer accuracy (e.g. microspectrometers) as well as with heights beyond 1 mm can be manufactured.

However, to achieve the outstanding properties of LIGA microstructures the comparably expensive deep lithography process step using X-ray radiation is required to produce the first microstructured devices. The subsequent moulding processes allow the production of microstructures in high numbers at low cost.

As a new opportunity Forschungszentrum Karlsruhe offers to customers from industry, research or science the production of microstructured devices by sharing a mask together with other customers at a reasonable price. A subsequent industrial mass production of microstructures could be carried out by our Licensee microParts GmbH, Dortmund.

It is planned to provide each customer wishing to take part in this experiment with a mask area of 0,5 cm x 0,5 cm for the production of customer designed microstructures. As a matter of course all customer designs will be treated confidentially.

The process sequence being the same for all users, requires a few restrictions and the definition of a standard procedure. The following conditions will be applied to the first LEMA run:

Material:	Nickel, PMMA
Height:	200 μm
Lateral dimensions:	≥10 μm
Edge details:	≥2 μm

Should your individual situation ask for a differing procedure, Forschungszentrum Karlsruhe is prepared to give you a specific offer according to your needs and specifications.

The cost for the LEMA participant will be DM 950,- (+VAT) for the production of microstructured devices.

The data for the structures to be produced shall be transferred in the GDS-II format. On special request, other CAD format will be accepted, too. We can also offer the CAD construction of the microstructures.

Please make sure to get in touch with our experts regarding the design rules and data format before delivering any design.

For further information please contact:

Forschungszentrum Karlsruhe GmbH

Postfach 3640

D-76021 Karlsruhe

Organization:

Dr. P. Bley,

Projektleitung Mikrosystemtechnik

Tel.: 07247-82-2777, Fax: 07247-82-5579

Design rules for the LIGA structures:

Dr. J. Mohr,

Institut für Mikrostrukturtechnik (IMT)

Tel.: 07247-82-4433, Fax: 07247-82-4331

Data format:

Dr. K.-P. Scherer,

Institut für Angewandte Informatik (IAI)

Tel.: 07247-82-5762, Fax: 07247-82-5785

Orders:

Hauptabt. Einkauf und Materialwirtschaft (EKM)

Frau Mazura

Tel.: 07247-82-5327, Fax: 07247-82-6122

Deadline for submission of the designs:

May 15,1995.

NEWS FROM AMS

The First Billion in Sales exceeded at AMS

The intended AMS sales of 1 billion Austrian Schillings (ATS) for 1994 was exceeded in the beginning of December. This represents an increase in sales of over 20% already at the beginning of December 1994 compared to the sales of the year 1993 of 812 million ATS. From 1992 to 1993 sales grew by 12%.

The development of the company exceeds the forecasts by the international finance analysts. Today the AMS share price gain since its flotation in July 1993 is 243%. Since this value has not been achieved by any of the 70 new investments since 1993 in Europe currently owned by the Rockefellers, the head of the family, David Rockefeller Senior and his son David Junior, invited the President and CEO of AMS. Mr. Horst Gebert, personally to the 50th anniversary celebration of the United Nations at its headquarters on the East River in New York City to present the AMS success story to the 110 family members.

David Rockefeller, Chairman of the Rockefeller and Co., Inc. Rockefeller Plaza, New York: "We *are delighted to be associated with you as an investor in your fine company."*

Note: The Rockefellers, who earned their money initially with the "Standard Oil Company", historically distinguish themselves by their generous support of the sciences, welfare, peace, the environment and the arts. The property on which the UN Headquarters today stand were donated 1944 by John Rockefeller II, one of the early advocates of the UN idea.

First ASIC Design Centre in Budapest opened by AMS

AMS has opened a further ASIC Design Centre in Budapest following the extraordinary success of the Design Centre in Dresden to guarantee the dynamic growth of the company: The Design Centre in Budapest will serve the newly developing markets of the East including Russia with innovative systems solutions. AMS is the specialist for the design of mixed analogue/digital circuits and the No.1 in Europe: Designs for ASICs, applications and development support and product engineering for the market segments communications, automotive and industrial electronics. This specialization plus the high quality standard of all AMS products are decisive for the success at AMS.

The address of the new design centre:

Austria Mikro Systeme International
Fejlesztó es Forgalmazó Kft
Reitter Ferenc Utca 39-49,
H-1037 Budapest
Tel: (0361) 270 5400
Fax: (0361) 270 5401

The new AMS design center is ready to perform with a highly qualified team of Hungarian employees - all experts in the design of mixed analogue/digital high performance circuits. The new design centre is equipped with state-of-the-art hardware and software for the independent design of systems solutions. The European network structure secures the exchange of data and experience of all AMS activities on-line. The first stage of the design centre is conceived for 15 design engineers.

Mr. Zoltan Huszka, the manager of the Design Centre Budapest has an outstanding track record of three decades in the research and development as well as in the design and production of integrated circuits. **Mr. Huszka is the pioneer in the field of microelectronics in Hungary:** The development and production of the very first TTL ICs in 1969 originates from Zoltan Huszka. In 1984 Mr. Huszka became head of the engineering department at MEV and in 1988 he took over the technical management as well. Since 1991 Mr. Zoltan Huszka has been director of Intermos. Zoltan Huszka comments his new position: *"Especially the daily pioneering spirit and the continuously new innovative product developments at AMS make this unique task so challenging."*

The advantage of this expansion is that the AMS customer will profit in an even higher degree of an increased service and the large resevoir of AMS' experience in the area of mixed analogue/ digital circuits and complex circuit designs. Over 100 top designers now work in the worldwide AMS engineering team.

AMS introduces new high density, high speed 0.8 Micron BiCMOS Process

AMS announces the introduction of a new AMS submicron BiCMOS process specially suited for ASIC products: A 0.8 micron BiCMOS process with effective channel lengths of 0.65 micron featuring superior bipolar analogue performance such as low noise, good matching, low sensitivity to process variations, high operating frequency and higher transconductance - thus, the ideal technology for high speed mixed signal systems on silicon!

The new process is based on the proven AMS 0.8 micron CMOS process and includes an additional high performance analogue oriented poly emitter 12 GHz bipolar module providing mixed signal and ECL, BiCMOS and CMOS design capabilities for 3V and 5V operation. A full set of I/O cells allow to interface to CMOS, TTL and ECL systems both in single-ended and in differential manner at speeds of up to 2.5 GHz.

The process is complemented by a high performance cell library including BiCMOS cells and differential ECL/CML cells in three speed/power variations. Interfacing between ECL and CMOS cells is supported by a full range of level converters. CMOS and BiCMOS cells can be freely mixed without any level conversion since a full swing BiCMOS buffering scheme is used for all BiCMOS core cells.

The existing 0.8 micron digital standard cell library designed for the AMS 0.8 micron CMOS process is fully compatible since the bipolar process module does not affect the CMOS device characteristics.

This new BiCMOS process is ideal for fast and high precision mixed signal circuits, for ATM transmission systems of up to 1.24 GBits/s, for wireless communication systems of up to 2 GHz, for high speed AD/DA converters of up to 200 MHz and for hard disk read channels.

For a free data sheet and further information please contact your local AMS sales office or AMS Corporate Communications, Schloss Premstatten, A-8141 Unterpremstatten, Austria.

Schloß Premstätten
A-8141 Unterpremstätten, Austria
Telex 312547 ams a
FAX (03136) 52 501, 53 650

ELECTRONICS, September 1994

CD-ROM drive rewrites magneto-optical data

Today (26 *Sept.)* at Datashow '94 in Tokyo, Matsushita Electric Industrial Corp. of Osaka will display for the first time prototype versions of a new drive that combines the high capacity of CD-ROM disks with the erase/rewrite capability of magneto-optical disks. Previously, the two formats were incompatible.

The new drive can play quadruple-speed CD-ROM disks and record or play 630 Mbytes of data to phase-change optical disks. CD-ROM data can be transferred to phase-change disks to allow modification or upgrades of software or multi-media programs.

The drive will be commercially available, company officials said, by spring 1995.

The key element that makes the drive possible is a newly developed microoptical head that combines a CD-ROM reading function with a rewriting function for large-capacity phase-change optical disks. Other impor- tant elements are improved phase-change optical disk materials and structure. They provide sufficient sen sitivity to directly overwrite optical data as fast as the quadruple-speed CD-ROM, using only 10 milliwatts of laser power.

The drive incorporates a tray loading mechanism that accepts CD-ROM bare disks or phase-change optical disk cartridges interchangeably.

OEM samples of internal drives will be available in November, priced at ¥ 100,000 (US$1,000). Volume pricing has not yet been determined.

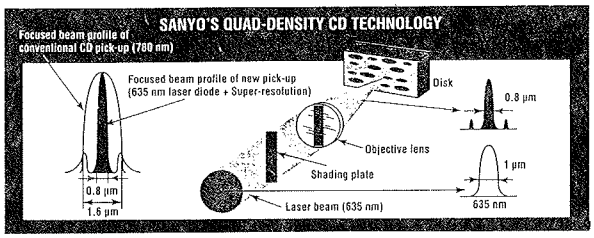
CD breakthrough quadruples capacity

On 4 Oct. at the Tokyo Electronics Show, **Sanyo Electric Co. Ltd** of Osaka will demonstrate a newly developed quadruple-density compact-disk technology. With the help of MPEG-2 video compression, **the new recording technique can put 135 minutes of full-motion video with a data transfer rate of 3 Mbytes/s on one standard CD**. In CD-ROM applications, a capacity of 2.5 Gbytes is possible while preserving compatibility with older CD-ROM disks.

CDs record data using pits. To increase recording density, more pits must be packed into a smaller area. To reduce the size of the pits, Sanyo researchers used a

635-nanometer laser, the shortest available, and further reduced beam spot size by using a lens with a larger aperture *(see illustration)*. Spot size was reduced to 0.8-micron from the usual 1.6-micron size.

To record smaller pits on the surface of the master disk, Sanyo developed and used a new disk mastering technology.



NEC TO BUILD SEMICON FAB

In April 1995, **NEC Corp.** of Tokyo will start construction on a US$800 million semiconductor plant in Livingstone, Scotland. **The new fab will produce 20,000 8-inch wafers per month using 0.35-micron process technology**. Volume production will begin in October 1996.

The plant will produce 64-Mbit DRAMs, advanced ASICs and microprocessors for the European market.

Hajime Sasaki, NEC executive vice president, said the plant is needed to meet an increased demand for 64-Mbit DRAM. He pegs the shortfall in worldwide capacity at 20%.

Toshiba to offer 0.4 micron ASICs

Toshiba Corp. of Tokyo has combined 0.4-micron process with doulbe- and triple-layer wiring technologies to build application specific integrated circuits (ASICs) with a usable gate count of up to 750,000 and a gate delay time of 0.19 nanoseconds when operated at 3.3 volts.

Three ASIC families will soon be available: TC200G-series gate arrays, TC200C-series cell-based ICs, and TC200E-series embedded arrays. Toshiba is taking gate array and IC development orders in October. Orders for embedded arrays will be taken starting in January.

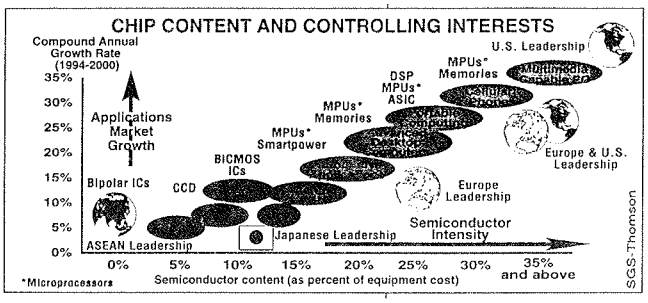
Semiconductors drive worldwide commerce

Semiconductor process technology is key to remaining competitive in worldwide commerce today. Furthermore, the ability to invest in state-of the-art process technology is essential to remaining a viable contender. Why has the integrated circuit become so important?

Jean Philippe Dauvin, director of economic strategies at SGS-Thomson Microelectronics Inc. in St. Genis, France, says the reason is that semiconductor content in all manufactured goods is steadily rising. "In the 1970s and 1980s, all manufactured equipment had only about 7% semiconductor content," he observes. By 1993, the content had risen to 11 %. This year the level should reach 13%. For some equipment, such as PCs, the content is much higher *(see illustration)*.

Furthermore, the types of semiconductors being produced are changing. Complex logic circuits with entire systems on a chip have replaced memories as the semiconductor industry mainstay.

Dauvin says that to keep pace with this demand, ever more costly fabs need to be built. In the 1970s, the average cost of a fab was US$40 millţn. Today, the cost is over $ 1 billion. The jump is significant in real terms, a 25-times increase.



However, assuming a constant wafer diameter of 150 mm, the cost increase per square millimeter of wafer is a more modest 2.5% per year. Meanwhile, the revenue per square millimeter of wafer has risen a whopping 15% per year.

In addition, while the industry has evolved over the past 25 years, there has been little consolidation. When players fail, others step in to take their place. Thus, the total number of large suppliers has remained relatively constant over the last two decades.

However, this situation can no longer remain, Dauvin contends. Those able to compete will be determined by the level of investment they are able to make. Dauvin says Intel will invest about $2.4 billion; Motorola, $ 1.6 billion; Samsung, $ 1.2 billion; and most Japanese companies, $900 million. SGS will spend about $750 million, as will Texas Instruments and AMD. Anyone investing less will not be able to keep pace with the pack.

In addition, there is a fundamental change in the nature of the industry as a result of the steadily rising semiconductor content in equipment, Dauvin contends. Today, IC demand is increasing faster than investment.

In the boom and bust cycles of the late 1980s, investment per year was growing at 70% per annum, while demand was growing at only 30%. This resulted in periods of overcapacity. Today, the ratios are more in line, Dauvin declares. The market has been growing 25% while investment has been growing at 31 %.

Dauvin joins the chorus of voices claiming that total investment will not keep pace with semiconductor demand throughout the rest of this decade. He estimates that by the end of this century,110 new state-of-theart fabs must be built. Assuming a price tag of $ 1 billion, that's $ 110 billion. If the top 10 companies each invest on average $ 1 billion for the next five years, only half the number of fabs needed will actually get built.

Samsung claims world's first 256M DRAM

Samsung Electronics Co. in Seoul announced in late August that it has developed a fully working 256-Mbit DRAM die using 0.25-micron technology to make 268 million cells.

Samsung's President Kim Kwang-ho said that, as far as he knows, none of Samsung's rivals, such as **NEC Corp.** of Tokyo and **Texas Instruments Inc.** of Dallas, have yet to succeed in coming up with a fully functional sample of a 256-Mbit DRAM die. "I believe it will take at least six months or a year for them to reach this stage," Kim said.

Samsung said the chip can be operated on a very low voltage, ranging from 2.2 volts to 2.4 V. Its self-developed multiple input/output architecture enables the chip to have a very fast access time of 40 nanoseconds. The chip fits into a 600-mil small outline J-lead package.

Samsung aims to have an engineering sample ready by 1996, but has not yet fixed the schedule for mass production, said Kim. Whether the company will use 12-inch wafers in the production of 256-Mbit DRAM also has not been decided.

Earlier this year, Samsung and NEC formed a strategic alliance to develop the 256-Mbit DRAM. Kim said the alliance would continue because it was formed to codevelop processes required for 256-Mbit DRAM production, not to develop the device itself. He said such strategic alliances among memory producers were unavoidable because of skyrocketing development costs.

Kim said the company has already kicked off the development of 1-Gbit DRAM by forming a task force for the project. Samsung has filed 129 patents involved in the 256-Mbit DRAM, 49 of them in the U.S. and other advanced nations.

Samsung had denied earlier reports of its 256-Mbit DRAM *(see EL, 22 Aug., cover)* because it wasn't until 26 Aug. that a 100% working die met internationally acceptable standards.

Swiss semicon company successfully works with SMIF

While Europe's big semiconductor manufacturers have only started projects on smart semiconductor fabs *(see EL 27 June, p. 1)*, a small Swiss company, **EM Microelectronic-Marin SA** in Marin, has worked with such a system, an SMIF (standard mechanical interface), for nearly four years.

SMIF offers a class 1 work environment within the processing machine. However, around the machine there is only a class 100 clean room.

"By using SMIF we were able to implement a class 1 fab at less than 70 % of the ordinary running costs of a class 1 fab," said Mougahed Darwish, president of EM.

EM manufactures about 140 million chips per year and has grown 10% per year over the last 10 years. It is 100% owned by **SMH AG** of Neuenburg, Switzerland, a watch manufacturer with a 1993 revenues of SFr 2.9 billion (US$22 billion).

A typical EM product is an IC that covers all functions needed in a watch. It consumes only 150 nanoamperes at 1.5-volt supply voltage, yet works at voltages down to 1 V and has an EEPROM as well as an oscillator on chip.

"We are leaders in Europe and in the U.S. in the very-low-power/low-voltage market," stated Darwish.

Some 50% of EM's revenue comes from SMH. Of its free-market business, 60% is customer-specific. An interesting market for EM is the contactless chipcard market, where it is focusing on identification cards. Another upcoming market is immobilizers for automobiles.

Despite delivering high volumes, the company serves niche markets with low-power and very-low-power products. Most frequencies are less than 25 MHz; in some applications up to 70 MHz. "Our goal is to reach 2- to 3-GHz transition frequency next year with our new BiCMOS technology," said Darwish.

Next year, EM will manufacture 4- and 8-bit microcontrollers running at "several MHz clock frequency, but with very low power."

KNJIGE IN ZBORNIKI

C.J. Farrell: A Theory of Technological Progress

A Theory of the development of artifacts and their technologies is presented. This theory starts by establishing a heirarchy of artifacts and classifying them in a simple scheme. Then the growth of a new artifact in the absence of substantial competition is modeled and illustrated with realistic examples. The model is further developed to explain the substitution in a special case in a more general theory which is necessary when an attacker has a performance advantage over the defender as is usually the case. This is quantified in several real instances. Finally the important role of stochastic events is shown by defining five categories and same of their known effects. (18 ref.)

Izvor: IEEE Eng. Manag. Rev. (USA), Voll. 22, No.1

1994 Symposium on VLSI Circuits.

Digest of Technical Papers, New York, N. Y. USA.

Conference held at: Honolulu, HI, USA, Date June 1994.

Sponsors: IEEE, Solid State Circuits Council, Japan Soc. Appl. Phys. IEICE of Japan.

The following topics were dealt with: data convertors, low power logic, phase-locked loops and high-speed interfaces, flash EEPROMs, digital system chips, dynamic memory concepts, signal processing circuits, SRAM chips, and communication circuits.

Second European Conference on Radiations and their Effects on Components and Systems (RADECS 93)

Conference held at: Saint Malo, France, Date Sept. 1993. The following topics were dealt with: environments

and emerging issues; dosimetry; system hardening; industrial data and radiation sources; basic radiation effects; radiation effects in non silicon devices; optical fibres; radiation hardening technology; SOI and other silicon technologies; single event phenomena; dose rate effects.

Izvor IEEE Trans. Nucl. Sci. (USA) vol. 41, No. 3 (June 1994)

NOVI PROIZVODI

Časopis EDN u broju od 8.12.1994 godine objavio je 100 elektroničkih proizvoda proizvedenih prošle godine koje čitaoci časopisa smatraju najboljima. U ovome i slijedećim brojevima našega časopisa pokušati ćemo naše čitaoce upoznati s dijelom tih proizvoda.

Miniature 8 W dc/dc converters are 100% burned in

The 800 series of 8W dc/dc converters is 100 % burned in for 72 hours. The units' six-sided metal case measures 1x2x0.375 in. They operate over a -30 to +71°C range with no derating or heatsinking. The series features 5, 12, and 15 V outputs in single-double-, and triple-output models. The units also have input filters and remote on/off control. $58 to $66. Conversion devices, Brockton, MA. USA. (508) 559-0880.

DIP converters output 1W

D-3 dc/dc converters output 1.2 W (1 W for 5 V output models). Housed in a DIP-type package measuring 0.5x0.4 in., the units accept inputs of 5, 12, 15 or 24 V, ±5, ±12, or ±15 V. Output voltage accuracy equals ±5%, and total output ripple and noise measures 150 mW p-p max. Operating range spans 0 to 70°C. $18.75 and $19.75 for single- and dual-output models, respectively, Alban Inc. Santa Clara, CA, USA, (408) 988-3949.

Voice chip attains consumer pricing

The ISD 1100 is a solid-state analog record and playback device that stores 10 sec of sampled audio. Because it stores the audio as analog charge levels in EPROM, the device does not need A/D conversion. IT CONTAINS INPUT AND OUTPUT PREAMPLIFIERS, agc, AND FILTERS ON CHIP. $5.48 in dips; $4.18 as bare die (1000). Information Storage Devices, San Jose, CA. USA, (800) 332-8638.

Wireless data link connects computer equipment

A pair of transceiver units known as Command enables a computer to communicate wirelessly with another computer or with peripheral equipment. The units connect to RS-232C ports and operate on the 900 MHz band. No FCC license is necessary. $429.95. Communications R&D Corp., Indianapolis, IN, USA, (317) 290-9107.

Digital-coupler IC replaces optocuplers

The ISO150 uses high-voltage capacitors instead of an LED and photodiode to transmit signals across the isolation barrier. This alternative device to high-speed optocuplers offers faster performance, lower power consumption, and better isolation specifications. The coupler also acts as transceiver, whereas optocuplers are unidirectional. Primary applications include digital isolation for A/D and D/A conversion, multiplexed data transmission, and I/O port isolation in instruments. The IC requires no external components. Key specifications include an 80-Mbps max power consumption per channel, 240 V-rms isolated partial discharge, and 16,5-mm creepage distance. In a 24-pin DIP, $7.75 (1000). Burr-Brown Corp. Tucson, AZ. USA, (602) 746-1111.

System adds cellular connection to Pcs.

The Ubiquity 2000 attaches to a mobile computer via a serial port and provides a range of voice and fax cellular-communication services. It transfers wireless data over cellular-digital-packet-data (CDPD) or circuit-switched cellular systems. The system permits clear, wireless voice and data communication inside building and in fringe areas. $1595. Pacific Communication Sciences Inc. San Diego, CA. USA, (619) 535-9500.

Heat-pipe heat sinks cool power semiconductors

A line of heat pipe heat sinks uses a non-ozone-depleting fluid. The heat sinks suit outside-traction applications. Standard models are available for semiconductor devices up to 3.94 in. in diameter and dissipate up to 3000 W. Models with thermal resistance as low at 0.01°C/W at 10-ft/sec airflow are available. $260 (1000). Thermacore Inc. Lancaster, PA. USA, (717) 569-6551.

Heat sinks cool TO220, 218, TO3-P, and multiwatt devices

A family of 1,65- and 2-in.-wide heat sinks mounts vertically and provides a threaded mounting hole. You can mount the heat sinks with tin-plated solderable studs or screws. $11 (1000); delivery is three to four weeks ARO. International Electronic Research Corp. Burbank, CA. USA, (213) 849-2481.

NiMH batteries hold 40% more juice than NiCd batteries

The DR19 and DR31 nickel metal-hybrid (NiMH) batteries last 40% longer than comparably sized NiCd nbatteries. The DR19 is a 10.8 V, 1500 mAhr battery in a 9x4/5 A package. The DR31 is a 10.8 V 2400 mAhr battery in a 9x4/3 A package. DR19 $99, DR31 $169 (retail). Duracell International Inc. Bethel, CA. (203) 769-3281.

"FLASH" MEMORIJE

Pretpostavljajući da će naići na zanimanje naših čitalaca prenosimo u širim izvodima djelove iz INTEL-ove brošure "One Memory Solution":

Over the past six years, Flash technology has come a long way. In fact, the Flash memory of today only vaguely resembles the flash you may be familiar with. With breakthroughs like 33 Mhz Synchronous Flash and Smart Voltage technology, and manufacturing gains to bring prices down 32x since 1986 (measured by cost/MB), Flash now meets or beats DRAM+ROM. SRAM+battery, or updated EPROM solutions in performance, functionality and overall cost.

With higher densities, greater functionality and JEDEC standardization, Flash truly requires a shift in thinking about memory system architectures. Because a single Flash chip can do the work that used to require several kinds of chips. So read on, and discover why Flash memory goes above and beyond the rest.

Flash Memory vs. DRAM+ROM

Flash technology is not only in high-volume production, but it's as fast or faster, and it's actually cheaper, than DRAM solutions. And the trend will just keep going as we continue to introduce smaller, faster, and smarter devices. Because Flash is a nonvolatile memory solution, it can perform the function of code DRAM and nonvolatile backup storage in your design. Flash immediately eliminates the need for redundancy, allowing for instantaneous start-ups and an overall increase in system performance.

Intel's new Synchronous 33 MHz Flash Memory solution, which can now reside on the processor local bus, approaches 2ns-level cache performance. It can eliminate DRAM+ROM by executing code directly from Flash at faster-than-DRAM speed.

Beyond that, Intel even offers a new 16 Mb Flash component that has a multiplexed address bus and is compatible with most DRAM RAS#/CAS# controllers, so you can get your hardware design up and running quickly, leaving more time for software development.
And there is no constraint on Flash components. Intel is a full production all the way up to 32 Mb.

Flash Memory vs. battery-backed RAM

Flash is an excellent alternative to battery-backed RAM (such as SRAM) being used as a nonvolatile solution. Flash memory is about one third of the cost, and that doesn't even include battery.

By eliminating the backup battery+RAM with Flash, you no longer have to worry about battery failure resulting a loss of data. Flash also allows you to build a more power and space-efficient design.

Flash has an 8x density advantage over SRAM. So in some applications, you can replace all of your battery-backed SRAM in one block of an Intel Boot Block Flash chip. The rest of the chip can be configured for boot code, BIOS, whatever you want. And in the end, your chip inventory and cost per design go down, and you have a more flexible, reliable solution.

Flash Memory vs. EPROM

In today's competitive time-to-money race, using Flash over EPROMs is like giving yourself an insurance policy against missing your design schedule. Because Flash is in-circuit reprogrammable, a feature that will save your company time and money on both ends of designe cycle.

In-circuit programming means Flash is much cheaper and faster to prototype and debug. And it allows you to respond to last-minute marketing requests. Flash-based systems can also be test-code programmed to test your systems on-line, then reprogrammed with production code on their way out the door, thus maintaining a just-in-time inventory. Using flash memory, you could even move up your launch dates.

And when you need to upgrade already-shipped systems to stay competitive, all you have to do is pop in a diskette or connect to a comm-link. No more expensive service calls, system disassembly or hustle with UV erasing. Customers will appreciate the reduction in downtime to.

Amazingly enough, Flash also offers features like Smart Voltage and memory integration that you'll never find in EPROMs. And Flash is completely scaleable to 32 Mb and beyond, while higher-density EPROMs become increasingly difficult to obtain.

New Intel Smart Voltage technology

Intel Smart Voltage technology is a quantum leap beyond any other Flash solution, making Intel Flash the lowest-power, most flexible solution available. Smart Voltage technology offers dual-supply pinouts that let designer select the integration of a 5V-only system, the power savings of 3.3 V logic or the high performance of a 12 V write operation.

Smart Voltage technology works like this: First, for systems supplied only by 5 volts. Smart Voltage Flash chips end the need for a separate 12 V source. Instead, they generate 12 internally with an on chip charge pump.

Second, in portable equipment, where low power consumption attends battery life, Smart Voltage Flash chips offer a separate 3.3 V read line. This slashes the power consumed for read operations by as much as 66 percent over 5 V chips. Moreover, future Smart Voltage devices will yield a 2.7 V read capability.

Third, in real-time systems where high performance is often a designer's first priority. Smart Voltage chips offer the speed of 12 V write cycles. The higher write voltage also speed the manufacturing process, shortening the system assembly speed the manufacturing process throughput time. Once programmed at the higher rate, Smart Voltage Flash chips can work in any of three scenarios.

Zbral in uredil M. Turina

KOLEDAR PRIREDITEV 1995

APRIL

04.04.-06.04.1995
SEMICON EUROPA
GENEVA, Switzerland
Info.: 0101 415 940 6961

40th Annual Gathering KOREMA
ZAGREB, Hrvatska
Info. 385 1 611 944 Ext.127

MAJ

03.05.-05.05.1995
SMT ASIC-HYBRID
NÜRENBERG, Germany
Info.: +49 711619 4634

04.05.-14.05.1995
CAD'95
CRIMEA, YALTA, Ukraine
Info.: +095/917-1719

14.05.-17.05.1995
10th EUROPEAN MICROELECTRONICS CONFERENCE
COPENHAGEN, Denmark
Info.: +45 4492 4492

16.05.-18.05.1995
CONTROL & INSTRUMENTATION
BIRMINGHAM, England
Info.: 081 302 8585

22.05.-26.05.1995
MIPRO 95
OPATIJA, Hrvatska
(info. 385 51 211 051)

JUNIJ

12.06.-16.06.1995
INTERTRONIC
PARIS, France
Info.: 0781 221 3660

14.06.-15.06.1995
INSTRUMENTATION Exibition
LIVINGSTON, England
Info.: 0822 614671

20.06.-22.06.1995
INTERNATIONAL MIXED SIGNAL TESTING WORKSHOP
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JULY

04.07.- 05.07.1995
1st IEEE INTERNATIONAL ON-LINE TESTING WORKSHOP
NICE, France
Info.: +1 409 862 2438

11.07.- 13.07.1995
SEMICON WEST
San Francisco, CA, USA
Info.: +1 415 940 6961

AUGUST

27.08.- 30.08.1995
5th EUROPIAN CONFERENCE ON ELECTRON AND OPTICAL BEAM TESTING
WUPPERTAL, GERMANY
Info.: +49 202 439 2972

SEPTEMBER

19.09.- 21.09.1995
AUTO TEST COM.
ATLANTA, USA
Info.: +1 370 287 1463

27.09.- 29.09.1995
23rd INTERNATIONAL CONFERENCE ON MICROELECTRONICS, MIEL '95
31st SYMPOSIUM ON DEVICES AND MATERIALS, SD '95
TERME ČATEŽ, Slovenija
Info.: +386 61 312 898

27.09. - 28.09.1995
INSTRUMENTATION Exibition
Warrington, ENGLAND
Info.: +44 822 674 671

NAVODILA AVTORJEM

Informacije MIDEM je znanstveno-strokovno-društvena publikacija Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale-MIDEM. Časopis objavlja prispevke domačih in tujih avtorjev, še posebej članov MIDEM, s področja mikroelektronike, elektronskih sestavnih delov in materialov, ki so lahko:

izvirni znanstveni članki, predhodna sporočila, pregledni članki, razprave z znanstvenih in strokovnih posvetovanj in strokovni članki.

Članki bodo recenzirani.

Časopis objavlja tudi novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter druge relevantne prispevke.

Strokovni prispevki morajo biti pripravljeni na naslednji način

- 1. Naslov dela, imena in priimki avtorjev brez titul.
- 2. Ključne besede in povzetek (največ 250 besed).
- 3. Naslov dela v angleščini.
- 4. Ključne besede v angleščini (Key words) in podaljšani povzetek (Extended Abstract) v angleščini.
- 5. Uvod, glavni del, zaključek, zahvale, dodatki in literatura.
- 6. Imena in priimki avtorjev, titule in polni naslovi podjetij, oz. institucij s tel. in fax. številko, kjer so zaposleni.

Ostala splošna navodila

1. V članku je potrebno uporabljati SI sistem enot oz. v oklepaju navesti alternativne enote.

2. Risbe je potrebno izdelati na belem papirju. Širina risb naj bo do 7.5 oz. 15 cm. Vsaka risba, tabela ali fotografija naj ima številko in podnapis, ki označuje njeno vsebino. Risb, tabel in fotografij ni potrebno lepiti med tekst, ampak jih je potrebno ločeno priložiti članku. V tekstu je potrebno označiti mesto, kjer jih je potrebno vstaviti.

3. Delo je lahko napisano in bo objavljeno v kateremkoli jugoslovanskem jeziku v latinici in v angleščini.

Uredniški odbor ne bo sprejel strokovnih člankov, ki ne bodo poslani v dveh izvodih.

Avtorji, ki pripravljajo besedilo v urejevalnikih besedil, lahko pošljejo zapis datoteke na disketi (1.2 ali 1.44) v formatih ASCII, wordstar (3.4, 4.0), wordperfect, word, ker bo besedilo oblikovano v programu Ventura 2.0. Grafične datoteke so lahko v formatu HPL, SLD (AutoCAD), PCX ali IMG/GEM.

Avtorji so v celoti odgovorni za vsebino objavljenega sestavka. Rokopisov ne vračamo.

Rokopise pošljite na naslov

Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 61000 Ljubljana

UPUTE AUTORIMA

Informacije MIDEM je znanstveno-stručno-društvena publikacija Stručnog društva za mikroelektroniku, elektronske sastavne dijelove i materijale - MIDEM. Časopis objavljuje priloge domaćih i stranih autora, naročito članova MIDEM, s područja mikroelektronike, elektronskih sastavnih dijelova in materijala koji mogu biti:

izvorni znanstveni članci, predhodna priopćenja, pregledni članci, izlaganja sa znanstvenih i stručnih skupova i stručni članci.

Članci će biti recenzirani.

Časopis također objavljuje novosti iz struke, obavijesti iz radnih organizacija, instituta i fakulteta, obavijesti o akcijama društva MIDEM i njegovih članova i druge relevantne obavijesti.

Stručni članci moraju biti pripremljeni kako slijedi

- 1. Naslov članka, imena i prezimena autora bez titula.
- 2. Ključne riječi i sažetak (najviše 250 riječi).
- 3. Naslov članka na engleskom jeziku.
- 4. Ključne riječi na engleskom jeziku (3Key Words) i produženi sažetak (Extended Abstract) na engleskom jeziku.
- 5. Uvod, glavni dio, zaključni dio, zahvale, dodaci i literatura.
- 6. Imena i prezimena autora, titule i puni naslovi firmi, odn. institucija sa tel. i fax. brojem u kojima su zaposleni.

Ostale opšte upute

1. U prilogu treba upotrebljavati SI sistem jedinica od. u zagradi navesti alternativne jedinice.

2. Crteže treba izraditi tušem bijelom papiru. Širina crteža neka bude do 7.5 odnosno 15 cm. Svaki crtež, tablica ili fotografija treba imati broj i naziv koji označuje njen sadržaj. Crteže, tabele i fotografije nije potrebno lijepiti u tekst, već ih priložiti odvojeno, a u tekstu samo naznačiti mjesto gdje dolaze.

3. Rad može biti pisan i biti će objavljen na bilo kojem od jugoslavenskih jezika u latinici i na engleskom jeziku.

Autori mogu poslati radove na disketama (1.2 ili 1.44) u formatima tekst procesora ASCII, wordstar (3.4. i 4.0), word, wordperfect pošto će biti tekst dalje obraden u Venturi 2.0. Grafičke datoteke mogu biti u formatu HPL, SLD (AutoCAD), PCX ili IMG/GEM.

Urednički odbor će odbiti sve radove koji neće biti poslani u dva primjerka.

Za sadržaj članaka autori odgovaraju u potpunosti. Rukopisi se na vraćaju.

Rukopise šaljite na adresu:

Uredništvo Informacije MIDEM
Elektrotehnična zveza Slovenije
Dunajska 10, 61000 Ljubljana
Slovenija

INFORMATION FOR CONTRIBUTORS

Informacije MIDEM is professional-scientific-social publication of Professional Society for Microelectronics, Electronic Components and Materials. In the Journal contributions of domestic and foreign authors, especially members of MIDEM, are published covering field of microelectronics, electronic components and materials. These contributions may be:

original scientific papers, preliminary communications, reviews, conference papers and professional papers.

All manuscripts are subject to reviews.

Scientific news, news from the companies, institutes and universities, reports on actions of MIDEM Society and its members as well as other relevant contributions are also welcome.

Each contribution should include the following specific components:

- 1. Title of the paper and authors' names.
- 2. Key Words and Abstract (not more than 250 words).
- 3. Introduction, main text, conclusion, acknowledgements, appendix and references.
- 4. Authors' names, titles and complete company or institution adress including tel. and fax. number where they are employed.

General information

1. Authors should use SI units and provide alternative units in parentheses wherever necessary.

2. Illustrations should be in black on white paper. Their width should be up to 7.5 or 15 cm. Each illustration, table or photograph should be numbered and with legend added. Illustrations, tables and photografphs are not to be placed into the text but added separatelly. Hower, their position in the text should be clearly marked.

3. Contributions may be written and will be published in any Yugoslav language and in english.

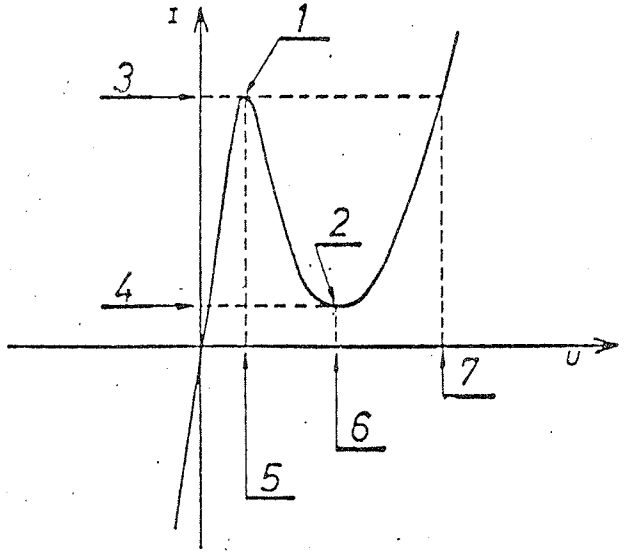
Authors may send their files on formatted diskettes (1.2 or 1.44) in ASCII, wordstar (3.4 or 4.0), word, wordperfect as text will be formated in Ventura 2.0. Graphics may be in HPL, SLD (AutoCAD), PCX or IMG/GEM formats.

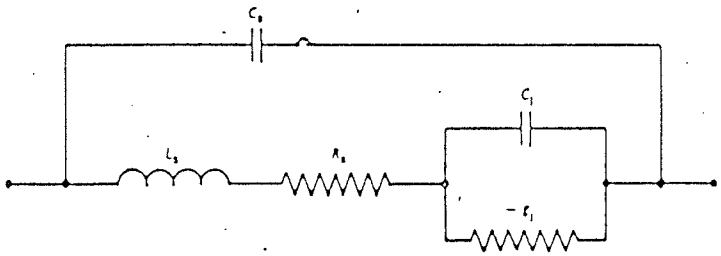
Papers will not be accepted unless two copies are received.

Authors are fully responsible for the content of the paper. Manuscripts are not returned.

Contributions are to be sent to the address:

Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 61000 Ljubljana,
Slovenia

1	2	3	4
2.3.1.3	• Tačka vrha • Vršna točka • Точка на врвот • Temenska točka	147–0/ID–1.3 • Peak point • Point de pic	Točka na karakteristiki, ki ustreza najnižji napetosti v prepustni smeri, pri kateri je diferencialna prevodnost enaka nič (glej sl. 1).
2.3.1.4	• Tačka dola • Dolna točka • Точка на долот • Dolinska točka	147–0/ID–1.4 • Valley point • Point de vallée	Točka na karakteristiki, ki ustreza tisti najnižji napetosti, ki je večja od napetosti v temenski točki, pri kateri je diferencialna prevodnost enaka nič (glej sliko 1).  Slika 1 1 – temenska točka 2 – dolinska točka 3 – temenski tok 4 – dolinski tok 5 – temenska napetost 6 – dolinska napetost 7 – napetost projicirane temenske točke

1	2	3	4
2.3.1.5	• Projektovana tačka vrha • Projicirana vršna točka • Точка на проицирање на врвот • Projicirana temenska točka	147–0/ID–1.5 • Projected peak point • Point isohypse	Točka na karakteristiki, kjer je tok enak toku v temenski točki, napetost pa je višja od napetosti dolinske točke (glej sliko 1).
2.3.1.6	• Područje negativne dinamičke provodnosti • Područje negativne dinamičke vodljivosti • Подрачје на негативна динамичка проводност • Področje negativne diferencialne prevodnosti	147–0/ID–1.6 • Negative differential conductance region • Region de conductance différentielle négative	Del karakteristike tunelske diode med temensko točko in dolinsko točko.  Slika 2 L_s – celotna zaporedna nadomestna induktivnost. R_s – celotna zaporedna nadomestna upornost C_j – kapacitivnost PN-spoja vsebne diode g_j – negativna prevodnost PN-spoja vsebne diode C_s – razsipana (vzporedna) kapacitivnost C_j in g_j sta parametra nadomestnega vezja in nista ekvivalentna parametrom C in g na priključkih. C_j in g_j sta funkciji delovne napetosti in je zaradi tega nujno označevanje delovne napetosti za določitev nadomestnega vezja.

1	2	3	4
2.3.2	Izrazi, ki se nanašajo na mejne vrednosti in karakteristike		
2.3.2.1	• Struja vrha • Vršna struja • Струја на врвот • Temenski tok	147–0/ID–2.1 • Peak point current • Courant de pic	Vrednost toka v temenski točki.
2.3.2.2	• Struja dola • Dolna struja • Струја на долот • Dolinski tok	147–0/ID–2.2 • Valley point current • Courant de vallée	Vrednost toka v dolinski točki.
2.3.2.3	• Napon vrha • Vršni napon • Напон на врвот • Temenska napetost	147–0/ID–2.3 • Peak point voltage • Tension de pic	Vrednost napetosti v temenski točki.
2.3.2.4	• Napon dola • Dolni napon • Напон на долот • Dolinska napetost	147–0/ID–2.4 • Valley point voltage • Tension de vallée	Vrednost napetosti v dolinski točki.
2.3.2.5	• Napon projektovane tačke vrha • Napon projicirane vršne točke • Напон на точката на проширање на врвот • Napetost projicirane temenske točke	147–0/ID–2.5 • Projected peak point voltage • Tension isohypse	Vrednost napetosti v projicirani temenski točki.