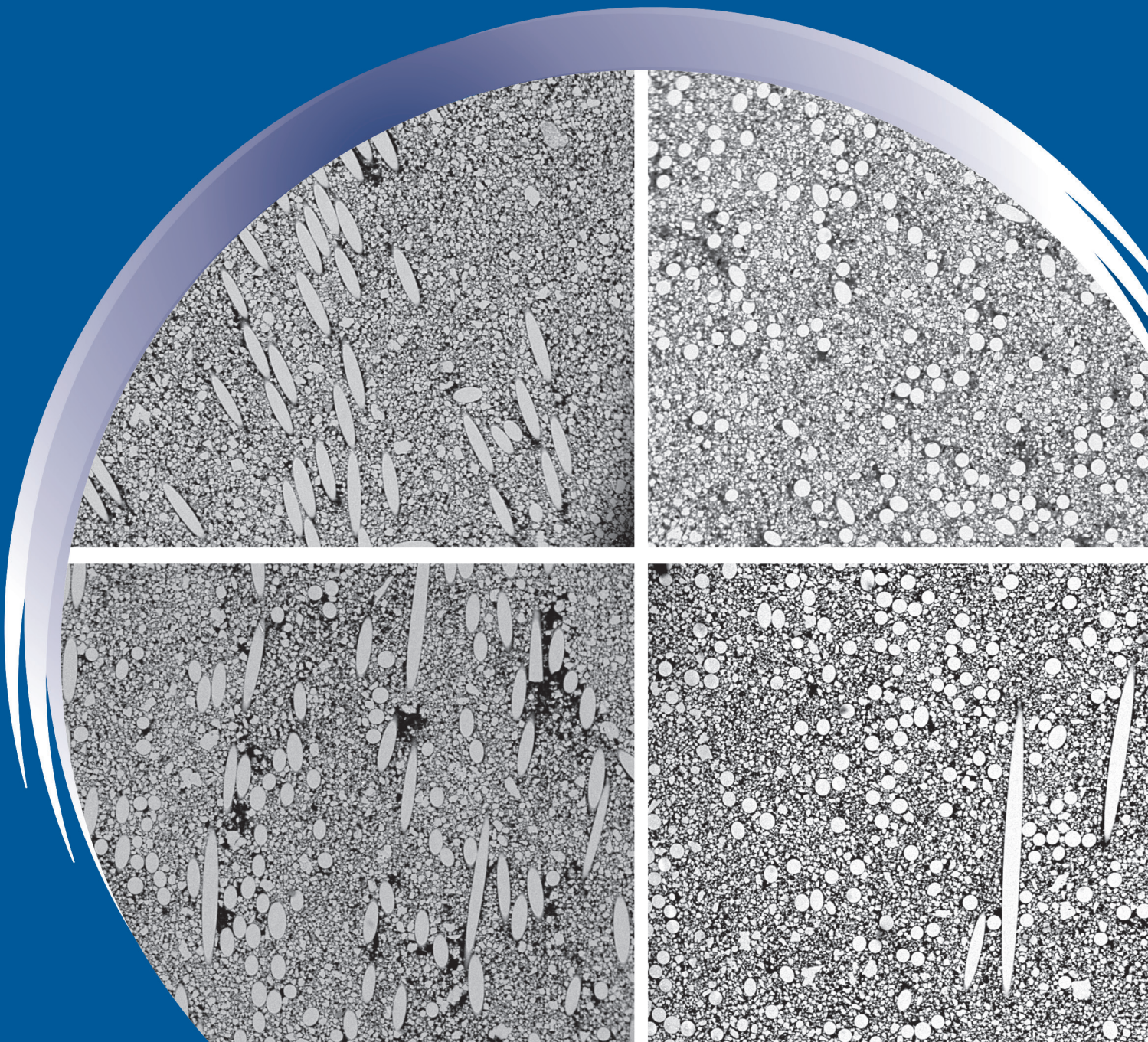
ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 45, No. 3 (2015), September 2015

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 45, številka 3 (2015), September 2015



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *3-2015*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 45, NO. 3(155), LJUBLJANA, SEPTEMBER 2015 | LETNIK 45, NO. 3(155), LJUBLJANA, SEPTEMBER 2015

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Headquarters | Naslov uredništva
Uredništvo Informacije MIDEM
MIDEM pri MIKROIKS
Stegne 11, 1521 Ljubljana, Slovenia
T. +386 (0)1 513 37 68
F. + 386 (0)1 513 37 71
E. info@midem-drustvo.si
www.midem-drustvo.si

Annual subscription rate is 100 EUR, separate issue is 25 EUR. MIDEM members and Society sponsors receive current issues for free. Scientific Council for Technical Sciences of Slovenian Research Agency has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials. Publishing of the Journal is cofinanced by Slovenian Book Agency and by Society sponsors. Scientific and professional papers published in the journal are indexed and abstracted in COBISS and INSPEC databases. The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™. |
Letna naročnina je 100 EUR, cena posamezne številke pa 25 EUR. Člani in sponzorji MIDEM prejemajo posamezne številke brezplačno. Znanstveni svet za tehnične vede je podal pozitivno mnenje o reviji kot znanstveno-strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinancirajo JAKRS in sponzorji društva. Znanstveno-strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC. Prispevke iz revije zajema ISI® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™.
Po mnenju Ministrstva za informiranje št.23/300-92 se šteje glasilo Informacije MIDEM med proizvode informativnega značaja.

Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 45, No. 3 (2015)

Content | Vsebina

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 45, No. 3 (2015), 175 – 179

Voltage-mode analog PID controller using a single z-copy current follower transconductance amplifier (ZC-CFTA)

Worapong Tangsrirat

Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Ladkrabang, Bangkok, Thailand

Abstract: This paper endeavours to design a proportional-integral-derivative (PID) controller based on the use of single z-copy current follower transconductance amplifier (ZC-CFTA). The developed PID controller consists of one ZC-CFTA, two truly grounded passive components and virtually grounded passive components. It does not require any passive component matching, and the realized controller parameters are adjustable electronically. The effects of parasitic elements and tracking errors of the ZC-CFTA are also investigated. Simulation results in PSPICE demonstrate the workability of the proposed PID controller.

Keywords: z-copy current follower transconductance amplifier (ZC-CFTA); proportional-integral-derivative (PID); analog controller; voltage-mode circuit

Analogni PID krmilnik v napetostnem režimu realiziran z enim dvo-izhodnim tokovnim sledilnikom, povezanim s transkonduktančnim ojačevalnikom (ZC-CFTA)

Izvleček: V tem članku si prizadevamo zasnovati proporcionalno-integralno-diferencialni (PID) krmilnik na osnovi enega samega dvo-izhodnega tokovnega sledilnika, povezanega s transkonduktančnim ojačevalnikom (ZC-CFTA). Razviti PID krmilnik je sestavljen iz enega ZC-CFTA, dveh zares ozemljenih pasivnih komponent in dveh navidezno ozemljenih pasivnih komponent. Parametri realiziranega krmilnika so elektronsko nastavljivi in ujemanje pasivnih komponent ni potrebno. Raziskani so tudi efekti parazitnih elementov in napake sledenja ZC-CFTA. Rezultati simulacij v PSPICE-u pokažejo izvedljivost predlaganega PID krmilnika.

Ključne besede: dvo-izhodni tokovni sledilnik, povezan s transkonduktančnim ojačevalnikom (ZC-CFTA); proporcionalni-integralni-diferencialni (PID) krmilnik; analogni krmilnik; vezje v napetostnem režimu

** Corresponding Author's e-mail: rworapong@gmail.com*

1 Introduction

The ubiquitous proportional-integral-derivative (PID) controllers are the most widely-used controllers in process industries, and gained widespread industrial acceptance for many decades [1]. This is owing to the attribute that they offer many good features, such as simplicity of design, low cost, robustness and wide applicability, as well as easy tunability of their parameters [2]. The enormous literature on PID process controllers includes a wide variety of design approaches based on different high-performance active elements, such as operational transconductance amplifiers (OTAs) [3], current differencing buffered amplifiers (CDBAs) [4], current-controlled current conveyors (CCCIIs) [5], second-generation current conveyors (CCIIs) [6]-[8], and current feedback operational amplifiers (CFOAs) [9]. In [3]-[5], the signal flow graph synthesis procedures for realizing analog PID controllers were presented. In active circuit realizations, they contain too many active

and passive components. The CCII can also be applied to construct PID process controllers, as demonstrated in [6]-[8]. However, at least two CCIIs and five passive components are required for these realizations. The work in [9] proposed a PID controller using a single CFOA. Although the circuit employs only one active component, it does not exhibit the feature of electronic tuning, and the passive components used in its construction are floating.

In 2008, the conception of the z-copy current follower transconductance amplifier (ZC-CFTA) has been introduced [10]. This device is a modified version of the conventional current differencing transconductance amplifier (CDTA) [11] by replacing the current differencing unit with a current follower and complementing the circuit with a simple current mirror for copying the z-terminal current. Therefore, the ZC-CFTA element is a cascade connection of the dual-output current follower and the operational transconductance amplifier. As a result, the capability of applications based on ZC-CFTAs is extended [12]-[14].

Our purpose in this study is to present an alternative circuit configuration for realizing an analog voltage-mode PID controller based on the use of the ZC-CFTA as an active element. The configuration uses only one ZC-CFTA, cooperating with four grounded passive elements, i.e. two truly grounded passive components and two virtually grounded passive components. The circuit also does not need passive element matching. Three realized parameters of the presented PID controller can be tuned to the desired valued by the transconductance (g_m) of the ZC-CFTA. In addition, the ZC-CFTA non-ideality effects including finite parasitic elements and transfer errors on the controller behavior are examined in detail. Also, PSPICE simulations are performed to demonstrate the performance of the presented controller circuit, and to verify the theoretical expectations.

2 ZC-CFTA Principle and Realization

The ZC-CFTA is a versatile active circuit building block, which is made by the cascade connection of two essential circuit blocks, i.e. a dual-output current follower at the front end, and an operational transconductance amplifier at the rear end. Fig.1 shows the electrical symbol and equivalent circuit of the ZC-CFTA. As shown in Fig.1, this device consists of a low-input-impedance current terminal (f) and three high-output-impedance current terminals (z, zc and x). The characteristic of an ideal ZC-CFTA can be represented by the following expression [12]-[14] :

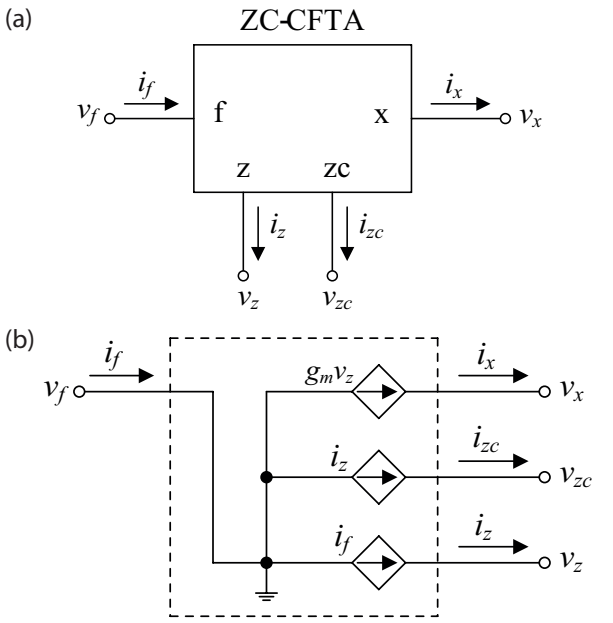


Figure 1: The ZC-CFTA.
(a) circuit symbol, (b) equivalent circuit.

$$i_{zc} = i_z = i_f \text{ and } i_x = g_m v_z \quad (1)$$

where g_m denotes the small-signal transconductance gain of the ZC-CFTA. In general, the value of g_m depends on the external supplied current.

The possible BiCMOS implementation of the ZC-CFTA used in this work is illustrated in Fig.2. Transistors Q_1-Q_7 act as a dual-output current follower that follows an input signal current (i_f) to output currents flowing through terminals z and zc (i_z and i_{zc}). Group of transistors Q_8-Q_{14} functions as an operational transconductance amplifier, which converts the impressed voltage at terminal z into the signal current at terminal x (i_x) by the transconductance g_m. From small-signal circuit analysis of this structure, the transconductance value g_m depends on an external biasing current I_O, and can be expressed as [14] :

$$g_m = \frac{I_O}{2V_T} \quad (2)$$

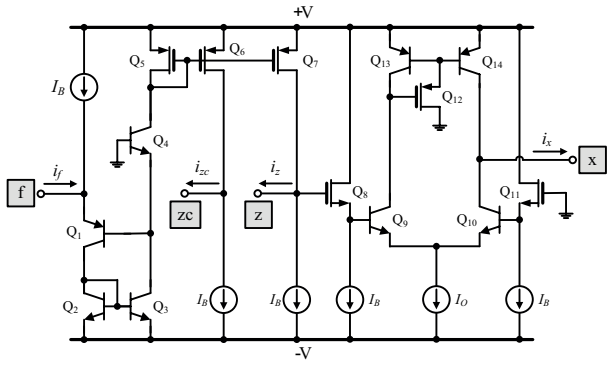


Figure 2: BiCMOS realization of the ZC-CFTA.

In addition, V_T is the usual thermal voltage, approximately 26mV at 27°C.

3 Proposed PID Controller Realization

The circuit implementation of the PID controller based on the use of the ZC-CFTA as an active component is shown in Fig.3. As can be seen, the proposed controller comprises one ZC-CFTA, two virtually grounded passive components (R_1 and C_1), and two truly grounded passive components (R_2 and C_2). These grounded passive elements can compensate for the parasitic impedances at their corresponding nodes. The circuit analysis of the proposed PID controller circuit in Fig.3 yields the following voltage transfer function :

$$\frac{V_{out}(s)}{V_{in}(s)}=\left(\frac{R_2}{R_1}+\frac{g_m R_2 C_1}{C_2}\right)+\frac{g_m R_2}{sR_1C_2}+sR_2C_1 \qquad (3)$$

In general, the voltage transfer function of an analog PID controller can be expressed as [15] :

$$\frac{V_{out}(s)}{V_{in}(s)}=K_p+\frac{1}{sT_i}+sT_d \qquad (4)$$

where K_p is the proportional gain, T_i is the integral time constant and T_d is the derivative time constant. Therefore, by comparing eq.(3) with eq.(4), the three parameters of the realized PID controller in Fig.3 are found out to be :

$$K_p=R_2\left(\frac{1}{R_1}+\frac{g_m C_1}{C_2}\right) \qquad (5a)$$

$$T_i=\frac{R_1C_2}{g_m R_2} \qquad (5b)$$

And

$$T_d=R_2C_1 \qquad (5c)$$

From eq.(5), the above three coefficients can be adjusted by appropriately setting the values of R_1, R_2, C_1, C_2 and g_m. It is further to be noted that the g_m-value can be used as a tool to tune the controller parameters for compensating the deviation from the ZC-CFTA non-ideality or the errors in passive component values.

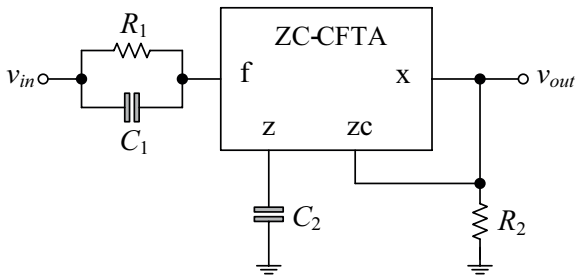


Figure 3: Proposed PID controller realization.

4 Non-ideal Performance Analyses

4.1 Tracking Error Effects

In non-ideal case, the current transfer from terminal f to terminals z and zc, as well as, the current at terminal x may differ from ideal values due to the current tracking error, and transconductance inaccuracy. Considering these errors, the terminal relationships of the non-ideal ZC-CFTA can be rewritten by :

$$i_{zc}=i_z=\alpha i_f \text{ and } i_x=\beta g_m v_z \qquad (6)$$

where α is the current tracking error, and β is the transconductance inaccuracy parameter. By repeating the analysis of the proposed PID controller circuit in Fig.3 and taking into account the parameters α and β of the ZC-CFTA, the controller parameters K_p, T_i and T_d can be obtained as :

$$K_p=\alpha R_2\left(\frac{1}{R_1}+\frac{\beta g_m C_1}{C_2}\right) \qquad (7a)$$

$$T_i=\frac{R_1C_2}{\alpha\beta g_m R_2} \qquad (7b)$$

And

$$T_d=\alpha R_2C_1 \qquad (7c)$$

As can be seen from eq.(7), the values of all PID controller parameters are slightly altered by the influences of the ZC-CFTA current tracking error and transconductance inaccuracy. To compensate for these small deviations, the g_m-parameter can be tuned by means of the ZC-CFTA bias current (I_O). On the other hand, if the controlled-gain current follower transconductance amplifier introduced in [16] is employed instead of the ZC-CFTA in Fig.3, the parameters α and β can be tuned by the controllable transfer gains to obtain the desired K_p, T_i and T_d values, or to compensate for the small errors that occur in their values. The inspection of eq.(7) indicates that the relative sensitivities of the three controller parameters with respect to the active and passive component values are found within unity in magnitude. In consequence, this controller circuit possesses low sensitivity performance.

4.2 Parasitic Element Effects

The practical model of the ZC-CFTA including essential parasitic elements is shown in Fig.4. As it is shown, the f-terminal exhibits the low-value serial parasitic resistance R_f and the z, zc and x-terminals exhibit large parasitic resistances R_z, R_{zc}, and R_x in parallel with low-value parasitic capacitances C_z, C_{zc} and C_x, respectively. When the circuit in Fig.3 is re-considered by taking the mentioned parasitic elements into account, the following assumptions can be made.

(a) Since the z-terminal is terminated by the external capacitor C_2, an extra parasitic pole ω_1 is introduced by R_z and C_2 (assuming $C_2 >> C_z$) at low frequencies, namely $\omega_1 \cong 1/R_zC_2$. For close to ideal operation at low frequencies, the operating frequency should be selected 10 times higher than ω_1. Thus, the low-frequency range of the proposed controller can be approximated as :

$$\omega \geq 10\omega_1 \cong \omega_L \tag{8}$$

(b) The external grounded resistor R_2 is connected in parallel with the parasitic impedances ($R_{zc}//C_{zc}$) and ($R_x//C_x$) of terminals zc and x. The extra pole ω_2, which is approximately equal to $\omega_2 = 1/(R_2//R_{zc}//R_x)(C_{zc}//C_x)$, appears only the high-frequency region of characteristic. Usually $R_2 << R_{zc}//R_x$, the pole ω_2 is located at about $\omega_2 \cong 1/R_2(C_{zc}//C_x)$. Thus, to obtain ideal response, the maximum operating frequency of the controller should be chosen as :

$$\omega \leq 0.1\omega_2 \cong \omega_H \tag{9}$$

(c) In conclusion, combining eqs.(8) and (9), the useful frequency range of the proposed PID controller circuit in Fig.3 can be defined simply as :

$$\omega_L \leq \omega \leq \omega_H \tag{10}$$

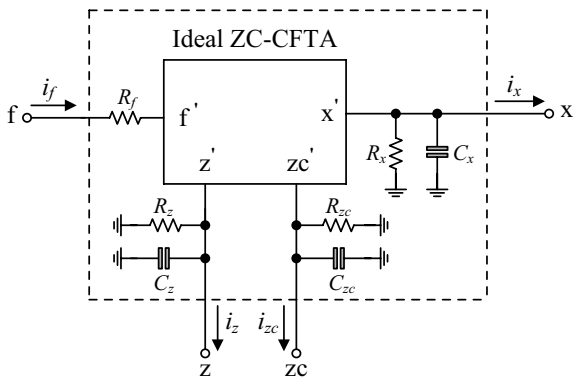


Figure 4: Non-ideal ZC-CFTA model including essential parasitic elements**.**

5 Simulation and Comparison of the Results

The performance of the proposed PID controller circuit in Fig.3 has been evaluated by means of PSPICE simulation. In simulations, the ZC-CFTA structure given in Fig.2 was characterized by 0.35-μm real BiCMOS process parameters. Transistor aspect ratios (W/L in μm/μm) were 7/0.35 and 14/0.35 for all the NMOS and PMOS transistors respectively. The circuit was biased with the following conditions: ±V = 1 V and I_B = 50 μA.

For our design example, the following active and passive component values were chosen: g_m = 1 mA/V (I_O = 52 μA), $R_1 = R_2$ = 1 kΩ and $C_1 = C_2$ = 1 nF. In this setting, the corresponding controller parameters were obtained as: K_p = 2, $T_i = 10^{-6}$ s and $T_d = 10^{-6}$ s. The total power consumption of the proposed controller is measured as approximately 23.7 mW. Fig.5 shows the ideal and the simulated frequency responses of the proposed PID controller circuit in Fig.3. As can be seen from the results, the ideal values and the simulation results are in agreement between 150 Hz and 1 MHz. It should be noted that the differences between the two responses in low- and high-frequency regions can be attributed to two extra parasitic poles ω_1 and ω_2, respectively.

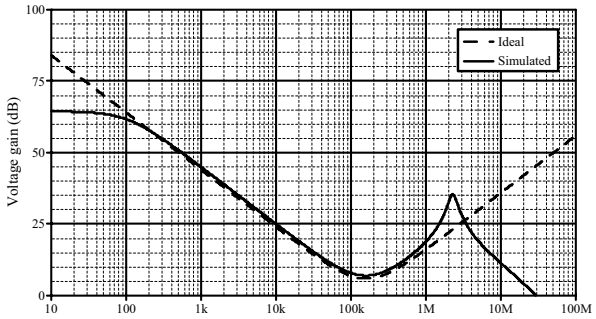


Figure 5: Ideal and simulated frequency responses of the proposed PID controller configuration of Figure 3.

To illustrate the time-domain characteristic of the proposed PID controller circuit, a 50-mV step signal voltage with 100-ns rise time is applied to the input of the circuit. Both ideal and simulated output voltage responses v_{out} are shown in Fig.6. From this result, an overall proportional action of the controller is obvious in the 0-100 ns period. At 100 ns, the sudden decrease in the controller output is due to the derivative action, since the input signal of the controller changes at a faster rate. After 100 ns, the action of the integral control mode is introduced. The controller output increases almost linearly since there is no change in the input for this period of time. As previously mentioned, the discrepancy between the ideal and the simulated results can be attributed to the parasitic impedances

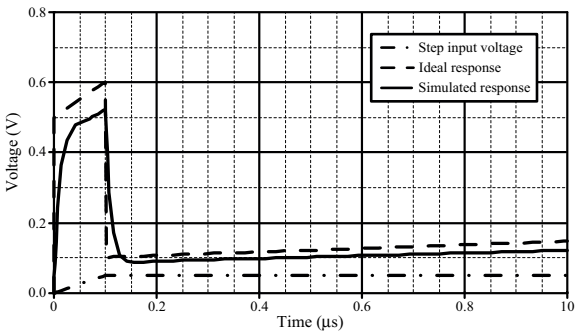


Figure 6: Step responses of the proposed PID controller configuration of Fig.3.

of the ZC-CFTA, most notably the finite port resistances R_z, R_{zc} and R_x.

6 Conclusions

In this paper, a simplified structure of the PID controller with single ZC-CFTA is introduced. The introduced PID controller has been realized using a minimum number of passive components, without requiring a passive component-matching constraint. The controller gains are adjustable by tuning the g_m-value of the ZC-CFTA. The effects caused by the parasitic elements and the transfer errors of the ZC-CFTA are also discussed. Simulation results confirm the theoretical analysis.

7. Acknowledgements

This work was supported by the Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL). The authors are also thankful to the reviewers for their valuable comments and helpful suggestions, which substantially improved the quality of the manuscript.

8 References

1. K. Astrom, T. Hagglund, *PID Controllers : Theory, Design and Tuning*, *2nd edition*, North Carolina, Instrument Society of America, 1995.
2. S. Bennette, "Development of the PID controller", *IEEE Control Systems Mag.*, vol.13, no.6, pp.58-65, 1993.
3. C. Erdal, A. Toker, A. Acar, "OTA-C based proportional-integral-derivative (PID) controller and calculating optimum parameter tolerances", *Turk. J. Elec. Engin.*, vol.9, no.2, pp.189-198, 2001.
4. A. U. Keskin, "Design of a PID controller circuit employing CDBAs", *Int. J. Elect. Eng. Educ.*, vol.43, no.1, pp.48-56, 2006.
5. C. Erdal, H. Kuntman, S. Kafali, "A current controlled conveyor based proportional-integral-derivative (PID) controller", *J. Electrical Electron. Eng.*, vol.4, no.2, pp.1243-1248, 2004.
6. S. Minaei, E. Yuce, S. Tokat, O. Cicekoglu, "Simple realization of current-mode and voltage-mode PID, PI and PD controllers", *Proc. IEEE Int. Symp. Industrial Electron.*, Croatia (2005) 20.
7. E. Yuce, S. Tokat, A. Kizilkaya, O.Cicekoglu, "CCII-based PID controllers employing grounded passive components", *Int. J. Electron. Commun. (AEU)*, vol.60, no.5, pp.399-403, 2006.
8. E. Yuce, S. Tokat, S. Minaei, O. Cicekoglu, "Low-component-count insensitive current-mode and voltage-mode PID, PI and PD controllers", *Frequenz*, vol.60, no.3-4, pp.29-33, 2006.
9. M. Sagbas, M. Koksal, U. E. Ayten, "Design of dominantly proportional PID controller using a single commercially available active component", *Proc. Int. Conf. Telecom. Signal Process.*, Italy, pp.427-430, 2013.
10. D. Biolek, R. Senani, V. Biolkova, Z. Kolka, "Active elements for analog signal processing: classification, review, and new proposals", *Radioengineering*, vol.17, no.4, pp.15-32, 2008.
11. D. Biolek, "CDTA- Building block for current-mode analog signal processing", *Proc ECCTD'03*, vol. III. Krakow, Poland, pp.397-400, 2003.
12. N. Herencsar, J. Koton, K. Vrba, I. Lattenberg, "Current follower transconductance amplifier (CFTA) - A useful building block for analog signal processing", *J Active Passive Electronic Devices*, vol.6, no.3-4, pp.217-229, 2011.
13. J. Satansup, W. Tangsrirat, "Realization of current-mode KHN-equivalent biquad filter using ZC-CFTAs and grounded capacitors", *Indian J Pure & Appl Phys*, vol. 49, pp. 841-846, 2011.
14. W. Tangsrirat, P. Mongkolwai, T. Pukkalanun, "Current-mode high-Q bandpass filter and mixed-mode quadrature oscillator using ZC-CFTAs and grounded capacitors", *Indian J Pure & Appl Phys*, vol. 50, no. 8, pp. 600-607, 2012.
15. R. C. Dorf, R. H. Bishop, *Modern Control Systems, 11th-edition*, New Jersey, Pearson prentice Hall, 2008.
16. W. Tangsrirat**,** "G_m-Realization of controlled-gain current follower transconductance amplifier", *The Scientific World Journal*, vol. 2013, Article ID 201565, 8 pages, 2013. doi:10.1155/2013/201565.

Arrived: 24. 09. 2014
Accepted: 02. 08. 2015

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 45, No. 3 (2015), 180 – 187

Distributed Energy Efficient Clustering Algorithm for Wireless Sensor Networks

Muruganantham Arunraja, Veluchamy Malathi, Erulappan Sakthivel

Department of Electrical and Electronics, Anna University, Regional Centre, Madurai

Abstract: Wireless sensor networks (WSN) are powered by finite energy source like batteries, which imposes stringent energy boundaries. Clustering of nodes avoids redundant message transmissions over the network. Thus conserves energy, communication bandwidth and achieves scalability. Here we propose a Distributed Energy Efficient Clustering Algorithm (DECA), a deterministic clustering approach where Cluster Heads (CHs) are selected based on their residual energy and priority using passive clustering technique. Nodes then associate with the CH with least communication cost and high residual energy. This method achieves longer life span than the previous energy efficient clustering algorithms in both homogeneous and heterogeneous networks. DECA has extended the WSN life span to 30% in the homogeneous environment and 50% in the multi-level heterogeneous environment.

Keywords: Wireless sensor networks; energy conservation; distributed clustering

Energijsko učinkovit algoritem distribuiranega grozdenja brezžičnih senzorskih omrežij

Izvleček: Brezžična senzorska omrežja (WSN) so napajana z omejenim virom napajanja, kot so baterije z strogimi omejitvami. Groznenje vozlišč odpravi prenose redundančnih sporočil, kar omogoča varčevanje energije in pasovne širine ter omogoča širitev. V članku predlagamo energijsko učinkovit algoritem distribuiranega grozdenja (DECA), deterministični način grozdenja, pri katerem je glava grozda (CHs) temelji na preostanku energije in prioriteti, z uporabo pasivne tehnike grozdenja. Vozlišča so združena z CH z minimalno ceno komunikacije in visokim ostankom energije. Z razliko od prejšnjih rešitev omenjena metoda omogoča daljšo energijsko neodvisnost v homogeneih in heterogenih omrežjih. DECa omogoča 30 % daljšo delovanje WSN v homogenih okoljih in 50 % veščjo v večnivojskih heterogenih okoljih.

Ključne besede: brezžično senzorsko omrežje; varčevanje z energijo; distribuirano grozdenje

** Corresponding Author's e-mail: researcharunraja@gmail.com*

1 Introduction

As the wireless sensor nodes are self-contained systems with limited energy resource, the life span is finite. By conserving the on board energy, the system life span can be increased, hence ensuring continued service. Clustering is an efficient hierarchical routing approach to conserve energy, where only a set of nodes performs the routing operation and therefore reducing the amount of redundant transmissions and collisions.

Due to its reduced deployment cost, smaller form factor and increased computing power, WSN are an inevitable element of today's industrial, military and medical establishments. Due to their ease of installation and lesser maintenance they proliferated to various disciplines. WSN consists of autonomous sensor nodes that are spatially distributed over the specific region to report about one or more parameters of interest. In a conventional WSN, densely deployed nodes sense data from the environment, pre-process it and communicate it to the sink node.

As the sensor nodes are self-contained systems with limited energy resource, the life span is finite. Most of the WSNs are deployed in hostile environments, where recharging is a difficult task. By conserving the on board energy, the system life span can be increased, thus ensuring continued service.

The tenacity of WSN is to collect accurate data for longer time span. Data accuracy is improved by increasing sampling frequency. Increased sampling

frequency, results in increased energy cost, thus reduces the life span. This imposes a conflict between data accuracy, and energy efficiency. The solution for the problem is derived by estimating the temporal correlation between the node data in time domain. The temporal correlation intimates the amount of redundant data communicated. By reducing the redundant data both accuracy and energy efficiency can be achieved. Temporal correlation can further be exploited to predict the future data from historical data. By effectively modeling the temporal correlation of a measured signal, a substantial amount of data transmission can be reduced.

In the physical space nearer sensors measure almost equal values due to their close proximity. In a denser network, nodes generate a hefty amount of spatially redundant data. Clustering of nodes can filter out the spatially redundant data locally. Clustering suffers inefficiencies when two or more CHs happened to be in close proximity or when the data load is not equally balanced between CHs. In certain clustering approaches, the clustering process itself consumes significant energy, due to its communication overheads.

The proposed clustering approach addresses the above mentioned problems, thus makes clustering more efficient. Here the clustering is initiated by a node that proclaims itself as CH. The neighbors of the node join the cluster as cluster members. Each node would like to become CH, but the proclamation delay of a node is inversely proportional to its weight. This passive clustering process reduces the clustering overhead, by avoiding data sharing between contending nodes. The cluster size is increased with respect to the distance from the base station, so as to balance the load between near and remote CHs. The one hop neighbors of the CH are disqualified from the contention to become CH, to avoid the formation of nearby CHs. Then from the rest of the nodes highest weight node initiates clustering. This continues until all the nodes are clustered.

Clustering suffers inefficiencies when two or more CHs happened to be in close proximity or when the data load is not equally balanced between CHs. In certain approaches, the clustering process itself consumes significant energy, results in less efficiency. An ideal clustering process should have least overheads and should assure energy efficient data collection along with uniform distribution of CHs.

2 Related works

Numerous works done on energy efficient clustering of WSN, yet most of the work concentrates on energy efficiency and data accuracy. Long term coverage of region of interest is not addressed in any of the works. The distributed sensor network is said to be efficient only if it covers a larger portion of the region of interest for a longer time span. The proposed work considers energy efficient coverage as its major point.

Energy conservation in WSN is analyzed by different approaches [1]. Some methods take up energy efficient routing as one of the tools for energy balancing between wireless nodes [2]. Some methods employ MAC based schemes, which ON/OFF the node circuitry in appropriate time slots so that energy expense can be drastically reduced [3].

Spatial correlation among the sensor nodes is used to reduce the data transmission by employing clustered aggregation schemes. Different kinds of clustering methods are listed by Younis et al [4]. Clustering is done in WSN in different application to achieve different goals.

Clustering may be centralized [5], where the base station collects the node parameters and announces the cluster heads and their cluster members. This one is effective for the small scale network. For large scale networks, distributed clustering methods [6] suit well, where the clustering, decision is made by individual sensor nodes by acquiring only local information from one hop neighbors. Clustering may also consider a single hop [7] or multi hop networks [8]. Usage of heterogeneous nodes [9] reduces the overhead during CH election.

LEACH [7] is one of the earliest and most sought clustering methods for energy efficiency WSN. The problem with leach is a random selection of CH which results in proximate CHs and unbalanced load distribution. There are other works [10], which depicts the node degree as one of the selection criteria for CH selection.

In [11], clustering is done by identifying similarity between sensor data. The nodes send their data to the base station, where the nodes are assigned to the appropriate cluster based on data similarity.

Different clustering approaches use different parameters for CH selection, based on the selection criteria, the algorithms can be divided. Deterministic algorithm [12] takes into account of node degree and node id etc., where these parameters are fixed during the deployment itself. Adaptive algorithms [13] consider the residual energy of node, mobility etc. These parameters vary over the operational span of the network. Hybrid algorithms [14] consider both the

deterministic and adaptive parameters for cluster head selection.

Several works done on exploiting temporal correlation of data, where linear regression methods are used to calculate the temporal relation between time series generated by sensors [15]. The schemes suffer from reduced accuracy and lack of adaptability towards dynamic variations in input signal. In [16], ARIMA based methods are used to predict the sensor data from previous values. Saintini et al [17] proposed a dual prediction scheme using LMS based adaptive filters. The advantage of this method is its ability to converge the prediction, without any prior model [18]. The scheme can still be improved by adapting the internal parameters.

Most of the existing literature either concentrates on spatial correlation based data aggregation or on temporal correlation based data reduction. DECA exploits spatio-temporal correlation between sensory data for energy efficient data collection and also it maintains maximum level data integrity. The work involves simple and computationally light weight algorithms, which makes the implementation simpler and less energy consuming in terms of computational cost. To achieve energy efficiency, numerous clustering approaches have been proposed. LEACH [7] selects CH on a random probability, which results in proximate CHs and unbalanced load distribution. SEP [19] assigns a weighted probability to each node based on its initial energy, where advance nodes get more chances to become a CH. In DEEC [20],CH formation is based on the residual energy of the entire network and residual energy of the node that wants to become a CH. Since SEP and DEEC are probabilistic clustering approaches, there might be cases when two CHs are selected in close vicinity of each other, increasing the overall energy expense of the network. Secondly, the number of CH nodes generated is not fixed, hence in some rounds it may be more or less than the preferred value.

Deterministic protocols eliminate uncertainty over the number of CHs and CH election. The weighted clustering algorithm [21] selects a node as a CH based on its weight. The weight of an individual node signifies the remaining battery energy, degree, mobility, and distances with the neighbors. Distributed clustering algorithm (DCA) uses application based weights of a node to select it as the CH [22]. Both the algorithms necessitate extensive control messages to construct a cluster, which makes them suitable only for a small wireless sensor network.

DECA is an energy aware passive clustering algorithm, where the clustering is performed without communicating nodal parameters. The DECA algorithm considers only self-estimating parameters for CH selection, thus a single announcement is enough to select a CH. The selection parameters are highly dynamic and support in better distribution of the load among sensor nodes. This forms energy efficient clusters with minimal clustering overheads.

3 Deca

The proposed DECA constructs the energy efficient clusters in two phases. The DECA consists of the following functional modules:

- An energy aware passive clustering approach that reduces clustering overheads and assures uniform energy distribution.
- A node association approach based on residual energy and communication cost of a CH.

The proposed work makes the following assumptions before designing the energy efficient protocol.

- Topology is static
- All nodes are aware of their location
- All the cluster members can reach CH in one hop
- CH can reach the base station in one hop or multiple hops

The actual purpose of creating clusters is to reduce the energy consumption of the sensor nodes and the bandwidth requirement for the network. The clusters in the network are attributed by a single CH, connected to multiple sensor nodes nearby. The sensor nodes transmit their data to the cluster head, which aggregates the data and forwards it to the base station. This process moderates the energy expense of the nodes and decreases the probability of data collisions. The energy model of the conventional cluster is given as

$$\sum_{i\in N}\sum_{j\in N}\{ly_{ij}(D_{ij}+E+E_{DA})+l_{ag}F_i x_i \quad (1)$$

Where y_{ij} = 1, if node 'j' is a cluster member of the CH node 'i'.

y_{ij} = 0, otherwise.

l, the length of data packet from cluster member to CH.

E, energy spent for receiving a data bit.

E_{DA}, data aggregation energy

l_{ag}, length of aggregated data packet

x_i=1, if node 'i' is a CH.

x_i=0, otherwise.

The data transmission energy from the cluster member to CH is given as

$$D_{ij} = \begin{cases} E + \varepsilon_{fs} d_{ij}^2 & ;if\ d_{ij} < d_0 \\ E + \varepsilon_{mp} d_{ij}^4 & ;if\ d_{ij} > d_0 \end{cases}. \quad (2)$$

Where d_{ij} the distance from sensor node 'i' to sensor node 'j'.

d_0, the threshold distance.

ε_{fs}, amplifier energy

ε_{mp}, amplifier energy

The data transmission energy from CH to Base Station is given as

$$F_i = \begin{cases} E + \varepsilon_{fs} f_i^2 & ;if\ f_j < d_0 \\ E + \varepsilon_{mp} f_i^4 & ;if\ f_i > d_0 \end{cases} \quad (3)$$

Where f_i, the distance from CH node 'i' to Base station.

3.1 Energy Efficient CH election

In the proposed work, higher energy nodes are elected as CH to attain energy efficiency. To distribute the load uniformly among the nodes, node priority is considered. Both the components constitute for the weight of the node. To reduce the energy consumption during clustering process, the passive clustering method has been proposed, where the proclamation delay is defined as the function of node's weight.

3.1.1 Weight Calculation of Node

In this work, each node is assigned with specific weight based on its suitability to become CH. The election of the CH is done on the basis of the largest weight among the neighbors. This means that a node becomes a CH or a cluster member, depending on its own and one hop neighbor's weights.

In WSN, there are several heuristics for selecting CHs. Node energy, node degree, distance from the Base Station(BS), node ID and cumulative time for which the node acted as CH (node priority) are the prominent heuristics. Since CHs are overloaded with multiple tasks, the rate of energy depletion is also high. Hence the CH elected should have high residual energy. Thus, for an energy efficient clustering approach, residual energy is the major indicator for the dominant set of nodes in both homogeneous and heterogeneous (energy) networks. Acquiring residual energy is again an internal task, doesn't need any communication.

3.1.2 Passive Clustering

In passive clustering, Cluster head is selected based on "first declaration wins" rule, therefore the node that first proclaims becomes the CH. In the earlier works, the proclamation delay is random. Random delay may results in selection of low energy nodes as CH, hence decreases the energy efficiency of the system. In the proposed work, to elect most appropriate nodes, the proclamation delay is made inversely proportional to the node's weight. Once the proclamation delay expires, the node proclaims itself as CH. If a node hears a proclamation before the expiration of its proclamation delay, it refrains itself from the contention to become CH. The waiting time T_w of node n is given as

$$T_w(n) = \frac{K}{E_{res}(n)} \quad (4)$$

Where k is a constant;

3.2 Node Association

When the node proclaims as CH, it advertises its residual energy and location information along with the proclamation. If a non CH node receives multiple proclamations, the advertisement serves as a key factor for selecting the most appropriate CH. The proclamation message format is indicated in table.1.Based on this information, a non-CH node estimates CH's compatibility towards it.

Table.1: CH proclamation format

CH ID	CH Residual Energy	CH Location

Due to diverse communication overheads and functionality, there is an asymmetry of energy between various nodes. Hence a good design for data collection should not put heavy burdens on low energy sensor nodes. Instead, the heavy burdens should be assigned to the high energy sensor nodes. The CH residual energy component helps in identifying the CH with highest energy near the sensor nodes.

If the CH is situated between the sensor node and BS, the communication cost will be reduced considerably. The CH location component helps in calculating the communication cost of the node to forward the data to BS through that CH. Thus the CHs location information has a crucial role in node association. Based on this information a non-CH node selects a CH, so that the total data transmission distance is minimized. The communication cost through a CH is estimated from the node to CH distance d_{toCH} and CH to BS distance d_{CHtoBS}. The

goal of the node associated process is to minimize the total distance.[Min ($d_{toCH+}d_{CHtoBS}$)]

The node selects CH with highest residual energy and lowest communication cost. The CHs aptness is the ratio between the residual energy of the CH and communication cost through this CH to BS.

If a node 'i' receives 'n' CH proclamations, the node estimates the weight of each CH as

$$W_{CH}(n_i) = E_{res}(n) / F(n_i) \quad (5)$$

Where $F(n_i)$, communication cost of node 'i' through CH (n) to BS.

$$F_n = LE_{elect} + L \in_{fs} d^2 \quad (6)$$

L: size of data packet

E_{elect}: Energy consumed by RF Module

$\in_{fs}$: RF Amplifier energy

d: Total distance from the node to BS

The node then associates with the highest weight CH in its vicinity. The CH with minimum residual energy is elected by very few nodes. This avoids repeated loading of few CH nodes.

4 Results and discussion

Here we evaluate the performance of DECA protocol using MATLAB. The proposed work has been simulated on a network consists of 100 randomly distributed nodes in a 100m X 100m field. We assume the base station is in the center of the sensing region. The radio parameters used in our simulations are shown in Table 2. The proposed DECA approach is compared with other energy efficient clustering protocols like LEACH, SEP and DEEC. The life time of nodes and total packets transmitted are estimated on both homogeneous and heterogeneous nodal energy levels. The life time is classified into stable period (until first node dies) and lasting period. The effectiveness of the clustering is measured by the ratio between stable period and unstable period.

Table.2: Simulation Parameters

Parameter	Value
E	50nJ/bit
ε_{fs}	10 pJ/bit/m2
ε_{mp}	0.0013 pJ/bit/m4
E_o	0.5 J
E_{DA}	5 nJ/bit/message
d_0	70 m
Message size	4000 bits
P_{opt}	0.1

In a homogeneous environment all the nodes are assigned with equal energy. DECA elects CHs based on residual energy and cumulative time the node acted as CH. Thus, in the homogeneous environment, DECA efficiently balances the load between multiple nodes and achieves longer stable period [Fig.1]. The stability period is elongated to 1110 rounds, compared to 910 rounds of LEACH protocol that has the second longest stable period.

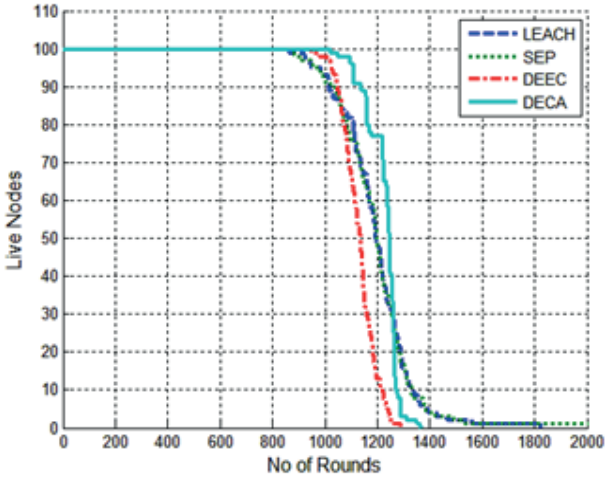


Figure 1: Node lifetime in homogeneous network

We then observe the performance of LEACH, SEP, DEEC and DECA under two different two-level heterogeneous networks. Fig.2.shows the performance when fraction of advanced nodes 'm' kept at 0.2 and additional energy factor 'a' set as 3. In another scenario 'm' is set at 0.3 and 'a' as 2. The unstable region of SEP and LEACH are also larger than our DECA protocol; it is because the advanced nodes die more slowly than the normal nodes in SEP and LEACH.

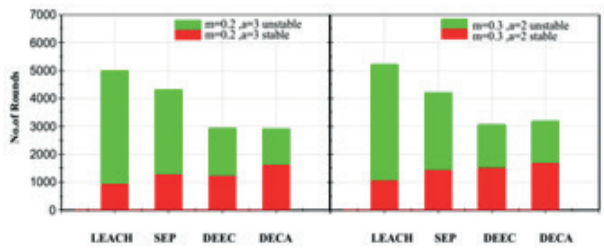


Figure 2: Stability period comparison in two-level heterogeneous network

For multi-level heterogeneous networks, the initial energy of nodes is randomly distributed in [E0,4E0].

The DECA protocol exhibits longer life span in the heterogeneous energy environment than all the protocols compared. The stability period is elongated from 1500 rounds (DEEC) to 2200 rounds as shown in fig.3. This is because LEACH treats all the nodes without discrimination. SEP has longer stability period than LEACH just because of discriminating nodes according to their initial energy. DEEC take initial energy and residual energy into account at the same time. The longer life span of DECA is attributed to the energy efficient selection of CHs and minimized data transmission distance.

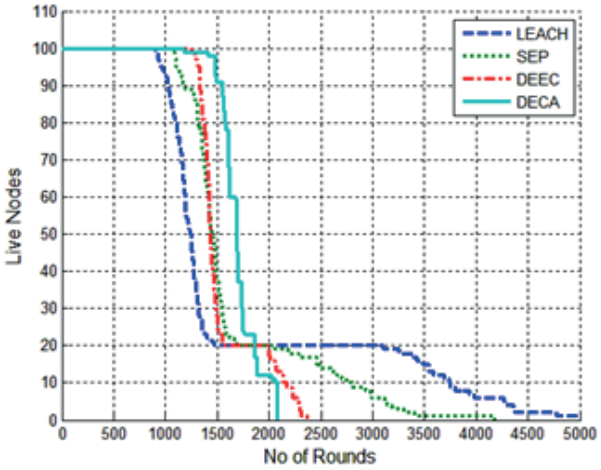


Figure 3: Node lifetime in multi-level heterogeneous network

We also examine the sensitivity of DECA to the degree of heterogeneity in the network by increasing the 'm' value from 0.1 to 0.9 and 'a' from 0.5 to 5.Being an energy-aware deterministic protocol, DECA outperforms other energy efficient clustering protocols. The difference between the stability period of DECA and other protocols increases with an increased fraction of advanced nodes 'me' as indicated in Fig.4.

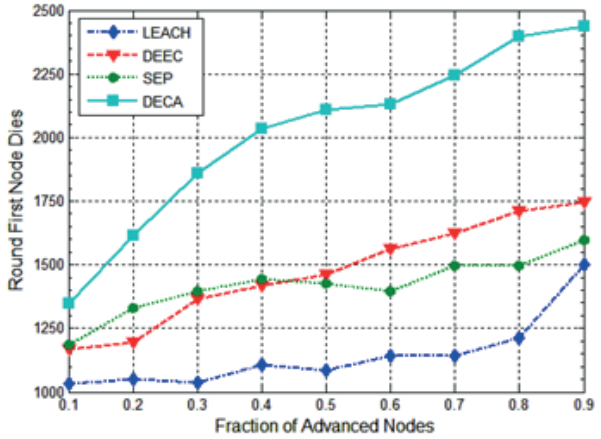


Figure 4: Round of First Node Dies for Different m when α= 2

The performance of DECA is observed to be close to that of an ideal upper bound obtained by distributing the additional energy of advanced nodes uniformly over all nodes in the sensor field. DECA is more resilient than LEACH in judiciously consuming the extra energy of advanced nodes. Thus DECA yields a longer stability period for higher values of extra energy as in Fig. 5.

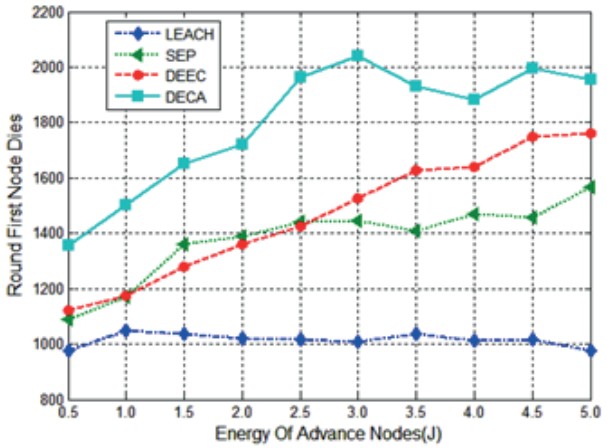


Figure 5: Round of First Node Dies for Different αwhen m=0.3

Fig.6. Shows the comparison of every protocol for number of packets that are sent to BS. Result shows

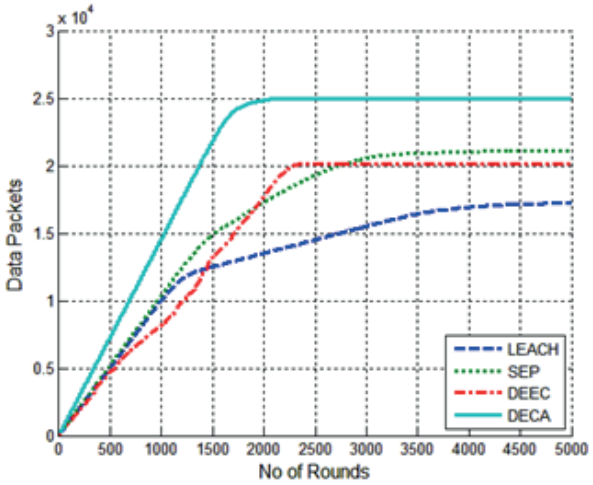


Figure 6: Packets sent to the BS Vs. Rounds

That DECA has highest successful data rate, as compare to other routing protocols. DECA achieves highest data rate along with longer stability period.

5 Conclusion

Our contribution involves a deterministic CH election protocol (DECA) that holds the distributed property of probabilistic models. Secondly, a novel node association technique is introduced through which

nodes join with the most appropriate CHs that are having least communication cost and high energy. The node association part, assures load is taken up by only high energy nodes. The network's energy expenses are reduced by shorter data paths. Thus DECA achieves uniform distribution of CH and longer stability period. DECA has extended the WSN life span to 30% in the homogeneous environment and 50% in the multi-level heterogeneous environment. The work shows good results in various kinds of heterogeneous environments. Future work involves construction of multi-level clusters using temporal correlations between sensor data.

6 References

1. G Anastasi, M Conti,M Di Francesco, A Passarella, "Energy conservation in wireless sensor networks: A survey", Ad Hoc Networks 7 (3), 537-568, 1041, 2009.
2. J. Heo, J. Hong, and Y. Cho, "EARQ: energy aware routing for real-time and reliable communication in wireless industrial sensor networks," IEEE Transactions on Industrial Informatics, vol. 5, no. 1, pp. 3–11, 2009.
3. D. Ganesan, A. Cerpa, W. Ye, Y. Yu, J. Zhao, and D. Estrin, "Networking issues in wireless sensor networks," Journal of Parallel and Distributed Computing, vol. 64, no. 7, pp. 799–814, 2004.
4. Ossama Younis, Marwan Krunz, Srinivasan Ramasubramanian: Node clustering in wireless sensor networks: recent developments and deployment challenges. IEEE Network 20(3): 20-25 (2006)
5. Tillaport, S. Thammarojsakul, T. Thumthawatworn and P. Santiprabhob, »An Approach to Hybrid Clustering and Routing in Wireless Sensor Networks«, In Proc. IEEE Int. Conf. Aerospace, 2005, pp. 1-8.
6. Chuan-Ming Liu, Chuan-Hsiu Lee, and Li-Chun Wang. Distributed Algorithms for Data-Gathering in Wireless Mobile Sensor Networks. Journal of Parallel and Distributed Computing, 67(11):1187-1200, 2007. (SCI)
7. W. R. Heinzelman, A. Chandrakasan, and H. Balakrishnan, "Energy-efficient communication protocol for wireless microsensor networks," in Proceedings of the 33rd Annual Hawaii International Conference on System Siences (HICSS '00), January 2000.
8. P. Ding, J. Holiday, A. Celik, "Distributed energy efficient hierarchical clustering for wireless sensor networks", IEEE international conference on distributed computing in sensor systems (DCOSS'05), Marina Del Rey, CA, June 2005.
9. M. Gerla, and J. T. C. Tsai, "Multi cluster, mobile, multimedia radio network", Wireless Networks, vol.1, issue: 3, 1995, pp.255-265.
10. G. Gupta and M. Younis, "Performance evaluation of load-balanced clustering in wireless sensor networks," in Proceedings of the 10th International Conference on Telecommunications (ICT '03), 2003.
11. Chong Liu, Kui Wu and Jian Pei, "An Energy-Efficient Data Collection Framework for Wireless Sensor Networks by Exploiting Spatiotemporal Correlation," IEEE T PARALLEL DISTR, Vol. 18, No. 7, July, 2007.
12. D. J. Baker and A. Ephremides, "The Architectural Organization of a MobileRadio Network via a Distributed Algorithm," IEEE T COMMUN, Vol. 29, no. 11, 1981, pp. 1694–1701.
13. FuadBajaber and IrfanAwan, "Adaptive decentralized re-clustering protocol for wireless sensor networks," JCOMPUT SYST SCI , pp. 282–292,2011.
14. "HEED: A Hybrid, Energy-Efficient, Distributed Clustering Approach for Ad Hoc Sensor Networks," IEEE T MOBILE COMPUT, vol. 3, no. 4, pp. 366-379, October 2004.
15. arlos.Carvalho, Danielo.G.Gomes, Nazim Agoulmine and José Neuman de Souza, "Improving Prediction Accuracy for WSN Data Reduction by Applying Multivariate Spatio-Temporal Correlation," Sensors ,Vol.11,no.11,pp. 10010–10037,2011.
16. Guorui Li and Ying Wang, "Automatic ARIMA modeling-based data aggregation scheme in wireless sensor networks," EURASIP J WIREL COMM,vol.85,2013.
17. Santini S and Römer K, "An adaptive strategy for quality based data reduction in wireless sensor networks," In: 3rd international conference on networked sensing systems, pp. 29-36, Chicago, USA, 31 May-2 Jun 2006
18. F. Akyildiz, W. Su, Y. Sankara subramaniam, and E. Cayirci, "Wireless sensor networks: a survey," Computer Networks, vol. 38, no. 4, pp. 393–422, 2002.
19. G. Smaragdakis, I. Matta and A. Bestavros, "SEP: A stable election protocol for clustered heterogeneous wireless sensor networks", Boston University Computer Science Department, (2004).
20. L. Qing and Qingxin Zhu, "Design of a distributed Energy-Efficient Clustering algorithm for heterogeneous Wireless sensor Networks", Computer Communications, pp. 2230-2237, 2006.
21. M. Chatterjee, S.K. Das, D. Turgut, WCA: a Weighted Clustering Algorithm for mobile Ad Hoc networks, Cluster Computing 5 (2) (2002) 193–204.

22. S. Basagni, Distributed clustering algorithm for ad-hoc networks, in: Proceedings of the International Symposium on Parallel Architectures, Algorithms, and Networks (I-SPAN), Fremantle, Australia, June 1999.
23. A. Ghosh and S. K. Das, "Coverage and connectivity issues in wireless sensor networks: a survey, "Pervasive and Mobile Computing, vol. 4, no. 3, pp. 303–334, 2008
24. B. Wang, H. B. Lim, and D. Ma, "A survey of movement strategies for improving network coverage in wireless sensor networks," Computer Communications, vol. 32, no. 13-14, pp. 1427–1436, 2009.
25. M. Cardei and J. Wu, "Energy-efficient coverage problems in wireless ad-hoc sensor networks," Computer Communications, vol. 29, no. 4, pp. 413–420, 2006
26. D. Bokal, B. Brešar and J. Jerebic, A generalization of Hungarian method and Hall's theorem with applications in wireless sensor networks, Discrete Appl. Math. 160 (2012) 460-470
27. Péter Schaffer, Károly Farkas, Ádám Horváth, Tamás Holczer, Levente Buttyán: Secure and reliable clustering in wireless sensor networks: A critical survey. Computer Networks 56(11): 2726-2741 (2012)
28. Badong Chen, Yu Zhu, Jinchun Hu, José C. Príncipe: Δ-Entropy: Definition, properties and applications in system identification with quantized data. Inf. Sci. 181(7): 1384-1402 (2011)
29. A. Khalili, M. A. Tinati, and A. Rastegarnia, "Steady-State Analysis of Incremental LMS Adaptive Networks with Noisy Links", IEEE Transactions on Signal Processing, vol. 59, no. 5, pp. 2416 – 2421, May 2011.
30. A. Rastegarnia, M. A. Tinati, and A. Khalili, "Performance Analysis of Quantized Incremental LMS Algorithm for Distributed Adaptive Estimation", Signal Processing, vol. 90, pp. 2621-2627, Aug. 2010.

Arrived: 03. 01. 2015
Accepted: 12. 05. 2015

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 45, No. 3 (2015), 188 – 194

Design of an active inductor based LNA in Silterra 130 nm CMOS process technology

Mohammad Arif Sobhan Bhuiyan, Jia Xien Chew, Mamun Bin Ibne Reaz, Noorfazila Kamal

Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, Bangi, Selangor, Malaysia

Abstract: In this paper, an active inductor based CMOS low noise amplifier (LNA) has been illustrated for 2.4 GHz ISM band RF receivers. The proposed LNA has three stages: the common gate amplifier, the active inductor and the output buffer. The LNA is designed in Silterra 130-nm CMOS process. It operates at 1.2V supply voltage and exhibit a high gain (S21) of 33dB and reverse isolation (S12) of -33.1dB. The power dissipation of the LNA is only 1.51mW with 8.51 dB noise figure and 35.5dB IIP3. In the proposed LNA, active inductor circuit replaces the usual passive spiral inductor to keep the size of the chip area at 0.0004mm2. Such an LNA will be a better choice for high performance, fully integrated, low cost and low power RF receivers.

Keywords: CMOS; LNA; Active Inductor; RF

Zasnova nizko šumnega ojačevalnika na osnovi aktivne dušilke s Silterra 130 nm CMOS tehnološkim procesom

Izvleček: V članku je prikazan CMOS nizko šumni ojačevalnik (LNA) na osnovi aktivne dušilke za RF sprejemnike v ISM frekvenčnem območju 2,4 GHz. Predlagani LNA je sestavljen iz treh stopenj: ojačevalnik s skupnimi vrati, aktivna dušilka in izhodni ojačevalnik. LNA je načrtovan za Silterra 130-nm CMOS proces. Deluje pri napajalni napetosti 1,2 V, ima veliko ojačenje (S21) 33 dB in majhno povratno ojačenje (S12) 33,1 dB. Poraba moči znaša le 1,51 mW, šumno število ima 8.51 dB in IIP3 35,5 dB. Pri predlaganem LNA aktivna dušilka nadomešča običajno pasivno spiralno dušilko, s čimer dosežemo velikost vezja le 0,0004 mm2. Tak LNA bo boljša izbira za visokozmogljive v celoti integrirane nizkocenovne RF sprejemnike nizkih moči.

Ključne besede: CMOS; LNA; aktivna dušilka; RF

** Corresponding Author's e-mail: asobhan@eng.ukm.my*

1 Introduction

The continuous advancement in CMOS technology allows the researchers to fabricate fully on-chip transceivers without compromising the performance issues. Therefore, the current trend is to design low power compact devices by eliminating bulky board level off-chip components. This resulted low power, small size and low cost wireless terminals for different applications such as RFID, Bluetooth, Zigbee, Wi-Fi, WLAN devices etc. [1, 2, 3]. The size and performance of such devices largely depend on the size and performance of their transceivers. Therefore performance enhancement of such wireless transceivers is very important.

An LNA is typically the first active amplification block of an RF receiver, as shown in Fig. 1. Its performance greatly affects the overall receiver performance. Main performance parameters of a typical LNA are: input matching S_{11} (dB), reverse isolation S_{12} (dB), gain S_{21} (dB), output matching S_{22} (dB), NF (dB), IIP3 (dBm), power dissipation (mW), Chip size (mm^2) etc. The type of mixture with which LNA is to be used is very important to determine the necessary trade off among the performance criteria. For example, the requirement for gain of the LNA, when used with active mixture, can be relaxed as such a mixer provides active gain while consuming some dc power. But its power consumption needs to be lowered to compensate for the power

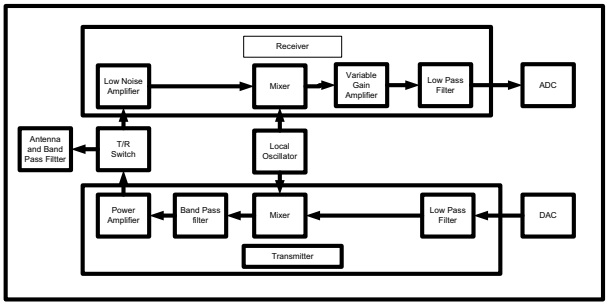


Figure 1: Analog front of a 2.45 GHz RF transceiver.

consumption from the active mixer. With a relaxed gain, the LNA should have good noise figure (NF) to avoid degrading the overall receiver NF.

LNA is a one of the crucial blocks of an RF receiver which deals with very low power signal. LNAs are usually designed in two common topologies: Common-Source LNA (CSLNA) and Common- Gate LNA (CGLNA) [3, 4]. These two topologies use passive inductors which results in larger chip area and thus increased cost. Generally, the parasitic effects and losses related to the substrate degrade the total performance of the LNAs. Therefore, various techniques have been used by the researchers to improve the LNA performance. Current-reuse technique in CGLNA is usually utilized to better the transconductance but the area becomes larger due to the usage of bulky passive inductors [5]. Noise cancelling techniques are also used to decrease the NF, but it suffers from high frequency effects [6, 7] and low voltage gain [8, 9].

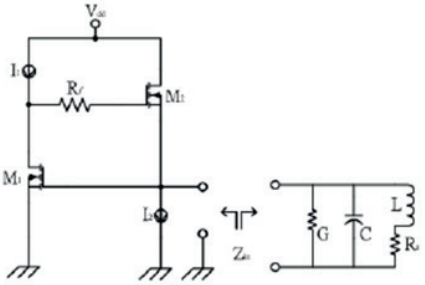


Figure 2: Typical single ended gyrator-C active inductor and its equivalent circuit [1].

To overcome the margins, active inductor based band pass filters have been introduced. Active inductors manage to constantly tune to protect temperature or process variations. Beyond that, active inductor only takes about 1% until 10% of passive active inductor area which can produce smaller chip area and cost [10]. Besides they also have higher inductance value, wide frequency tuning range and higher quality factor which are essential for different circuit designs [11]. However, inductor-less LNA although reduces chip size but can cause high power dissipation [12, 13]. Fig. 2 shows a typical single ended gyrator-C active inductor and its equivalent circuit.

In this paper, an LNA design with low power dissipation and high gain for 2.4 GHz ISM band RF receivers has been proposed in Silterra 130-nm CMOS process. The inductor-less approach made the LNA design compact and power efficient.

2 The active inductor based LNA

In LNA design, CGLNA is preferred for its excellent input impedance matching characteristics [14]. The conventional common gate amplifiers commonly utilize resistive feedback which experiences parasitic capacitance effect and relatively higher power dissipation at higher frequencies. The proposed LNA is structured in three interconnected modules, as illustrated in Fig. 3, Common gate amplifier, Active inductor and Common drain amplifier. The signal will first pass through a common gate amplifier and then to the active inductor and lastly into a common drain amplifier which will act as a buffer.

Figure 3: Modules of the active inductor based LNA.

2.1 Common Gate Amplifier

The proposed circuit of a common gate amplifier is shown in Fig. 4. Here, M11 acts as an active resistor instead of source resistor. The transconductance of the transistor M8 is the input impedance of the amplifier. The common gate amplifier topology is a good choice because of its high reverse isolation and good impedance matching characteristics and thus any extra impedance matching network is not required. Biasing voltage (V2) is applied to make sure that the transistor M8 is always in saturation mode.

2.2 Active Inductor

A double feedback active inductor used in the proposed LNA is shown in Fig. 5 [15].

The negative feedback action involves the long tail pair transconductor consisting of transistors M3, M_4 and sources J_2, J_3 whereas the source J_4 converts the input voltage to a current for the internal capacitor of transistor M2, c_{gs2} to be charged. While the transistor M_2 converts back the capacitor voltage to the input current. For positive feedback action, the long-tail

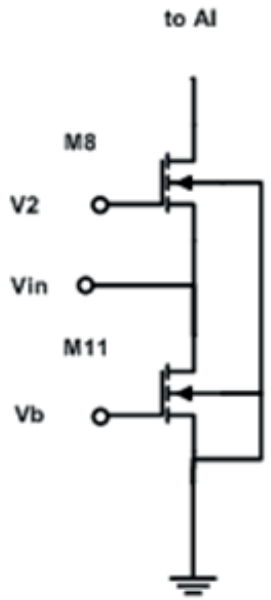


Figure 4: Common gate amplifier.

pair transconductor converts the input voltage into an oppositely directed current which enters the input node. It realizes a negative resistance of $-2/g_{m3}$ (where $g_{m3} = g_{m4}$) that is parallely tied with the inductor. For the proposed topology, the currents in the unwanted coupling routes have been balanced. For a voltage applied at the input of the inductor, the currents

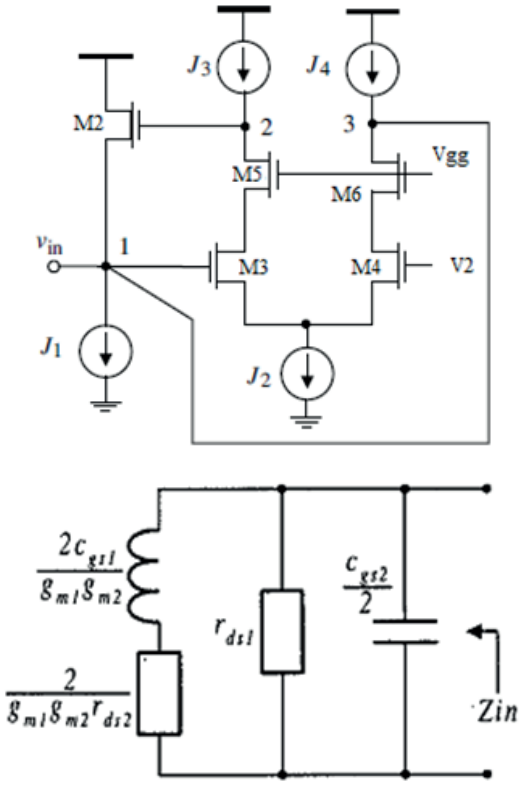


Figure 5: Double feedback active inductor and its equivalent circuit [15].

through c_{gs2} and c_{gs3} are combined at the common-source terminals of M3 and M4 which acts as virtual ground potential. This current follows the drain of the transistor M4 as the current flowing through c_{gs4} is insignificant because of the almost zero signal voltage across it. Consequently, the currents through the unwanted coupling paths are counterbalanced and therefore, the drain current of M_1 makes the input current and the inductor loss is taken out.

The Q-enhancement technique is applied in almost all modern on-chip inductor circuits in order to compensate their high losses. Generally, the Q factor of the regulated cascode active inductor circuit is relatively low because of its equivalent parallel resistive loss which is not compensated by the negative feedback operation. Therefore, in our proposed circuit, the currents in the undesirable coupling paths have been compensated. For an input voltage to the inductor, the currents flowing through cgsl and cgs2 are summed at the common-source terminals of M2 and M3 which exhibit virtual ground potential. This current will then flow out of the drain terminal of M3 because the current in cgs3 is negligible since the signal voltage across it is almost zero. Moreover, from the first-order small-signal analysis, it is evident that, if gm3 = gm2 and cg3 = cgs2, the active inductor will become lossless (infinite Q). But in practice, it is not possible for some factors like finite drain-source resistances, other parasitic capacitances of the transistors etc.

2.3 Common Drain Amplifier

The common drain amplifier is also known as source follower or a buffer. It is widely utilized in final stage of LNA design due its small output impedance to achieve a better output impedance matching for the LNA. A simple buffer is added to the final stage of the proposed LNA design. Its schematic is shown in Fig. 6 and transistor M9 is used as active resistor. Transistor M10 is used as a common drain amplifier.

2.4 Proposed Active Inductor Based LNA

Finally, all three sub-circuits are tied together and the whole schematic circuit of the proposed LNA is shown in Fig. 7. In this circuit, the enhanced active inductor has been formed by transistors M3 to M6. The common gate amplifier is formed by transistor M8. On the other hand, M0, M1 and M7 act as constant current source. Finally, M9 and M10 comprise the output buffer.

It is obvious that amplifiers add noise and distortion to the desired signal. Therefore, noise analysis is very important for every amplifier circuit. The noise figure gives a measure of the amount of noise added to a

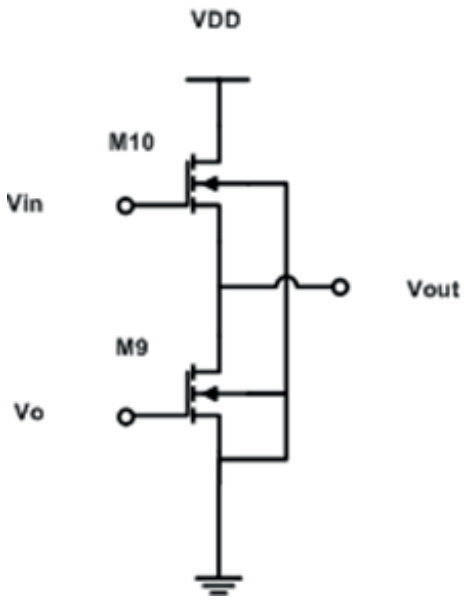


Figure 6: Common drain amplifier.

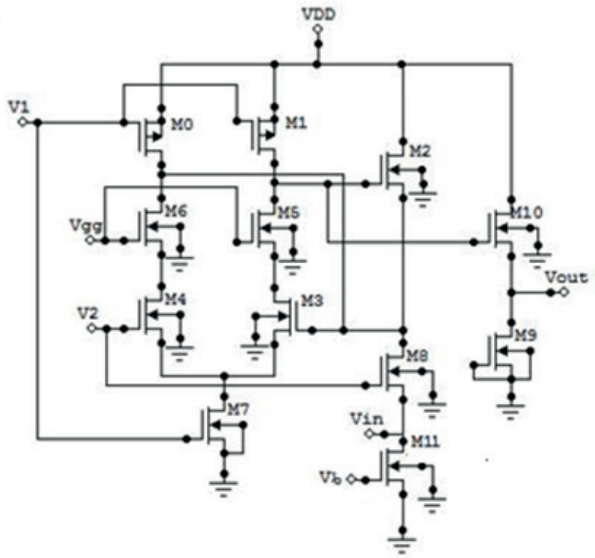


Figure 7: Schematic of the active inductor based LNA.

signal transmitted through the network. For any circuit, therefore, the noise figure minimization is also very important. But it is also inevitable that maximum gain and minimum noise cannot be obtained at the same time.

For the noise analysis of the active inductor, let us consider that it is terminated with a resistance, R, the value of which is greater than (1/gm1) and also neglecting the flicker noise of the transistors used, the spot noise figure can be approximately expressed as:

$$NF \approx 10\log\left[1+\frac{2}{3r}\left(\frac{1}{gm2}+\frac{1}{gm3}+\frac{1}{gm4}+\frac{gm5}{gm3^2}\right)\right] \quad (1)$$

It can be seen from (1) that the noise figure of the inductor can be minimised by maximising the small-signal transconductances of M2, M3 and M4 while the transconductances of M5 and M6 should be kept at minimum values. Increasing the transconductances of M2, M3 and M4 corresponds to the increasing of parasitic capacitances hence a trade-off between noise performance and frequency response. On the other hand, reducing the transconductances of M5 and M6 seems to be not a critical problem in compromising the performance since they serve as just current followers.

Generally, the noise effects in a common-gate topology include both the thermal and the flicker noise. Thus, the noise factor of the common-gate amplifier can be approximately showed as

$$NF \approx \frac{K}{C.f}\left(\frac{gm1\,1^2+gm8^2}{(WL)m8}+2\frac{gm2^2}{(WL)m2}\right)+ \\ +\ \frac{2}{3}\left(\frac{gm1\,1^2+gm8^2}{(WL)m8}+2\frac{gm1\,1+gm8+2gm2}{gm8^2}\right) \quad (2)$$

where K is a process-dependent constant, C is the gate capacitance of the MOSs, and f is the operating frequency of the amplifier.

The final stage is the common-drain configuration which is nothing but a source follower. The noise factor of this stage is derived as:

$$NF \approx \frac{2}{3}\left(\frac{1}{gm10}+\frac{1}{gm10^2.R}\right) \quad (3)$$

Where R is the resistance of the active resistor (M9).

If we consider all the transconductances (gm) same, it will be obvious that a higher value of gm can improve the noise figure but it will also increase the total power consumption. Moreover, the increased parasitic capacitances of the transistors will degrade the performance specially in high frequencies. Therefore, a trade off has been made.

3 Results and discussion

The proposed LNA circuit has been verified by using the simulation tool ELDO RF in Mentor Graphics environment. The process parameters for the transistors used in this work correspond to Silterra 130-nm CMOS technology. The power supply for the circuit is 1.2V.

The operating temperature of the circuit is 300K while the noise temperature is set to 290K for measuring the LNA noise figure. The voltage biases for the LNA are V1=0.59V, V2=0.40V and Vgg =0.79V. The transistor sizes are given in Table I.

Table 1: Components used in the LNA circuit

Transistor	Width (μm)	Length (μm)
M0, M1	1.27	0.13
M2	0.84	0.13
M3, M4	9.11	0.13
M5,M6	0.36	0.13
M7	12.15	0.13
M8	3.66	0.13
M9	25	0.13
M10	4.58	0.13
M11	8	0.13

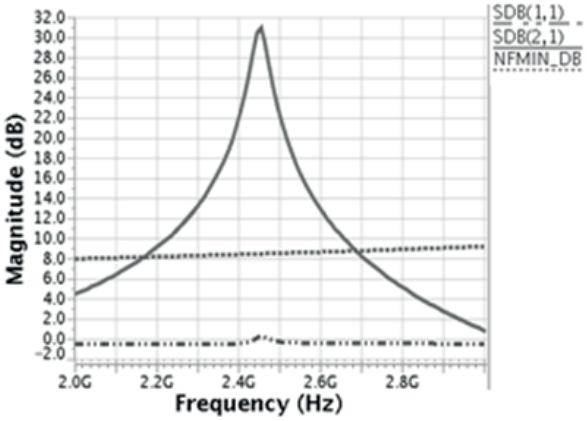


Figure 8: Gain (S21), reflection coefficient (S11) and minimum NF.

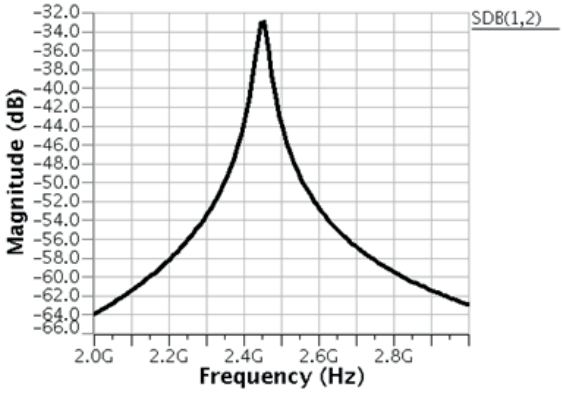


Figure 9: Simulation result for reverse isolation (S12).

The simulation results are shown in Fig. 8 and Fig. 9. At the center frequency of 2.45GHz, the LNA is able achieve 33dB of forward gain (S_{21}) and a minimum noise figure (NF) of 8.51dB. The reverse isolation (S_{12}) is -33.1dB whereas the reflection coefficient (S_{11}) is 0.2dB. The power dissipation of the LNA is measured to be 1.51mW. The IIP3 is measured to be 35.5dB. The bandwidth of the proposed LNA is 28 MHz. The transient output voltage is shown in Fig. 10.

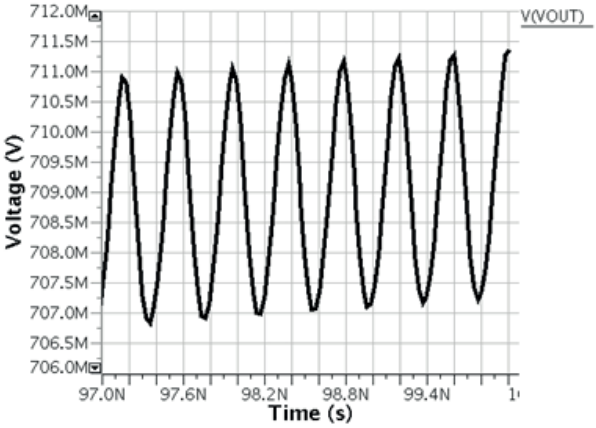


Figure 10: The transient output voltage waveform.

A transistor (M11) commonly seen to be used with the CG topology to stabilize the transconductance of the amplifying transistor is removed. The existence of that transistor shows no significant effect on the LNA performance during the simulation. The bias voltage for transistor M9 is best when it is grounded. By grounding the bias voltage of transistor M9, no changes on the center frequency is observed. However, an improvement in the LNA gain is observed.

All of the transistors are operating at saturation region except for transistor M9. By changing the transistor width of M2, M3, M4, M8 and M10, the LNA center frequency, gain and minimum NF can be tuned. However, the higher the center frequency, the lower the gain is. It is also observed that the minimum NF increases as the gain increases. But, the gain increases steeper than the minimum NF. The transistor widths are tuned to achieve maximum gain while maintaining an acceptable minimum NF.

The layout of the LNA is designed using Mentor Graphics IC Design environment. The transistor sizes are optimized to obtain a balance between chip area and performance. The transistors are positioned in such a way that it is as compact as possible to achieve a small chip area which is measured at 0.0004 mm^2. The layout of the LNA is shown in Fig. 11.

The proposed active inductor based LNA is compared with other previously published active inductor based LNA design in Table II. This work has the highest gain and lowest power consumption while also being the smallest LNA. It also shows better linearity as evident

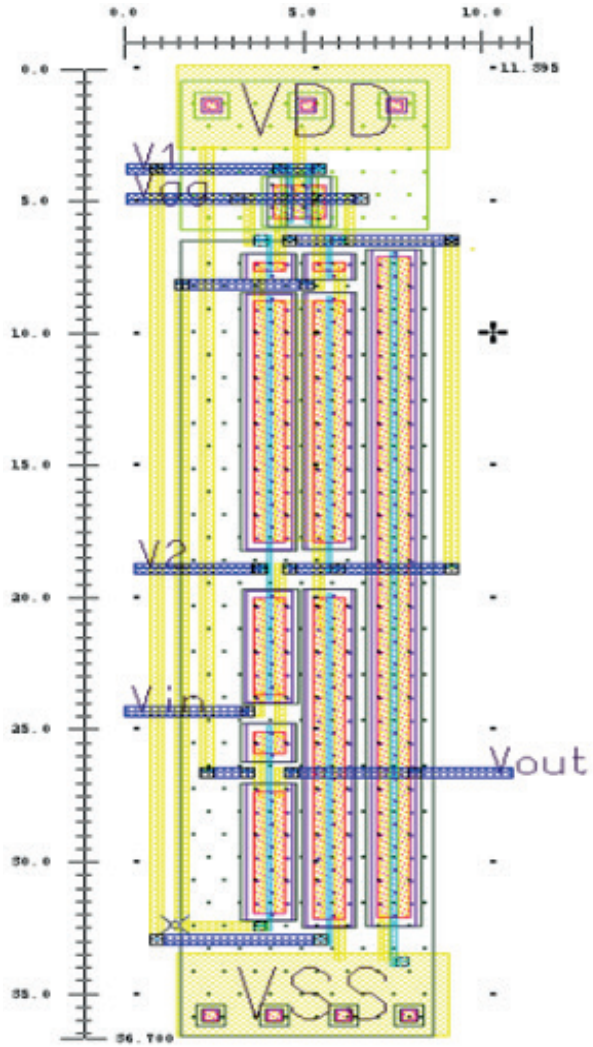


Figure 11: The core layout of the LNA (11.9 x 36.7) mm^2

from iip3 value. The low power consumption is due to the fact that less number of MOSFETs used in the design and the lower supply voltage when compared with other works. However, this work suffers from relatively higher noise figure due to the simple common gate topology used for the amplification and also for using smaller sized transistors.

Table 2: Performance comparison

	This work	[16]	[17]	[18]	[19]	[20]	[21]
Gain, S_{21} (dB)	30.7	11.2	22	14	11.8	19	15
Frequency (GHz)	2.45	2.0-11.2	0.8-2.5	0.37- 2.18	2.3-15.2	1-5	3.2-6.3
Noise Figure (dB)	8.51	2.0-4.0	3.02	3.55-4.5	1.9-3.8	2.1	0.95
Power Consumption (mW)	1.51	13.5	19.6	14.58	13.3	4.2	4.7
IIP3(dB)	35.5	-	-	-10	-	-	-
Supply Voltage	1.2	1.2	1.8	1.8	1.2	1.2	1.8
CMOS Process (nm)	130	130	180	180	130	180	180
Chip Area (mm2)	0.0004	0.09	0.03	0.04	0.093	-	-

4 Conclusion

In this paper, a low power compact design of LNA is proposed using Silterra 130-nm CMOS technology. It exhibits high forward gain (S_{21}) of 33dB, high reverse isolation (S_{12}) of -33.1 dB and high IIP3 of 35.5 dB at 2.45GHz. The LNA operates at supply voltage of 1.2V and consumes only 1.51mW of power. However, the LNA shows a competative NF of 8.51dB. In this design passive spiral inductors are avoided to keep the size very small at 0.0004 mm^2. Such an LNA will be suitable for high performance, fully integrated, low cost and low power RF receivers.

5 Acknowledgment

This work is supported by the research grant Economic Transformation Programme (ETP-2013-037) from Universiti Kebangsaan Malaysia and the Ministry of Science, Technology and Innovation (MOSTI) respectively.

6 References

1. M. A. S. Bhuiyan, M. B. I. Reaz, J. Jalil and L. F. Rahman. Design of a nanoswitch in 130 nm CMOS technology for 2.4 GHz wireless terminals. *Bulletin of the Polish Academy of Sciences Technical Sciences,* 62(2), pp.399-406, 2014.
2. M. I. B. Idris, M. B. I. Reaz and M. A. S. Bhuiyan. A low voltage VGA for RFID receivers. *IEEE International Conference on RFID Technologies and Applications,* pp. 1-4, 2013.
3. M. A. S. Bhuiyan, M. B. I. Reaz, J. Jalil, L. F. Rahman and T. G. Chang. Design trends in fully integrated 2.4 GHz CMOS SPDT switches. *Current Nanoscience,* 10(3), pp. 334-343, 2014.
4. R. M. Weng, C. Y. Liu and P. C. Lin. A low-power full-band low-noise amplifier for ultra-wideband receivers. *IEEE Transaction on Microwave Theory and Techniques,* 58(8), pp. 2077-2083, 2010.

5. M. Khurram and S. M. R. Hasan. A 3-5 GHz current-reuse gm-boosted CG LNA for ultra wideband in 130 nm CMOS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* 20(3), pp. 400-409, 2012.
6. F. Bruccoleri, E. A. M. Klumperink and B. Nauta. Wide-band CMOS low-noise amplifier exploiting thermal noise cancelling. *IEEE Journal of Solid-State Circuits,* 39(2), pp. 275-282, 2004.
7. Y. H. Yu, Y. S. Yang and Y. J. Chen. A compact wideband cmos low noise amplifier with gain flatness enhancement. *IEEE Journal of Solid-State Circuits,* 45(3), pp. 502-509, 2010.
8. Z. Wang, K. S. Yeo and K. Ma. An inductorless and capacitorless LNA with noise and distortion cancelation. *Computer Research and Development (ICCRD),* 3, pp. 270-274, 2011.
9. K.H. Chen and S. I. Liu. Inductorless Wideband CMOS low-noise amplifiers using noise-cancelling technique. *IEEE Transactions on Circuits and Systems I: Regular Papers,* 59(2), pp. 305-314, 2012.
10. H. Aljarajreh, M. R. Rifin, M. Mamun, S. Amin, and W. M. D. W. Zaki. low noise amplifiers in RFID systems, *Journal of Engineering and Applied Sciences*, 8, pp. 21-28, 2013.
11. C. Andriesei, L. Goras, F. Temcamani, and B. Delacressoniere, Wide tuning range active RF bandpass filter with MOS varactors, *Romanian Journal of Information Science and Technology*, 12, pp. 485-495, 2009.
12. F. Belmas, F. Hameau and J. M. Fournier. A low power inductorless LNA with double Gm enhancement in 130 nm CMOS. *IEEE Journal of Solid-State Circuits,* 47(5), pp. 1094-1103, 2012.
13. S. V. Krishnamurthy, K. El-Sankary, E. El-Masry, Noise-cancelling CMOS active inductor and its application in RF band-pass filter design, *International Journal of Microwave Science and Technology*, 2010, pp. 1-8, 2010.
14. H. J. liu, Z. Li and M. Zhang. A 2.4 GHz 1V low power LNA in subthreshold region, *3rd International Conference on Multimedia Technology ICMT 2013),* pp. 191-199, 2013.
15. U. Yodprasit and J. Ngarmnil. Q-enhanced technique for RF CMOS active inductor. *Proceedings IEEE International Symposium Circuits Systems,* 5, pp. 589-592, 2000.
16. M. .M. Reja, I. Filanovsky and K. Moez. A CMOS 2.0-11.2 GHz UWB lna using active inductor circuit. *IEEE International Symposium Circuit and Systems,* pp. 2266-2269, 2008.
17. H.B. Kia, A.K. Aain, I. Grout and I. Kamisian. A reconfigurable low-noise amplifier using a tunable active inductor for multistandard receivers. *Circuits, Systems, and Signal Processing,* 32(3), pp. 979-992, 2012.
18. M. Gao, Y. Wang, Y. Wang and D. Guo. Design of wideband CMOS LNA with active inductor and using noise-canceling technique. *3rd International Conference on Anti-counterfeiting, Security, and Identification in Communication, 2009 (ASID 2009),* pp. 262-265, 2009.
19. V. K. Bhardwaj, A. Agarwal and H. Kumar. CMOS LNA based on tunable active inductor for UWB applications. *2012 2nd Interanational Conference on Power, Control and Embedded Systems,* pp. 1-3, 2012.
20. J. Manjula and S. Malarvizhi. Low power low noise tunable active inductor for narrow band lna design. *International Journal of Computer Applications*, 47(17), pp. 39-43, 2012
21. M. I. Malek and S. Saini. Improved two stage ultra-wideband cmos low noise amplifier with out band rejection using low noise active inductor. *2015 International Conference on Signal Processing and Communication Engineering Systems (SPACES-2015),* pp. 157-161, 2015.

Arrived: 14. 01. 2015
Accepted: 18. 08. 2015

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 45, No. 3 (2015), 195 – 203

Digital Signal Processing for a Multi-Channel Chemical Sensor Interface

Mario Trifković, Dušan Raič, Drago Strle

University of Ljubljana, Faculty for Electrical Engineering, Ljubljana, Slovenia

Abstract: This paper presents digital signal processing for a miniature, multi-channel, multi-sensor detection system, based on chemically functionalized COMB micro-capacitors and low noise integrated analog electronics. The presented system is capable of detecting traces of different molecules in the air. Currently, it is possible to detect less than 3ppt of target molecules in the atmosphere at room temperature in a 1 Hz bandwidth. For such multi-channel measurements with extreme requirements regarding sensitivity, it is necessary to have the appropriate analog signal processing electronics, as well as digital signal processing hardware, algorithms, and software. The complete architecture of the DSP part of a multi-channel sensor measurement system is explained, together with some simulation and the measured results.

Keywords: Digital Signal Processing DSP, decimation filter, FPGA, measurement of capacitance changes, measurement system

Digitalno signalno procesiranje več-kanalnega merilnega sistema za merjenje kapacitivnosti kemično modificiranih COMB senzorjev

Izvleček: Članek opisuje digitalno signalno procesiranje miniaturnega, večkanalnega detekcijskega sistema, ki temelji na kemično modificiranih COMB senzorjih, integriranem nizko-šumnem analognem integriranem vezju ter vezju za digitalno procesiranju signalov. Predstavljen detekcijski sistem zaznava različne molekule v zraku v izjemno majhnih koncentracijah; detekcijski nivo pri sobni temperaturi znaša 3 molekule TNT med 1012 molekulami nosilnega plina pri pasovni širini 1Hz. Pomemben gradnik več-kanalnega senzorskega merilnega sistema s skrajnimi zahtevami glede občutljivosti, je tudi primerno digitalno procesiranje signalov, ustrezna arhitektura, algoritmi in pomožni programi, ki jih predstavljamo v članku skupaj s rezultati nekaterih pomembnih simulacij ter nekaterimi merilnimi rezultati.

Ključne besede: Digitalno Signalno Procesiranje DSP, CIC decimacijski filter, FPGA, merjenje spremembe kapacitivnosti, merilni sistem

** Corresponding Author's e-mail: mario.trifkovic@fe.uni-lj.si*

1 Introduction

Vapor detection systems already exist on the market. Chemo-mechanical sensors, initiated in the mid-1990s are based on a cantilever where adsorption of the target molecules on a modified surface bends the cantilever [1]. However, position measurement is difficult because of changing temperature, pressure, sensor vibration, etc. A differential capacitance comb-shaped (COMB) sensor and associated low noise electronics provide much lower sensitivity to the environmental influences. In this work, we present the DSP (Digital Signal Processing) part of a multi-channel detection system based on the measurements of the capacitance difference between modified (chemically treated, i.e. functionalized) and reference (untreated) capacitors [2]. The primary role of DSP is to extract useful information from the ΣΔ modulator bit-stream. As an important part of the complete detection system, it must be designed properly to get optimal results in as short time as possible, without introducing additional noise.

This paper is organized as follows. A general description of the entire measurement system is given in Section 2 with a short explanation of the analog signal processing module implemented on the ASIC (Application–Specific Integrated Circuit). Section 3 describes a 30-channel digital signal processor, while

Section 4 describes its implementation on the FPGA. The user interface and some measurement results are presented in Section 5 while the conclusions are given in Section 6.

2 Measurement system

A simplified block diagram of the signal processing electronics and data processing software running on the PC is shown in Figure 1. The whole measurement system is basically a lock-in amplifier [2] built from: low noise, analog front-end (AFE) electronics; digital front-end (DFE) control logic and the DSP. The AFE and DFE are integrated into the ASIC (application specific integrated circuit) designed in 0.25um BCD (BIPOLAR-CMOS-DMOS) process, while the DSP is currently realized on the FPGA. The AFE consists of necessary analog electronic components [2],[3] which are programmable, so that different gains, frequencies, and excitation signals for the sensors can be adjusted. The AFE configuration is set by DFE through a Serial Peripheral Interface (SPI). The existing ASIC is capable of processing the signals from two differential sensors. Each sensor must be calibrated, since the initial difference of two capacitors in one differential sensor can reach up to 10%. Therefore, a programmable capacitor array is implemented on the AFE part, which is connected in parallel to each sensor's capacitor. The programmability range of the calibration capacitors is from 1fF to 64fF in steps of 1fF.

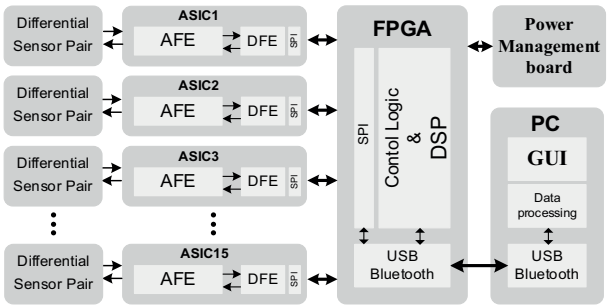


Figure 1: Measurement system block structure

The measurement results of each sensor are proportional to the capacitance difference caused by adsorption of the target molecule to the modified sensor. During calibration, in a natural atmosphere without traces of the target molecules, we calibrate the difference between each differential capacitor and bring the result close to zero. In this way the dynamic range of the measurement channel is increased so that higher channel gains and excitation voltages are possible. The multi-channel measurement system consists of 15 ASICs, each with two differential sensors; thus a 30 – channel measurement system is implemented. Each digital signal from the AFE carries the information of the capacitance difference. Signals from all sensors are connected to the FPGA, where DSP algorithms extract the information. The results of the DSP processing are sent to the PC via Bluetooth or USB interface, where further signal processing prepares the results for the presentation and storage.

The decisive parts regarding the sensitivity of the entire measurement system are differential comb capacitors and low noise electronics, which must be capable of detecting a low number of adsorbed target molecules on the surface of the functionalized capacitor [2]. The block diagram of one ASIC channel including two sensors is shown on Figure 2 [2],[3]. Two differential sensors can be connected to one measurement channel.

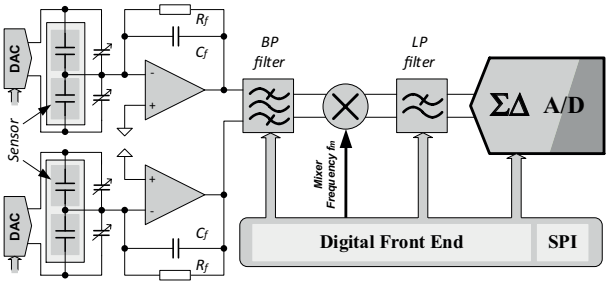


Figure 2: Block diagram of the ASIC including two sensors [2],[3].

Sensors are driven by square-wave signals V_s with slightly different frequencies. The difference in charges from the sensor is transformed into the voltage using a low noise charge amplifier with the help of the excitation signals. The output voltage of the charge amplifier can be calculated according to (1).

$$V_{cho}(s) = V_s \cdot \frac{\Delta C}{C_f} \cdot \frac{s}{1/(C_f \cdot R_f) + s} \tag{1}$$

The frequencies are selected well above the *1/f* noise corner frequency of the charge amplifier. The amplitude and frequency of the excitation signals are fully programmable. The output signal of the charge amplifier V_{cho} is band-pass filtered and amplified. The signal contains the main spectral components from two sensors and corresponding higher harmonics due to square-wave excitation signals. Therefore, the analog mixer generates the differences and sums of all main and harmonic spectral components. The differences are $f_{o1} = f_{s1} - f_m$ for the first sensor, and $f_{o2} = f_{s2} - f_m$ for the second. Low frequency signals are amplified, while high frequencies and the remains of the higher harmonics from the mixing products are

attenuated by a programmable analog low-pass filter. The resulting signal is finally quantized with a second order Σ-Δ A/D converter, implemented in the AFE part of the ASIC [2],[3]. The described AFE structure enables the possibility of using one analog channel for more sensors, avoiding the influence of the DC offset voltage and the *1/f* noise.

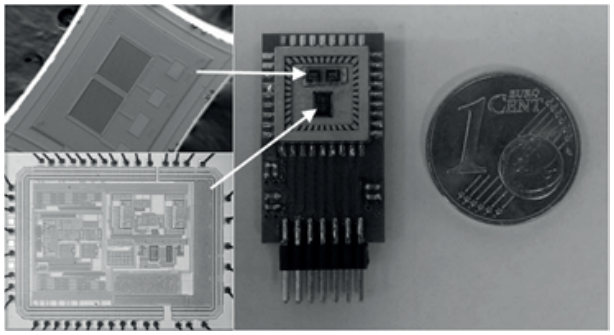


Figure 3: System in Package (SiP) measurement board: (left) COMB differential sensor and ASIC. (right) measurement board.

The SEM micrograph of a differential COMB capacitive sensor and photomicrograph of the ASIC is shown on the left side of Figure 3. The PCB with one ASIC and two differential sensors as a System In Package (SiP) is presented on the right side of Figure 3; for a size comparison an 1 Euro-cent coin is added. The ASIC and sensor sizes are 2.5×2mm and 1.2×1.5mm, respectively.

Another important part of the system is the digital part implemented on the FPGA. It consists of the SPI (Serial Peripheral Interface), a communication unit for the connection with the PC, a command decoder, excitation signal generators, a data encoder, a multi-channel DSP, and an additional digital signal processing hardware for extracting the information from the decimation filters. In next section, the DSP part will be described in detail. The block diagram of the complete implementation on the FPGA is shown in Figure 4.

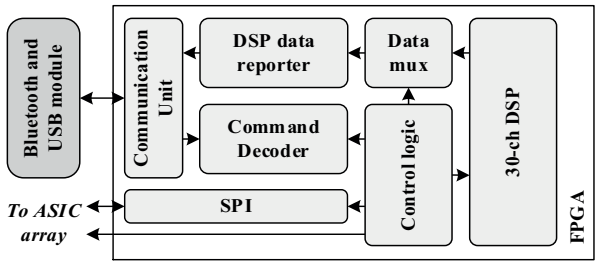


Figure 4: Block diagram of the FPGA implementation

The visual representations of DSP results are managed by the Graphical User Interface (GUI) developed to run on the PC (see Figure 1). It allows us to control various parameters of the analog part, as well as the parameters of the DSP module. It is possible to control various gains, excitation frequencies, voltages, and calibration capacitors in the AFE part, while in the DSP part we can control frequencies and phases of the down-mixing signals and decimation ratio of the last decimation filter. The programmability of the last decimation filter enables the possibility to adjust the bandwidth and the output data rate.

3 Digital signal processing

Each ASIC converts the capacitance changes from two differential sensors into a digital bit-stream, which is captured by the DSP for further digital signal processing. The DSP was designed and tested with a top-down design approach using Matlab and Simulink [4],[5]. After modeling, the DSP algorithms were coded to the Register Transfer Level (RTL) using VHDL, and then synthesized and implemented on the FPGA. The hierarchical Simulink environment makes it possible to efficiently model, simulate, and design all circuits on a high hierarchical level. Another important advantage of the high-level approach is to model and simulate the analogue and digital parts together in a very short time. In this way the appropriate decisions can be executed early in the design process, which improves the efficiency of the design. Signals used for driving, mixing, down-sampling timing, and further filtering must be strictly coherent (the measurement period is a multiple of every signal period and their ratios are prime numbers). All digital filters are realized with Cascaded Integrator – Comb (CIC) decimation filter architecture [6], as shown in Figure 5. The purpose of the CIC decimation filter is to remove the out-of-band shaped quantization noise and to reduce the data rate to the Nyquist rate. The order of the decimation filter should be larger than the order of the modulator to sufficiently suppress the out-of-band quantization

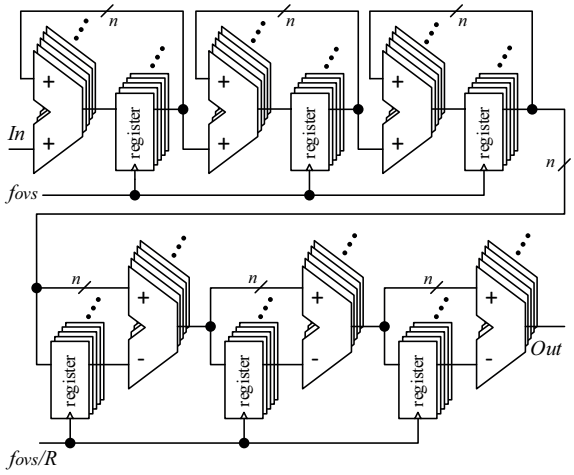


Figure 5: 3rd order CIC decimation filter structure [6]

noise. In our case we use a 3rd order sinc decimation filter with the standard structure [6] presented in Figure 5. The filter word length is optimized in such a way that no additional quantization noise due to finite word lengths is added into the filtering process [6]. In the full-precision mode, all registers following the first register must support the maximum accumulation produced by the first integrator section.

According to the known CIC filter properties, the overflows of the integrating and differentiating sections are not significant if the wrap-around two's complement arithmetic is used with a modular wrap-around property [4]. The integrating stages run with the oversampling frequency, while the comb sections run with a sampling frequency divided by the factor *R* (oversampling ratio). The decimation ratio in the first decimation filter stage is small in order to generate coherent signals.

The transfer function in the z-domain and the corresponding maximum dynamic range growth at DC for the decimation filter are given in (2), where *N* is the order of the filter and *R* is the decimation factor [6], [7], [8].

$$H_{dec}(\mathrm{z}) = \left[\frac{1-z^{-RM}}{1-z^{-1}}\right]^N \Rightarrow \left|H_{dec}(\mathrm{e}^{j0})\right| = RM^N \quad (2)$$

In our case, the comb filter differential delay *M* is always equal to 1 and will not be addressed in further equations. It is known that the transfer function has zeros f_Z defined in (3), where *k* is the integer multiplier ($k \in \mathbb{Z}$).

$$f_Z = k \cdot f_{dec} = k \cdot \frac{f_{ovs}}{R} \quad (3)$$

All components in the pass-band are mapped around the multiples of the output sampling frequency f_Z. If we define f_{cut} to be the passband cutoff frequency of a usable pass-band *f*, then the imaging regions are defined as (4).

$$\left(f_Z - f_{cut}\right) \le f \le \left(f_Z + f_{cut}\right) \quad (4)$$

The passband cutoff frequency has to be smaller than $f_{ovs}/2R$ in order to avoid aliasing of the imaging frequency bands around the zeroes f_z. To attenuate those regions in the cascaded filter structure, the decimation rates are selected in such a way that the zeroes of all filters are covered with zeroes caused by the output sampling frequency of the previous filter. By increasing the number of stages, we improve the filter's ability to reject the image components. Unfortunately, the attenuation at the passband edge is increased as well, which can be compensated with appropriate FIR filter in series after CIC filter. In our case the relevant signals after digital down-mixing become DC components, therefore the compensation filter is unnecessary. This process is shown in Figure 7 below.

The main parts of the DSP are: the configuration register, down-mixers, frequency dividers, and CIC filters. As previously mentioned, each ASIC process the signals from two sensors and thus each bit-stream contains information from two sensors. The DSP separates those two components into separate channels; each channel is followed by digital filter to reduce the bandwidth and provide appropriate outputs for further processing. The block diagram of a complete DSP is presented in Figure 6.

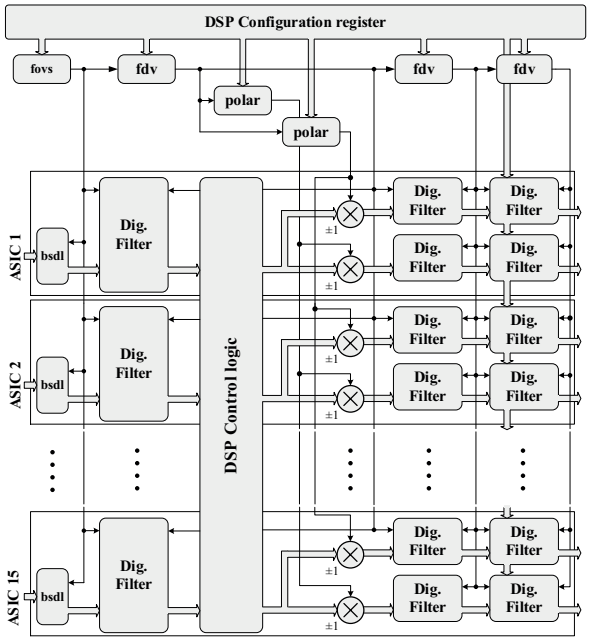


Figure 6: Block diagram of the DSP

The output of each ΣΔ - modulator is a stream of 1-bit data, with the frequency of 6.25 MHz. The first decimation filter performs only a rough filtering to remove high frequency-shaped quantization noise of the bit-stream, using decimation rate $R_1 = f_{ovs}/f_{dec1} = f_{ovs}/2f_N = 16$. Accordingly, the output rate is reduced from f_{ovs} to $f_{dec1} = f_{ovs}/R_1 = 390625\ Hz$. The spectrum contains two main components at frequencies f_{o1} and f_{o2} and the remains of the attenuated high frequency of the mixing process and thermal noise. The amplitudes of the main spectral components are proportional to the corresponding sensor capacitance difference and excitation signal amplitudes. The noise, which reduces the signal-to-noise ratio (SnR) of the measurement, can be reduced by decreasing the bandwidth of the digital

results. The main spectral components of each channel are translated to DC by mixing the output signal from the first filter with two digital square-waves with frequencies f_{o1} and f_{o2}. The results are two separated DC digital signals, as shown in Figure 6, where G_{D1}, G_{D2} and G_{D3} represent the gain of the filters.

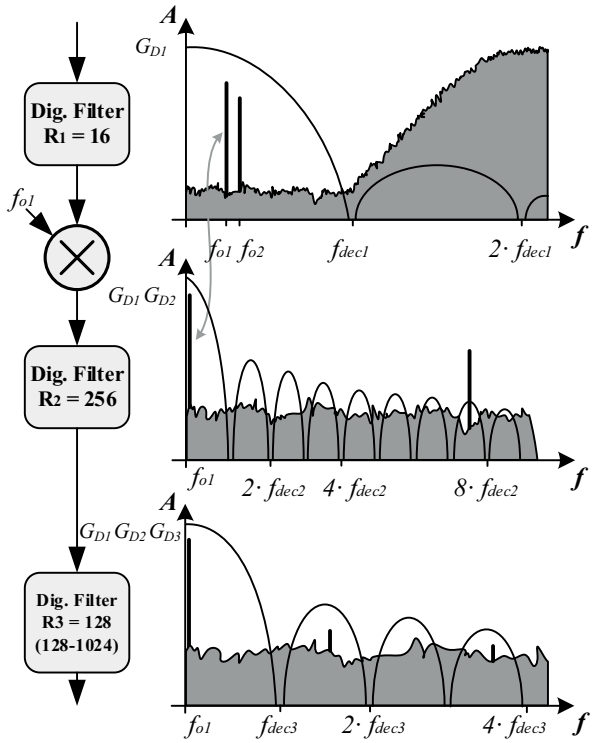


Figure 7: Digital signal processing for one channel

In order to remove the remains of the high frequency spectral components and to reduce the data rate, two additional decimation filters are used with the default decimation rates R_2 = 256 and R_3 = 128 with zeroes at $k{\cdot}f_{dec1}/R_2$ and $k{\cdot}f_{dec2}/R_3$, respectively. This procedure is presented in Figure 7. The bandwidth and the output data rate after both low-pass digital filters is reduced to $f_{ovs}/(R_1R_2R_3) \cong 12$ Hz. With the ability to change the last decimation rate in a range from 128 to 1024, we can reduce the output data rate down to ~ 1.5Hz. The results are then transferred to the PC for further filtering, decimation, storage, and presentation.

4 Implementation of the dsp and other digital parts

The majority of the digital circuits including the DSP are implemented on the FPGA as shown in Figure 4. For correct operation of all decimation filters, we have to ensure appropriate word length to prevent data distortion due to the overflow. The highest pass-band gain occurs at the DC, which is a function of the number of stages as defined in (2). Since the two's complement arithmetic is used, the maximum required number of bits B_{MAX} for the accumulation is calculated by using (5) [6], where $N{\cdot}\lceil log_2 R \rceil$ represents the maximum register growth.

$$B_{MAX} = N \cdot \lceil \log_2 R \rceil + B_{IN} \tag{5}$$

B_{IN} is the number of input bits, N is number of stages and R is the decimation ratio. Brackets $\lceil x \rceil$ represents ceil function (the smallest integer not less than x). In multistage decimation CIC filters, this can result in large register widths due to register growth for every added decimation filter by $N{\cdot}\lceil log_2 R \rceil$, leading to high consumption of hardware resources. The word-length of registers is possible to control by truncation and unbiased rounding to even numbers in each output stage. This reduces the gain of the filter by a factor of 2^{Btr}, where *Btr* is the number of cut off LSB bits. Truncation also increases the overall quantization noise, which has to be below the noise of analog electronics. With the help of the Matlab Simulink system simulations we have found that the output word-length of 22-bits in the second, and 24-bits in the third decimation filter are long enough to maintain the 100 dB dynamic range. The complete system is designed in such a way that the quantization noise generated in the modulator and in the decimation filters is always smaller than amplified thermal noise generated in the charge amplifier. The overall truncation noise variance σ at each filter output is defined in (6), where B_{MAX} is the maximum register growth according equation (5), and B_{OUT} is an output word-length [6].

$$\sigma^2 = \frac{\left(2^{B_{MAX}-B_{OUT}}\right)^2}{12} \tag{6}$$

The total quantization noise variance of all digital filters is then calculated using (7), where σ_k is the output variance of the error for each filter.

$$\sigma_{out}^2 = \sum_{k=1}^{n} \sigma_k^2 \tag{7}$$

A detailed description of the quantization noise can be found in [6]. In our case, the first 3rd order decimator (R_1 = 16) requires 14 bits, the second decimator (R_2 = 256) requires 38 bits with output truncation to 22 bits, and the third decimator with programmable down-sampling ratio R_3 from 128 to 1024 requires 43 to 52 bits (depending on the R factor) with output truncation to 24 bits. The FPGA resources allow us to build simple CIC filter structures with equal (maximal) number of internal bits for all integrator and comb stages. In the

integrated version of the system it will be considered to use the Hogenauer pruning technique to reduce usage of the silicon area, as well as power consumption. The word-length profiles of CIC decimation filters in each channel are shown in Figure 8.

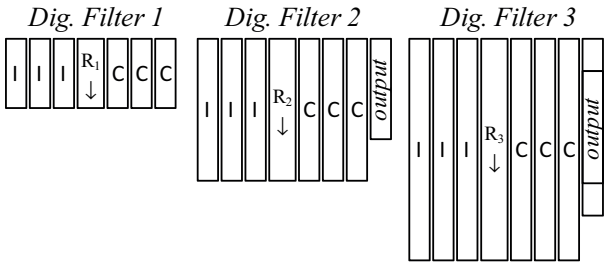


Figure 8: Word-length profile of CIC decimators

The word-length of the last decimator changes according to equation (5), due to the controllable decimation rate. The highest word-length *Bmax(R=1024)* has been used to assure appropriate accumulation for all selectable decimation rates defined by R^m, where *m* is in the range of 7 to 10. The wrap-around two's complement arithmetic also provides correct results before truncation for lower decimation rates. Truncation without adjustment at the output, starting from MSB, would result in the output value reduced by the factor $2^{Bmax(1024)-Bmax(R)}$, where *Bmax(R)* represents the word-length of the selected decimation rate *R*. This happens because of the larger word-length at smaller decimation rates that would be otherwise smaller according to (5). To get the correct result it is necessary to truncate the output, left shifted for *Bmax1024 – BmaxR* bits. The position of truncation output bits at different decimation rates is shown in Figure 9.

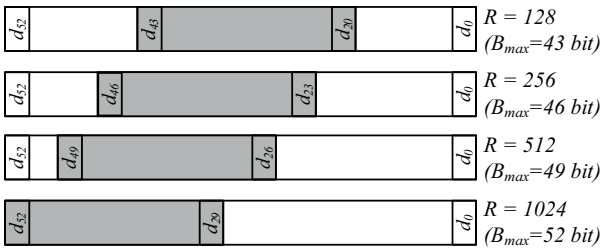


Figure 9: Truncation at last decimator according to decimation rate R

Another issue in order to assure correct system operation is the need for the synchronization of sensor excitation signals with the down-mixing signals f_{o1} and f_{o2}.

Synchronization is needed because the excitation signals are generated in the ASIC, while the down-mixing signals f_{o1} and f_{o2} are generated in the physically separated block (FPGA). Those two pairs of signals must have the same phase to obtain a valid measurement

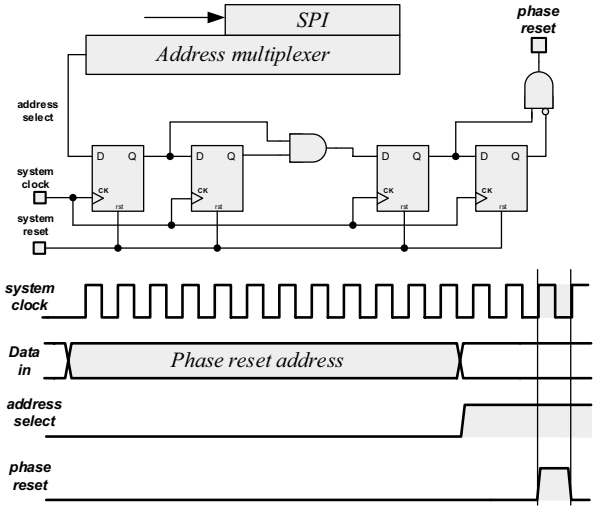


Figure 10: Phase reset circuit implemented in the ASIC and in the FPGA with timing diagram

result. The synchronization takes place with the simultaneous phase reset in the ASIC and FPGA at the beginning of each measurement cycle. The reset circuit shown in Figure 10 is initiated by the simultaneous decoding of the unique SPI address in both systems. The first two flip-flops prevent the meta-stability, while the other two realize the front edge detector. When required, the reset pulse with one clock cycle width is generated in both systems.

Another significant part of the system is the DSP data reporter, responsible for proper data transfer from the DSP to the communication unit. Generally, the DSP data reporter is a finite state machine, which converts the last filter output into a stream of hexadecimal characters. The universal asynchronous receiver/transmitter transfer rate was adapted to send the results from 30 channels at the smallest selectable decimation rate (i.e. the highest output rate). A simplified block diagram of the DSP data reporter with the communication and PC data processing units is shown in Figure 11.

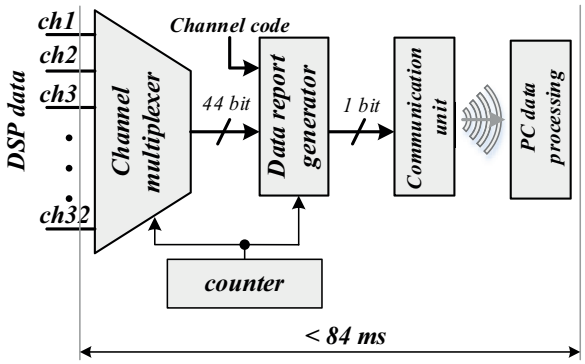


Figure 11: DSP data reporter block diagram with Communication unit

Table 4.1 shows the device utilization summary of the implementation on the FPGA for the entire digital system.

Table 4.1: FPGA hardware utilization summery

Logic Utilization	*Used*
Number of Slices	20698
Number of Slice Flip Flops	23377
Number of 4 input LUTs	25261
Number of bonded IOBs	59
Number of GCLKs	3

5 Measurement results and data processing

The measurements were performed in a controlled laboratory environment using a gas generator and the measurement system, described in Section 2 and 3, and shown in Figure 12. Figure 13 shows the Graphical User Interface (GUI), written with the C# (C Sharp) programming language in the Visual Studio environment.

The GUI allows us to control the current system parameters through ASIC and DSP settings. The digital response at the DSP output is *ΔN,* which is dimensionless

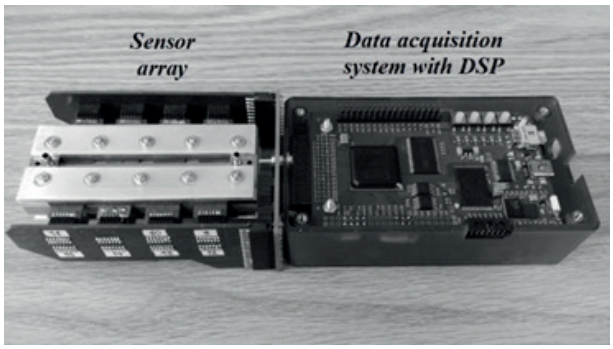


Figure 12: Measurement system with Sensor array and Data acquisition system

and proportional to the relative change of the capacitance $\Delta C_x/C_f$. ΔN can be estimated using (8), where ΔV_{sx} is the excitation signal amplitude, G_A is the gain of complete analogue measurement path and G_{D1}, G_{D2} and G_{D3} are the gains of the DSP part [2].

$$\Delta N \cong \Delta V_{sx} \cdot \frac{\Delta C_x}{C_f} \cdot G_A \cdot G_{D1} \cdot G_{D2} \cdot G_{D3} \tag{8}$$

It is also necessary to consider the gain loss due to truncation at the output of last two decimation filters. The gains of truncated filters in equation (8) have to be reduced according to (9).

$$G_{D1} = R_1^N,\ G_{D2} = \frac{R_2^N}{2^{B_{MAX2}-B_{OUT2}}},\ G_{D3} = \frac{R_3^N}{2^{B_{MAX3}-B_{OUT3}}} \tag{9}$$

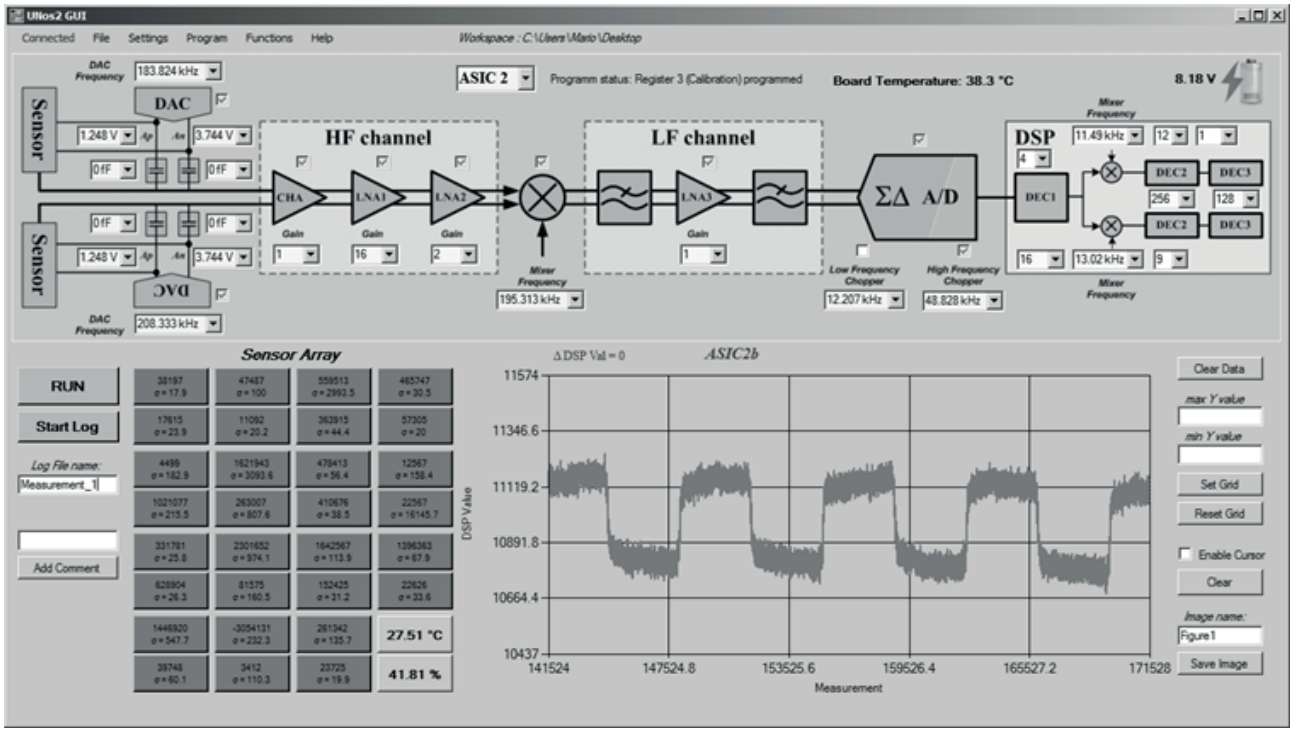


Figure 13: User interface with a measurement result on the modified sensor

The DSP provides ~1.5 to ~12 results per second depending of the last decimation rate. Those results can be filtered on the PC, using the moving average filter according to (10).

$$AVG(n) = AVG(n-1) + \frac{x(n)}{M} - \frac{x(n-M)}{M} \qquad (10)$$

The moving average period *M* can be set with a constant value from 8 to 512. The algorithm in the GUI also calculates a standard deviation of the results and generates Matlab scripts for further analysis. All results can be stored in the files for off-line processing and examination. To monitor environmental conditions of the gas mixtures, one measurement channel is dedicated for the temperature and the humidity sensor.

The DSP result presented in Figure 14 shows the consequence of switching the input gas between dry N_2 and the N_2 contaminated with the target molecules (TNT with ½ vapor pressure) for one channel with 12Hz bandwidth. The modified sensor surface is functionalized with APS molecules [2], while the untreated reference sensor is used as a control sensor to track only environmental changes without the response to the target molecules. We estimate the normalized sensitivity S_{TNT} in 1 Hz band using (11) [2], where ΔN is the difference between two results from DSP and *BW*=12Hz (after DSP filtering).

$$S_{TNT} \cong \frac{3.5 \cdot 10^{-12}}{\left(\Delta N_{TNT}\sqrt{BW}\right)} = \frac{3.5 \cdot 10^{-12}}{\sqrt{Hz}} \qquad (11)$$

The measured, input referred noise level of the DSP is much smaller than the equivalent input referred thermal noise level of the charge amplifier. From this, we can conclude that DSP does not bring additional noise to the system. The long measurement times are the consequence of slow gas flow, caused by piezoelectric pumps capacity (15 ml/min) and relatively big nonfunctional volume of connecting tubes.

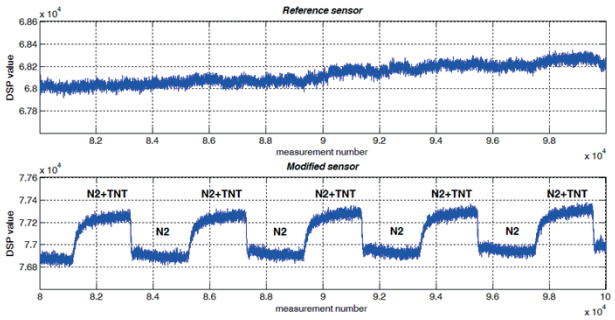


Figure 14: Measured response of the system, switching between pure N2 and a mixture of N2 and 50% vapor pressure of TNT at room temperature. The environmental drift in the reference sensor is repeated in the modified sensor.

6 Conclusions

The implementation of Digital Signal Processing for a miniature, multi-channel, vapor trace detection system is presented. At the moment the detection system it is capable of detecting vapor traces of different explosives. The 30-channel measurement system including all measurement boards (ASICs + sensors), consumes a relatively low amount of energy (approximately 200mA at 7.2V). A further plan is to integrate a complete detection system, which could lead to a cheap, efficient, and very selective vapor trace detection system for different molecules in the air. Integration will reduce the volume and power consumption of the complete system. The power and silicon area will also be reduced with appropriate pruning technique for internal word-length reduction in filter registers. We also plan to upgrade the GUI with an automatic sensor calibration and test engine to be able to verify the operation of each ASIC in the array during the startup time.

7 Acknowledgments

The authors acknowledge the financial support of the Slovenian research agency, ARRS under contract number J7-5497.

8 References

1. Boisen A, Dohn S, Keller S S, Schmid S and Tenje M 2011 Cantilever-like Micromechanical Sensors Rep. Prog. Phys. 74 1–31
2. Strle D., Štefane B., Zupanič E., Trifkovič M., Maček M., Jakša G., Kvasič I. and Muševič I. (2014). "Sensitivity Comparison of Vapor Trace Detection of Explosives Based on Chemo-Mechanical Sensing with Optical Detection and Capacitive Sensing with Electronic Detection". MDPI Sensors 2014, 14(7), 11467-11491
3. Strle, D., Stefane, B., Nahtigal, U., Zupanic, E., Pozgan, F., Kvasic, I., Macek, M., Trontelj, J., Musevic, I. (2012). "Surface-Functionalized COMB Capacitive Sensors and CMOS Electronics for Vapor Trace Detection of Explosives". Sensors Journal, IEEE, 12(5), 1048-1057.

4. Raič, D., Strle, D. "Advanced Decimator Modelling with HDL Conversion in Mind in Engineering Education and Research using MATLAB"; InTeh: Rijeka, Croatia, 2014.
5. Drago Strle (2011). Mixed-Signal Circuits Modelling and Simulations Using Matlab, Engineering Education and Research Using MATLAB, Dr. Ali Assi (Ed.), ISBN: 978-953-307-656-0, InTech, DOI: 10.5772/21556.
6. Hogenauer, E.B.: "An Economical Class of Digital Filters for Decimation and Interpolation", IEEE Trans. on Acoustics, Speech, and Signal processing, Vol. ASSP-29, No. 2, April 1981, pp. 155 – 162.
7. Meyer-Baese U. Digital Signal Processing with Field Programmable Gate Arrays. Springer; 2001.
8. Newbold, R.: "Practical Applications in Digital Signal Processing"; Prentice Hall, 2013, ISBN 978-0-13-303838-5.

Arrived: 04. 02. 2015
Accepted: 16. 09. 2015

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 45, No. 3 (2015), 204 – 215

Grid-Tied Smart Inverter Safety Functionality: Fast Power Quality Event Detection

Isabel M. Moreno-Garcia, Antonio Moreno-Munoz, Aurora Gil-de-Castro, Rafael Real-Calvo, Emilio J. Palacios-Garcia, Miguel J. González-Redondo

Department of Computer Architecture, Electronics and Electronic Technology, University of Cordoba, C. Rabanales, Ed. Leonardo Da Vinci, Cordoba, Spain

Abstract: This paper addresses the fast detection of electric signal disturbance for advanced smart inverter functionality within the framework of large scale grid integration of renewable energy sources. A statistical-based technique under the fault detection and isolation (FDI) paradigm is proposed for fast detection in power systems. The aim is to improve the performance of interconnection systems and the electricity grid's energy efficiency. The new method developed is based on the CUmulative SUM (CUSUM) algorithm and is applied to a wide set of power quality events to analyse its performance. The results show that the method generates residuals that are robust to noise and accurately estimates the time locations of underlying transitions in the power system. The main advantage of the proposed technique is its early event detection, with respect to other traditional methods, because it performs sample-by-sample evaluations. Moreover, the proposed technique does not require much computational effort, which means that the presented detection method is suitable for integration into the multifunction relay protection subsystems available in novel smart inverters.

Keywords: Change detection algorithms; event detection; power quality; power system protection; real-time system

Varnostna značilnost pametnega omrežnega razsmernika: Hitra detekcija dogodka kvalitete moči

Izvleček: Članek naslavlja hitro detekcijo moten električnega signala pri naprednih pametnih razsmernikih v okvirju široke omrežne integracije obnovljivih virov energije. Za hitro detekcijo je predlagana statistična metoda odkrivanja napak in njihovih izolacij (FDI). Cilj raziskave je izboljšanje povezav in učinkovitost prenosa električne energije. Nova metoda temelji na kumulativnem seštevalnem algoritmu (CUSUM), ki je z namenom analize učinkovitosti apliciran na širok set dogodkov kvalitete moči. Rezultati nakazujejo, da metoda generira ostanke, ki so neobčutljivi na šum in natančno ocenjujejo časovno lokacijo osnovnih prenosov v sistemu. Največja prednost predlagane tehnike, v primerjavi z obstoječimi, je hitra detekcija dogodka na osnovi medvzorčnih ocen. Nadalje, nova tehnika ne zahteva velike računske moči, zaradi česar je primerna za integracijo v večopravilne stikalne zaščitne sisteme razsmernika.

Ključne besede: algoritem detekcije sprememb; detekcija dogodkov; kvaliteta moči; zaščita močnostnega sistema; sistem v realnem času

* *Corresponding Author's e-mail: p92mogai@uco.es*

1 Introduction

Nowadays, energy is a vital means of achieving social development. Nevertheless, energy production is a source of significant environmental impact, and the improper use of increasing amounts of energy is one of the factors involved in major potential environmental degradation. The transition to a more sustainable societal model is perhaps the most important challenge faced today. The increasing pressure on natural resources due to the introduction of millions of new consumers to markets, economic dependency on energy sources located outside of our territories, and climate change, as a consequence of increased global warming in recent decades, are only some of the issues that must be addressed to prevent reductions in levels of well-being.

One method of avoiding this unbalance is for industrialised countries to reach environmental sustainability by decreasing their energy intensity, reducing their consumption of fossil fuels, diminishing greenhouse gas emissions and increasing the security of their energy supply [1]. In this context, a long-term commitment to renewable energy sources (RES) seems to be the only adequate answer to all of these issues. An example can be seen in the recent solar boom of 2010-12 and its integration into electrical systems in different countries. However, the growing penetration of solar generation raises several economic, regulatory and technical questions, some of which are closely related to power quality (PQ) [2]. Moreover, the growing coexistence of both conventional and distributed generation in the same electrical system is causing a reconsideration of the traditional power system towards the smart grid. This approach will require the global integration of large numbers of independent and autonomous systems from different stakeholders. Due to the market trend towards diversifying distributed energy resources (DERs), large infrastructure systems, such as the electric power grid, may be viewed as complex systems-of-systems. This will pose new challenges for the integration of these intelligent sub-systems, so they can participate collectively and in a timely manner. This radical shift from the traditional centralised philosophy will require the implementation of real-time information in the whole electrical system.

DERs not only include generation units but also aggregated flexible resources like storage for electrical and thermal energy and/or flexible loads. Thus, DER systems that generate AC output, often with variable frequencies, such as wind, microturbine or flywheel storage, need AC-DC conversion. For DC output systems like PV, fuel cells and batteries, a DC-DC conversion is typically needed to change the DC voltage level. Accordingly, MW-scale power electronics converters are essential components in new DER plants. Due to advancements of technology, the costs of power electronics have decreased significantly, sizes have also become smaller and performance has improved. Up to now, most DERs only produce power; they do not contribute to the ancillary services required to control the power system and ensure stable operation. However, the main inconveniences of DERs include their inherent variability and uncertainty.

Part of the solution to moderating the impact of DERs on the grid lies in the DER units themselves, particularly in the interconnection equipment, such as inverters, that connects DERs to the electric power system. Driven by Germany's 2011 LV-MV Directives [3], inverters can contain smart features such as reactive power control to aid with grid integration. By the end of 2015, over 50% of inverters can carry these functions. This percentage could increase through disruptive energy-storage innovations being incorporated into the inverter [4].

Thus, there is a growing need for a high-performance embedded system that supports both existing functionalities and future operational requirements. Standards like IEC 61727 [5], IEEE 1547 [6] and VDE 0126-1-1 [7] establish criteria and requirements for the interconnection of DERs with electric power systems. The requirements shall be met at the point of common coupling (PCC). Although the devices used to meet these requirements can be located elsewhere, the current trend is to include it within the inverter itself [8,9]. Recently, we have presented the complete characteristics of a smart inverter for distributed energy resources (SIDER), and some possible new active functions can still be developed [10,11]. In the smart grid, SIDER can contribute to the reliability and stability of the entire power-supply infrastructure. It must respond to PQ events and fault conditions within the sub-cycle range by incorporating extremely fast response times. What is more, due to market expectations, self-diagnosis and self-healing functionalities must play a fundamental role in achieving the high PQ demanded, as well as subsequent trust in the smart grid paradigm.

The rest of this paper is organised as follows. An overview of the methods proposed for detecting of PQ disturbances is presented in Section 2. In Section 3, we propose a statistically based detection method with an FDI approach. Section 4 studies the performance of the method detecting different PQ disturbances. Finally, the conclusions are given in Section 5.

2 Detection of power quality events

The automated power quality analysis entails the following stages: the detection, segmentation and characterization of the power quality event. This information is useful to determine its cause and to establish limits of responsibilities between a network operator and final customer. An extensive and updated classification of different techniques available can be found in [12]; unfortunately, an analysis of their suitability for each of the above mentioned stages has not been clearly established. These stages can be preceded by a pre-processing stage of signal de-noising and normalisation. We have addressed the second and third stages thoroughly in prior works [13–18]. Thus, this paper focuses on the experimental research effort toward fast detection of electric signal disturbance within the framework of advanced smart inverter requirements.

Nowadays, well-known signal processing methods have been applied to detect PQ disturbances with satisfactory results. Evaluating electrical system disturbances involves studying voltage and current deviations from the ideal waveform. In general, these deviations can be classified into two groups under the PQ paradigm: variations and events [19]. The former (eg, harmonics, overvoltages, unbalances, etc.) are generally regarded as small and gradual deviations from the voltage/current sine wave, characterised as steady-state phenomena; the latter produce sudden, large deviations of the waveform, are characterised as non-stationary random phenomena, and are usually caused by incidents involving the electrical system's operation conditions. According to [20], the event detection methods can be grouped into time-dependent waveform feature [21], signal transformation [22] and parametric models [20]. Many studies have analysed the advantages and disadvantages of these methods. In particular, [23], shows the statistical performance of various detectors of a signal affected by a dip, using methods based on root mean square (RMS), Kalman filter, wavelet, peak voltage, missing voltage and generalized likelihood ratio test (GLRT). However, despite the wide range of PQ event parameters (frequencies, magnitudes, and durations), it is difficult to find a single method that is suitable for detecting of all types of them. For example, the commonly used wavelet transform is suitable for detecting of transients but fails for short- and long-duration variations (such as sags and swells, particularly those with a nonrectangular shapes) [24]. The situation is similar for HOS; the behavioural differences in frequency between the transients and sag (or swell) demands, which the sliding window used to extract HOS features, were completely different in both cases. For the transients, after a high-pass filter, the width of the window may be less than one cycle; for the last events, which are roughly of the same frequency as the "healthy" signal (ideal power-line sine wave), the window must contain a cycle of the 50-Hz sine wave [25]. Thus, in this paper, to unify the statistical treatment of all PQ events, it will be necessary to choose a new variable that exclusively distils the information of the perturbation from the waveform, without any losses (a descriptor).

Moreover, disturbance detection is a critical task and an effective protection requirement that is needed to successfully control the interconnection of a DG system to the grid. It must be performed on-line and in strict real-time, with the less number of false detection and accomplishing the temporary response specifications suitable for monitoring parameters and planned protective actions. Fig. 1 shows a comparison of the main standards in PQ applications and protection, referring to the response times needed to disconnect the equipment of the DG system's equipment when the voltage exceeds the allowable operating ranges.

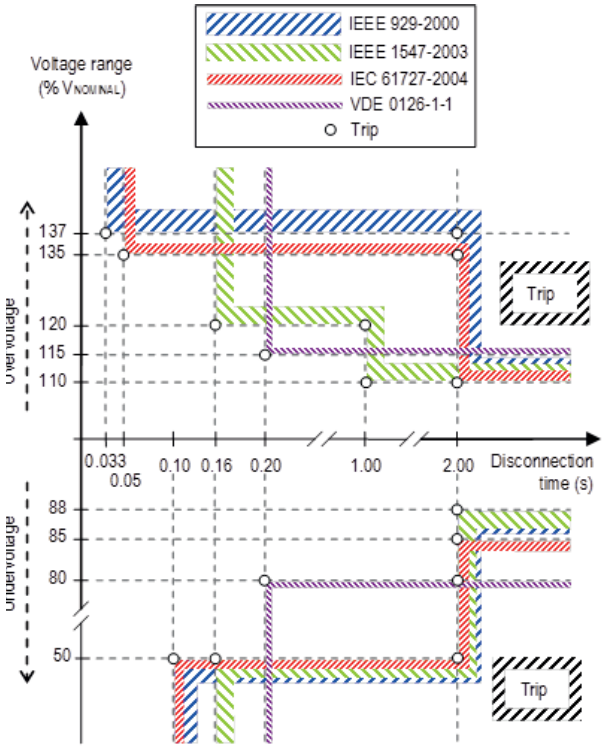


Figure 1: Comparison of responses to abnormal voltage according to different standards.

As shown in Fig. 1, IEEE 929 [26] and IEC 61727 [5] are very similar with respect to operating ranges and disconnection times. In these standards, being outside the normal range of operation is necessary to disconnect the equipment in < 2 s. One can see that at a relatively large distance from the percentage of nominal voltage, the trip points require low disconnection times (≤ 0.10 s). IEEE 1547 [6] aims for such high percentages of rated voltage to not be achieved, seeking a compromise solution to the overvoltages, so that disconnection times can be increased. Finally, the VDE 0126-1-1 [7] standard seeks to provide a compromise solution and greater simplicity in controlling the device with only two trip points for overvoltages and undervoltages, respectively.

Thus, to prevent failures of high relevance to the power system, the protection devices integrated with the grid must be able to detect disturbances in early stages. We are definitely dealing with a problem of change point detection within the FDI domain, in response to the specific fault. A thorough survey can be found in [27]. The problem of change detection has remained an area of strong interest in recent years, as well as the study of parametric statistical tools for detecting abrupt changes in discrete time signals and dynamic systems [28,29]. According to the model-based filtering

introduced in [29], and bearing in mind that most of the detection methods use a detection parameter (DP) joint a threshold, the detection of abrupt changes in the processed signals can be conceived in three steps:

- *Residual generation:* The basic principle is that residuals from are generated signal modelling. These residuals are expected to be zero (or zero mean) under no-fault conditions. In practical situations, the residuals are corrupted by the presence of noise, unknown disturbances, and uncertainties in the system model. The aim of the method is to generate robust residuals insensitive that are to these noises and uncertainties but are sensitive to faults.
- *Detection parameter generation:* The filter residuals must be treated in order to be transformed into a distance measure (DP) that measures the deviation from the no-change hypothesis.
- *Stopping rule:* This step is based on a statistical algorithm to make decisions on whether the deviation of a DP is significant.

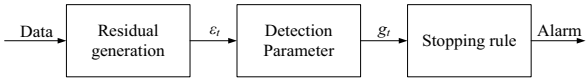


Figure 2: Block diagram of the detection method based on filtering [29].

3 The proposed detection algorithm

This work mainly focuses on a quantitative model-based approach to FDI, so that it can be used to develop more efficient and reliable equipment. The detection methods included in an intelligent electronic device (IED) allow PQ measurement and provide, protection functions and predictive tools, making the device ready to be used in the new smart grid model with the characteristics described in [30], i.e. fast registration of the events, transmission to the power network control system and smart relay protection devices [5].

In our work [31] a high-capacity IED was designed to be embedded into inverter equipment took PQ, protective relay functions and synchronisation standards into account. For a fast activation of the protection functions, the detection instant should be as close as possible to when the disturbance start. Therefore, the analysis window should be as short as possible. Thus, the requisites of the algorithm are low computational load, high accuracy and robustness. What is more, if we wanted to detect the event in real-time the challenge is to make the decision in less than a half-cycle, obviously. In prior work [31], a detection method based on a CUSUM test of Page was initially proposed. In that work, the signals used were generated by a power system with a frequency was 50 Hz, in which the IED captured every half cycle (10 ms) while operating in real-time [11]. The CUSUM algorithm was selected because it operates sample to sample, making it suitable for fast detection. This algorithm accumulates the difference between the sample mean and a target mean, and plots it cumulatively. A change in the DP gradient, either increasing or decreasing, indicates a departure from the normal circumstances of the residual values [32,33]. The acquisition process, which is executed with a high priority loop, is joined in the detection process by CUSUM, which is executed with a normal priority loop that occurs in a time below 10 ms. The preliminary results from applying the CUSUM algorithm to real-time PQ detection were sufficient but not entirely satisfactory, as will be explained below. Moreover, the method's performance was only quantified using synthetic disturbances.

Thus, this paper provides a following step and analyses the CUSUM method with real three-phase disturbances. A modification of the original algorithm proposed in [31] is needed to detect an event in a real environment with the lowest number of false detection. The new proposed technique for fast detection of three-phase events and the new methods used to generate residuals are presented here; additionally, the rules to calculate the DP and decide whether to stop are thoroughly described.

3.1 Residual generation

As mentioned above, the aim of the residual generation in our work [31] was to model the signal in order to obtain robust residuals that are insensitive to these noises and uncertainties but are sensitive to faults. To this end, the first idea suggested was a unified analysis of the three-phase power system using the Clark Transform. However, for an unbalanced event, the transformation output adds a ripple component over the DC value, which is twice the source fundamental frequency f_o. To get the DC values, a notch filter or a low-pass filter with a its cut-off frequency lower than $2*f_o$ Hz is recommended to remove the ripple component [34–36]. Unfortunately, the use of an additional filtering step causes a delay in the event detection; hence it increases the response time, which results in a delay in the overall response time.

Therefore, a new method was needed here to overcome the above mentioned deficiency. A simple method called the peak detection method [37, 38], generally used in power electronics converters [39, 40], can be used to obtain our input variable. The peak detection method offers fast response time as well which, of less than a quarter of a cycle. This method is very simple

to implement and has a low computational burden; however when it was applied in real environment, it proved very sensitive to noise. Thus, the peak detection method was rejected in the early stages of this research.

A filtering method was finally considered. In residual generation, an adaptive filter takes the measured signal and transforms it into a sequence of residuals that are similar to white noise before the change occurs. The filtering approach is used to separate the signal from the noise. For this purpose, finite impulse response (FIR) or infinite impulse response (IIR) filters can be used, as long as designed by any standard method (Butterworth, Chebyshev, etc.) [29]. In this work, a high pass Butterworth filter was used to generate the residuals.

3.2 Detection parameter algorithm

The next step is to threat the residuals through a statistical algorithm in order to detect any abrupt change in the input signal early. To this end, several approaches can be used: analysing of the mean or variance of the residuals, analysing the square of the residuals or other options based on probability ratios.

In this work, the statistical algorithm used to develop the mentioned change detector (DP) is the CUSUM method, which is based on the mean and variance of the residuals. It was selected method because it requires minimal computational effort and operates sample to sample, which it is very appropriate for fast online detection. The change detection of the CUSUM method is labelled as a change in the mean of the filtered signal. The input to the CUSUM algorithm is called distance the measure, s_t, which is set with the residuals from the filter, $s_t = \varepsilon_t$ (Fig. 2).

The CUSUM algorithm directly includes all of the information in the sample sequence by plotting the cumulative sums of any deviation of the sample values from a target value. The CUSUM method is widely used across industries for monitoring deviations in a process with respect to a target value and also for finding evidence of change in the a process's mean; in particular, it has been successfully employed in power system fault detection [29, 42–44]. The CUSUM method is easy to handle and useful for detecting the locations of change points. The combination of information from several samples makes the CUSUM algorithm a suitable method for detecting abrupt changes of PQ events in real-time. The CUSUM version used in [31] was the so-called tabular or two-sided CUSUM method [28,32]; it was designed to detect high and low changes in mean processes, as well as record the cumulative sums of the signal samples in two directions. In this paper, the DP proposed to detect disturbances is only based on the statistical estimator for detecting an increase in the mean of the residuals, which is given by Eq. (1).

$$g_t = \max\left(g_{t-1} + s_t - \left(\mu_0 + K\right), 0\right) \quad (1)$$

where the DP, which is named g_t, sums the inputs s_t from the filter. In Eq. (1), μ_0 is the ideal mean of the process control state and K is the reference value set with a value that allows for a fast fault detection, which is usually half of the difference between the value of the average target control state and the value of the average at which the process is considered out of control [32]. The constant value given by the sum of μ_0 and K has been removed to prevent false alarms. In this work, unlike the previous one [31], these parameters are configured. The μ_0 parameter has been set to the mean of the samples processed to the current time, and the K parameter was configured at 0.5 times the standard deviation of the filtered signal.

3.3 Stopping rule

The purpose of the stopping rule phase is to detect when a process is considered to be out of control. In signal processing, the aim is to give an alarm when any statistic crosses a decision interval called a threshold, H. As mentioned above, non-zero residuals are generated if there is a disturbance in the processed signal. This situation produces a change in the mean of the samples processed at the current time, so that the change detection algorithm, g_t, must indicate the variation. The main problem in statistical change detection is determining the optimal threshold value to obtain high accuracy in change detection and a low rate of false alarms.

Regarding the preliminary results obtained with synthetic signals, the DP deviations from zero were considered to be produced by changes in the pure sinusoidal shape of the signal. However, with the measured signals, false alarms were generated in many cases when the threshold H was initialised to zero. To set a threshold H that avoids false alarms, 127 measured events were filtering and analysed. Later, the CUSUM algorithm was used to obtain the DP, and the results were studied through of a probability density function (PDF).

Fig. 3 shows the PDF. One can see that setting the threshold lower than the critical DP, the zero value, increases the probability of detection, but also produces an increase in the number of false alarms, due to the underlying noise of the real measurements. Thus, a threshold that is slightly greater than zero must be selected to avoid this problem and to design a

robust detection algorithm; 0.05 was the final threshold selected for use.

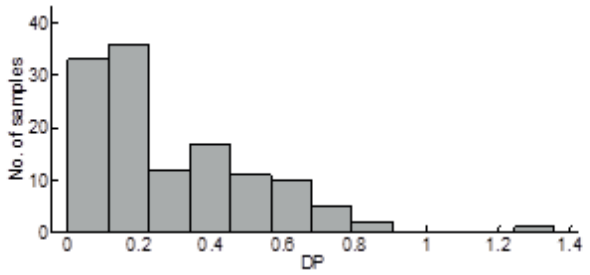


Figure 3: Results from designing the threshold over 127 disturbances.

Finally, the block diagram of the proposed technique is illustrated in Fig. 4. In this diagram, the signals are three-phase signals with no disturbance. In the residual generation block, the signals per phase are filtered and the residuals for each are obtained. Then, the residuals are treated using the CUSUM algorithm and the DP per phase is calculated. Finally, the diagnostic logic block makes the decision by using the established threshold and following the stopping rule: the start of a disturbance must be triggered (*T*) when the DP is across the threshold.

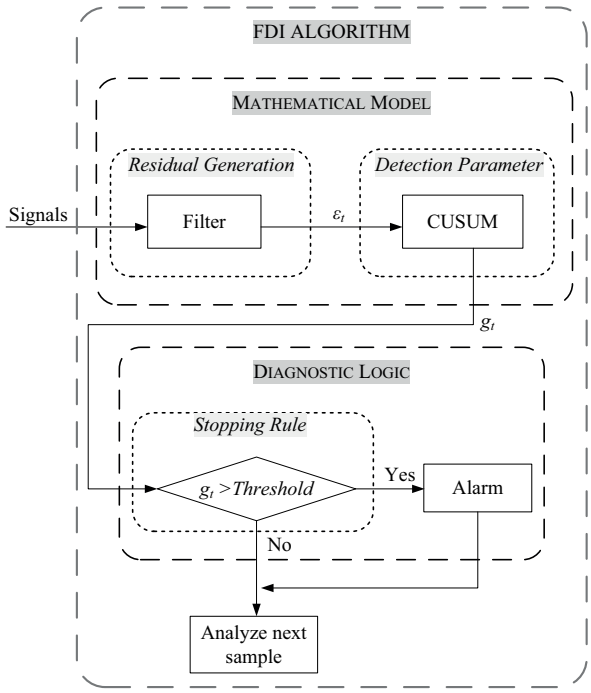


Figure 4: Block diagram of the proposed method for disturbance detection

This paper introduces further improvements in the algorithm and covers another critical issue in the online detection: the delayed detection. This issue is directly related to the ability of the selected algorithm to generate the detection signal alarm when a change occurs in real-time. An additional counter, called *N*, is used to reduce the effect of the analysis window and accurately calculate the start of the transition. The *N* parameter, introduced by Montgomery [32], estimates the first out of control instant of the process and indicates the number of consecutive times that the DP is non-zero after crossing *H*. Hence, the *N* parameter can be used to determine the time elapsed between the start of the transition (*S*) and the detection instant (*T*). Then, the non-stationary state of the process is triggered as a result of subtracting *N* from the initially set trigger point, *T*.

4 Experimental results

In order to validate the detector, other results from analysed measured signals are presented in this section. Considering that a design goal is to use the proposed technique alone for a wide range of PQ event parameters, the following cases are studied: dip, overvoltage, transient and interruption. All data used in this paper were obtained from measurements with the sampling rate f_s = 4800 Hz and 50 Hz power system frequency. Thus, each cycle contains 96 samples, or 20 ms. In this section, all of the signals' horizontal axes show the time in samples. The characteristics of the Butterworth used are 5th-order high pass, with a cut-off frequency of 3600 Hz.

Let us assume that the values of the DP that cross the threshold after a detected transition in the time of one cycle below are not considered to be transitions but effects of the previous transitions detected.

4.1 Dips

Fig. 5 shows a three-signal with a multi-stage dip (top graph) and the detection parameters with the same threshold (bottom graph).

From Fig. 5, one can see that there are three detection areas that correspond with the development between stages of the dip. The next figures, Figs. 6, 7 and 8, zoom into the detection areas. The DP per phase is individually shown in these figures, and the trigger instants *T* (vertical dashed line) and the calculated starting instant *S* (vertical solid line) are included in each one. Remember that *T* is the first instant when DP is across *H* (horizontal dashed line) and that *S* is the result of subtracting the counter *N* from *T*.

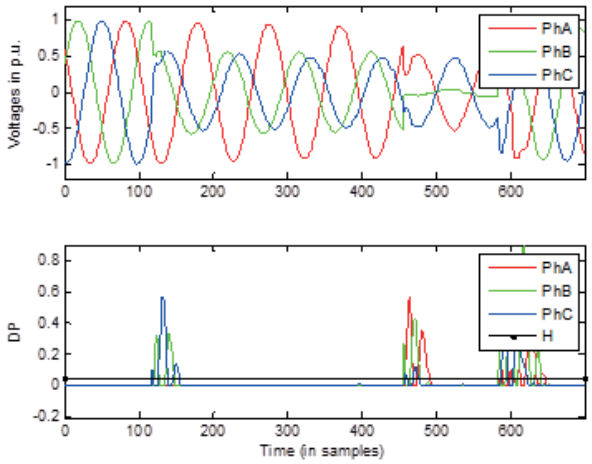


Figure 5: From top to bottom: input signal with multi-stage dip and detection parameters with the threshold

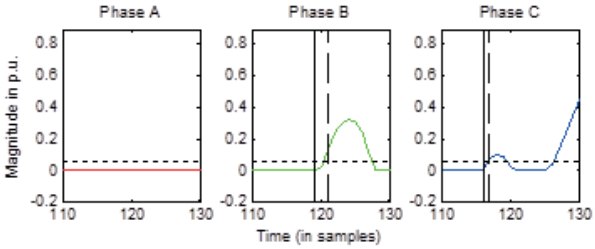


Figure 6: From left to right: zooms of the first detection area in phases A, B and C.

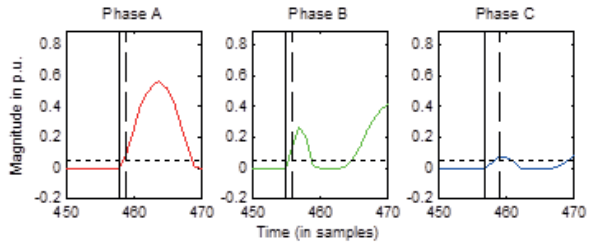


Figure 7: From left to right: zooms of the second detection area in phases A, B and C.

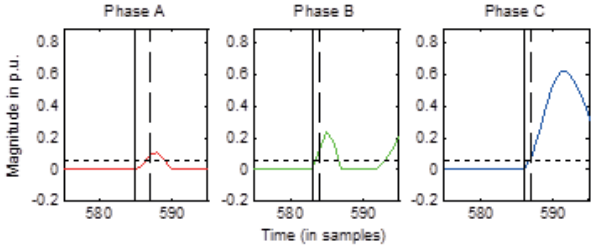


Figure 8: From left to right: zooms of the third detection area in phases A, B and C.

The detection instants calculated by the method are shown in samples in Table 1.

Table 1: Detection instants for multi-stage dip

Phase	First transition		Second transition		Third transition	
	T (sample)	S (sample)	T (sample)	S (sample)	T (sample)	S (sample)
A	-	-	459	458	587	585
B	121	119	456	455	584	583
C	117	116	459	457	587	586

For each detection transition area, the final trigger was set to the minimum value of the *S* parameter in the three phases. Hence, for the analysed dip, the final triggers were set at samples 116, 455 and 583, for the first, second and third areas, respectively. Figure 9 shows the original waveforms and the RMS voltage over a half-cycle rectangular window, with the triggers (vertical lines), showing the transitions.

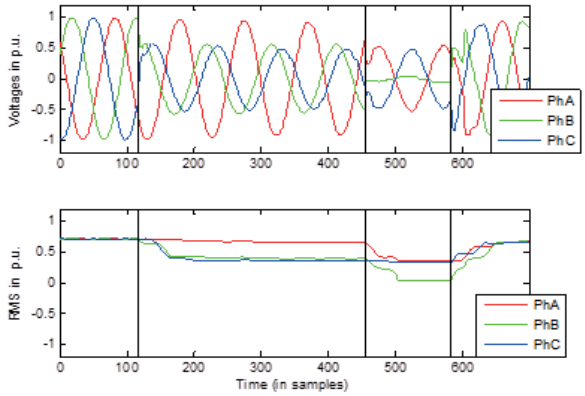


Figure 9: From top to bottom: input signal with triggers and RMS voltages with triggers.

4.2 Overvoltages

An example of a voltage dip due to single-phase fault with overvoltages in the non-faulted phases is shown in Fig. 10. As with in the prior case, there are three detection areas.

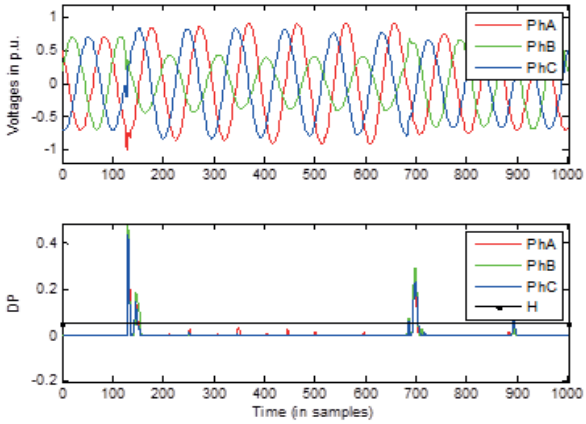


Figure 10: From top to bottom: input signal with overvoltage and detection parameters with the threshold.

The next figures, Figs 11, 12 and 13, zoom in on the detection areas.

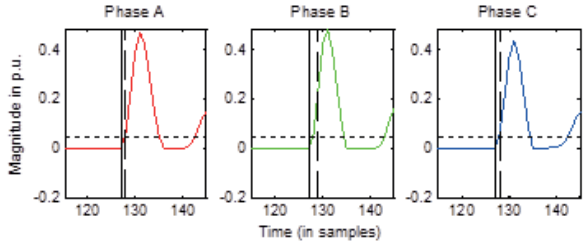


Figure 11: From left to right: zooms of the first detection area in phases A, B and C.

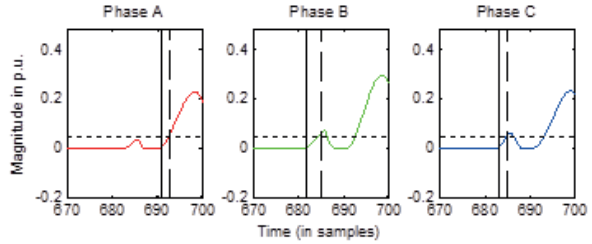


Figure 12: From left to right: zooms of the second detection area in phases A, B and C.

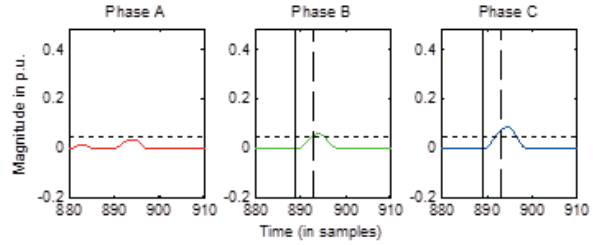


Figure 13: From left to right: zooms of the third detection area in phases A, B and C.

The detection instants, triggered instants *T* and the calculated starting instant *S* are shown in samples in Table 2.

Table 2: Detection instants for overvoltages.

Phase	First transition		Second transition		Third transition	
	T (sample)	S (sample)	T (sample)	S (sample)	T (sample)	S (sample)
A	128	127	693	691	-	-
B	129	127	685	682	893	889
C	128	127	685	683	893	889

The final triggers are set to the minimum value of the *S* parameter in the three phases per transition. Thus, the values of the triggers are set at samples 127, 682 and 889, for the first, second and third transition areas respectively. Fig. 14 shows the original waveforms and the RMS voltage over a half-cycle rectangular window with the triggers (vertical lines), showing the transitions.

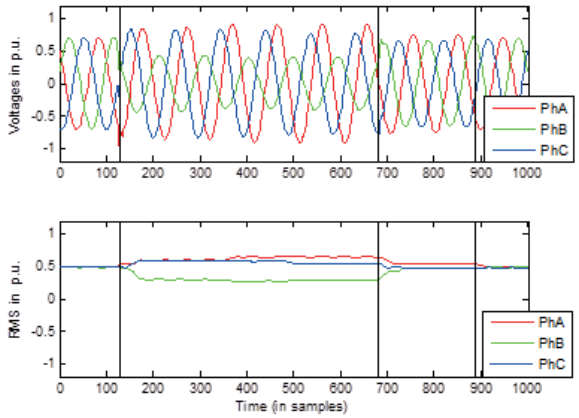


Figure 14: From top to bottom: input signal with triggers and RMS voltages with triggers.

4.3 Transients

In this case, the detection of a transient is presented. Fig. 15 shows the original waveform with the transient around sample number 500 and the DPs resulting from CUSUM. Fig. 16 shows a zoom of the original waveforms in the area of the transient. One can see that the three phases are affected by the disturbance. The DPs per phase in the transient area are individually shown and zoomed in Fig. 17. Also, the trigger instants *T* (vertical dashed line) and the calculated starting instant *S* (vertical solid line) are included in the graphs of Fig. 17. The trigger point (*T*) is sample 487 for phases A and B, and sample 490 for phase C. The starting instant (*S*) is sample 486 for phases A and B, and sample 488 for phase C. Thus, the final trigger was set to the sample 486. The final trigger is shown in Fig. 18 with the original waveforms and the RMS voltage over a half-cycle, rectangular window.

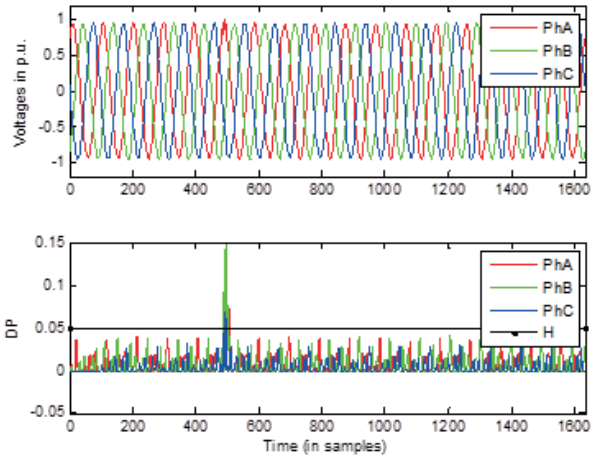


Figure 15: From top to bottom: input signal with transient and detection parameters with the threshold.

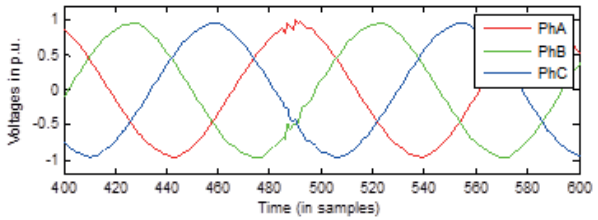


Figure 16: Zoom of the transient area.

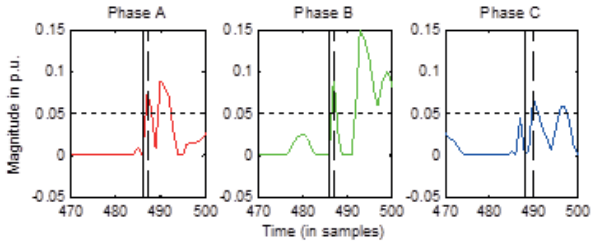


Figure 17: From left to right: zooms of the transitions for phases A, B and C.

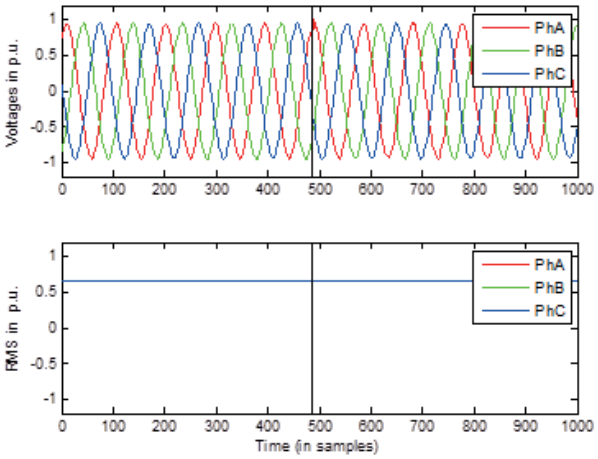


Figure 18: From top to bottom: input signal with the trigger and RMS voltages with the trigger.

4.4 Interruptions

Fig. 19 shows the original waveform of an interruption (top graph) and the calculated DPs per phase (bottom graph). Zooms of the detection parameters in the area of the interruption are individually shown in Fig. 20, including the trigger instants *T* (vertical dashed line) and the calculated starting instant *S* (vertical solid line). The trigger points (*T*) for phases A, B and C are sample 492, sample 489 and sample 484, respectively. The starting instants (*S*) for phases A, B and C are sample 491, sample 486 and sample 481, respectively. The final trigger is shown in Fig. 21, with the original waveforms and the RMS voltage over-half cycle rectangular window. The final trigger is set to the minimum value of the *S* parameter in the three phases, which occurs at sample 481.

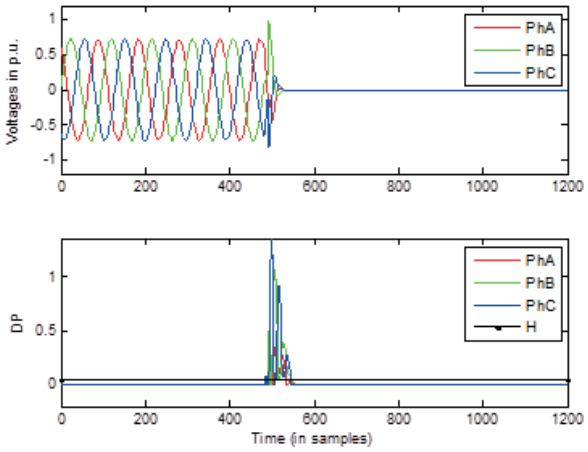


Figure 19: From top to bottom: input signal with the interruption and detection parameters with the threshold.

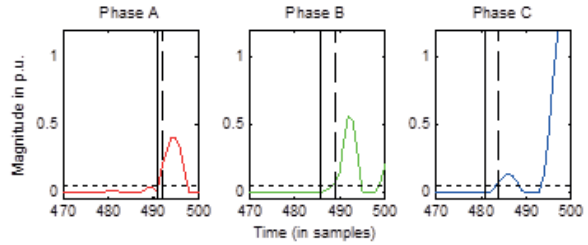


Figure 20: From left to right: zooms of the transitions in phases A, B and C.

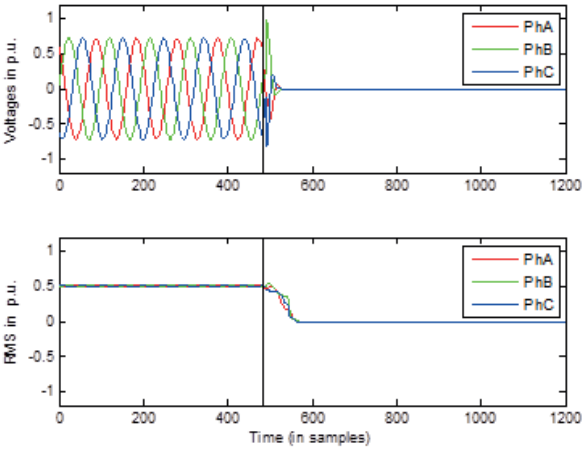


Figure 21: From top to bottom: input signal with the trigger and RMS voltages with the trigger.

5 Conclusions

The present study provides a useful technique for fast online detection of PQ events. The proposed method, based on the CUSUM algorithm as a statistical estimator, accurately detects the transition for three phases of different PQ events. Furthermore, the main advantages of the solution given in this paper are that the

CUSUM algorithm is extremely easy to implement and has very little computational burden, making it appropriate for an effective protection requirement. Another advantage of the CUSUM method is it performs sample-by-sample evaluation, making it suitable for early event detection. Moreover, the method overcomes the detection-delay problem inherent to the analysis windows of the conventional methods by including a counter that determines the time elapsed between the start of the transition and the detection instant. Additionally, a robust threshold setting for the detection index has been proposed, configured with high sensitivity and a low false-alarm rate. The CUSUM statistical estimator has been used to determinate the threshold. To this end, a probability density function of the detection parameter results has been made in order to apply CUSUM to a wide set of real measurement signals has been made. The implemented tests and experimental results show the effectiveness of this algorithm for detecting events and triggering with high precision the instant in which the three-phase signals start to deviate due to any disturbance. In summary, the proposed technique does not require much computational resolution and is very well chosen for implementation in protective relays. It is a robust detection algorithm that is capable of detecting PQ events in real-time.

6 Acknowledgements

This research is partially supported by FEDER-INNTERCONECTA project Total Integrated GRid Intelligent System (TIGRIS) ITC-20131002, under contract no. 12013095 and by FEDER-INNTERCONECTA project PV-On Time ITC-20131005, under contract no. 12013096. In addition, this work has been supported by the Spanish Ministry of Economy and Competitiveness under Project TEC2013-47316-C3-1-P.

7 References

1. Bassi AM. Evaluating the Use of an Integrated Approach to Support Energy and Climate Policy Formulation and Evaluation. Energies 2010;3:1604–21. doi:10.3390/en3091604.
2. Moreno-Muñoz A, De la Rosa JJG, López MA, Gil de Castro AR. Grid interconnection of renewable energy sources: Spanish legislation. Energy Sustain Dev 2010;14:104–9. doi:10.1016/j.esd.2010.03.003.
3. Elektrotechniker VD. Technical minimum requeriments for the connection to and parallel operation with the low-voltage distribution networks 2011.
4. Guerrero-Martínez M., Romero-Cadaval E, Minambres-Marcos V, Milanés-Montero MI. Supercapacitor Energy Storage System for Improving the Power flow in Photovoltaic Plants. Inf Midem-Journal Microelectron Electron Components Mater 2014;44(1):40–52.
5. IEC 61727. Photovoltaic (PV) systems – Characteristics of the utility interface. Int Electrothecnical Com 2004.
6. IEEE Std 1547. IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems 2003:1–28.
7. V 0126-1-1. Automatic disconnection device between a generator and the public low-voltage grid. VDE 2013.
8. Fairley P. How rooftop solar can stabilize the grid [News]. IEEE Spectr 2015;52:11–3.
9. Katiraei F, Sun C, Enayati B. No Inverter Left Behind: Protection, Controls, and Testing for High Penetrations of PV Inverters on Distribution Systems. IEEE Power Energy Mag 2015;13:43–9.
10. Romero-Cadaval E, Minambres-Marcos VM, Moreno-Munoz A, Real-Calvo RJ, Gonzalez de la Rosa JJ, Sierra-Fernandez JM. Active functions implementation in smart inverters for distributed energy resources. 2013 Int. Conf. Compat. Power Electron., IEEE; 2013, p. 52–7.
11. Moreno-Garcia I-M, Moreno-Munoz A, Domingo-Perez F, Pallares-Lopez V, Real-Calvo R-J, Santiago-Chiquero I. Implementation of a Smart Grid Inverter through Embedded Systems. Electron Electr Eng 2013;19:3–6. doi:10.5755/j01.eee.19.3.1378.
12. Mahela OP, Shaik AG, Gupta N. A critical review of detection and classification of power quality events. Renew Sustain Energy Rev 2015;41:495–505. doi:10.1016/j.rser.2014.08.070.
13. De la Rosa JJG, Fernandez JMS, Ayora-Sedeno D, Aguera-Perez A, Palomares-Salas JC, Moreno-Munoz A. HOS-based virtual instrument for power quality assessment. 2011 7th Int. Conf. Compat. Power Electron., IEEE; 2011, p. 1–5.
14. De la Rosa JJG, Sierra-Fernandez JM, Aguera-Perez A, Sedeno DA, Palomares-Salas JC, Montero AJ, et al. HOS and CBR measurement system for PQ assessment. 11th Int. Conf. Electr. Power Qual. Util., IEEE; 2011, p. 1–6.
15]. De la Rosa JJG, Moreno-Munoz A, Palomares JC, Aguera A. Automatic classification of Power Quality disturbances via higher-order cumulants and self-organizing networks. 2010 IEEE Int. Symp. Ind. Electron., IEEE; 2010, p. 1579–84.
16. Gonzalez de la Rosa JJ, Aguera Perez A, Palomares Salas JC, Moreno-Munoz A. Amplitude-frequency classification of Power Quality transients using higher-order cumulants and Self-Organizing

Maps. 2010 IEEE Int. Conf. Comput. Intell. Meas. Syst. Appl., IEEE; 2010, p. 66–71.
17. De la Rosa JJG, Moreno-Munoz A, Gallego A, Piotrkowski R, Castro E. Spectral Kurtosis based system for transients' detection: Application to termite targeting. 2009 IEEE Sensors Appl. Symp., IEEE; 2009, p. 188–93.
18]. De la Rosa JJG, Moreno A, Puntonet CG. A Practical Approach To Higher-Order Statistics. An Application to Electrical Transients Characterization. 2007 IEEE Int. Symp. Intell. Signal Process., IEEE; 2007, p. 1–6.
19. Moreno-Muñoz A. Power Quality. Springer London; 2007. doi:10.1007/978-1-84628-772-5.
20. Bollen M, Gu I, Santoso S, Mcgranaghan M, Crossley P, Ribeiro M, et al. Bridging the gap between signal and power. IEEE Signal Process Mag 2009;26:12–31.
21. Gu IYH, Ernberg N, Styvaktakis E, Bollen MHJ. A Statistical-Based Sequential Method for Fast Online Detection of Fault-Induced Voltage Dips. IEEE Trans Power Deliv 2004;19:497–504.
22. De Apráiz M, Barros J, Diego RI. A real-time method for time–frequency detection of transient disturbances in voltage supply systems. Electr Power Syst Res 2014;108:103–12. doi:10.1016/j.epsr.2013.11.007.
23. Moschitta A, Carbone P, Muscas C. Performance Comparison of Advanced Techniques for Voltage Dip Detection. IEEE Trans Instrum Meas 2012;61:1494–502. doi:10.1109/TIM.2012.2183436.
24. Radil T, Ramos PM, Janeiro FM, Serra AC. PQ Monitoring System for Real-Time Detection and Classification of Disturbances in a Single-Phase Power System. IEEE Trans Instrum Meas 2008;57:1725–33. doi:10.1109/TIM.2008.925345.
25. Agüera-Pérez A, Carlos Palomares-Salas J, de la Rosa JJG, María Sierra-Fernández J, Ayora-Sedeño D, Moreno-Muñoz A. Characterization of electrical sags and swells using higher-order statistical estimators. Measurement 2011;44:1453–60. doi:10.1016/j.measurement.2011.05.014.
26.] IEEE 929. IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems 2000:i – .
27. Hwang I, Kim S, Kim Y, Seah CE. A Survey of Fault Detection, Isolation, and Reconfiguration Methods. IEEE Trans Control Syst Technol 2010;18:636–53.
28. Basseville M, Nikiforov IV. Detection of abrupt changes: theory and application. 1993.
29. Gustafsson F. Adaptive filtering and change detection. 2000.
30. Gudzius S, Markevicius LA, Morkvenas A. Characteristics of Fault Detection System for Smart Grid Distribution Network. Electron Electr Eng 2011;112:123–6.
31. Moreno-Garcia IM, Moreno-Munoz A, Domingo-Perez F, Lopez VP, Real-Calvo R, de la Rosa JJG. Smart Grid Inverter Interface: Statistical approach applied to event detection. 2012 IEEE Int. Work. Appl. Meas. Power Syst. Proc., IEEE; 2012, p. 1–6. doi:10.1109/AMPS.2012.6343987.
32. Montgomery DC. Introduction to Statistical Quality Control. 2008.
33. Kenny P. Better Business Decisions from Data: Statistical Analysis for Professional Success. Apress; 2014.
34. Montero-Hernandez OC, Enjeti PN. A Fast Detection Algorithm Suitable for Mitigation of Numerous Power Quality Disturbances. IEEE Trans Ind Appl 2005;41:1684–90. doi:10.1109/TIA.2005.857459.
35. Redfern MA, Al-Nasseri H. Protection of micro-grids dominated by distributed generation using solid state converters 2008:670–4.
36. Pires VF, Guerreiro M. A Current Differential Line Protection Using a Synchronous Reference Frame Approach 2008:198–203.
37. Kuen-Der Wu, Jou H-L. An orthogonal peak detector for multiphase sinusoidal signals. IEEE Trans Instrum Meas 2000;49:1216–23.
38. Mansor M, Rahim NA. Voltage sag detection - A survey. 2009 Int. Conf. Tech. Postgraduates, IEEE; 2009, p. 1–6.
39. Lee D-M, Habetler TG, Harley RG, Keister TL, Rostron JR. A Voltage Sag Supporter Utilizing a PWM-Switched Autotransformer. IEEE Trans Power Electron 2007;22:626–35. doi:10.1109/TPEL.2006.890004.
40. Teke A, Saribulut L, Tumay M. A Novel Reference Signal Generation Method for Power-Quality Improvement of Unified Power-Quality Conditioner. IEEE Trans Power Deliv 2011;26:2205–14.
41. Moreno-García I, Moreno-Muñoz A, Pallarés-López V, Real-Calvo R. Platform for Embedded Systems Design in the Smart Grid Framework. In: Sambath S, Zhu E, editors. Adv. Intell. Soft Comput., vol. 133, Berlin, Heidelberg: Springer Berlin Heidelberg; 2012, p. 593–600. doi:10.1007/978-3-642-27552-4.
42. Noori MR, Jamali S, Shahrtash SM. Security assessment for a cumulative sum-based fault detector in transmission lines. 2011 10th Int. Conf. Environ. Electr. Eng., IEEE; 2011, p. 1–5. doi:10.1109/EEEIC.2011.5874792.
43. Mohanty SR, Pradhan AK, Routray A. A Cumulative Sum-Based Fault Detector for Power System Relaying Application. IEEE Trans Power Deliv 2008;23:79–86.

44. Xingze He, Man-On Pun, Kuo C-CJ. Quickest detection of unknown power quality events for smart grids 2012:1–4.
45. Bollen MH, Gu I. Signal Processing of Power Quality Disturbances. Wiley; 2006.
46. Subasi A, Yilmaz AS, Tufan K. Detection of generated and measured transient power quality events using Teager Energy Operator. Energy Convers Manag 2011;52:1959–67.

Arrived: 06. 06. 2015
Accepted: 04. 09. 2015

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 45, No. 3 (2015), 216 – 221

Thermal properties of polymer-matrix composites reinforced with E-glass fibers

Barbara Bertoncelj[1,2], Katarina Vojisavljević[3], Marko Vrabelj[2,3], Barbara Malič[3]

[1]Domel, d.o.o., Železniki, Slovenia
[2]Jožef Stefan International Postgraduate School, Ljubljana, Slovenia
[3]Jožef Stefan Institute, Ljubljana, Slovenia

Abstract: The influence of the fraction of the glass-fiber (EGF) reinforcement, from 0 to 15 wt%, on the thermal properties of the polymer-matrix composites with the $CaCO_3$ mineral filler is studied. The proper ratio of glass-fibers and mineral filler is important for obtaining good mechanical, and at the same time good thermal properties of the composites used in production of high-quality components in electro industry. For this purpose, the thermal stability and the thermal properties of the fiber-reinforced composites are determined from a set of different characterization techniques and linked with the microstructural changes induced by the different fiber content. The composites are stable upon heating to 260 °C, and undergo thermal oxidation between 280 and 560 °C, as found by thermogravimetric and differential thermal analysis. The specific heat capacity, C_p, of the composites slightly increases with increasing EGF content for 0 to 10 wt% EGF, with respective values 0.899 J/gK and 0.903 J/gK at 20 °C. Slightly lower C_p values of the composite with 15 wt% EGF could be related to a non-uniform distribution of EGF and presence of voids evidenced by scanning electron microscopy. Thermal conductivity of the composites decreases with increasing EGF content from 0.960(6) W/mK to 0.878(2) W/mK for 0 and 15 wt% EGF, respectively.

Keywords: glass-fiber composites; thermal stability; specific heat capacity; thermal conductivity

Toplotne lastnosti kompozitov na osnovi polimerov, ojačenih s steklenimi vlakni

Izvleček: V članku smo raziskovali toplotne lastnosti kompozitov na osnovi polimerov, ojačanih z različnimi deleži steklenih vlaken (od 0 do 15 utežnih %) in z dodanim mineralnim polnilom $CaCO_3$. Primerno razmerje steklenih vlaken in polnila omogoča doseganje dobrih mehanskih in istočasno tudi toplotnih lastnosti kompozitov, ki jih uporabljamo za proizvodnjo komponent v elektro-industriji. Toplotno stabilnost in toplotne lastnosti kompozitov smo analizirali z vrsto metod. S termično analizo smo zasledovali termično stabilnost in termični razpad kompozitov. Izkazalo se je, da so kompoziti termično stabilni do temperature ~ 260 °C, nato v temperaturnem območju od ~280 °C do 560 °C pride do oksidacije in termičnega razpada polimerne faze. Specifična toplotna kapaciteta, C_p, kompozitov narašča z naraščajočim deležem vlaken od 0 do 10 %. Nekoliko nižje vrednosti C_p kompozita s 15 % deležem vlaken povezujemo z nehomogeno razporeditvijo steklenih vlaken in prisotnostjo por v mikrostrukturi, ki smo jo analizirali z vrstičnim elektronskim mikroskopom. Toplotna prevodnost kompozitov se znižuje z naraščujočim deležem vlaken in je v območju od 0.960(6) W/mK do 0.878(2) W/mK za kompozita z 0 in 15 % vlaken.

Ključne besede: kompoziti s steklenimi vlakni; termična stabilnost; specifična toplotna kapaciteta; toplotna prevodnost

** Corresponding Author's e-mail: barbara.bertoncelj@domel.com*

1 Introduction

Glass-fiber reinforced polymer-matrix composites, including bulk molding compounds (BMCs) [1], are widely used in electro and automotive industry due to their easy processing, light weight, low cost and the possibility to tailor their properties. BMCs are available as pre-prepared mixtures of the polymer matrix, short glass fibers and mineral fillers. Such composites are usually processed by injection or compression molding – the techniques commonly used for mass production of small complex shaped components.

Functional properties of the composites strongly depend on the weight fractions and properties of in-

dividual constituents, i.e. polymer matrix, fibers and mineral filler particles. In assembling parts for electrical motors, such as housings, yokes and shaft insulation, the composite material should effectively dissipate the heat generated during the operation of the device to avoid possible defects. For that reason, the composite materials should have high thermal conductivity. The latter can be enhanced by incorporating fibers, metal or ceramic filler particles with high thermal conductivity, such as carbon fibers, carbon black powder, silver and alumina, into the polymer matrix [2-6].

It was shown that the thermal conductivity of the fiber reinforced composites is strongly influenced by the microstructural parameters, such as the fiber volume content, fiber diameter and fiber orientation [7].

Kalaprasad et al. studied the effect of fiber composition and fiber orientation of low-density polyethylene composite laminates reinforced with glass fibers in the amounts of up to 20 % on the thermal conductivity and thermal diffusivity at cryogenic and high temperatures. They observed that the thermal conductivity of the composites increased with the fiber content and with temperature. They also reported that the difference between the thermal conductivity parallel and perpendicular to the fiber direction was marginal because of the isotropic nature of the glass fibers [8].

In our previous work we investigated the effect of E-glass fibers (EGF) weight content and distribution on mechanical properties of the polymer-matrix composites. We found that the highest flexural strength along with the highest degree of the EGF distribution homogeneity was achieved for the samples with 10 and 15 wt% of EGF, i.e., 109 ± 4 MPa and 121 ± 15 MPa, respectively. Note that the polymer content was 21 wt%. At an even higher EGF weight content the flexural strength decreased, which was attributed to increased fiber-fiber interactions and consequent poorer stress transfer between the fibers, while at the EGF content below 10 wt% there were not enough fibers to give a sufficient mechanical strength to the composites [9].

The aim of this work was to study the effect of the EGF weight content and their microstructure on the thermal properties of the composites as this is important for their application in electro industry. The thermal stability of the composites was studied by thermal analysis, and the materials were analysed by differential scanning calorimetry, in the expected temperature interval of operation, i.e. between room temperature and 180 °C, so that the values of the specific heat capacity could be extracted. Furthermore, the thermal conductivity of the composites was measured at room temperature depending on the weight fraction of EGF.

2 Experimental

Four sets of BMC test samples were commercially prepared from compounds containing 21 wt% of polymer-matrix (PM) based on thermosetting unsaturated polyester and with varying fractions of EGF and $CaCO_3$ mineral filler (MF). The sample with the mineral filler only was prepared as reference. The composition of the samples, denoted as BMC-0, BMC-5, BMC-10 and BMC-15 in further text, is presented in Table 1.

Table1: Composition and density of the BMC composite samples.

Sample	PM (wt%)	EGF (wt%)	MF (wt%)	ρ (g/cm^3)
BMC-0	21	0	79	1.96
BMC-5	21	5	74	1.91
BMC-10	21	10	69	1.87
BMC-15	21	15	64	1.86

Compression molding technique was used to prepare the test specimens according to the standard ISO 3167 [10]. The dimensions of the specimens and the cutting position for obtaining the plan-view and cross-sectional samples for microstructural characterization are shown in Figure 1. The arrow indicates the flow of the compound during the molding process.

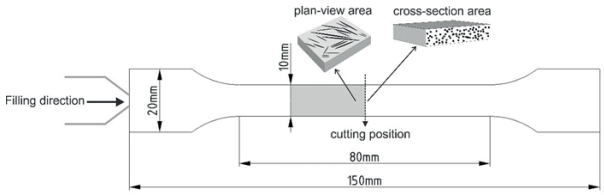


Figure1: Dimensions of the test specimens and the cutting position for obtaining the plan-view and cross-sectional surfaces for microstructural characterization. According to [11].

The samples for microstructural analysis were prepared by standard metallographic techniques. Field emission scanning electron microscope JSM-7600F (FE SEM, JEOL Ltd., Tokyo, Japan) was used for microstructural characterization. The polished plan-view and cross-section surfaces of all samples were sputter-coated with a thin carbon layer to avoid charging in SEM. SEM images were taken in the backscattered-electron mode (composition contrast mode - COMPO) at an accelerating voltage of 15 kV.

The density of the samples was determined by the water immersion technique and calculated according to the equation,

$$\rho = \frac{m_s}{m_s - m_w} \cdot \rho_w \quad (1)$$

where the m_s is the mass of the sample in the air, m_w is the mass of the sample when immersed in the water and ρ_w is the water density at room temperature [12].

Thermal stability of the samples was studied by thermogravimetric and differential thermal analysis (TG-DTA) using a thermal analyzer Netzsch STA 409 PC. The samples of about 5 mm in diameter and the thickness of ~ 3 mm were placed into platinum-rhodium crucibles and heated from room temperature to 650°C at a heating rate of 5K/min in synthetic air atmosphere.

The differential scanning calorimetry (DSC) curves were measured by a differential scanning calorimeter DSC 204 F1 (Netzsch, Germany). The samples of about 5 mm in diameter and the thickness of ~ 1 mm were put in Pt crucibles with lids, and heated in a calorimeter with a heating rate of 2°C/min from room temperature to 180°C. To determine the specific heat capacity C_p of the BMC samples, sapphire (Netzsch, diameter of 5.2 mm, thickness of 1 mm) was used as the standard material. The C_p values at different temperatures (20°C, 100°C and 180°C) were extracted from the linear fit of the experimental curve.

Thermal transport properties of the composites were measured with the transient plane source technique [13] by using the HotDisk TPS 2500S equipment (Hot Disk AB, Gothenburg, Sweden) at room temperature. The samples for measuring the thermal conductivity were also prepared by compression molding, but they were of different dimensions, i.e. 340×80×4 mm. During the HotDisk measurement a thin disk sensor (kapton, 2 mm diameter), used both as the heat source and the temperature monitor, was sandwiched between two individual samples. The material was heated at 50 mW for 5s. The length of the current pulse was chosen short enough so that the sensor could be considered in contact with an infinite solid throughout the transient recording. In this way the thermal properties of the surrounding material could be determined by measuring the temperature increase of the disk sensor in a short period of time. [14, 15]

3 Results and discussion

3.1 Microstructure

SEM micrographs of plan-view and cross-sectional areas of all composite samples are collected in Figure 2. In the BMC-0 sample we can observe irregularly shaped $CaCO_3$ filler particles with the sizes from a few μm up to a few 10 μm in the polymer matrix. Note that the plan-view and cross-sectional areas were very similar, meaning that the distribution of the filler particles does not depend on the compound filling direction (see Fig. 2a).

We observe that in the plan-view microstructures of the EGF-reinforced composites the fibers are mainly oriented in the direction of the compound filling flow during the molding process. This is also apparent from the intersections of the glass fibers in the cross-section micrographs (see Fig. 2b, d, f): namely, the cross-sections of the fibers that are perpendicular to the cutting position are circular and others, which are cut at an angle, are oval-shaped. At lower weight contents of EGF (≤ 10 wt%) the fibers are uniformly distributed in the PM. At the EGF content of 15 wt% we observe clustering of the fibers, meaning that their distribution is not homogeneous [9]. Presence of voids in the vicinity of the clusters may be related to a poor adhesion between the fibers and the PM in the latter sample (see Fig. 2f).

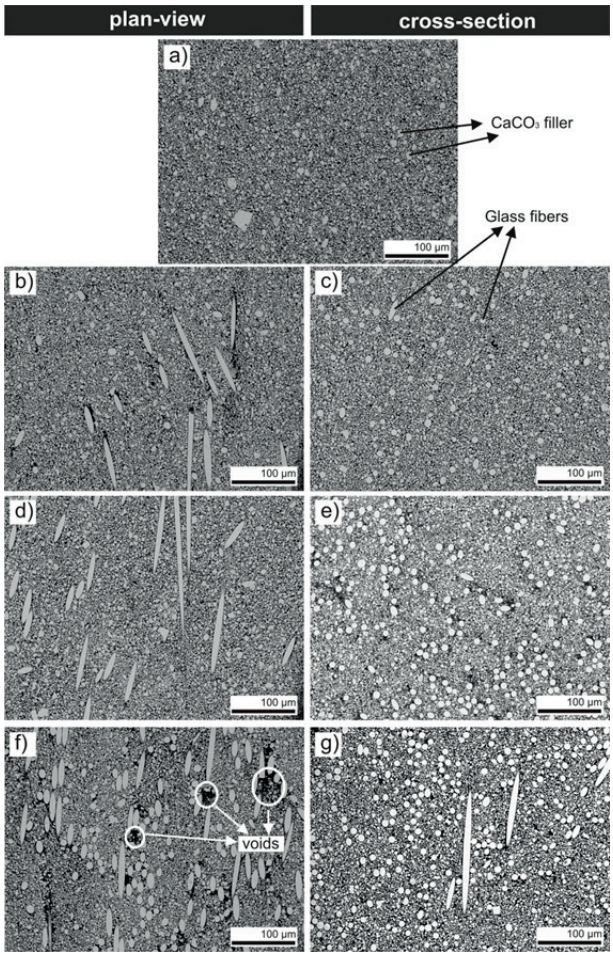


Figure 2: SEM micrographs of the plan-view and cross-sectional surfaces of the BMC samples: BMC-0: a, BMC-5: b, c, BMC-10: d, e, BMC-15: f, g.

The densities of the composite samples are slightly decreasing with increasing EGF weight fraction, from 1.96 g/cm^3 to 1.86 g/cm^3, for BMC-0 and BMC-15, respectively (cf. Table 1). Such small decrease could be tentatively connected to the porosity in the latter sample, but also to the increased weight fraction of the fibers. Note that the densities of the dispersed phases, EGF and $CaCO_3$ are quite similar, 2.54 g/cm^3 and 2.65 g/cm^3, respectively [16].

3.2 Thermal stability

The thermal analyses of the BMC-0 and BMC-10, which was selected as a representative EGF-reinforced composite, are collected in Figure 3. The TG-DTA curves reveal that the samples are thermally stable upon heating to 260°C. A slight inclination of the TG curves of both samples upon heating from room temperature to around 260°C, accompanied by a hardly discernible endothermic DTA signal, is attributed to evaporation of volatile species. The major weight loss occurs in the temperature range between 320°C and ~560°C and is accompanied by endothermic (383 °C) and exothermic (398 °C and 448 °C) events. It is attributed to the oxidation and thermal degradation of the PM [17]. Above the temperature of 560 °C only inorganic phase is still present, i.e. the glass fibers and $CaCO_3$ mineral filler, as confirmed by X-ray diffraction (pattern not shown here). The overall mass losses of 21.83 % and 20.85 % for the samples BMC-0 and BMC-10, respectively, correspond well to the initial content of the PM (21 wt%). This confirms the complete decomposition of the PM during the thermal treatment to 650°C.

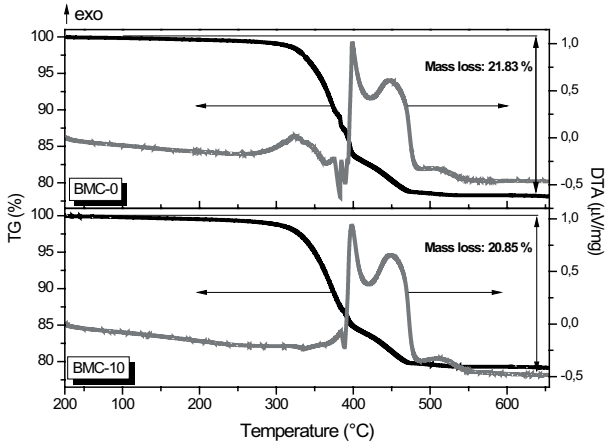


Figure 3: TG and DTA curves of the BMC-0 and BMC-10 composites.

The thermal stability of the composites confirmed by TG-DTA, i.e. the absence of any thermal effects between 25°C and 180°C, allowed us to measure the specific heat capacity, C_p, of the samples over the mentioned temperature interval by DSC. The C_p values at 20, 100 and 180°C were extracted from the linear fits of the C_p curves, calculated from the values of the heat flow measured during the heating of the sample.

The C_p of the sample with the mineral filler only, is 0.899 J/gK at 20 °C and it increases with temperature to 1.154 J/gK at 180 °C, see Table 2. The values of C_p of the samples with 5 and 10 wt% EGF are almost the same, and also very similar to the sample without EGF, and they show a similar, slight increase of C_p with temperature. Only the sample BMC-15 steps out from the observed trend, since the C_p values at all temperatures are lower than the values obtained for the samples without EGF or with lower EGF contents. This difference could be tentatively related to a non-uniform microstructure of the BMC-15 sample and/or to the presence of the voids between the clustered fibers, see Fig. 2f.

Table 2: Specific heat capacity (C_p) of the composites, obtained from the linear fit of the C_p experimental curves.

	C_p [J/gK]			
	BMC-0	BMC-5	BMC-10	BMC-15
20°C	0.899(1)	0.903(1)	0.903(1)	0.861(1)
100°C	1.027(1)	1.039(1)	1.038(1)	0.991(1)
180°C	1.154(1)	1.175(1)	1.174(1)	1.122(1)

3.3 Thermal conductivity

The thermal conductivity, λ, of the composites with different weight portions of EGF is shown in Figure 4. The values of λ for the composite BMC-0 is 0.960(6) W/mK and it decreases with increasing EGF content to 0.878(2) W/mK for the composite BMC-15.

The reported values of thermal conductivity for the polymer matrix, EGF and $CaCO_3$ mineral filler are respectively, a few 0.1 W/mK, ~1-1.3 W/mK and ~4.6-5.6 W/mK, see Table 3.

A slight decrease of the thermal conductivity of the polyamide-matrix composites with increasing glass fiber content (0 -5 wt%) was also observed by Li et al.

Table 3: Thermal conductivity, λ, of the polymer, glass fibers and $CaCO_3$ mineral filler obtained from literature.

	PM	EGF	$CaCO_3$
λ (W/mK)	0.12 – 0.50[16]; 0.1 – 0.3[18]	1.04[20]; 1[21]; 1.1[22]; 1.3[19]	5.6[20]; 4.6-5.5[23]

[22]. The composites contained alumina or magnesium hydroxide fillers with respective λ values of 30 and 80 W/mK. The authors explained that the decreased thermal conductivity of the composites was related to the formation of the thermally-resistive network of the glass fibers (cf. Table 3) which limited the heat transfer between the filler-particles. We propose a similar trend in our case, namely the increasing fraction of the heat-resistive glass fibers contributes to a gradual slight decrease of the thermal conductivity of the composites. In addition, the thermal conductivity of the composite with 15 wt% EGF could be affected also by the presence of voids, see Fig. 2f.

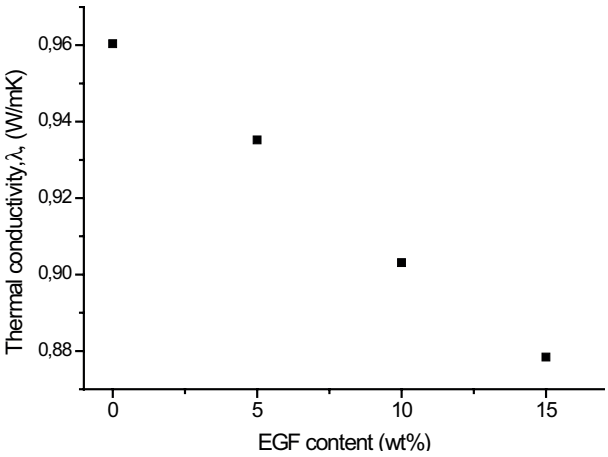


Figure 4: Thermal conductivity of the BMC samples versus the EGF content.

4 Conclusions

In the present study, we examined the thermal stability, specific heat capacity and thermal conductivity of the composites with glass-fibers in the amounts from 0 to 15 wt%. We found that the thermal stability of the composites is not influenced by the glass-fiber content, the composites proved to be stable to ~260 °C. The specific heat capacity of the composites slightly increases with the increasing glass-fiber content (0 to 10 wt%) and with temperature. However, the composite with the highest fiber content, 15 wt%, exhibited slightly lower values which could be tentatively related to its non-uniform microstructure. The thermal conductivity of the composites was found to slightly decrease with increasing fiber fraction, with the value of 0.878 W/mK for the composite with 15 wt% of fibers. Such decrease could be explained by the formation of the network of thermally resistive glass-fibers which effectively hinder the heat transfer through the material.

The right balance of the thermal properties, and fiber distribution homogeneity, necessary for a suitable mechanical performance can be achieved by tailoring the EGF and $CaCO_3$ mineral filler content. Based on the results presented in this and our previous work [9] the composites with 10 wt% showed optimal mechanical and thermal properties.

5 Acknowledgement

BB gratefully acknowledges the financial support of the Ministry for Education, Science and Sport of the Republic of Slovenia and the European Commission through the European Social Fund. BM and KV acknowledge the financial support of the Slovenian Research Agency (P2-0105).

We acknowledge Jena Cilenšek from Electronic Ceramics Department, Jožef Stefan Institute, for assistance with thermal analysis.

6 References

1. R. Burns, "Polyester molding compounds". New York, M. Dekker, 1982.
2. S. Han, D.D.L. Chung, "Increasing the through-thickness thermal conductivity of carbon fiber polymer-matrix composite by curing pressure increase and filler incorporation", Composite Science and Technology, Vol. 71, 2011, pp. 1944-52.
3. B. Rudin, D. Drummer, "Heat conductive thermosets for the injection molding process", 2nd International Electric Drives Production Conference (EDPC), Nuremberg, 2012, pp. 1-4.
4. Y. H. Yu., C.C.M. Ma, C.C. Teng, Y.L. Huang, H.W. Tien, S.H. Lee, I. Wang, "Enhanced thermal and mechanical properties of epoxy composites filled with silver nanowires and nanoparticles", Journal of the Taiwan Institute of Chemical Engineers, Vol. 44, 2013, pp. 654-9.
5. J. P. Hong, S.W. Yoon, T. Hwang, J.S. Oh, S.C. Hong, Y. Lee, J.D. Nam, " High thermal conductivity epoxy composites with bimodal distribution of aluminium nitride and boron nitride fillers", Thermochimica Acta, Vol. 537, 2012, pp. 70-5.
6. S. Li, S. Qi, N. Liu, P. Cao, "Study on thermal conductive BN/novolac resin composites", Thermochimica Acta, Vol. 523 (1-2), 2011, pp. 111-5.
7. R. Arambakam, H. V. Tafreshi, B. Pourdeyhimi, "A simple simulation method for designing fibrous insulation materials", Materials and Design, Vol. 44, 2013, pp. 99-106.
8. G. Kalaprasad, P. Pradeep, G. Mathew, C. Pavithran, S. Thomas, "Thermal conductivity and thermal diffusivity analyses of low-density polyethylene

composites reinforced with sisal, glass and intimately mixed sisal/glass fibres", Composites Science and Technology, Vol. 60, 2000, pp. 2967-77.
9. B. Bertoncelj, K. Vojisavljević, J. Rihtaršič, G. Trefalt, M. Huskić, E. Žagar, B. Malič, "A Voronoi-diagram analysis of the microstructures in bulk-molding compounds and its correlation with the mechanical properties". (submitted)
10. ISO 3167: Plastics-Multipurpose test specimens, International Organization for Standardization, Geneva, Switzerland. https://www.iso.org
11. B. Bertoncelj, K. Vojisavljević, J. Rihtaršič, G. Jelenc, B. Malič, "Effect of E-glass fiber and mineral filler content on microstructure, mechanical, dielectric and thermal properties of Bulk Molding Compound", 50th International Conference on Microelectronics, Devices and Materials proceedings., M. Topič (ed.), P. Šorli (ed.), I. Šorli (ed.), Ljubljana: MIDEM - Society for Microelectronics, Electronic Components and Materials, pp. 227-232, 2014.
12. M. N. Rahaman, "Ceramics Processing". CRC Press, Boca Raton, pp. 358-359, 2007.
13. S. E. Gustafsson, "Transient plane source technique for thermal conductivity and thermal diffusivity measurements of solid materials", Rev. Sci. Instrum. Vol. 797 (62), 1991, pp. 797-804.
14. Y. He, "Rapid thermal conductivity measurement with a hot disk sensor, Part 1.Theoretical considerations", Thermochimica Acta, Vol. 436 (1-2), 2005, pp. 122-129.
15. Y. He, "Rapid thermal conductivity measurement with a hot disk sensor, Part 2. Characterization of thermal greases", Thermochimica Acta, Vol. 436 (1-2), 2005, pp. 130-134.
16. W.D. Callister, "Materials science and engineering", New York, John Wiley & Sons, Inc., 2007.
17. A.P. Mouritz, Z. Mathys, A.G. Gibson, "Heat release of polymer composites in fire". Composites: Part A, Vol. 37, 2006, pp. 1040-54.
18. Barcelo, A.G. Kostianoy (ed.), "The Handbook of Environmental Chemistry, Vol. 11". Berlin, Springer-Verlag, 2010.
19. A. Patnaik, P. Kumar, S. Biswas, M. Kumar, "Investigations on micro-mechanical and thermal characteristics of glass fiber reinforced epoxy based binary composite structure using finite element method", Computational Materials Science, Vol. 62, 2012, pp. 142-51.
20. P.K. Mallick, "Particulate Reinforced Polymers". In Comprehensive composite materials: Chapter 2.09. A. Kelly (ed.), C.H. Zweben (ed.). Amsterdam, Elsevier, 2000.
21. Technical data sheet, Sain-Gobain Vetrotex, Germany. Available at: http://glassproperties.com/glasses/E_R_and_D_glass_properties.pdf
22. M. Li, Y. Wan, Z. Gao, G. Xiong, X. Wang, C. Wan, "Preparation and properties of polyamide 6 thermal conductive composites reinforced with fibers". Materials and Design, Vol. 51, 2013, pp. 257-61.
23. Almaz Optics, Inc., USA. Available at: http://www.almazoptics.com/CaCO3.htm

Arrived: 20. 07. 2015
Accepted: 16. 09. 2015

Boards of MIDEM *Society* | *Organi društva* MIDEM

MIDEM *Executive Board* | *Izvršilni odbor* MIDEM

Supervisory Board | Nadzorni odbor

Court of honour | Častno razsodišče

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
ISSN 0352-9045

Publisher / Založnik:
MIDEM Society / Društvo MIDEM
Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia
Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, Ljubljana, Slovenija

www.midem-drustvo.si