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MORPHOLOGICAL AND OPTICAL INVESTIGATION OF LEAD ZIRCONATE TITANATE (20/80) ULTRA-THIN FILMS

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Key words: Atomic Force Microscopy, Faceting, Optical Properties, Growth Mechanisms

Abstract: Ultra-thin (<20 nm) lead zirconate-titanate films with Zr/Ti ratio of 20/ 80 have been deposited on single crystal MgO substrates by sol-gel techniques. Atomic force microscopy reveals a smooth surface consisting of pyramids or domes. The surface morphology is discussed in terms of a double-step growth process: epitaxial growth in the early stages followed by growth on screw dislocations.

Measurements of the optical extinction spectra for the PZT (20/80) ultra-thin films are reported and modelled to extract the data on the energy gap.

Morfološke in optične raziskave ultratankih plasti PZT (20/80)

Kjučne besede: mikroskopija na atomsko silo, AFM mikroskopija, zirkonijevega titanata, optične lastnosti, mehanizmi rasti

Izvleček: Nanesli smo ultratanke plasti (<20 nm)zirkonijevega titanata z razmerjem Zr/Ti 20/80 na podlage iz kristalnega MgO s tehniko sol-gel. Preiskava z AFM mikroskopijo pokaže gladko površino sestavljeno iz piramidastih ali kupolastih struktur. Površinsko morfologijo razložimo z dvostopenjskim procesom rasti : začetna epitaksijalna rast, ki ji sledi rast na vijačnih dislokacijah.

Prikažemo tudi meritve optičnega ekstinkcijskega spektra ultratankih plasti PZT (20/80), ki jih uporabimo pri modeliranju in izračunu vrednosti za energijsko režo.

1. Introduction

Lead zirconate titanate, $Pb(ZrTi)O_3$ (PZT), ceramics have excellent ferroelectric and optical properties that make them useful for various electronic and optoelectronic applications /1/. Due to the refractive index dispersion n (λ), the low optical loss, high transmittance, together with the strong electro-optic Kerr effect, PZT thin films could also be used for optical and electro-optical applications, e.g. optical shutters and modulators /2/. Ultra-thin films (<20 nm) are particularly interesting in this respect since nonlinear effects become important if light can be confined within the film. Moreover, surface roughness becomes an important parameter to control if one seeks to fabricate thin films with optimal optical properties. Recently, new devices have been proposed composed of arrays of ferroelectric nano-capacitors made by self-patterned ultra-thin films /3, 4/.

Fundamental studies on ferroelectric properties show that the grain size and film thickness are important for the limit of ferroelectricity /5, 6, 7/. A number of papers /8-12/ have appeared recently covering different optical properties of ferroelectric PZT bulk ceramics and thin films. There is a lack of information on optical properties of PZT ultra-thin films. Generally, transmission (T) and reflection (R) spectra are used to determine the optical properties i.e. the absorption coefficient (n), the extinction coefficient (k) and the energy band gap (E_g) of thin films. Modelling of these spectra is very sensitive to errors, especially because different experimental set-ups are used. Usually, two methods are used for calculating the optical properties: the Swanepoel's method /11/ and transfer matrix formalism /12/. However, different characteristic values of the optical properties are obtained by applying these methods to the same sample /11, 12/. This difference is coming mainly from the "resolution" method. The basics of the Swanepoel´s method consist in solving the equations for T and R of the light with wavelength λ. The system of equations for T and R has more than one solution, since T and R values vary to a great extent with λ. The problem of guaranteeing that the system has a singular solution is solved using the maxima and minima of the transmission spectrum. Considering the Swanepoel's approach /11/ the experimental transmission spectrum is enclosed by the envelope function of the transmittance maxima (T_M) and by the envelope function of the transmittance minima (T_m) which are function of the wavelength λ (Figure 1). The strong drawback of this method it is that it induces errors when one draws the envelopes.

Recently, an alternative method has been proposed in order to determine the optical properties of ferroelectric thin films /12/. The key of the method consists of applying the transfer matrix formalism on modelling the complex dielectric function. The strong drawback of this procedure comes from the difficulty of the mathematical calculus that is rather complex and very sensitive to errors.

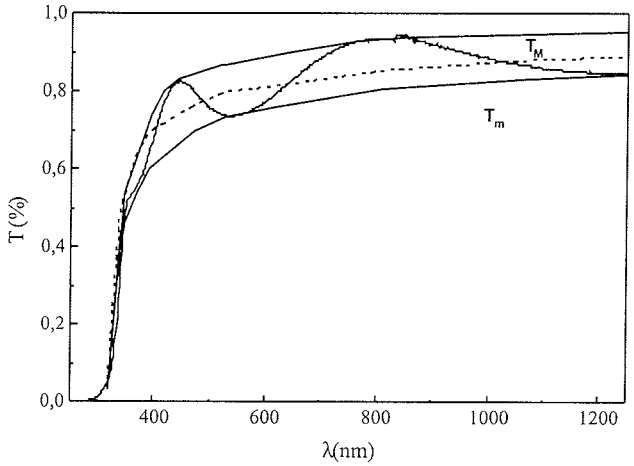

Figure 1. The T_M and T_m envelope of the experimental transmission spectra, according to Swanepoel's approach /11/.

In this work, optical extinction measurements are proposed as a quality check of the films of $PbZr_{0,20}Ti_{0,80}O_3$ as thin as 15 nm. Band gap energies (E_g) and the extinction coefficient (k) for these films are reported under the assumption of a direct band-to-band transition.

2. Experimental

Stoichiometric $PbZr_{0,20}Ti_{0,80}O_3$ films were prepared from the sols derived from methoxyethanol solutions. Lead acetate was dehydrated under vacuum (49 mbar) at room temperature for 15 hours. A 1M stock solution of Pb was obtained by mixing the anhydrous $Pb(CH_3COO)_2$ with 2-methoxyethanol followed by two vacuum distillations (60 mbar at 60 °C each) and dilutions with the solvent. Ti isopropoxide and Zr n-propoxide were mixed with 2-methoxyethanol, followed by two vacuum distillations (66 mbar at 80 °C each). The resultant solution was mixed with the Pb stock solution and 2-methoxyethanol. Two vacuum distillations (66 mbar at 90°C) were again performed to complete the reaction and remove any remaining reaction by-products. The Pb/Zr/Ti solution was partially hydrolysed with an equal volume of a 1 M water mixture in 2-methoxyethanol to obtain a 0.25 M sol.

The films were deposited on MgO (001) single crystal substrates by spin-coating. Prior to deposition, the substrate was thermally treated at 1100 °C for 1 hr to obtain well-defined vicinal surfaces and a reproducible surface finish /13/.

The sol was syringed through a 0.2 μm filter onto the substrate and spun at 6000 rpm/ 60 s. A two-step hot plate treatment was then used at 95 °C and 300 °C for 5 min each. Finally, the amorphous film was placed in an inverse-crucible configuration, together with some lead oxide powder to provide a lead oxide-rich atmosphere, and heated in a chamber furnace to 750 °C.

The surface microstructure of the films was characterized with Atomic Force Microscopy (AFM; Nanoscope IIIa). The equipment allowed the determination of the average surface roughness for selected areas and line scans to determine peak to trough height differences.

The optical extinction spectra were recorded at room temperature using a Carry 17D PC double beam UV-VIS-NIR scanning spectrophotometer.

3. Results and discussion

3.1. Atomic Force Microscopy

The AFM images of the ultra-thin $PbZr_{0.2}Ti_{0.8}O_3$ film, in Figure 2, reveal faceted structures that are either pyramids or domes /14/. The density of the pyramids is low, but these are very well defined, with a wide square base and four facets. The surface profiles indicate that the typical height of the pyramids is about 120 nm. The domes, which cover the majority of the substrate, are closely packed and have a square base top surface, and four faces. The film surface is smooth; the average root mean square (rms) roughness is 5 nm, calculated from the AFM data. The height of the domes and equivalently the thickness of the film were estimated at 15 nm. This was measured using a step, made during the sample processing.

Three different structures, domes, super-domes and pyramids, were observed on tetragonal PZT (52/48) films deposited on Nb doped $SrTiO_3$ substrates /15, 16/. The morphology depended on the dilution of the precursor solutions and the crystallisation temperatures. In our work, only pyramids and domes were observed. As depicted in Figure 2, some of the domes resemble "super-domes" /16/, but this could be an artefact; the angle of the tip used for the AFM analysis is about 8°, which could blur the real profile /17/. A similar morphology to that seen in the present work has been reported for germanium grown on silicon by Metalorganic Chemical Vapour Deposition (MOCVD) /18, 19/.

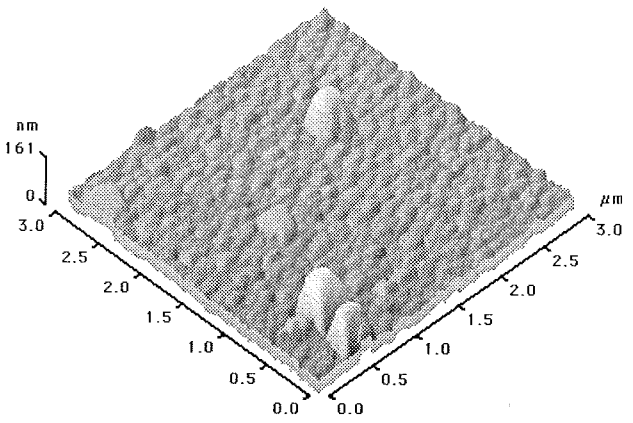

Figure 2. Atomic force microscope image of the surface of the $PbZr_{0.2}Ti_{0.8}O_3$ film, deposited on single crystal MgO.

It was mentioned that AFM revealed closely-packed domes having no holes or empty space in between them. The kinetic model, presented by Srolovitz /20, 21, 22/, explains the formation and evolution of holes in a continuous film as the direct result of volume diffusion and surface evaporation/ condensation. Lead diffuses readily from the bulk of the film to its surface in $Pb(Zr,Ti)O_3$. These phenomena lead to compositional inhomogeneities, due to segregation and evaporation. Additionally, this diffusion promotes the formation of capillary holes through the film thickness. Hence, the suppression of lead oxide surface evaporation by using lead oxide rich atmosphere also reduces the initiation of capillary holes and their further evolution.

The very low roughness of the film could be explained by the following model of nucleation and growth. The base of the domes is wider than their height, suggesting that lateral growth preferentially takes place. In the early stages of crystallisation, the first 2 to 6 monolayers, perovskite nuclei having stoichiometric composition, form on the MgO surface /23/. These nuclei spread laterally and coalesce, due to the very good lattice match between the MgO (a_{MgO} = 0,421 nm) and PZT (a_{PZT} = 0,414 nm), forming an epitaxial film. As the temperature increases, the film acts as a site for uniform growth in three dimensions, either perpendicular or horizontal to the substrate surface /23, 24/; in turn, large dome structures will grow. Strain induced dislocations are present not only at the film-substrate interface, but also develop in the growing epitaxial film. The dislocation periodicity decreases as the film thickness increases, due to the greater stress relaxation. At higher temperatures, the greater surface mobility increases the rate of growth on imperfections leading to a low density of large faceted pyramids resulting in smooth PZT film /25/.

3.2. Optical characterisation

Optical extinction (E) spectra were recorded to characterise the optical properties and to determine the band transition energy of the ultra-thin film. Given the low density of pyramids, one can assume that the optical extinction is measured on a film, about 15 nm thick, composed of domes. An MgO substrate, heat treated at 1100 °C for 1 hour, was used as the reference body. The spectra are presented in Figure 3. A local maximum is present between 3 5 - 3.6 eV (Fig. 2).

According to the Beer-Lambert law, the absorption coefficient (a) is related by the optical extinction (E) and film thickness (d) by the following relationship:

$$\alpha = E/d \qquad (1).$$

The extinction coefficient (k) is directly connected with the absorption coefficient by the relation /10/:

$$\alpha = 4\pi k / \lambda \qquad (2),$$

where λ is the wavelength. Thus, the equation (1) and (2) could be used to obtain the dispersion relationships for k

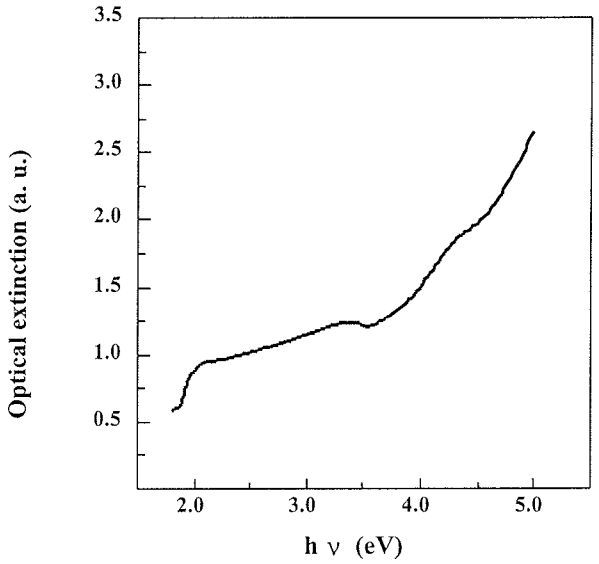

Figure 3. Optical extinction spectrum of the $PbZr_{0.2}Ti_{0.8}O_3$ film on MgO.

versus wavelength. To our knowledge, this is the first report for k of ultra-thin PZT films. The latter is shown in Figure 4.

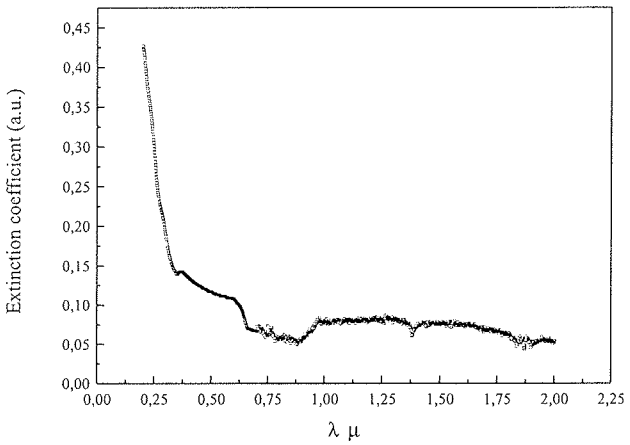

Figure 4. The extinction coefficient k of PZT (20/80) ultra-thin film on MgO as a function of the wavelength.

The extinction coefficient of the film is nearly constant ($k \approx 0,08$) for $\lambda > 1\,\mu m$ and rapidly increases for shorter wavelengths. This increase is related to an interband absorption in PZT (20/80).

Moreover, for a direct band gap material, the absorption coefficient can be expressed as a function of the incident photon energy (hn):

$$\alpha = (\tilde{A}\, h\nu)(h\nu - E_g)^{1/2} \qquad (3)$$

where A is a constant and E_g is the band gap /10/.

Thus, the plot $d(\ln(\alpha h\nu))/d(h\nu)$ vs. $h\nu$ in Figure 5, will have a divergence at $h\nu = E_g$ /26/, which corresponds to a transition energy of 3.52 eV. This is in reasonable agreement

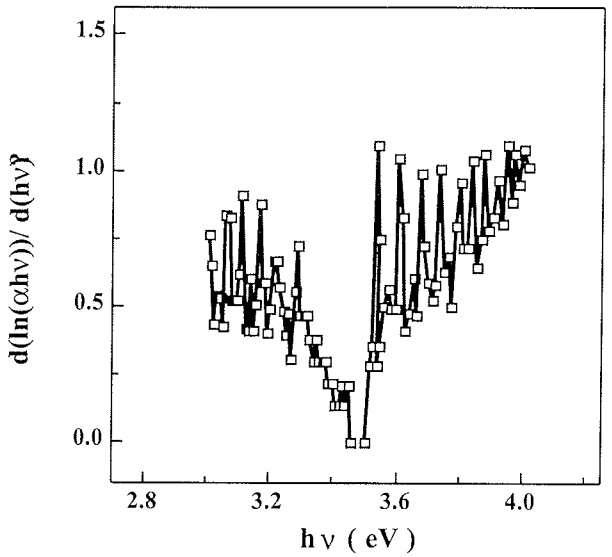

Figure 5. Plot of d(ln(αhν))/ d(hν) vs. hν. The observed divergence at hν = 3,52 eV is attributed to a band transition.

with the value reported in the literature for the band gap energy (E_g) of PZT (20/80) thin films /10, 26, 27/.

Figure 6 is the plot of $(\alpha h\nu)^2$ vs. hν where a linear behaviour can be seen at high photon energies. Such behaviour has been observed for PZT materials and attributed to a direct band transition /10, 28/.

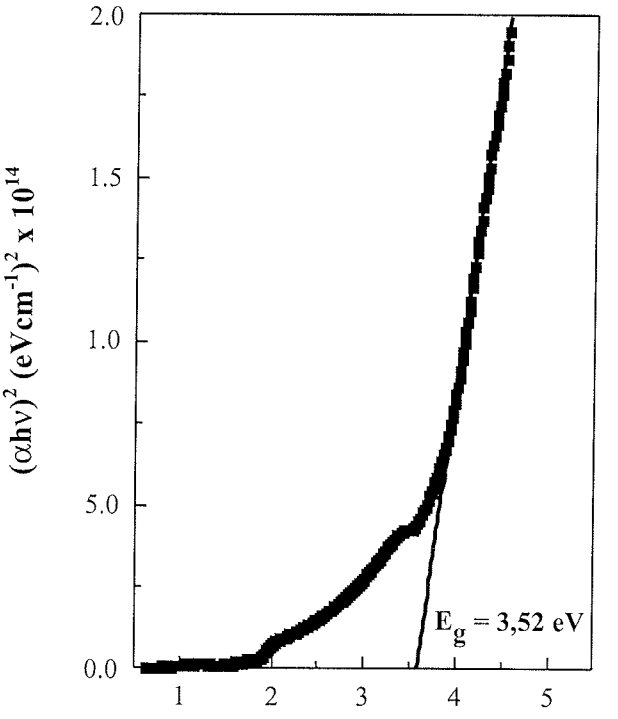

Figure 6. Plot of $(\alpha h\nu)^2$ vs. hν for the $PbZr_{0.2}Ti_{0.8}O_3$ film.

4. Conclusions

PZT (20/80) ultra-thin films have been deposited on MgO (001) substrate by sol-gel techniques. Dilute solutions and high rotation rates were utilized to obtain films approximately 15 nm thick. The surface morphology of the film was analyzed by AFM techniques, which evidenced a complex structure, consisting of pyramids and domes. The density of pyramids is low; however, the domes are closely packed and completely cover the substrate. This leads to a relatively smooth film.

Optical extinction spectra permit the calculation of band transition energy equal to 3.52 eV. Linear behaviour at high incident photon energy indicates a direct band-to-band transition in PZT ultra-thin films.

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THICK-FILM RESISTORS WITH LOW AND HIGH TCRS ON LTCC SUBSTRATES

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Key words: thick-film, resistors, NTC, LTCC, interactions, electrical parameters

Abstract: Low-Temperature Co-fired Ceramic (LTCC) materials, which are sintered at the low temperatures typically used for thick-film processing, i.e., around 850°C, are widely used for ceramic multi-chip modules (MCM-C). Thick-film resistors with low TCRs (Du Pont, 2041, nominal sheet resistivity 10 kohm/sq.) and thick-film NTC thermistors with high negative TCRs (EMCA-Remex, 4993, nominal resistivity 1 kohm/sq.) which were developed for alumina substrates, were evaluated on glassy LTCC substrates. The electrical and microstrutural characteristics of films fired on alumina or co-fired on "green" LTCC substrates were compared. The electrical characteristics (TCRs, sheet resistivities and noise indices) of 2041 resistors fired on both substrates are similar indicating that the resistors are compatible with the LTCC material. In the case of the NTC 4993 thermistors the resistivities, beta factors and noise indices of the thermistors fired on LTCC substrates significantly increased, indicating the interactions between the thermistor layers and the LTCC substrates. The changes in the electrical parameters were attributed to the diffusion of a silica-rich phase from the LTCC into the thermistor films.

Debeloplastni upori z nizkimi in visokimi odvisnostmi upornosti od temperature na LTCC substratih

Kjučne besede: debeli filmi, upori, NTC, LTCC, interakcije, električne karakteristike

Izvleček: Keramika z nizko temperature žganja (LTCC - Low temperature co-fired ceramics) se sintra pri temperaturah, tipičnih za debeloplastno tehnologijo, to je okrog 850°C. Uporablja se za izdelavo keramičnih večplastnih struktur (MCM-C). Debeloplastni upori z nizkimi TCR (Du Pont, 2041) in debeloplastni NTC termistorji (EMCA Remex, 4993), ki so bili razviti za žganje na inertnih Al_2O_3 substratih, so bili testirani na steklastih LTCC podlagah. Primerjane so električne in mikrostrukturne karakteristike plasti, žganih na Al_2O_3 in LTCC podlagah. Električne karakteristike (plastne upornosti, TCR in šum) 2041 uporov, žganih na obeh vrstah podlag, so primerljivi, kar pomeni, da so testirani upori kompatibilni z reaktivnimi LTCC podlagami. Za NTC 4993 termistorje so rezultati pokazali, da upornosti, beta faktorji (strmina odvisnosti upornosti od temperature) in šum narastejo po žganju na LTCC podlagah. Spremembe električnih karakteristik pripisujemo predvsem difuziji SiO_2 bogate steklaste faze med žganjem iz LTCC v NTC upore.

Introduction

Ceramic multi-chip modules (MCM-Cs) are multilayer substrates with buried conductor lines, which means they have a high density of interconnections. An additional advantage of the smaller size and higher density is the ability to integrate screen-printed resistors, or occasionally, capacitors and inductors. These screen-printed components can be placed either beneath the discrete components on the surface of the multilayer dielectric or buried within the multilayer structure. Low-temperature co-fired ceramic (LTCC) materials, which are sintered at the low temperatures typically used for thick-film processing, i.e., around 850°C, are widely used for the production of MCM-Cs, especially for telecommunications and automotive applications. LTCCs are either based on crystallisable glass or a mixture of glass and ceramics; for example, alumina, silica or cordierite ($Mg_2Al_4Si_5O_{18}$) /1-6/. The composition of the inorganic phase in most LTCC tapes is similar to, or the same as, materials in thick-film multilayer dielectric pastes. To sinter to a dense and non-porous structure at these, rather low, temperatures, it has to contain some low-melting-point glass phase. This glass would (or could) presumably interact with, for example, thick-film resistors leading to changes in the electrical characteristics. Some of the results for the resistor/LTCC combinations and the influences on the electrical characteristics can be found in /7-10/.

The main required characteristics for thick-film resistor materials are a long-term stability and relatively narrow tolerances of the sheet resistivities after firing. A very important characteristic is a low temperature coefficient of resistivity (TCR), which for most modern resistors is around or under $100x10^{-6}$/K. However, for temperature-sensing or temperature compensating applications the resistors with a large temperature dependence of resistivity - thermistors -are required. The thermistors with negative TCRs have very large and strongly non-linear temperature vs. resistivity dependence. The dependence of the specific resistance ρvs. temperature is described by:

$$\rho = \rho_0 \times \exp(B/T) \quad (1)$$

where ρ_0 is the resistivity (ohm.cm) at "infinite" temperature, T(K) is the temperature and B (K) is the thermistor constant (also called the beta factor or the coefficient of temperature sensitivity). Resistivity at "infinite" temperature is determined by the total number of "B" lattice sites in a spinel structure that can take part in the "hopping" conductivity process (there is no contribution to the overall conductivity if ions with different valences are on the A sites because the distance between the two A sites in a spinel lattice is too great for an electron "hopping" mechanism). The B is defined as the ratio between the activation energy for electrical conduction and the Boltzman constant. Basically it is a "steepness" of the resistivity vs. temperature curve. For the calculation of B from measured resistances at different temperatures the equation (1) is normally rewritten as

$$B = \ln (R_1/R_2) / (1/T_1 - 1/T_2) \quad (2)$$

where T(K) is again the temperature and R_1 and R_2 (ohm) are the resistances at T_1 and T_2, respectively.

These materials with large, negative TCRs (NTC) are based on solid solutions of transition-metal oxides. Mostly, due to their long-term stability, the compounds are solid solutions of Mn_3O_4, Co_3O_4 and NiO oxides with the spinel structure /11-13/. The general formula of the spinel structure is AB_2O_4. It is based on oxygen atoms arranged in an fcc (face-centred-cubic) structure containing tetrahedral (A) and octahedral (B) lattice sites. The electrical charge transport is via the hopping of electrons between the B^{3+} and B^{4+} ions present at the octahedral sites in the lattice. This is shown schematically in Fig. 1 for the NiO-doped Mn_3O_4. The spinel Mn_3O_4 (Mn^{2+} $2Mn^{3+}O_4$) is non-conducting. When some of the manganese 3+ ions are substituted by the nickel 2+ ions the same number of manganese ions change their valence from 3+ to 4+ in order to preserve the overall electrical neutrality. Electron hopping between the Mn^{3+} and the Mn^{4+} can take place.

The values of the resistivities and the beta factors of the NTC materials depend on the ratio of the oxides. The resistivities range from a few hundred ohm.cm to a few tens of kohm.cm, and the beta factors from 2500 K to 4000 K. These electrical characteristics are shown in the ternary phase diagram of Mn-Co-Ni-oxides for the resistivities (Fig. 2.a) and the beta factors (Fig. 2.b) /13/. The compositions with minimum resistivities, and maximum and minimum beta factors are indicated by arrows. The solid solutions with the lowest resistivities (rich on manganese oxide) also have the lowest temperature coefficients of expansion, i.e. 8.2×10^{-6}/K. A partial substitution of the iron ions (3+) on the B sites or the copper ions (1+) on the A sites increases or decreases the resitivities, respectively /14-17/.

Conductivity – electron "hopping"

"A" sites	"B" sites		
Mn^{2+}	$Mn^{3+}Mn^{3+}$	O_4	– non-conducting
	$\mathbf{xNi^{2+}}$ $\mathbf{xMn^{4+}}(2\text{-}x)Mn^{3+}$	O_4	- conducting

$Mn^{4+} + e^- \text{----------} > Mn^{3+}$

Fig. 1. Conductivity mechanism in NiO-doped Mn_3O_4 spinel - schematic

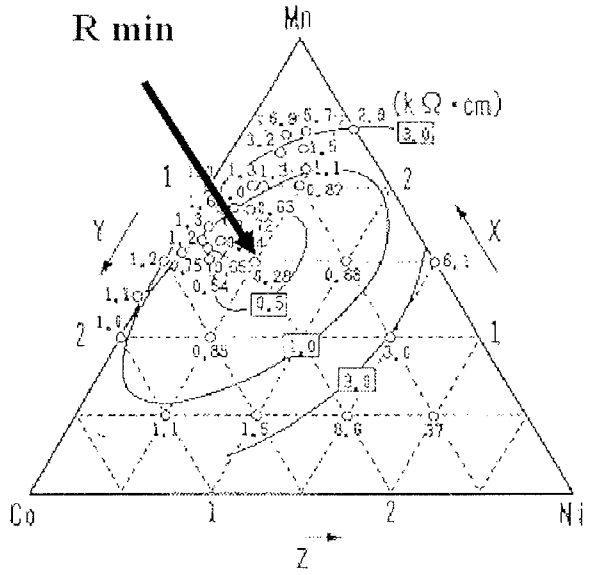

Fig. 2.a: Ternary phase diagram of Mn-Co-Ni-oxides. The minimum resistivity is indicated by the arrow /13/

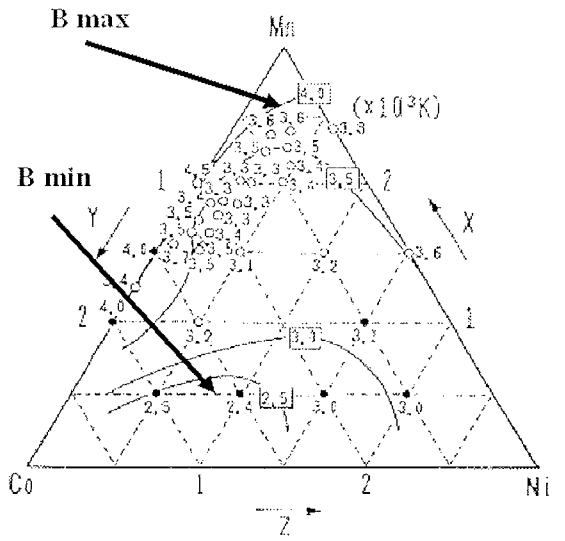

Fig. 2.b: Ternary phase diagram of Mn-Co-Ni-oxides. The maximum and minimum beta factors are indicated by the arrows /13/

The fired thickness of the thick-film layers is usually between ten and twenty micrometers. As mentioned before, the resistivities of the different spinel compositions are between a few hundred ohm.cm and a few tens of kohm.cm, and can be increased up to 1 Mohm.cm with the partial substitution of manganese ions with iron ions. These are useful values for pellet-type components. How-

ever, due to the dimensions of the thick-film resistors the values of the sheet resistivities (ohm/sq.) are between two and three orders of magnitude higher than the resistivities (ohm.cm) of the materials themselves. The glass phase, which is added for better sintering of the thick-film layers at relatively low firing temperatures (850°C), further increases the resistivity. Therefore, materials for thick-film NTC resistors usually include some phase with a low specific resistance, generally RuO_2. RuO_2 has a relatively low specific resistivity, 40 x 10^{-6}ohm.cm, and a positive, linear, metallic-like dependence of resistivity vs. temperature, with a TCR of 7000x10^{-6}/K for single crystals and a few 1000x10^{-6}/K for sintered microcrystalline samples /18,19/. The addition of ruthenium oxide decreases the specific resistance, reduces the noise and improves the stability of the resistors. However, due to the RuO_2 high, positive and linear metallic-like TCR /14,20/ it also decreases the beta factors.

As most of the thick-film resistors were developed for firing on alumina substrates their compatibility with (rather glassy) LTCC substrates needs to be evaluated. The aim of this work is to compare the electrical and microstrutural characteristics of the low TCR "normal" thick-film resistor 2041 (10 kohm/sq., Du Pont) and the 4993 NTC thermistor (1 kohm/sq., EMCA Remex) fired on 96% alumina and co-fired on Du Pont LTCC 951 substrates. The 2041 resistor was chosen because of its high stability and low noise. The conductive phase is based on a mixture of RuO_2 and $Pb_2Ru_2O_{6.5}$ /21,22/. The nominal beta factor of NTC 4993 thermistors is 1200 K. As mentioned above, both thick-film materials were developed for alumina substrates.

The X-ray spectra of the Du Pont LTCC 951 tapes, unfired and fired at 850°C, are shown in Fig. 3 /23/. The unfired material is a mixture of alumina and glass. After firing, peaks of anorthite ($(Na,Ca)(Al,Si)_4O_8$) phase appear. The peaks of alumina and anorthite are denoted by "A" and asterisk, respectively.

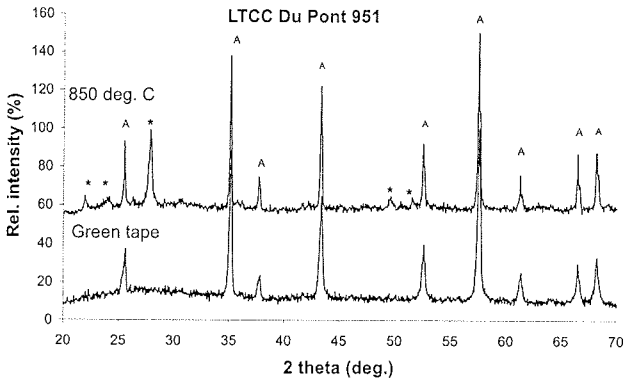

Fig. 3: X-ray spectra of green and fired (850°C) Du Pont LTCC 951 tapes /16/. The peaks of alumina and anorthite are denoted "A" and asterisk, respectively

Experimental

The 2041 resistors and NTC 4993 thermistors were screen printed and fired for 10 min at 850°C on 96% alumina and on green LTCC (951, Du Pont) substrates. The LTCC substrates were made by laminating three layers of LTCC tape at 70°C and at a pressure of 200 bar. The thick-film resistors were terminated by Pd/Ag electrodes that were pre-fired at 850°C on alumina substrates, and cofired together with the printed thermistors and LTCC substrates. The dimensions of the resistors for the microstructural analysis and the X-ray diffraction (XRD) analysis, which were printed and fired without conductor terminations, were 12.5x12.5 mm^2.

For the microstructural investigation the samples were mounted in epoxy in a cross-sectional orientation and then cut and polished using standard metallographic techniques. A JEOL JSM 5800 scanning electron microscope (SEM) equipped with an energy-dispersive X-ray analyser (EDS) was used for the overall microstructural and compositional analysis. Note that boron oxide, which is also present in the glass phase, cannot be detected in the EDS spectra because of the low relative boron weight fraction in the glass and the strong absorption of the boron K_α line during EDS analysis in the glass matrix. Dried thermistors (150°C) and thermistors fired at 850°C were analysed by X-ray diffraction (XRD) analysis with a Philips PW 1710 X-ray diffractometer using Cu K_α radiation. X-ray spectra were measured from 2 Θ=20° to 2 Θ=70° in steps of 0.02°.

Cold (from -25°C to 25°C) and hot (from 25°C to 125°C) TCRs were calculated from resistivity measurements at - 25°C, 25°C, and 125°C. The current noise was measured in dB on 100-mW loaded resistors using the Quan Tech method (Quan Tech Model 315-C).

Results and discussion

2041 resistors

X-ray spectra of dried 2041 resistors and resistors fired at 850°C on alumina and LTCC substrates are shown in Fig. 4. The spectra of RuO_2 (denoted RuO2) and $Pb_2Ru_2O_{6.5}$ (denoted RU) are added. As mentioned above the conductive phase of the 2041 resistor material is based on a mixture of ruthenium oxide and ruthenate. The spectra of 2041 resistors, fired on alumina and LTCC substrates, are nearly the same, which indicates the compatibility of the 2041 with LTCC.

The microstructure of the surface of the 2041 resistor, fired at 850°C is shown in Fig. 5. Cross-sections of the 2041 fired at 850°C on alumina and LTCC substrates are shown in Figs. 6.a and 6.b, respectively. The substrate is on the right. The 2041 resistor is a multiphase mixture consisting of conductive phase (white grains), dark-grey grains (rich in Si and Zr, presumably $SrZrO_4$), and a light-grey glass phase.

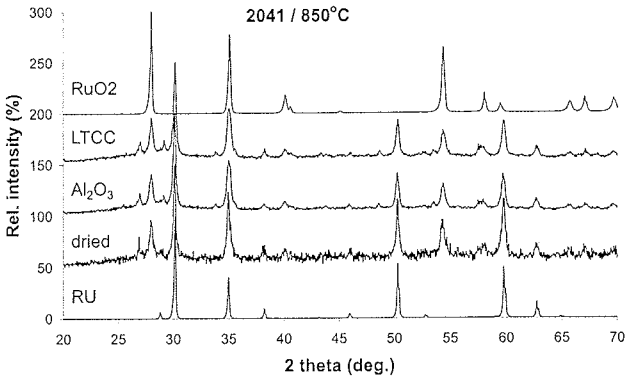

Fig. 4: X-ray spectra of dried 2041 resistors and resistors fired at 850°C on alumina and LTCC substrates. The added spectra of RuO_2 and $Pb_2Ru_2O_{6.5}$ are denoted RuO2 and RU, respectively.

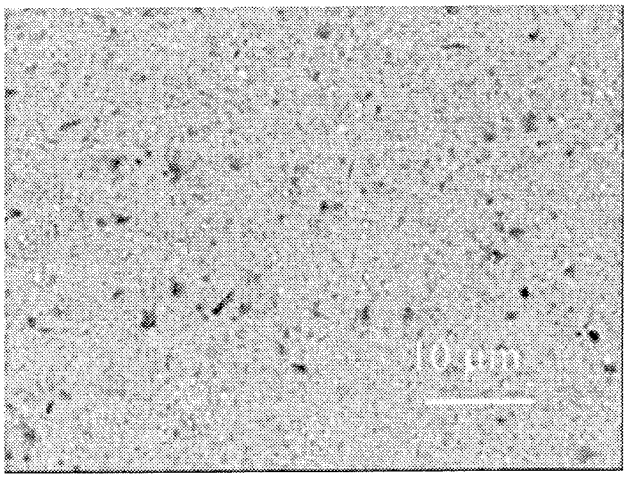

Fig. 5: The microstructure of the surface of the 2041 resistor, fired at 850°C

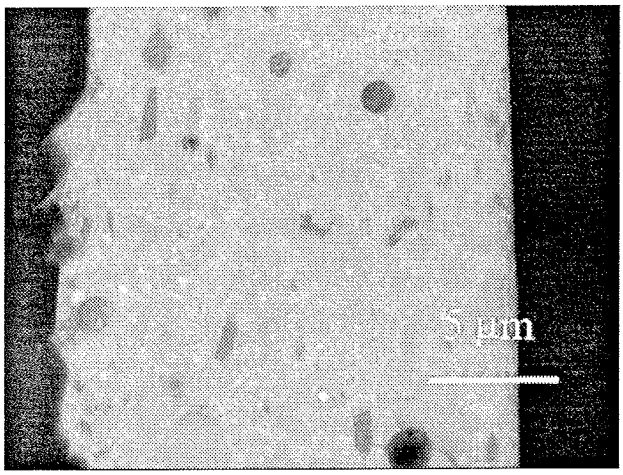

Fig. 6.a: Cross-section of the 2041 resistor, fired at 850°C on alumina. The alumina substrate is on the right.

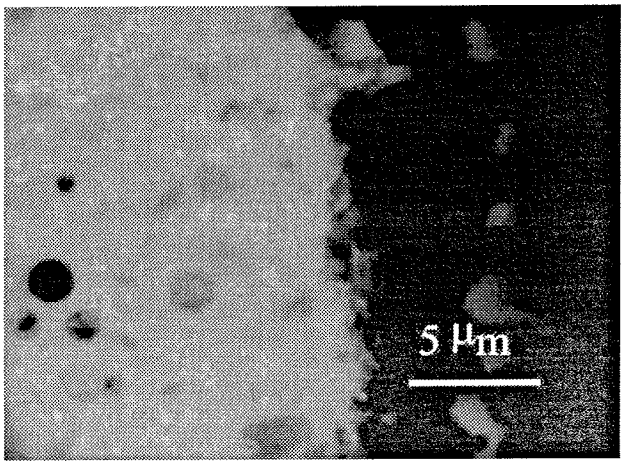

Fig. 6.b: Cross-section of the 2041 resistor, fired at 850°C on LTCC. The LTCC substrate is on the right.

The EDS micro-analyses over the whole cross-sections of the 2041 films (area 15x15 um^2) on the alumina and LTCC substrates are presented in Table 1. The compositions are given for elements and for oxides in at. % and mol. %, respectively. The concentration of oxygen is calculated by difference and not measured directly. The concentrations of the elements are similar for the resistors fired on alumina and on LTCC substrates. This indicates that there was no significant (or observable) interaction between the glassy LTCC material and the 2041 resistor.

Table 1: The EDS analyses of the concentration of elements (in atomic %) and oxides (in mol. %) in the 2041 films fired at 850°C on the alumina and LTCC substrates

Element (at. %)	Al_2O_3 substrate	LTCC substrate	Oxide (mol. %)	Al_2O_3 substrate	LTCC substrate
Mg	/	<1	MgO	/	<3
Al	4	3	$AlO_{1.5}$	11	8
Si	17	17	SiO_2	45	44
Ca	2	4	CaO	5	10
Zn	1	1	ZnO	3	3
Zr	<1	<1	ZrO_2	<3	<3
Ru	6	6	RuO_2	16	15
Ba	1	1	BaO	3	3
Pb	6	5	PbO	16	13
O	67	66			

The electrical characteristics, i.e., sheet resistivities, cold (-25°C to 25°C) and hot (25°C to 125°C) TCRs and noise indices of the 2041 resistors fired on alumina and LTCC substrates are shown in Table. 2. Note that the noise indices are expressed in "dB" and "uV/V". These two units are "connected" with a simple equation, i.e,. noise (dB) = 20 x log noise (uV/V) The dependence of the relative sheet resistivities vs. temperature of the 2041 resistors fired at 850°C on alumina or LTCC substrates is shown in Fig. 7.

Table 2: Sheet resistivities, cold (-25°C to 25°C) and hot (25°C to 125°C) TCRs, and noise indices of the 2041 resistors on alumina and on LTCC substrates.

Substrate	R sheet (ohm/sq.)	Cold TCR ($x10^{-6}$/K)	Hot TCR ($x10^{-6}$/K)	Noise (dB)	Noise (uV/V)
A_2O_3	850	2540	2580	-11	0,28
LTCC	180	3070	3075	-32	0,02

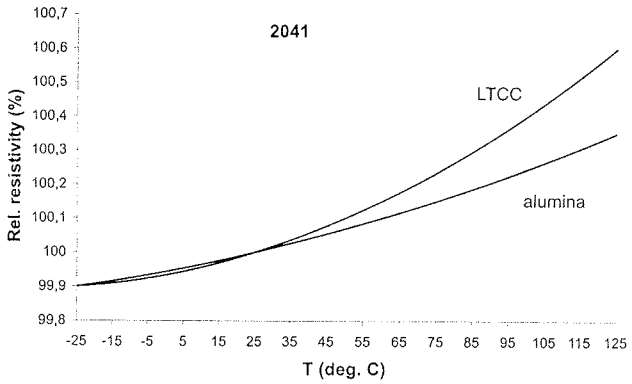

Fig. 7: Relative resistivity vs. temperature of the 2041 resistors fired at 850°C on alumina or LTCC substrates

The electrical characteristics, summarised in the Table 2, tentatively confirm that there is no significant interaction between the 2041 resistor material and the glassy LTCC substrates. The resistivity vs. temperature curve of resistors fired on LTCC substrates is a little more "steep", but the TCR values are still well inside the required +/- 100x10^{-6}/K values. All the presented results, i.e., XRD and EDS analyses as well as electrical characteristics strongly indicate the (very useful) compatibility between the 2041 resistors and the LTCC substrates when resistors are cofired on the LTCC.

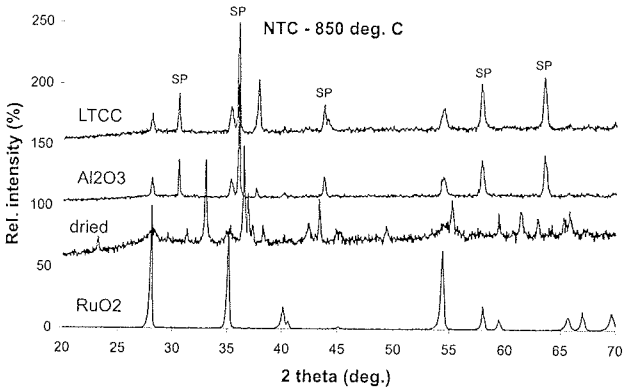

Fig. 8: The X-ray diffraction spectra of the NTC 4993 thermistors fired at 850°C on alumina and on LTCC substrates. The spectrum of ruthenate, denoted "RuO2", is also included. Peaks of spinel phase are denoted "SP".

NTC 4993 thermistors

The X-ray diffraction spectra of the NTC 4993 thermistors dried at 150°C and fired at 850°C on alumina and cofired on LTCC substrates are shown in Fig. 8. The spectrum of ruthenium oxide, denoted "RuO2", is also included in the graph. It is interesting to note that peaks of spinel phase (denoted "SP") appear after firing, but are not present in the dried thick-film. This means that the active phase is formed during the firing and is not included as a prereacted compound. In the fired layers the X-ray analyses show mainly spinel and RuO_2, which is added to the thick-film NTC materials, as mentioned in the Introduction, to decrease the specific resistance and to improve the stability and the current noise. The presence of a few (unmarked) X-ray peaks, most notably the one at 2 Θ = 38°, could be tentatively attributed to un-reacted oxides. The temperature of the formation of the spinel solid solution in the investigated thick-film NTC thermistors, as seen from the X-ray spectra, is relatively low. In the production of discrete components the required firing temperatures are from 1000°C to over 1200°C /11,14,24,25/. The lower temperature of the spinel synthesis in thick-film materials as compared to bulk ceramics is presumably due to the presence of the liquid glass phase which appears in thick-film resistors at temperatures around 700°C /26,27/.

The microstructure of the surface of the NTC 4993 thermistors fired at 850°C is shown in Fig. 9. The microstructure is glassy and porous with pore dimensions up to 10

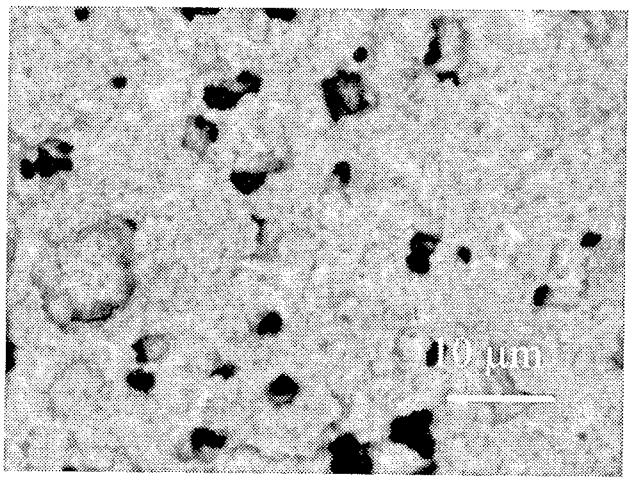

Fig. 9: The microstructure of the surface of the NTC 4993 thermistor, fired at 850°C

um. The lighter phase is a glass phase. Cross-sections of the NTC 4993 thermistors fired at 850°C on alumina and LTCC substrates are shown in Figs. 10.a and 10.b. respectively. In both cases the films are porous. The interaction layer on the interface between the NTC films and the substrates is observed for both substrates. The thin, light-coloured phase on the alumina side is lead-oxide rich and indicates the diffusion of PbO into the alumina ceramics. The darker interface within the LTCC substrate near the interface is rich in alumina which presumably diffused from the LTCC into the NTC film.

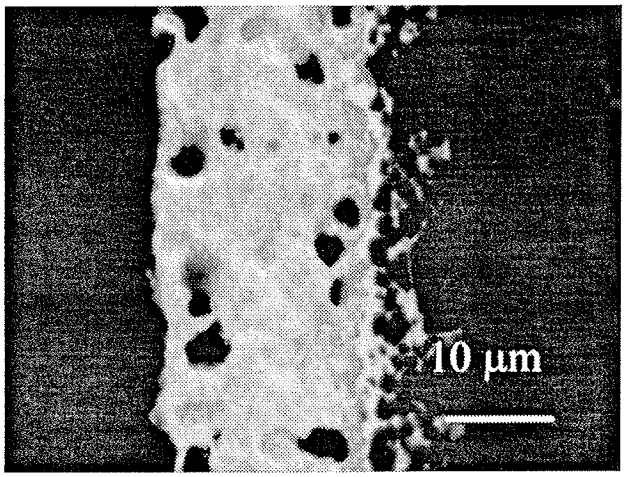

Fig. 10.a: Cross-section of the 4993 NTC thermistor, fired at 850°C on alumina. The alumina substrate is on the right

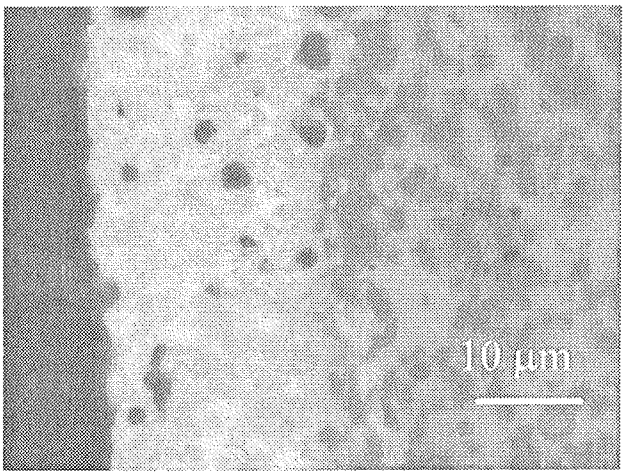

Fig. 10.b: Cross-section of the 4993 NTC thermistor, fired at 850°C on LTCC. The LTCC substrate is on the right

The overall analyses of the NTC layers (area 15x15 um^2) showed the presence of mainly Al, Si, Mn, Co, Ni, Cu, Ru and Pb. As mentioned in the Introduction, copper oxide and ruthenium oxide are added to lower the specific resistance of Mn-Co-Ni solid solutions. The results of the analysis are present in Table 3. The compositions are given for elements and for oxides in at. % and mol. %, respectively. The concentration of oxygen is calculated by difference and not measured directly. The elemental ratio between Mn-, Co- and Ni-oxides is roughly 5/2/1, which puts this composition in the region of solid solutions with the lowest specific resistances between 0.5 and 1 kohm.cm /13/. Note that a higher concentration of SiO_2 in the NTC films fired on LTCC substrates than the films on alumina substrates, indicates a significant diffusion of silica from the LTCC into the thick-film NTC thermistors during firing.

Table 3: The EDS analyses of the concentration of elements (in atomic %) and oxides (in mol. %) in the NTC 4993 thermistors fired at 850°C on the alumina and LTCC substrates

Element (at. %)	Al_2O_3 substrate	LTCC substrate	Oxide (mol. %)	Al_2O_3 substrate	LTCC substrate
Al	7	7	$AlO_{1.5}$	17	15
Si	5	9	SiO_2	12	19
K	<1	<1	$KO_{0.5}$	<2	<2
Ca	<1	<1	CaO	<2	<2
Mn	10	11	MnO_x	24	23
Co	4	4	CoO_x	10	9
Ni	2	2	NiO	5	4
Cu	6	6	CuO	14	13
Ru	2	2	RuO_2	5	4
Pb	4	4	PbO	10	9
O	57	55			

The electrical characteristics, i.e., sheet resistivities, cold (-25°C to 25°C) and hot (25°C to 125°C) TCRs, beta factors and noise indices of the NTC 4994 thermistors fired on alumina and LTCC substrates are shown in Table. 4. Note that the noise indices are expressed in "dB" and "uV/V". The noise indices are expressed in "dB" and "uV/V".

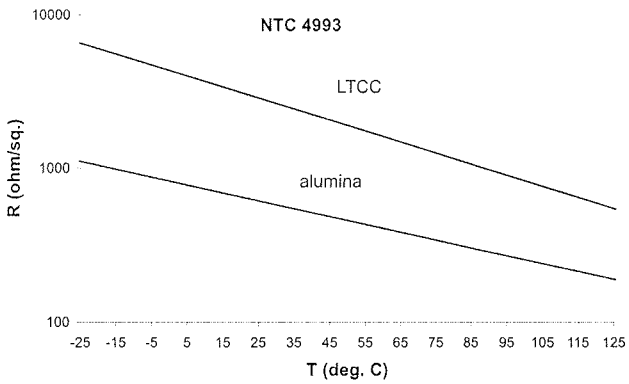

Fig. 11: Logarithm of sheet resistivities vs. temperature of NTC 4994 thermistors fired at 850°C on alumina or LTCC substrates.

Table 4: Sheet resistivities, cold (-25°C to 25°C) and hot (25°C to 125°C) TCRs, beta factors and noise indices of the 2041 resistors on alumina and on LTCC substrates.

Substrate	R sheet (ohm/sq.)	Cold TCR ($x10^{-6}$/K)	Hot TCR ($x10^{-6}$/K)	B (K)	Noise (dB)	Noise (uV/V)
Al_2O_3	550	-22700	-6510	1240	-12.2	0.25
LTCC	2250	-41500	-7550	1660	7.4	2.34

These two units are "connected" with a simple equation - see the comments relating to Table 2. The dependence of the relative sheet resistivities vs. temperature of the 2041 resistors fired at 850°C on alumina or LTCC substrates is shown in Fig. 11.

The sheet resistivities of the NTC 4993 thick-film thermistors (nominal sheet resistivity 1 kohm/sq,) are, at room temperature, around 500 ohm/sq. on alumina, while on the LTCC substrates they are four times higher. Similarly, the cold and hot TCRs and the beta factors of the thermistors fired on LTCC are higher than the values fired on alumina. These results could be attributed to the diffusion of the glassy phase, mainly SiO_2, from the LTCC substrates into the NTC films during firing. The additional glass presumably "breaks up" some of the conductive paths through the resistor film, thereby increasing the sheet resistivities as well as the noise indices. However, if the higher current noise of the NTC 4993 thermistors fired on LTCC substrates is acceptable the investigated thick-film NTC materials could be used on LTCC substrates.

Conclusions

Low-Temperature Co-fired Ceramic (LTCC) materials, which are sintered at the low temperatures typically used for thick-film processing, i.e. around 850°C, are convenient and widespread technique for MCM-C (Ceramic multi-chip modules). LTCC materials are based either on crystallizable glass or a mixture of glass and ceramics. As most of the thick-film resistors were developed for firing on alumina substrates their compatibility with (rather glassy) LTCC substrates needed to be evaluated. The "normal", i e., low TCR thick-film resistor 2041 (10 kohm/sq., Du Pont) and the 4993 NTC thermistor (1 kohm/sq., EMCA Remex) were fired on 96% alumina and co-fired on green Du Pont LTCC 951 tapes. The electrical and microstructural characteristics were compared.

The X-ray spectra of the 2041 resistors fired on alumina and LTCC substrates are nearly the same, which indicates the compatibility of the 2041 with LTCC. Also, the electrical characteristics of 2041 resistors fired on both substrates are similar indicating that the resistors are compatible with the LTCC material. The EDS analyses did not show any significant interaction between the 2041 resistors and the LTCC substrates.

For the NTC 4993 thermistors the XRD analysis showed that the spinel active phase is formed during the firing and is not included as a pre-reacted compound. There were no significant differences in the X-ray spectra between thermistor films fired on alumina or on LTCC substrates. The electrical characteristics, i.e., the sheet resistivities, beta factors and noise indices of the thermistors fired on LTCC substrates as compared to films fired on alumina significantly increased, indicating the interaction between the thermistor layers and the LTCC substrates. The changes in the electrical parameters were attributed to the diffusion of a silica-rich phase from the LTCC substrates into the thermistor films.

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REVIEW OF VARIOUS REALIZATIONS OF INTEGRATED MONOLITHIC TRANSFORMERS

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Key words: integrated transformer, coupling coefficient, planar structure, stacked structure.

Abstract: The integrated transformer is an essential component in many RF integrated circuits. Planar and stacked transformers on a silicon substrate are widely used in low-noise amplifiers, active mixers, voltage control oscillators, filters, etc. This paper gives an overview of different configurations of integrated transformers, their layouts and fundamental electrical characteristics. This review, also, compares the advantages and disadvantages of various integrated monolithic transformer realizations regarding the occupied area on chip, the coupling coefficient, the inductances values and the parasitic effects. Some possibility for improvement of transformer performances, such as using patterned ground shield or design structures with variable width of turns in the primary and secondary winding are proposed, too.

Pregled različnih izvedb integriranih monolitnih transformatorjev

Ključne besede: integrirani transformatorji, koeficient sklopitve, planarna struktura, nakopičena struktura

Izvleček: Integrirani transformator je bistven element v mnogih RF integriranih vezjih. Planarni in nakopičeni transformatorji na silicijevi rezini se uporabljajo pri izvedbi malošumnih ojačevalnikov, aktivnih mešalnih vezjih, napetostno krmiljenih oscilatorjih, filtrih in podobno. V prispevku podajamo pregled različnih možnih konfirguracij integriranih transformatorjev, njihov razpored na površini in osnovne električne značilnosti. Primerjamo tudi prednosti in slabosti različnih izvedb tovrstnih transformatorjev glede površine, ki je zasedajo na čipu, koeficienta sklopitve, vrednosti induktance in parazitnih efektov. Predlagamo tudi nekatere izboljšave transformatorskih lastnosti, z uporabo ozemljenega oklopa ali načrtovanjem strukture s spremenljivo širino linij v primarnem in sekundarnem navitju.

I. Introduction

Constant growth of wireless applications brought to an intensive need for mobile communications and mobile communication devices. According to some research data /1/, the annual worldwide sales of cellular phones have exceeded the figure of $2.5B and in Europe only the profit from equipment and service for mobile communications has overcome $30B. Due to growing need for wireless communication devices radio frequency and wireless market is continuing its development. As well known, there are three main generations of mobile systems, as shown in Fig. 1 /2, 3/.

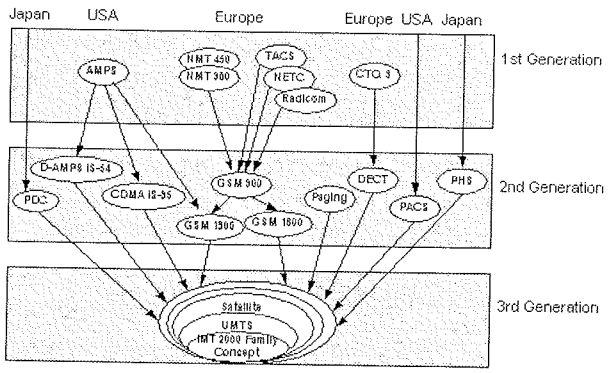
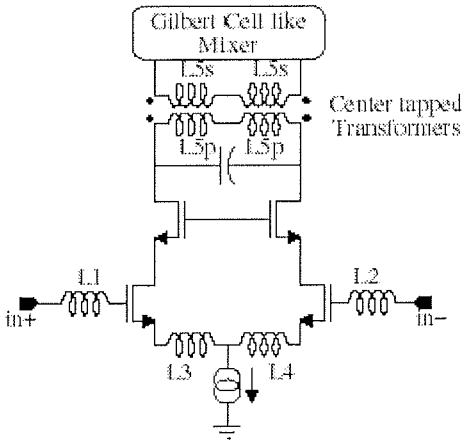


Fig. 1. Mobile communication generations /2/.

Nowadays, the second generation of mobile systems is widely established, using GSM (Global System for Mobile Communications) as a most successful digital wireless service. But different standards that are in use worldwide are quite inadequate for successful interconnecting. So, it was suggested that the third generation of mobile systems should give a worldwide high-performance standard UMTS. UMTS is to provide data rates up to 144Kbits/s, 384 Kbits/s and 2 Mbits/s in macrocellular, microcellular and indoor environments respectively. This would unlock services such as real-time video, mobile entertainment, etc /4/. But, there are many difficulties present that apply to implementation of this technology.

Mobile communication is mainly concentrated on long distance range applications. For short-range distance between the emitter and the receiver, such as in wireless LAN (WLAN), different standards have been introduced. In industry, for WLAN are used standards sanctioned by WECA (the Wireless Ethernet Compatibility Alliance) based on standard created by the 802.11 committee of the IEEE. According to this standard spectrum around 2.4GHz (for Wi-Fi or IEEE802.11a) and 5GHz (for HiperLAN or IEEE802.11a) are used with transmission speeds of 11Mbps. Another standard for short-range communications (10-100m) is Bluetooth. It uses 2.4GHz ISM band and has transmission speed of 780kbs/s. These standards intend to take primate in mobile communications for low band applications.

Silicon based RF (radio frequency) integrated circuits are becoming more and more competitive in wide band frequency range. An essential component of these IC (integrated circuits) is integrated (or on-chip) transformer. They are widely used in mobile communications, microwave integrated circuits, low noise amplifiers (LNA) /5, 6/, active mixers /7, 8/, baluns (give balanced output for unbalanced input) /9, 10/. They are required in impedance matching, signal coupling, and phase splitting applications. Transformers are proved effective for miniaturized sensors, actuators, filters and power converters that should be integrated on chip modules and installed in various electronic systems /11-17/. In Fig. 2 are shown some of the most common applications of the monolithic transformer in LNA and active mixer /8/.



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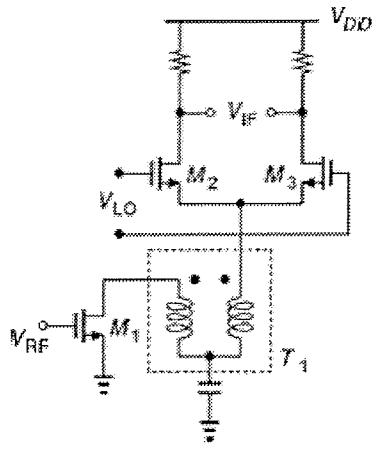


b)

Fig. 2. Integrated transformer in a) LNA application b) active mixer.

In LNA circuit transformer provides an inductive feedback path aiming to improve the linearity and the stability of the circuit. Fig. 2b shows a useful example, where transformer having current gain is placed in the current path of an active mixer.

Although significant efforts have been made in order to improve the characteristics of on-chip transformers, it is still a great problem to bring in piece the opposite demands for low cost, low supply voltage, low power dissipation and low distortion, but high frequency of operation in RF implementation of these transformers /15/. Commonly used transformers are fabricated on lossy silicon substrate hence they are from the start limited to a lower quality factor, coupling coefficient and high parasitic effects between the component and the substrate. However, low cost of Si IC fabrication over GaAs or quartz IC fabrication still dictates the usage of silicon substrates.

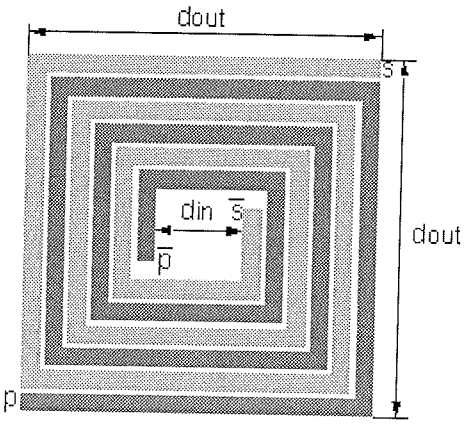
Arbitrary transformer layouts also impact the transformer characteristics. These layouts include parallel windings, interleaved windings, overlay windings and concentric spiral windings and they result in planar or stacked configurations. Planar transformers generally have lower self-inductance, parasitic capacitances and coupling factor, but higher resonant frequency compare to stacked which engage less chip area and has higher inductance values and lower quality factor. Width of the windings, spacing between coils and material used for their fabrication also has influence on overlay characteristics of the transformer.

In order to give the general insight in transformer configurations various constructions will be presented in this paper. We will closely clarify the influence of substrate conductivity, mutual coupling, symmetry and process parameters on transformer behaviour. We also propose some techniques for improvement of integrated transformer performances.

II. Fundamental Characteristics of Integrated Transformers

As well known, monolithic transformer is one of the indispensable elements of many RF ICs. Fig. 3 represents a typical configuration of monolithic planar transformer, its electrical equivalent symbol and layout in the chip /12/.

Transformer is characterized by the inductance (*Lp*, *Ls*) and the voltage (*Vp*, *Vs*) of the primary and the secondary winding and its operation is based upon the mutual inductance of the windings. According to the *Lenz* law variations of the magnetic flux produced by the current flow in the primary winding i_p induce a current i_s in the secondary winding that flows out the terminal $\bar{S}$. They also provide a positive voltage V_s between the secondary terminals. It is important to emphasize that DC signals are blocked by the transformer therefore linking windings at different voltages is possible. There are two ways of connecting the primary and the secondary terminals - in non-inverting or inverting manner. The phase of V_s depends on the choice of the reference terminal. In non-inverting connection an AC signal source and the ground are on primary terminals P and $\bar{P}$, giving a minimal phase shift of the signal at the S output while $\bar{S}$ is grounded. An inverting connection differs in as much that terminal S is now grounded and at the $\bar{S}$ output



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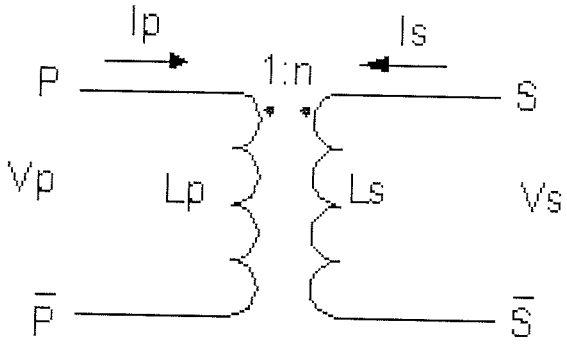

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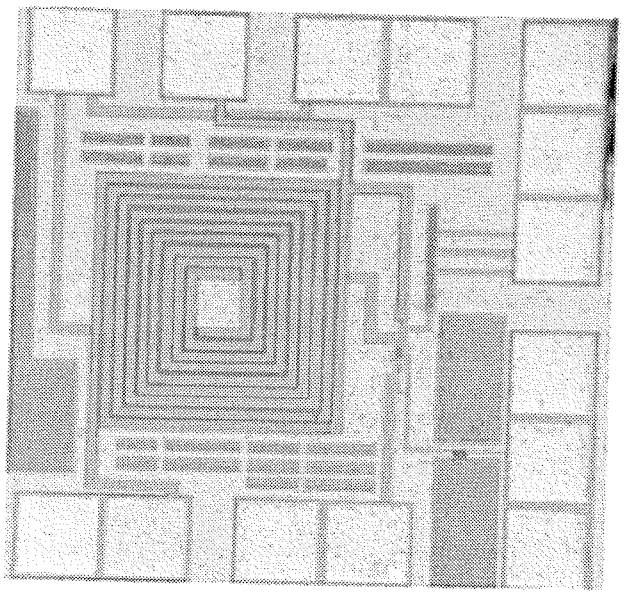

c)

Fig. 3. Monolithic planar transformer a) physical layout b) schematic symbol c) the view on the chip.

produced signal is in antiphase to the signal applied to the primary. Phase shifting is just one of the by-products that take place when using this two constructions /18, 19/.

Due to its common use, it is crucial that insertion losses of the transformer are brought to a minimum. These losses are invoked with finite metal resistance, finite inductances of coils, substrate dissipation and magnetic coupling factor. The metal ohmic losses can be reduced by using high conductive materials for windings or by increasing its thickness. Substrate losses are minimized by utilizing substrate materials with high resistivity or placing isolation layers (made usually by silicon-dioxide) between the substrate and the transformer coils.

There are three main electrical parameters that describe every monolithic transformer - the transformer turns ratio *n*, *k*-factor and *Q*-factor. The transformer turns ratio is related with the current and voltage transformation between the windings as shown (in accordance with symbol 1 : n in Fig. 3b)

$$n = \frac{V_s}{V_p} = \frac{i_p}{i_s} = \sqrt{\frac{L_s}{L_p}}. \qquad (1)$$

Lp and *Ls* represent the inductance of primary and secondary winding of the transformer. Generally, value of the ratio *n* is around 1 for symmetrical structures, but in the case of step-up or step-down transformer topology it can be greater or less than 1, respectively.

The strength of the magnetic coupling between the primary and the secondary is represented by the *k*-factor, which is closely related with the mutual inductance as well as with the self-inductance of the windings

$$k = \frac{M}{\sqrt{Lp \cdot Ls}}. \qquad (2)$$

In the expression (2) *M* stands for mutual inductance of the primary and the secondary coil. The value of *k*-factor primarily depends upon the width and spacing of the metal traces and the substrate thickness. By increasing the number of turns in transformer and decreasing the space between the windings higher values for *k*-factor can be achieved. For the ideal transformer *k*-factor is 1, but for the most fabricated constructions *k* is in range 0.75 to 0.9 /18/.

Quality factor, *Q*-factor, is more technology than geometry dependent factor and it can be calculated by the following equation

$$Q = -\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})}. \qquad (3)$$

Y_{11} represents input admittance of the transformer. *Q*-factor is dimensionless and it is proportional to the ratio of the resultant magnetic energy stored in the transformer to the energy dissipated per unit time cycle /20/. Reaching high values for *Q*-factor represents a problem. Great efforts have been made in order to improve this parameter, but the results are not still satisfying.

III. Various Realizations of Integrated Transformers

Prior to integrated transformers on-chip inductors on silicon substrate have been fully analyzed. Many researches have been performed in order to explain, define and illustrate design, modeling and optimization of integrated inductors. But in spite of the many similarities between inductors and transformers significant difference caused by magnetically induced losses are present between their equivalent models. Therefore, only some of the experiences that are used for improvement of inductors can be implemented for transformers, so there are still many unknown rules that are present in the field of monolithic transformer theory.

As inductors, on-chip transformers are usually fabricated by deposition of conductive metal layers on silicon substrate. These metal coils are mainly square and can be placed in planar or stacked configuration. The planar configuration engages larger area on chip in order to achieve higher inductances and *Q*-factor and to minimize the substrate losses. On the other hand, vertically stacked constructions require less chip area for same values of inductance and have high mutual inductance, but a lower *Q*-factor. Which of these layout structures are to use is strongly dependent on the application in which transformer is needed.

A. Tapped (nested) Transformer

Tapped transformer is illustrated in Fig. 4. This is planar transformer and its secondary winding is placed around the primary. Thus, the common periphery between two windings is limited to just a single turn. Due to such configuration, mutual coupling between adjacent conductors mainly contributes to the self-inductance of each winding and not to mutual inductance between the windings. This implies a lower *k*-factor (not higher than 0.6). Both windings can be implemented on the top metal layer and therefore the parasitic capacitance between substrate and windings is minimized. Another disadvantage of this layout is non-symmetrical structure. Tapped transformer can be useful in high-performance broadband amplifiers and other three terminal applications.

B. BifilarTransformer

Bifilar transformer is illustrated in Fig. 5. This is also planar transformer and it is constructed from two parallel conductors that are interleaved. Therefore, mutual coupling between windings have higher influence on mutual inductance. As a result *k*-factor has higher values than in tapped configuration. Self-inductance values of the primary and secondary windings are not equal, because of the non-equal length of the metal. In this structure windings are also placed on the top metal layer. This implies an asymmetrical structure, which can be corrected in the manner shown in the interleaved structure.

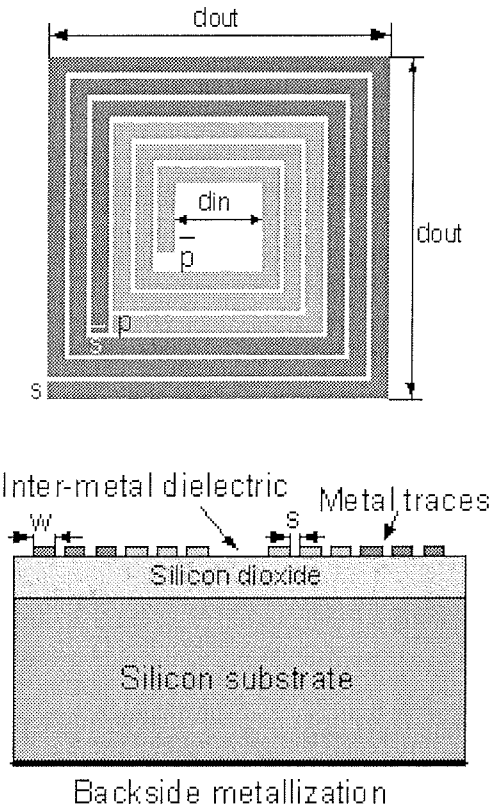

Fig. 4. Tapped transformer.

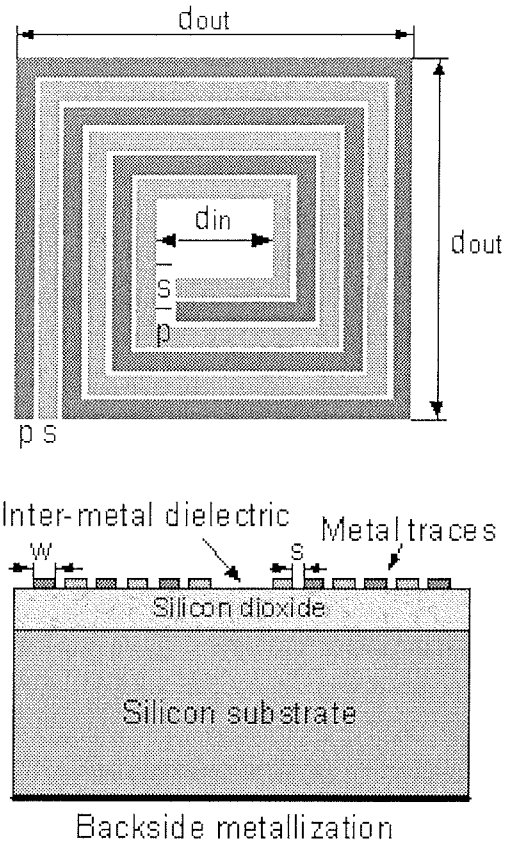

Fig. 5. Bifilar transformer.

C. Interleaved Transformer

This is the most commonly used layout and with it full symmetry of the transformer is achieved. As shown in the Fig. 6 primary and secondary winding are identical and therefore they have almost identical self-inductance value. This configuration gives *k*-factor approximately around 0.7 /21/. Again, placing the primary and the secondary winding on the top layer can minimize the parasitic capacitance between windings and the substrate. Another advantage of this design is that the transformer terminals are an opposite sides of the physical layout, which facilitates connections to other circuitry. It is frequently used in four terminal applications.

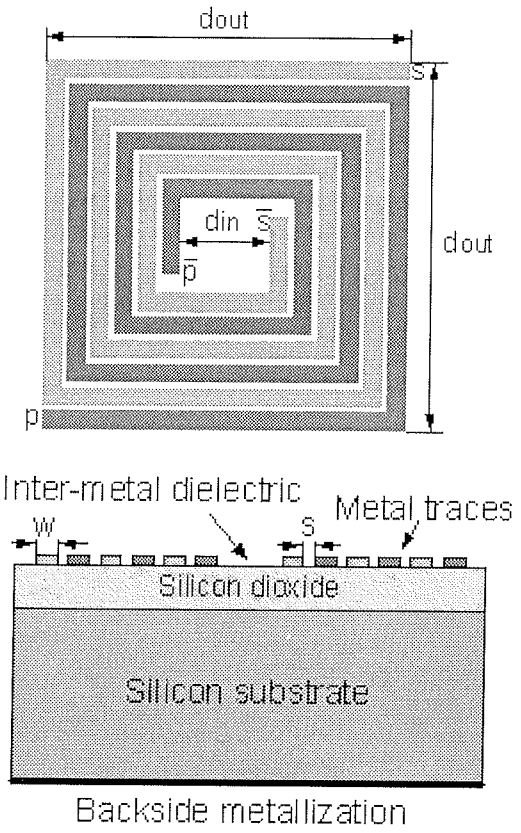

Fig. 6. Interleaved transformer.

To gain higher step-up ratio, transformer shown in Fig. 7 is commonly used. As depicted 1:5 turns ratio is designed with one secondary winding and five individual turns for the primary (connected in parallel). This configuration leads to drastic failure of the primary inductance value and slightly decreases the *k*-factor by increasing step-up ratio /18/. Therefore, the input impedance must be low in order to efficiently couple a signal into the primary of the transformer. The step-up transformer is an ideal feedback element for RF amplifiers.

D. Stacked Transformer

Stacked transformer, or vertical-coupling structure /22/, represents a multiple conductor layer structure, as shown in Fig. 8a and Fig. 8b. This configuration has the advan-

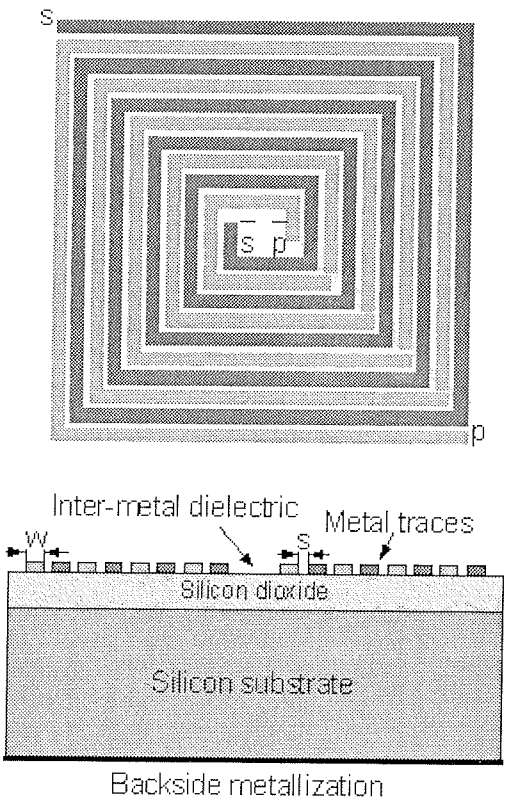

Fig. 7. The step up, 1:5 interleaved transformer.

tage of area efficiency and higher mutual coupling between the windings due to placing the primary coil on top of the secondary. Typical thickness of the dielectric between the layers is 1μm. Stacked transformers mainly have high *k*-factor, up to 0.9, and high mutual inductance, but low self-resonance frequency and therefore relatively small bandwidth /23/. For its fabrication three metal layers are needed, compared to tapped, bifilar and interleaved structure, which require two metal levels. This is not a symmetrical structure. The primary and the secondary winding are placed in adjacent metal layers causing different distances from the substrate. Also, their thickness often differ implying asymmetry in the electrical response of the transformer and unequal resistance of the windings. The lower winding shields the upper one from the influence of the conductive substrate causing difference in the parasitic capacitance to the substrate. In order to improve its characteristics the windings are placed in slightly offset position (horizontally or diagonally shifted), resulting in higher *Q*-factor and resonant frequency, Fig. 8c.

Also, better characteristics of this transformer can be gained by placing the primary winding on lower metal layer. In this manner the substrate losses are slightly increased, but the parasitic capacitance between the windings becomes significantly decreased, thus the self-resonant frequency increases /8/. Non-symmetrical configuration of the stacked transformer can be a limiting factor of its usefulness, but current trends in silicon technology are focused on improving its characteristics and performances.

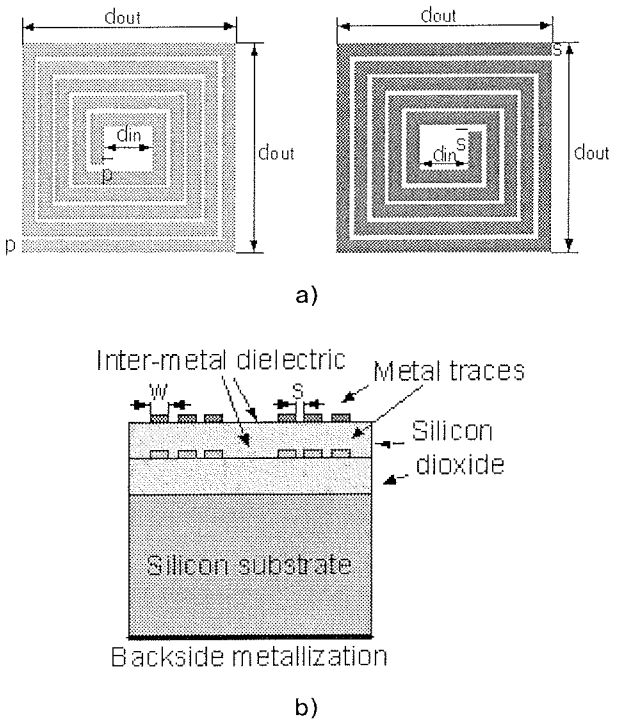

Fig. 8. Stacked transformer a) layout
b) non-offset position
c) offset position of the windings.

Another structure of the stacked transformer can also be used. Fig. 9 /8/ depicts transformer with 1-to-2 step-up ratio. This configuration uses three different metal layers for placing the windings. As shown in Fig. 9 secondary windings are interconnected by via and slightly offset compared to the primary winding placed in between. The number of spirals used for each winding impacts the voltage (or current) gain at a desired frequency. The concept of stacked transformer can be applied, also, to more metal layers to achieve higher voltage gain.

E. Stacked Interleaved Transformer

Fig. 10 represents another realization of monolithic transformer /24, 25/. This is a symmetrical structure and it occupies small area on chip. It consists of two interleaved transformers that are stacked on top of one another. In this structure both the primary and the secondary winding are

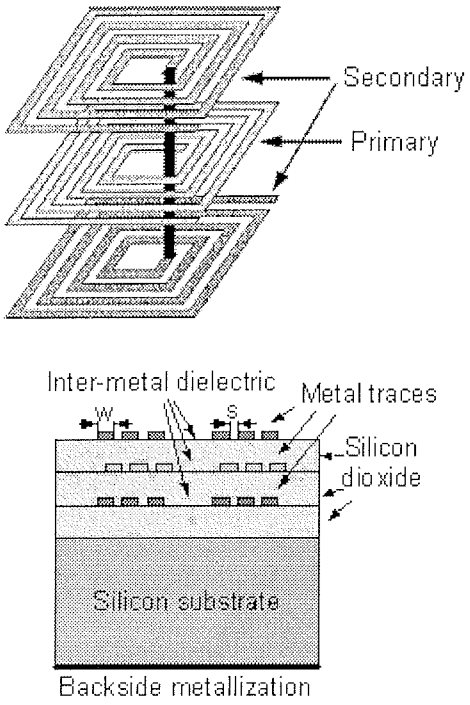

Fig. 9.1: 2 stacked transformer structure.

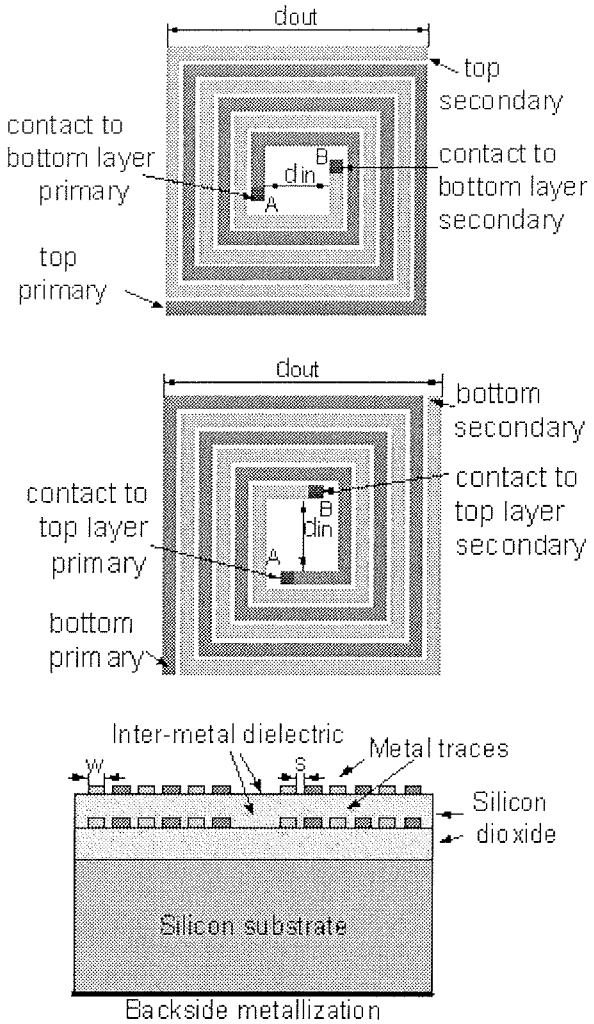

Fig. 10. Stacked interleaved transformer.

present in both metal layers achieving in this manner a full symmetry of the layout. This also implicates reduction of the parasitic capacitance between primary and secondary windings. Matching ends of windings in top and bottom layer are interconnected by vias (A and B in Fig. 10). Stacked interleaved transformer has higher value of the self-inductance of the windings, but lower mutual inductance than the stacked configuration. However, the values of total inductance for these two configurations are approximately the same. This transformer is used in narrowband applications that require symmetry.

F. Central-taped Transformer

Transformer shown in Fig. 11 represents also a mixture of interleaved (Fig. 6) and stacked (Fig. 8) configuration. Depicted transformer has a square structure, consisting of two groups of interleaved coils that are divided along a horizontal symmetry line, forming turns ratio of 4:5. One of the advantages of such construction is alleviation in connecting transformer to other circuitry, due to placing both terminals to the outside edge of the transformer. This construction shows good mutual couplings, which is favored by interwounding of the inductors. Center-taped transformer is utilized in power dividers/combiners and baluns.

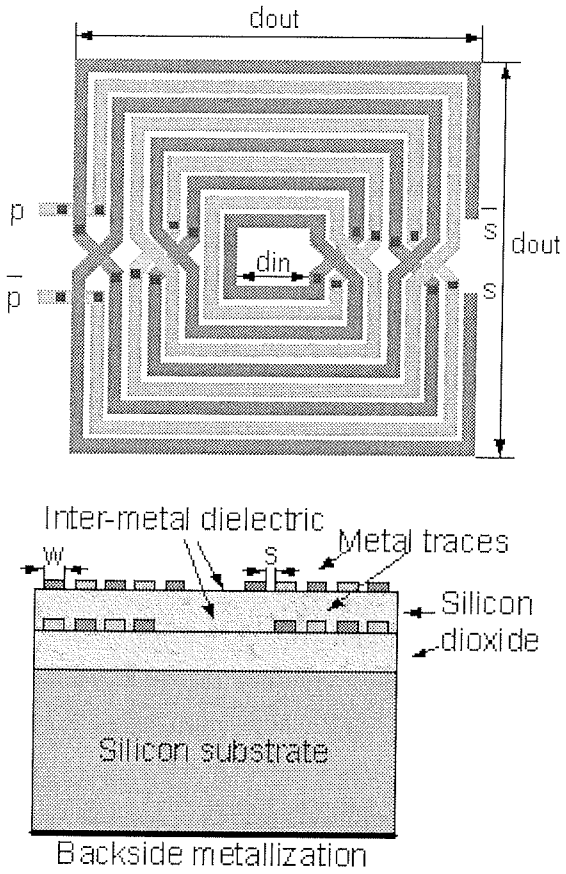

Fig. 11. Central-taped transformer.

Similar transformer configuration is depicted in Fig. 12 /26/. The primary and the secondary winding are laid on the same upper metal layer. Windings don't form whole square segments, yet their parts are connected by vias through one of the lower metal layers at points on vertical symmetry axis. In this configuration, as in center-tapped, primary and the secondary terminals are on opposite outside edges of the transformer and as result connection of the transformer to other electrical components is easy.

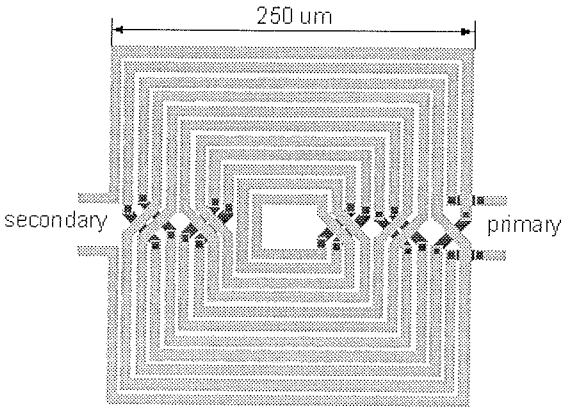

Fig. 12. Integrated transformer with L_p=5.5nH, L_s=7nH, k=0.83 and Q_p= Q_s =10 at 1.7GHz /26/.

The primary and the secondary winding can have other shapes not only square, like octagonal or circular. A special planar winding scheme for circular monolithic transformers which results in a very high coupling coeficient *k* is depicted in Fig. 13 /27, 28/. For realization other values than 1:1 of the turn ratio, different numbers of primary and secondary turns must be used. This implements that some adjacent conductors belong to the same winding which results in a lower *k*-factor. A solution for this problem is to use an interlaced winding-scheme /28/. The monolithic transformer shown in Fig. 13 consists of six primary turns P1-P6 and two secondary turns. The center taps PCT and SCT are available. Fig. 13 shows a three-dimensional top view of the transformer. The outer diameter is about 200 μm and the inner diameter is about 50 μm.

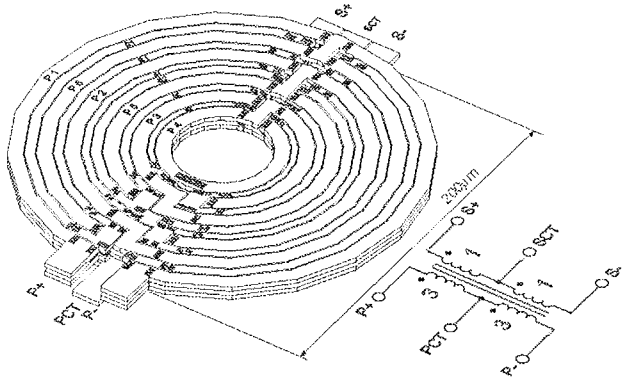

Fig. 13. 3-D-view of the planar high coupling performance transformer /28/.

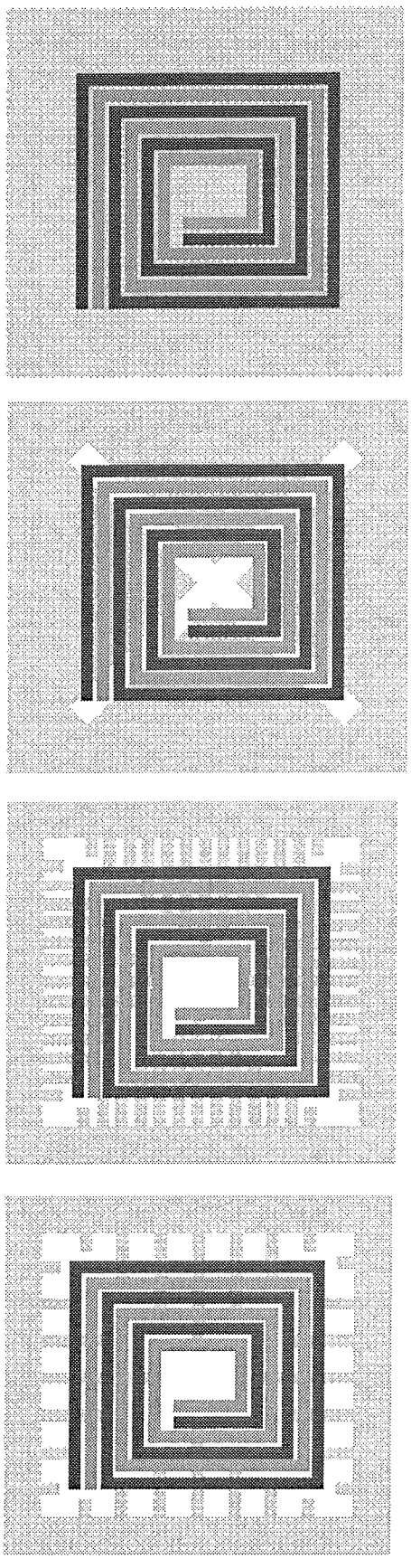

Fig. 14. The various patterned ground shields constructions a) solid ground b) coarse ground c) patterned ground d) bar ground /29/.

IV. Some Techniques for Improvement of Transformer Characteristics

One of additional techniques for improvement of transformer characteristics is implementing patterned ground shields - PGS /29/. PGS is placed between the silicon substrate and the transformer windings, onto the silicon or slightly above it. It is commonly made of aluminum or polysilicon. The main reason for introducing PGS is to limit flow of magnetically induced eddy currents in the silicon substrate. Some designs of PGS are depicted in Fig. 14.

Solid PGS (Fig. 14a) gives good results in preventing losses invoked by the electrical field. But losses caused by the magnetic field and induced eddy currents in PGS are substantial. Therefore the shield must be patterned. In Fig. 14c, 14d are depicted two ways of patterning the shield. In Fig. 14c PGS has metal strips with a 40μm width and 10μm spacing, while in Fig. 14d width of the strips is the same but the spacing between them is 60μm. As shown in /29/ transformer using PGS with larger spacing has lower values of inductance and *Q*-factor, but has higher resonant frequency and larger bandwidth than the other configuration. Introduction of these PGS leads to lower values of inductance and *Q*-factor and voltage gain on lower frequencies, but give better *k*- and *Q*-factor on frequencies higher than 4GHz compared to transformers without PGS. On frequencies higher than 14GHz shields lose their purpose leaving the transformer with the same characteristics as without PGS.

In order to decrease substrate losses it is advisable to use surrounding metal tracks for ground pads in the vicinity of on-chip components, Fig. 15. This ground ring enables dissipation of the magnetic flux in the conductive silicon substrate. According to the previous experience with inductors position of the ground ring implicates variations of the self-resonance frequency of the transformer and usage of substrate area is increased. As the ground pads are moved farther from the transformer resonance frequency increases, till it doesn't reach a saturation value.

Bulk and surface micromachining are techniques compatible with standard IC industry of inductors and transformers. By means of these techniques, electrical coupling losses can be reduced. They employ substrate removal underneath planar components (inductor, transformer...). In this way substrate losses and electrical coupling are eliminated from the component, resulting in substantial increase of self-resonant frequency and quality factor /30/-/33/. However, when the silicon substrate is removed, magnetically induced losses (eddy currents) become much more relevant. They are directly dependent on the time varying magnetic flux through the coils. They represent frequency dependant losses and they increase while the coil width increases, so they must be taken into account /31/.

The recently new solutions have been developed based on layout optimization and finding the optimum value between the magnetically induced and ohmic losses in metal

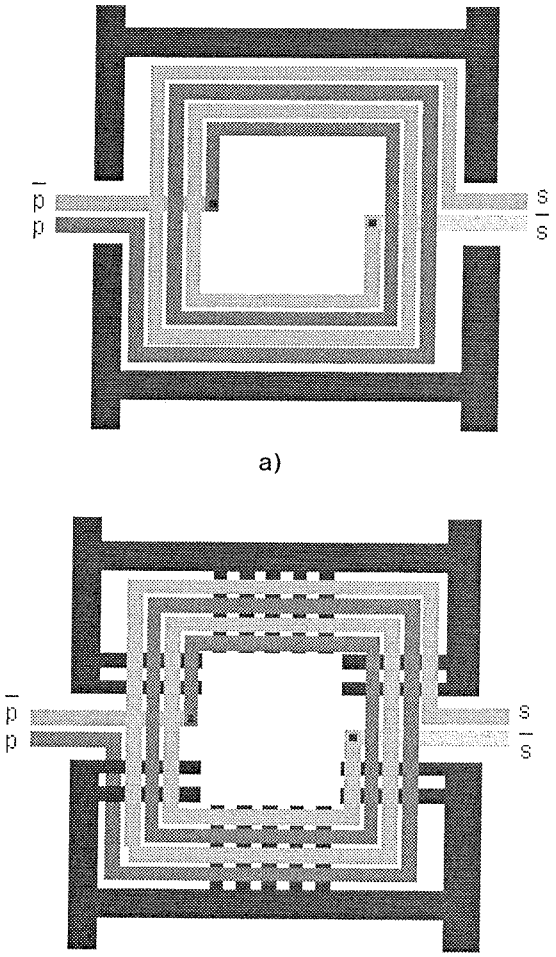

Fig. 15. Interleaved transformer with
a) the ground ring, and
b) the ground ring and the PGS.

coils. The first step of this optimization is analyzing the series resistance of the transformer's coils. It is widely known that ohmic losses of this resistance decrease while the

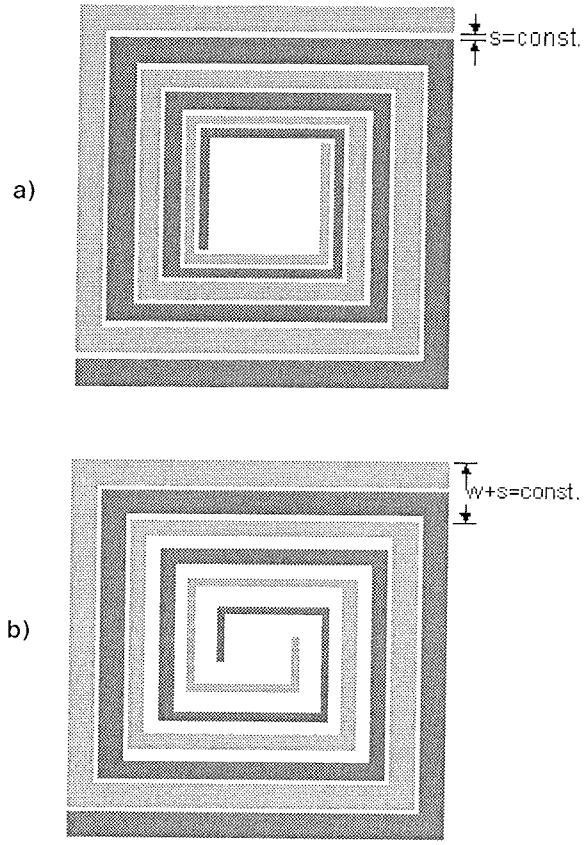

Fig. 16. Planar transformer with variable width of conductor segments.

width of the metal strips increases, but the magnetically induced losses enhance. So, there must be an optimum strip width, which minimize series resistance and maximize *Q*-factor. Layout optimization techniques can be used not to find the optimum width of the coil, but to embrace the width and/or the pitch (the thickness) of every turn as the variable part of the design. For inner turns narrow strips are used to optimize magnetic field losses, which are at the highest value in the center of the primary or secondary

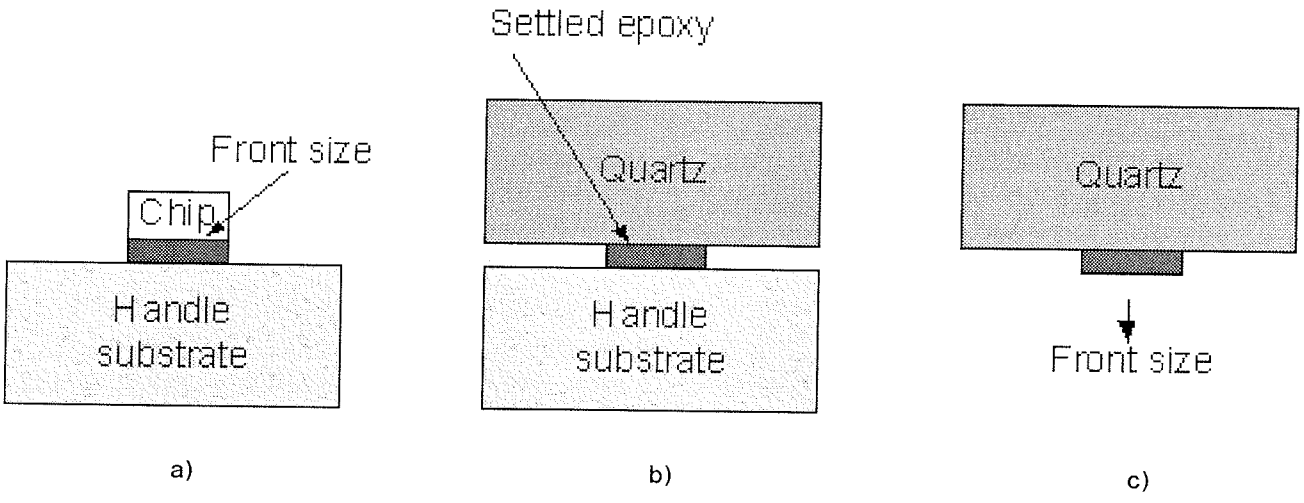

Fig. 17. Substrate transfer technique /29/.

coil of integrated transformers. The wide strips optimize the outer turns, where ohmic losses are predominant. In this manner much better results can be obtained (higher *Q*-factor and resonant frequency) /30/.

Planar transformers with variable conductor width of the primary and the secondary winding can be realized in two configurations as it can be seen from Fig. 16. The form shown in Fig. 16a is more used, where the spacing between adjacent turns is constant (*s*=const.). The configuration depicted in Fig. 16b has property that the total distance between neighboring segments is constant (*w*+*s*=const.)

Another advanced technique can be used to improve characteristics of the monolithic transformer at high frequencies /29/. By employing a substrate transfer technique lossy silicon substrate is replaced with lossless quartz substrate. First step in this process is to mount the transformer die onto a peace of insulating quartz by dissolvable epoxy glue (Fig. 17a). Then silicon substrate is removed by mechanical polishing with diamond sand paper until 30μm of silicon is left. This remain of silicon is removed by reactive plasma etching at room temperature. Following step is to use epoxy to attach another piece of quartz onto the etched surface of the die (Fig. 17b). By dissolving the epoxy glue in acetone substrate transfer technique is finished (Fig. 17c). Transformer on the quartz substrate has improved *Q*-factor and voltage gain at higher resonant frequency. However, the influence of the substrate on the *k*-factor and inductance is negligible. The usage of this technique is not yet so popular due to more complicated fabrication.

V. Conclusion

Integrated monolithic transformer performances greatly depend on geometrical and process parameters. Opposite demands are often expected and therefore a good balance should be found among self-inductance value, mutual coupling, parasitic capacitances, resonant frequency and naturally the cost of fabricated component. In this paper we have presented various transformer configurations and gave their fundamental characteristics. As we have said, planar structures occupy plenty space on chip, but they have high resonant frequency and therefore can be used in band-wide applications. Tapped transformer has also a low *k*-factor and fairly low self-inductance. Interleaved and bifilar configurations have pretty high values for coupling coefficient, but low self-inductance. On the other hand, stacked structures engage less chip area and are used in narrow-band circuits as a terminal device due to their low self-resonant frequency. Hence, this work compares the advantages and disadvantages of various monolithic integrated transformer realizations and, also, gives some possibility for improvement of integrated transformer performances.

Acknowledgement

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ARITMETIČNA-LOGIČNA ENOTA Z ZAPOREDNO LOGIKO ZA IZRAČUN UTEŽNE VSOTE S PROGRAMIRNIMI VEZJI

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Kjučne besede: digitalna obdelava signalov, nerekurzivna digitalna sita, aritmetično-logična enota, koncentrirana aritmetika, zaporedna aritmetika, implementacija, programirna vezja

Izvleček: V članku je opisana izvedba aritmetično-logične enote z zaporedno logiko za sprotno določitev utežne vsote implementirane v programirna vezja (FPGA). Aritmetično logično enoto lahko uporabimo pri načrtovanju in izvedbi digitalnih FIR sit. Celotna struktura sita ima modularno zasnovo, ki podpira enostavno razširitev digitalnega FIR sita glede na poljubno število koeficientov. Zgradba modulov temelji na uporabi zaporedne logike za izvajanje aritmetičnih operacij. Pri načrtovanju smo se omejili na 16-bitni zapis vhodno-izhodnega signala digitalnega FIR sita. Načrtovanje digitalnega FIR sita z opisano aritmetično logično enoto za izračun utežne vsote koeficientov zagotavlja majhno aparaturno kompleksnost in linearno naraščanje aparaturne kompleksnosti sita glede na število koeficientov. FIR sito je zasnovano tako, da se lahko uporabi kot samostojno vezje. Opisana aritmetično logična enota v sistemu digitalnega FIR sita omogoča sproten vnos koeficientov v času med dvema vzorcema vhodnega signala, zato jo lahko uporabimo tudi kot FIR enoto v sistemu adaptivnega sita. Za načrtovanje aritmetično-logične enote in njene uporabe pri izvedbi digitalnih FIR sit smo uporabili programski paket Xilinx ISE 6.1 WebPack, ki podpira vnos, sintezo vezja in implementacijo v programirna vezja. Izbrali smo programirno vezje XC3S-400, družine Spartan, firme Xilinx. Vanj smo implementirali digitalna FIR sita z 8, 16, 32 in 64 koeficienti. Simulacijo digitalnega FIR sita smo opravili s programskim paketom ModelSim. Pri tem smo na osnovi rezultatov simulacije ugotovili, da lahko pri 16-bitnem zapisu vhodnega signala, dosežemo frekvenco vzorčenja 4.4MHz.

Arithmetic Logic Unit for Weighted Sum Calculation with Programmable Logic Cell Array

Key words: digital signal processing, FIR filter, arithmetic logic unit, concentrated arithmetic, serial arithmetic, VHDL, implementation, FPGA.

Abstract: In this article the design of the arithmetic logic unit with serial arithmetic procedure for weighted sum calculation and programmable logic cell array implementation is presented. This arithmetic logic unit is especially intended for adaptive FIR digital filter realization because all the coefficients of the digital filter can be changed simultaneously between two input samples. FIR digital filter with proposed arithmetic logic unit with serial arithmetic is shown in Fig. 3. It can be designed in the modular structure (Fig. 5) that allows the whole system to be expanded to any number of coefficients with minimal effort. The previous realizations of digital filters in programmable circuits were focused on reduction of the complexity of the hardware realization /5/. The idea that stands behind the serial arithmetic structure is the reduction of hardware implementation complexity. It is shown that the hardware complexity increases linearly with the number of coefficients used (Table 1 and Fig. 8).

The FIR digital filter in the modular structure consists of *N* cells. One cell of the modular structure is elementary arithmetic block (Fig. 4) and consists of serial multiplier (Fig. 6), serial adder (Fig. 7) and FIFO register.

The filter has been designed in the Xilinx ISE 6.1 environment. The basic units, serial multiplier, serial adder and FIFO register of digital filter structure is designed with VHDL. The Xilinx schematic editor was used for connections between basic units. The test application is made with FIR digital filter of 16 coefficients and a 16-bit quantization of input and output signal. The Xilinx FPGA circuit XC3S-400 is used for implementation of FIR digital filter structures with 8, 16, 32 and 64 taps. The 64 taps FIR digital filter occupy only 72 % of input output blocks (IOB) and 78 % of slices of the whole XC3S-400 circuit used for this application. At 71 MHz clock frequency a sample frequency of input-output signal of 4.4 MHz has been obtained. The processing of one output signal sample needs 16 clock pulses.

1. Uvod

Programirna vezja so zanimiva za implementacijo digitalnih FIR sit, kjer izračun izhodnega otipka poteka brez. uporabe zunanjega pomnilnika, za zapis delnih vsot koeficientov /1/. Struktura digitalnega FIR sita, ki uporablja aritmetično-logično enoto z zaporedno logiko za izračun utežne vsote, omogoča vpis vektorja koeficientov v času med dvema otipkoma vhodnega signala. FIR sita s takšno aritmetično-logično enoto so zanimiva v sistemih adaptivnih digitalnih FIR sit, kjer se koeficienti dinamično spreminjajo. Pri načrtovanju struktur digitalnih FIR sit, ki omogočajo vnos koeficientov v času med dvema otipkoma, ločimo strukture s porazdeljeno aritmetiko /1, 2/ in strukture s koncentrirano aritmetiko /3/. Obe strukturi je možno implementirati v eno programirno vezje, če uporabimo načrtovalske postopke, ki zmanjšajo aparaturno kompleksnost izvedbe. Aparaturna kompleksnost je odvisna od načina implementacije diskretnega sistema. Pri povsem strojni implementaciji je aparaturna kompleksnost diskretnega sistema v glavnem odvisna od števila množilnikov za izračun izhodnega signala /4/. Zaradi tega je uporabljeno število množilnikov za implementacijo nekega sistema najpomembnejši parameter aparaturne kompleksnosti. Drugi kriterij

pri implementaciji diskretnih sistemov je zahteva po pomnilniku. Velikost potrebnega pomnilnika je odvisna od potrebnega števila lokacij za shranjevanje notranjih spremenljivk diskretnega sistema. Kot tretji kriterij računske kompleksnosti omenimo zbiranje in razmeščanje podatkov znotraj strukture. Zadnji, četrti kriterij pa je vpliv končne dolžine besede na čas izračuna izhodne vrednosti. Vse štiri opisane kriterije smo upoštevali pri izbiri strukture digitalnega FIR sita in pri njegovi implementacijo v programirno vezje.

Pokazali bomo, da je možno z upoštevanjem vseh naštetih kriterijev v eno programirno vezje družine Spartan-3 ob uporabi 16-bitne aritmetike in 16-bitne kvantizacije vhodnih signalov, implementirati digitalno FIR sito s 100 koeficienti. Osnovno strukturo nerekurzivnega digitalnega FIR sita opišemo s konvolucijsko enačbo, ki jo opišemo tudi kot utežno vsoto,

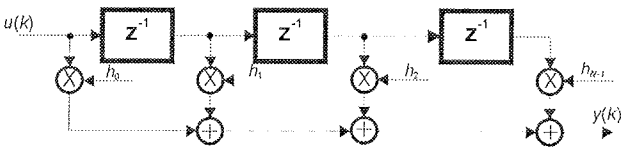
$$y = \mathbf{h}\mathbf{u}^T = \sum_{n=0}^{N-1} h_n u_n. \qquad (1)$$

V konvolucijski enačbi je vektor koeficientov **h** digitalnega FIR sita določen s komponentami, $\mathbf{h}=[h_0, h_1,...h_{N-1}]$, in vektor koeficientov vhoda s komponentami, $\mathbf{u}=[u_0, u_1,...u_{N-1}]$. Izvedbe digitalnih FIR sit so bile vedno povezane z iskanjem postopkov za zmanjšanje kompleksnosti algoritma, saj pomeni direktna izvedba enačbe (1) *N* množenj in *N* seštevanj za izračun otipkov izhodnega signal. Očitno je, da kompleksnost izračuna izhodnega otipka narašča z uporabljeno kvantizacijo vektorja koeficientov digitalnega FIR sita **h** in vektorja koeficientov vhoda **u**. Aparaturna kompleksnost digitalnega FIR sita narašča z večanjem števila koeficientov. Za implementacijo enačbe (1), bi bilo ugodno poiskati takšno strukturo digitalnega FIR sita, kjer bo aparaturna kompleksnost s kvantizacijo vhodno-izhodne besede in s številom koeficientov čim počasneje naraščala..

Znani pristop zmanjšanja potrebnih aritmetičnih operacij je uporaba aritmetično-logične enote na osnovi porazdeljene aritmetike, kjer se delne vsote koeficientov izračunajo vnaprej in se zapišejo v posebni pomnilnik /5/. Tako se potrebne operacije za izračun izhodnega signala *y(k)* omejijo na seštevanje in deljenje z dve. Žal pa takšne strukture ni možno uporabiti v sistemih adaptivnih digitalnih FIR sit, saj se v teh sistemih koeficienti dinamično spreminjajo. Rešitev je uporaba enote za sproten izračun koeficientov, ki je aparaturno najkompleksnejši del pri izvedbi digitalnega FIR sita v strukturi porazdeljene aritmetike /8/.

Klasični način implementacije aritmetične-logične enote za izračun utežne vsote temelji na strukturi koncentrirane aritmetike. V strukturi koncentrirane aritmetike ločimo dve obliki nerekurzivnih digitalnih sit. Prva je struktura s porazdeljenimi seštevalniki, ki jo prikazuje slika 1.

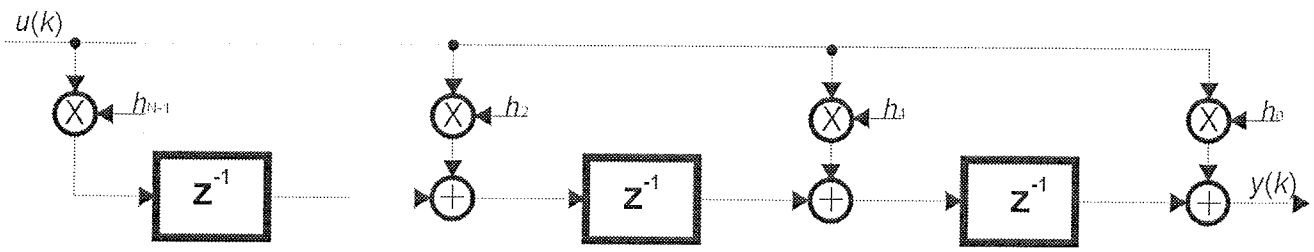
Druga struktura digitalnega FIR sita je izvedba z enim globalnim seštevalnikom. Blokovno shemo prikazuje slika 2.



Slika 2: Nerekurzivno digitalno sito v strukturi koncentrirane aritmetike s skupnim globalnim seštevalnikom
Fig. 2: The FIR digital filter structure in concentrated arithmetic with a global adder

Strukturo digitalnega FIR sita v koncentrirani aritmetiki s porazdeljenim seštevalnikom je enostavneje implementirati v programirno vezje. V programirnem vezju je enostavneje realizirati večje število zaporednih seštevalnikov, kot pa globalen seštevalnik. Poleg tega je struktura s porazdeljenimi seštevalniki tudi primernejša za modularno zgradbo nerekurzivnega digitalnega sita, kjer je možno enostavno povečati število uporabljenih koeficientov. Podana struktura nerekurzivnega digitalnega sita s slike 1 zadosti drugemu kriteriju o zahtevi po pomnilniku in tretjemu kriteriju o zbiranju in razmeščanju podatkov znotraj strukture. Pri uporabi strukture z globalnim seštevalnikom je potrebno za povečanje stopnje nerekurzivnega digitalnega sita spremeniti celotno strukturo globalnega seštevalnika.

Postopek implementacije nerekurzivnega digitalnega sita v programirno vezje omogoča pomembno zmanjšanje aparaturne kompleksnosti izvedbe aritmetičnih operacij. Pri tem se število potrebnih aritmetičnih operacij ne spremeni. Za zmanjšanje aparaturne kompleksnosti aritmetičnih operacij uporabljenih v nerekurzivnem digitalnem situ smo uporabili zaporedno logiko /7/. Vse spremenljivke so zapisane na bitnem nivoju. Takšen zapis omogoča zmanjšanje aparaturne kompleksnosti implementacije enot za izvaja-



Slika 1: Nerekurzivno digitalno sito v strukturi koncentrirane aritmetike s porazdeljenimi seštevalniki
Fig. 1: The FIR digital filter structure in concentrated arithmetic with a distributed adder

nje aritmetično-logičnih operacij. Princip je podoben cevljenju, ki ga poznamo pri mikroprocesorjih. Ideja je v tem, da se zahtevna operacija razbije na več enostavnih, katere pa lahko tečejo hitreje. Z enostavno implementacijo več enakih struktur za izvajanje aritmetičnih operacij dosežemo njihovo sočasno izvajanje. Zaradi sočasnega izvajanja aritmetično-logičnih operacij je izračun otipka izhodnega signala odvisen samo od dolžine zapisa B_u vhodne besede $u(k)$.

2. Izvedba aritmetično-logičnih operacij z zaporedno logiko

Za ponazoritev izvedbe aritmetično-logičnih operacij z zaporedno logiko vzemimo izračun produkta po enačbi (1) med vektorjem koeficientov **h** nerekurzivnega digitalnega sita z N koeficienti in vektorjem vhodnega signala **u**.

V enačbi sta vektorja **h** in **u** dimenzije N. Za izračun otipka izhodnega signala $y(k)$ potrebujemo N množenj. Če so vrednosti komponent vektorja množitelja u_n omejene na intervalu [- 1 1], jih lahko zapišemo v binarni obliki z dvojiškim komplementom.

$$u_n = -b_{n,0} + \sum_{i=1}^{Bu} b_{n,i} 2^{-1} \qquad n = 0,1,...,N-1 \tag{2}$$

V enačbi (2) je z B_u določena dolžina binarne besede za zapis vrednosti u_n, z $b_{n,i}$ so označene binarne spremenljivke, ki zavzemajo le vrednosti 0 ali 1. Predznak določa prvi najbolj utežen bit $b_{n,0}$, $b_{n,Bu-1}$ pa je najmanjši utežni bit. Z uporabo binarnega zapisa spremenljivke u_n v enačbo (1) zapišemo z,

$$y = \sum_{n=0}^{N-1} h_n \left(-b_{n,0} + \sum_{i=1}^{Bu-1} b_{n,i} 2^{-1} \right). \tag{3}$$

Z zamenjavo vrstnega reda seštevanj dobimo izraz, ki omogoča izračun skalarnega produkta dveh vektorjev **h** in **u** na drugačni osnovi. Iz enačbe (3) zapišemo izraz za delne produkte p_n med komponentami vektorja koeficientov vhoda u_n in komponentami vektorja koeficientov sita h_n,

$$p_n = \sum_{i}^{Bu} h_n b_{n,i} \qquad n = 0,1,...,N-1, \tag{4}$$

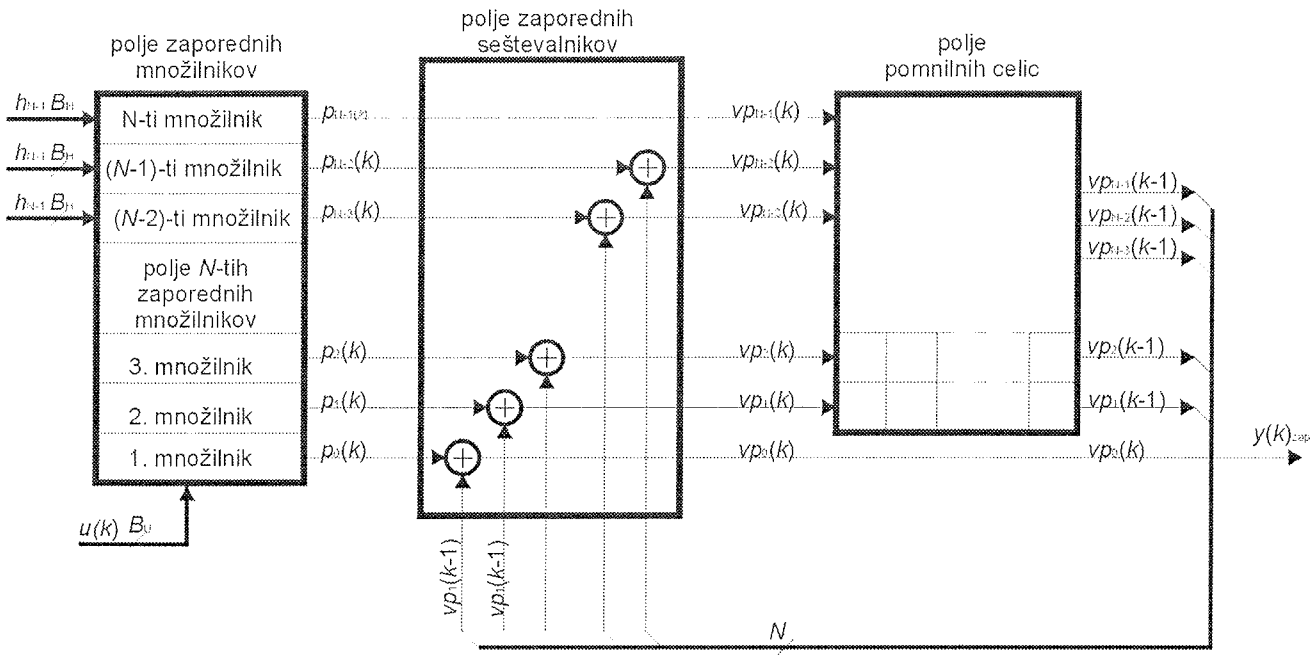
in izraz za izračun delnih vsot produktov vp_n vsot iz delnih produktov p_n,

$$vp_n = p_n + \frac{1}{2} p_{n+1} \qquad n = 0,1,...,N-1. \tag{5}$$

Izračun utežne vsote med vektorjema **h** in **u je**,

$$y = \mathbf{hu}^T = \sum_{n=0}^{N-1} vp_n. \tag{6}$$

Izraz (6) predstavlja tudi izračun izhodne vrednosti nerekurzivnega digitalnega sita z N koeficienti na zasnovi MAC (Multply and Accumulate) strukture. Na osnovi podanih enačb (4), (5) in (6) smo načrtali nerekurzivno sito v strukturi koncentrirane aritmetike s porazdeljenimi seštevalniki.



Slika 3: Povezava treh osnovnih enot nerekurzivnega digitalnega sita v strukturi koncentrirane aritmetike s porazdeljenimi seštevalniki

Fig. 3: Tree structure of FIR digital filter in concentrated arithmetic with distributed adder

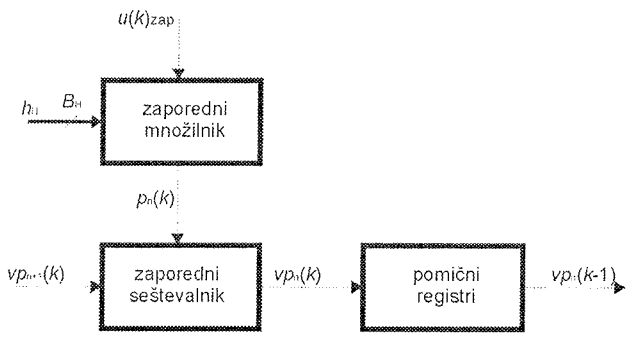
Strukturo nerekurzivnega digitalnega sita smo organizirali tako, da smo pri njeni implementacijo uporabili zaporedno logiko za izvajanje aritmetično-logičnih operacij. Shematsko povezavo treh glavnih enot nerekurzivnega digitalnega sita v strukturi koncentrirane aritmetike s porazdeljenimi seštevalniki, prikazuje slika 3.

Digitalno FIR sito v strukturi koncentrirane aritmetike s porazdeljenimi seštevalniki sestavljajo tri glavne enote: polje zaporednih množilnikov, polje zaporednih seštevalnikov in polje pomnilnih celic.

Tako organizirana struktura digitalnega FIR sita je osnova za implementacijo v programirno vezje.

3. Uporaba zaporedne logike za izvajanje aritmetično-logičnih operacij pri implementaciji digitalnega FIR sita

Namesto povezave osnovnih enot, ki določajo strukturo digitalnega FIR sita s slike 3, lahko strukturo digitalnega FIR sita prikažemo in opišemo tudi kot povezavo posameznih celic, ki vsebujejo zaporedni množilnik, zaporedni seštevalnik in pomični register. Blokovno shemo celice prikazuje slika 4.



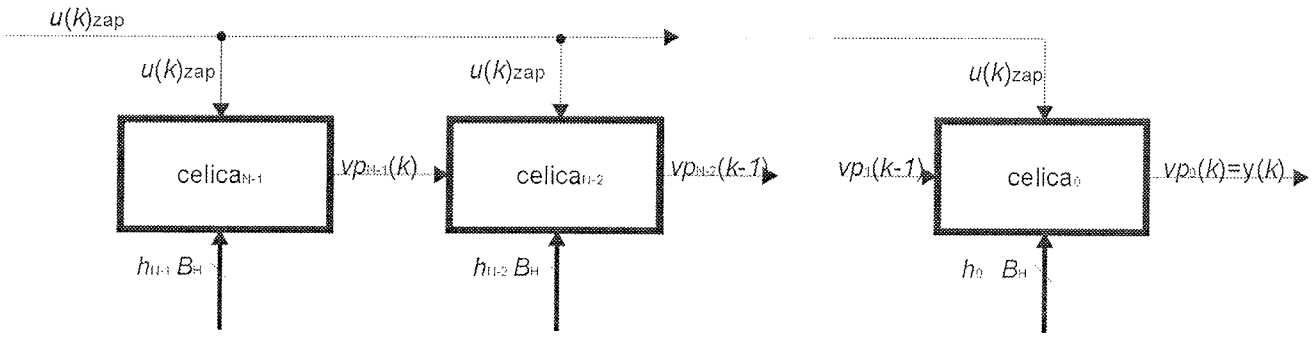
Slika 4. Blokovna shema celice nerekurzivnega digitalnega sita
Fig. 4: The cell block scheme of FIR digital filter

Zaradi uporabe zaporedne logike za izvajanje aritmetično-logičnih operacij pri implementaciji nerekurzivnega digitalnega sita, je struktura celice simbolno prikazana z eno vrstico povezave polja zaporednih množilnikov, zaporednih seštevalnikov in polja pomičnih registrov s slike 3. To smo storili zaradi preglednosti in enostavne razširitve nerekurzivnega digitalnega sita na poljubno število koeficientov. Blokovno shemo strukture digitalnega sita zgrajeno z povezavo *N* celic prikazuje slika 5.

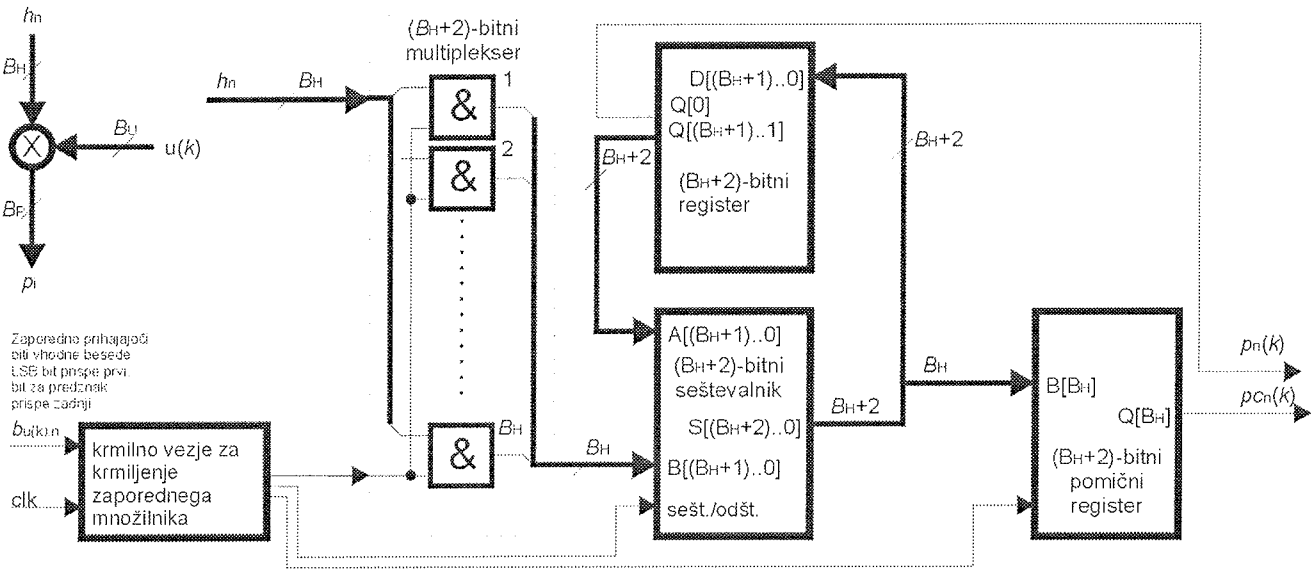
Struktura digitalnega FIR sita je sedaj sestavljena iz *N* enakih gradnikov, ki smo jih poimenovali celice in jih označili z zaporednim številom koeficienta digitalnega FIR sita. Pri tem je z vrednostjo 0 označena celica prvega koeficienta, z vrednostjo *N*-1 pa je označena celica zadnjega koeficienta. Podana zaporedna vezava enakih celic digitalnega FIR sita poenostavi implementacijo FIR sita v programirna vezja, prav tako tudi poenostavi razširitev digitalnega FIR sita na poljubno število koeficientov. Ta oblika strukture digitalnega FIR sita omogočil, da krmilni del sita, ki skrbi za pravilne prenose vmesnih rezultatov in za brisanje registrov ostane popolnoma nespremenjen.

Struktura digitalnega FIR sita z uporabo celic, je v celoti načrtana z uporabo zaporedne logike za izvajanje aritmetično-logičnih operacij. Ugotovimo lahko, da je digitalno FIR sito, prikazano na sliki 5, sestaviljeno z *N* celicami. Le za prvo in zadnjo celico smo uporabili drugačno zasnovo. Prvo celico ($celica_0$) smo načrtali brez zaporednega seštevalnika, zadnjo celico ($celica_{N\_1}$) smo načrtali brez pomičnega registra.

Najkompleksnejši element celice s slike 4 je zaporedni množilnik, ki opravlja produkt med otipki vhodnega signala $u(k)$ in komponentami $h_n(k)$ vektorja koeficientov nerekurzivnega digitalnega sita. Vhodni signal množitelja $u(k)$ digitalnega sita je zapisan v zaporedni obliki z dvojiškim komplimentom. in ga podaja enačba (2). Signal množenca $h_n(k)$ koeficienta digitalnega sita je zapisan v vzporedni obliki. Vrednost vmesnega produkta $p_n(k)$ se izračuna po enačbi (4) z zaporednim množilnikom.



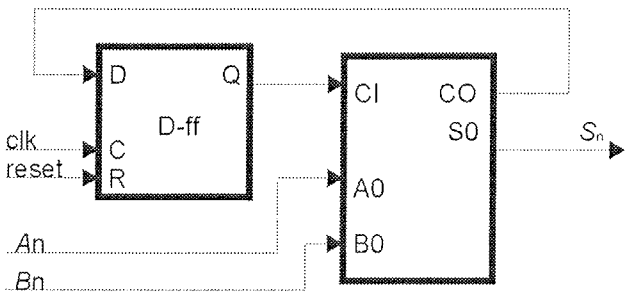
Slika 5: Medsebojna povezava N celic nerekurzivnega digitalnega sita
Fig. 5: The cell structure of the digital FIR filter



Slika 6: Blokovna shema zaporednega množilnika
Fig. 6: Serial multiplier block scheme

Takšna izvedba množilnikov z zaporednim izvajanjem množenja dveh spremenljivk $h_n(k)$ in $u(k)$ močno zmanjša aparaturno kompleksnost celotnega vezja. Pri iterativnem deljenju z 2 ostane na izhodu $Q[0]$ bitnega registra, dolžine B_H+2, vrednost ostanka $p_o(k)$, ki je dolžine B_U bitov. Ta ostanek je v zaporedni obliki, zato ima prikazani zaporedni množilnik na sliki 6 za izhodno vrednost zmnožka $p_m(k)$ dva izhoda: izhod utežnega dela besede $p_n(k)$ dolžine B_H bitov in izhod najmanj utežnega dela besede $p_{om}(k)$ dolžine B_U bitov. Za končno vrednost delnega produkta smo uporabili le zgornjih 16 bitov. Podana oblika zaporednega množilnika potrebuje le en seštevalnik, multiplekser dolžine B_H bitov, ki ga sestavlja polje B_H dvovhodnih IN vrat in zadrževalnik vmesnih vsot. Za krmiljenje zaporednega množilnika digitalnega FIR sita skrbi krmilno vezje.

Drugi element celice je zaporedni seštevalnik, ki izračuna vrednost delne vsote $vp_n(k)$ po enačbi (5). Blokovno shemo zaporednega seštevalnika prikazuje slika 7.



Slika 7: Blokovna shema zaporednega seštevalnika
Fig. 7: Serial adder block scheme

Na sliki 7 je prikazan zaporedni seštevalnik ima dva vhoda. Na vhod A_n je pripeljemo n-to komponento delnega produkta $p_n(k)$ in na vhod B_n pripeljemo n-to komponenta delnega produkta $p_{n+1}(k)$, ki se iterativno deli z dve, kot to opisuje izraz (5). Izhod S_n predstavlja novo izračunano vrednost vsote delnega produkta vp_n.

Tretji sestavni del celice, prikazane na sliki 4, je pomični register (FIFO). Sestavljen je iz D pomnilnih celic velikosti B_U-bitov.

Poleg treh opisanih enot celice, je za delovanje sita potrebno še uporabiti enoto za sinhronizacijo in enoto za vpis koeficientov. Za znižanje cene končnega izdelka pa je potrebno imeti v mislih čim manjše število uporabljenih priključkov, s tem bo tudi zunanji vmesnik programirnega vezja manjši.

Ob inicializaciji programirnega vezja, je vanj potrebno vpisati vektor koeficientov digitalnega FIR sita **h**. Struktura nerekurzivnega digitalnega sita pa se lahko preuredi tudi tako, da so koeficienti zapisani že v samem čipu, če aplikacija ne zahteva spreminjanja koeficientov. Čas vnosa koeficientov namreč podaljša inicializacijo nerekurzivnega digitalnega sita za 16 period signala ure. Takšna struktura nerekurzivnega sita omogoča prilagajanje sita uporabljeni aplikaciji. Pri uporabi nerekurzivnega digitalnega v adaptivnem sistemu je možen sproten vnos koeficientov.

Načrtovanje sita je potekalo s programskim paketom ISE 6.0 podjetja Xilinx. Na najvišjem nivoju je potekalo načrtovanje na osnovi shematskega vnosa z načrtovalskim orodjem Xilinx ECS (Engineering Capture System). V jeziku VHDL je potekalo načrtovanje zaporednega množilnika, FIFO registrov in zaporednih seštevalnikov.

4. Rezultati

Implementacijo digitalnega nerekurzivnega digitalnega sita v programirno vezje smo opravili s pomočjo programskega

razvojnega orodja ISE 6.1 podjetja Xilinx. Za testno aplikacijo digitalnega FIR sita smo uporabili 16 koeficientov s 16-bitno kvantizacijo. Prav tako smo vhodno-izhodno besedo zapisali s 16-bitno kvantizacijo. Na osnovi simulacijskih rezultatov dobljenih s programom ModelSim smo ugotovili, da znaša največja frekvenca osnovnega signala ure 71MHz. Za procesiranje enega otipka potrebujemo 16 period osnovnega urinega signala, kar omogoča frekvenco vzorčenja 4.4MHz.

Odvisnost linearnega naraščanja strukture digitalnega FIR sita od stopnje sita, smo preverili z implementacijo štirih različnih stopenj digitalnih FIR sit v programirno vezje XC3S-400 firme Xilinx /9/. Vezje je družine Spartan-3 s sistemom 400k vrat kar ustreza 8,064 logičnim celicam. Velikost matrike konfiguracijskih logičnih celic (CLBs Configurable Logic Blocks) je dimenzije 32×28, kar znese 896 konfiguracijskih logičnih celic. Vsaka celica zaseda v strukturi programirnega vezja štiri rezine (Slices). Uporabljeno programirno vezje XC3S-400 s 3584 rezinami je eno manjših v družini Spartan-3. Ta družina vsebuje vezja od 50k vrat do 5M vrat, kar je od 200k do 20M rezin (Slices).

Implementacijo smo izvedli za sita z 8, 16, 32 in 64. koeficienti. V tabeli 1 je podana zasedenost programirnega vezja glede na število vhodno izhodnih priključkov (IOB) in število uporabljenih rezin (Slices). Pri vseh digitalnih FIR sitih smo uporabili 16-bitno kvantizacijo vhodno-izhodne besede.

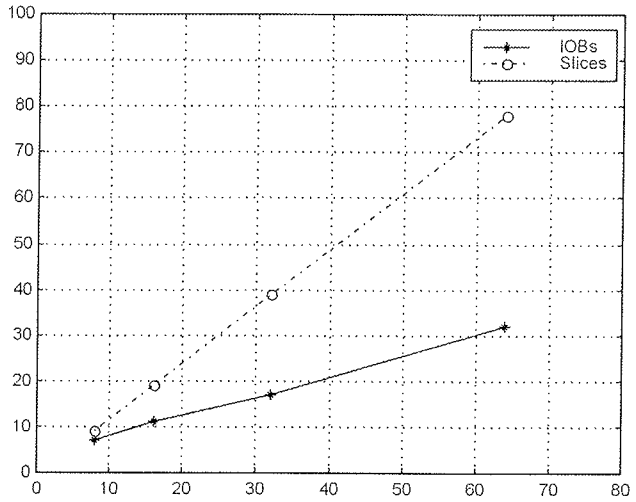
Tabela 1: Zasedenost programirnega vezja XC3S-400 pri implementaciji digitalnega FIR sita z 8, 16, 32 in 64. koeficienti

Table 1: The programmable FPGA device XC3S-400 utilization for 8, 16, 32 and 64 taps digital FIR filter

število koeficientov	8	16	32	64
število vhodno-izhodnih priključkov (IOBs) (max 221)	16 (7%)	25 (11%)	39 (17%)	72 (32%)
število rezin (Slices) (max 3584)	349 (9%)	702 (19%)	1407 (39%)	2829 (78%)

Na sliki 8 podajamo odvisnost zasedenosti programirnega vezja XC3S-400 glede na število vhodno-izhodnih priključkov in glede na število uporabljenih rezin (Slices) v odvisnosti od stopnje sita. Izbrali smo digitalna FIR sita z 8, 16, 32 in 64. koeficienti.

Iz slike 8 vidimo, da zasedenost programirnega vezja narašča praktično linearno s stopnjo digitalnega FIR sita. Zasedenost programirnega vezja XC3S-400 pri implementaciji digitalnega FIR sita s 64. koeficienti in 16-bitno vhodno-izhodno besedo znaša 78% strukture in 72% vhodno-izhodnih priključkov uporabljenega programirnega vezja XC3S-400. V večja programirna vezja družine Spartan 3 pa lahko brez težav implementiramo nerekurzivna digitalna sita z več kot 100 koeficienti.



Slika 8: Odvisnost zasedenost programirnega vezja XC3S-400 od stopnje sita pri implementaciji digitalnega FIR sita z 8, 16, 32 in 64. koeficienti

Fig. 8: The programmable FPGA device XC3S-400 utilization for 8, 16, 32 and 64 taps digital FIR filter

Takšno izvedbo aritmetične logično enote za izračun utežne vsote in njeno uporabo v digitalnih FIR sitih lahko izvedemo FIR sita s 100 koeficienti le z enim programirnim vezje družine Spartan-3.

5. Zaključek

V prispevku smo opisali aritmetično-logično enoto z zaporedno logiko za izračun utežne vsote s programirnimi vezji. Opisano aritmetično-logično enoto smo uporabili pri implementaciji digitalnega FIR sita. Podrobno smo opisali strukturo aritmetične-logične enote, pri katerem smo uporabili zaporedno logiko za izvajanje aritmetičnih operacij. V ta namen smo razvili zaporedni množilnik, kjer je množitelj podan v zaporedni obliki, množenec pa v vzporedni obliki. V nerekurzivnem digitalnem situ z N koeficienti smo uporabili N zaporednih množilnikov. Za implementacijo N-1 porazdeljenih seštevalnikov, smo uporabili zaporedne seštevalnike. Postopek načrtovanja je potekal s pomočjo programskega paketa Xilinx ISE 6.1 WebPack. Na najvišjem nivoju smo uporabili shematski vnos strukture, na najnižjih nivojih smo opisali posamezne enote v VHDL jeziku. S takšnim pristopom smo zelo dobro izkoristili strukturo programirnega vezja. Uporaba aritmetično logične enote za izračun utežne vsote v digitalnem FIR situ omogoča njegovo implementacijo v le eno programirno vezje družine Spartan-3 firme Xilinx. Takšna izvedba digitalnega FIR sita, ki omogoča vpis vseh koeficientov v času med dvema otipkoma vhodnega signala, je primerna za uporabo v adaptivnih sistemih. Opravili smo implementacijo štirih različnih stopenj digitalnega FIR sita v programirno vezje XC3S-400: z 8, 16, 32 in s 64. koeficienti. Pri vseh treh stopnjah smo uporabili 16 bitno kavantizacijo vhodno-izhodne besede.

Z ugotavljanjem odvisnosti med zasedenostjo programirnega vezja in stopnjo nerekurzivnega digitalnega sita smo pokazali, da zasedenost programirnega vezja narašča praktično linearno s številom koeficientov sita. Pokazali smo tudi, da zaseda implementacija digitalnega FIR sita s 64. koeficienti in 16 bitno kavntizacijo vhodno-izhodne besede 72% vhodno-izhodnih priključkov in 78% notranje strukture programirnega vezja XC3S-400. S tem smo tudi pokazali, da uporaba opisane aritmetične logične enote za izračun sprotne utežne vsote v digitalnem FIR situ, omogoča implementacijo digitalnih sit z 100 koeficienti v eno samo programirno vezje.

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INTEGRAL NONLINEARITY DETERMINED BY SELECTION ORDER OF CURRENT ARRAY UNITS IN DA CONVERTERS

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Key words: CMOS D/A converter, current array, bits-selection-order, thermometric converter

Abstract: This paper analyses characteristic of switching-scheme for the curent source array that was used in 14-bit CMOS DA Converter. It presents 8-bit thermometric bits-selection-order (BSO) analysis results, where the single bit current source is constructed as a group of two equal cell-units. The BSO order algorithm varies position of the group, while the current-cells inside the group are always placed simetrically over the center of the layout area. Bit-selection-order value is a decimal code value of the position selection. The final solution is compared with straight horizontal and straight vertical BSO with different error distributions from which posible integral nonlinearity (INL) of the final product, can be estimated. The analysis of error distribution influence on INL further demonstrates that with bits mixed selection-order INL error is always below 0.05 LSB when average current error is below 1%.

Integralna nelinearnost določena z zaporedjem izbire tokovih virov v DA pretvornikih

Kjučne besede: CMOS D/A pretvornik, polje tokovnih virov, zaporedje preklapljanja bitov, termometričen pretvornik

Izvleček: Ta članek obravnava karakteristiko preklopne sheme za polje tokovnih virov, ki je bilo uporabljeno v 14-bitnem CMOS digitalno - analognem pretvorniku. Predstavljeni so rezultati analize 8-bitnega termometričnega zaporedja izbire (BSO), kjer je bitni tokovni vir zgrajen kot enota dveh enakovrednih osnovnih tokovnih celic. BSO algoritem spreminja mesto bitnega tokovnega vira, medtem ko sta osnovi tokovni celici vedno postavljeni simetrično, glede na center geometrije polja tokovnih virov. BSO vrednost predstavlja decimalno kodo izbire mesta bitnega tokovnega vira. Integralna nelinearnost (INL) končnega izdelka je ovrednotna z različnimi porazdelitvami napake (Slika 3), glede na vodoraven (Slika 1) in navpičen (Slika 2) BSO algoritem. Analiza vpliva porazdelitve napake na INL kaže, da je INL napaka pri mešanem BSO (Slika 4) vedno pod 0,05 LSB, če je povprečna tokovna napaka pod 1%.

1. Introduction

Low integral nonlinearity (INL) in high-bit-count DA Converters is dificult to accomplish with resistor-strings, R2R converters, or binary-weighted current sources /6, 1, 3, 5, 2/. Studies and measurenments indicate that there are non-constant process parameters and region gradient over silicon wafer. In our research we used aproach of two current arrays where each of the array was controlled with thermometer coders.

It is therefore our goal to search for the most suitable organisation of an array, number of current units in one step group and, on the most suitable switching-scheme for 8-bit current array.

As already explained in /4/, to suppress the linear error, the current step must be split into more than one current units per-step. To minimize the silicon area, only two current units per one unit group were used and placed symetrically over center of the array. Considering last statement we have 2 x 256 current units.

Because of technology isues, seperated functional blocks (sources, switches an selectors) would result in an increased circuit area. In our research our goal is to combine all functions in one cell - current logic block (CLB) cell /8/.

CLB cells are composed of:

- current source with cascode devices,
- switches to one of two current outputs and
- digital selection circuit, which determines the state of the switches from horizontal and vertical control signals.

Proportion of CLB dimensions is set to 1:10, so the shape of current array was chosen to be 8 x (32 x 2) with additional columns for biasing circuit.

2. First accession

Two reference selection-orders of the BSO were used in analysis:

- horizontal selection-order (Figure 1) and
- vertical selection-order (Figure 2).

For both reference principles, unit group consists of two CLB cells, placed symmetrically to center.

To find proper solution, we have to cosider which effects have influence on the resulting INL error and how does the gradient of the process parameters effect the INL error (Figure 3 /7/).

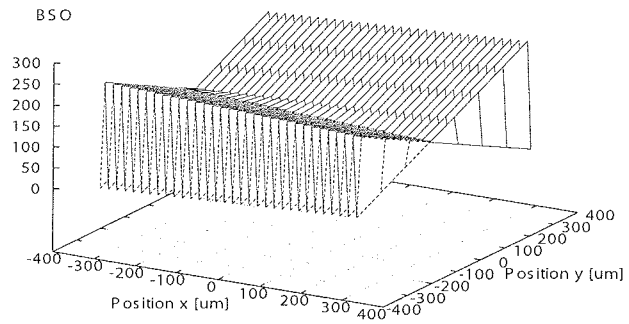

Figure 1: Horizontal selection-order.

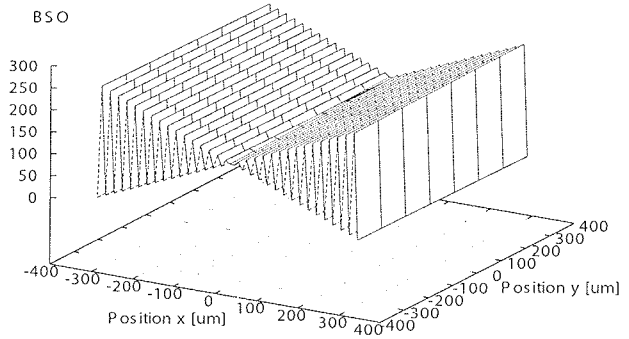

Figure 2: Vertical selection-order.

All the results are found in Figure 5. It is evident that all even order distributions yield zero INL error, as we already assumed when splitting step units in two current cells (CLB's). As can be seen in Figures 3.c and 3.g for 1-D parabolic error distribution INL error results (Figures 5.c and 5.g) are resembling. The main difference is that in Figure 5.g, vertical 1-D error distribution, the ratio between horizontal an vertical BSO is four times higher than in horizontal 1-D distribution (Figure 5.c) which corresponds to CLB array shape 8 x (32 x 2).

Superior results are achieved for vertical selection-order. Selected step order goes more frequently from one edge to the other vertically (8 steps) than horizontally (32 steps) which means that final solution will include best results if selections are distributed through all array area as frequently as possible. Simmilar results are presented in Figure 5.e.

3. Proposed solution - mixed selection-order

To build more flexible BSO algorithm, it is possible to cover more complex parameters gradient over silicon as well as taking into account any CLB array shape. The BSO anal-

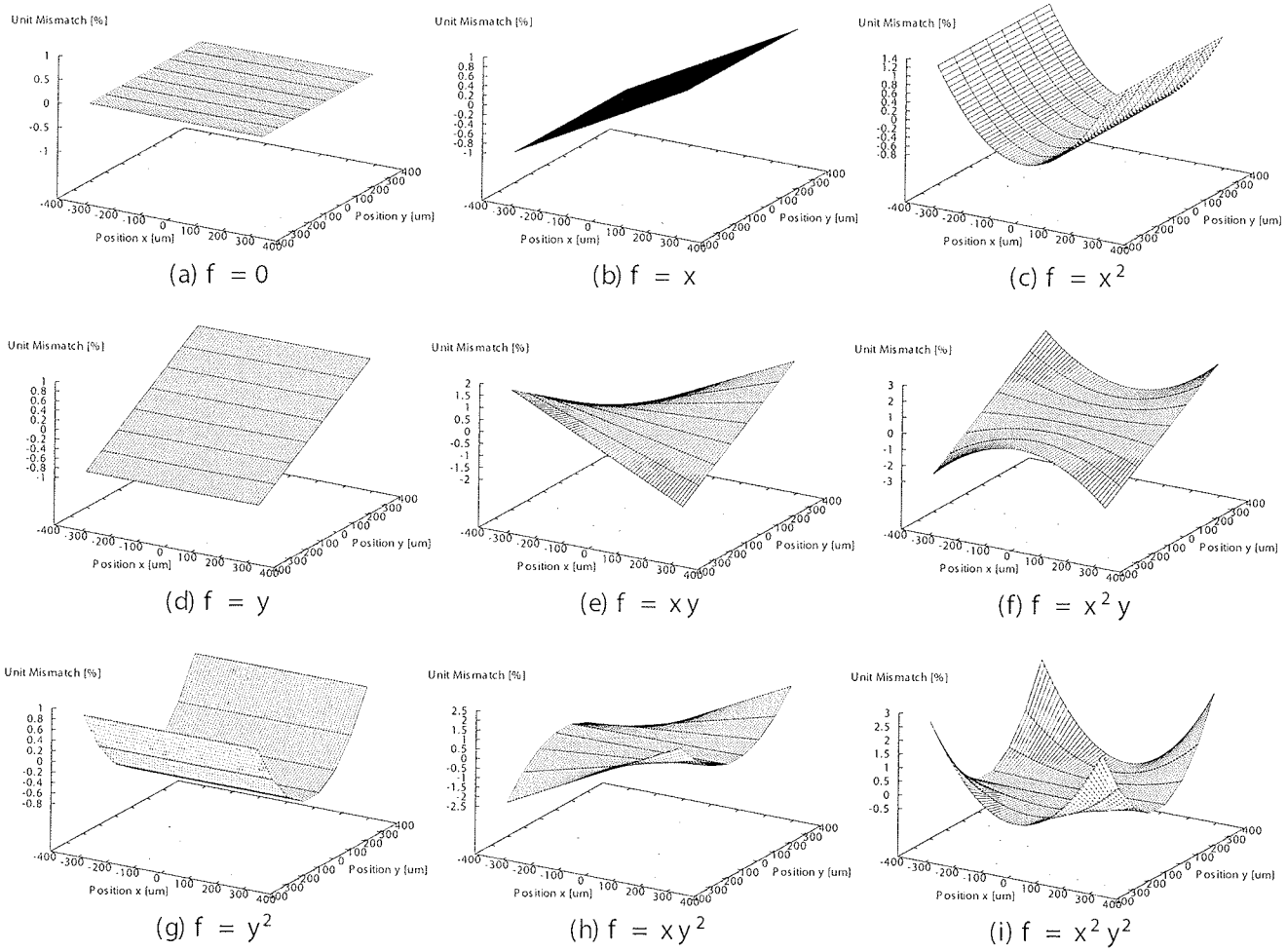

Figure 3: Error distribution through array area.

ysis indicates that the most encauraging results can be achieved by mixing horizontal and vertical bits order. In our research, we proposed bits mixed selection-order (BMSO), as shown in Figure 4.

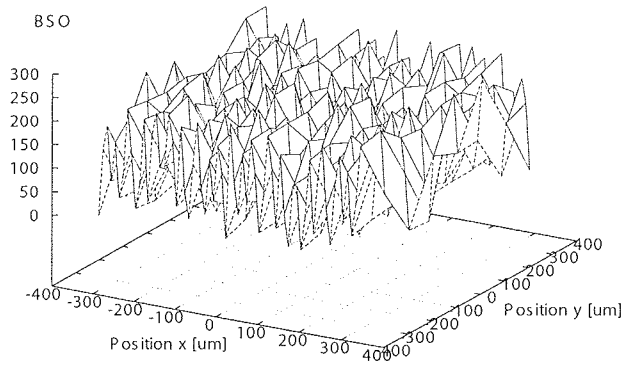

Figure 4: Mixed selection-order.

Using this approach, it is therefore evident that the random parameter distributions are covered much better, even with only two unit cells building the MSB group.The results of INL errors from Figure 5 show that for most common errors (Figure 5c, 5g and 5i), INL error is always below 0.05 LSB when average current error does not exceed 1% thermometric active area (Figure 3).

4. Conclusions

Theoretical analysis supported by the predicted and realistic distribution of the process parameters over the silicon area was implemented on integrated digital to analog converter, costructed by the thermometric 8-bit subblock. After the measuring, results will determine resolution for the overall high resolution D/A. Through we can conclude that the complete converter can be covered only by thermometric subblocks, probably including a less complicated autocallibration block.

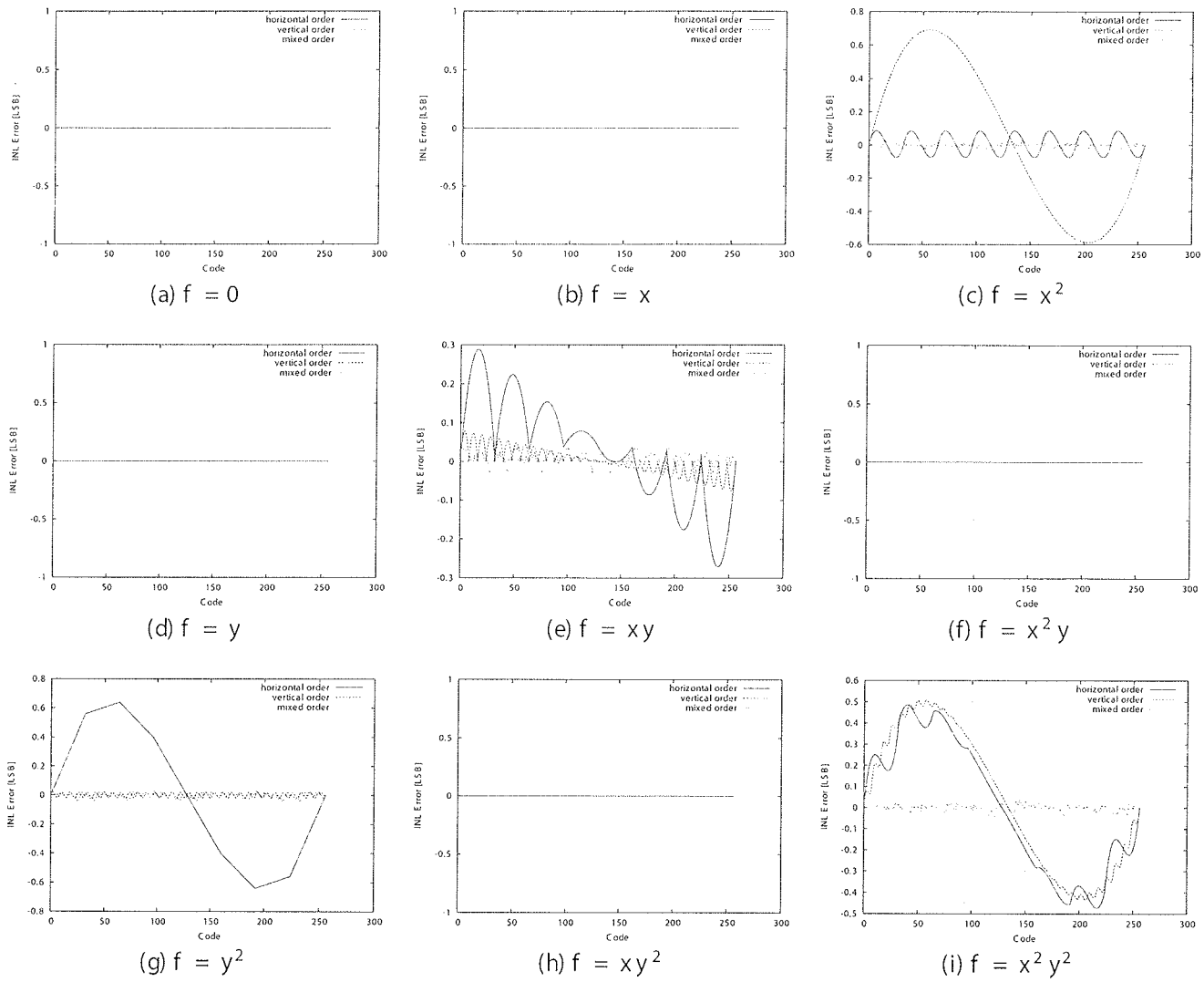

Figure 5: INL vs. selection-order.

5. Acknowledgments

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DEVELOPMENT OF USB 2.0 COMPLIANT GPIB CONTROLLER

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Key words: Automated measurement, Computer interfaces, General Purpose Interface Bus

Abstract: This paper describes a development of a custom designed General Purpose Interface Bus (GPIB) controller which is used as the interface between GPIB and PC. The controller is designed as a Universal Serial Bus (USB) 2.0 compliant external device, which provides plug-and-play operation, high speed of data transfer and is powered fully from the USB. In contrast to conventional GPIB controllers in the form of PC cards, such a design extends its usage to notebooks or other computers with no available I/O slots. The FLASH program memory based AT90S8515 microcontroller which is used for data transfer and protocol handling also enables easy firmware upgrade. For simple controller usage the appropriate driver is developed in a graphical programming language LabVIEW, which we use for instrument control software development.

Razvoj GPIB krmilnika združljivega z USB 2.0

Kjučne besede: Avtomatizirane meritve, računalniški vmesniki, GPIB

Izvleček: Članek opisuje razvoj krmilnika za GPIB vodilo (General Purpose Interface Bus), ki se uporablja kot vmesnik med GPIB vodilom in osebnim računalnikom. Krmilnik se na računalnik priključi preko univerzalnega serijskega vodila (USB), ki omogoča enostavno uporabo, visoko hitrost prenosa podatkov in nudi napajanje. Za razliko od običajnih GPIB krmilnikov, ki so osnovani kot vtične kartice, je ta krmilnik primeren tudi za prenosnike in računalnike brez prostih razširitvenih rež. Jedro krmilnika je mikrokrmilnik AT90S8515, ki je vsebuje FLASH spomin in tako omogoča enostavno nadgradnjo programske opreme. Za enostavno uporabo krmilnika smo izdelali tudi gonilnik za programski jezik LabVIEW, ki ga tudi uporabljamo za avtomatizacijo meritev.

1. Introduction

Personal computers became necessary equipment in science laboratories in the last decade /1/. One of reasons is their usage in measurement automation and documentation which is achieved with computer-controlled instruments. A very popular interface for connection between the PC and instruments is General Purpose Interface Bus (GPIB), which is still the most common interface, although several other types of interfaces (Universal Serial Bus (USB), IEEE 1394, Ethernet, etc.) are on the move /2/, /3/. Reasons for this include numerous GPIB instruments available and low latency when compared to otherwise faster standards in parentheses above /4/.

To connect instruments to a PC a suitable GPIB controller is required which is usually in a form of a computer card. Because of relatively simple design and low-cost components we have decided to develop a GPIB controller ourselves. Since we wanted the controller to be applicable also for notebooks, we have chosen USB, which is the most common built-in interface on contemporary computers. Our concept was accepted as Design idea in EDN Journal /5/. In the following, the development of the USB based GPIB controller will be presented in detail and an example of its usage will be given.

2. Development of USB based GPIB controller

GPIB /6/, initially named Hewlett-Packard Interface Bus (HP-IB), later standardized as IEEE-488 and IEC-625, is a parallel bus that uses 24-pin connector to connect devices in a star or a bus configuration. There are three main types of devices on the GPIB bus; controller, talker and one or more listeners. The bus can have only one active controller, which is a bus master and addresses devices to talk or listen by use of GPIB bus commands. A talker transmits data that are received by one or more listeners.

The GPIB controller we developed is designed as a USB device controlled by a host PC, where one port of the controller is connected to the USB and other to a GPIB bus. The controller is built on a double-sided PCB that fits into a box of outer dimensions of 123 mm x 30 mm x 70 mm.

In order to simplify the usage of the GPIB controller a LabVIEW driver was developed, which communicates with the controller by a custom developed protocol through USB using a virtual COM port (VCP) driver. To simplify adaptation of existing programs in LabVIEW, the driver is compatible to the built-in one. In the following sections the hardware, protocol, firmware and the driver are described in detail.

3. Hardware

The controller can be divided into three main parts, where the microcontroller as the central block represents the communication gateway between PC (through USB interface) and GPIB bus (through GPIB line drivers), as shown in Fig. 1.

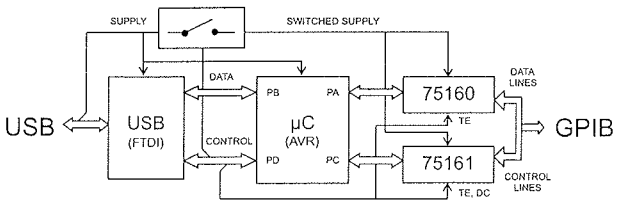

Fig. 1: Block diagram of the USB based GPIB controller

USB interface is based on a FTDI FT245BM integrated circuit /7/ that provides an 8-bit parallel interface to the microcontroller and a virtual COM port on the PC side. Built-in buffer (FIFO) greatly simplifies firmware in the microcontroller. The integrated circuit provides USB 2.0 compatibility and allows data transfer under USB 1.1 specification, i.e. 12 Mb/s. It also provides an output line that goes low when it is enumerated and USB is not in suspend state. External memory chip provides storage for information such as product description and maximum current consumption and can be programmed directly from a host PC.

At GPIB side of the controller appropriate line drivers are required to meet GPIB standard specifications of 48 mA sink current and high impedance state when no power is applied. Standard integrated circuits, 75160 /8/ and 75161 /9/ developed especially for GPIB are used, while sequence control is completely implemented in controller's firmware. The most important control signals for operation for data transfer are Attention (ATN), Data Valid (DAV), Not Ready For Data (NRFD), Not Data Accepted (NDAC) and End Or Identity (EOI). Direction of signals is controlled by TE (Talk Enable) input for data and handshake lines and by DC (Direction Control) for management lines. Both signals are controlled by the firmware.

An AVR microcontroller Atmel AT90S8515 /10/ is used to control all circuitry. It is a 44 pin RISC device with in-circuit programmable FLASH memory and many peripheral units, which are not all utilized in our case, since besides input / output (I/O) ports the only peripheral unit used is timer. In-circuit programming through a 6-pin connector simplifies firmware design and its upgrades. The microcontroller runs at its maximum frequency of 8 MHz to allow the fastest data transfer possible. Both external interrupts are used in conjunction with the USB interface. One triggers when USB goes to suspend state, while the other wakes up the microcontroller on the first received byte.

USB provides power supply of +5 V / 500 mA and thus allows low power devices to be used without additional power supply. In our design USB interface with memory IC and microcontroller are powered directly from USB, while GPIB buffers are powered from USB through a transistor switch. Overall maximum current consumption of the controller is 320 mA during normal operation and is minimized during USB suspend state, by disconnecting the GPIB buffers from the power supply and setting the microcontroller to low-power mode.

Fig. 2 shows the PCB of the controller, while Fig. 3 shows the controller with connected USB and GPIB cables. The PCB was made using milling machine and partially assembled on the manual SMD placer that we use for research & development prototypes and educational purposes. Predominant use of SMD components in the controller makes its fabrication easily automated and lowers the cost of components.

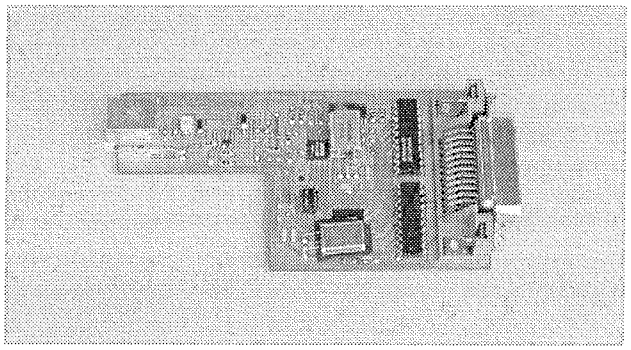

Fig. 2: Top view of printed circuit board of the controller

Fig. 3: The controller with connected cables

4. Protocol

The controller communicates with the PC through a logical serial interface which does not provide control signals and registers like plug-in boards and therefore a certain protocol is necessary to distinguish between data and control bytes.

We have developed a protocol, which is based on the AT protocol for modems; commands begin with letters IB, which are followed by a one character command code and an optional binary or character parameter. Bus commands are sent as binary values, which enables each of 256 possible values to be transferred. The problem of transferring binary data or a problem of data transparency was solved by a protocol similar to Binary Synchronous Communication (BSC) protocol /11/ in which three control characters are used to transfer a binary data block. These are Data Link Escape (DLE), Start Of Text (STX) and End Of Text (ETX). A data block always begins with the pair DLE/STX and ends with DLE/ETX. If a DLE is to be transferred anywhere in the data stream, it is followed by another DLE,

denoting it as a part of the data as can be seen in Fig. 4. Bus addressing when sending or receiving data is not implemented in firmware and has to be done by sending bus commands, which is implemented in the driver. The controller commands are listed in Table 1. All responses of the controller are one byte long to allow simple interpretation and include success code or error specific code.

DLE	STX	*data*	DLE	DLE	*data*	DLE	ETX

Fig 4: BSC protocol

5. Firmware

The AVR microcontroller is used to control all lines of the GPIB interface and to communicate with the PC through the USB interface. Main loop of firmware program contains two major successive operations: (a) waiting for IB delimiter and receiving a command and (b) executing the command. If the command is in error (i.e. too long or an invalid command code) it is rejected and a Negative Acknowledge (NAK) is returned to the PC.

Data and bus command transfer have a time limit for each transferred byte. If time-out occurs the microcontroller's program sends an error code to the PC and the loop repeats. When USB goes into suspend state the transfer is also interrupted and is followed by powering off the GPIB drivers and putting the microcontroller into low-power mode. The microcontroller wakes up again when another byte is received. The program was written in C language, compiled by CodeVision AVR and is approximately 1500 words (3.0 KB) long.

The execution speed of the microcontroller mainly determines the maximum data transfer rate which is in our case theoretically limited to 225 KB/s. Actual measured transfer rates using HP54522A digital oscilloscope were 190 and 174 KB/s for talking and listening, respectively.

6. PC driver

We designed a driver in LabVIEW /12/ environment as a collection of VIs, since LabVIEW is widely implemented at our faculty and at the same time it is one of the most popular programs for measurement control and automation. LabVIEW allows fast development of complex and easy-to-use programs. The driver is compatible with the LabVIEW's built-in GPIB driver simplifying adaptation of existing programs to the new interface. Only one additional input is required, i.e. serial port number. VIs are described below.

USB GPIB Initialization opens serial port, powers on the controller and initializes it according to specified parameters (re-addressing required, REN state).

USB GPIB Write transfers data to a device. It also addresses the device if an address is given and the device is not already addressed. After data exchange, the function deaddresses the device if specified at initialization. This addressing logic is the same for all functions.

USB GPIB Read reads data from a device. The VI will stop reading when EOS is detected or specified number of bytes received. This is additional option to the EOI implemented in firmware. Data transfer mode for write and read (EOI, End Of String character (EOS)) can be adjusted with a parameter.

Command	Function
IB	Powers on and initializes the controller.
IBCx, IBcx	Sends byte *x* (binary) as a bus command. ATN line can be released after transfer or not, which enables multi-byte commands to be sent.
IBdata	Sends binary data to GPIB bus. Returns error if there is no listener.
IB?	Receives binary data till EOI is detected, timeout or cancelled.
IBB	Receives one byte (ignores EOI).
IBIx	Sends identification string to the PC.
IBZ	Conducts interface clear.
IBO	Powers off the controller.
IBe	Sets EOI mode for sending data.
IBt, IBT	Sets timeout for handshake and total timeout.
IBm	Controls state of REN line.
IBDE\AA, IBDTx, IBDCx, IBDMx, IBD?x	Debug commands enables each line of the GPIB bus to be independently controlled. They are useful when developing new protocol and for hardware debugging.

Table 1: Controller commands

USB GPIB Clear resets a device or all devices using Selected Device Clear (SDC) or Device Clear (DCL). Which command is send depends on whether an address is given.

USB GPIB Read STB reads status byte using serial poll.

USB GPIB Wait RQS calls USB GPIB Read STB in regular interval waiting for request bit to be set. This bit is an indicator that a device needs attention (ex. measurement is finished).

USB GPIB Close powers off the controller and closes serial port.

The microcontroller performs only simple tasks while higher level operations are implemented in the driver. For example: the controller cannot address a device, send data to it and de-address using a single command from the PC. This must be implemented in three steps, i.e. with three controller commands. This separation enables many features to be implemented or updated without changing the controller's firmware and enables faster and simpler updates since the reprogramming of the microcontroller is not required.

Since many other programs (Visual Designer, FieldPoint and HPVee and other programs like MATLAB, C++ or Visual Basic) support virtual serial port, our USB based GPIB controller needs no hardware or firmware changes, but only specific drivers to be implemented in these programs.

7. Discussion and conclusions

The USB GPIB controller was developed as a compact plug-and-play device with maximum transfer rate of 225 KB/s. Predominant use of SMD components in the controller makes its fabrication easily automated and lowers the cost of components.

Firmware of the microcontroller can be upgraded to support other GPIB features like operation as a device. Upgrading can be very simplified by using newer version of microcontroller, ATmega8515, which features self-programming that enables firmware to be upgraded directly from a PC (without opening the controller). This would enable users to download new firmware from the Internet and install it themselves. At the same time, ATmega8515 with its 16 MHz clock frequency would double maximum transfer rate, since the microcontroller is the limiting factor. The speed can be further increased by using special GPIB circuits.

Many features can be added in the driver and therefore performed in the field, without using a microcontroller programmer. Nevertheless, drivers can be upgraded easily in LabVIEW programming environment as well as easily adapted to other programming environments that support serial port. VISA drivers would also be beneficial and would additionally ease conversion of existing programs. Nonetheless, USB interface enables the controller to be used with both, desktop computers and notebooks. In this way, researchers may use their notebooks to run self-built virtual instruments with the USB GPIB controller in a laboratory. Furthermore, non-standard features can be also implemented. GPIB printer emulation was already successfully applied and used for digital oscilloscope's (HP 54600B) waveform printout. The controller is comparable (concerning speed and dimensions) to commercial controllers like National Instruments' GPIB USB B.

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AFFINITY OF CONTACT MATERIALS TO FORM THE ELECTRIC DRAWN ARCS

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Key words: drawn electric arc, arc formation, sliding contact, commutator, arc ignition voltage, contact material.

Abstract: Electro mechanic contacts are widely used in several appliances, because they are cheap, but also very robust, capable to withstand overvoltage and overcurrent surges, and when used in electric relays they enable galvanic separation of electric circuits. Especially they are necessary with commutators of universal electric motors for they are enabling commutation. These motors achieve high power per a unit of volume due to their high shaft speed, and they are produced at relatively low costs for a unit of power. So, they are economically very important for their numerous production, and they use sliding contacts for their operation. The sliding contacts are mechanical contacts, as switching contacts are, and so electric arcs ignite between their contact members during commutation. Therefore it is very important to determine contact materials with a small tendency to form the electric arcs. The arcs between electrodes of the sliding contacts are usually drawn arcs, so that affinity of the contact material to form the drawn arcs is very significant attribute of determining the right contact mate-rials. Conclusions made for the sliding contacts are also useful for the switching contacts.

Težnja kontaktnih materialov k tvorjenju električnih potegnjenih oblokov

Kjučne besede: potegnjeni električni oblok, nastanek obloka, drsni kontakt, komutator, nape-tost vžiga obloka, kontaktni material.

Izvleček: Elektromehanski kontakti so množično uporabljeni v številnih napravah, ker so poceni, vendar robustni, zmožni vzdržati prenapetostne in preto-kovne preobremenitve in kadar so uporabljeni v električnih relejih omogočajo galvansko ločitev tokokrogov. Posebno so nepogrešljivi pri komutatorjih univerzalnih električnih motorjev, kajti omogočajo komutacijo. Ti motorji razvijejo veliko moč na enoto volumna zaradi velike hitrosti vrtenja in njihovi proizvodni stroški na enoto moči so relativno majhni. Zaradi njihove velikoserijske proizvodnje so ekonomsko zelo pomembni. Za svoje obratovanje pa uporabljajo drsne kontakte. Drsni kontakti so mehanski kontakti, kakor so tudi stikalni kontakti in zato se med njihovimi kontakti pri komutaciji vžgejo električni obloki. Zato je zelo pomembno določiti kontaktne materiale z majhno tendenco tvorjenja električnih oblokov. Obloki med drsnimi kontakti so ponavadi potegnjeni obloki, tako da je težnja kontaktnih materialov k tvorjenju potegnjenih oblokov zelo pomembna lastnost pri določanju pravega kontaktnega materiala. Zaključki, narejeni za drsne kontakte, so uporabni tudi za stikalne kontakte.

1. Introduction

Talking about affinity of the contact materials to form the electric drawn arcs, we must have in mind that it is not a physical quantity, but rather a conception, which is numerically estimated by one or more physical quantities. To begin with, we consider the voltage - current (*UI*) stationary electric arc characteristics, for instance of the copper contacts, shown in Fig. 1 as hyperbolae, in relation to the pure resistive load, shown in the same figure - the line marked with the label "break" /1/. This line illustrates the load characteristic of the electric arc at the breaking of an electric resistive circuit by the axial switching contacts. This drawn arc ignites at the voltage of 13.1 V, which is slightly over the voltage of the asymptote of the hyperbolae, and at the current of 1.95 A. The voltage of the asymptote is defined as the minimal arc voltage U_m by Holm /1/ and it is the property of the material. But we name it as the infimum arc voltage because it is the greatest lower limit voltage. The arc burns until its length is 0.8 mm and is extinguished at the voltage of 48.7 V and at the current of 0.73 A.

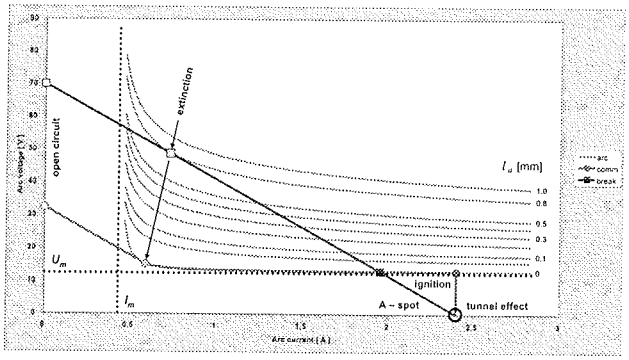

Fig. 1: The UI stationay and load arc characteristics.

Legend:
arc stationary arc characteristics,
comm load arc characteristic at resistance commutation,
break load arc characteristic at breaking resistive load.

If another contact material is taken into consideration then the hyperbolic characteristics are the same curves, but voltage (U_m) and the current (I_m) the asymptotes have different values. The current asymptote is defined as the infimum arc current and is also the property of the material. If the value of the U_m - asymptote is higher than the one of copper the arc ignites at a lower current, and of course, at a higher voltage, and its length is shorter at the point of the extinction. The values of the arc voltage and the arc current at its extinction are also changed. Because the ignition and the length of the arc are depended on the U_m - asymptote, we decide that the infimum arc voltage is just the proper quantity to define affinity of the contact material to form the electric drawn arc.

It seems very simple to define affinity of the contact materials to form the drawn arcs between the axial switching contacts, but in the case of the sliding contacts, such as they are in the commutators, is a much more difficult task. Namely, the drawn arc ignites and burns at a macroscopic geometrical separation of the axial switching contacts, but researching the arc phenomenon with the sliding contacts it must be taken into account, that the drawn arc ignites and burns between the overlapping electrodes with no macroscopic geometrical separation of them /2/,/3/. If we consider only the *UI* stationary arc characteristics and the load characteristic of the arc during the resistance commutation, shown in Fig. 1 - the diagram marked with the label "comm", it is not selfevident that the infimum arc voltage is the measure of this kind of affinity. The arc ignites at the infimum value of the arc voltage and at the full value of the current through the contact. It burns at the voltage, which slightly rises from the infimum arc volt-age of 13 V up to 15.2 V for copper, and is extinguished at the latter value of the voltage and at the current of 0.59 A. Its length is in the range of some nanometres throughout its burning, so it is a short arc. It is exactly the same with another contact material: the ignition occurs at the infimum arc voltage and at the full current, the burning is at its length of some nanometres and at the corresponding voltage, and extinction is nearly at the current asymptote, which value is the infimum arc current. Therefore we have to establish the mathematical model of electric current conduction through the gap of some nanometres between the commutator bar and the brush during the commutation to make a clear definition of affinity of the contact materials to form the drawn arcs. When the commutator bar moves over the brush, the thickness of the gap between them varies, and so the way of the current conduction alters from tunnel effect to arc conducting mode - Fig. 2.

If the thickness of the gap is so large, that its corresponding voltage drop equals to or is greater than the infimum arc voltage U_m, the arc ignites. With the same thickness of the gap, some contact materials form the drawn arcs, but some not, depending on their infimum arc voltage. As this voltage is the property of the contact material, it fully determines affinity of the contact material to form the electric drawn arc.

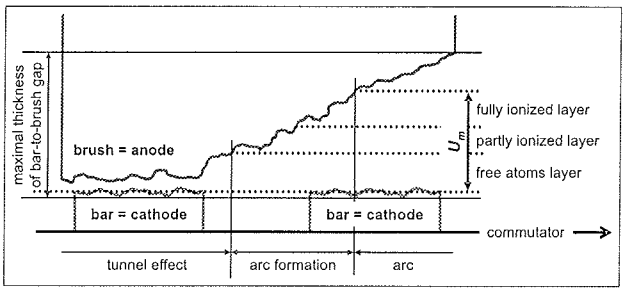

Fig. 2: The formation of the electric drawn arc during the commutation.

There are many physical constants and variables in this paper that are not explained in the text, so their definitions are present in the chapter of used symbols at the end of the paper. We also deal with many chemical elements, although they could not be used as pure materials in contact technique. The direct current case is considered by this model.

2. The mathematical model of the drawn arc formation

With the sliding contacts of the commutator, a very thin insulating film arises on the contact surface /1/,/4/. This film is the collector film. Beside it, there is also the gap between the contacts. The gap is filled with atoms and molecules of an external medium, and also with the atoms of the contact materials. The gap and the film thickness are up to a few nanometres, so that no ionization occurred.

The electric current flows due to tunnel effect. One contact member is a cathode, the other one is an anode. The charge carriers are free electrons in the electric field of the gap, so they are accelerated when moving along the path through the gap. They are emitted from the cathode by three ways:

- by the field emission, called also the cold emission;
- by the thermionic emission including also the Schottky effect, which is depended on the electric field, but its contribution is not included in the cold emission;
- by the emission due to the different work functions of the cathode and anode materials.

Considering the cathode is still cold, only the field emission is taken into account, and the current density is defined by the Fowler - Nordheim equation /5/,/6/ and /7/, which is equal to Eq. (1) for the electron emission from the smooth and unstained metal cathode in vacuum:

$$j_E = \frac{e^2}{8\cdot\pi\cdot h\cdot\frac{m_e^*}{m_e}}\cdot\frac{E^{*2}}{V_{\phi\kappa}^*}\cdot e^{-\frac{8\cdot\pi\cdot\sqrt{2\cdot m_e^*}\cdot e}{3\cdot h}\cdot\frac{V_{\phi\kappa}^{*3/2}}{E^*}+\frac{\sqrt{8\cdot m_e^*\cdot e^3}}{3\cdot h\cdot\varepsilon_0}\cdot V_{\phi\kappa}^{*-1/2}} \quad (1).$$

Experiments show that the electric field /8/, the work function /8/,/9/, which is defined as the voltage V_{fk} , and the

effective electron mass /10/,/11/ changed due to a contamination of the cathode, but the roughness of the cathode surface effects only the electric field intensity. So the following substitutions must take place to describe exploatation condition of the contacts:

$$E^* = \beta \cdot E \quad \Leftarrow \quad \beta \geq 1 \tag{2},$$

$$V_{\phi\kappa}^* = \frac{V_{\phi\kappa}}{\upsilon} \quad \Leftarrow \quad \upsilon \geq 1 \tag{3},$$

$$m_e^* = \frac{m_e}{\mu} \quad \Leftarrow \quad \mu \geq 1 \tag{4}.$$

The collector film and the moleculas of the air gases in the very thin gap are considered as the contanimation over the cathode surface. Therefore the equation, describing the current density due to the cold emission from the cathode, overlayed with the collector film and being in the air, is:

$$j_E = \frac{e^2 \cdot \mu}{8 \cdot \pi \cdot h} \cdot \frac{\beta^2 \cdot E^2 \cdot \upsilon}{V_{\phi\kappa}} \cdot e^{-\frac{8\pi\cdot\sqrt{2\cdot m_e}\cdot e}{3\cdot h\cdot\sqrt{\mu}}\cdot\frac{1}{\beta\cdot E}\sqrt{\frac{V_{\phi\kappa}^3}{\upsilon^3}}+\frac{\sqrt{8\cdot m_e\cdot e^3}}{3\cdot h\cdot\varepsilon_0\cdot\sqrt{\mu}}\sqrt{\frac{\upsilon}{V_{\phi\kappa}}}} \tag{5}.$$

The current density is known in the most cases, so that the electric field intensity is calculated from Eq. (5) by some iterative method.

The commutator bar moves over the brush, so the thickness of the gap increases, as it is demonstrated in Fig. 2. Presuming the electric field is homogeneous the acceleration of the electrons in the gap is constant. The kinetic energy of the electron is /11/:

$$W_{ek} = \frac{m_e \cdot c^2}{\sqrt{1-\frac{v^2}{c^2}}} - m_e \cdot c^2 \tag{6}.$$

When the electron achieves such a velocity, that his kinetic energy is:

$$W_{ek} = \frac{W_{i1}}{N_A} \cdot \left(1 + \frac{m_e}{m_a}\right) \tag{7},$$

the ionization of the atoms in the gap begins. The energy W_{i1} is the first ionization energy of one mole of the gaseous element in the gap.

Two values of the electron velocity are derived from Eqs (6) and (7). The first one is the average value of the linear motion of the electron /2/, and the second one is the rootmeansquare value needed for the ionization when collision between the electron and the atom is not centric. The average value of the electron velocity is:

$$v_{e\_avg} = c \cdot \sqrt{1 - \frac{m_e \cdot c^2}{\frac{W_{i1}}{N_A} \cdot \left(1 + \frac{m_e}{m_a}\right) + m_e \cdot c^2}} \tag{8},$$

and the rootmeansquare value or, as it is also called, the effective value is:

$$v_{e\_rms} = c \cdot \sqrt{1 - \frac{m_e \cdot c^2}{2 \cdot \frac{W_{i1}}{N_A} \cdot \left(1 + \frac{m_e}{m_a}\right) + m_e \cdot c^2}} \tag{9}.$$

The motion of the electron is accelerated, so there is a constant force on the electron. This is the force of the electric field on the electron, and the vectors of the force and of the electric field are colinear:

$$F = e \cdot E \tag{10}.$$

This force is also the function of the electron mass and his acceleration /11/, and the vectors of the force and of the acceleration are colinear:

$$F = \frac{m_e}{\sqrt{\left(1 - \frac{v_{e\_rms}^2}{c^2}\right)^3}} \cdot \frac{dv}{dt} \tag{11}.$$

A path the electron must move over to get the sufficient velocity for the ionization of the atom is derived from Eqs (10) and (11). This path is:

$$s = \frac{m_e \cdot c^2}{e \cdot E}\left(\sqrt{1 + 2 \cdot \frac{W_{i1}}{N_A} \cdot \frac{1}{m_e \cdot c^2} \cdot \left(1 + \frac{m_e}{m_a}\right)} - 1\right) \tag{12}.$$

Because the electric field is homogeneous, the voltage over this path is equal to:

$$U = \frac{m_e \cdot c^2}{e}\left(\sqrt{1 + 2 \cdot \frac{W_{i1}}{N_A} \cdot \frac{1}{m_e \cdot c^2} \cdot \left(1 + \frac{m_e}{m_a}\right)} - 1\right) \tag{13}.$$

These two equations (12) and (13) are simplified according to the following rule of small numbers: $\sqrt{1+2\cdot\delta} \approx 1+\delta \Leftarrow \delta << 1$. So, the path and the corresponding voltage are:

$$s = \frac{W_{i1}}{e \cdot E \cdot N_A} \tag{14},$$

$$U = \frac{W_{i1}}{e \cdot N_A} \tag{15}.$$

These are the basic equations that determine the path of the electron flow and the voltage over this path, which is sufficient for the ionization. If the gap is shorter than this path the current flows due to tunnel effect. The ionization means the end of tunnel effect, and it is also the beginning of the formation of the drawn arc. Comparing the drawn and the discharging arc, the ionization is present at the formation of them both, but for the latter one, the overvolt-

age between the contact members and the breakdown of the gap medium are the cause of the ignition. In the case of the drawn arc, the current conduction smoothly turns from tunnel effect to arc conducting mode, when the ionization begins.

While the tunnel conduction has only one kind of the charge carriers, which are the electrons emitted from the cathode, the drawn arc conduction has the following charge carriers:

- the electrons passed from the cathode by the field emission;
- the electrons passed from the cathode by the thermionic emission at the higher value of the cathode temperature as with tunnel effect;
- the cathode and the anode ions, which resulted from the ionization of the free atoms of the cathode and the anode materials in the conducting volume of the gap.

When the thickness of the gap sufficiently increases the ionization begins, but not the ionization of the cathode and the anode atoms at the same time. If the first ionization energy of the cathode material is lower as the first ionization energy of the anode material the ionization of the cathode atoms takes place, while the anode atoms are still not ionized. Further increase in the gap thickness - Fig. 2, causes that the electrons get the higher kinetic energy, sufficient to ionize the free anode atoms. So, there are three layers within the arc illustrated in Fig. 3:

- the first one, where the kinetic energy of the electrons is not sufficient to ionize any free atoms in this layer; the free cathode and anode atoms only are present there, therefore this one is named ***the free atoms layer***;
- the second one, where, in the discussed case, the cathode atoms are ionized, but the anode atoms are still neutral; this layer is ***the partly ionized layer***;
- the third one, where all atoms are ionized is called ***the fully ionized layer***.

The free atoms layer is in literature /1/,/4/ defined as ***a cathode layer***, but only the cathode atoms and ions are taken into account with its definition. To distinguish between our arc model, which considers the cathode and the anode atoms and ions, and the other arc model from the literature, we define the arc layers in this special way. The difference between the free atoms layer and the cathode layer, as defined in the literature, occurs when the first ionization energy of the cathode material is higher than that of the anode material.

When the fully ionized layer is established the drawn arc ignites. The question arises about the length of the path through the fully ionized layer. It must be so large that the ions, while moving along this path, get the sufficient kinetic energy to heat the cathode to such amount that the cathode atoms pass from the cathode to the gap by vaporization or by sublimation, and that the thermionic emission of

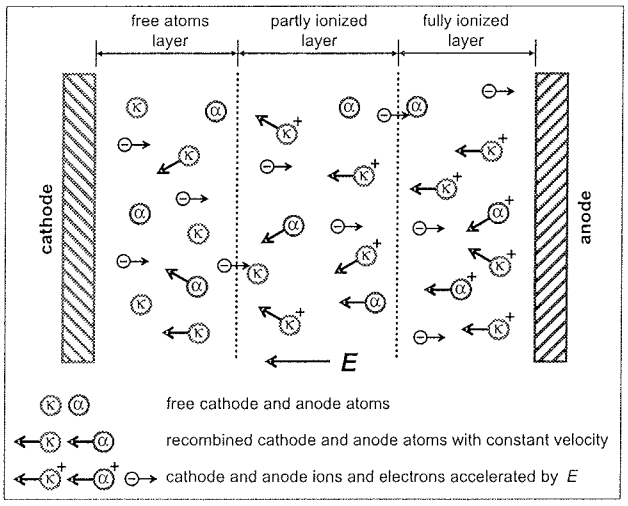

Fig. 3: The arc layers.

the electrons is established. Further on, travelling toward the cathode, they are recombined, and their collisions against the cathode are nonperpendicular. There must also be equilibrium of the charge carriers, so that the arc is neutral to the external medium.

The mathematical model of the drawn arc formation has the following presumptions:

- there is only the field emission with tunnel effect;
- the electric field intensity is constant while the current conduction passes from tunnel effect to arc conducting mode; the electric field is also homogeneous;
- the contact current is constant while the current conduction passes from tunnel effect to arc conducting mode;
- the motion of the electrons in the gap between the cathode and the anode is linear;
- the collisions of the particles are not centric, nor they are perpendicular;
- the ions are recombined before they collide against the cathode;
- the arc is externally neutral;
- the arc temperature is equal to the cathode temperature at the instant of the arc formation;
- the ratio between the number of the free cathode atoms and ions and the number of all free atoms and ions in the conducting volume is calculated as the cathode and the anode temperatures are equal;
- the external medium is air under the normal pressure, or is optionally vacuum;
- the total pressure of gases in the conducting volume between the cathode and the anode is equal to the pressure of the external medium, unless it is determined by the thermionic emission to be higher.

There are the cathode and the anode atoms in the gap, which are ionized by the collisions with the electrons. The

first ionization energy of the cathode atoms is not equal to the one of the anode atoms. Therefore the electrons that ionize the cathode atoms have the different average and effective values of the velocity than the electrons that ionize the anode atoms. The ratio between the number of the free cathode atoms and ions and the number of all free atoms and ions in the conducting volume must be determined to calculate the overall average velocity of the electrons. This ratio is according to the ideal gas law:

$$\eta_\kappa = \left.\frac{p_{v\kappa}(T_\kappa)}{p_{v\kappa}(T_\kappa)+p_{v\alpha}(T_\alpha)}\right|_{T_\alpha=T_\kappa} = \frac{p_{v\kappa}(T_\kappa)}{p_{v\kappa}(T_\kappa)+p_{v\alpha}(T_\kappa)} \quad (16).$$

In Eq. (16), there are the saturated vapour pressures of the cathode and the anode atoms and ions. They are determined according to the Clapeyron - Clausius equations /11/:

$$\frac{d\,p_{v\kappa}(T_\kappa)}{d\,T_\kappa} - \frac{L_{v\kappa}(T_\kappa)\cdot p_{v\kappa}(T_\kappa)}{R\cdot T_\kappa^2\cdot\left(1-\frac{V_{\mu l\kappa}}{V_{\mu v\kappa}}\right)} = 0 \quad (17),$$

$$\frac{d\,p_{v\alpha}(T_\kappa)}{d\,T_\kappa} - \frac{L_{v\alpha}(T_\kappa)\cdot p_{v\alpha}(T_\kappa)}{R\cdot T_\kappa^2\cdot\left(1-\frac{V_{\mu l\alpha}}{V_{\mu v\alpha}}\right)} = 0 \quad (18).$$

The L_{vk} and L_{va} are the values of the latent heat of vaporization of the cathode and the anode materials depended on the cathode temperature. Their functions are presented as the linear interpolated equations between the boiling and the critical temperatures:

$$L_{v\kappa}(T_\kappa) = L_{vb\kappa}\cdot\frac{T_{c\kappa}-T_\kappa}{T_{c\kappa}-T_{b\kappa}} \quad (19),$$

$$L_{v\alpha}(T_\kappa) = L_{vb\alpha}\cdot\frac{T_{c\alpha}-T_\kappa}{T_{c\alpha}-T_{b\alpha}} \quad (20).$$

The ratios between the volume of one mole of the material in liquid state and the one in gaseous state are neglected in Eqs (17) and (18) as $\frac{V_{\mu l\kappa}}{V_{\mu v\kappa}} \approx 0 \;\wedge\; \frac{V_{\mu l\alpha}}{V_{\mu v\alpha}} \approx 0$. So, the saturated vapour pressures for the cathode and the anode materials are:

$$p_{v\kappa}(T_\kappa) = p_{vb}\cdot e^{-\frac{L_{vb\kappa}}{R\cdot(T_{c\kappa}-T_{b\kappa})}\left(\frac{T_{c\kappa}}{T_\kappa}-\frac{T_{c\kappa}}{T_{b\kappa}}-\ln\frac{T_\kappa}{T_{b\kappa}}\right)} \quad (21),$$

$$p_{v\alpha}(T_\kappa) = p_{vb}\cdot e^{-\frac{L_{vb\alpha}}{R\cdot(T_{c\alpha}-T_{b\alpha})}\left(\frac{T_{c\alpha}}{T_\kappa}-\frac{T_{c\alpha}}{T_{b\alpha}}-\ln\frac{T_\kappa}{T_{b\alpha}}\right)} \quad (22),$$

where $p_{vb} = 101.325\ [\mathrm{kPa}]$ is the saturated vapour pressure of any material at the boiling temperature by the definition of the boiling point.

Presuming the current density is known, the density of the electrons is calculated:

$$n_e = \frac{j}{e\cdot\left(\eta_\kappa\cdot v_{e\kappa\_avg}+(1-\eta_\kappa)\cdot v_{e\alpha\_avg}\right)} \quad (23),$$

where the v_{ek_avg} and v_{ea_avg} are the average values of the velocities of the electrons that are to ionize the cathode and the anode atoms respectively. According to the ideal gas law we get the following equation:

$$p_{v\kappa}(T_\kappa)+p_{v\alpha}(T_\kappa) = \max\left(\frac{n_e}{\alpha\cdot N_A}\cdot R\cdot T_\kappa, p_{ext}\right) \quad (24).$$

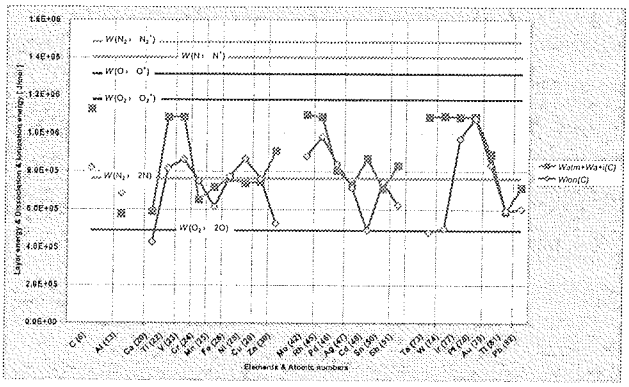

Fig. 4: The layer energy in comparison to the ionization and dissociation energy of nitrogen and oxygen.

Legend:

Watm+Wa+i(C) *layer energy of free atoms layer and partly ionized layer together - anode is carbon,*

Wion(C) *layer energy of fully ionized layer - anode is carbon,*

$W(N_2 \rightarrow N_2^+)$ *the first ionization energy of nitrogen molecules,*

$W(N \rightarrow N^+)$ *the first ionization energy of nitrogen atoms,*

$W(N_2 \rightarrow 2N)$ *dissociation energy of nitrogen molecules,*

$W(O_2 \rightarrow O_2^+)$ *the first ionization energy of oxygen molecules,*

$W(O \rightarrow O^+)$ *the first ionization energy of oxygen atoms,*

$W(O_2 \rightarrow 2O)$ *dissociation energy of oxygen molecules.*

The ionization coefficient α is less than 1 with the whole conducting volume of the gap. The cathode temperature is calculated from this Eq. (24) by some iterative method.

The pressure of the external medium is $p_{ext} = 101.325\ [\mathrm{kPa}]$ when it is air, but zero with vacuum.

The question is, why the external medium is so important. The external medium is air, so it contains the nitrogen molecules (78%) and the oxygen molecules (21%). If the saturated vapour pressure of the catode and the anode atoms

and ions together is less than the pressure of external medium the molecules of the external gas are also present in the gap, but their partial pressure is less than the external pressure. There are also the collisions between the electrons and the nitrogen and the oxygen molecules. This collisions are elastic, unless the kinetic energy of the electons is sufficient to ionize the nitrogen and the oxygen moleculas, or to dissociate them and further on, to ionize the gaseous atoms. Though the collisions are elastic, the velocity vector of the electrons changes by impacts, and cosequently the final kinetic energy of the elecrons changes. The sufficient kinetic energy of the electrons for full ionization is gained after they have moved along the path through some layer, so we define this energy to be the layer energy. According to Eq. (14) the layer energy is not depended on the particles, which are either the electrons or the ions. The layer energy of the free atoms layer and the partly ionized layer together and the layer energy of the fully ionized layer for several cathode materials, while the anode is carbon, are compared with the first ionization energy of the molecules, the dissociation energy and the first ionization energy of the atoms of nitrogen and of oxygen. The results are shown in Fig. 4. The dissociation energy of the nitrogen and the oxygen molecules is achieved with some cathode materials in the first two layers of the arc. But no ionization energy of the nitrogen and the oxygen particles is ever achieved. The elastic collisions and the dissociation of the nitrogen and the oxygen molecules waste the kinetic energy of the electrons, so that the total ionization of the cathode and the anode atoms is not attained in the fully ionized layer. To establish the arc, the cathode temperature is increasing, so that the total saturated vapour pressure of the cathode and the anode atoms and ions forces the nitrogen and the oxygen particles out of the conducting volume of the gap. Then the conditions for the arc formation exist.

The current density due to the thermionic emission is defined by the Richardson - Dushman equation /5/:

$$j_T = \frac{4\cdot\pi\cdot m_e\cdot e\cdot k^2}{h^3}\cdot T_\kappa{}^2\cdot e^{\frac{e}{k\cdot T_\kappa}\left(-\frac{V_{0\kappa}}{\upsilon}+\sqrt{\frac{e\cdot\beta\cdot E}{4\cdot\pi\cdot\varepsilon_0}}\right)} \quad (25).$$

The presumptions have the following effects on the total current density and on the crosssection of the conducting path between the cathode and the anode, that is the crosssection of the arc:

$$E = const \Rightarrow j = j_E + j_T \quad (26),$$

$$I = const \Rightarrow A_{arc} = A_{scl}\cdot\frac{j_E}{j_E + j_T} \quad (27).$$

The current density increases, but the cross-section constricts. A narrow ionized conducting channel, something similar as a pilot streamer at discharges /12/, arises. It is a hot flow of the electrons, the cathode and the anode ions and atoms. The absence of the ions of the air gases of the external medium is the main difference between the drawn and the discharge arcs. There is a loop in this procedure: Eq. (26) effects Eq. (23), but the algorithm converges.

The results of the temperature calculations for the electrodes, both of the same metal, are presented in Fig. 5. The comparison is carried out between the air medium and the vaccum, and further on, the cathode temperatures toward the melting and the boiling temperatures. The cathode temperatures are somehow between the melting and the boiling points, but there are some exceptions.

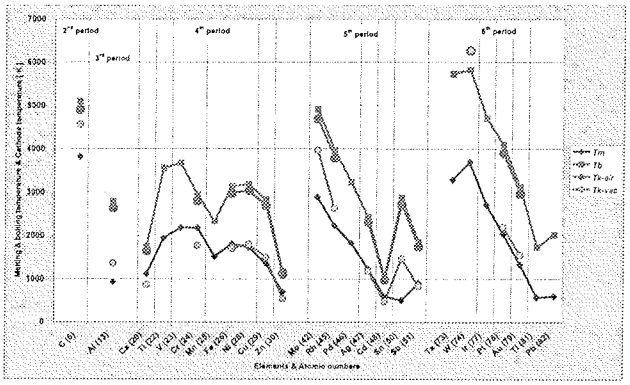

Fig. 5: The cathode temperatures, melting and boiling temperatures.

Legend:

Tm	*melting temperature,*
Tb	*boiling temperature,*
Tk-air	*cathode temperature in air,*
Tk-vac	*cathode temperature in vacuum.*

So far we presume that both, the cathode and the anode atoms and ions are present in the conducting volume of the gap. The number of the cathode atoms and ions N_{a+ik} and the number of the anode atoms and ions N_{a+ia} are natural numbers unequal to zero. But it could happen, especially with refractory materials, that either one of them is zero. It means, that it is possible with the great mathematical confidence, that the atoms and ions of one material are absent in the tiny conducting volume of the gap. The Dirac and Heaviside functions are introduced to include such cases into the mathematical model. The used Dirac function is symmetrical, but the Heaviside function is asymmetrical:

$$\begin{aligned} \mathcal{U}_+(x\le 0) &= 0 \\ \mathcal{U}_+(x>0) &= 1 \end{aligned} \quad (28).$$

While the electron moves along the sufficient path, it achieves the energy to ionize the cathode atom, which has the corresponding voltage drop, derived from Eq. (15), and equals to:

$$U_\kappa = \frac{W_{i1\kappa}}{e\cdot N_A}\cdot\mathcal{U}_+\left(N_{a+i\kappa}\right) \quad (29).$$

The corresponding voltage for the ionization of the anode atoms is:

$$U_{\alpha} = \frac{W_{i1\alpha}}{e \cdot N_A} \cdot \upsilon_{+}(N_{a+i\alpha}) \qquad (30).$$

The voltage drop of the free atoms layer is:

$$U_{atm} = \min_{U \neq 0}(U_{\kappa}, U_{\alpha}) = \\ = \frac{\min(W_{i1\kappa} \cdot (\delta(N_{a+i\kappa})+1), W_{i1\alpha} \cdot (\delta(N_{a+i\alpha})+1))}{e \cdot N_A} \qquad (31).$$

The voltage of the partly ionized layer is:

$$U_{a+i} = \max(U_{\kappa}, U_{\alpha}) - \min_{U \neq 0}(U_{\kappa}, U_{\alpha}) = \\ = \frac{\max(W_{i1\kappa} \cdot \upsilon_{+}(N_{a+i\kappa}), W_{i1\alpha} \cdot \upsilon_{+}(N_{a+i\alpha}))}{e \cdot N_A} - U_{atm} \qquad (32).$$

All atoms are ionized at the far end of the partly ionized layer, looking from the cathode. Then the full ionized layer begins. In this layer, the ions are accelerated toward the cathode by the electric field. But, when they leave this layer, they are recombined, because they are not immune to the collisions from the electrons. From this point on, the recombined atoms move toward the cathode uniformly with the constant velocity, hence there is no force on them due to the electric field, for they are neutral. The velocity of the ions is gained in the fully ionized layer, and the corresponding kinetic energy must be sufficient to heat the cathode to cause the vaporization or the sublimation of the cathode material, and to cause also the thermionic emission of the electrons. The average kinetic energy of the ion, either it is of the cathode or of anode material, is:

$$W_{ionk} = \frac{\eta_{\kappa} \cdot L_{v\kappa}}{N_A} + \frac{e \cdot V_{\phi\kappa}}{\upsilon} \qquad (33),$$

Because the energy of the work function is:

$$\phi_{\kappa} = e \cdot V_{\phi\kappa} \qquad (34)$$

the voltage drop of the full ionized layer, derived from Eq. (15), is:

$$U_{ion} = \frac{\eta_{\kappa} \cdot L_{v\kappa}}{e \cdot N_A} + \frac{\phi_{\kappa}}{e \cdot \upsilon} \qquad (35).$$

The infimum arc voltage is the sum of the layers voltages - Eqs (31), (32) and (35), and it is:

$$U_m = U_{atm} + U_{a+i} + U_{ion} = \\ = \frac{\max(W_{i1\kappa} \cdot \upsilon_{+}(N_{a+i\kappa}), W_{i1\alpha} \cdot \upsilon_{+}(N_{a+i\alpha}))}{e \cdot N_A} + \\ + \frac{\eta_{\kappa} \cdot L_{v\kappa}}{e \cdot N_A} + \frac{\phi_{\kappa}}{e \cdot \upsilon} \qquad (36).$$

There is one parameter in the calculation of the cathode temperature - Eq. (24), which has not been fully defined. It is the ionization coefficient of the whole conducting volume. The volume occupied only by the ions is the volume of the fully ionized layer. There are some ions also in the partly ionized layer, but we neglect them when estimating the ionization coefficient. The density of the ions and atoms together is constant throughout the whole conducting volume, so the coefficient is the ratio of the volume of the fully ionized layer and the whole conducting volume. Presuming the crosssection area is uniform the coefficient is the ratio of the thickness of the fully ionized layer and the arc path. Because the electric field is homogeneous the ionization coefficient becomes:

$$\alpha = \frac{U_{ion}}{U_m} \qquad (37).$$

So, this equation leads to another loop in the mathematical model - Eq. (24), but the convergence still exists.

The results of this mathematical model are shown in Fig. 6. The infimum arc voltage directly depends on the energy of the first ionization of the cathode and the anode material, on the latent heat of vaporization of the cathode material, and on the energy of the work function of the cathode. These quantities are the properties of the contact materials. But, this voltage also depends on the cathode temperature indirectly through the ratio between the number of the free cathode atoms and ions and the number of all free atoms and ions. The whole model is recalculated at the contact current I = 1 A, at the crosssection of the conducting path A_{scl} = 5×10 ^{6} m^2, and the coefficients b, u and μ being unit.

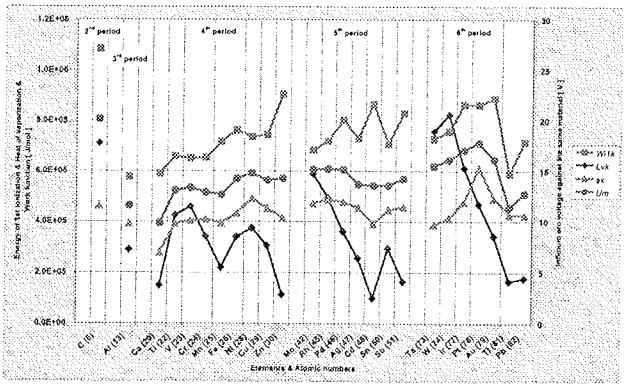

Fig. 6: The infimum arc voltage with its influential quantities depended on the cathode material against the anode of the same material.

Legend:

Wi1k	*energy of 1st ionization of cathode material,*
Lvk	*latent heat of vaporization of cathode material,*
ϕk	*energy of work function,*
Um	*infimum arc voltage.*

It has to be emphasized that the cathode temperature depends mainly on the latent heat of vaporization of the cathode and the anode material, their boiling and critical temperatures, and the external pressure.

3. The comparison of the results

The infimum arc voltage is determined not only by the cathode material, but also by the anode material. The diagrams in Fig. 7 show the infimum arc voltage depended on the cathode material when facing the anode made by the same material, and the one of tungsten and of carbon. The next diagrams in Fig. 8 present the comparison of the infimum arc voltage achieved by our model and the values of the minimal arc voltages according to Holm, Fink and Gaulrapp /1/, which are considered as experimental values. But, as stated in the literature /1/ and presented in Fig. 8, several researchers got very different results of their experimental determination of the minimal arc voltage, although they are determined by the contact electrodes of the same material. These authors considered that minimal arc voltage is essentially determined only by the cathode material, nevertheless the contact electrodes are made of the different material. That is the significant difference from our model.

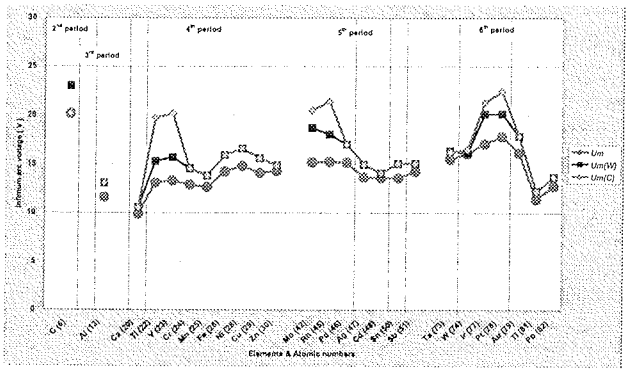

Fig. 7: The comparison of the infimum arc voltage of several combinations of materials.

Legend:
Um *infimum arc voltage with cathode and anode of the same material,*
Um(W) *infimum arc voltage with anode of tungsten,*
Um(C) *infimum arc voltage with anode of carbon.*

Some researcher of the commutation phenomenon /2/,/3/ discovered by their experiments, that there was practically no difference in the infimum arc voltage whether the cathode was made of carbon and the anode of copper, or just the opposite, the cathode was of copper and the anode of carbon. And their observations are confirmed by the model: the cathode against the anode C-Cu 12.5 V, Cu-C 15.6 V by the model, C-Cu or Cu-C from 14 V to 20 V by their measurements /2/, and C-Cu 20 V and Cu-C 13 V by Holm /1/, and further on, the cathode temperature 2835 K by the model and up to 2273 K by their estimation of the experiment /2/.

The comparison between the model results and the experimental results by several researchers /1/ is illustrated in Fig. 8. Having in mind uncertainties of the experimental results, and the fact that the results of the model are presented without any contamination of the electrodes and with no roughness of the contact surfaces, the results are estimated as very good and useful.

4. Conclusions

The evaluation of affinity of the contact materials to form the drawn electric arc carried out by defining the infimum arc voltage for several combination of the contact materials is only one aspect of determining the proper contact materials. The second parameter to be taken into account is the cathode temperature, which is also obtainable by this model, especially, when reducing it under the calculated value by heat transfer to the external medium, and so avoiding the arc.

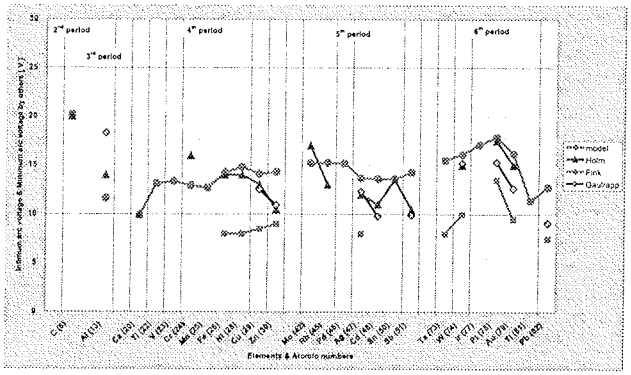

Fig. 8: The comparison of the infimum arc voltage and minimal arc voltage with the electrodes of the same material according to several researchers /1/.

Legend:
model infimum arc voltage by our model,
Holm minimal arc voltage by Holm /1/,
Fink minimal arc voltage by Fink /1/,
Gaulrapp minimal arc voltage by Gaulrapp /1/.

There are many mechanical properties, for instance elasticity, plasticity and hardness and the frictional wear of the materials and the electric properties as it is the contact and the bulk resistance, which must be considered when determining the contact materials for an application. Nevertheless, this model is a good mathematical tool to determine the contact material from the viewpoint of the drawn arc formation. The model is applicable to the switching contacts, and these conclusions are also valid for them.

5. Used symbols

α coefficient of ionization
β enhancement factor of electric field intensity
δ Dirac function
υ decreasing factor of work function
η_k ratio between number of free cathode atoms and ions and number of all free atoms and ions
ϕ_k work function energy in vacuum
ε_0 dielectric constant in vacuum
μ factor between rest and effective electron mass
A_{arc} cross-section of arc
A_{scl} cross-section of path of current conducting by t unnel effect
c light velocity in vacuum
e elementary charge
E electric field intensity
E^* enhanced electric field intensity
e^x exponential function
F force
h Planck constant
I contact current
j contact current density
j_E current density due to cold emission
j_T current density due to thermionic emission
k Boltzmann constant
L_{vk} molar latent heat of vaporization of cathode material
$L_{v\alpha}$ molar latent heat of vaporization of anode material
L_{vbk} molar latent heat of vaporization of cathode material at boiling temperature
$L_{vb\alpha}$ molar latent heat of vaporization of anode material at boiling temperature
m_a rest atom mass
m_e rest electron mass
m_e^* effektive electron mass
N_A Avogadro number
N_{a+ik} number of free cathode atoms and ions
$N_{a+i\alpha}$ number of free anode atoms and ions
n_e electron density
p_{vk} saturated vapour pressure of cathode atoms and ions
$p_{v\alpha}$ saturated vapour pressure of anode atoms and ions
p_{vb} saturated vapour pressure of boiling point
R general gaseous constant
s path through layer
T_k cathode temperatrure
T_{bk} cathode boiling temperature
$T_{b\alpha}$ anode boiling temperature
T_{ck} cathode critical temperature
$T_{c\alpha}$ anode critical temperature
U layer voltage
U_{a+i} partly ionized layer voltage
U_{atm} free atoms layer voltage
U_{ion} fully ionized layer voltage
U_m infimum arc voltage
v_+ asymmetrical Heaviside unit function
v particle velocity
v_{e_avg} average electron velocity
v_{ek_avg} average electron velocity up to ionization of cathode atom
$v_{e\alpha\_avg}$ average electron velocity up to ionization of anode atom
v_{e_rms} effective (root-mean-squere) electron velocity
$V_{\phi k}$ work function voltage
$V_{\phi k}^*$ decreaced work function voltage
$V_{\mu l\alpha}$ mole volume of anode material in liquid state
$V_{\mu lk}$ molar volume of cathode material in liquid state
$V_{\mu v\alpha}$ molar volume of anode material in vapour state
$V_{\mu vk}$ molar volume of cathode material in vapour state
W_{ek} electron kinetic energy
W_{i1} molar energy of 1st ionization
W_{i1k} molar energy of 1st ionization of cathode atoms
W_{i1a} molar energy of 1st ionization of anode atoms
W_{ionk} average ion kinetic energy

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APLIKACIJSKI ČLANEK
APPLICATION ARTICLE

Nove tehnologije in ergonomija v beli tehniki
New Technologies and Ergonomics in White Goods

Konrad Steblovnik, GORENJE POINT, Velenje, Slovenija

Predgovor h prevodu članka

Ko smo konec julija 2004 prejeli obvestilo, da so sprejeli objavo članka z zgornjim naslovom na redni letni konferenci IATC (www.iatc.com) v Chicagu, pravzaprav nismo bili preveč presenečeni. Naš namen je bil predstaviti nove tehnologije pri upravljanju aparatov, s katerimi smo se pričeli v Gorenju ukvarjati že pred štirimi leti in, ki so zasnovane na povsem novih pristopih implementacije uporabniško prijaznega upravljanja s pomočjo grafičnih LCD prikazovalnikov, občutljivih na dotik za gospodinjske stroje. IATC je ameriška konferenca, ki predstavlja predvsem nove tehnologije in komponente za področje bele tehnike, zaradi tega je bila seveda predstavitev naših rešitev za njih zelo zanimiva. Moramo poudariti, da je predavanje, ki smo ga imeli v okviru te konference poželo veliko zanimanje in tudi demonstracija upravljanja PG5 je vzbudila veliko pozornost.

S člankom smo želeli predstaviti predvsem, kot že sam naslov pove, kaj lahko obvladovanje najnaprednejše elektronske tehnologije in komponent doprinese k oblikovanju gospodinjskih strojev z naprednimi rešitvami in uporabniško prijaznim upravljanjem. V članku pa se nismo ukvarjali z ergonomijo samo, ampak predvsem s tem, kakšna mora biti zgradba programske in strojne opreme naprednih elektronskih sklopov, da lahko dosežemo zastavljene cilje. Poudariti moramo, da danes v Gorenju v celoti obvladujemo načrtovanje takšnih in podobnih naprednih elektronskih sistemov, kar nam omogoča, da postaja Gorenje prvo, in najbolj napredno na tem področju in sicer z lastnim znanjem (!), kar pomeni seveda, da nam ni potrebno deliti naših idej z zunanjimi partnerji.

Pot, ki jo je Gorenje "ubralo" na tem področju, je zagotovo prava, kar dokazujejo že tri nagrade, ki so jo Gorenjski oblikovalci prejeli za aparate, v katere vgrajujemo sklope, ki so zasnovani na tej tehnologiji. Članek je bil napisan štiri mesece prej, kot pa smo bili obveščeni o prvi prejeti nagradi. Napisali smo ga septembra 2004.

Povzetek članka

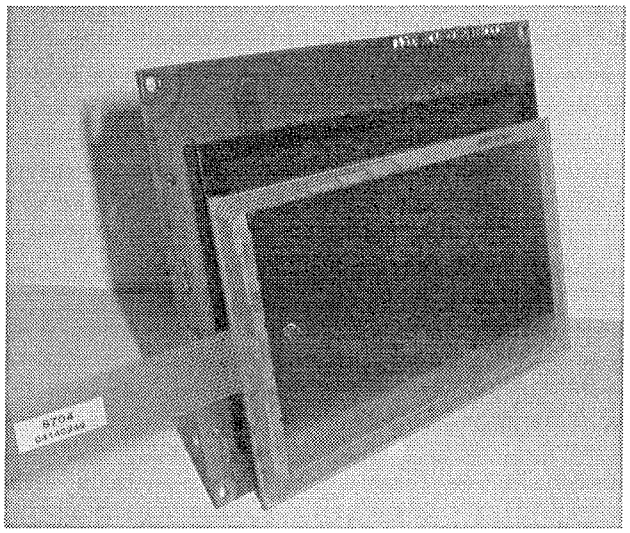
Namen tega članka je, da predstavimo razvoj uporabniškega vmesnika za aparate bele tehnike, ki smo iz ga izvedli z grafičnim prikazovalnikom tipa LCD in z vgrajeno enoto, ki je občutljiva na dotik. Ta vrsta vhodno izhodne naprave nudi pomembno fleksibilnost pri načrtovanju uporabniško prijaznih grafičnih vhodno izhodnih vmesnikov za aparate. Razvili smo dinamične in moderne uporabniške vmesnike, ki so zasnovani na menujskih principih, za nove generacije naprav najvišjega razreda - pralne stroje, sušilce, hladilnike, zamrzovalnike in pečice. Ta naprava ima primerno ceno in omogoča implementacijo velikega števila dodatnih in uporabnih funkcij za ciljne naprave. Tega standardne elektromehanske rešitve ne omogočajo. V članku opisujemo osnovne tehnološke rešitve za načrtovanje ergonomskega uporabniškega vmesnika. Ne ukvarjamo pa se s samo ergonomijo. Predstavili bomo tudi določene izkušnje pri načrtovanju aplikacij s takšno komponento na področju bele tehnike. Za optimalno implementacijo smo uporabili hitri 16-bitni mikrokontroler. Zaradi zahtevne izvedbe smo moralo posebno pozornost nameniti elektromagnetnim interferenčnim problemom.

V okviru projekta smo morali razviti popolnoma nov LCD prikazovalnik, ki je prirejen našim zahtevam in ima resolucijo 240X128 grafičnih točk.

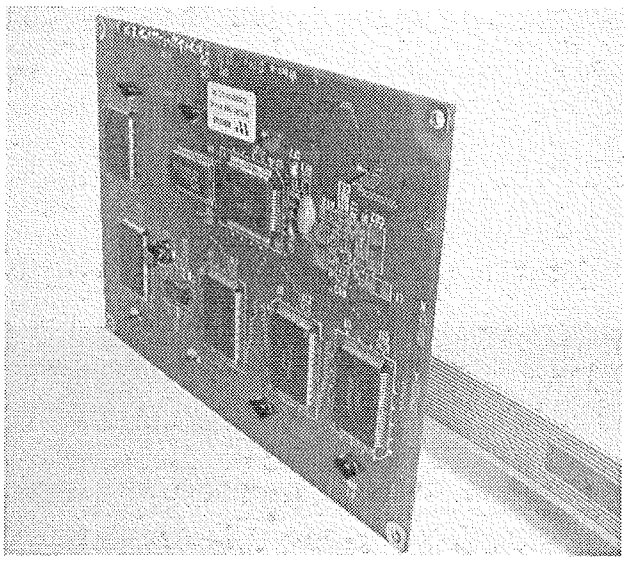
Izhodišča

Področje velikih gospodinjskih strojev tvorijo tri glavne skupine aparatov: kuhalni aparati, pralno pomivalni stroji in hladilno-zamrzovalni stroji. Za vsako izmed teh moramo imeti posebni pristop do oblikovanja. Preučili smo, kako se moramo lotiti razvoja novih uporabniških vmesnikov, ki bi bili zasnovani na novih tehnoloških rešitvah, pa bi še vedno zagotavljala dovolj enostavno upravljanje aparata, primerno za različne tipe uporabnikov: tradicionalnih in modernih vrst. Pod izrazom nove tehnologije imamo v mislih elektronske sklope za kontrolo ciljnih aparatov s pomočjo modernih vrst komponent: mikrokontrolerji z vgrajenimi programskimi pomnilniki tipa "flash", grafičnimi prikazovalniki vrste LCD, različnimi vrstami senzorjev, triaci, stikalnimi napajalniki, itd. Odločili smo se za implementacijo dodelanega GUI (Graphic User Interface - grafični uporabniški vmesnik) s pomočjo grafičnega LCD vmesnika, občutljivega na dotik, kot vhodno-izhodne enote. Prepričani smo, da ponuja takšen pristop najboljše rešitve, ne samo za uporabnika, pač pa lahko s posebnimi dodatnimi razvojnimi orodji optimiramo ciljni aparat že v fazi razvoja. Opisali bomo pred-

nosti uporabe takšnega grafičnega LCD prikazovalnika kot vhodno-izhodne naprave gospodinjskega stroja. Celotna ideja izvira v razvojno/raziskovalnem projektu, ki je bil sprožen pred tremi leti (v času nastanka tega prevoda so to že štiri leta, op. avtorja), kjer je bil vključen razvoj demonstracijski aparatov, zasnovanih na LCD prikazovalnikih za vse tri omenjene skupine bele tehnike: KA, HZA in PPA. Rezultate projekta smo predstavili na največjem evropskem sejmu bele tehnike HOMETECH 2002 v Berlinu. Zelo dober odziv na tem sejmu nas je opogumil, da smo nadaljevali z razvojem na grafičnih LCD prikazovalnikih, občutljivih na dotik za belo tehniko. Dejansko LCD prikazovalnik ni nova komponenta na področju bele tehnike, vsekakor pa LCD, občutljiv na dotik to je.



Pogled od spredaj: *LCD prikazovalnik z ločeno enoto, ki je občutljiva na dotik*



Pogled od zadaj: *LCD krmilnik in gonilniki.*

Slika 1: Standardni LCD prikazovalnik z ločeno ploščo, ki je občutljiva na dotik.

Danes lahko z gotovostjo trdimo, da smo napravili uspešen prvi korak in smo plasirali na trg prvi pralni stroj z vgrajenim LCD prikazovalnikom, ki ima vgrajeno enoto, ki je občutljiva na dotik. Kmalu mu bodo sledili še drugi aparati (dejansko je Gorenje po objavi članka dalo na trg še hladilno-zamrzovalne aparate z vgrajenim LCD prikazovalnikom te vrste, pripravljamo pa še pečice, op. avtorja).

Pri izdelavi demostracijskega sistema, smo uporabili standardni LCD prikazovalnik z zunanjo enoto, občutljivo na dotik, ki jo vidimo na sliki 1. in ima naslednje lastnosti:

- 114mm X 64mm vidno področje,
- 240 X 128 grafičnih točk,
- standardni grafični krmilnik z dodatnimi LCD gonilniki,
- 8 bitni paralelni vmesnik,
- ločena digitalna enota, občutljiva na dotik,
- LED osvetlitev v beli barvi.

Na sliki 1 vidimo, da sta LCD zaslon in enota, občutljiva na dotik ločena med sabo, poleg tega vidimo na spodnji sliki veliko količino integriranih vezij, ki jih ta rešitev potrebuje za krmiljenje zaslona. Mehanske dimenzije 143mm X 103mm X 12mm so prevelike.

Na omenjenem demonstracijskem sistemu smo za krmiljenje sistema uporabili osem-bitni mikrokontroler.

V članku bomo opisali predvsem izkušnje, ki smo jih pridobili pri raziskavi in razvoju krmilne enote te vrste. Ne bomo se ukvarjali s samo ergonomijo, pač bomo razpravljali o novih tehnoloških rešitvah ter različnih možnostih, ki jih ponuja takšen pristop pri razvoju uporabniških vmesnikov nove vrste. Vodilo vseh teh aktivnosti je bilo v glavnem naslednje: *"Kako razviti gospodinjski stroj, ki bo služil uporabniku na najboljši možni način, kot to pričakuje, da pa lahko še vedno uporabimo moderno in napredno tehnologijo, ki pa ne bo uporabniku v oviro pač pa v pomoč?"* Članek opisuje nekatere pristope in omejitve pri načrtovanju novih tehnologij za to področje, hkrati pa poizkuša osvetliti, kako pomembna je izbira ustrezne tehnologije, da lahko še vedno načrtujemo ergonomske uporabniške vmesnike brez omejitev.

Opis integriranega lcd zaslona, občutljivega na dotik

Naše delo smo nadaljevali na osnovi izkušenj, ki smo jih pridobili pri razvoju demonstracijskega sistema.

Standardna rešitev, ki je opisana v prvem poglavju ima nekaj šibkih točk in pomanjkljivosti:

- necelovita izvedba,
- prevelike mehanske dimenzije,
- preveč polprevodniških elementov,
- visoka cena.

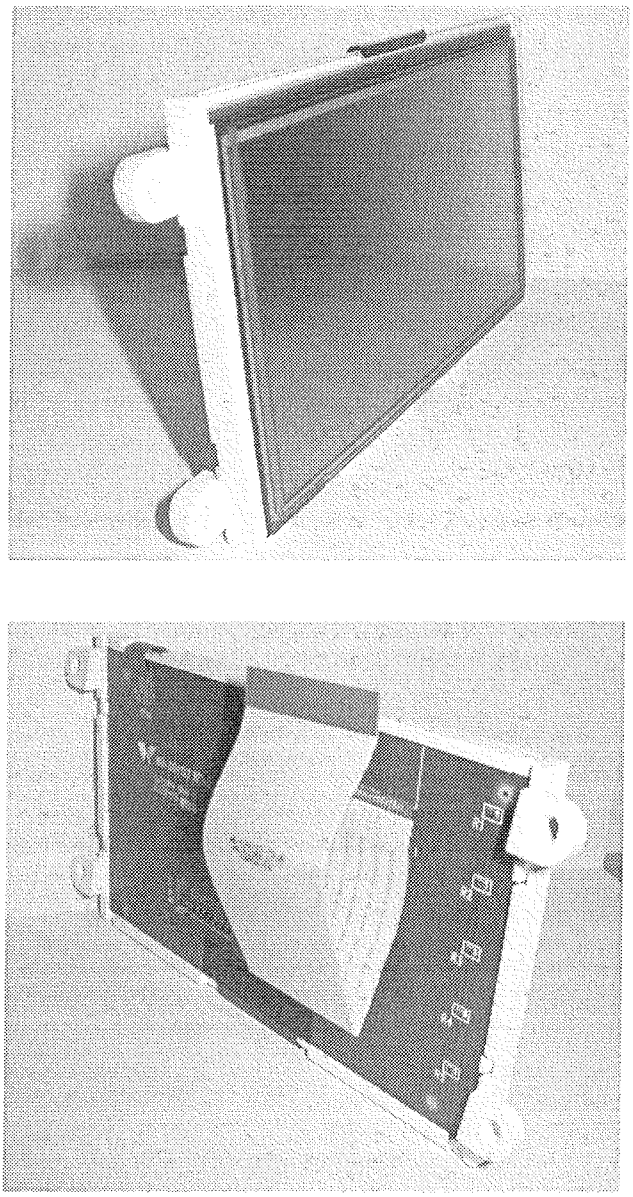
Prvi korak po uspešni marketinški predstavitvi novega pristopa je bil namenjen temu, da definiramo, oblikujemo in razvijemo LCD prikazovalnik, z integrirano enoto, občutljivo na dotik, ki bo ustrezal našim zahtevam. Postavili smo naslednje osnovne zahteve:

- Komponenta mora biti celovita in v enem kosu, za katero določa njene zunanje dimenzije aparat, v katerega ga bomo vgradili.
- Komponenta mora biti primerna za vse tri programe PPA, HZA in KA. (Tu se je kasneje v fazi razvoja pokazalo, da imajo posamezni programi tako veliko posebnosti, da ni bilo mogoče v celoti poenotiti prikazovalnika).
- Osnovna barva prikazovalnika je modra na beli podlagi.
- Dimenzije vidnega področja določa naprava.
- Enota, občutljiva na dotik mora biti analogna, da lahko dinamično oblikujemo tipke za vnos.
- Mehanske omejitve za vgradnjo prikazovalnika v aparat narekujejo zelo celovito obliko v enem kosu. Zaradi tega smo morali poiskati rešitev za polprevodniške krmilne elemente v enem kosu z veliko stopnjo integracije. Najnovejša polprevodniška tehnologija to omogoča.
- Zelo pomembni parameter za izbiro je bilo temperaturno območje, ki je v osnovi različno za vse tri programe.
- LCD prikazovalnik mora ustrezati naslednjim osnovnim zahtevam za ergonomski grafični uporabniški vmesnik:
  - resolucija grafike 128X240 grafičnih točk,
  - dinamično določljive tipke za vnos,
  - hitri grafični prikazovalnik in krmilnik, ki ne bo povzročal neprijetni vidnih učinkov pri osveževanju slike na zaslonu.

Zaradi vseh zgornjih zahtev, je hitro postalo očitno, da standardne rešitve ne bomo mogli uporabiti. Zaradi tega smo se odločili za razvoj prikazovalnika, ki je prirejen našim zahtevam. To tehnologijo najbolj obvladujejo na daljnem vzhodu, zaradi tega smo tudi sami iskali partnerja na Tajvanu in se po primerjalnih analizah odločili za proizvajalca Wintek. Sliko novega LCD prikazovalnika z vgrajeno enoto, občutljivo na dotik, ki smo ga razvili skupaj z njimi, lahko vidimo na sliki 2. Električne in mehanske lastnosti v celoti ustrezajo našim zahtevam, tudi cena je primerna.

Prikazovalnik ima naslednje lastnosti:

- Posebni okvir s primernimi mehanskimi dimenzijami: 135mm X 80mm X 6mm.
- Analogna enota, občutljiva na dotik je del prikazovalnika in je vgrajena.
- Grafični krmilnik in LCD gonilniki so integrirani v eno komponento - t.i. enočipna rešitev.



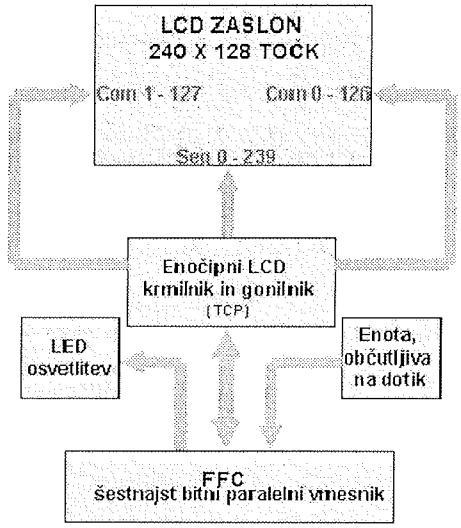
Slika 2. LCD prikazovalnik, prirejen našim zahtevam.

- LCD prikazovalnik je povezan z gibljivo kabelsko povezavo na glavno upravljalno elektronsko ploščo. Vmesnik je šestnajst bitni.
- LCD tehnologija je vrste STN blue.
- Resolucija slike je usklajena z zahtevami: 240X128 grafičnih točk.
- LED osvetlitev je integrirana in bele barve.
- Kot gledanja je 12 urni ali 6 urni.

Slika 3 prikazuje zgradbo strojne opreme prikazovalnika.

Brez opisa samega LCD polprevodniškega krmilnika in gonilnika je zgradba prikazovalnika dokaj enostavna in ne zahteva posebne razlage. Sestavlja ga LCD steklo - LCD prikazovalna plošča z dodano enoto, občutljivo na dotik, vgrajeni grafični krmilnik in LCD gonilniki, LED osvetlitev in gibljivi povezovalni kabel tipa FFC, ki predstavlja šestnajst

bitni podatkovni vmesnik. Imenujemo ga lahko visoko integrirani LCD prikazovalnik, z vgrajenimi komponentami. Ni naš namen, da bi na tem mestu opisovali tehnologijo LCD prikazovanja.



Slika 3: Zgradba LCD prikazovalnika.

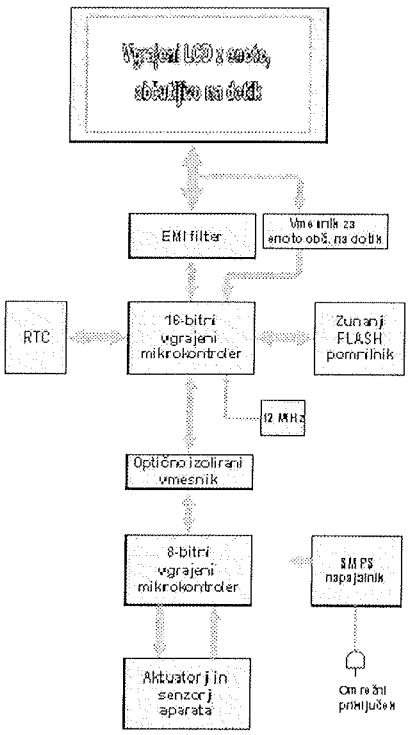
Vse opisane lastnosti LCD zaslona pomembno vplivajo na načrtovanje ergonomskih lastnosti ciljnega sistema.

Implementacija strojne opreme – elektronski sklop za upravljanje aparata

Vzporedno z načrtovanjem in razvojem LCD prikazovalnika je potekal tudi razvoj samih elektronskih sklopov za upravljanje aparatov. V opisu, ki sledi, bomo povzeli pristop k načrtovanju strojne opreme elektronskega sklopa za aparate in hkrati poudarili nekatere vidike načrtovanja strojne opreme, ki vplivajo na to, da bomo lahko oblikovali ergonomski upravljalni vmesnik. Obstaja seveda veliko število posebnih lastnosti, ki vplivajo na načrtovanje posameznih aparatov. Pri načrtovanju strojne opreme pa smo imeli vedno v mislih omenjeni ergonomski vidik. Deloma bomo pokazali, kako so nekateri detajli pri tem delu pomembni, kadar imamo v mislih ergonomijo ciljnega sistema. Na sliki 4 smo prikazali zgradbo strojne opreme ciljnega elektronskega sklopa. Načelna zgradba strojne opreme je zelo podobna za različne aparate tega razreda PPA, HZA in KA programov.

Glavni šestnajst bitni mikrokontroler z zunanjim pomnilnikom štiri do osem megabitnim pomnilnikom tipa "flash" deluje kot krmilnik LCD prikazovalnika in procesira vse funkcionalnosti grafičnega uporabniškega vmesnika, ki so vgrajeni za ciljni aparat. V poglavju 5 bomo opisali tri osnovne vrste takšnega uporabniškega vmesnika. Krmilni mikrokontroler je povezan na LCD prikazovalnik preko šestnajst bitnega vodila. LCD prikazovalnik krmilimo torej preko dovolj hitrega šestnajst bitnega vodila. Zaradi relativno dolgega gibljivega povezovalnega kabla smo morali vgraditi posebne elemente, ki zmanjšujejo elektromagnetne medsebojne vplive med krmilnikom in okolico.

Vmesnik za enoto, občutljivo na dotik uporablja isti paralelni vmesnik kot LCD. Notranji oscilator z zunanjim kristalom smo uporabili za generiranje sistemske ure. Frekvenca sistemskega vodila je 50 MHz. Dodali smo še zunanjo uro realnega časa, s pomočjo katere generiramo sistemsko uro. Poleg šestnajst bitnega mikrokontrolerja smo vgradili še osem bitni mikrokontroler, ki neposredno krmili vse aktuatorje in senzorje ciljnega aparata. Ta mikrokontroler krmili naprave aparata neposredno in je zaradi tega neposredno povezan na omrežje. Posledično to pomeni, da smo morali zagotoviti galvansko ločitev med LCD upravljalno enoto in osem bitnim krmilnim sistemom.



Slika 4: Zgradba strojne opreme.

Da smo lahko vpeljali ergonomske lastnosti v sistem, smo morali pri načrtovanju strojne opreme sistema torej upoštevati naslednja pravila:

- Uporabiti smo morali šestnajst bitni mikrokontroler za krmiljenje grafičnega uporabniškega vmesnika in LCD zaslona. Procesna moč tega mikrokontrolerja je celo 25 MIPS, kar je dovolj dobro, da lahko osvežujemo zaslon brez stranskih učinkov utripanja in izvajamo celo animacije za dodatno izboljšavo uporabniško prijaznih lastnosti sistema. *Uporabili smo torej optimalno procesno moč sistema za optimalno izvedbo uporabniško prijaznega grafičnega vmesnika za upravljanje aparata.*

- Paralelni vmesnik med šestnajst-bitnim mikrokontrolerjem in krmilnikom LCD prikazovalnika je šestnajst bitni. *S tem smo dosegli največjo možno hitrost prenosa podatkov do LCD.*
- Notranje vodilo mikrokontrolerja deluje s hitrostjo 50 MHz, kar zagotavlja dovolj veliko procesno moč sistema.
- Programski pomnilnik je štiri do osem megabitni. S tem imamo na razpolago dovolj velik prostor za kompleksne tekstovno orientirane upravljalne menuje za vse evropske jezike (za evropski trg je vgrajenih celo do 34 jezikov). Vsi teksti, ikone, slike ter animacije so neposredno dosegljive, kar omogoča hitri odziv informacij na zaslonu brez zakasnitev in utripanja.

Vse naštete lastnosti so zelo pomembne in nam dovoljujejo načrtovanje kakršnegakoli grafičnega uporabniškega vmesnika brez omejitev v izbrani resoluciji. Uporabnik ne vidi nobenih stranskih učinkov pri prikazovanju informacij na zaslonu.

Implementacija programske opreme

Programska oprema tega sistema je seveda ustrezna strojni opremi in sami aplikaciji. Ravno tako, kot smo strojno opremo sestavili iz dveh glavnih mikrokontrolerjev - šestnajst bitnega za upravljanje z grafičnim upravljalnim vmesnikom ter osem bitnega za krmiljenje aparata, smo tudi programsko opremo sestavili iz dveh ločenih procesnih oziroma operacijskih sistemov, ki sodelujeta preko serijske ožičene povezave in s primernim komunikacijskim protokolom. Dejansko smo uporabili zaporedje ukazov in statusnih odgovorov za komunikacijo med obema sistemoma. V resnici deluje procesor, ki krmili aparat kot podrejeni procesor. Vgrajeni je še tretji mikrokontroler, ki krmili posebno elektroniko za pogon motorja. Tega dela nimamo namena opisovati.

Zgradbo programske opreme prikazuje slika 5.

Organizacijo programske opreme lahko opišemo na osnovi plastne zgradbe. Glavna dela obeh sistemov podsistemov sta dva operacijska sistema. En del teče na šestnajst bitnem mikrokontrolerju in je namenjen za upravljanje celotnega sistema kot realno časovni operacijski sistem, drugi del pa teče na osem bitnem mikrokontrolerju in deluje kot jedro sistema za krmiljenje aparata.

Takšna plastna zgradba programske opreme prinaša potrebno fleksibilnost pri vzdrževanju sistema in nadaljnjem razvoju. Implementirali smo posebno plast, ki se imenuje grafični uporabniški vmesnik aparata (Appliance GUI), ki upravlja LCD zaslon kot menujsko orientirani uporabniški vmesnik. Takšna zgradba tudi doprinese dejstvu, da dosežemo veliko fleksibilnost pri načrtovanju ergonomskih uporabniških vmesnikov. Spremenimo lahko praktično samo en del programske opreme in lahko dejansko dobimo popolnoma novi uporabniški vmesnik. Preostali del programske opreme in celotna strojna oprema ostaneta dejansko nespremenjena in dobimo lahko praktično novi aparat. *Ergonomijo aparata lahko izboljšamo dejansko že med koriščenjem naprave. Izboljšave lahko praktično opravimo glede na odziv s trga.*

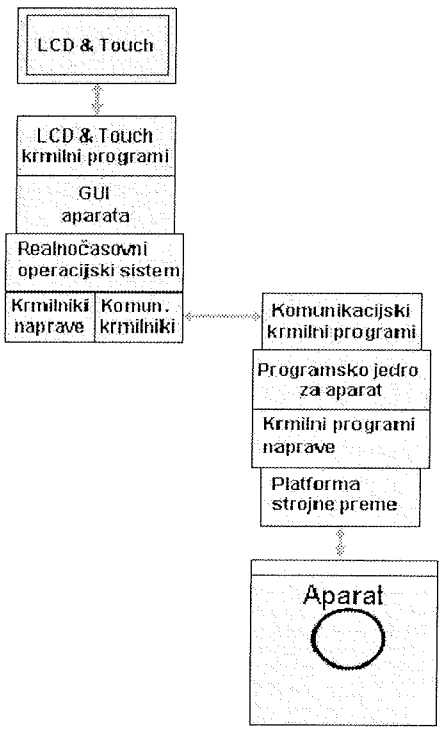


Figure 5: Zgradba programske opreme.

Opis grafičnega uporabniškega vmesnika

Na kratko bomo opisali tri različne pristope za načrtovanje grafičnega vmesnika te vrste za tri različne ciljne aparate:

- PPA (pralni stroj in sušilnik perila),
- HZA (hladilnik, zamrzovalnik in kombi),
- KA (pečica, kuhalnik).

Sledijo tri različne vrste menujev:

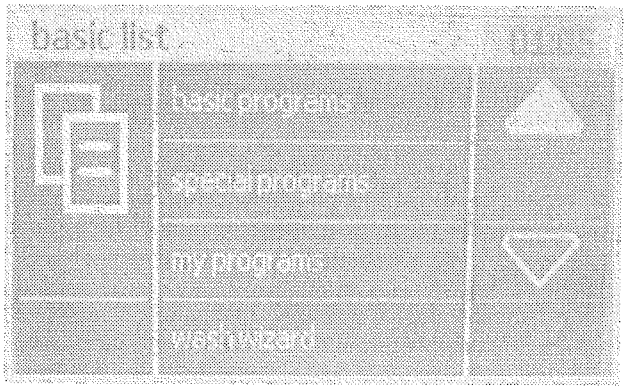
- Tekstovno orientirani grafični uporabniški vmesnik za PPA,
- Vmesnik, zgrajen na osnovi ikon za HZA,
- Mešani tip za KA.

Tekstovno orientirani grafični uporabniški vmesnik

Prvi primer prikazuje tekstovno orientirani grafični vmesnik na sliki 6, ki prikazuje osnovni menu za pralni stroj. Izberemo lahko:

- Osnovni programi
- Moji programi
- Čarovnik pranja
- Orodja.

Menuji so lahko seveda v različnih jezikih, kot na primer na sliki 6 je menu v angleščini. Funkcije aparata lahko izberemo s pritiskom na polje, ki vsebuje ustrezni tekst. Na desni strani sta tipki za izbiro dodatnih funkcij.



Slika 6: Menujsko orientirani GUI

Dejansko nimamo namena opisovati sistema upravljanja pralnega stroja. Navajamo pa samo nekaj osnovnih možnosti:

- Povprečni uporabnik bo na primer pričel pranje v treh korakih z zaporedjem ukazov: *"Osnovni programi > Belo perilo > START"*.
- Uporabnik, ki nima veliko znanja o pranju bo na primer uporabil naslednje zaporedje ukazov: *Čarovnik pranja > Belo perilo > .....*
- Napredni uporabnik pa bo uporabil, *Moji programi, Dodatni programi, Orodja*, ali nekatere druge, hkrati pa bo poizkusil uporabiti dodatne nastavitve glede na svoje želje in potrebe.

Vmesnik, zgrajen na osnovi ikon

Slika 7 prikazuje še drugi tip grafičnega vmesnika, ki je zasnovan na principu ikon. Ta vmesnik prikazuje v glavnem ikone. Polje z ikono je hkrati tudi ukazna tipka. S pritiskom na določeno polje izberemo ustrezno funkcijo. Dodatni teksti so seveda lahko v različnih jezikih, na tej sliki je to sedaj slovenski jezik. Uporabnik lahko izbere seveda njemu domači jezik.

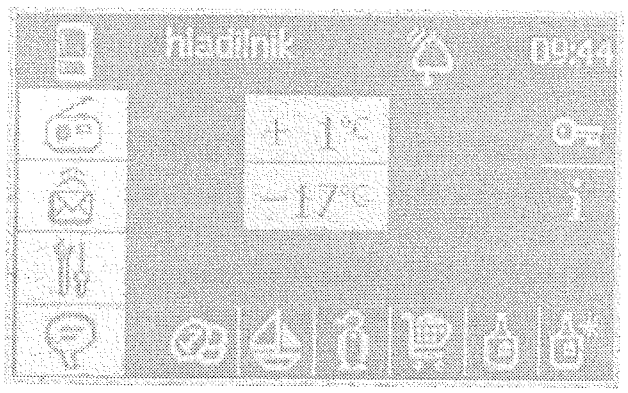


Figure 7: Grafični vmesnik z ikonami.

Mešani tip grafičnega vmesnika

Obe strani zaslona zasedajo ikone in tipke. Na zaslonu imamo hkrati še tekst, ki ustreza nameščenim ikonam.

Zgornji trije primeri prikazujejo, kako nam ta tehnologija omogoča prilagodljivo in napredno načrtovanje različnih grafičnih sistemov upravljanja.

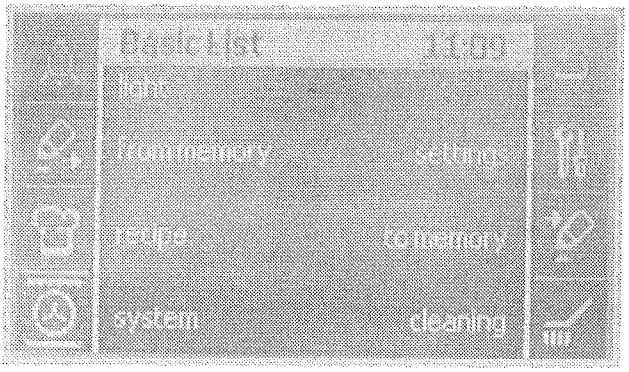


Figure 8: Mešani tip grafičnega vmesnika.

Z opisanimi pristopi lahko dejansko načrtujemo inteligentne in prilagodljive grafične vmesnike z vsemi modernimi grafičnimi strukturami, ki jih na primer najdemo v okolju PC oken.

V fazi načrtovanja uporabniškega grafičnega vmesnika lahko torej uporabimo različne pristope pri oblikovanju upravljalnih struktur.

Povezljivost in ergonomija

Povezljivost v beli tehniki postaja vse bolj atraktivna za trg. Bodoči aparati bodo postali terminali svetovnega sistema storitev, ki bodo postale neposredno dostopne preko globalnega storitvenega omrežja. Aparati, ki bodo delovali kot terminali takšnega svetovnega omrežja, bodo postajali bolj in bolj zapleteni s številnimi dodatnimi funkcijami. Takšni aparati bodo običajno postali del svetovnega spleta - Interneta. Uporaba takšnih aparatov bo postala kompleksna in bo zahtevala primerno izučenega ali pa zelo dovzetnega uporabnika. Za modernega uporabnika takšna naprava ne bo predstavljala ovire pri uporabi. Čedalje bolj pomemben bo postajal uporabniško prijazen grafični vmesnik za upravljanje, ki bo na primeren način predstavil nove funkcionalnosti aparatov. Za takšne cilje je zelo primerna opisana vhodno-izhodna naprava, saj bomo za povezani hišni sistem vsekakor potrebovali uporabniško prijazne grafične vmesnike za upravljanje. Uporabnik bo lahko dosegal te naprave tudi preko drugih vhodno-izhodnih naprav grafičnega tipa.

Zaključek

LCD z vgrajeno enoto, občutljivo na dotik vsekakor ni nova naprava na trgu. Uporablja se že v različnih napravah: me-

rilni opremi, dlančnikih, prenosnih telefonih, itd. Opisana implementacija za področje bele tehnike pa je vsekakor nova na svetovnem trgu. Menimo, da bodo imele opisane lastnosti našega LCD zaslona z vgrajeno enoto občutljivo na dotik pomemben vpliv na ergonomske lastnosti aparatov bele tehnike in bodo vplivale na bodoče pristope pri oblikovanju bele tehnike. Vsekakor pa smo prepričani, da se tudi pri razvoju platforme strojne in programske opreme grafičnih LCD uporabniških vmesnikov nismo ustavili, ampak bomo nadaljevali razvoj takšnih in podobnih modernih elektronskih naprav za uporabo v naših aparatih.

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HIPOT-R&D d.o.o., Šentjernej, Slovenia

The HIPOT-R&D Research and Development in Technologies and Systems Company is established in 1996 to act as a research organisation for local electronic elements companies. Current research and development activities are organised in the HIPOT-R&D Company through research and development group. This group is responsible for research, development and technology transfer in the fields of thick-film hybrid microelectronics, sensors (mostly pressure sensors), electronics, electronics technologies, and electromechanical devices and systems. In the field of research and development, as well as in system upgrading the company works in close relationship with scientific institutions and technical associations both in Slovenia and worldwide. The co-operation with research partner "Jožef Stefan" Institute in Ljubljana is traditional and goes back to the 1970s. One part of the HIPOT-R&D Company is located in Ljubljana at the "Jožef Stefan" Institute and other part is in Šentjernej at the same location as industrial partner HYB d.o.o.. This distribution enables a very good co-operation between partners.

Company address

HIPOT-RR d.o.o.

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HYB d.o.o., Šentjernej, Slovenia

The HYB Hybrid Circuits and Sensors Company (it is in the category of SME) has experience in the production of custom thick-film hybrid circuits from 1972 and experience in the production of pressure sensors for medical applications from 1986 and for industrial applications from 1994.

A thick-film hybrid circuit can be described as a small, self-contained electronic circuit (module) made up of a ceramic substrate with a thick-film technology and a variety of different component types mounted on it with different assembling techniques. The markets for these products are mainly where reliability, space, weight are at a premium. Moreover in most cases the customer provides these and some other special performance requirements. This is known as a custom-designed hybrid circuit. The HYB has a complete technical staff to handle all aspects of the design and manufacture process.

HYB is renowned European designer and producer of pressure sensors for medical and industrial applications. The company is capable to design, construct, develop and manufacture pressure sensors with silicon or ceramic sensor elements and required signal conditioning electronic circuit.

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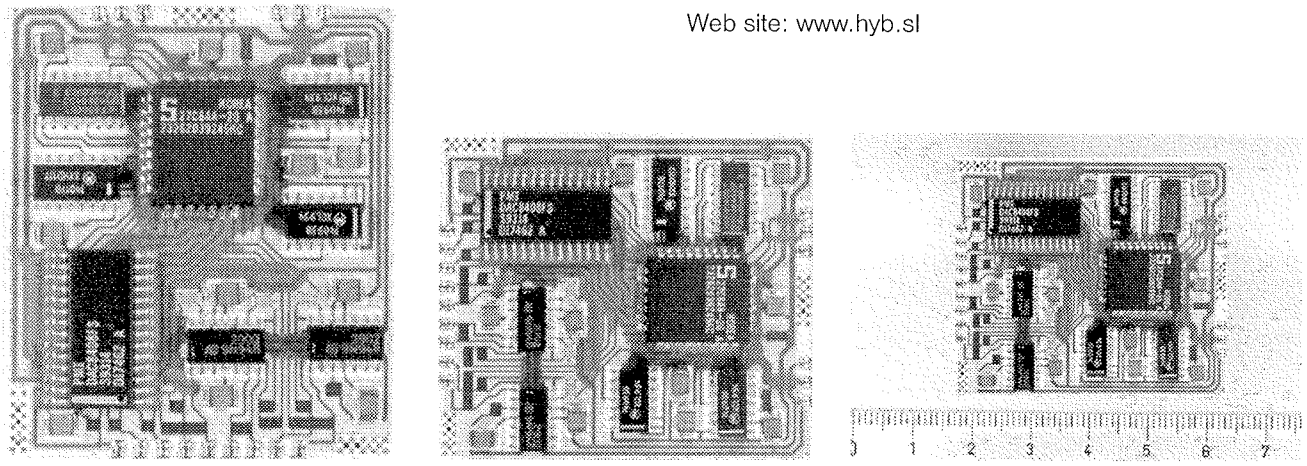
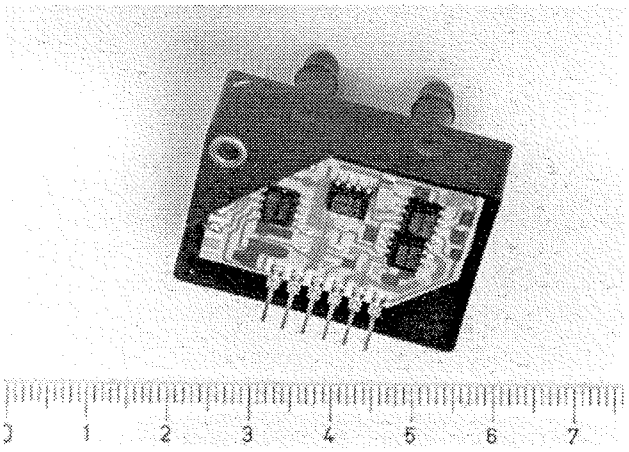
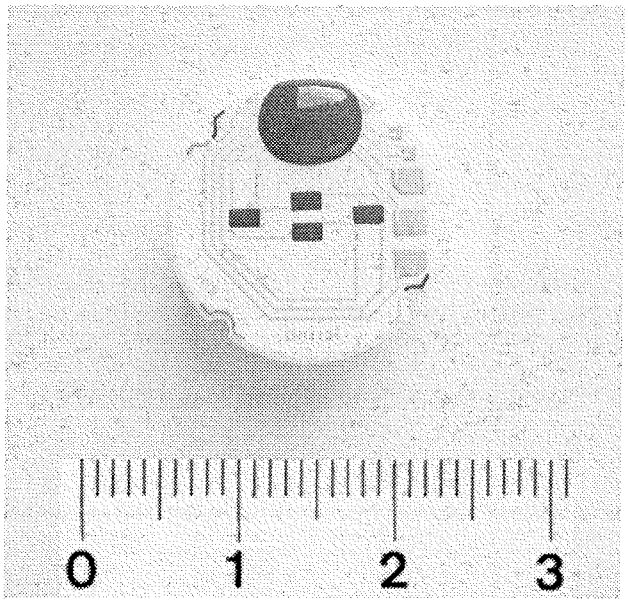


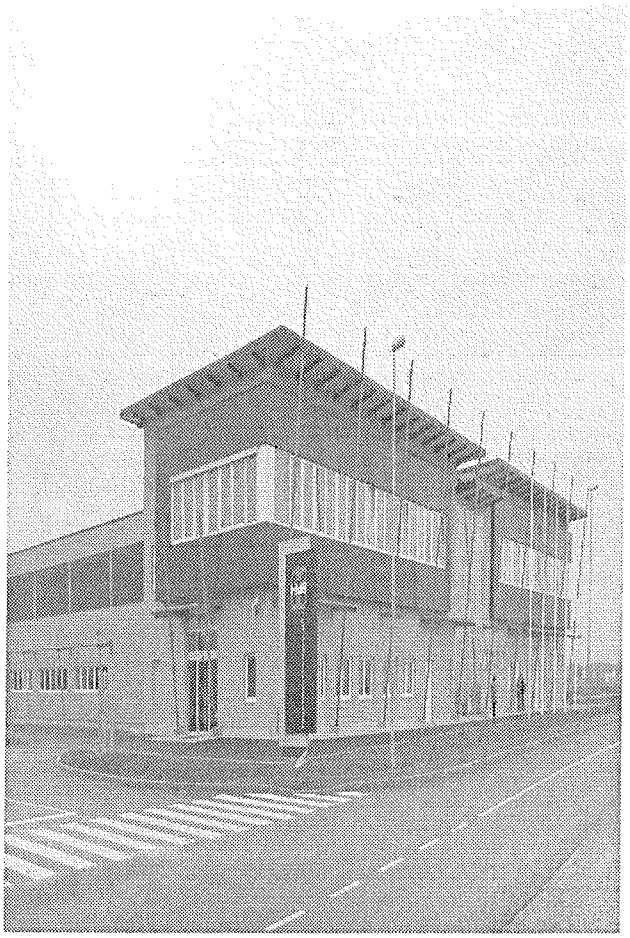
The example of custom designed thick-film hybrid circuit with SMD components.

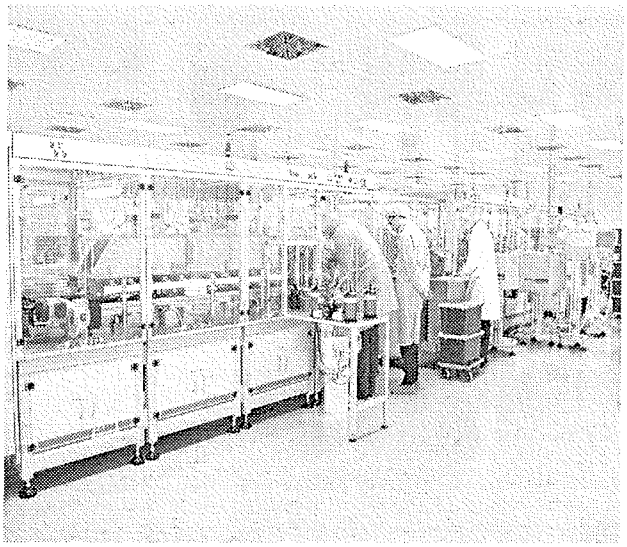


Pressure sensor with thick-film hybrid circuits for signal conditioning was designed for industrial applications.



Ceramic pressure sensor (with ASIC for signal conditioning) is using especially in harsh environment.





Production plant of the HYB Company in Šentjernej, Slovenia

EMPS 2006

4th European Microelectronics and Packaging Symposium with Table-Top Exhibition

Terme Čatež, Slovenia, May 22—24, 2006

http://www.EMPS2006.com

Call for Papers

Abstract deadline: October 31, 2005

The Technical Programme Committee invites authors to submit abstracts of original work describing recent developments in the field of microelectronic packaging and interconnection. The topics of the EMPS 2006 follow the motto *"Everything in electronics between the chip and the system"* and include:

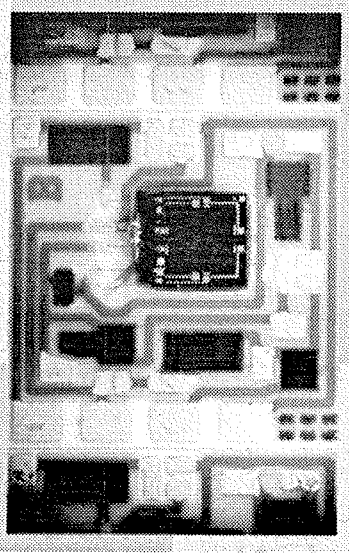
- **Materials & technologies**
- **Advanced packaging & MEMS**
- **Interconnection technologies & substrates**
- **Semiconductor structures and circuits**
- **Passive components, active devices & systems**
- **Electrical, thermal, mechanical and multi-physics simulations**
- **Microelectronic applications**
- **Quality & reliability**

Please submit your 300-word abstract with a title and author-contact information before October 31, 2005 via the conference website: www.EMPS2006.com

The Technical Programme Committee will evaluate all abstracts and authors will be informed about the acceptance of their abstract by December 31, 2005.

Every two years the International Microelectronics And Packaging Society, IMAPS, Europe organises the European Microelectronics and Packaging Symposium, EMPS, in a different European country. The EMPS brings together specialists from industry and academia, and is a great opportunity for presenting and discussing on the subject of microelectronic packaging and interconnection technologies.

EMPS 2006 will take place in the modern business centre at Hotel Terme, situated in the pleasant surroundings of Terme Čatež, the largest natural health resort in Slovenia.



Prior to the symposium there will be a satellite Workshop on **Ferroelectric Thin- & Thick-films Processing and Their Applications in MEMS** on May 21, 2006

Organised by:

MIDEM – Society for Microelectronics, Electronic Components and Materials – IMAPS Slovenia Chapter
Dunajska 10, SI-1000 Ljubljana,
Slovenia
http://www.midem-drustvo.si/

In co-operation with:

Jožef Stefan Institute, Electronic Ceramics Department

Jamova 39, SI-1000 Ljubljana,
Slovenia
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Hybrid Circuits and Sensors

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NOVICE NEWS

IC makers team up on phase-change memory

CHIP MAKERS Infineon, IBM and Macronix have launched a joint research initiative to explore the potential of a *new* form of computer memory called phase-change memory (PCM).

PCM is a novel technology that stores data by changing the state of a special material from an amorphous to a crystalline structure, rather than storing data as an electrical charge.

While in its early stages, the technology shows potential for high speed, high density storage of data. It also has the advantage of retaining data even when power is turned off. The initiative combines IBM's strengths in the research of fundamental materials and physics, Infineon's expertise in high volume manufacturing of various memory technologies and product types and Macronix's experience in non-volatile memory technologies.

"This collaborative effort reinforces IBM's commitment to explore new phenomena for memory applications," said IBM Research vice president TC Chen. "The project will aim to develop the materials for high performance, advanced non-volatile memory and evaluate these materials in realistic memory chip demonstrations."

Wilhelm Beinvogl, senior vice president at Infineon's Memory Products Group, added: "The initiative underlines Infineon's strong momentum in the evaluation and development of interesting emerging memory technologies.

"With this partnership combining resources from specialists in different areas, Infineon continues its long history of R&D cooperations."

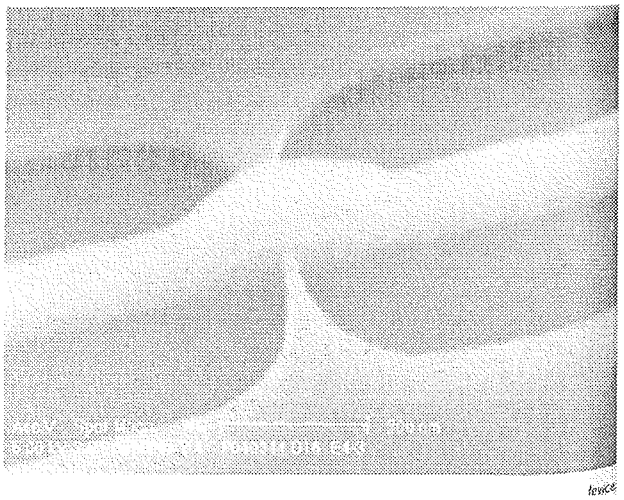
The research will be conducted at IBM's TJ Watson Research Center in New York and the IBM Almaden Research Lab in San Jose. Around 20-25 employees from across the three companies will be seconded to the project.

Emerging alternative devices.

IC industry is looking for innovative transistor architectures that are able to improve device performance and minimize current leakage at the 32nm technology node and beyond. Multiple-gate FETs (MuGFETs) based on the FinFET architecture are possible candidates. The main feature of the FinFET is that the active area of the transistor is realized as a thin silicon wire between the source and drain contacts (i.e. non-planar). In triple-gate FinFETs, the gate wraps around the rectangular silicon fin from three sides. This new technology goes beyond bulk silicon and relies heavily on the use of high-quality, very thin silicon-on-insulator (SOI) wafers.

IMEC studies new non-planar CMOS transistor architectures such as MuGFETs and develops the process steps that are necessary to fabricate these structures. The circuit behavior of these devices is investigated by making ring oscillators, SRAM cells and RF structures.

In 2004, IMEC researchers were able to demonstrate the smallest SRAM cell ever reported (0,314μm^2), using six triple-gate FinFET-style transistors. The SRAM cell achieves excellent static-noise margin of 240mV at 1,0V operation and shows good functionality down to 0.4V with a symmetric butterfly curve. Further, the cell shows great potential for scaling down to the 32nm node. The triple-gate transistors have a silicon fin that is 70nm high – 40nm higher than typically reported so far – and 35nm wide.

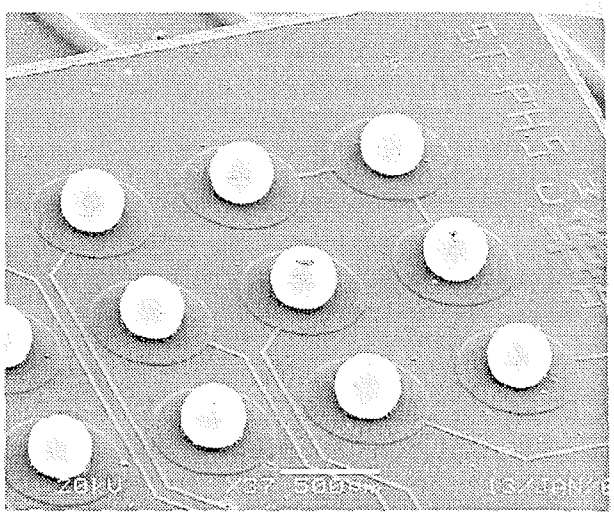


Emerging CMOS devices for future technology generations (EMERALD). The objective of the EMERALD program is to build and study CMOS device architectures, which have better scaling properties than traditional bulk devices for the 45nm generation and beyond.

Leadfree solder joints

European legislation forces the electronics industry to banish lead from electronic products. This also accounts for solder bumps used in flip-chip technology, traditionally made of SnPb. Solder bumps are used in combination with under-bump metallurgy (UBM).

In this context, IMEC studies Sn solder bumps and the influence of different UBMs (Cu and Co). Scanning electron microscope pictures, measurements on solder joint hardness, and reliability tests were performed. The use of cobalt UBM in combination with lead-free solder bumps resulted in 40% higher reliability as compared to Cu UBM. This is due to a more gradual variation in hardness over the solder joint stack ensuring a more elastic structure.

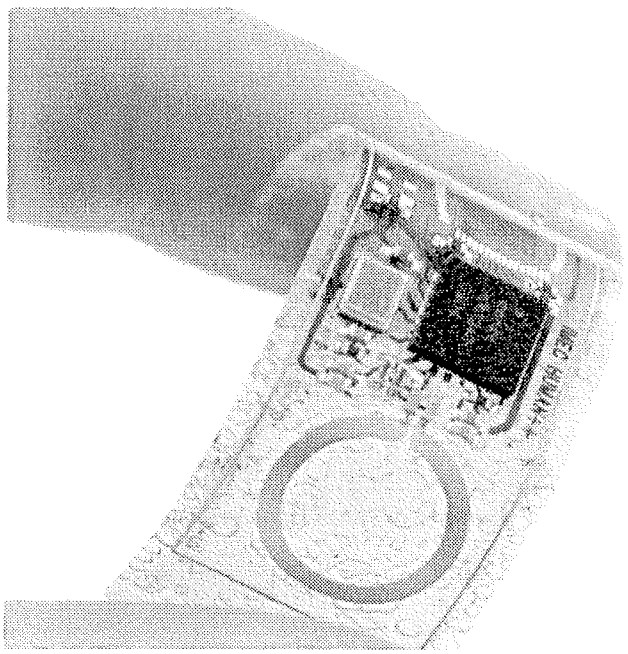


ELFNET (European Lead Free soldering NET work) is a European research network that unites national organizations, technical experts and industry bodies in microelectronics. This network aims to coordinate, integrate and optimize research, enabling electronics producers in the EU to meet an EU directive to introduce lead-free soldering by July I, 2006. IMEC represents Belgium in this initiative.

Wireless body-area network

Individual sensor nodes measuring vital body information can be linked to form a network. IMEC developed such a prototype sensor network or WBAN constituting three nodes: a 24-channel EEG node, a single-channel ECG node and a single EMG node. These sensor nodes – measuring brain, heart and muscle activity respectively - send their data wirelessly to an USB stick. From here, data can be stored on a PC and further be analyzed by medical experts.

Since all nodes in the network share the same medium, a medium-access-control (MAC) protocol for low-power sensor networks has been implemented. The time-division-multiple-access (TDMA)-based protocol gives each sensor node its slot to transfer the data packets. The base stationsends a multicast beacon to keep the nodes synchronized. This sensor MAC approach drastically improves power consumption since all nodes can be put in low power sleep mode until sensor data have to be sent.



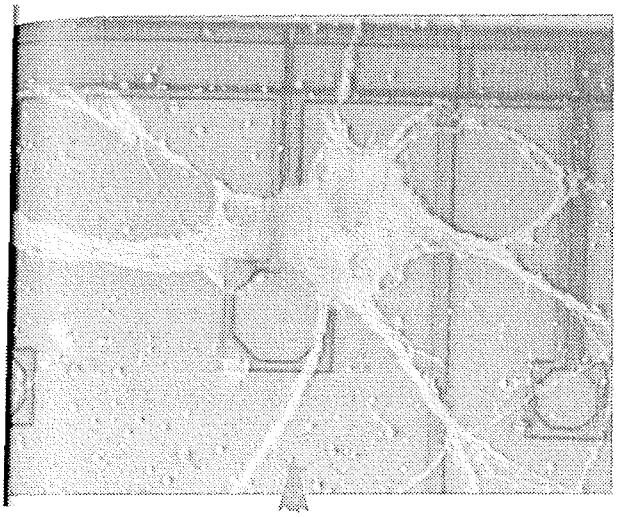
Continuously striving towards further miniaturization, IMEC researchers have developed a 25-channel low-power ASIC that is able to execute 24-channel EEG and ECG measurements. The ASIC measures only 7x7mm^2 as compared to the PCB - developed last year - with the same functionality, measuring 160x140mm^2. This sensing layer will in a further stage of the research be integrated in the existing 3D stack, offering a complete intelligent cube for biomedical monitoring.

Neurons on chip

The growth of brain cells (neurons) on a chip active surface is an exploratory research domain aiming at realizing a two-way interface between these two very different worlds. Applications include the study of neurological disorders such as Alzheimer and Parkinson, the screening of neurological drugs, the production of brain-controlled prostheses and the use of implants to restore neurological or sensory functions.

IMEC studies the possibilities of neurons on chip together with the Hebrew University of Jerusalem in Israel (HUJI) and the academic hospital of the K.U.Leuven. Within this framework, IMEC developed a very sensitive transducer based on a dual-gated GaAs thin field-effect transistor (FET).

However, sensitive transducers alone will not do the trick. Patterned biometric surfaces ensure survival of the neurons in this artificial environment and control the position of the neural network to enhanced signals. In 2004, IMEC created patterns of poly-L-lysine (PLL) - a cytophylic peptide - by means of micro-contact printing. Onto this pattern, simplified hippocampal neuronal networks self-assembled.



In 2004, a unique packaging technology was worked out that allows for the tricky combination of housing the neurons in an aqueous solution while at the same time keeping the electronics substrate and bonding wires dry. The transducers are flip-chip bonded on a ceramic carrier. An open window of 3x3mm^2 is provided in the carrier to allow access to the active area of the chip. An open glass container with neuron culture can be glued on top of this carrier opening.

Passports to feature Infineon security chips

NUMBER ONE European chip maker Infineon has announced that the German government is using its security chips for use in new electronic passports.

The German Passport Office is due to begin issuing the new electronic passports in November this year and Infineon's chips are designed to prevent the passports being counterfeited.

The holder's information -such as date of birth, photo, passport number - will be stored encrypted on a chip. From 2007, the chip will also store a print of the holder's index finger.

The data stored on the chip -which is invisibly integrated into the surface of the passport - can only be accessed when the passport is opened, and is transmitted wirelessly to special read-write devices.

The chip features more than 50 security methods to ensure that personal data is protected against unauthorised read-out and manipulation.

These techniques include RSA (a special computing algorithm for encrypting data, named after its inventors Ronald Rivest, Adi Shamir and Leonard Adleman).

It is estimated that a billion standard PCs operating in parallel would have to keep computing for about a million years in order to retrieve information encrypted using this method. Other security features include protective shields on the surface of the chip and sensors that prevent hackers from reading out the chip by applying different voltages.

"We've equipped our chips with the best possible protection mechanisms," said Infineon executive vice president Peter Bauer.

"A host of security certificates prove that Infineon's security controllers have successfully passed the world's most stringent security tests conducted according to international standards."

According to market analyst Gartner, Infineon is the global leader in the market for chip for card applications, having generated the greatest sales revenues in this area seven years in a row.

Infineon spins off wearable electronics operations

NUMBER one European chip maker Infineon has sold its wearable electronics operations to Interactive Wear in a management buy-out.

Under the deal, Germany-based Interactive Wear has acquired Infineon's wearable electronics patents and licenses, developmental hardware and software and customer base.

The company has also taken ownership of Infineon's wearable electronics parts inventory and finished wearable electronics products. The two companies have agreed not to disclose the sale price.

Infineon said it had decided to dispose of its wearable electronics division as part of its strategy of focusing on its core operations.

"By spinning off wearable electronics activities, Infineon is following through on its strategy and is concentrating on its core business," said Infineon corporate vice president Dominik Asam.

Markus Strecker, Infineon's former head of engineering for wearable electronics, has been appointed chief technical officer of Interactive Wear. He is joined by Andreas Roepert (chief executive officer) and Awa Carlinska (chair of the supervisory board).

Roepert said: "Thanks to the technological head start and network of partners that we acquired from Infineon, and to the extremely positive market appraisal from various analysts, who anticipate a market volume of up to US$1 billion for technical textiles in 2008, we see excellent market opportunities and developmental potential for our company."

300 Percent Growth Rate in the VoIP Market for Infineon

Infineon Technologies has announced that its revenues in VoIP (Voice over Internet Protocol) CPE (Customer Premises Equipment) products grew at the rate of 300 percent from 2003 to 2004, much higher than the 70.2 percent average for the total market of 102 million US-Dollars (source: iSuppli 2005).

The worldwide number of residential VoIP-users is expected to be approximately 5 million in 2004 and to increase to 200 million subscribers in 2010. Consequently Infineon ranked as the worlds fifth largest supplier of VoIP ICs in 2004, up from number 10 position in the previous year.

E-Beam Lithography to Fraunhofer Nanoelectronic

Leica Microsystems and Fraunhofer CNT report the start-up of a Leica SB351 DW e-beam system at the recently opened Fraunhofer Center for Nano-electronic Technology (CNT) in Dresden, Germany. Representing a two-digit million amount capital investment, this system will be used for selected processes used in the development of high-density storage devices and high performance transistors.

The Leica system uses a variable shape beam to enable high precision direct write patterning down to 45 nm feature size. The system meets all requirements for the 65 nm technology node for 300 mm wafer lithography.

Research results from a project (T207) sponsored by MEDEA+/BMBF were instrumental in the development of this system. BMBF supports the challenging 65 nm CMOS process on 300 mm wafer project, in particular the Use of electron beam technology for wafer direct writing with minimal 25 nm feature sizes sub-project.

Fraunhofer CNT took over an 800m^2 clean room facility on May 31, 2005, which was previously owned by Infineon. Dresden offers an excellent location for joint R&D in nano-electronics between research institutes and material and system manufacturers. Research will focus on the development of selected process steps for the production of high density storage devices and high performance transistors. Infineon Technology Dresden, IMS Chips Stuttgart and Leica Microsystems Jena were involved in an intense collaborative effort before the delivery of the Leica system.

Intel to invest $345 million at two manufacturing sites

Intel Corporation today announced plans to invest $345 million in two of the company's existing manufacturing sites in Colorado and Massachusetts. The investments will be used to increase the capacity of the wafer fabrications facilities (fabs), Fab 17 in Hudson, Massachusetts and Fab 23 in Colorado Springs, Colorado.

Both fabs are 200mm facilities that produce primarily chipsets communications and flash memory components for a variety of Intel platforms.

"These investments will increase the capacity of our 200mm manufacturing network to support our platform initiatives and will give us additional supply flexibility across a range of products," said Bob Baker, senior vice president, general manager, Technology and Manufacturing Group. "For Intel, manufacturing is a key competitive advantage that serves as the underpinning for our business and allows us to provide customers with leading-edge products in high volume. The decision to investment in our sites in Colorado and Massachusetts reflects the strategic importance of these facilities and our outstanding team of employees."

In Colorado Springs $190 million will be invested as part of an upgrade to a second clean room within Fab 23 that will allow Intel to complete final processing steps for microprocessors – produced on 300mm wafers at other Intel locations – prior to final testing and packaging. Construction on the project is set to begin immediately, which will allow processing of advanced microprocessors in the second half of 2007. The project is expected to create several hundred new jobs in Colorado Springs over the next three years.

In Hudson, Intel's $155 million investment will be used to increase overall capacity at Fab 17 by adding new manufacturing equipment and reconfiguring portions of the factory. The additional capacity will be used to manufacture a variety of logic products, including chipsets to support Intel's platform initiatives for mobile, desktop and server systems. This investment in Hudson will result in the creation more than 300 new manufacturing jobs.

STMicroelectronics Simplifies Emerging Energy Metering Applications with Smart Power Technology

Geneva, June 20, 2005 - STMicroelectronics (NYSE: STM) has announced the availability of a new device that incorporates all of the core circuitry required to implement fully electronic electricity meters. The STPM01addresses a wide range of electricity metering requirements, operating as a stand-alone power meter in the simplest low-end equipment or as a peripheral in sophisticated microprocessor-based meters that support functions such as remote metering, reactive power measurement, multiple tariffs and tamper detection.

Electric utility companies around the world are increasingly looking to replace the traditional electromechanical meter, which has remained essentially unchanged for over a century, by electronic meters. Among the many advantages of electronic meters are increased accuracy, reliability and robustness, easy calibration and reconfiguration, and the ability to incorporate advanced functions such as multi-tariff billing, tamper proofing, pre-payment, power outage detection, power factor measurement and automated meter reading services.

Jointly developed by ST and ISKRAEMECO, one of the world's largest meter manufacturers, the STPM01 is a standard device modified from an ASIC solution built for ISKRAEMECO using ST's advanced BCD6 smart power technology, allowing all of the necessary analog, digital and power circuits to be integrated on a single chip. The major blocks include analog signal conditioning, two Analog-to-Digital Converters, a hardwired dedicated Digital Signal Processor (DSP), an SPI interface to an external MCU, a block of 56 OTP (One Time Programmable) bits for calibration and configuration, a Voltage-to-Frequency converter to drive a stepper motor display in low-end applications, and two current-limited, low-drop voltage regulators to supply the analog (3V) and digital (1.5) circuitry.

The flexible and configurable analog front-end allows the device to work with a variety of current sensors, including current transformers, microOhm shunts and Rogowski coils. The dedicated DSP performs real-time calculations of active, reactive and apparent power, RMS voltage and current, and line frequency, using innovative algorithms for which ISKRAEMECO has filed patent applications.

The SPI interface is used to control, configure and calibrate the device using the OTP block and to transmit the digital output data to an external MCU, which handles data collection and management in high-end applications. In addition, the computed power values are also converted internally into pulses to directly drive stepper motor displays in the most cost-sensitive low-end applications.

The OTP block, which is accessible via a simple PC interface and software, allows fast and accurate calibration of the voltage and current sensors, phase correction and temperature drift. Additional features of the STPM01 include Live and Neutral wire current monitoring for tamper detection in secure energy meters; LED drivers to indicate power, tamper detection and no-load conditions; and a zero-crossing signal that can be used to avoid arcing when switching heavy inductive loads in industrial control applications.

The STPM01 offers high performance in terms of accuracy, allowing full compliance with the IEC62052-11 and IEC62053-2X specifications for single-phase class 0.5 wattmeters, while a Synchronisation pin also supports three-phase metering applications. The device operates over a wide range of mains voltage (40-300VRMS) and line frequency (45-65Hz), and can measure up to 200ARMS. In addition to the lower component cost due to the high level of integration, the STPM01 also reduces hidden manufacturing costs associated with calibration, thanks to the fast, tamper-proof OTP block.

The STPM01 is supported by two demo boards/reference designs: a Measurement Board that allows the STPM01 to operate as a stand-alone solution for stepper driving, and a Control Board equipped with an ST7 MCU, LCD display and RTC that connects to the Measurement Board via the SPI to provide a complete solution for medium/high-end applications.

The STPM01 is priced at approximately US$2.00 in quantities of 1000 pieces.

Further information on ST's range of interface and metering IC is available at www.st.com/interface and http://www.st.com/metering