

A NEW APPROACH IN TESTING ANALOG-TO-DIGITAL CONVERTERS

Martin Kollár

Technical University of Košice, Slovakia

Key words: testing ADC, integral non-linearity, differential non-linearity.

Abstract: This paper describes a new approach in testing static parameters of analog-to-digital converters (ADCs). The input of an ADC to be tested is connected to a generator of saw-tooth impulses. In comparison to ordinary approaches, the measured decision levels are not related to zero potential but to the decision levels of an additional ADC, which is of same type as tested ADC. Approximating principle-based test system, with a digital-to-analog converter (DAC) in the feedback, measures these differences, which are in the extreme case in the range of a few least significant bits (LSB) of tested (additional) ADC. It has been proposed a special algorithm, to which output codes of tested and additional ADC enter, to control this DAC, which output is added through a resistive divider to the input of additional ADC. By using this approach, there are no special requirements on the precision of input saw-tooth impulse generator and precision of the obtained integral non-linearity (INL), differential non-linearity (DNL) characteristics mainly depends on DAC used. It was also shown that using 8 bit DAC the precision is in the range of a few hundredths of LSB. By simulations with MATLAB, the theoretical considerations are verified.

Nov pristop k preizkušanju analogno-digitalnih pretvornikov

Ključne besede: testiranje analogno-digitalnih pretvornikov, integralna nelinearnost, diferencialna nelinearnost

Izveček: V prispevku opisujemo nov pristop k preizkušanju statičnih parametrov analogno-digitalnih pretvornikov (nadalje ADC) Vhod pretvornika, ki ga želimo preizkusiti, priklopimo na generator impulzov. V nasprotju s standardnim pristopom, kjer merjene nivoje primerjamo z ničelnim potencialom, jih v našem primeru primerjamo z drugim pretvornikom istega tipa kot ta, ki ga preizkušamo. Če upeljemo testni sistem tako, da dodamo digitalno-analogni pretvornik (DAC) v povratni vezavi, je ta sposoben meriti razlike, ki so v skrajnem primeru v območju zadnjega pomembnega bita (LSB – Least Significant Bit) testiranega (dodatnega) pretvornika. Predlagamo poseben algoritem, kjer izhodne kode testiranega in dodatnega pretvornika peljemo v DAC, katerega izhod preko uporovnega delilnika vrnemo nazaj v dodatni ADC. Pri takem pristopu točnost generatorja vhodnih impulzov ni pomembna in sta integralna in diferencialna nelinearnost odvisni predvsem od uporabljenega DAC pretvornika. Pokažemo, da je, če uporabimo 8 bitni DAC, točnost v območju nekaj stotink LSB. Teoretična predvidevanja smo potrdili s simulacijo z MATLABom.

Introduction and motivation

The price of mixed-signal integrated circuits is dominated by the ever-increasing testing cost of the analog blocks and converters. In particular, the full test of an ADC implies the determination of two kinds of parameters, the static errors linked to some deviations of the converter transfer function, and the dynamic features expressing the distortion and noise of the converted signal introduced by the converter. Static errors are generally deduced from a histogram-based test /1/ lying on a statistical analysis of the occurrence frequency for each output code, while dynamic parameters are usually evaluated from the spectral distribution of the converted signal, computed using a Fast Fourier Transformation (FFT) /2/.

Although the principles of both the static and dynamic tests have been well elaborated /1-3/ more work remains to be done on its feasibility issues. The test methods have been originally proposed under the assumption that the input source of reference signal is without uncertainties.

Let us assume that the full scale (FS) of a tested 12 bit ADC is in the range of a few V. Then the LSB will be in the range of a few mV. Since, the precision of signal generator should be at least two orders higher than LSB of ADC be-

ing tested /3/, in this case the generator absolute error should be in the range of a few hundredths of mV. A serious problem appears here because if it will be 16 bit ADC, the generator absolute error should be in the range of a few thousandths of mV.

To avoid such requirements on high precision of input generator a new approach will be presented in the following part of this letter. Originality consists in that all measurements of decision levels of tested ADC are not related to zero potential but to decision levels of an additional ADC. Thus, if this additional ADC is of same type as that to be tested, the maximal measured values will be in the range of a few LSB of tested ADC.

To be more detailed, let us assume a tested and additional ADC with an element of transfer characteristic according to Fig.1. By using an ordinary approach the voltages V_1 , V_2 are measured in relation to zero potential, while using a new approach the voltages V_1' , V_2' are measured in relation to a decision level output code i of an additional ADC. The voltages in both approaches have to be generated with the same absolute error. However, using new approach the acceptable relative error can be much greater than that in the ordinary approach.

The principle of this new method including also a possible hardware realization is depicted in the following sections.

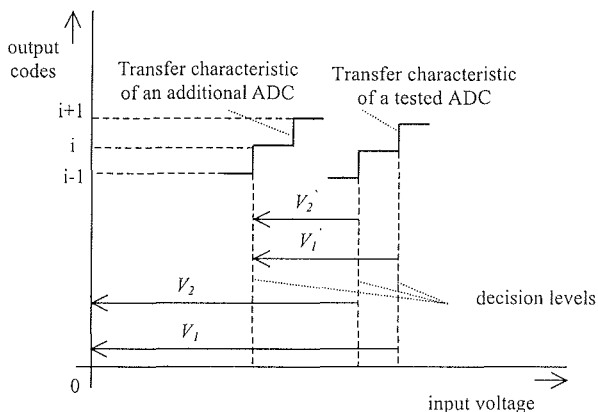


Figure 1. Principle of a new approach in testing ADCs

Principle of the new method

Fig. 2 shows a complete scheme of test system. As it can be seen the output codes of additional and tested ADC are processed in a microprocessor (μP). Also DAC, which output voltage through a precise resistive divider R_2/R_1 is added to input of tested ADC, is controlled by μP . According to Fig.1, by increasing input voltage from saw-tooth impulse generator, because of given transfer characteristics, the output code i at first will be generated by additional ADC and then with a time delay by tested ADC. However, by adding a voltage from resistive divider R_2/R_1 which is smoothly greater than V_2 the output code i at first will be generated by tested ADC and then with a time delay by additional ADC.

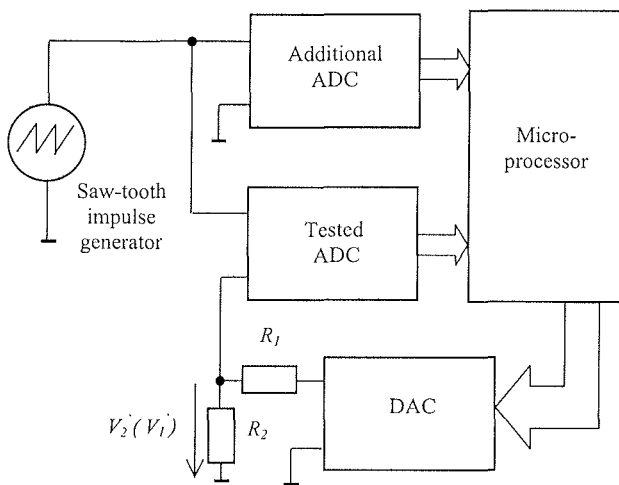


Figure 2. Block diagram of new test method

To achieve very short time of measurement of voltage difference V_2' approximating principle based conversion can be used. For example, by using 8 bits DAC the saw-tooth impulse must be generated 8 times by input generator.

During the first impulse is only done a decision whether difference voltage is positive or negative. In case that it is positive value which means that output code i at first will be generated by additional ADC and then with a time delay by tested ADC, the voltage at resistive divider output will be set to $FS/2$, where FS is a full scale of DAC relating to resistive divider output. During the second impulse is tested by μP whether additional or tested ADC at first generates output code i . In case that again at first additional ADC generates output code i , the output voltage of resistive divider will be set to $FS/2+FS/4$. In opposite case this voltage will be set to $FS/2-FS/4$. Thus the output voltage of resistive divider is approximately set during the following six cycles. The approximating principle of conversion is well known /4/ therefore here only its summary is made.

In the same manner difference voltage V_1' is measured. Since, in this case the measurement is related to decision level of output code i from additional ADC and to decision level of output code $i+1$ from tested ADC, μP tests during each cycle, which one from these output codes is generated as first. From measured V_1', V_2' DNL of output code i is calculated using formula /4/

$$DNL(i) = \frac{(V_1' - V_2' - LSB)}{LSB} \tag{1}$$

where LSB is value of ideal least significant bit of tested (additional) ADC.

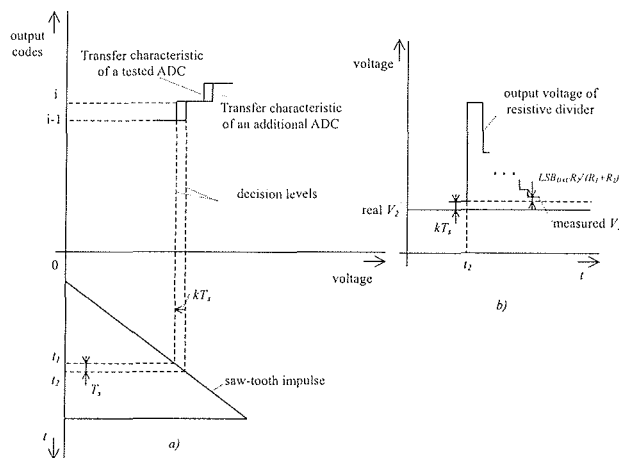


Figure 3. Precision of measured V_2'

From (1) it is clear that the precision of calculated DNL is determined by precision of measured V_1', V_2' . Fig.3a shows an example when the difference between actual decision levels of output code i of tested and additional ADC is smoothly lower than kT_s , where k is slope of saw-tooth impulse and T_s sampling period. In the moment t_1 output code $i-1$ is at output of additional and tested ADC, while in the moment t_2 it will be output code i . In this case, it is not possible to decide whether by tested or additional ADC at first was generated output code i . Thus, instead to be decreased, the output voltage of DAC will be increased about value $FS/2^n$, where n is actual step of approximating con-

version. In the remaining conversion steps this voltage will be increased but with the resolution $LSB_{DAC} \cdot R_2 / (R_1 + R_2)$, where LSB_{DAC} is least significant bit of DAC, shown in Fig3b. Therefore the maximal error of measured V_2' is given by formula

$$\Delta_{V_2'} = |kT_s| + \left| \frac{R_2}{(R_1 + R_2)} LSB_{DAC} \right| \quad (2)$$

Since the same error is for measured V_1' , the maximal error of measured DNL is given by formula

$$\Delta = 2 \left(|kT_s| + \left| \frac{R_2}{(R_1 + R_2)} LSB_{DAC} \right| \right) \quad (3)$$

If nominal parameters are such that kT_s is about hundredths of LSB, then an extreme change of slope about 100 % reflects to error $2kT_s$ and thus does not influence markedly the resultant precision.

Measurement of INL and DNL characteristic

It is described in previous section, the difference voltages V_1', V_2' have to be measured to obtain DNL in given output code i . In this section, an algorithm is described by using of which the complete INL and DNL characteristic is obtained passing the full scale of tested and additional ADC s times, where s is the number of bits of DAC used. By assuming that

$$\overline{DNL} = \begin{pmatrix} DNL\left(-\frac{N}{2}\right) \\ \vdots \\ DNL\left(\frac{N}{2}-1\right) \end{pmatrix} \quad \text{and} \quad \overline{INL} = \begin{pmatrix} INL\left(-\frac{N}{2}+1\right) \\ \vdots \\ INL\left(\frac{N}{2}\right) \end{pmatrix} \quad (4)$$

where N is the number of output codes of tested (additional) ADC we can write that

$$\overline{DNL} = (\overline{V_1} - \overline{V_2}) / LSB - \overline{E}, \quad (5)$$

where

$$\overline{V_1} = \begin{pmatrix} V_1\left(-\frac{N}{2}\right) \\ \vdots \\ V_1\left(\frac{N}{2}-1\right) \end{pmatrix}, \quad \overline{V_2} = \begin{pmatrix} V_2\left(-\frac{N}{2}\right) \\ \vdots \\ V_2\left(\frac{N}{2}-1\right) \end{pmatrix} \quad \text{and} \quad \overline{E} = \begin{pmatrix} 1 \\ \vdots \\ 1 \end{pmatrix}_{(N-1) \times 1}, \quad (6)$$

and

$$\overline{INL} = \begin{pmatrix} 1 & 0 & 0 & \dots & 0 \\ 1 & 1 & 0 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & 1 & \dots & 0 \\ 1 & 1 & 1 & \dots & 1 \end{pmatrix} \overline{DNL} \quad (7)$$

Then, for example, because $INL(i) = \sum_{r=-N/2}^{i-1} DNL(r)$ it could seem that maximal error of $INL(i)$ is $\Delta | -N/2 - i + 1 |$. However, it should be noted that maximal error of DNL in (3) does not represent the systematic error, but the maximal value of random signal with rectangular probability of distribution and zero mean $/4/$. Therefore, the maximal error of measured DNL remains in the range of a few hundredths of LSB. This fact will be verified by simulation with MATLAB in the following section.

To measure vector $\overline{V_2}$ the following algorithm is to be implemented to μP .

```

declaration of input variables {
    i=-N/2+1;
    y1=-N/2;
    y2=-N/2;
    p=1;
    A=FS;
    V2=zeros (N-1,1); } zero matrix
                             } (N-1)x1

global cycle {
    while p<9
        one saw-tooth impulse cycle {
            while i<N/2-1
                test cycle {
                    output DAC=V2(i);
                    while (y1<i & y2<i)
                        y1=output (additional ADC);
                        y2=output (tested ADC);
                    end
                    if y1=i
                        yp(i)=V2(i)+A/2;
                    else
                        yp(i)=V2(i)-A/2;
                    end
                    V2(i)=yp(i);
                    i=i+1;
                }
            end
            A=A/2;
            i=-N/2+1;
            p=p+1;
            y1=-N/2;
            y2=-N/2;
        }
    end
}
    
```

At the beginning the variables are declared. Into variable **A** the full scale **FS** of DAC is saved and zero column matrix **V2**, **yp** are defined. The algorithm contains a global cycle with two embedded cycles. During the test cycle, whether output code i is at first generated by tested or additional ADC is tested. If, for example, the output code i is at first generated by additional ADC the output of DAC will be enlarged about $A/2$ (at the beginning $A=FS$) and this value is saved into element **V2(i)**. Then, i is incremented about 1 and this procedure will repeat. Thus, from one saw-tooth impulse cycle vector $\overline{V_2}$ after 1st step of conversion will be obtained. Then, the variable **A** will be decreased in half and i will be set to $-N/2+1$. The whole procedure will repeat. The result will be vector $\overline{V_2}$ after 2nd step of conver-

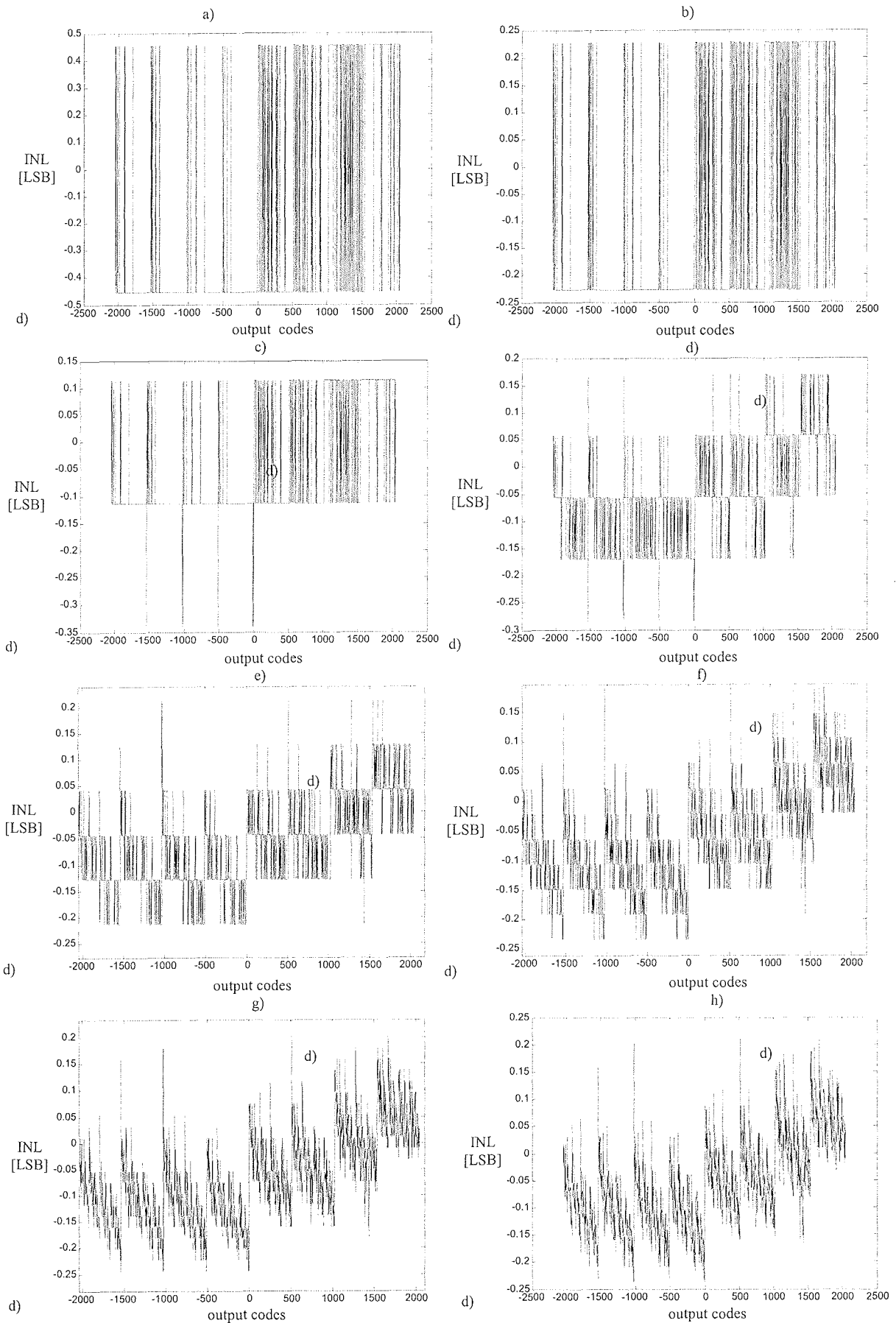
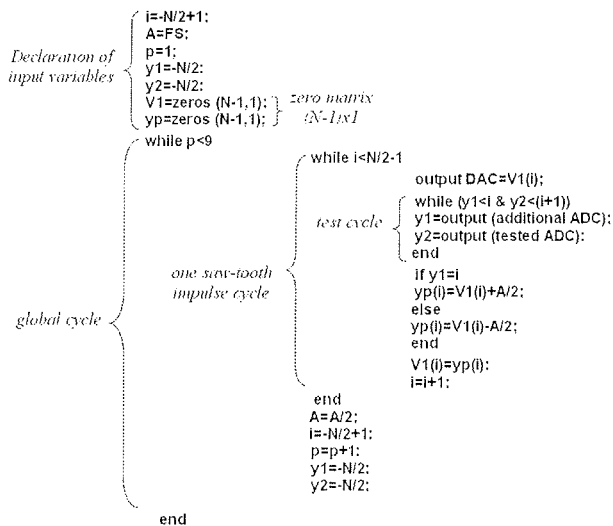


Figure 4. INL characteristic after: a)1st, b)2nd, c)3rd, d)4th, e)5th, f)6th, g)7th, h)8th step of conversion

sion. The number of steps of conversion depends on number of bits of DAC. In above algorithm the number of steps is 8 because 8 bit DAC is being used.

To measure vector \vec{V}_1 the following algorithm is to be implemented to μP .



As it can be seen, the only difference is in test cycle, where it is tested whether at first will be generated output code i by additional ADC or output code $(i+1)$ by tested ADC.

The complete INL and DNL characteristic can be obtained by means of equations (5),(7).

Results of simulation

The test system according to Fig.2 was simulated in MATLAB. 12 bit ADC in PC-LAB-1200 was used as tested. Its transfer characteristic was obtained by using histogram-based test method /4/. For simplicity, 12 bit ADC with ideal transfer characteristic was used as additional. The parameters of saw-tooth impulse were as follows: $k= 4.10^2 \text{ V}\cdot\text{s}^{-1}$, $V_{max}= 9 \text{ V}$ and $V_{min}= -9 \text{ V}$. The output voltage from DAC ranged from -8 to 8 V , the resistive divider ratio was $1/1000$ and sampling period T_s of the system was 10^{-7} s .

INL characteristics calculated by means of (5) and (7) from vectors \vec{V}_1 , \vec{V}_2 after given steps of conversion are shown in Fig.4. The resultant INL characteristic is shown in Fig.4h. The difference between this characteristic and that ideal (obtained by using histogram-based test) is shown in Fig.5. As it can be seen the maximal error is equal to -0.014 LSB .

Very interesting was to study the dependence of this error on precision of input saw-tooth impulse generator. The slope of the saw-tooth impulse was changed from 4.10^2 to $8.10^2 \text{ V}\cdot\text{s}^{-1}$ and results of simulation showed maximal error equal to -0.033 LSB . In spite of such extreme error of

input saw-tooth impulse generator the error of measured INL remains in the range of a few hundredths of LSB.

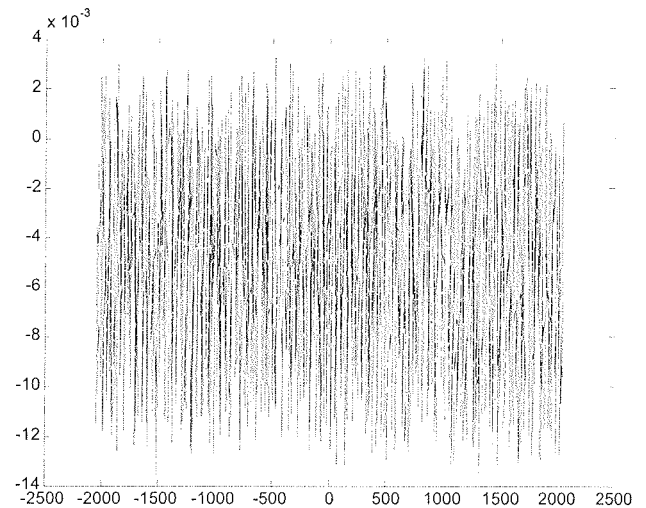


Figure 5. Absolute error of measured INL

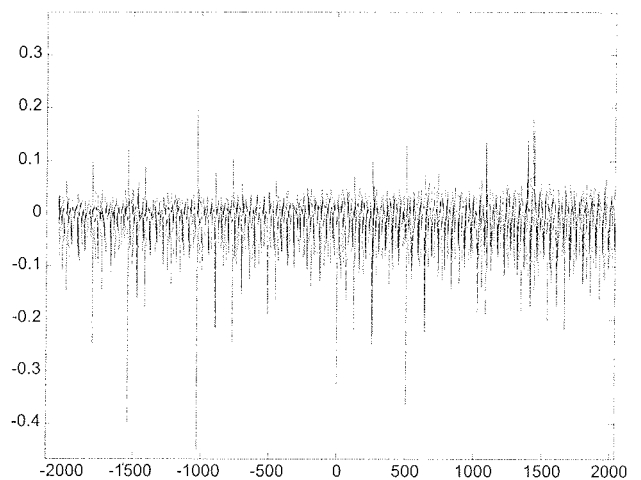


Figure 6. Resultant DNL characteristic of tested ADC

Other source of uncertainty that could be taken into account is the resistive divider. However, because, on the present the resistive dividers with relative error 0.01% are standardly produced, this source of uncertainty can be omitted. Also as to DAC, if its maximal INL and DNL is a few LSB_{DAC} at the output of resistive divider it is error only a few hundredths of LSB using 8 bit DAC. By using DAC with higher number of bits the situation can be only better.

The resultant DNL characteristic calculated by means of (5) is shown in Fig.6 and corresponding absolute error is in Fig.7.

As to test time, because $k= 4.10^2 \text{ V}\cdot\text{s}^{-1}$, $V_{max}= 9 \text{ V}$, $V_{min}= -9 \text{ V}$, the sampling period is 10^{-7} s and measurement range of tested ADC is to be passed 8 times to measure voltage vector \vec{V}_1 , and 8 times to measure vector \vec{V}_2 using 8 bit DAC, its value is 0.72 s .

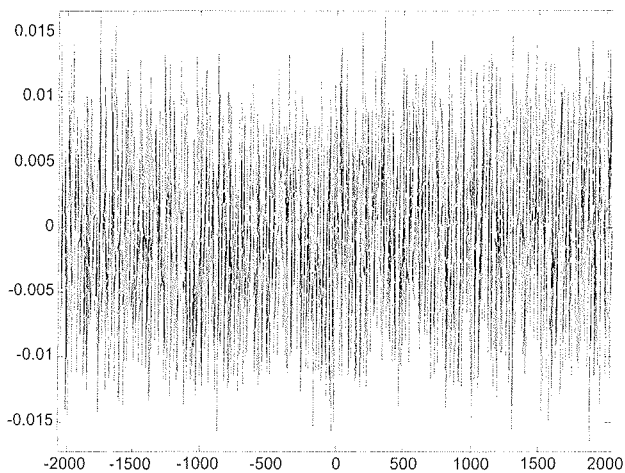


Figure 7. Absolute error of DNL

Conclusions

A new approach in testing ADCs has been presented. In comparison to ordinary approaches, decision levels of tested ADC are not measured to zero potential but to the decision levels of an additional ADC. Thus, there are not special requirements on precision of input signal generator. It has been shown that the precision of measured INL and DNL characteristic is in the range of a few hundredths of LSB. Very interesting is knowledge that the test system is immunized in face of input generator extreme errors.

References

/1/ Kuyel, T.: Linearity Testing Issues of Analog to Digital Converters. *IEEE International Test Conference*, pp.747-756, 1999.

/2/ European project DYNAD.: Methods and Draft Standards for the Dynamic Characterization and Testing of Analog-to-Digital Converters, published on web at: <http://www.fe.up.pt/~hsm/dynad>

/3/ IEEE Std. 1057-1994. *IEEE Standard for digitizing waveform recorders*. The institute of electrical and electronics engineers, Inc. New York, USA, 1994, p.80.

/4/ Michaeli, L.: *Modeling of Analog-to-Digital Interfaces*. Mercury-Smekal Press, Košice, p.160, 2001, (In Slovak).

Acknowledgements

This work has been supported by the Grant Agency of the Slovak Republic VEGA grant. No.1/9030/02 "Methods for testing of unconventional analog-to-digital converters and reducing their uncertainty".

Martin Kollár, MSc., Ph.D.
Department of Theory of Electrical Engineering and Measurement,
Technical University of Košice,
Park Komenského 3, 043 89 Košice, Slovakia.
Tel: +421-55-6022579;
Fax: +421-55-6023989
E-mail: Martin.Kollar@tuke.sk

Prispelo (Arrived): 09.08.2004 Sprejeto (Accepted): 30.08.2004