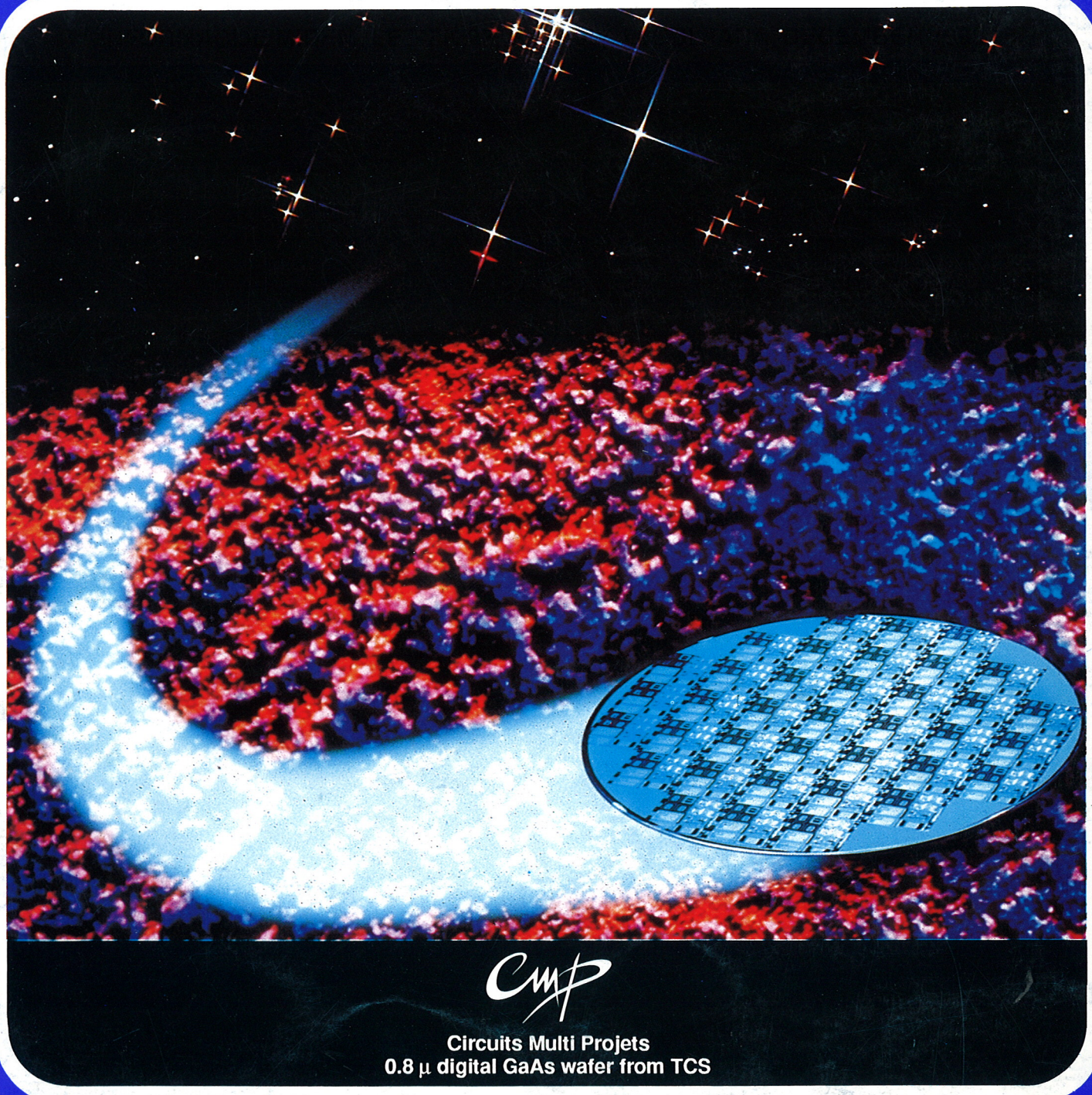
UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 4 ◦1993

Strokovno društvo za mikroelektroniko elektronske sestavne dele in materiale

Časopis za mikroelektroniko, elektronske sestavne dele in materiale
Časopis za mikroelektroniku, elektronske sastavne dijelove i materijale
Journal of Microelectronics, Electronic Components and Materials

INFORMACIJE MIDEM, LETNIK 23, ŠT. 4(68), LJUBLJANA, DECEMBER 1993



INFORMACIJE MIDEM 4 ° 1993

INFORMACIJE MIDEM	LETNIK 23, ŠT. 4(67), LJUBLJANA,	DECEMBER 1993
INFORMACIJE MIDEM	GODINA 23, BR. 4(67), LJUBLJANA,	DECEMBAR 1993
INFORMACIJE MIDEM	VOLUME 23, NO. 4(67), LJUBLJANA,	DECEMBER 1993

Izdaja trimesečno (marec, junij, september, december) Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale.
Izdaja tromjesečno (mart, jun, septembar, decembar) Stručno društvo za mikroelektroniku, elektronske sastavne dijelove i materiale.
Published quarterly (march, june, september, december) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Naslov uredništva
Adresa redakcije
Headquarters

Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 61000 Ljubljana, Slovenija
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Scientific Council for Technical Sciences of Slovene Ministry of Science and Technology has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials.
Publishing of the Journal is financed by Slovene Ministry of Science and Technology and by Society sponsors.

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Grafična priprava in tisk
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Printed by
BIRO M, Ljubljana

Naklada
Tiraž
Circulation
1000 izvodov
1000 primjeraka
1000 issues

I.Šorli: Društvo MIDEM in njegove dejavnosti	244	I. Šorli: MIDEM Society and its Activities
ZNANSTVENO STROKOVNI PRISPEVKI		PROFESSIONAL SCIENTIFIC PAPERS
MIEL-SD 93 VABLJENA PREDAVANJA		MIEL-SD 93 INVITED PAPERS
M.B.Johnson, H.W.M.Salemink: Rasterska tunelska mikroskopija presekov heteroslojnih polprevodnikov: Atomska ločljivost, sestava, fluktuacije in dopiranje	245	M.B.Johnson, H.W.M.Salemink: Cross-Sectional Scanning Tunneling Microscopy on Heterostructures: Atomic Resolution, Composition, Fluctuations and Doping
C.Cini: Mešana bipolarna - CMOS - DMOS tehnologija za pametna močnostna integrirana vezja	253	C.Cini: Mixed Bipolar-CMOS-DMOS Smart Power IC Technology
J.Furlan, W.Kusian, G.Conte: Tandemske amorfne silicijeve sončne celice	259	J.Furlan, W.Kusian, G.Conte: Tandem Amorphous Silicon Solar Cells
A.J.Williams, I.R.Harris: Magneti kovin prehoda in redkih zemelj: proizvodnja, lastnosti in uporaba	264	A.J.Williams, I.R.Harris: Rare Earth-Transition Metal Magnets: Their Processing, Properties and Applications
J.W.Ciognani, E.Gramegna, M.Wiegand: Pregled trenutnega stanja razvoja keramične in poliimidne tehnologije za multičip module	272	J.W.Ciognani, E.Gramegna, M.Wiegand: An Overview of Recent Developments in Ceramic and Polyimide Technologies for Multichip Modules
M.Maček: Pregled sodobnih postopkov mokrega čiščenja silicijevih rezin	275	M.Maček: A Review of Advanced Wet Cleaning
UPORABA POLPREVODNIŠKIH IN MIKROELEKTRONSKIH KOMPONENT		APPLICATION OF SEMICONDUCTOR AND MICROELECTRONIC COMPONENTS
J.Novak: Mikroelektronika v službi natančnega merjenja pomikov in zasukov. Integrirano vezje RLX 12510	284	J.Novak: Use of Microlectronic Technology for Exact Position and Shaft Measurements. RLX 12510 Integrated Circuit
KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA		CONFERENCES, COLLOQUYUMS, SEMINARS, REPORTS
M.Slokan, I.Šorli: 21.Mednarodna konferenca o mikroelektroniki, MIEL'93 in 29.Simpozij o elektronskih sestavnih delih in materialih, SD'93, 29.09. - 01.10.1993, Bled, Slovenija	285	M.Slokan, I.Šorli: 21st International Conference on Microelectronics, MIEL'93 and 29th Symposium on Devices and Materials, SD'93, 29.09. - 01.10.1993, Bled, Slovenia
ESSDERC 93	288	ESSDERC 93
D.Križaj: EPE - 5.evropska konferenca o močnostni elektroniki in njeni uporabi	289	D.Križaj: EPE - 5.th European Conference on Power Electronics and Applications
A.Zalar: ECASIA 93 - 5.evropska konferenca o uporabi metod za analizo površin in faznih mej	290	A.Zalar: ECASIA 93 - 5.th European Conference on Application for Surface and Interface Analysis
A.Cvelbar: ICTF 9 - 9.mednarodna konferenca o tankih plasteh	292	A.Cvelbar: ICTF 9 - 9th International Conference on Thin Films
A.Pregelj: 44.posvetovanje o metalurgiji in kovinskih gradivih ter 1. posvetovanje o materialih	293	A.Pregelj: 44th Symposium on Metallurgy and Metal Compounds and 1st Symposium on Materials
PREDSTAVLJAMO PODJETJE Z NASLOVNICE		REPRESENT OF COMPANY FROM FRONT PAGE
CMP servis	294	CMP Service
VESTI	301	NEWS
KOLEDAR PRIREDITEV	309	CALENDAR OF EVENTS
TERMINOLOŠKI STANDARDI	310	TERMINOLOGICAL STANDARDS
MIDEM prijavnica	315	MIDEM Registration Form
VSEBINA LETNIKA 1993	318	CONTENT - VOLUME 1993
Slika na naslovnici: CMP - Multičip servis; GaAs rezina z digitalnimi integriranimi vezji z minimalno razsežnostjo 0.8 μm izdelano v firmi TCS		Front page: CMP - Multi-Projets Circuits; 0.8 μm digital GaAs wafer from TCS

VSEBINA CONTENT

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- *publishing of the professional Journal - **Informacije MIDEM***
- *organization of professional seminars, workshops and colloquiums, as well as other publishing activities covering the field*

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Dr. Rudolf Ročak

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UDK 621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 23(1993)4, Ljubljana

CROSS-SECTIONAL SCANNING TUNNELING MICROSCOPY ON HETEROSTRUCTURES: ATOMIC RESOLUTION, COMPOSITION FLUCTUATIONS AND DOPING

M.B. Johnson and H.W.M. Salemink
IBM Research Division, Zurich Research Laboratory, Ruschlikon, Switzerland

INVITED PAPER
21st International Conference on Microelectronics, MIEL'93
29th Symposium on Devices and Materials, SD'93
September 29 - October 1, 1993, Bled, SLOVENIA

Key words: semiconductors, STM scanning tunneling microscopy, analysis, structural properties, chemical properties, electronic properties, spatial dimensions, atomic scale, nanometer scale, Al-Ga-As-Ga-As heterostructure, measurements, dopants, UHV ultrahigh vacuum, experimental results

Abstract: Cross-sectional scanning tunneling microscopy on semiconductor structures is evolving into a technique to analyze structural, chemical, and electronic properties on the atomic and nanometer scale in all spatial dimensions, in particular in the lateral and in-depth spatial dimensions of the structure. This technique has been used on the ultrahigh vacuum cleaved (110) plane of (001)-grown AlGaAs/GaAs heterostructures. We report on measurements of i) interface roughness, as well as alloy fluctuations and ordering; ii) the variation of electronic properties over an interface as well as fluctuations within the alloy; and iii) the distribution of individual dopant sites.

Rasterska tunelska mikroskopija presekov heteroslojnih polprevodnikov: atomska ločljivost, sestava, fluktacije in dopiranje

Ključne besede: polprevodniki, STM mikroskopija skanirna tunelna, analiza, lastnosti strukturne, lastnosti kemične, lastnosti elektronske, dimenzije prostorske, skala atomska, skala nanometerska, Al-Ga-As-Ga-As heterostrukture, meritve, dopanti, UHV vakum ultravisoki, rezultati eksperimentalni

Povzetek: Rasterska tunelska mikroskopija presekov polprevodniških struktur se razvija v tehniko, ki bo sposobna analizirati strukturne, kemične in elektronske lastnosti na atomski in nanometrski skali v vseh prostorskih dimenzijah, še posebej v lateralni in vertikalni prostorski dimenziji raziskovane strukture. Omenjeno tehniko smo uporabili na vzorcih AlGaAs/GaAs z orientacijo (001) na površini razcepljeni v smeri (110) in pripravljeni v ultravisokem vakuumu. V delu prikazujemo meritve i) hrapavosti površine kakor tudi fluktuacijo urejenosti in sestave legure, ii) spremembe elektronskih lastnosti po površini kakor tudi znotraj legure in iii) porazdelitev posameznih atomov dopantov

1. Introduction:

As semiconductor devices become smaller, knowledge of the electronic properties on the nanometer scale and of the crystallographic and chemical structure on the atomic scale will be of paramount importance in all dimensions. However, conventional analytical tools do not readily afford this knowledge on such a scale. For example in molecular beam epitaxial (MBE) growth, electron diffraction is usually used during epitaxy to monitor the layer-by-layer growth,[1] whereas high-resolution transmission electron microscopy (TEM)[2] and X-ray diffraction[3] are used to determine the structure after growth. These techniques, however, produce crystallographic information averaged over many lattice unit cells. The electronic parameters of such structures are often derived from photoluminescence[4] and photoemission[5] which measure semiconductor properties related to the band structure (eg. valence-band offset and band gap), including their variation across interfaces, but again averaged over many lattice unit cells in volume or a large surface area. Analysis of electronic properties of device structures by capacitance-voltage (C-V) or current-voltage (I-V) probes and spreading resistance profiling (SRP) require modeling and are difficult to extend to the lateral dimensions.[6] Similarly, analysis of electronic properties of devices by means of the device performance itself requires sophisticated modeling, and the determination of the physical characteristics is difficult. Finally, chemical profiling techniques such as secondary ion mass spectroscopy (SIMS) and Auger electron spectroscopy (AES) are limited to a depth resolution in the range of 5 nm and are difficult to extend to lateral dimensions.[6] On the other hand scanning tunneling microscopy (STM)[7-9] is an extremely surface- sensitive tool with atomic lateral res-

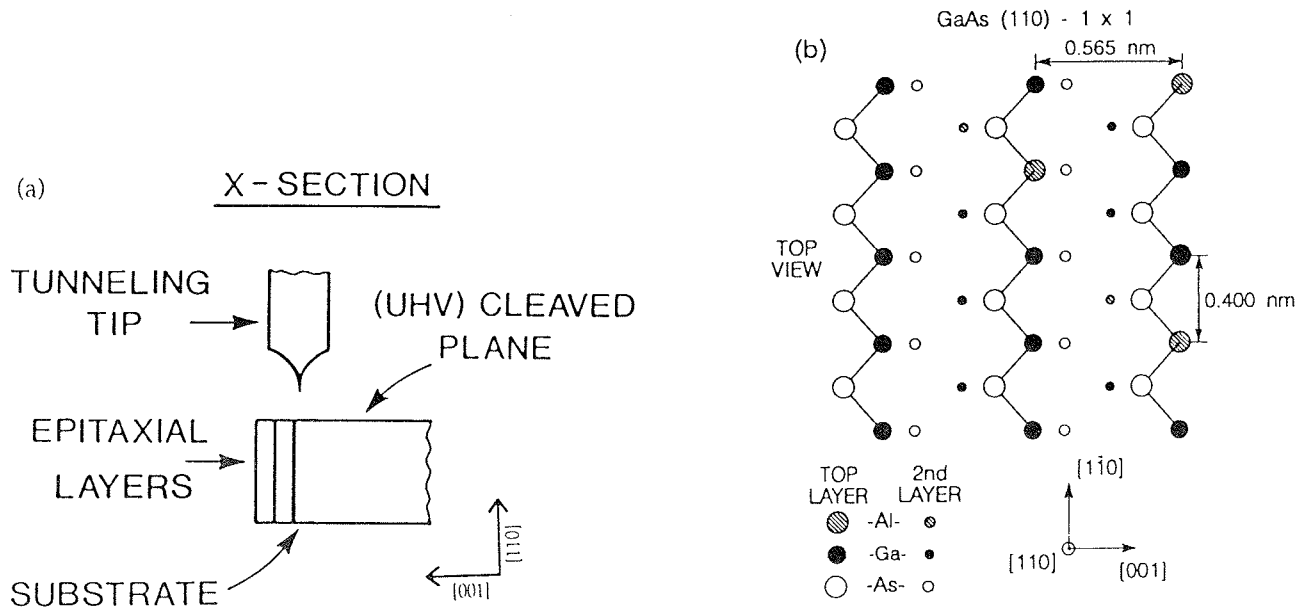

Fig. 1: (a) Sketch of cross-sectional STM on heterostructures. /© 1991 Elsevier Science Publishers B.V./ (b) Top view of atomic arrangements of the group-III Ga and Al and group-V As sites on the (110) face. Tunneling can be out of the group-V valence As states or into the group-III conduction states by negative and positive sample voltage. The [001] and [110] directions and dimensions are shown. The distance to the next monolayer in the (110) plane is 0.2 nm. /© 1990 John Wiley & Sons, Inc./

olution and sensitivity to crystallographic, chemical and electronic information. Thus when used on a suitable cross-sectional surface, STM can yield structural, chemical, and electronic information in the depth and lateral dimensions with unprecedented resolution. Hence there is growing interest in the analysis of epitaxially grown multilayers by cross-sectional STM (XSTM).[10-18] Figure 1(a) shows the XSTM configuration. The preparation of this cross-sectional surface is a crucial requirement for successful application of XSTM. The best results require an atomically flat, uncontaminated surface. This is readily achieved in the III-V materials system with a (110) facet cleaved in ultrahigh vacuum (UHV). The work of this paper concerns AlGaAs/GaAs heterostructures (see Fig. 1(b)) where we demonstrate: i) spatial resolution and chemical sensitivity on an atomic scale, which allows the measurement of interface roughness, as well as alloy fluctuations and ordering; ii) electronic sensitivity on a near-atomic scale, which allows the measurement of the variation of band structure within alloys and across interfaces; and iii) the direct sensitivity to dopants, which allows the determination of dopant density. The extension of this work to other heterostructure systems, such as Si and SiGe, depends principally on the generation of a cross-sectional surface that is atomically flat and uncontaminated.

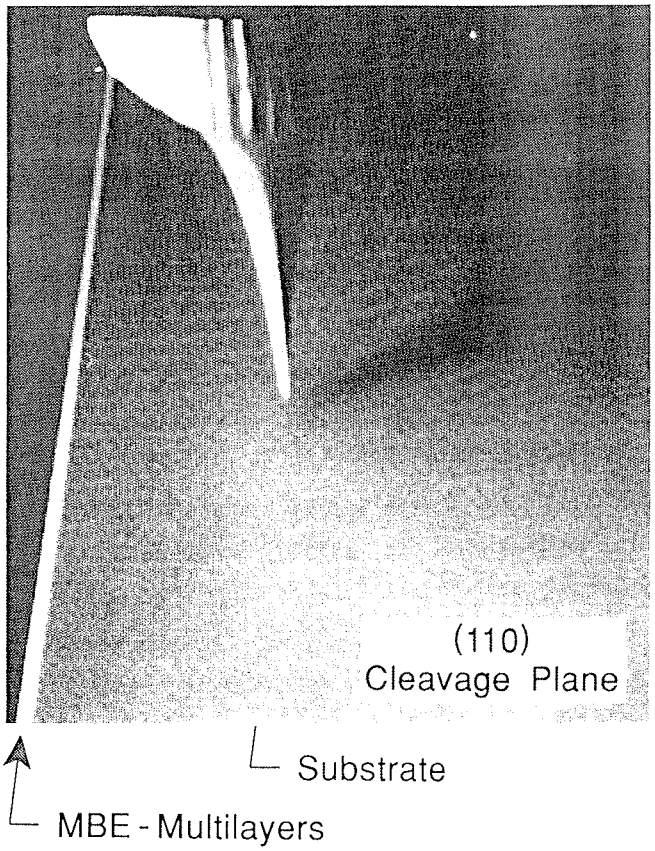

Fig 2: Secondary electron SEM image of tunneling tip in approach to cleaved multilayer stack. In the (110) cleaved cross section, the multilayer stack is seen as a white stripe to the left of the (gray) substrate (see also Fig. 1a). Note the tip shadow on the substrate due to blocking of the electron beam. This effect at close proximity ($\cong 1.0\ \mu m$) is used to guide the tip towards the multilayer stack (SEM magnification factor is 10 K).

2. Experimental

The results described in this paper are obtained with two UHV-STM's: one early system built into a UHV-compatible SEM (scanning electron microscope),[19] and a second version with optical access instead of the SEM. Both STM's have been successfully used to study cross

sections of nanometer-size, MBE-grown multilayer structures. The SEM is used for three purposes: i) to evaluate the apex shape of the tunneling tip, ii) to analyze the suitability of the particular cleavage plane under study and iii) to guide the STM tip into the area of interest within the heterostructure stack, typically with a positional accuracy of 25 nm. Figure 2 shows an SEM image of the tunneling tip in approach to the cleaved sample. An iterative method for guiding the tip to the edge[18] using reliable positioning piezo-sliders as well as more reliable tip preparation and sample cleaving methods have largely replaced the use of SEM in recent work. Pressure in the STM environments is $<4 \times 10^{-11}$ mbar. The GaAs/AlGaAs multilayer samples were grown by MBE on (001) GaAs substrates. The results described here are for highly-doped p-type (Be) samples with dopant concentration ranging from 1 to -10 x 10^{18} cm^{-3} and Al concentration in the alloy typically $Al_xGa_{1-x}As$ with x=0.30 to 0.35. Various different structures are used in the stack, and several repetitions of the stack are grown to facilitate the location of the structure of interest. Atomic resolution on III-V heterojunctions became routine after several improvements were made, notably i) thinning back the substrate to 150 μm by mechanical polishing (to facilitate the (110) cleaving across the stack), ii) use of lower tunneling current (0.1 nA or lower) and more highly doped samples and iii) optimization of the tip preparation procedure.[20]

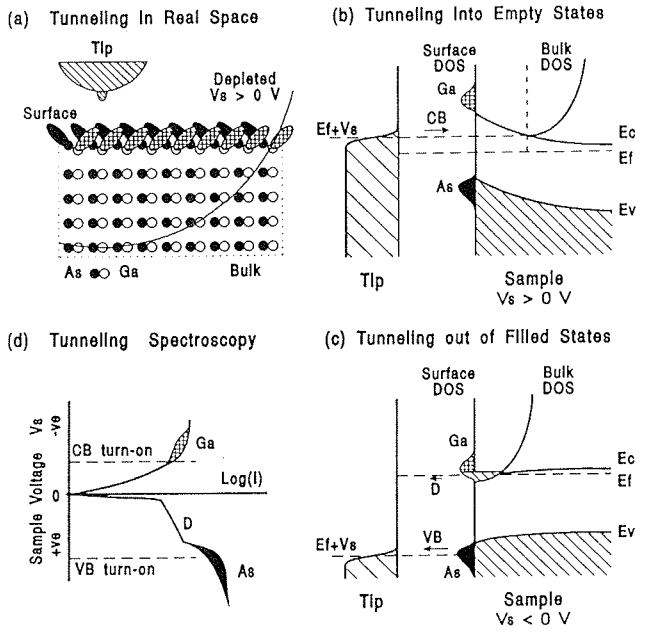

Fig 3: Schematic views of STM tunneling on n-type GaAs (clockwise). (a) Tunneling between tip and sample in real space. (b) Tunneling energy diagram for sample voltage > 0 sensitive to empty Ga and Al states; also sketched is the tip-induced band-bending with the semiconductor in depletion. (c) Tunneling energy diagram for sample voltage < 0 sensitive to filled As states; also sketched is the tip-induced band-bending with the semiconductor in accumulation. (d) Schematic current-voltage characteristic with contributions from VB and CB; D shows tunneling via dopant levels. From /26/.

The atomic arrangement on the (110) cleavage plane (top view) is drawn in Fig. 1(b). Note that for AlGaAs material a fraction of the group-III sites is replaced. On the charge-neutral (110) plane the group-III and V atoms maintain their valence character. As a result the filled (group V) and empty (group III) states can be sensed by tunneling out of or into the sample[8] as shown in Fig. 3. In addition the valence and conduction band (VB and CB) turn-ons can be determined with respect to E_F via simultaneous current voltage spectroscopy.[21, 22] Spectroscopy on the clean UHV cleaved III-V (110) surface displays both VB and CB band onsets and a gap region of approximately 1.45 eV, free of surface states, as reported previously.[21]

3. Results and Discussion

In this work we describe four different sets of STM measurements, each associated with various aspects of GaAs/AlGaAs heterostructures. They are: i) filled-state images that show Al sensitivity and hence interface roughness as well as alloy fluctuations and ordering. Furthermore these images allow the determination of the layer metrology by STM and this is compared to that obtained with HRTEM; ii) filled-state images in combination with I-V spectroscopy that are sensitive to the variation of the band structure across a AlGaAs/GaAs interface and within the AlGaAs layer; and iii) filled-state images of a Be-doped GaAs buffer layer, of a Zn-doped GaAs substrate, and of a Be-doped sample with variable doping concentrations that are directly sensitive to the electronically active dopant atoms and allow the direct measurement of dopant density.

An STM image of a heterostructure stack consisting of a series of adjacent, equally thick pairs of $Al_{0.3}Ga_{0.7}As$/GaAs layers of 10, 5, 2, and 1 nm thickness is shown in Fig. 4./see Ref. 23/ Figure 4(a) shows the bulk-band diagram for the stack. Figure 4(b) shows an area of nearly 30 x 50 nm with all layers in one period of the stack clearly displayed. The image was taken with a sample voltage of -2.1 V and a demand current of 0.1 nA, thus probing the As-related filled states.[8] Note that atomic corrugation is apparent in both the [001] and [110] directions. In the image in Fig. 4(b) the GaAs regions are uniform, while the AlGaAs ternary regions have a mottled texture.[24] Several types of localized features are present in the layers, but the discussion here concerns the clean regions. Figure 4(c) shows that the topographic corrugation on line C-C' of Fig. 4(b) extends through one period of the stack along the [001] direction away from localized contamination features. In the GaAs regions the corrugation is regular with an amplitude of 0.03 nm, while in the 10 and 5 nm thick AlGaAs layers the corrugation is irregular and the layers appear nearly 0.1 nm lower than the surrounding GaAs. The smaller 2 and 1 nm thick AlGaAs layers are observ-

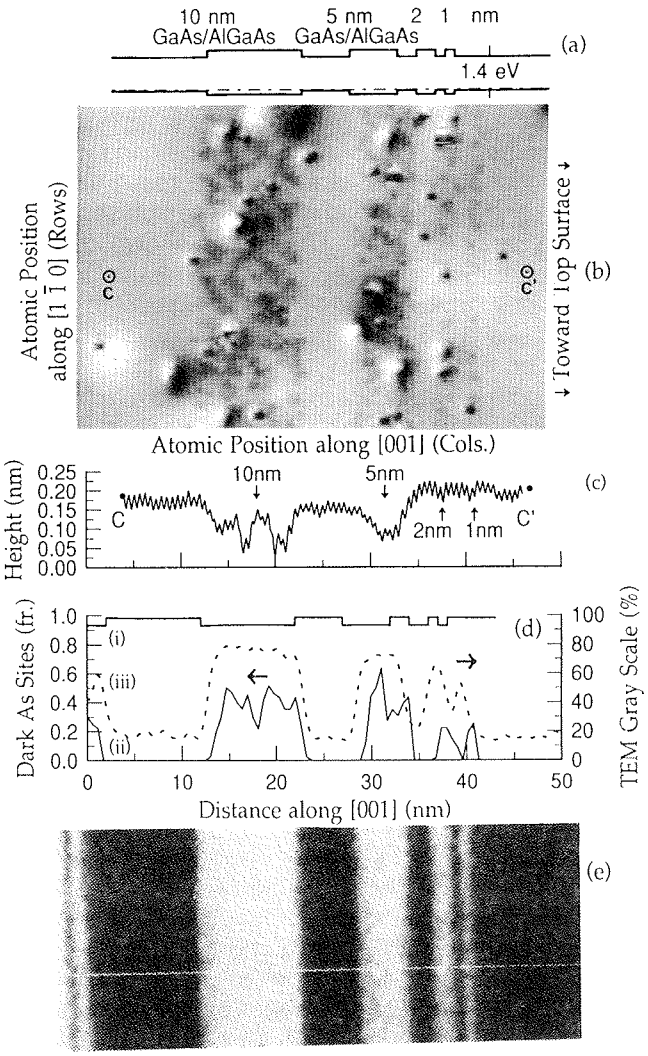

Fig. 4: Large-scale STM image of a (110)-cleaved GaAs/AlGaAs heterostructure stack. (a) Calculated bulk-band structure for the as-grown heterostructure. (b) Topographic image of the stack taken with a sample voltage of -2.1 V and a demand current of 0.1 nA. The image is nearly 50 x 50 nm and the As sublattice is indexed along the [110] and [001] directions. The relative tip height is represented by a gray scale, from 0 (black) to 0.43 nm (white). (c) Topographic corrugation along line C-C' in registry with that displayed in (b). (d) Comparison of STM with dark-field TEM. (i) Intended growth plan. (ii) TEM gray scale across layers from dark- field image (e) (iii) Fraction of dark As sites along a [110] corrugation line in the neighborhood of C-C' versus position along the [001] direction. (e) TEM dark-field image of the stack in registry with (d). From /23/.

able, but their contrast is much less than that of the two thicker layers. Note that this height variation is not real topography because there are no atomic steps on the surface; instead, it is electronic in nature. The regular corrugation in the GaAs is the result of the homogeneous As surface site bonding configuration there. In contrast, the bonding configuration of As surface sites in the ternary AlGaAs is variable depending on the number of Al nearest-neighbor sites. Because the Al-As bond is more ionic than the Ga-As bond, Al nearest-neighbors result in more charge being transferred to the nearest As sites, thereby lowering the energy and changing the spatial extent of the As-related surface state. Thus the As corrugation fluctuates depending on the number of Al atoms bonded to the surface As. Conversely the fluctuation of the As corrugation indicates a variation of the number of Al atoms bonded to the surface As. The apparent topographic lowering in the thicker AlGaAs layers is the result of the different electronic properties of the barrier region; it most probably occurs because the barriers are completely depleted, which requires the tip to approach the surface. The distance over which this apparent height varies from GaAs to the AlGaAs - about 3-4 [001] corrugations - and the lack of contrast in the 1 and 2 nm barrier is consistent with the expected wave function penetration of the holes from the quantum wells into the barriers that result from the near-atomic scale variation of band offsets.

Figure 5 shows an expanded image of the 10 nm thick AlGaAs layer. The occurrence of dark or light bands 3-4 lattice spacings in width (about 2 nm) extending in the [112] and [1̄12] directions is clearly visible (it is also displayed in parts of the 5 nm layer). This suggests that

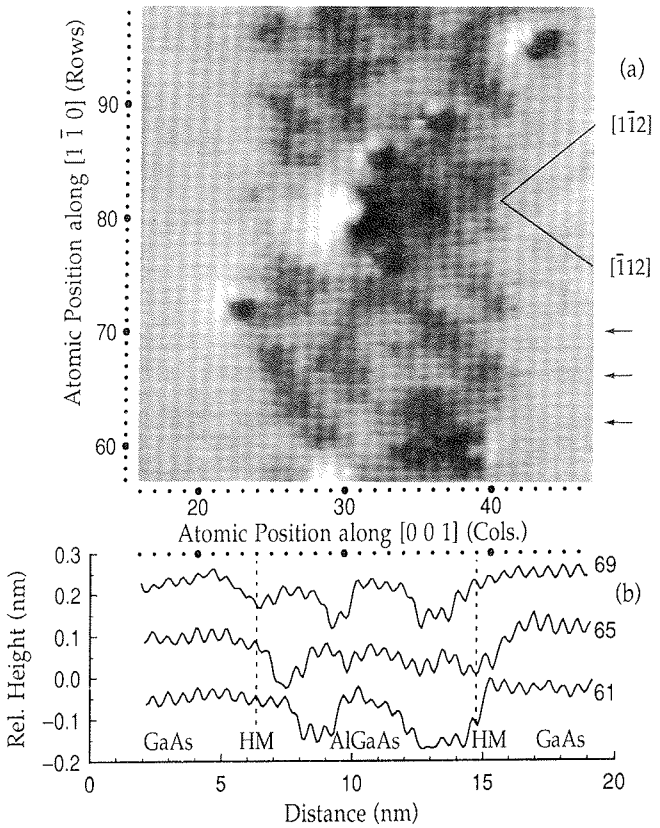

Fig. 5: Expanded STM image of 10 nm AlGaAs layer in Fig. 4 (a) Topographic image of an area of about 20 x 20 nm; relative tip height represented by a gray scale from 0 (black) to 0.38 nm (white). The [112] and [1̄12] directions are indicated. (b) Topographic line scans along rows 61, 65, and 69 as indicated. The positions of the half- maximum of the AlGaAs layer are indicated by HM. From /23/

Al-rich regions nucleate at the GaAs/AlGaAs interface in isolated positions and grow preferentially. The interfaces shown in Fig. 5 also have roughness on this 2 nm length scale. This is in agreement with measurements made by other techniques.[2]

Finally, we consider quantitative metrology of these layers on the (sub-)nanometer scale. Let us consider selected contamination-free regions in the image in Fig.4(b) that span the entire superlattice period in a piecewise manner near line C-C'. From these regions we can determine the fraction of dark As sites along the [110] row in this area. In Fig. 4(d) curve (iii) shows this fraction of dark As positions plotted versus its position along the [001] direction - typically more than 30 sites per vertical line are counted. This fraction of dark As positions is indicative of the Al fraction, and is sufficient for estimating the actual thickness of the layers grown, as shown. Curve (ii) is the percentage gray scale from the TEM dark field image shown in Fig. 4(e) which is also indicative of Al content. And finally, curve (i) indicates the intended growth plan for the stack. Comparing curves (ii) and (iii) (STM and TEM) shows 4% agreement in the layer thickness's which is reasonable, considering that different parts of the wafer were measured. Note the TEM and STM-measured GaAs layers are systematically longer than the matching AlGaAs layer.

Local I-V curves can be acquired simultaneously with the topography to assess the transition in the electronic band structure across the GaAs- AlGaAs interface. /see Ref. 22/ In Fig. 5(a) the filled-state image of an interface is shown together with the sampling points for the I-V curves at a 1.5 nm grid. In the interest of high stability in spectroscopy, topographic resolution is traded off slightly. A set of I-V curves from a line across the interface is shown in Fig. 5(b) and the transition region is noted by the drop in the VB turn-on voltage. The observed VB turn-on energy is plotted as a function of distance to the interface in Fig. 5(c) together with the calculated positions for the bulk (C) and surface (S) VB edge energy. The tip-induced electrostatic depletion of the semiconductor is explicitly taken into account in curve (S).[22] The lack of change at the CB onset is somewhat surprising and possibly due to interference with surface states. Note the fluctuations in the VB edge in the AlGaAs from the experimental data: this might reflect the local variation of the VB edge energy due to the Al fluctuations (Fig. 4) and the effect of the lateral extent of the depletion region present during spectroscopy measurements /.Fig. 1(a)/. The data in Fig. 5 demonstrate the measurement of electronic band parameters on a near-atomic scale in semiconductor structures.

Figure 7 shows a filled-state image of a Be doped p-type GaAs MBE-grown buffer layer with p =1 x 10^{19} cm^{-3}. /see Ref. 25/ Nine hillock features are observed scattered throughout the 31 x 29 nm scan and labeled on the perimeter of the image. Figure 7(b) shows corrugation traces across several of these hillock features in [001] and [110] directions. In Fig. 7(b) the hillocks have a height of up to 0.02 nm and a diameter of about 2

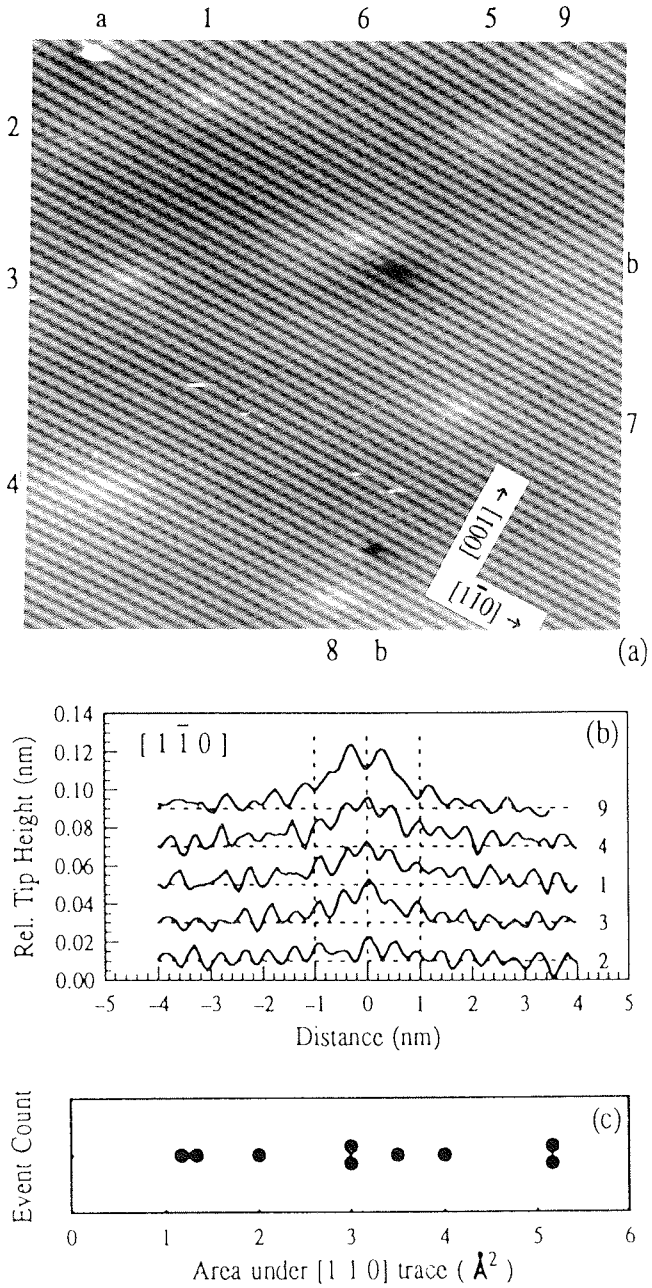

Fig. 7: (a) STM image of a (110)-cleaved, 1 x 1^{19} cm^{-3}, Be-doped GaAs surface. Image displays 31 x 29 nm of the As sublattice taken with sample voltage -2.1 V and demand current 0.1 nA. The relative tip height is represented by a gray scale from 0 (black) to 0.2 nm (white). Nine hillocks (dopants) are identified using numbers at the closest point on the perimeter. (b) Tip height traces along the [110] direction of a selection of the hillocks identified in (a). (c) Scatter plot of area under the [110] tip height traces (integrated intensity) of all nine hillocks - note the uniform distribution. From /25/

nm.[25,26] These hillocks correspond to the enhancement of the surface density of states expected in the neighborhood of Be acceptor sites which gives rise to a slight increase of the tip-surface distance as observed. The observed diameter - roughly the size of the acceptor

Bohr radius (2.5 nm) - and height of these hillocks are in agreement with calculations of the change in the surface density of states due to a nearby dopant and its effect on tunneling process. At a doping density of 1 x 10^{19} cm^{-3} in the area shown in Fig. 7(a) one expects two dopant atoms per monolayer. Thus the observation of nine hillocks indicates a sensitivity to dopant atoms in the top five monolayers corresponding to about 1 nm (the distance between monolayers is 0.2 nm in the [110] direction). This is in agreement with the acceptor Bohr radius and the calculations described above.[27]

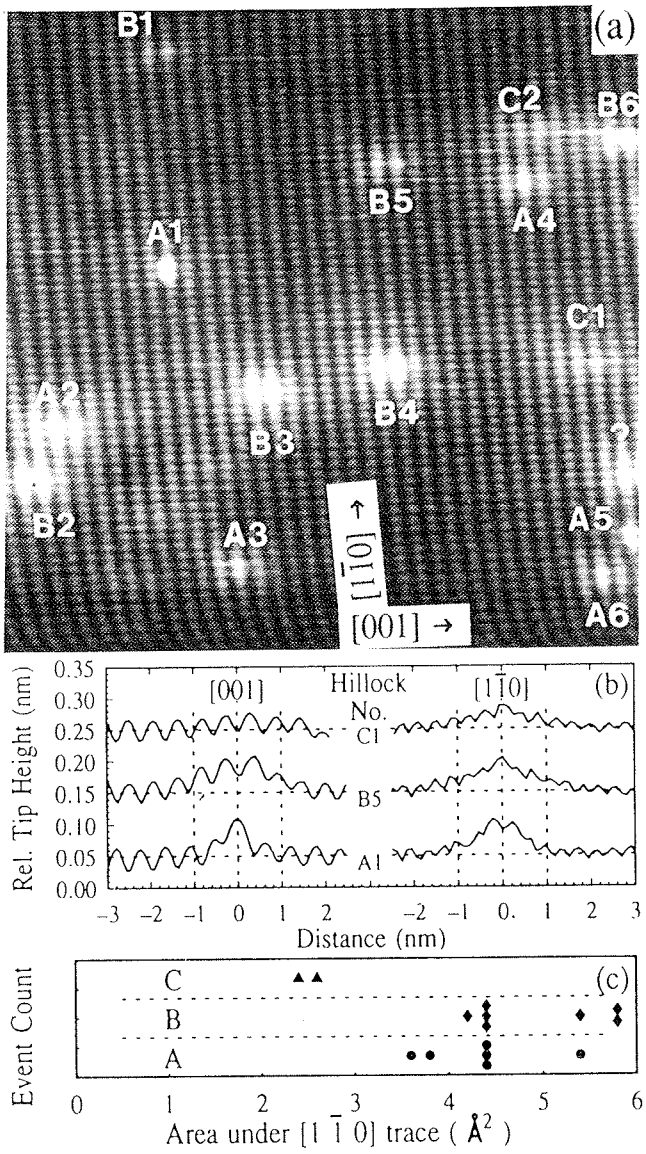

Fig. 8: (a) STM image of a (110)-cleaved, 5 x 10^{19} cm^{-3}, Zn-doped GaAs surface. Image displays 20 x 28 nm of the As sublattice taken with sample voltage -2.1 V and demand current 0.1 nA. The relative tip height is represented by a gray scale from 0 (black) to 0.2 nm (white). Six type A hillocks, six type B hillocks, and one type C hillock are identified with numbers. (b) Tip height traces along the [110] and [001] directions of a selection of the hillocks of type A, B, and C identified in (a). (c) Scatter plot of area under the [110] tip height traces (integrated intensity) or all hillocks labeled. From /25/

Figure 8 shows a filled-state image of a very highly-Zn doped p-type GaAs substrate buffer layer with p =5 x 10^{19} cm^{-3}. /see Ref. 25/ Many hillock features are scattered throughout the 20 x 28 nm scan. The prominent hillock features are labeled A, B and C according to their symmetry. Corrugation traces of examples of each of these types of hillock in [001] and [110] directions are shown in Fig. 8(b). The diameter and height of these hillocks are similar to those observed above for the Be-doped buffer layer. Moreover in this case, the number and symmetry of the features indicate that hillock feature A corresponds to a dopant in the top layer, feature B to a dopant in the second layer and C to a dopant in a still deeper layer. Thus the dopant can be localized in all three dimensions with atomic precision.

An STM image of a heterostructure modulation-doped stack consisting of 100 nm thick layers of Be-doped GaAs between 2.5 nm thick AlGaAs marker layers is shown in Fig. 9. /see Ref. 28/ Figure 9(b) is a large-scale STM image and (c)-(f) present a series of depth profiles (along the growth direction) over a single set of the modulation-doped layers. Figure 9(b) shows the 100 x 50 nm STM topographic image of a set of GaAs layers including the AlGaAs marker layers (spotted dark vertical lines) imaging the filled As states. Above and in registry with Fig. 9(b), Fig. 9(a) shows the intended growth plan including Be concentration, growth interruptions (marked GI), and the delta-doped layer (marked δ). Figure 9(c) shows several horizontal line scans taken across Fig. 9(b) at the positions indicated. Note that atomic corrugation is observed throughout the STM image as indicated in the inset (enlarged 5x). In the STM image /Fig. 9(b)/ the dark spots are cleave-induced As vacancies[5] and are not of interest here. The white spots indicate individual ionized dopants in the top several atomic layers. They are typically 2 nm in diameter and about 0.05 nm in height as shown above. The overall contrast - dark in the middle and bright on the sides - is due to the tip approaching the sample by about 0.1 nm in the low doped region in the middle of the image as indicated by the line scans in Fig. 9(c). Figure 9(f) shows SIMS and C-V profiles of a typical set of the GaAs layers between the AlGaAs markers. Figure 9(d) plots a line scan corresponding to the average of all the line scans making up the top half of the image in Fig. 9(b). Figure 9(e) is a histogram plot of the white spots (ionized dopant sites) counted in 10-nm- wide vertical stripes between the marker layers versus horizontal position along with the SIMS data (dotted) for comparison. The disagreement between the intended doping and the SIMS data is due to the segregation to the surface, and to bulk diffusion of the Be during growth. The SIMS plot is thought to reflect the actual Be concentration. Figure 9(d) shows qualitative agreement between the linear plot of the average tip height and the logarithmic plot of the Be concentration. The average tip height is sensitive to the dopant concentration because the surface band bending under the tunneling tip that affects the tip height is governed by the dopant concentration. The histogram of the Be dopant sites in Fig. 9(e) shows quantitative agreement with the SIMS Be concentration. This agree-

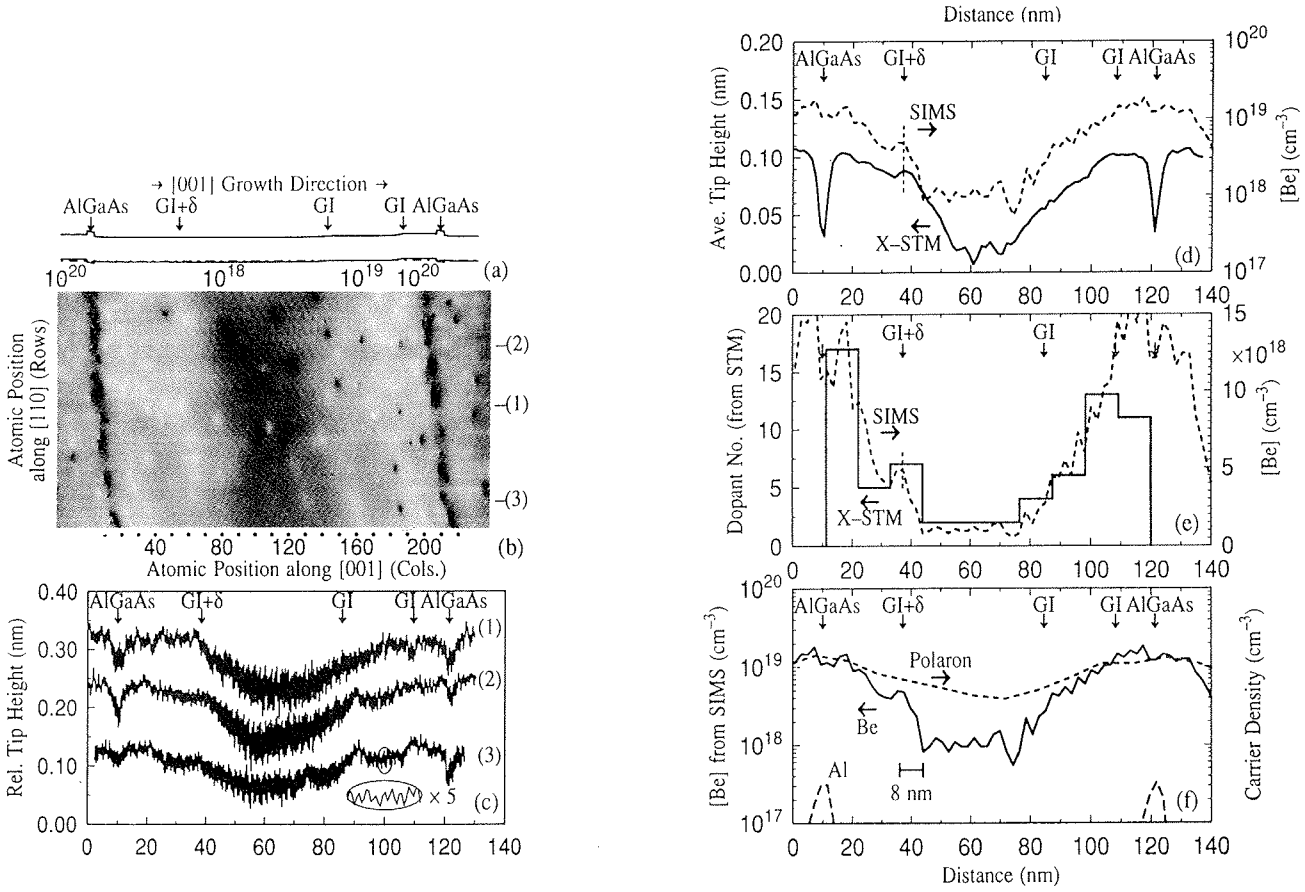

Fig. 9: Large-scale STM image of GaAs layers with variable dopant concentration and various depth profiles. (a) Calculated bulk-band structure for the intended heterostructure. In registry below, (b) shows the topographic image, 100 x 50 nm in size, of the layers taken with sample voltage -2.1 V and demand current 0.1 nA. The relative tip height is represented by a gray scale from 0 (black) to 0.2 nm (white). (c) Several topographic line scans across the image (b) along the [100] direction with the AlGaAs layers vertically aligned.Note the atomic corrugation shown in inset. (d) Line scan (solid) corresponding to the averaged line scan over the top half of Fig. 1(b) taking the slight drift into account. The line scan is smoothed slightly to remove atomic corrugation and is compared to the Be concentration measured by SIMS (dotted, right log. axis). (e) Dopant histogram determined by counting the white hillocks (dopants) in a series of rectangles across (b) (solid, left linear axis) and compared to the measured Be concentration measured by SIMS (dotted, right linear axis). (f) Be concentration (solid) and Al counts (dotted) measured by SIMS as well as dopant concentration determined by Polaron C-V analysis (dashed). From /28/

ment is for a sensitivity of the STM to the top 1 nm as was observed above. Thus both the dopant number and the relative tip height can be used to indicate the dopant concentration. The former shows the actual position of the dopant while the latter shows the behavior of the bands at the surface which is sensitive to the carrier concentration. Note the weak signature of the delta-doped layer is observed in the SIMS profile, the average tip height profile in Fig. 9(d), and dopant number histogram in Fig. 9(e). Thus STM appears to be an ideal tool for the study of such delta-doped layers.

4. Summary

Cross-sectional STM on heterostructures is evolving into a technique to analyze structural and electronic properties on the atomic and nanometer scale in all spatial dimensions. Because of the cross-sectional aspect involved, this represents both lateral and in-depth spatial dimensions. Other conventional techniques average one or more dimensions over a given length scale. In this work on the (110) plane of (001)-grown III-V heterostructures this high-resolution capability has been used to measure directly: i) interface roughness as well as alloy fluctuations and ordering; ii) the variation of electronic properties over an interface as well as fluctuations within the alloy; and iii) the distribution of individual dopant sites. In the future, such issues as incorporation of bulk and delta doping as well as their interdiffusion in III-V materials can be investigated. The extension of this technique from III-V materials to other heterostructure systems, such as Si and SiGe structures, is critically dependent on the preparation of a suitable cross-sectional surface.

Acknowledgments

We acknowledge the MBE growth provided by H.P. Meier, expert sample preparation by L. Perriard and H. Richard, technical assistance from U. Maier, STM software provided by B. Michel, transmission electron microscopy provided by R. Broom, and SIMS analysis provided by F. Cardone.

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Prispelo (Arrived): 11.12.93 **Sprejeto (Accepted): 23.12.93**

UDK 621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 23(1993)4, Ljubljana

MIXED BIPOLAR-CMOS-DMOS SMART POWER IC TECHNOLOGY

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SGS - THOMSON Microelectronics, Milano, Italia

INVITED PAPER
21st International Conference on Microelectronics, MIEL'93
29th Symposium on Devices and Materials, SD'93
September 29 - October 1, 1993, Bled, SLOVENIA

Key words: semiconductors, integrated circuits, BCD technology, power transistors, bipolar transistors, CMOS circuits, DMOS circuits, power ciircuits, signal circuits

Abstract: First introduced in the mid eighties, mixed bipolar-CMOS-DMOS (BCD) smart power IC technology has brought significant advances in the art of integrating signal and power circuits on the same chip. This paper describes the origin and evolution of the BCD technology family from the beginning to the present day, using as examples some practical integrated circuit designs that exploit effectively its benefits.

Mešana bipolarna - CMOS - DMOS tehnologija za pametna močnostna integrirana vezja

Ključne besede: polprevodniki, vezja integrirana, BCD tehnologija, transistorji močnostni, transistorji bipolarni, CMOS vezja, DMOS vezja, vezja močnostna, vezja signalna

Povzetek: Od sredine osemdesetih let, ko se je prvič pojavila, pa do danes, je mešana bipolarna - CMOS - DMOS (BCD) tehnologija omogočila izreden napredek in prinesla nove možnosti pri integraciji digitalne in močnostne elektronike na enem čipu. V tem prispevku opisujemo začetke in razvoj družin BCD tehnologij do danes. Obenem predstavljamo nekaj načrtanih in izdelanih integriranih vezij kot praktične primere vseh možnosti, ki jih ta tehnologija ponuja.

INTRODUCTION

In the early eighties power integrated circuits were produced using pure bipolar technology. These devices, mainly operating in switching mode, were severely limited by the poor efficiency of bipolar power transistors. This poor efficiency meant that a significant amount of power was dissipated inside the device, and since there is a limit to the dissipation capacity of an IC package this represented a fundamental limitation on the delivered power available. Pure bipolar power ICs suffer from another limitation: the poor density of bipolar logic.

Clearly the answer to these problems was to use DMOS/CMOS technology. DMOS power devices solved the dissipation problem, while CMOS provided very high density signal circuits. However, at the same time it was necessary to guarantee the high-precision analog performance that only bipolar technology can provide. Consequently the ideal solution was to combine bipolar, CMOS and DMOS on the same chip. This was achieved by SGS-THOMSON in 1986 with the introduction of a new technology called Multipower-BCD.

While most smart power IC processes are created by adding power elements to an existing signal process or vice-versa, "BCD" technology emerged from a project to develop a completely new, optimal process. Borrowing elements from junction- isolated IC technology and discrete DMOS technology, it allowed the integration of bipolar, CMOS and DMOS structures on the same chip (figure 1).

IC technologies combining power DMOS with signal circuits had existed previously, but where this technology differed lay in the use of isolated DMOS power transistors having all of the contacts on the top surface. In contrast, other processes used discrete-type DMOS structures where the lower surface of the die is the drain contact, so that two or more DMOS devices can only be placed on the same chip if they have a common drain contact. In contrast, with Multipower-BCD designers were free for the first time to integrate any number of DMOS power transistors connected in any way including bridge configurations.

In the first version of BCD technology, now called BCDI, the minimum breakdown voltage was specified at 60V, a figure defined by the original target application of the

MULTIPOWER BCD 20/60 II

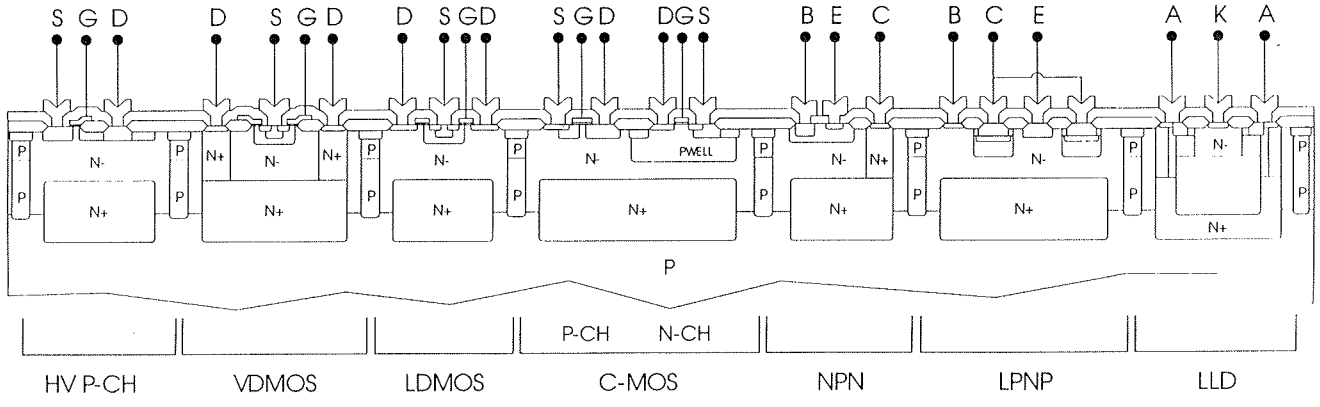

Fig. 1 *"BCD" technology, developed in the mid-eighties, combined vertical DMOS and junction isolation technologies. Since the DMOS transistors are fully isolated and have all contacts on the top surface any kind of power stage can be integrated.*

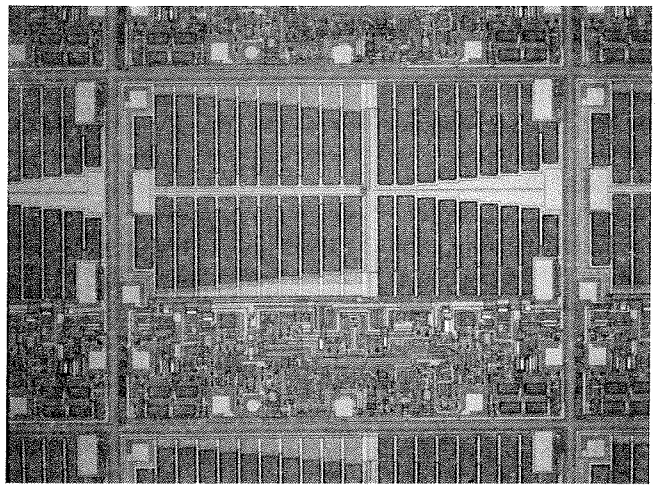

Fig. 2 *Because BCD technology allows the integration of isolated DMOS transistors it became possible to realize integrated circuits like this H bridge motor driver, the first BCD IC to be marketed.*

technology. BCDI was developed at a time when most smart power devices were used in applications like motor and solenoid driving in computer peripherals, where supplies for 30-50V are commonly used.

The first commercial product to be developed using this technology was the L6202 H-bridge motor driver (figure 2). A bipolar bridge with identical power performance was designed at the same time for the purpose of comparison. Both chips operated on 48V supplies and delivered 1.5A continuous output current. But while the L6202 was assembled in a DIP package and needed no heatsink, its bipolar counterpart needed a power package and a hefty heatsink. Eliminating this heatsink was a dramatic demonstration of the importance of reduced dissipation in power ICs.

There were other advantages in favor of the BCD version, too. Since a DMOS power stage has intrinsic recirculation diodes no external discrete diodes were needed, saving components. Moreover, the BCD version offered CMOS logic, which allowed designers to consider the use of complex logic in power ICs.

Though the BCD IC had many advantages over a bipolar equivalent it should be emphasized that the die size of the two chips was almost identical. And since the BCD process uses standard production equipment and is roughly equivalent in terms of process complexity this means that the die cost was comparable.

HIGHER CURRENT

Having demonstrated the benefits of low dissipation, designers set out to explore other limits of power IC technology, beginning with output current. The first BCD

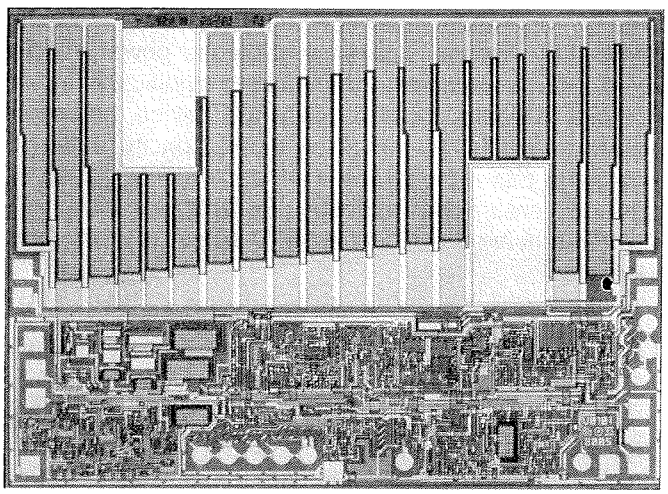

Fig. 3 *BCD technology has also been applied effectively in the power supply field. This high power switching regulator IC delivers 10A output current, more than twice that of an equivalent bipolar power IC.*

IC to enter this unexplored territory was the L4970 switching regulator, a one-chip switchmode power supply delivering 10A output current (figure 3).

To deal with current levels this high it was necessary to have two thicknesses of interconnect metal: a thin layer for normal signal interconnections and a thicker layer for the main connections to the DMOS power transistor. This thicker metal reduced the voltage drop on the metal tracks inside the chip, while the thinner signal metal allowed the use of finer pitches, hence greater density.

A new bonding technique was developed, too, to reconcile the conflicting needs of power and signal connections. Thick aluminum bonding wires are needed for the high current connections because a single gold wire would be insufficient and multiple wires inherently unreliable. However, these thicker wires need a larger bonding pad on the die so if they were used for all of the connections silicon area would be wasted. The answer to this problem was to use thick aluminum wires just for the power connections and thin gold wires for the signal connections.

Operating at switching frequencies up to 500kHz the L4970 also demonstrated the speed advantage of DMOS power transistors in fast switching designs. Even at high frequencies the efficiency of the device is high enough to allow a DIP- packaged version to deliver 4A the output current capability of a similar bipolar device in a Multiwatt power package.

HIGHER VOLTAGE

After raising the current limits, smart power designers turned towards higher voltages to extend the range of applications. The first step was the development of a 100V version, designed to satisfy the needs of applications in telecommunications and automotive. Though the battery voltage in automotive applications is only 12V this higher voltage capability is needed to ensure survival in an environment where high voltage transients occur.

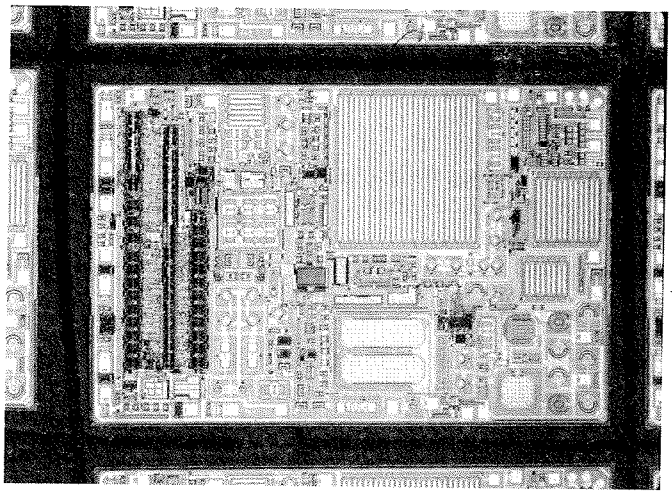

Fig. 4 *High voltage technology is useful in both industrial and telecom applications. This IC, produced with 250V BCD technology, is a solid-state hook switch for telephone sets.*

The 100V process was followed by a 250V version, aimed at telecom and industrial applications. While it was sufficient to increase the epitaxial layer thickness to reach 100V, more substantial changes were required to reach 250V. Most important of these is the use of a technique where the isolation diffusions are made in two parts. A seed of dopant is implanted in the substrate before epi growth; during subsequent processing this expands, meeting a conventional diffusion from above (figure 5).

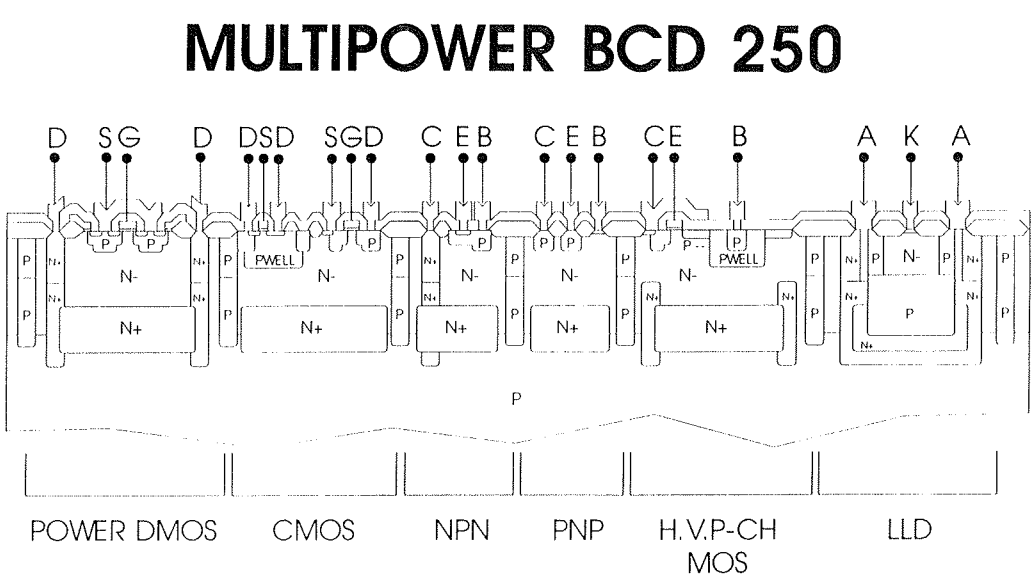

Fig. 5 *Cross section of the BCD250 technology. Compared to the lower voltage versions, this 250V technology has a thicker epitaxial layer so the top- bottom isolation technique is used.*

An example of the application of high-voltage technology in the telecom field is the telephone hook switch shown in figure 4.

In the high voltage field another version called BCD-Offline extends the capability of the technology to "offline" voltages (up to 700V). This process exploits the reduced surface field approach to integrate lateral DMOS high-voltage transistors.

BCD-Offline combines on a single chip low voltage CMOS and bipolar control circuits with high-voltage grounded-source lateral double-diffused MOS transistors (HV LDMOS) and grounded-source lateral insulated gate bipolar transistors (HV LIGBT). In source-follower configuration the source can float up to 20V.

A full custom circuit for a fluorescent lamp application is the first circuit in BCD- Offline technology to be qualified for production. This circuit, shown in figure 6, includes all of the functions for a fluorescent lamp driver in the preheat, ignition and on-state phases, driving two external MOS transistors.

Other products in development or qualification include a custom lamp driver with power factor correction and a high voltage half bridge driver aimed at appliance motor applications. This motor driver will be a standard part sold on the merchant market. BCD-Offline circuits are also in development for other applications such as power supplies.

SGS-THOMSON has derived lower voltage versions of this technology, rated at 300V and 170V, which will be suitable for application fields such as telecom, where circuits using high voltage technology are used to produce subscriber line interface circuits and hook switches.

HIGHER COMPLEXITY

While the trends towards higher current and voltage were easily predictable, at the end of the eighties a new trend emerged that was not expected by most experts in the field: the advent of high complexity smart power ICs.

Two factors made this possible. Firstly, the fact that BCD technology allowed the integration of isolated DMOS transistors meant it was possible not only to integrate any kind of power stage, but also any number of power stages. Second, the dissipation of power DMOS transistors was low enough to ensure that when multiple power stages are integrated the overall power dissipation is within the limits of normal packages.

High complexity smart power reached the market in 1988 when SGS-THOMSON introduced a single IC that integrated two 1A stepper motors drivers, a 3A solenoid driver and a 5V switchmode power supply (figure 7). This

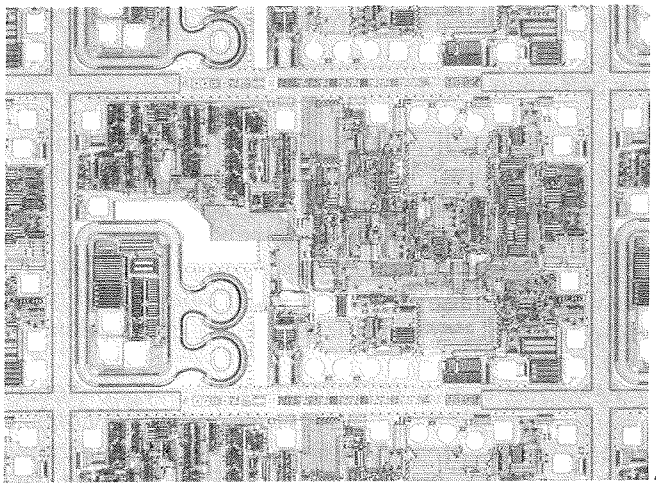

Fig. 6 *A new development, "BCD-Offline" technology is suitable for offline supply circuits or fluorescent lamp ballast circuits, like the proprietary device shown in this photo.*

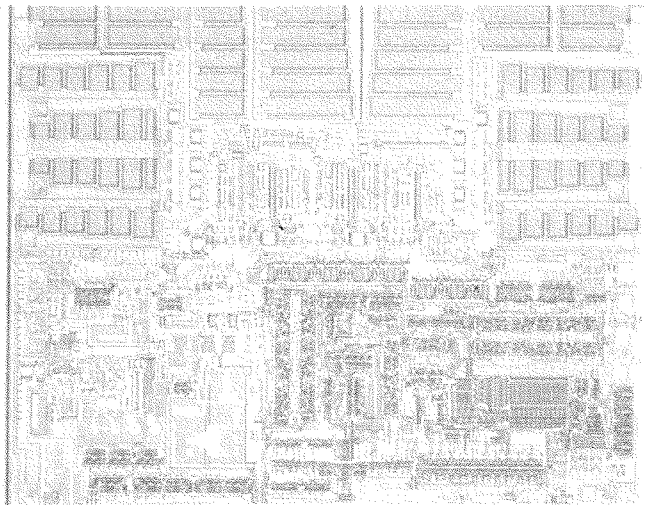

Fig. 7 *The first example of an LSI smart power IC, this circuit integrates two 1A motor drivers, a 3A solenoid driver and a 5V switching power supply.*

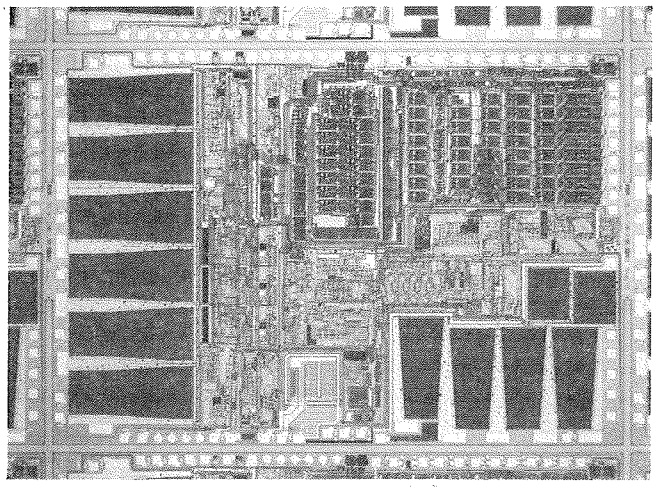

Fig. 8 *When the second generation 2.5 µm BCD technology was introduced it was applied to make very complex ICs like this disk drive circuit that integrates the spindle motor driver and head positioner of a hard disk drive.*

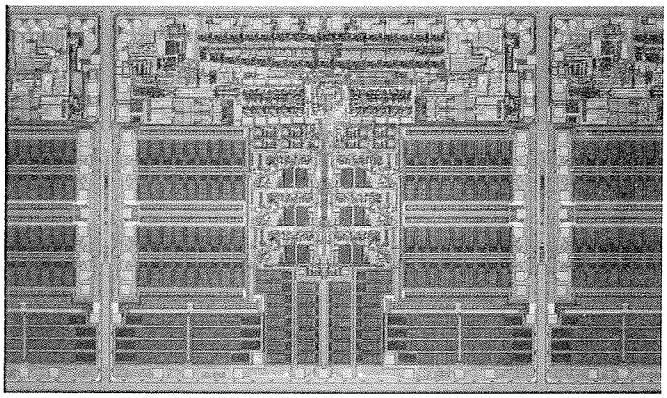

Fig. 9 *Another example of LSI smart power is this IC that controls and drives the three motors of a fax machine. Because of the very low dissipation of the power DMOS output stage this IC is packaged in a plastic PLCC package.*

chip, designed for a portable typewriter application, was controlled by loading commands through a bus into a set of internal registers. Among the innovative features of this device was the use of output stages that could be configured under software control.

The arrival of complex smart power chips prompted an acceleration of the trend towards finer lithographies. In fact soon after the introduction of the L6280 a second generation BCD process was introduced with 2.5m lithography. This doubled both the current density in the power stages and the component density in the signal section. As a result complex chips became much more cost effective.

This second generation BCD technology has found applications in many fields. One area where it has had the greatest impact is in hard disk drives for computers. Very little space is available in 2.5" and sub 2.5" drives, so

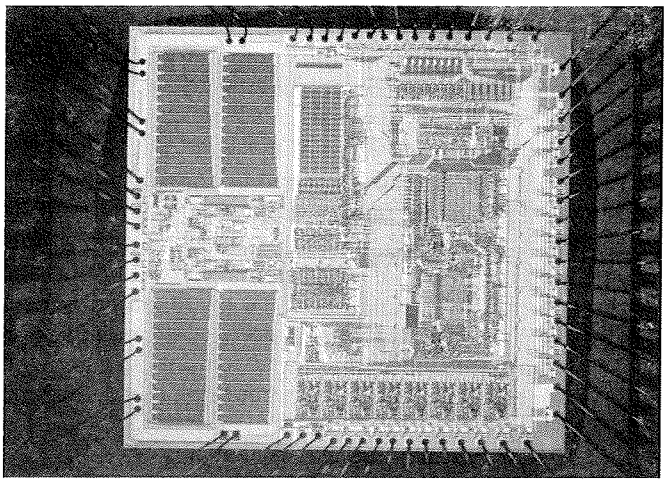

Fig. 11 *The first smart power IC to integrate a microcontroller, this technology demonstrator IC combines an 8-bit microcontroller core plus a 3A/60V power section.*

drive designers are always looking for new ways to reduce the component count. With BCD2 they were able to integrate all of the circuits for controlling the spindle motor and head positioner on a single chip. Figure 8 shows a circuit that integrates this function.

Similar circuits are used in other products where several motors must be driven. An example is the complex IC shown in figure 9, which was developed for a Japanese fax machine application. This IC drives the scanner, paper feed and cutter motors.

In 1993 a third generation BCD technology was announced (figure 10). Compared to the second generation this version offered a significant gain in density, thanks to a shrink from 2.5 to 1.2 μm lithography. More importantly, however, it brought the process into line with SGS-THOMSON's CMOS processes used for logic and memory circuits. Consequently, this version not only allows the integration of bipolar, CMOS and DMOS, but

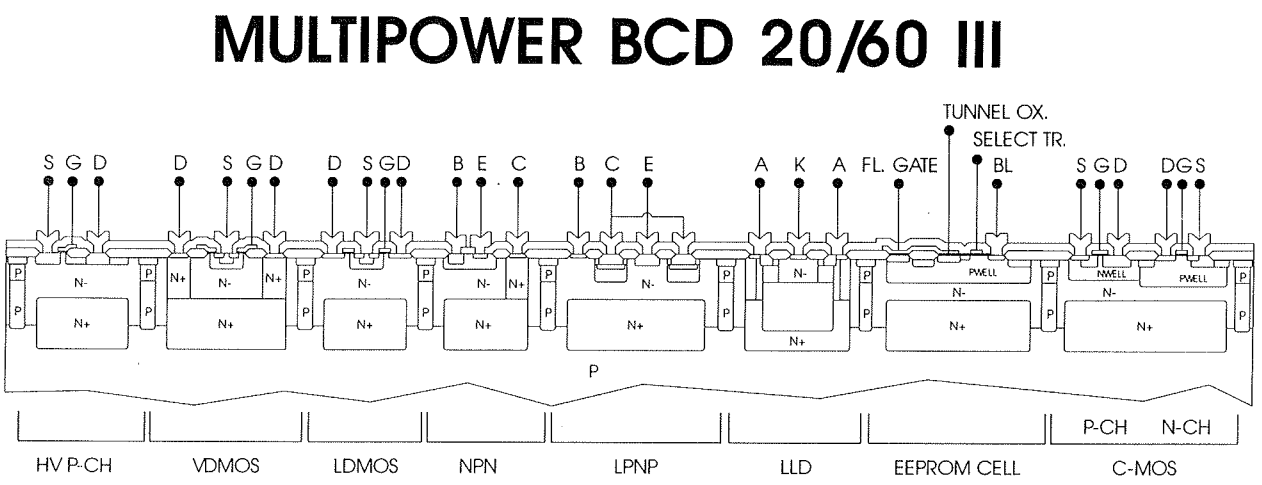

Fig. 10 *In the third generation BCD technology minimum linewidths of 1.2 μm are used. Other important characteristics are two levels of polysilicon, three levels of metal and a modular process structure that permits the inclusion of additional functions like EEPROM to the basic flow chart.*

it also lets designers insert in a BCD chip any cell or macrocell available within the company, including micro cores and advanced non-volatile memories.

Designers have been wary of the idea of integrating a micro on a power chip, expressing concerns that high voltage, high current pulses might disturb the micro. To allay these fears a demonstrator chip was produced in the spring of 1993 that integrated a 60V/3A bridge and a standard SGS-THOMSON ST6 microcomputer core (figure 11). Since this was a demo chip designed to demonstrate feasibility the program memory was external. In fact all of the internal connections in this chip are available externally for evaluation purposes.

Future evolutions of BCD technology, already planned, will reduce the lithography to 0.8 then 0.5 μm. In addition, new functionalities like flash memory will be added.

Technologies like BCD3 make it possible to reduce the component count of applications by integrating a microcontroller with the circuits it controls. However, the technology also allows designers to create a completely new type of general purpose power integrated circuit that is completely defined by software. Such circuits will have a microcontroller, memory, supply and some uncommitted power DMOS devices. Through software it will be possible to define the output configurations and define the functionality of the circuit. These general purpose circuits will become the power equivalent of PLDs, and greatly simplify small production runs or prototyping where a large volume custom circuit is unthinkable.

EMERGENT APPLICATIONS

In parallel with the development of these very high complexity circuits, there has also been an increase in the number of application fields where smart power technologies like BCD are applied.

While the technology was first applied in computer peripherals, it has spread to other sectors such as automotive, telecom and consumer. Automotive applications are primarily in the control and driving of motors, solenoids and relays, all applications that are growing very rapidly as electronic engine controls and electronic-based systems like ABS become more common. In addition, though, smart power is also a key technology behind multiplex wiring schemes. Telecom applications of smart power technologies include functions like the telephone hook switch, and subscriber line interface components for switching systems. Consumer applications include audio power amplifiers, like the 100W/100V device shown in figure 12, and power circuits for monitors, TVs and VCRs.

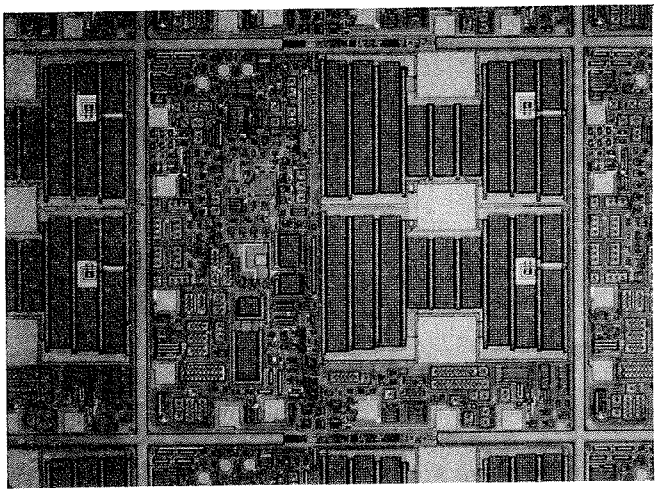

Fig. 12 *In addition to the trend towards greater complexity, there is also a trend to use smart power technologies in new application areas. This audio power amplifier, for example, uses BCD100 technology to achieve an unprecedented 100W output power (180W peak).*

Additionally there are some important new application areas related to the development of high voltage technology: fluorescent lamp driving and motor control for appliances. In both cases there is a major new market driving technology and product development.

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Prispelo (Arrived): 23.01.94 ***Sprejeto (Accepted): 25.01.94***

TANDEM AMORPHOUS SILICON SOLAR CELLS

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INVITED PAPER
21st International Conference on Microelectronics, MIEL'93
29th Symposium on Devices and Materials, SD'93
September 29 - October 1, 1993, Bled, SLOVENIA

Key words: photovoltaic energy, solar cells, tandem cells, amorphous silicon, state of the art, conversion efficiency, stability, series tandem, parallel tandem, fabrication

Abstract - Recent progress in the field of amorphous silicon tandem solar cells is reviewed. The advantages of series connected tandem cells with regard to single junction amorphous solar cells are discussed. Partitioning a thicker cell into two or three thinner cells results in higher inherent built-in electric fields in the cells with better conversion efficiency and stability. A new approach is described, utilizing parallel connection of cells in tandem structure to additionally improve efficiency, stability and sensitivity to thickness tolerances. The essential similarities and differences between series and parallel tandem cell arrangements are discussed and the present status of tandem cells fabrication is presented.

Tandemske amorfne silicijeve sončne celice

Ključne besede: energija fotonapetostna, celice sončne, celice tandemske, silicij amorfni, stanje razvoja, izkoristek konverzijski, stabilnost, tandem serijski, tandem paralelni, izdelava

Povzetek: Prikazani so dosežki s področja amorfnih silicijevih tandemskih celic. Opisane so prednosti serijskih tandemskih celic proti eni sami amorfni silicijevi sončni celici. Razdelitev debelejše celice v dve ali tri tanjše vodi do večjih vgrajenih električnih polj v posameznih celicah in k boljšim izkoristkom pretvorbe in večji stabilnosti delovanja. Opisan je novi pristop z vzporedno vezavo posameznih celic, pri kateri je pričakovati dodatno izboljšanje izkoristka, stabilnosti in neobčutljivosti na tolerance debelin celic. Prikazane so glavne podobnosti in razlike med serijsko in paralelno vezavo ter trenutno stanje tehnologije izdelave tandemskih celic.

INTRODUCTION

The majority of photovoltaic energy conversion devices on the market today are silicon solar cells, including most efficient but expensive single crystalline devices, less expensive recrystallized metallurgical silicon devices, as well as low cost thin film solar cells from amorphous silicon which received a great attention during the last decade as one of the most prospective materials for low cost solar cells.

Amorphous silicon (a-Si) can be inexpensively deposited on large substrates of various materials and shapes. During its deposition it needs to be treated to relatively low temperatures in the range of 200-300°C. Due to high light absorption of a-Si, the a-Si solar cell thickness can be very small, typically less than 1μm.

The main limitation in obtaining high solar cell conversion efficiency are poor transport properties of charge carriers in amorphous silicon. The photogenerated electrons and holes which make up the collected solar cell photocurrent have very short diffusion lengths which are much too short to provide effective collection of these carriers. Therefore, the a-Si cell has to be very thin and an aiding electric field is built inside of the cell to assist more effective charge separation and collection. On the other hand, the cell should be sufficiently thick in order to provide a suitable absorption of light flux. These opposing criteria directed to the idea of tandem a-Si solar cell structures where the individual cells are deposited sequentially forming a multilayer solar cell structure in which the unit cells are optically and electrically connected in series /1/. Since the collected photocurrent must be the same in all unit cells, each consecutive cell in a series tandem structure must be thicker than the preceding one.

A parallel connected tandem a-Si cell structure in which the individual cells are optically connected in series and electrically in parallel has been proposed recently /2/. This configuration which is presently under intensive investigations is hoped to outperform its series tandem counterpart with respect to conversion efficiency and stability promising also lower sensitivity of solar cell efficiency on nonuniform a-Si deposition rate in large area solar cell modules /3/.

SERIES TANDEM CELL STRUCTURE

In series tandem structures two or three cells are optically and electrically connected in series, as shown in Fig. 1 /1/. The front p^+in^+ cell is covered by a transparent conductive oxide (TCO) layer providing electric contact to the p^+ layer of this cell. The metal on n^+ layer is serving for electric contact to the back p^+in^+ cell. Junctions n^+p^+ interfacing consecutive unit cells are acting as ohmic contacts, electrically interconnecting succeeding p^+in^+ cells.

The individual cells in such serially stacked devices can use the same amorphous material in all unit cells. Such structure which affords a sufficient absorption of photon flux and enables a satisfactory collection of photogenerated carriers is regarded as one of the most practical solutions. The fact that the electric current in a series connected tandem cell is the same in all unit cells demands a greater thickness of each consecutive cell. Consequently, a practical stacked a-Si cell structure consists of only two cells. A triple tandem structure would require an unacceptably thin front and thick back unit cell. Most frequently these double stacked cells are fabricated by depositing thin layers of TCO, amorphous

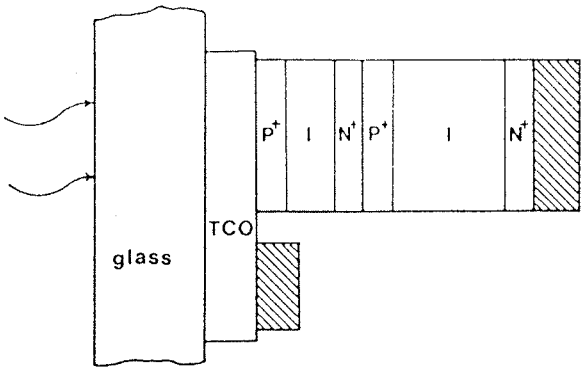

Fig. 1: The basic series tandem structure.

silicon and metal on a glass substrate, as shown schematically in Fig. 2. The p^+ and n^+ layers are indispensable for creating the built-in electric field in i-layers assisting charge carrier separation and collection. Since the diffusion lengths in highly doped a-Si are extremely short, these dead layers must be very thin, usually in the range between 15 and 30nm.

Even a very thin p^+ layer of the front cell parasitically absorbs a large amount of photons at short wavelenghts. For this reason the energy gap of the front p+ layer is increased to about 2eV by mixing amorphous silicon with carbon, resulting in a sort of optical window. In spite of a wider band-gap a relatively large part of light flux is absorbed in this so-called p^+ window layer, as shown in Figs. 3.a and b, representing the calculated portions of the absorbed sunlight flux in specific layers of a double stacked tandem cell for two sets of solar cell thicknesses, given in Table I. It can be noticed from these plots that the absorbed fluxes in i-layers of both cells are matched when the top cell is much thinner than the bottom cell.

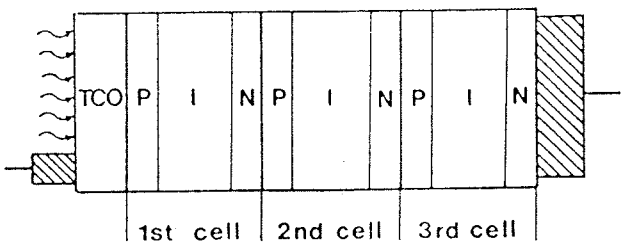

Fig. 2: Schematic presentation of double-stacked a-Si/a-Si series tandem solar cell.

The absorbed photons in both i-layers generate electrons and holes which are collected at opposite electrodes. The effectiveness of this charge collection greatly depends on the density of localized states in the gap of a-Si. Higher is the density of states in the i-layer, greater is the decrease of the built-in electric field and higher are thermal recombinations of photogenerated carriers, resulting in a decreased collection efficiency. The so-called Staebler-Wronski effect (SW effect), which originates from increased states density in the gap during a strong illumination, is the main cause of unstable operation of a-Si cells. When decreasing the thicknesses of individual cells in a-Si tandem structures, the built-in electric field in i-layers increases, and the solar cell degradation due to SW effect is reduced.

Table I Thicknesses of thin layers selected for calculation of absorptance

	Thickness (nm)	
layer(s)	case (a)	case (b)
TCO	200	200
P_1	15	15
I_1	30	470
N_1	15	15
$P_1/I_1/N_1$	60	500
P_2	15	15
I_2	370	570
N_2	15	15
$P_2/I_2/N_2$	400	600

The initial efficiency of double stacked a-Si/a-Si cells has been obtained around 11% /4/. However, after light induced degradation the stabilized efficiencies of 8% were obtained in large area modules.

The second kind of series tandem cell structure consists of two or three p^+in^+ amorphous cells having different band-gaps. This so-called multi-gap amorphous solar cell uses the principle of spectral splitting. As shown in Fig. 4, the incident light enters the first cell made from a wide band-gap material, absorbing only the blue portion

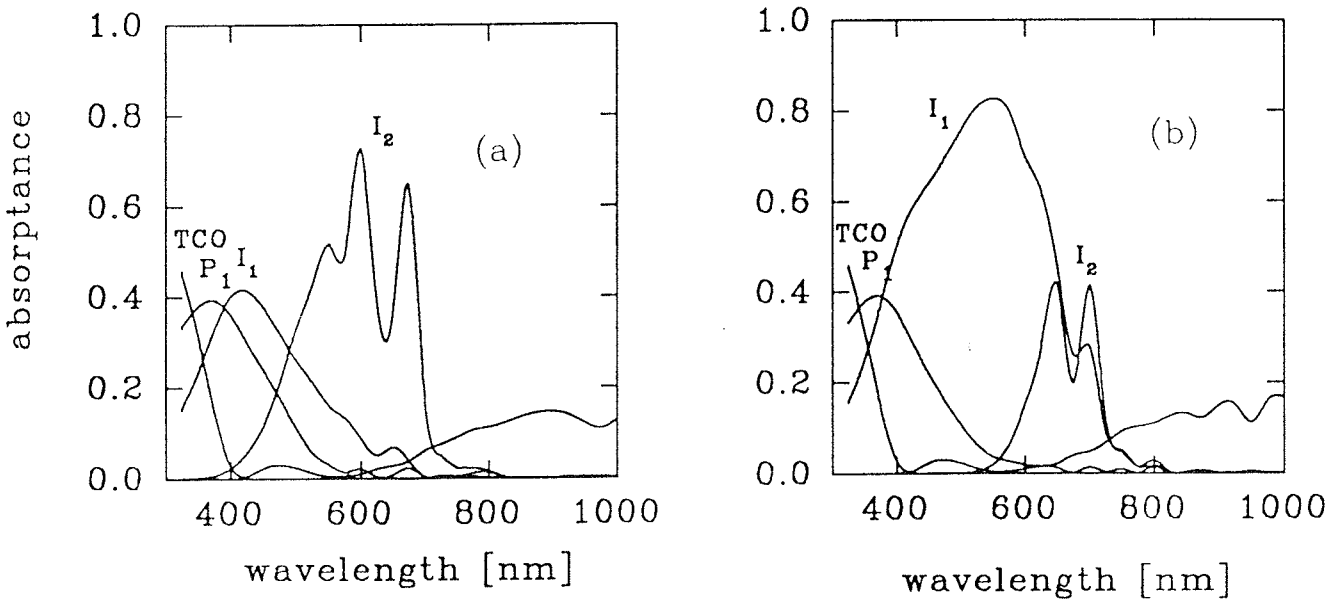

Fig. 3: Absorptance of sunlight in various layers of a double-stacked a-Si/a-Si solar cell in cases of an unmatched (a) and a matched (b) structure.

of the solar spectrum and producing inherently high open-circuit voltage. Higher wavelength light passes through the first cell without being absorbed and generates charge carriers in amorphous material of the second cell having smaller band-gap. The rest of the long wavelength flux which passes also the second cell is finally absorbed in the third cell made from the smallest band-gap material. A typical three cell configuration uses amorphous silicon-carbon, amorphous silicon, and amorphous silicon-germanium as semiconductor materials in such tandem configuration. As in case of double stacked a-Si/a-Si tandem structure the photogenerated currents in all cells in series must be equal, so that the thicknesses of individual cells are tailored with regard to their light absorption properties and carrier collection capabilities.

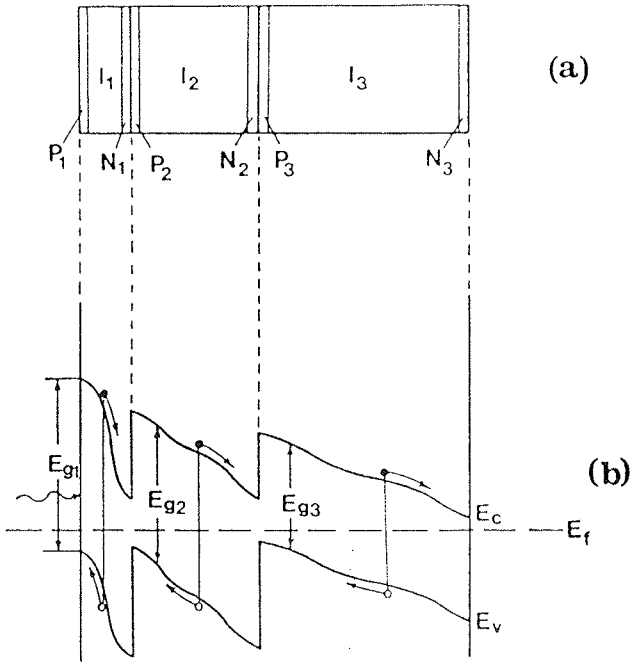

Fig. 4: Multi-gap stacked solar cell structure (a) with its band-gap representation (b).

Triple cell modules have been fabricated with initial conversion efficiencies between 10 and 11%, which degraded for less than 20% after extended light soaking /5/.

PARALLEL TANDEM CELL STRUCTURE

A new a-Si tandem solar cell structure has been proposed recently in which individual cells are optically connected in series and electrically in parallel /2/. This structure, shown schematically in Fig. 5, consists of two or more a-Si cells stacked in the sequence pin-nip-pin-...etc. At each interface between consecutive cells the electric contact to both joining cells is provided by a thin transparent conductive layer.

In contrast with series tandem structure in which the current passing all unit cells is the same, the parallel tandem arrangement requires equal photovoltages in all cells. This voltage, being in the vicinity of the open-circuit voltage, does not vary strongly with different light generated and collected charge carrier densities. This is because the voltage at the maximum cell collection efficiency markedly depends on strongly varying dark current and much less on gradually changing photocurrent component. This suggests that all unit cells in a parallel tandem arrangement must have equal dark characteristics, demanding the same amorphous semiconductor for all unit cells.

Intensive studies and experiments are currently carried on in fabricating a double stacked parallel tandem structure, and computer simulation of parallel tandem cell has also been initiated /3/. Computer modelling of a-Si tandem cells has indicated that the expected sensitivity of a parallel tandem arrangement on the thickness variations of individual cells is much lower than in case of series tandem structure. As an example, Fig. 6 shows

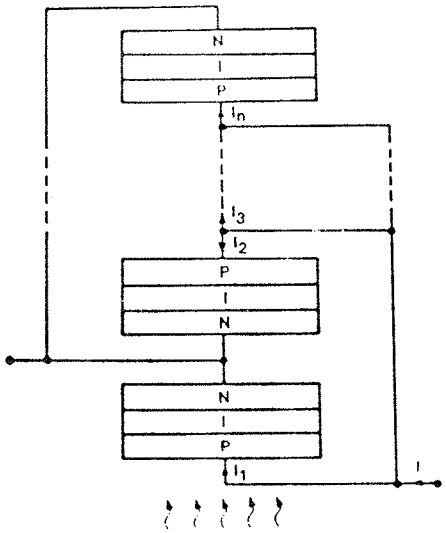

Fig. 5: Parallel tandem a-Si cell connection.

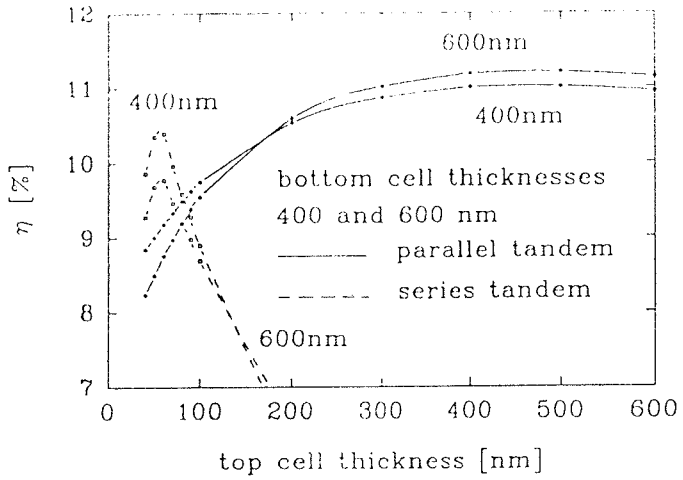

Fig. 6: Series and parallel tandem cell efficiency as function of top cell thicknesses.

the computed conversion efficiency of parallel and series tandem cells having a fixed bottom cell thickness and a varying top cell thickness. It can be noticed that in contrast with series tandem cell the thickness of the front cell in parallel connection can vary broadly not affecting strongly the conversion efficiency. Since the thickness of unit cells in parallel tandem connection is not critical it can be expected that this tandem arrangement will outperform the series tandem structure by having a smaller decrease of conversion efficiency due to nonuniform a-Si deposition rate in large area solar cell modules. Considering the fact that all unit cells in a parallel tandem structure can be made equally thin it can be expected that a structure consisting of multiple thin cells in parallel connection will behave very stable after strong illumination, having a very weak SW effect.

FABRICATION OF TANDEM CELL STRUCTURES

A variety of methods, such as chemical vapor deposition and sputtering, could be used to deposit a-Si based solar cells. However, the only technique which produced ac-

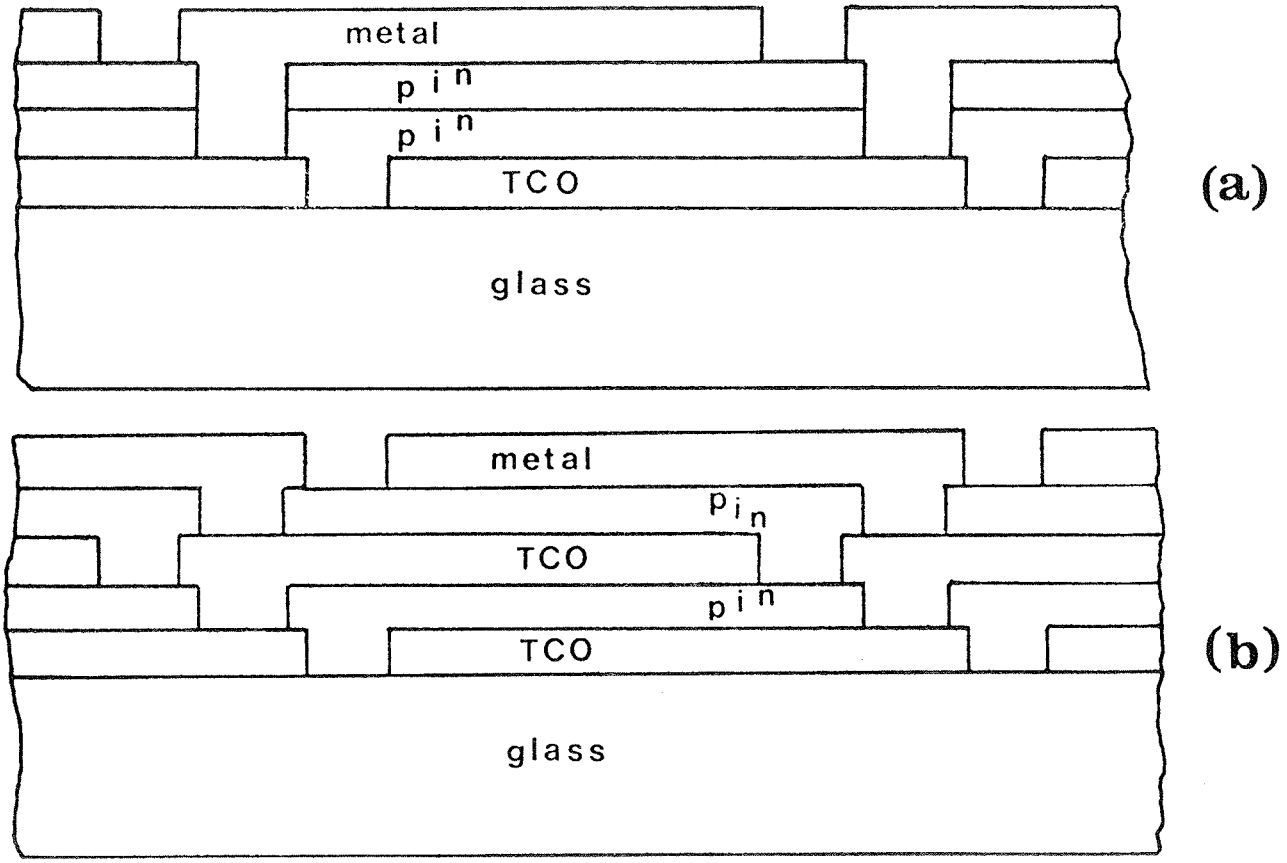

Fig. 7: Cross-sectional view with laser scribe pattern of double stacked series connection (a) and parallel connection (b).

ceptable undoped and doped amorphous silicon layers is plasma enhanced chemical vapor deposition or shortly glow-discharge process. The existing reactors can produce today the monolithic modules with active areas greater than 40cm x 100cm where the individual cells are patterned and interconnected into panels. The delineation of the monolitic pattern can be achieved by photolitography, mechanical abrasion, lift-off techniques or laser scribing. The most attractive approach for large area photovoltaic modules is that of laser scribing process, where laser cuts off the layers that have been deposited on the substrate. The typical laser scribe pattern of a two cell series tandem connection is shown in Fig. 7.a. The same patterning principle can be used for delineation of parallel tandem arrangement, shown in Fig. 7.b. Multiple cell panels can be made as extensions of cross sectional presentations in Figs. 7.a and b.

CONCLUSIONS

Tandem amorphous solar cell consisting of serially connected unit cells presents an improvement of electrical characteristics when compared to those of single amorphous silicon cell. The partition of a single cell into two or three cells connected in series results in smaller thickness of each unit cell while maintaining long enough path for photons to be moderately absorbed. The consequence of thinner intrinsic layers of individual cells are higher built-in electric field strengths with an improved collection efficiency of photogenerated carriers. Higher internal electric field causes also smaller cell instability due to Staebler-Wronski effect. The concept of parallel connected stacked solar cell represents a meaningful alternative to the conventional series connected arrangement. The parallel connected structure promises a higher conversion efficiency and a smaller sensitivity to unit cell thickness variations and will seemingly suffer a lower Staebler-Wronski effect.

ACKNOWLEDGEMENT

The work on parallel tandem cell structure is supported by the Commission of the European Communities, Programme Joule II.

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Prispelo (Arrived): 10.12. 93 ***Sprejeto (Accepted): 23.12. 93***

RARE EARTH - TRANSITION METAL MAGNETS: THEIR PROCESSING, PROPERTIES AND APPLICATIONS

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INVITED PAPER
21st International conference on Microelectronics, MIEL'93
29th Symposium on Devices and Materials, SD'93
September 29 - October 1, 199, Bled, SLOVENIA

Key words: permanent magnets, sintered magnets, hard magnetic materials, rare eart, processing, magnetic properties, applications, production, Nd-Fe-B magnets, HDDR magnets, hysteresis loops

Abstract: The properties and production of hard magnets are described by particular reference to the NdFeB-type magnets. Thus both the intrinsic properties (e.g. saturation magnetisation Ms) and extrinsic properties (e.g. intrinsic coercivity H_{ci}) are discussed and it is shown how these properties are exploited in sintered magnets and their applications.

Magneti kovin prehoda in redkih zemelj: proizvodnja, lastnosti in uporaba

Ključne besede: magneti trajni, magneti sintrani, materiali trdomagnetni, zemlje redke, procesiranje, lastnosti magnetne, uporaba, proizvodnja, Nd-Fe-B magneti, HDDR magneti, zanke histerezne

Povzetek: V delu opisujemo lastnosti in uporabo trdih magnetov s posebnim poudarkom na NdFeB magnetih. Prikazane so tako nasičenjska magnetizacija, Ms, kakor tudi koercitivna sila, H_c, še posebej glede na izdelavo in uporabo sintranih magnetov.

Introduction

The term hard magnet is used as an alternative to the term permanent magnet and describes a magnetic material which can be permanently magnetised by the application of a magnetic field. This behaviour is illustrated by the hysteresis loop and a typical loop for a good hard magnet is shown in Fig. 1. In production the objective is to produce a square hysteresis loop with as large a value as possible of the remanence, Br, and as high a value as possible of the intrinsic coercivity, Hci. Such properties ensure a large value of the maximum energy product, $(BH)_{max}$, which is a useful figure of merit for hard magnets. Essentially the higher is (BH)max the smaller is the volume of the magnet required to produce a given magnet flux. Thus the progress in hard magnetic technology over this century can be illustrated by the change in (BH)max as a function of time (Fig.2). In the early part of this century, gradual progress was made and magnets were made from steels. These were followed by the alnicos (Al-Ni- Co) which were discovered in the thirties and were improved significantly over a period of some thirty years by a process of "alloy engineering". (Alnicos are still used extensively but are being replaced in many applications by the rare earth-transition metal-type magnets). The next major step was the appearance of the

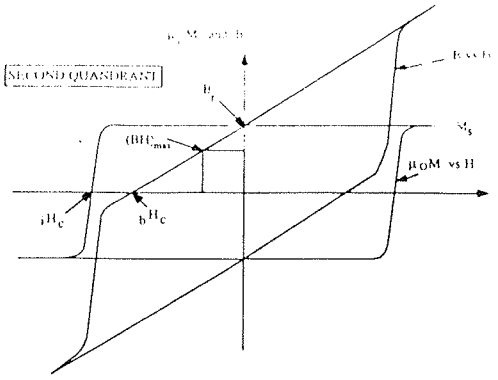


Fig. 1: A hysteresis loop for a good hard magnet.

ceramic magnets based on strontium (and barium) ferrite ($SrFe_{12}O_{19}$) in the fifties and this represented the first significant exploitation of magnetic materials exhibiting the intrinsic property of magnetocrystalline anisotropy the significance of which will be discussed later. These magnets are still used extensively and have the enormous advantage of being extremely cheap.

Perhaps the most exciting development in hard magnetic materials this century (equivalent in superconducting technology to the appearance of the high Tc superconductors) was the development of the $SmCo_5$ magnets by Strnat and co-workers (1,2). This lead to a steep

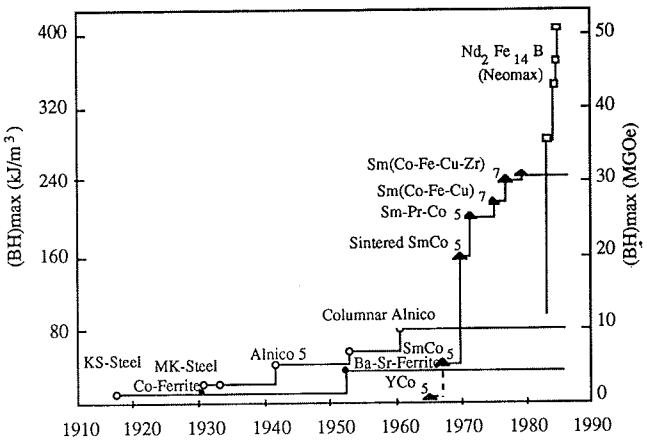


Fig. 2: The variation of $(BH)_{max}$ with time over this century

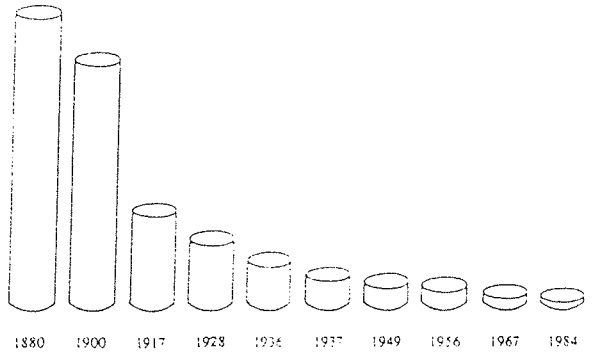


Fig. 3: These magnets all develop the same magnetic flux and the reduction in size is achieved by increasing values of $(BH)_{max}$

rise in $(BH)_{max}$ values with the subsequent development of the $Sm_2(Co,Fe,Cu,Zr)_{17}$- magnets (2,3) and most recently, the NdFeB-magnets (4,5). A consequence of these spectacular improvements in $(BH)_{max}$ is a dramatic reduction in the size of the magnets required to produce a particular magnetic flux and this is illustrated in Fig. 3. The intrinsic and extrinsic properties of magnetic materials will now be considered with particular reference to the NdFeB- magnets.

More recently magnetic materials based on Sm-Fe-N (6) have been developed where nitrogen in the interstitial sites of the Sm_2Fe_{17} structure raises the Curie point from 120°C to 480°C and the anisotropy field of the nitride is twice as high as $Nd_2Fe_{14}B$.

Intrinsic Magnetic Properties

The value of the remanence (Br) depends on the value of the saturation magnetisation(Ms) and the squareness of the hysteresis loop (see Fig. 1). The Ms depends predominantly upon the magnetic moment on the transition metal atoms (Fe,Co). The ferromagnetic phase in the NdFeB-type magnets is the tetragonal compound

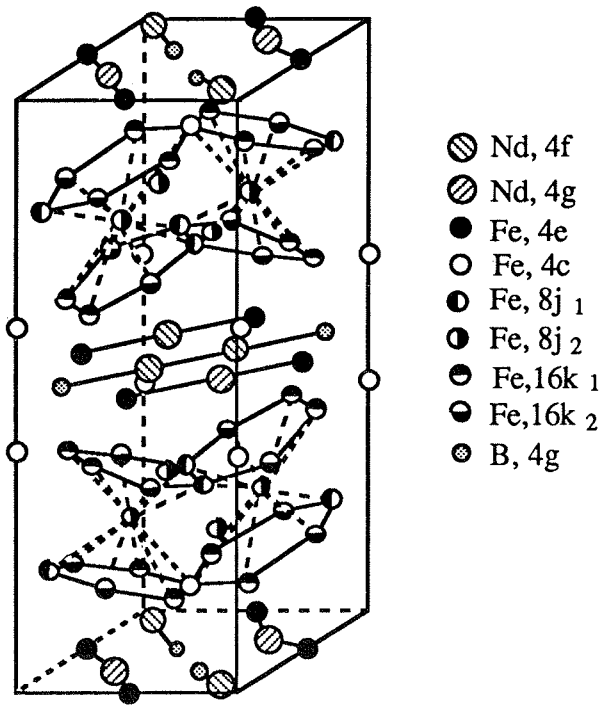


Fig. 4: The structure of the tetragonal compound $Nd_2Fe_{14}B$.

$Nd_2Fe_{14}B$ (Fig.4) with a mean Fe-moment of 2.50μ_B. The Curie-point of this compound is around 585K which means that it can be heated to this temperature before the ferromagnetism disappears. An essential characteristic of the compound with regard to magnet production is that it exhibits easy magnetisation along the c-axis of the tetragonal cell i.e. uniaxial magnetocrystalline anisotropy. This arises largely from the rare earth neodymium atoms where the 4f spin-orbit - lattice interactions produce the anisotropy in the magnetisation behaviour. This is the reason for the presence of the expensive and reactive rare earth metal and the practical significance of this behaviour is that fine single crystal particles of the compound can be aligned preferentially along their c-axis. The particles can be locked into this configuration by sintering and this, together with the development of an appropriate microstructure (see later), is the basis for the production of a NdFeB-hard magnet.

Extrinsic Magnetic Properties

It is not sufficient just to have the necessary intrinsic magnetic properties in order to make an effective hard magnet, it is also necessary to develop the essential extrinsic property of coercivity. Thus, once the magnetic domains are aligned along the favourable c-axis orientation then it should be made as difficult as possible for reverse domains to form and to demagnetise the magnet. How is this achieved?

The theoretical maximum value of the coercivity is the same as the anisotropy field H_A for a particular ferromagnetic phase which is given by the expression:

$$H_A = \frac{2K_1}{Ms}$$

where K1 is the anisotropy constant.

In reality the coercivity values of rare earth-transition metal hard magnets are much less than the appropriate H_A values and this behaviour can be ascribed to the nucleation of reverse domains from imperfections within particular magnetic materials. The reduced coercivity Hc at temperature T is given by the general expression:

$$Hc(T) = \alpha\,(T)\frac{2K_1}{Ms} - NMs$$

where α (T) is a temperature dependent microstructural parameter, and N takes account of demagnetising fields. The formation of reverse domains can be retarded by a pinning or a nucleation mechanism. In the case of the $Sm_2(CoFe,Cu,Zr)_{17}$- type magnets (2,3), the first mechanism operates and the favourable domain configuration is "pinned" by fine precipitates so that a pinning potential well has to be overcome before a reverse domain can form and a series of obstacles have then to be overcome for the domains to propagate throughout the bulk of the material. This behaviour is reflected in a distinct kink in the first quadrant magnetisation behaviour of these magnets (Fig. 5). In the case of the NdFeB-type magnets (5) it is believed that it is the nucleation mechanism which predominates and this is reflected in the first quadrant magnetisation behaviour where a high initial permeability and easy c-axis magnetisation is achieved (Fig.6). Having produced a favourable alignment of the domains, the microstructure of the magnet is such that high reverse fields are required to nucleate, sustain and propagate reverse domains. Electron microscope studies (7) have shown that the $Nd_2Fe_{14}B$ matrix is free of any imperfections and it is thought that reverse domains originate at irregularities at the grain boundaries. A typical composition of the NdFeB-type magnet is $Nd_{15}Fe_{77}B_8$ (atomic percent) whereas the composition of the $Nd_2Fe_{14}B$ compound is $Nd_{11.8}Fe_{82.3}B_{5.9}$. The excess neodymium in the former forms predominantly a Nd-rich grain boundary phase

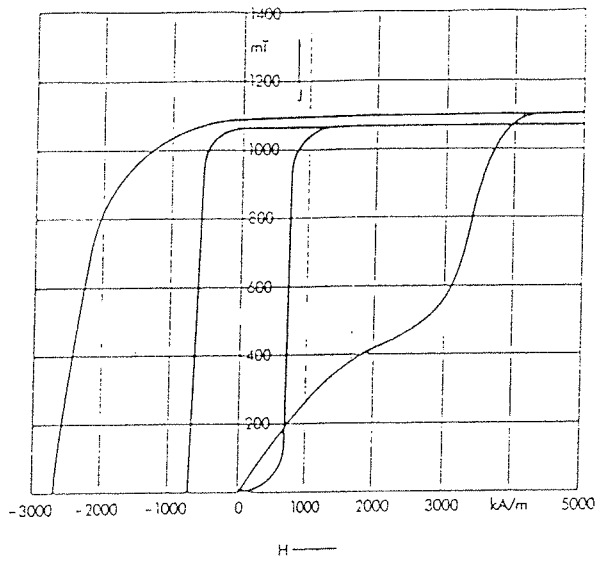


Fig. 5: The magnetisation behaviour of a 2/17-magnet.

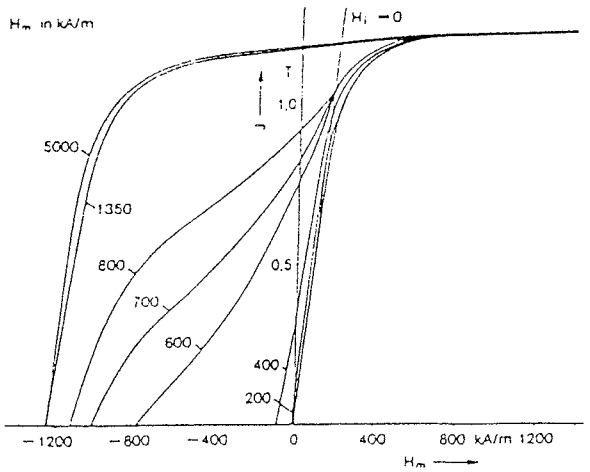


Fig. 6: The magnetisation behaviour of a NdFeB-magnet.

(part of a eutectic which melts at 903K) which is therefore liquid at the sintering temperature of around 1320K. The influences of the grain boundary material are at least three fold in character:

(1) it produces liquid phase sintering with the attendent densification.

(2) it produces smooth grain boundaries and hence reduces the incidence of irregularities (e.g. steps) for reverse domain nucleation. It is known that sharp corners act as nucleation sites for reverse domains.

(3) It provides a barrier to the propagation of reverse domains between grains i.e. it provides the grains with magnetic isolation.

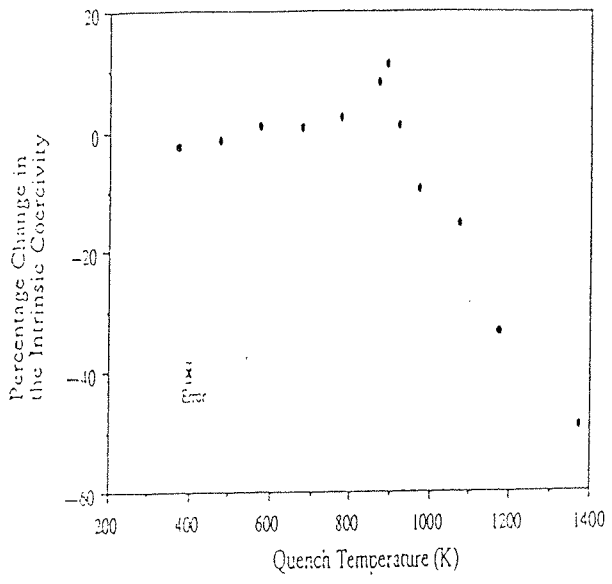


Fig. 7: The effect of quenching on the H_{ci} values of a NdFeB magnet initially slowly cooled from the sintering temperature.

There might also be an element of domain pinning by grain boundary phases and the constitution of the boundary material is complex (7) and sensitive to heat treatment.

The importance of the grain boundary materials is shown in the effect of quenching (8) on the magnetic properties of the sintered NdFeB-type magnets. This is shown in Fig.7. and it can be seen that quenching an initially slowly cooled magnet from above the melting point of the grain boundary material results in a marked deterioration in the values of H_{ci} which become progressively worse with increasing quenching temperature. This was attributed to the incomplete coverage of the grain boundaries by the Nd-rich material on quenching but it was also possible that subtle changes in the constitution also had some influence. The original properties could be recovered by annealing the quenched magnets at 903K.

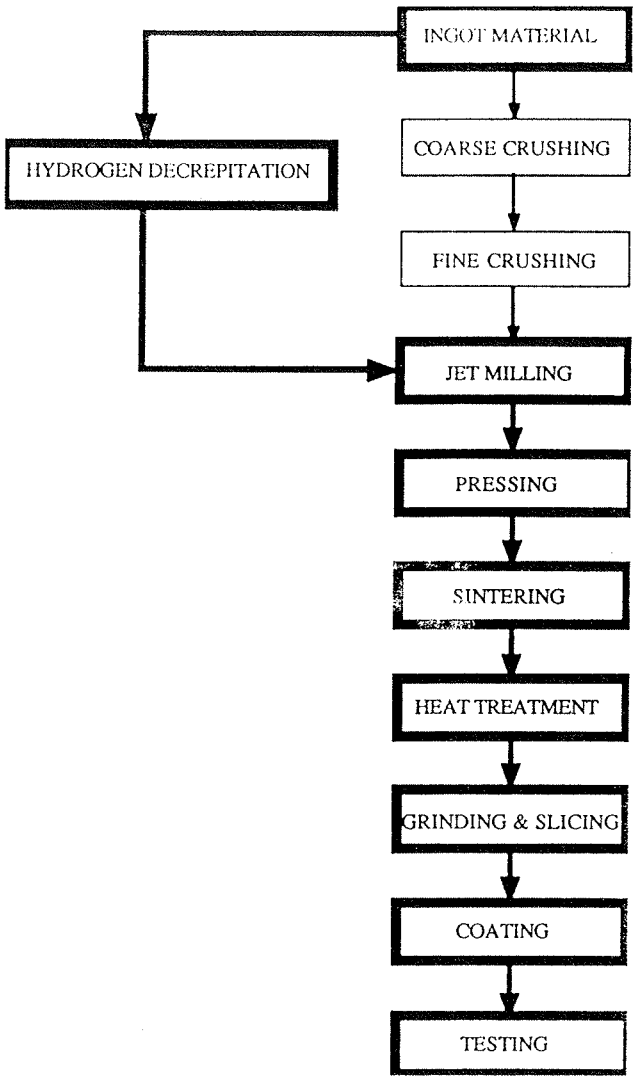
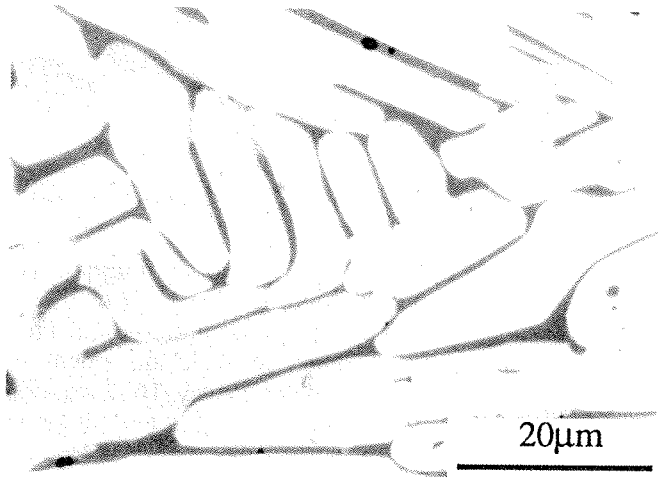


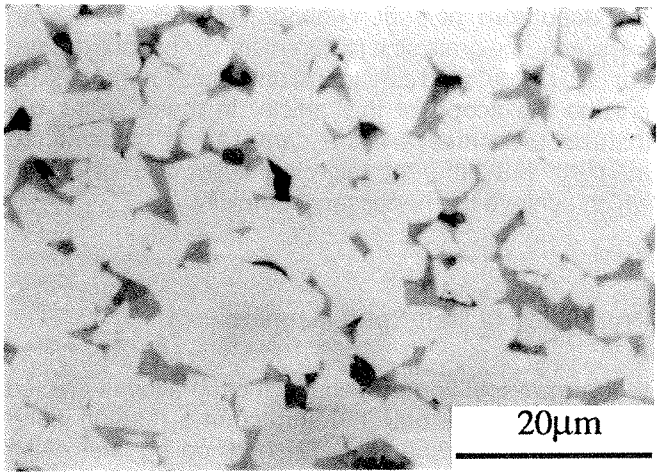
Fig. 8: The production sequence of a NdFeB-magnet.

Production of Sintered Magnets

The previous considerations have shown that the production of an effective sintered magnet depends upon obtaining the appropriate intrinsic properties, Ms and H_A (uniaxial) by the selection of a suitable compound and obtaining the necessary coercivity by the formation of a suitable microstructure. The production sequence for a sintered NdFeB-type magnet is show in Fig. 8. and a very similar procedure is adopted for the production of the strontium ferrite, $SmCo_5$ and $Sm_2(Co,Fe,Cu,Zr)_{17}$ magnets (although the latter also requires a step ageing treatment). The process consists of converting the coarse grained randomly oriented cast ingot into a fine grained, highly oriented sintered magnet; the change in microstructure is shown in figure 9. The hydrogen decrepitation (HD) process (9) provides an effective and convenient means of providing particulate material which is very suitable for jet milling. This process depends on the affinity of the $Nd_{15}Fe_{77}B_8$ and related alloys for hydrogen and the subsequent desorption of hydrogen during vacuum sintering. The decrepitation process is represented schematically in Fig. 10.



(a)



(b)

Fig. 9: The microstructures of the NdFeB (a) cast ingot and (b) sintered magnet.

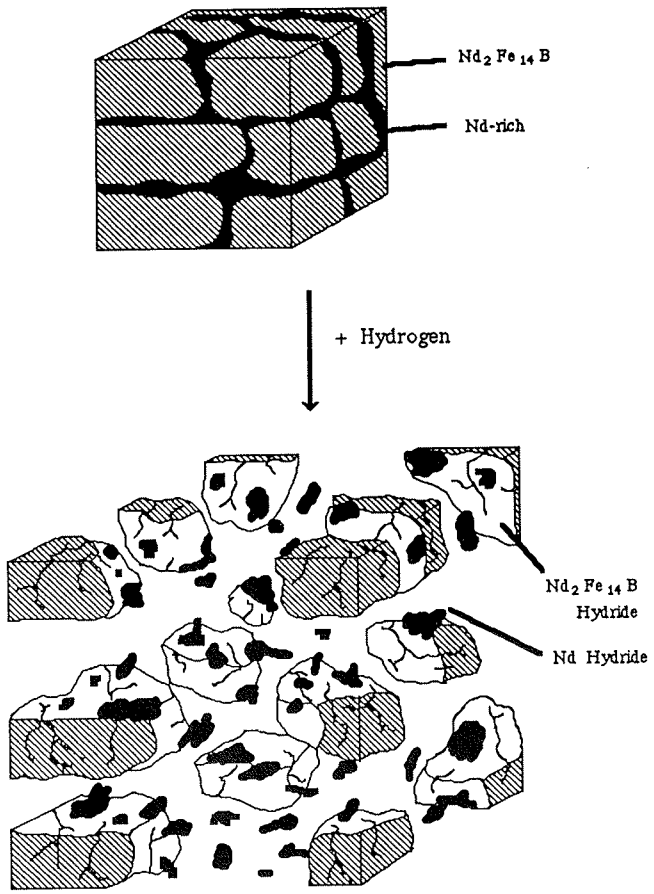


Fig. 10: A schematic representation of the HD-process.

The production of fine grained sintered magnets requires the formation of fine jet-milled powder of ≅ 2μm particle size and the sintering temperature and time have to be controlled carefully to avoid the growth of large grains which degrade the coercivity. The influence of the grain size distribution (10) on the H_{ci} values is illustrated in Figure 11.

It should be noted that NdFeB - magnets can also be produced from melt-spun ribbons (11) which exhibit an extremely fine grain size (≅ 20nm) and from hot extruded bar (12) but detailed consideration of these materials are outside the scope of this article. In these cases the intrinsic properties are the same as in the sintered magnets but different microstructures are produced which achieve the necessary coercivity.

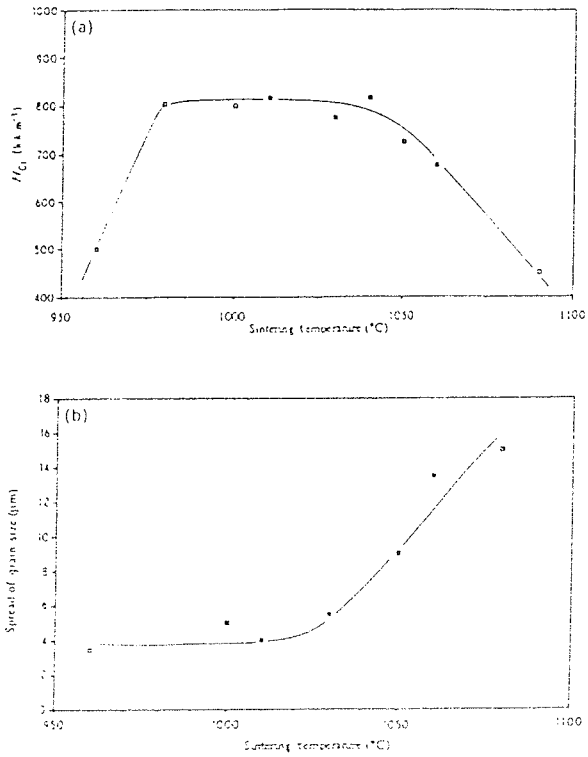


Fig. 11: The influence of the grain size distribution of a NdFeB magnet on the value of H_{ci}.

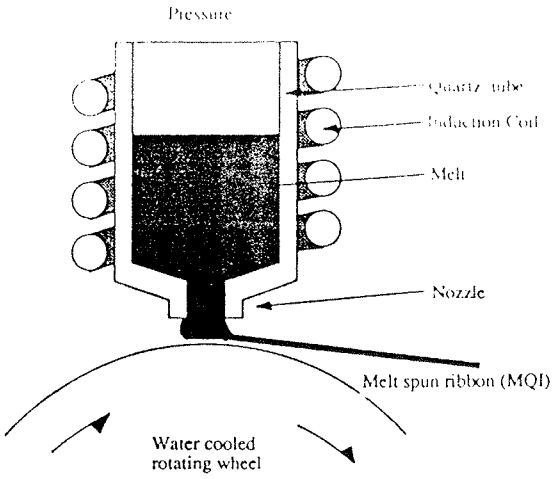


Fig. 12: A schematic representation of the melt spinning process.

Production of Melt-Spun Magnets

In the melt-spinning procedure, molten alloy is ejected through an orifice onto the surface of a rotating water cooled substrate wheel (fig. 12), and cooling rates of the order of one million °C/s are achieved. The microstructure and magnetic properties of the NdFeB ribbons formed by melt- spinning are very sensitive to the quench rate (13). High quench rates produce essentially amorphous ribbons having negligible intrinsic coercivity. Optimum quench rates yield ribbons with the highest coercivities; they are comprised of roughly spherical $Nd_2Fe_{14}B$ grains (20- 100 nm in diameter) (fig.13). At wheel velocities below the optimum, the slow cooling rate produces ribbons that consist of larger grains and are characterised by low coercivities. Ribbon melt-spun at high rates have an amorphous or partially crystalline structure, but can be annealed to nearly duplicate the properties of the optimally quenched materials (14).

Fabrication of the magnet requires consolidation of the magnetically isotropic ribbons. The processes for this

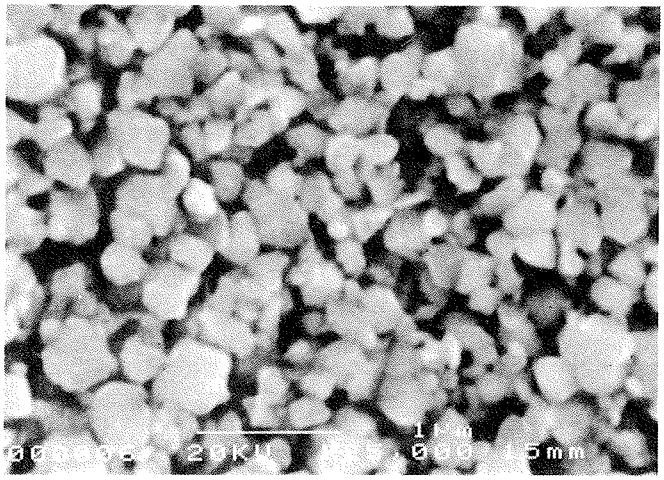


Fig. 13: SEM micrograph of a polished and etched melt spun flake.

have been developed by the Delco Remy Division of General Motors. They have named the magnet material Magnequench and there are three grades. The first and simplest procedure is to cold press, optimally quenched ribbons with a bonding agent. The resulting bonded magnet which remains magnetically isotropic, is commonly referred to as an "MQI" type magnet.

The crystals of MQI material are randomly oriented so that the magnets are isotropic and can be magnetised along any axis. A considerable flux density of about 3T is required to magnetise the magnets to 99% of saturation. The isotropic nature of the material limits the (BH)max to 56-80 kJm^{-3} (7-10 MGOe).

Improved densification of melt-spun ribbons is afforded by the second procedure, hot pressing. Appropriate temperatures and pressures vary with composition; but for compositions near $Nd_{13.5}Fe_{81.7}B_{4.8}$, full density is achieved for T ≅970K and P ≅100 MPa. If optimally quenched ribbons are used, grain growth is not excessive at these temperatures. To ensure the most desirable grain size, however, it is preferable to hot press over- quenched ribbons, which are either amorphous or consist of undersized grains. These "MQII" type magnets exhibit only slight (≅10%) magnetic alignment and require a flux density of about 3T for magnetisation to 99% of saturation. They are 100% dense and this gives them a higher (BH)max than "MQI" of 100-120 kJm^{-3} (12-15 MGOe).

Substantially greater alignment (>75%), and hence greater energy products, can be obtained by the third procedure, in which an initial hot press is followed by another in a die cavity having a larger diameter. This second hot press, termed die upset forging, produces bulk lateral plastic flow and a reduction in ribbon thickness. Such magnets are 100% dense, and have been obtained with energy products as large as 320 kJm^{-3} (37 MGOe). The required magnetising flux density of 2.5T is lower than for the isotropic MQ magnets. A review of the processing and properties of Magnequench has been given by Carlisle (1986) and more recently by (13).

Production of HDDR Magnets

An alternative to the production routes already mentioned is the Hydrogen Disproportionation Desorption and Recombination (HDDR) process (16,17). In this case the intrinsic properties are achieved, in the same way as sintered magnets, with the use of $Nd_2Fe_{14}B$ as the magnetic phase, however the extrinsic properties are generated by a very different method to that used for sintered NdFeB magnets.

A schematic representation of the HDDR process is illustrated in figure 14. The first stage is hydrogen decrepitation of the ingot material, producing a hydrided powder. This powder is then heated in a 1bar pressure of hydrogen up to 800°C, with the effect of disproportionating the Nd2Fe14B phase to Nd hydride, iron and ferroboron. After 2 hours at 800°C the powder is placed in a vacuum for a further hour before cooling. This causes the desorption of the Nd hydride, with the result that recombination of the $Nd_2Fe_{14}B$ occurs. The microstructure of the powder is now very different to the as cast starting material because nucleation of the Nd2Fe14B occurred at many sites within the origin grains and now the average grain size is ≅0.3μm (fig.15). This grain size is approximately the same as the critical grain size for single domain particles in $Nd_2Fe_{14}B$. This means that it is energetically favourable to have only one domain in each grain, hence making it difficult to form reverse domains.

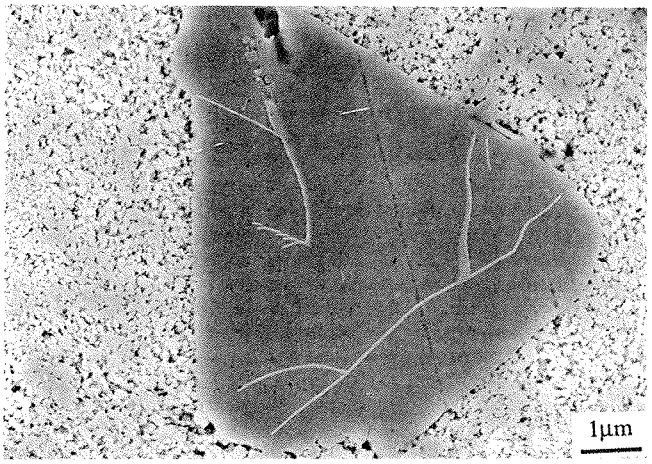


Fig. 15: SEM micrograph of a polished and etched HDDR particle, showing a large grain surrounded by fine grained material.

The powder cannot be sintered because the grains would grow and the coercivity would be lost. Therefore the powder must be bonded or alternatively hot pressed, which is a process rapid enough to avoid grain growth.

The powder produced is isotropic, i.e. its magnetic properties are the same when magnetised in any direction. This is because the powder particles consist of many grains which have random orientation. However, it is possible to make anisotropic powder by adding various elements e.g. 0.1 at% Zr to the alloy, and in this case the fine grains have an overall preferred orientation

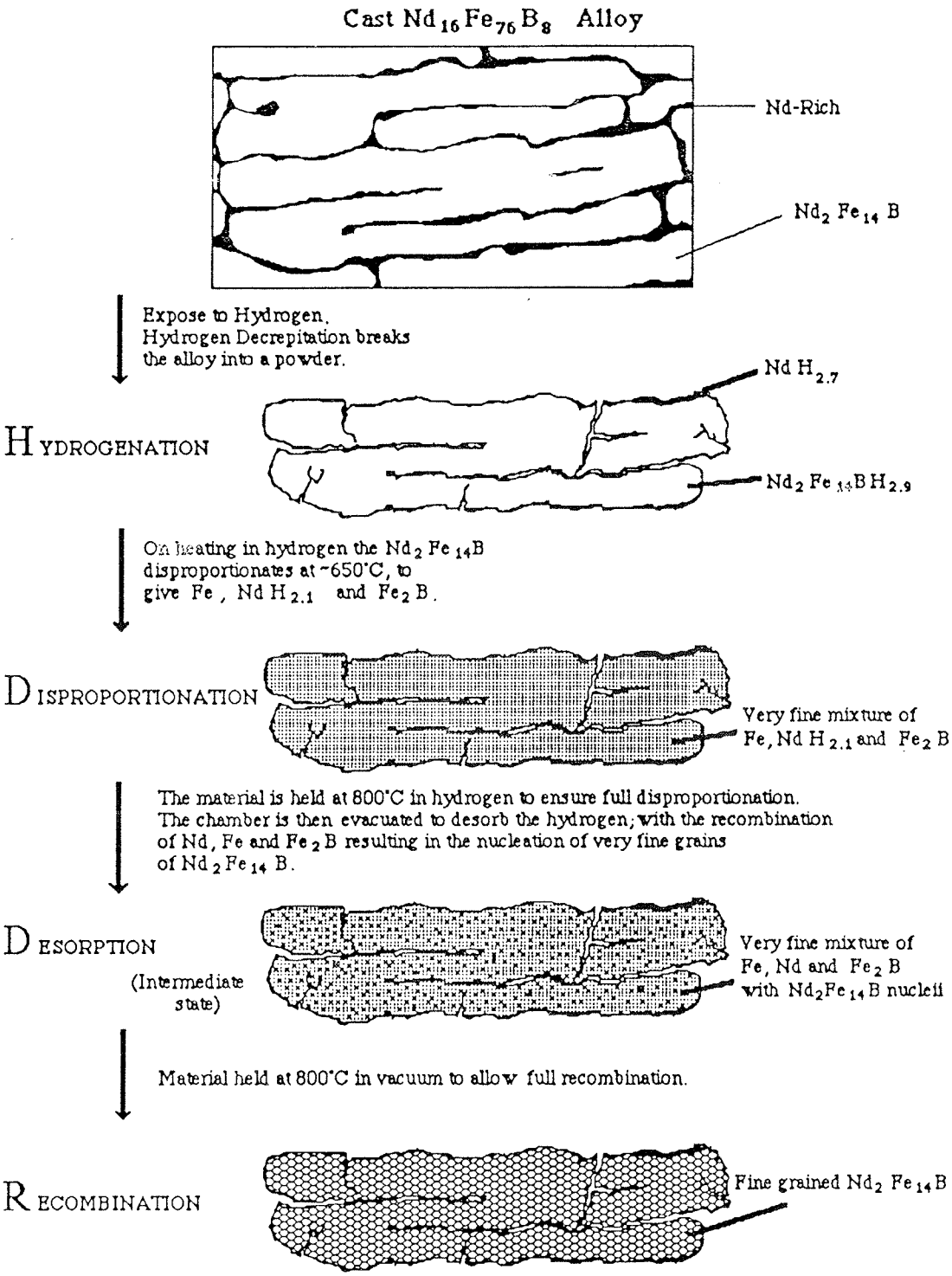


Fig. 14: A schematic representation of the HDDR-process.

related to the orientation of the original $Nd_2Fe_{14}B$ grain. The best energy product of 34MGOe has been achieved by hot pressing anisotropic HDDR powder (18).

Applications

Due to the increased energy product provided by rare earth-transition metal magnets new and miniaturisation of existing applications have become possible. Electric motors with increased power or reduced size / weight are perhaps one of the major advantages of these magnetic materials, for example hand held power tools and small ear phones are now possible. The use of voice coils to generate precise movement is utilised for example in a compact disc player for the scanning and focusing of the laser beam.

Permanent magnet body scanners are now possible, where previously liquid helium cooled superconductors have been required to generate the magnetic fields

required. Medical applications include magnetic clasps for sealing wounds, holding dental crowns in place and to assist in correcting misaligned teeth.

Future Prospects

There is still considerable scope for the development of NdFeB-type magnets to give improved temperature performance and improved corrosion resistance. This is illustrated by recent work (19, 20) on the beneficial influences of V and Mo additions. There is also scope for the discovery of new hard magnets with improved Curie temperatures and perhaps (BH)max values when compared to NdFeB. A particular challenge is the development of magnets based on Mn-rich alloys which would exploit the enhanced magnetic moment of Mn compared with that of Fe. A major problem here is the propensity of Mn to form anti-ferromagnetic alloys but efforts should be encouraged by the prospect of much enhanced (BH)max values.

Acknowledgements

Thanks are due to CEAM, EURAM and SERC for support of the research programme into rare earth-transition metal magnets at Birmingham

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Prispelo (Arrived): 21.12.93 ***Sprejeto (Accepted): 23.12.93***

AN OVERVIEW OF RECENT DEVELOPMENTS IN CERAMIC AND POLYIMIDE TECHNOLOGIES FOR MULTICHIP MODULES

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INVITED PAPER
21st International Conference on Microelectronics, MIEL'93
29th Symposium on Devices and Materials, SD'93
September 29 - October 1, 1993, Bled, SLOVENIA

Key words: semiconductors, integrated circuits, multichip modules, state of the art, overview, size reduction, interconnections, interconnect technology, circuit density, signal processing, processing rates, decreasing distances, thick film technology, LTCC technology, Green tape semi - automatic line, thin film technology

Abstract: MultiChip Modules are gaining wide acceptance as a powerful method to interconnect several ICs in the same board. The increasing size of ICs, the higher power required to operate them and their physical closeness create new problems to the interconnect designers, mainly due to TCE mismatch between Silicon and PCB materials and to the need of a low dielectric constant of the interconnect media. Ceramic MCMs appear to be well positioned to provide a cost effective solution to today interconnect requirements.
The paper will review the latest development of DuPont in terms of materials and processes for the fabrication of Ceramic MCMs, either by extending the area of application of thick film hybrids, with limited investments, or by using Low Temperature Co-fired Ceramics (LTTC) technology, better known as Green Tape, with equipment developed "ad hoc" for large volume production, requiring an important capital investment.
The paper will also mention the latest DuPont developments on organic materials for MCMs, including Photosensitive and "low stress" polyimides.

Pregled trenutnega stanja razvoja keramične in poliimidne tehnologije za multičip module

Ključna besede: polprevodniki, vezja integrirana, moduli multichip, stanje razvoja, pregled, zmanjševanje velikosti, povezave vmesne, tehnologija povezav, gostota vezij, procesiranje signalov, hitrosti procesiranja, zmanjševanje razdalj, tehnologija debeloplastna, LTCC tehnologija, Green tape linija polavtomatska, tehnologija tankoplastna

Povzetek: Multičip moduli se vse bolj uveljavljajo kot način povezave nekaj integriranih vezij na eni tiskani plošči. Vse večja površina čipov, vse večja moč potrebna za njihovo krmiljenje, ter vse manjša razdalja med čipi povzročajo nove probleme načrtovalcem tiskanih plošč predvsem zaradi razlike v TCE med silicijem in materialom za PCB plošče ter potrebe za nizko vrednostjo dielektrične konstante povezovalnega medija. Keramični multičip moduli ponujajo tehnično in stroškovno zanimivo rešitev za vse omenjene probleme.
V članku pregledno podajamo trenutno stanje razvoja materialov in procesov za keramične multičip module v firmi DuPont. Gre bodisi za primer dodatne uporabe tehnologije debeloplastnih hibridov z majhno začetno investicijo, bodisi za uporabo nizkotemperaturno sintrane keramike (LTTC), bolj znane kot "Green Tape", na opremi razviti "ad hoc" za velikoserijsko proizvodnjo, ki pa zahteva večji investicijski zalogaj.
Na koncu omenjamo nekaj najnovejših rezultatov firme DuPont na področju organskih materialov za multičip module, kot so fotosenzitivni in "low stress" poliimidi.

Introduction

The evolution in electronics is linked to the continuous development of semiconductors where the reduction in size has to be matched by the evolution in interconnect technology. As the number of functions and the circuit density on the chip increases, the chips become larger with higher number of I/O's, requiring finer lines to interconnect the ICs on the substrate.

Faster signal processing is another characteristic of advanced ICs with typical clock rates of 50-100 MHz for actual microprocessors; single packaged chips mounted printed circuit board are too far apart to handle those clock frequencies, thus requiring either a further integration on the chip, or physically narrowing the distance between the ICs; alternatively possible solutions are to decrease the dielectric constant of the interconnect media or to use transmission line control.

Without entering in the discussion about the integration of semiconductor technologies, not always possible, nor always economical, the solution of interconnecting sev-

eral ICs on the same substrate, known as MultiChip Module (MCM), is certainly a powerful method.

The choice of the interconnect technology depends on several factors such as cost, performance, technology availability and so on; at the same time the interconnection density is also dependent on cost, component dimensions and, to a larger extent, upon the type of ICs used (pitch size and number of I/O's). MCMs require in general fine lines, small vias and multilayer structures to interconnect the ICs on the same substrate with maximum efficiency.

Via formation represents certainly one of the most critical steps in the process of miniaturisation of multichip modules. Fig 1 shows how line density (line pitch) is almost a function of via definition.

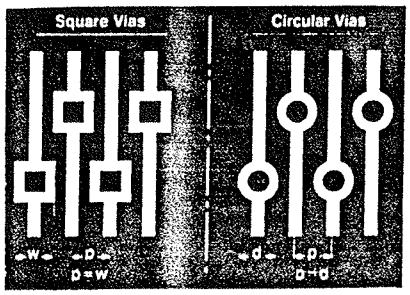

Fig. 1 Line pitch is a function of via definition

Today chips having more than 320 I/O's and with a pitch of 150 microns interconnected on a multilayer represent typically the new requirements for the "high end" of the interconnect market. Furthemore the interconnect substrate is not only to meet the performance, but needs to be cost competitive and to follow the IC price/time typical "learning curve".

MultiChip Modules have opened new opportunities to thick film technology which needs to be accompanied by a certain evolution of the technology itself, to respond to the new challenging requirements in terms of density, miniaturisation, signal speed, controlled impedance and so on. Furthermore ceramic MCMs can be fabricated at reasonable cost not only for the military market but also for commercial applications.

In this brief overview the major emphasis will be on DuPont developments on materials and processes for ceramic MCMs, including Low Temperature Cofired Ceramic (LTCC) technology, better known as "Green Tape". Some of these innovations, to be considered as extension of thick film technology, should allow the thick film hybrid manufacturers and users to extend the area of application of multilayer hybrid circuits without incurring in large capital investments, Furthermore the benefits and the convenience of LTCC technology for ceramic MCMs will be reviewed; Green Tape* requires an important investment in term of equipment and has to be considered as an evolution of thick film technology.

Since the via formation is a critical part of the multilayer interconnect fabrication, we shall review the DuPont techniques capable of resolving small vias, as experienced in practice from the hybrid users standpoint, taking real applications as examples.

Extensions of Thick Film Technology

Diffusion Patterning. In this overview "Diffusion Patterning" system of materials and process will be described; this technique allows to separate the via formation process from the screen printing of the dielectric (Fig. 2) Diffusion Patterning is the step taken by Blaupunkt to increase the complexity and the miniaturisation of their car radio circuits, by achieving finer lines and multilayer structures even for consumer applications.

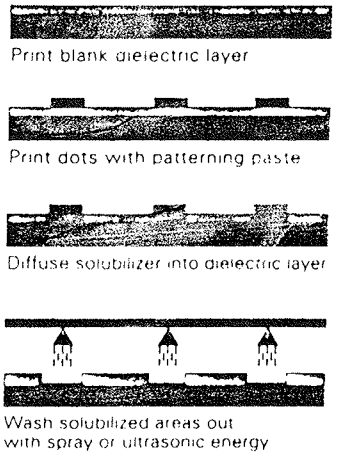

Fig. 2 Schematic of diffusion pattering process

FODEL Photosensitive Meterials. Another method to extend thick film capabilities is to use photosensitive dielectric and conductive pastes (FODEL); Dassault Electronique, after an evaluation of other available technologies, such as silicon-on-silicon, thin film/polyimides and high-and low-temperature co-fired ceramics, has chosen FODEL dielectric and conventional thick film gold for their existing hybrid macromodules. Fig. 3 describes the FODEL photoimaging process. Dassault are also qualifying FODEL dielectric and photosensitive conductor materials for their next generation of High Density MCMs-C.

Evolution of Thick Film Technology

Green Tape*. A new semi-automatic line for the production of approximately 1 million square inches of Green-

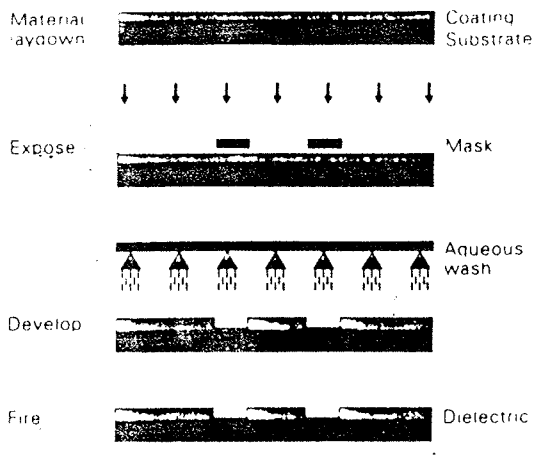

Fig. 3 *Substractive photo imaging*

Tape* circuits has been set up at Sorep in Chateauburg, France.

The line consists of machines specifically designed and assembled for the LTCC technology by Officine Baccini, a high precision thick film equiment manufacturer in Italy.

The key attribute of LTCC is that it offers to the designers the possibility of making multilayer structures with multiple shielding and voltage lines, without incurring in the cost penalty associalted with other interconnect technologies (fig. 4)

The excellent reliability and the good thermal dissipation combined with high density capability of Green Tape* circuits, make the LTCC technology a valid solution for MCMs, with performances similar to thin film circuits but at considerably lower cost. Other advantages of Green Tape* circuits are double side utilisation of the substrate, easy fabrication of "blind" vias and the possibility of special shaped substrates, including cavities for IC chips. The material is also suitable for designing modules with mixed analog and digital signal at high frequency; recent studies indicate that LTCC can be used within the range of 8-30 GHz with high stability.

One of the major advantage of LTCC technology is its potential adaptability to meet the evolving requirements from the market. DuPont offers dielectric tape foils at various thicknesses and dielectric constants. Green Tape* materials can also match TCE of GaAs and Silicon, allowing better reliability of large bare chips mounted on the substrate. Furthermore LTCC will allow to "bury" components, such as resistors and capacitors, in its structure eliminating the need of solder joints and reducing the number of decoupling capacitors.

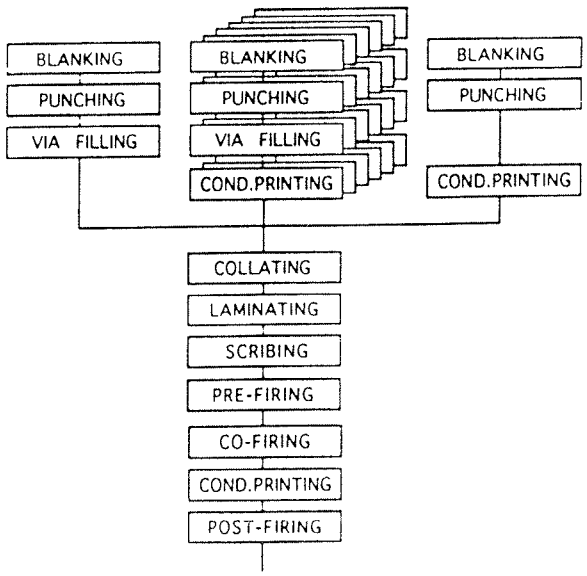

Fig. 4 *Process flow for single sided 8-layer LTCC circuit.*

Thin film/Polyimide technology

There will be a brief overview of DuPont recent developments on conventional and photosensitive poyimides as dielectrics for MCMs, type D, using thin film conductors. A brief discussion on the various type of polyimide materials available from Dupont and on their characteristics will follow.

As a conclusion some preliminary studies between photosensitive polyimides and a low K dielectric tape materials system will also be described.

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Prispelo (Arrived): 11.01.94 *Sprejeto (Accepted): 13.01.94*

UDK 621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 23(1993)4, Ljubljana

A REVIEW OF ADVANCED WET CLEANING

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Key words: semiconductors, integrated circuits, mass production, quality assurance, ultralarge scale integration, silicon wafers, wafer surface, surface microroughness, metal contamination, particle contamination, ultraclean surface, wet cleaning, RCA cleaning method, literature survey

Abstract: In order to manufacture ultralarge scale integrated devices with high performances and reliability in large volume the wafer surface must be kept ultraclean all the time. At present the only suitable method is wet cleaning. Advanced wet cleaning methods were developed from standard RCA cleaning based on hydrogen peroxide mixtures. New efforts were concentrated to prevent silicon surface etching during RCA cleaning, and to prevent hydrophobic Si surface contamination in diluted HF or buffered HF solutions and/or during subsequent DI water rinsing. In this article a review of the latest results in improved wet chemical cleaning is presented.

Pregled sodobnih postopkov mokrega čiščenja silicijevih rezin

Ključne besede: polprevodniki, vezja integrirana, proizvodnja množična, zagotavljanje kakovosti, stopnja integracije ultravisoka, rezine silicijeve, površine rezine, mikrohrapavost površine, kontaminacija s kovinami, kontaminacija z delci, ultra čistost površine, čiščenje mokro, RCA metoda čiščenja, pregled literature

Povzetek: Za masovno izdelavo kvalitetnih in zanesljivih integriranih vezij z ultravisoko stopnjo integracije je potrebno doseči dobro kontrolirano proizvodnjo. Zato je ključnega pomena skrajna čistost površine rezine. Trenutno je edina primerna metoda, ki omogoča ustrezno čiščenje, mokro kemijsko čiščenje. Izpopolnjene metode temelje na standardni metodi RCA, ki imajo za osnovo kisle in bazične raztopine vodikovega peroksida. V zadnjem času so napori usmerjeni proti preprečitvi jedkanja površine v peroksidni raztopini amonijevega hidroksida in preprečitvi kontaminacije hidrofobne površine Si rezine med jedkanjem v razredčenem HF, oz. pufrskem jedkalu, in med poznejšim izpiranjem v vodi. Članek podaja pregled najnovejših dosežkov na področju izpopolnjenega čiščenja silicijevih rezin.

Introduction

The importance of clean Si substrate surface in the fabrication of semiconductor devices has been recognized since the early days of semiconductor manufacturing in the 1950s. As the requirements for improved device performances and reliability in the era of VLSI and ULSI technologies have become more and more stringent, methods to avoid contamination and processes to generate ultraclean surfaces have become critically important. Now it is generally accepted that over 50% of yield losses in modern IC fabrication is due to the microcontamination. Especially detrimental effect have metal impurities if present on the wafer surface; during high temperature processing they might diffuse into the wafer interior. Another problem are the organic contaminants and native oxide that can prevent selective epitaxy. Therefore, microcontamination must be minimized before every high temperature step (oxidation, diffusion, epitaxy). Similarly, contaminants (especially particles) must be removed from the surface before and/or after low temperature steps (CVD, dopant implantation, plasma processes). Last but not least, wafers must be postcleaned after photoresist stripping at every mask level.

Throughout the history of the semiconductor manufacturing many wafer cleaning techniques have been developed and been used. But the wet process is still employed to clean the Si wafer due to its remarkable characteristics: it causes no damages on the wafer and it is effective at low temperature. Foundations of the modern wet cleaning were established by W. Kern et al. in 1965 in RCA and published in 1970, Ref. /1/. The original two step cleaning process did remain basically unchanged for more than 25 years.

The state of the Si surface in modern technologies with critical dimensions reduced to the submicron and even sub-half micron level is becoming far more important than in the 1970s. With the introduction of Total Reflection X-Ray Fluorescence Spectroscopy (TRXRF) for the surface contamination analysis, Scanning Tunneling Microscopy (STM) and Atomic Force Microscopy (AFM) for the surface microroughness determination, new standards for the state of the silicon surface have been established. Besides cleanliness of the surface, microroughness becomes increasingly important factor in the 1990s.

Wet cleaning procedure

During the early stage of semiconductor manufacturing (until the 1970s), the Si wafer cleaning was based on the organic solvent extraction, boiling nitric acid, aqua regia, concentrated hydrofluoric acid and mixtures of sulfuric-chromic acid. All of the methods mentioned had

some problems, such as contamination with chromium or waste disposal in the case of the sulfuric-chromic acid mixture. Generally speaking the chemicals had high level of impurities and particles and so tended to contaminate the surface of the wafer. Particles from the wafer surface were removed by ultrasonic treatment in detergent solution or by brush scrubbing. Malfunction of these methods can cause serious problems.

Successful immersion wet cleaning of the wafer surface consists of three basic steps:

- removal of organic contaminants
- oxide removal
- removal of alkaline and metal contaminants.

Two different approaches have been adopted:

a) RCA process mentioned in the introduction with so called oxide terminated silicon surface,

b) dilute HF cleaning process with hydrogen terminated silicon surface.

Both approaches have pros and cons. RCA cleaning is relatively complicated (3 different solutions, instability of the solution due to decomposition of H_2O_2 at elevated temperatures, problems of cross contamination, Si surface etching, Ref. /2/) but yields the Si surface passivated with 1.5 nm of relatively clean native oxide. On the other hand, the dilute HF cleaning is relatively simple and generates chemically cleaner bare silicon surface. Unfortunately this clean hydrophobic surface can be easily contaminated with particles and organic material from rinsing DI water /3,4/. It was reported in Ref. /6/ that the organic contamination can carbonize at high temperatures in nonoxidizing atmosphere and form β-SiC that can start polycristallinic growth during epitaxial deposition. Even contamination with phosphorous from DI water with about 100 ppb of TOC were reported, Ref. /4,5/.

RCA cleaning

Original RCA process for bare and oxidized silicon wafers was based on a two step oxidizing and complexing treatment in hydrogen peroxide solutions:

The first process step was designed to remove organic surface film by oxidative breakdown and dissolution in hot mixture of water diluted ammonium hydroxide and peroxide (10 min, 5:1:1 H_2O:H_2O_2:NH_4OH, 75-80°C, known as SC-1 or APM). During this step, group IB and IIB metals as well as heavy metals Au, Ag, Cu, Ni, Cd, Zn, Co and Cr are dissolved and removed by complexing by ammonium hydroxide; so called amino complexes are formed ($Cu(NH_3)_4^{+2}$ in case of copper).

In the second step the rinsed wafers are exposed to a mixture of hot water diluted hydrogen peroxide and hydrochloric acid (10 min, 6:1:1 H_2O:H_2O_2:HCl, 75-80°C, known as SC-2 or HPM). During this step the alkali ions and cations such as Al^{3+}, Fe^{+3} and Mg^{+2} that in NH_4OH form insoluble hydroxides are removed. The second step is also designed to eliminate all metallic contaminants that were not entirely removed during the first alkaline cleaning step.

After the introduction in the 1970s the original scheme have been modified. Optional sulfuric-hydrogen peroxide (10 min, 2:1 H_2SO_4:H_2O_2, 100-130°C known as SPM) mixture as a first step to remove gross organic contaminants was introduced. The contaminated hydrous oxide formed during APM cleaning can be removed during another optional step by etching off in diluted or buffered HF (DHF, BHF) before HPM treatment. However, unless ultra pure and particles free point-of-use ultrafiltrated HF is used, more harm than good can be done. Highly reactive HF treated Si surface can be easily contaminated with organic contaminants and particles from HF solution, DI water and air. Contrary to the APM solution, HPM does not eliminate these contaminants. If the preclean is used, than DHF step can not be harmful, since APM removes all the contaminants. On the other hand, the level of contamination in APM can be significantly reduced using ultra pure peroxide with low Al and stabilizer content. Bare silicon wafers after HPM treatment should not be exposed to DHF, since the clean passivated surface would be destroyed, and could easily be recontaminated.

Original immersion technique using fused silica beakers and overflowing quenching with DI water to terminate the reaction have been changed during the years to more refined automated wet bench immersion systems (for instance Ref. /7/). There are also tendencies to change the original immersion technique to centrifugal spray cleaning /8/, megasonic cleaning /9,10/, closed system chemical cleaning /11/, and dry (vapor) wafer cleaning /12/.

Literature survey

From the 1972, when Henderson /6/ published that HF cleaning after HPM can produce roughening and carbon contamination of the surface during vacuum heating, up to now many independent articles verifying the effectiveness of RCA cleaning have been published. For instance Meek et al. /13/ showed that APM/HPM cleaning is much more effective removing Cu and Ca as HF-HNO_3. Gluck /14/ repored in 1978 that desorption efficiency of APM for gold is better than efficiency of HPM, but the sequential treatment APM+HPM is the most effective method to remove gold in high (10^{14} at/cm^3) concentration. In 1983 Phillips et al. /15/ compared the efficiency of various aggressive reagents including aqua regia, hot fuming HNO_3, H_2SO_4-H_2O_2, APM and HPM. The most effective procedure to clean with inorganic materials purposely contaminated wafers was SPM followed by APM/DHF/HPM sequence. Their results were confirmed

in 1986 by Becker et al in Ref. /16/. It was also shown that the reversed sequence DHF/APM/HPM is far more effective for particle removal but slightly less for metal ion removal as the original one.

RCA cleaning generates very clean surfaces as long as very clean chemicals are used. It was reported /17,18/ that high Al contamination found on the wafer surfaces after APM and five times less after HPM clean, originated from even sub ppm contaminated hydrogen peroxide. In 1989 Morota et al. /19,20/ postulated the most appropriate model for contamination of the silicon surface during cleaning in APM, HPM and DHF solutions. The absence or presence of the SiO_2 film on the surface affects adsorption of metals. Desorption of Al and Fe was most effective with DHF, and desorption of Cu and Cr with HPM. Metals with high enthalpy of oxide formation adsorb on oxidized Si surface by oxide formation (Al, Cr, Fe), whereas metals with high electronegativity (Au, Pt, Ag) deposit electrochemically onto the bare Si surface. Tables I and II represent tendencies of metals to precipitate directly onto the silicon (I) and to form oxide (II).

Particle removal efficiency was studied by many authors. They all agree that reversed sequence HF/APM/HPM generate the cleanest surface, Ref. /3,4,16,21/. Later Ohmi et al. /22/ showed that 1:1:5 APM efficiently removes particles larger than 0.5 μm, but increases the number of smaller ones, measured as a haze, and latter recognized as surface etching. APM solution with lower NH_4OH concentration effectively removes all particles, Ref. /22/.

Negative aspects of RCA cleaning are etching of the silicon surface in alkaline solution APM. Up to the end of 1980s measurements did not reveal any attacking of the

Table I
Electronegativity of metals according to Ref. /30/.

$M^+ + e^- \text{---> } M$

Element	Electron Negativity (Pauling)	Half-Cell Reduction Potential /V/	-
Au	2.4	1.68	⇑
Pt	2.2	1.19	
Ag	1.9	0.80	
Hg	1.9	0.79	
Cu	1.9	0.34	
Si	1.8	0.10	Tendency to be precipitated on bare Si
Pb	1.8	-0.13	
Sn	1.8	-0.14	
Ni	1.8	-0.23	
Fe	1.8	-0.41	
Zn	1.6	-0.76	
Al	1.5	-1.66	
Mg	1.2	-2.34	
Ca	1.0	-2.87	
Na	0.9	-2.71	
K	0.8	-2.92	

Table II
Enthalpy of oxide formation according to Ref. /30/.

$M + O_2 \text{---> } MO_2$

$\Delta H < 0$, (Heat Releasing Process)

Oxide	ΔH_{25}^{293} /kJ/mol/	-
Al_2O_3	-1675	⇑
Cr_2O_3	-1130	
CrO_2	- 583	
CrO_3	- 580	
Fe_3O_4	-1118	
Fe_2O_3	-822	
SiO_2	-909	Tendency to be included into oxide film
NiO	-241	
CuO	-155	

silicon surface as long as the hydrogen peroxide concentration was not depleted to less than 75% of the original recommended concentration, Ref. /4/. However, severe silicon surface roughening was reported in Ref. /24/ for cleaning in water diluted NH_4OH, less severe for BHF and none for APM. On the other hand, it was reported that APM (80°C, 5:1:1) solution slightly etch the SiO_2 and Si_3N_4 films. Measured etch rates were from 0.13 /4/ to 0.4 nm/min /25/ for thermal SiO_2 film, and 0.09 /4/ to 0.2 nm/min /25/ for CVD deposited Si_3N_4 film.

Extensive work of Grundner et al. /26,27/ showed that the hydrophobic silicon surface state after the DHF dip is due to Si-H, some $Si\text{-}CH_x$ and Si-F groups, while hydrophilicity is caused by Si-OH groups. It was also shown that the contact angle of a water droplet is in good correlation with the silicon surface status. Typically, for the hydrophobic surface the angle is higher than 80, wheras for the hydrophilic one is less than 20. Generally, the higher is the contact angle after cleaning, the better is quality of the thermally grown oxide.

Present understanding of Si surface cleaning

Any effective cleaning must left undamaged, smooth, ultraclean Si surface completely free from particles, organic materials, metallic impurities, adsorbed molecule impurities and native oxide. The very first step of any wafer cleaning must be the removal of organic

surface contamination preventing full exposure of the surface to the action of subsequent cleaning. This is mostly done by SPM and partially by APM cleaning. Control of the first technique is quite poor due to high temperature of the mixture and its composition instability. In beginning of the 1990s the new, low temperature Ozone-Injected Ultrapure Water techniques have been developed, Ref. /36/.

It is expected that it will replace the old SPM solutions due to high organic impurity removal efficiency, better controllability of the process and less chemical waste.

Removal of metallic impurities

Metallic impurities on the wafer surface can cause irreversible damage on semiconductor devices such as increase of p/n junction leakage current, poor dielectric breakdown voltage, and a decrease of carrier lifetime. Results from Figs.1 a and b show that for the modern sub and sub-half micron ULSI devices the contamination of the silicon surface should be kept below 10^{11} at/cm^2

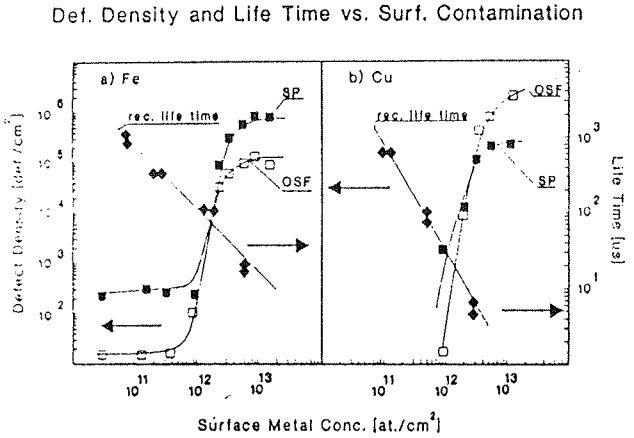

Figure 1: Dependence of the surface defects (saucer pits: SP, oxidation stacking faults: OSF), and the recombination carrier lifetime on the surface metal concentration after the two step annealing (1150°C/1h N_2 + 1000°C/16h O_2); (a)-Cu and (b)-Fe, Ref. /28/.

in order to prevent these damages, Ref. /28/. Such a low surface concentration can be assured only with ultra clean chemicals (contamination below 10 ppb), as shows Fig.2. This limit is significantly lower than it was obtained at the end of 1980s. Concentration of typical unwanted metals (most frequent are Fe, Al and Ca) in native oxide for the commercially available wafers was measured in the range between 10^{11} to 10^{13} at/cm^2, Ref. /29/. In the same range was the contamination measured after plasma etching and ion implantation /37/. APM step of the conventional RCA cleaning can hardly reduce the contamination to the values below 10^{11} at/cm^2. The reason for this is the tendency of Al, Cr and Fe to form oxides (Table II) on the silicon surface during APM cleaning. The tendency for contamination is directly related to the cleanliness of the APM (especially hydrogen peroxide) chemicals. As shows Fig.3, Ref. /31/, subsequent HPM treatment reduces the unacceptable high iron level to below XRTRF detection limit 3x10^{10} at/cm^2. Anyway, the most effective way to keep the contamination as low as possible is to use ultra pure chemicals and/or to remove the contaminated thin oxide by the controversial etching in water diluted HF.

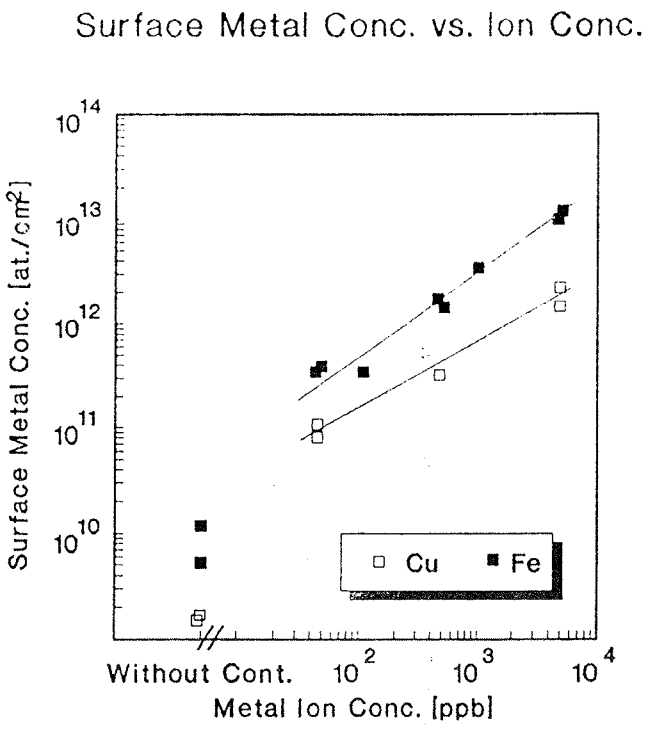

Figure 2: Relationship between the surface metal concentration measured by ASS and metal concentration in the contaminated solution. Ref. /28/.

Highly electronegative metal ions (Cu...) are directly adsorbed onto the Si surface (Table II). They can be only partially removed by HPM step of RCA cleaning which

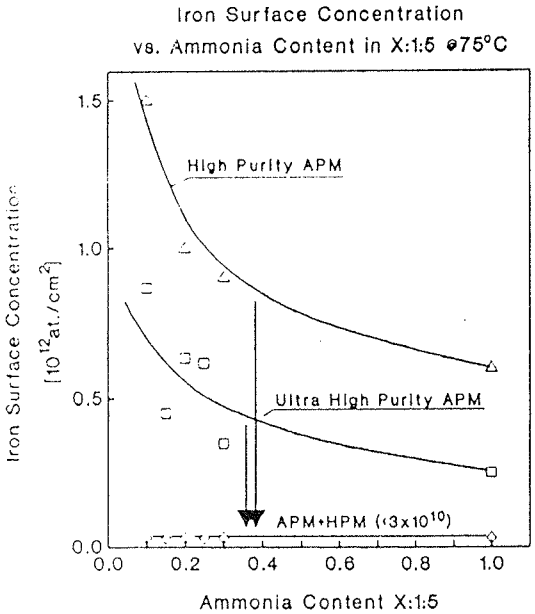

Figure 3: Iron surface concentration measured after APM cleaning step with chemicals of different purity levels. Iron contamination is significant even after ultra high pure APM clean. Final HPM cleaning is essential to get very clean surface with iron contamination below detection limit 3x10^{10} at./cm^2, Ref. /31/.

leaves sometimes unwanted passivated surface. In a case where the hydrogen terminated surface is needed the last step must be DHF cleaning. Unfortunately it is ineffective to remove directly adsorbed ions like Cu. Even more, the surface can easily be contaminated with these metals (as well as with particles and organic contaminants) in contaminated conventional DHF (Fig. 2) and/or during final DI water rinse.

Cross contamination can be prevented and metallic impurities removal can be enhanced by addition of H_2O_2 to the DHF. Fig. 4 shows that improved DHF (0.5%HF +10%H_2O_2) almost completely prevents cross contamination of p and n silicon surface in up to 1 ppm contaminated solution, but not of the doped n^+ and p^+ surfaces. It is also important to prevent contamination during BHF etching of thick oxide layers. The addition of fluorocarbonated (FC) surfactants to improve wetability of the Si surface also reduces the cross contamination of p, n and p^+ surfaces to below 10^{11} at/cm^2 as shows Fig 5. Only contamination on n + surfaces can not be prevented in BHF63 (6%HF+30% NH_4OH) contaminated with 10 ppb of Cu.

Once the surface is contaminated it is very important to clean it. Besides the mentioned RCA cleaning very good results on n and p type wafers can be obtained with improved DHF, while BHF solutions even with added surfactants are not effective. Fig. 6, Ref. /30/, shows the ability of different solutions to clean copper contaminated n and p wafers (10 min dip in 1ppm contaminated water increase surface concentration to 10^{13} - 10^{14}

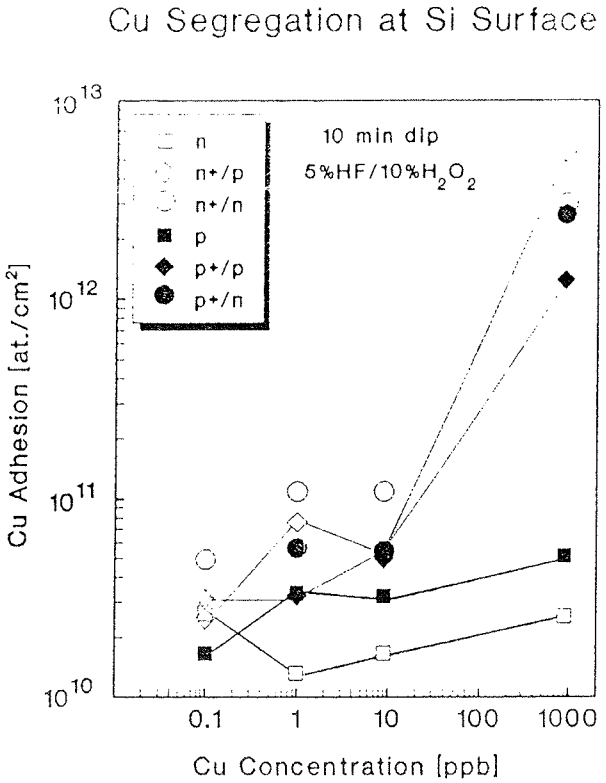

Figure 4: Copper segregation at six different Si surfaces in contaminated 0.5% HF+10% H_2O_2 solution at room temperature, Ref. /37/. (a) n, n^+ on n, n^+ on p, (b) p, p^+ on p, p^+ on n Si wafers.

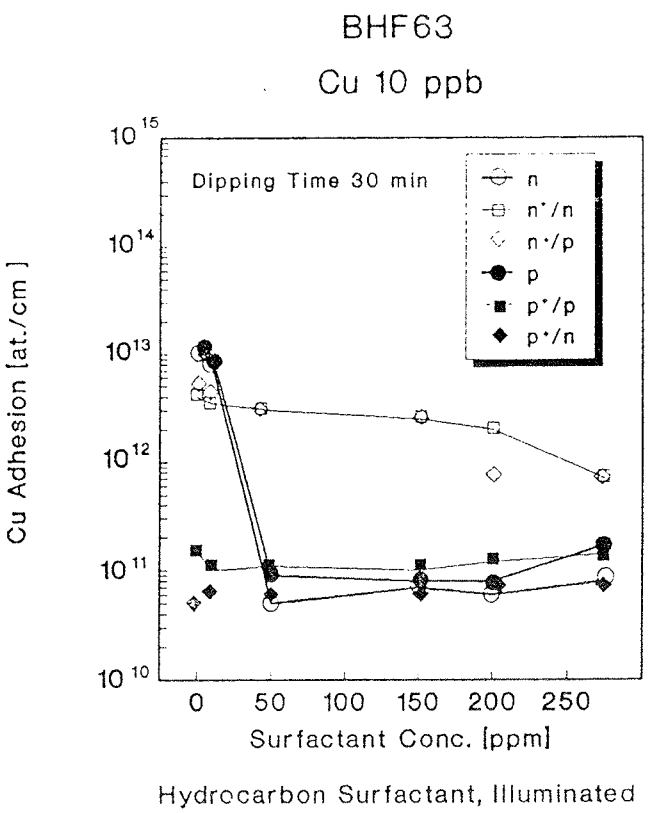

Figure 5: Cu segregation at six different Si surfaces in contaminated (10 ppb Cu) BHF63 with hydrocarbon surfactant dependent on surfactant concentration, Ref. /37/.

at/cm^2). Obviously, DHF (0.5% HF), as well as BHF (A is the conventional solution with the NH_4F concentration of 35-38%, and B is advanced solution: 17% of NH_4F, 0.17%HF and 400 ppm of a surfactant) do not remove copper from the surface. APM and HPM solutions lower the Cu surface concentration to the 10^{11} level. The most effective is cleaning in water diluted solution of 0.5%HF+10%H_2O_2 for more than 1 min at room temperature. In this way high Cu concentration can be

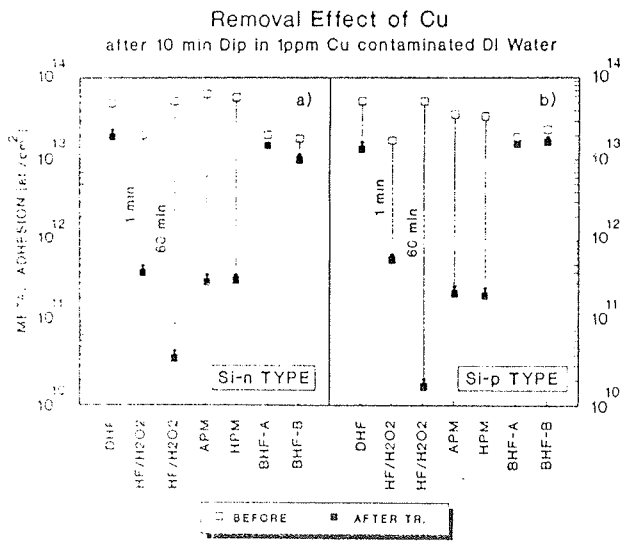

Figure 6: Copper surface contamination removal efficiency for several cleaning methods: (a) n-type, (b) p-type (100) Si surface, Ref. /30/.

reduced to the acceptable level below 10^{11} at/cm^2 in a relatively short time, Ref. /37/.

Unfortunately advanced DHF solution with hydrogen peroxide does not remove the copper-like metals from n^+ and p^+ surfaces. At present, there is no other choice but to use the APM+HPM cleaning.

Particle adhesion and removal

Efficiency of APM and other alkaline solutions to remove particles from the wafer surface has been known for almost 10 years. The most comprehensive explanation of the particle removal mechanisms have been postulated by Itano et al. /32/. According to their results the particle deposition (or removal) depends on the pH value of the solution. With increased pH value, silicon etch rate increases, whereas deposition rate decreases. For pH values higher than 10, the haze count increases very abruptly due to irregular surface etching.

Figure 7 shows particle removal efficiency for APM solutions with different NH_4OH concentrations (X:1:5) at 80°C, Ref./32,33/. The highest efficiency for 10 min cleaning is obtained in 0.05:1:5 solution. For concentrations higher than 0.1:1:5, efficiency drops due to the extensive etching.

Particle removal efficiency depends on etching of the silicon surface. Fig. 8 shows etch rates as measured by

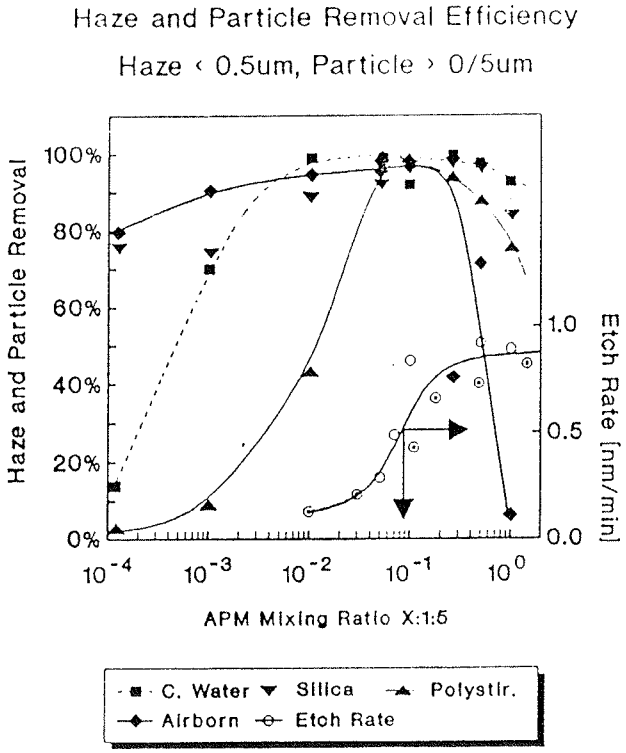

Figure 7: Haze and particle removal efficiency in APM with different NH_4OH concentrations at 80°C. The optimum solution is 0.05:1:5 with etch rate 0.25 nm/min. Solutions with etch rate higher than 0.6 nm/min (1:1:5) may cause surface etching, Ref. /32,33/.

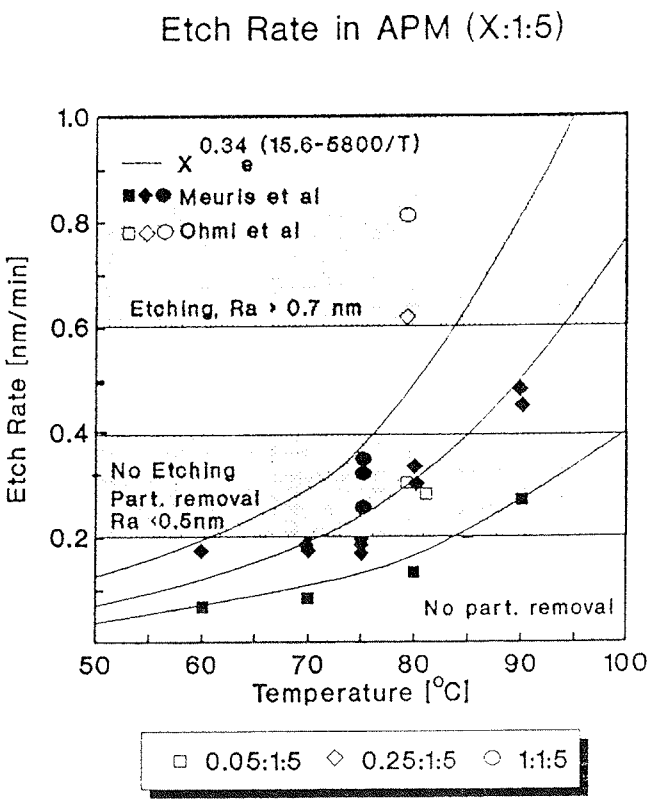

Figure 8: Silicon etch rate in APM as measured by Meuris et al, Ref. /31/ and Ohmi et al, Ref. /33/. In Ref. /31/ the cold water is used for rinsing after APM cleaning, while in Ref. /33/ hot water is used. The most efficient particle removal is obtained with solutions having etch rate 0.2 - 0.4 nm/min. For the etch rate higher than 0.6 nm/min the silicon surface is roughened with average microroughness R_a < 0.7 nm. Si surface microroughness

Meuris et al. /31/, and Ohmi et al., /33/. A large discrepancy in etch rates is due to the difference in wafer rinsing. In Ref. /31/ wafers were rinsed in cold DI water, while in Ref. /33/ wafers were rinsed in hot DI after APM cleaning. It is also shown in Ref. /33/ that the surface roughness is almost 2 times higher for the hot water rinse than for the cold water rinse. In Fig. 8 one can see two main regions regarding particle removal efficiency. Safe and efficient particle removal is guarantied for solutions with etch rate 0.2-0.4 nm/min. Average surface roughening in this region is below 0.5 nm. Solutions with etch rate over 0.6 nm/min cause extensive surface roughening with average R_a > 0.7 nm. Solutions with etch rate from 0.4 to 0.6 nm/min should also be avoided due to unreliable control of the etch rate. Solutions with the highest efficiency and low etching rate (0.25 nm/min) are 1:1:5 solution at 65°C, 0.25:1:5 at 75°C with cold water rinse and 0.05:1:5 at 80°C and hot water rinse.

Sisurface microughness

Dielectrics in modern ICs are very thin. Oxide thicknesses are sometimes even less than 10 nm. For such thin layers, the average surface microroughness R_a should be close to the atomic dimensions ($R_a \cong 0.2$ nm).

Fig. 9 shows microroughness measured by STM after cleaning in different solutions for 10 min, Ref./33/. One can see that HPM and SPM cleaning do not damage the surface (small increase of R_a for SPM is due to 4 times repeated cleaning). On the other hand, frequently used conventional BHF with NH_4F concentration of 35-38% drastically increases microroughness. Advanced BHF (17% of NH_4F, 0.17% of HF, 400 ppm of surfactant) does not attack the surface. Surprisingly, even 0.5% DHF significantly deteriorate the surface. Triplett et al. even show in Ref. /34/ that surface microroughness after DHF etching depends on the rinsing time in water. APM cleaning increases microroughness as one can see in Fig. 9. Microroughness depends on the silicon material ($R_a^{epy} < R_a^{FZ} < R_a^{CZ}$), surface point defect concentration (after 4h wet oxidation at 1000oC $R_a^{epy} \cong R_a^{FZ} \cong R_a^{CZ}$), and APM etch rate.

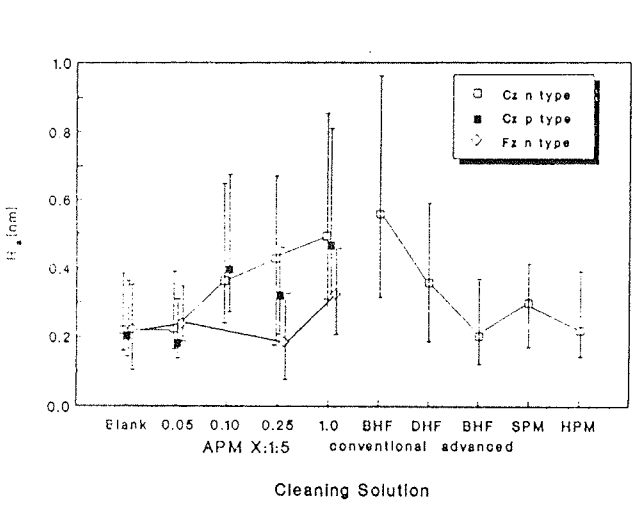

Figure 9: Average surface microroughness R_a of n-type Cz wafer after cleaning in different solutions under the following conditions: etch time 10 min, APM and HPM temperature 80°C, 4 times repeated SPM cleaning and cold DI water rinse after APM, Ref. /33/.

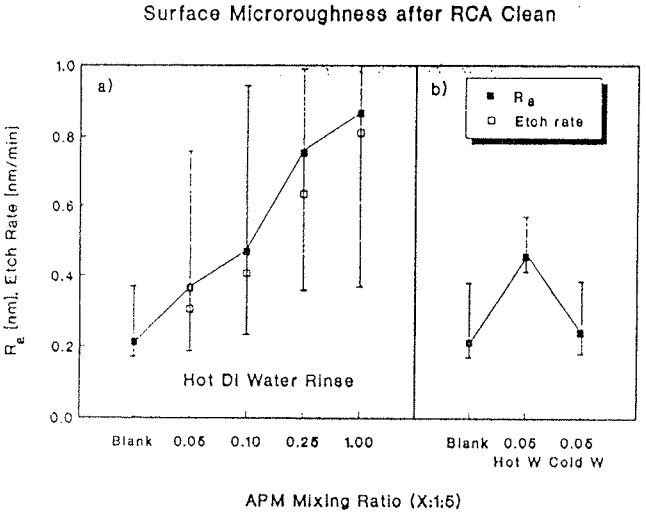

Figure 10: (a) Average surface microroughness R_a of wafers treated in an entire RCA cleaning process with different APM solutions and using hot water rinse after APM. (b) Surface microroughness after APM cleaning in 0.05:1:5 solution and hot and cold (room temperature, RT) DI water rinse, Ref. /33/.

Fig. 10.a illustrates the relationship between microroughness after RCA clean, etch rate, and APM concentration, Ref. /33/. Average microroughness after 10 min etching in APM at 80°C with hot water rinse equals about 10% of the removed silicon thickness. As shows Fig. 10.b surface roughening can be halved by using cold instead of hot water rinse after APM step.

A parameter directly related to the long term quality of the oxide is its charge to breakdown (Q_{bd}). Results show that it decreases with average surface microroughness. The dependence is shown in Fig.11 for measurements with a constant electric field 9.5 MV/cm, Ref /33/. Obviously the surface microroughness must be kept below 0.4 nm to assure the highest possible oxide quality ($Q_{bd} > 30$ C/cm^2).

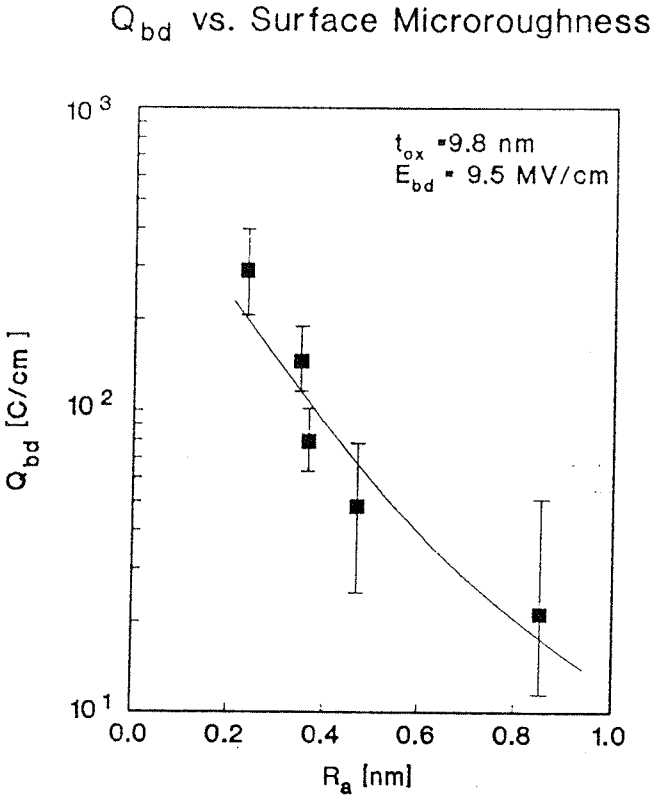

Figure 11: Surface microroughness dependence of Q_{bd} under a constant field of 9.5 MV/cm for p-type CZ wafer, Ref /33/.

Hydrogen terminated surface

The thickness of thermal grown thin oxides in modern ULSI IC technologies approach the thickness range of the native oxide grown on the Si surface exposed to air and to the thin oxide grown during cleaning in the APM and HPM solutions. Such an oxide can not be tolerated; so the last cleaning step must be etching of the contaminated native oxide in the DHF. After the DHF cleaning the Si surface is hydrophobic. In Ref. /35/ was shown that the contact angle of a water droplet is a very good measure of the surface status and oxide quality. When

the contact angle exceeds 60° the surface is covered with less than 1% of oxygen monolayer. Typically contact angle for the DHF cleaned and DI water rinsed surface is about 70°.

As it was shown the DHF treatment can cause metal and particle contamination. To prevent particle adhesion and improve cleaning efficiency the effects of the following three possible additives have been studied during the last years:

- hydrogen peroxide, H_2O_2,
- isopropanol (IPA),
- FC surfactants

In Fig. 4 it was already shown that the addition of H_2O_2 into the DHF (0.5%) enables Cu removal from contaminated silicon surface and prevent Cu segregation onto p and n silicon surface in contaminated DHF. Fig. 12, Ref./33/, represents Cu removal efficiency from n type Si for H_2O_2-DHF solution at room temperature as a function of hydrogen peroxide concentration. As one can see almost complete removal of Cu is guarantied for 60 min cleaning in solution with 5-10% of H_2O_2 in DHF. Even such a prolonged etching in DHF with more than 0.1% of H_2O_2 added does not increase the average surface microroughness from the initial value and does not destroy the hydrophobic nature of the Si surface. The contact angle measured after cleaning in 3%H_2O_2 - 0.5%DHF exceeds 60, Ref. /35/, whereas for the 0.5% DHF exceeds 70. Unfortunately addition of hydrogen peroxide to the DHF does not solve the problem of particles contamination in DHF solutions. Only minor improvements (times 2) in particle contamination was reported in Ref. /38/.

Very significant reduction of the particle deposition was reported for DHF mixtures with minute amounts of IPA, Ref. /38/. Addition of 200-1000 ppm of IPA to 0.5%DHF almost does not change the state of the surface. The contact angle after 60 s dip in solution with 200 ppm IPA is identical to what is obtained when no IPA is added and it is no longer changed by subsequent DI- water rinse. When 1000 ppm of IPA is added to the 0.5%DHF solution the particle density after rinsing is comparable to what is obtained after standard RCA clean. As a result, almost 50% increase in yield on gate oxide capacitors was reported.

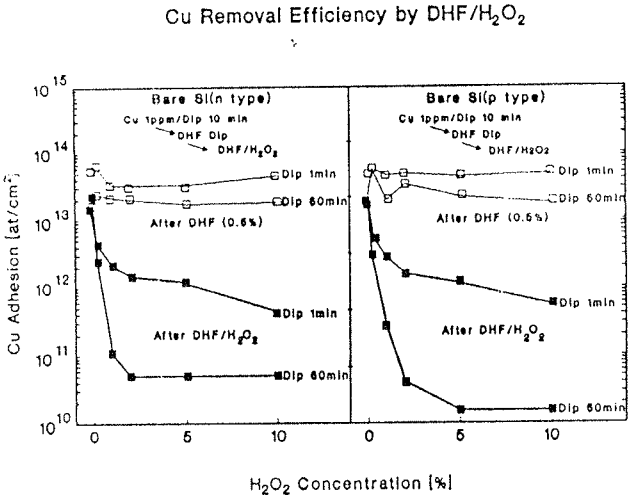

Figure 12: Copper removal efficiency by DHF-H_2O_2 with H_2O_2 concentration ranging from 0-10% for 10 and 60 min dipping time, Ref. /33/.

Effect of addition of surfactants to the DHF solution is still under study. But it is already known that the contact angle after treatment nearly equals that one measured after treatment with 0.1%IPA +0.5%DHF, Ref. /35/.

Conclusions

An ultraclean Si wafer surface is essential for achieving the advanced ultra large scale integrated production which incorporates low-temperature and high selectivity processes. Such a surface is completely free of particles, organic impurities, metallic impurities, native oxide, surface microroughness and adsorbed impurities. Since metallic impurities can cause fatal damage to device characteristics the contamination level must be suppressed to below 10^{11} atom/cm^2 . The only method to remove trace impurities from the surface at the present is wet cleaning.

An advanced improved wet cleaning process proposed in Ref. /36/ consists of the following steps:

- removal of organic contaminants in $H_2O + O_3$ at room temperature. This is highly effective replacement for classical SPM cleaning at 130°C. Total removal of organic contaminants is essential for effectiveness of subsequent cleaning steps.
- removal of particles, organic and metal impurities in APM. Advanced 0.05:1:5 solution is highly effective to remove surface particles and partially effective to remove Cu like metals precipitated onto the surface, and does not deteriorate the surface smoothness.
- removal of native oxide and metals in DHF + H_2O_2 generate native oxide free surface clean of metals which tends to incorporate into the native oxide (Fe, Al, Ca...) as well as Cu-like metals. This solution is very appropriate to clean n and p type surfaces with the highest demands for cleanliness and smoothness, such as the wafer surface before gate oxidation. Since this solution attacks the n^+ and p^+ surfaces, the only method to remove metal contaminants from them is still APM + HPM cleaning.

Further improvements in cleaning could be obtained using DHF solution heated to 70°C, cleaning in an inert ambient, or even in using dry wafer (vapor) cleaning in an enclosed system, as it is for instance Advance 600/2 Vertical Reactor Cluster Tool for polysilicon gate application /35,39/. In such a system, the wafer surface is never exposed to air, neither before oxidation, nor before polysilicon deposition. The result is a significant improvement of the oxide quality.

In order to decrease the metal concentration on the Si wafer surface to less than 10^{10} atoms/cm^2, the concentration of metals with electronegativity higher than Si (for example Cu) in chemicals and water should be de-

creased to less than 10 ppt which is hard to reach even with present ultraclean chemicals. A very promising way to delivered such clean chemicals is point of use chemical generation which is useful for preparation of HF, HCl, NH_4OH and ozonated ultra pure water.

Acknowledgement

The author would like to thank J. Razinger for helpful discussions and a carful reading of the manuscript.

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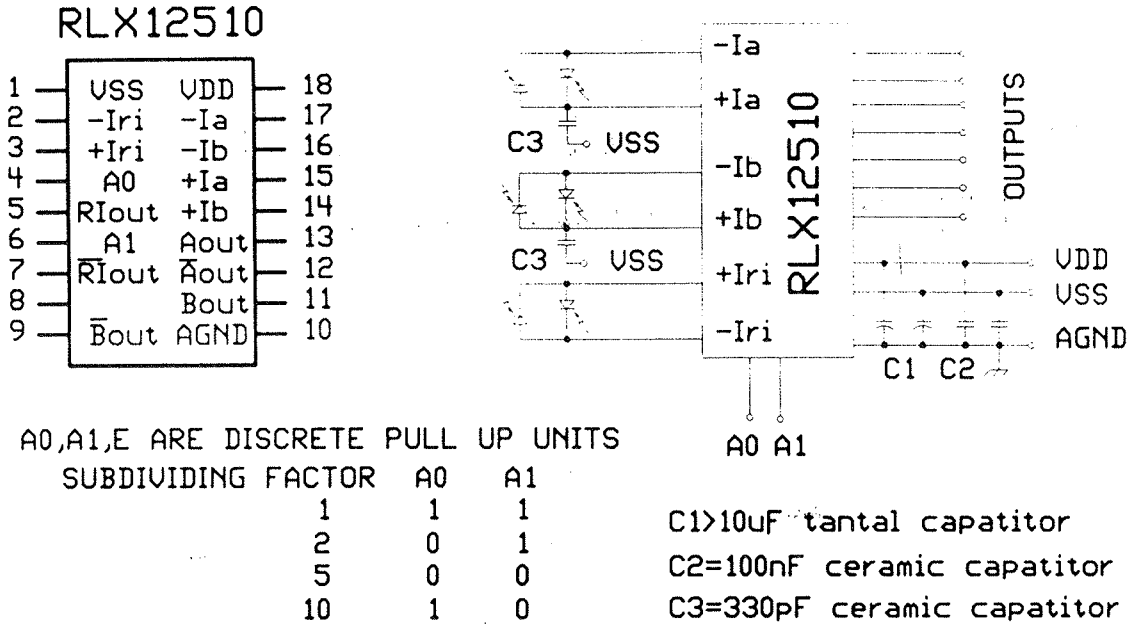
Prispelo (Arrived): 15.09.93 ***Sprejeto (Accepted): 21.11.93***

UPORABA POLPREVODNIŠKIH IN MIKROELEKTRONSKIH KOMPONENT

Mikroelektronika v službi natančnega merjenja pomikov in zasukov
Integrirano vezje RLX 12510

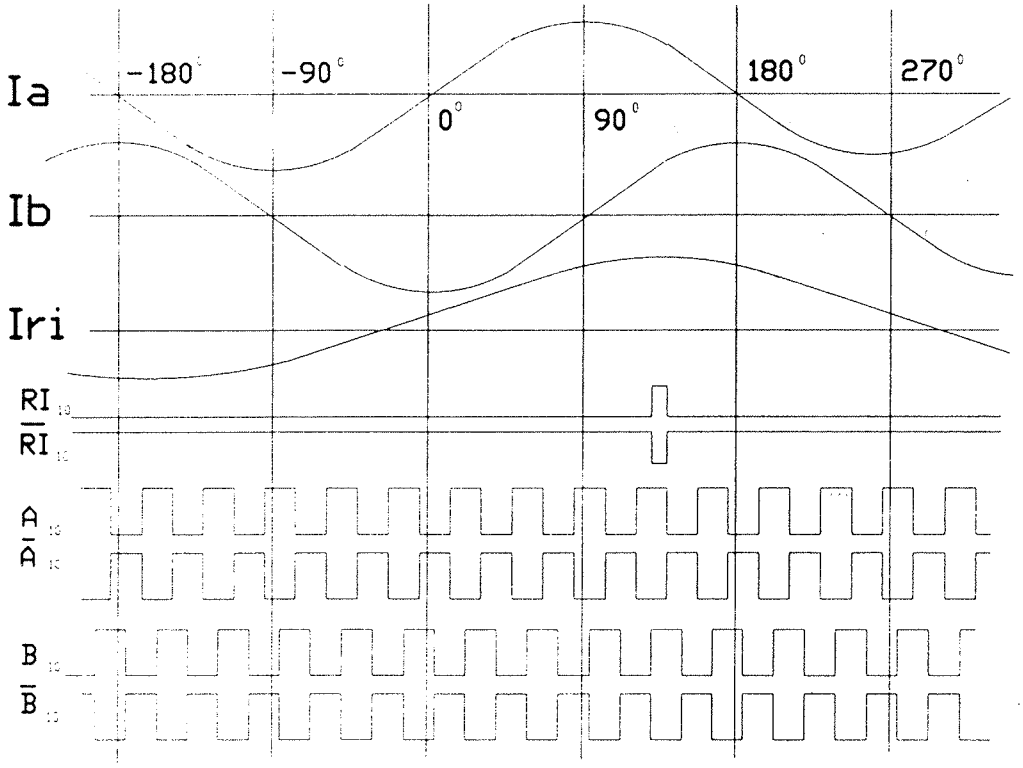
Potrebe po natančnem merjenju pomikov in zasukov se v današnjem času povečujejo z rastočo avtomatizacijo industrijskih procesov. Optoelektrični princip merjenja se uporablja že dalj časa za natančno merjenje na obdelovalnih in merilnih strojih, v kontrolnih, optičnih in navigacijskih napravah. Merilni dajalniki (inkrementni in



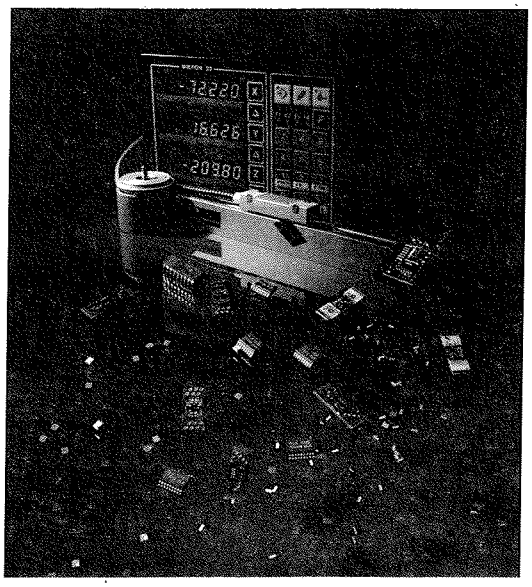
A0,A1,E ARE DISCRETE PULL UP UNITS

SUBDIVIDING FACTOR	A0	A1
1	1	1
2	0	1
5	0	0
10	1	0

C1>10uF tantal capatitor
C2=100nF ceramic capatitor
C3=330pF ceramic capatitor



Aplikacija vezja RLX 12510 v merilnem dajalniku pomika ali zasuka



absolutni) se odlikujejo po relativno velikem območju merjenja (nekaj metrov) in visoki natančnosti (+-1μm/m). Merilna dolžina in natančnost sta lastnost merilnega rastra vgrajenega na primernem nosilcu. Pomemben delež pri doseganju optimalne ločljivosti in natančnosti pa ima obdelava merilnih signalov, ki se generirajo na fotodiodah pri medsebojnem premikanju fazno zamaknjenih rastrov.

Merilni dajalniki pomikov in zasukov se prek signalnih kablov povezujejo z elektronskimi napravami. Digitalni signali so za prenos in nadaljno obdelavo najprimernejši. Zaradi tega moramo šibke sinusne signale iz fotodiod okrepiti in pretvoriti v digitalne. Za dosego primerne ločljivosti moramo opraviti tudi dodatno analogno digitalno delitev.

Funkcijo pretvorbe opravlja naročniško integrirano vezje RLX12510, ki vhodne sinusne signale pretvori v digitalne tako, da eno periodo sinusa razdeli na 1, 2, 5, ali 10 period digitalnega signala. Faktor pretvorbe izbiramo z dvema digitalnima vhodoma. Vezje pretvori in obdela tudi referenčni signal. Vezje je izvedeno v 5 mikronski CMOS tehnologiji, odlikuje se z relativno nizko porabo, visoko vhodno frekvenco in enojnim napajanjem.

V podjetju RLS merilna tehnika se ukvarjamo z razvojem in proizvodnjo merilnih dajalnikov in pripadajoče elektronike. Za lastne potrebe in za potrebe trga smo skupaj z Laboratorijem za mikroelektroniko Fakultete za elektrotehniko in računalništvo v Ljubljani razvili vezje RLX 12510. Razvoj na tem področju poteka naprej v smislu združevanja fotodiodnega senzorskega polja s pretvorniškim vezjem na enem samem monolitnem vezju.

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KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA

21. MEDNARODNA KONFERENCA O MIKROELEKTRONIKI, MIEL'93
29. SIMPOZIJ O ELEKTRONSKIH SESTAVNIH DELIH IN MATERIALIH, SD'93
29.september - 1.oktober, 1993, Bled, Slovenija

MIEL-SD'93 je letos združil dve prireditvi z dolgoletno tradicijo: 21.Mednarodno konferenco o mikroelektroniki, MIEL'93 in 29.Simpozij o elektronskih sestavnih delih in materialih, SD'93. Organiziral ju je MIDEM, Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale.

Konferenca je potekala na Bledu od 29.septembra do 1.oktobra 1993. Tudi letos je to bila priložnost za srečanje številnih strokovnjakov iz vse Evrope z namenom obravnavati nove raziskovalne in razvojne dosežke na področjih, ki jih zajema društvo MIDEM. Udeleženci so prišli iz Avstrije, Češke, Hrvaške, Italije, Slovaške, Slovenije, Švice in Velike Britanije (prijavljeni avtorji iz Rusije niso prišli). Zaradi političnih razmer v tem delu sveta se je v primerjavi s preteklimi leti precej omejil mednarodni značaj konference, zato si je društvo MIDEM zastavilo kot enega pomembnih ciljev, da bi konferenca v bodoče spet dobila širše mednarodno obeležje.

Letošnja konferenca MIEL je bila razdeljena v šest sekcij: Integrirana vezja, Elementi na osnovi amorfnega silicija, Fizika polprevodniških elementov, Modeliranje in Tehnologija. Šesta sekcija, Vzgoja, je bila letos dodana zaradi naraščajočega pomena izobraževanja za boljše razumevanje mikroelektronike pri nespecialistih - uporabnikih. Na konferenci predstavljeni referati so tako podajali nove dosežke pri raziskavah mikroelektronskih in polprevodniških tehnologij, procesiranja, modeliranja procesov in komponent ter novega načrtovanja polprevodniških vezij in komponent. Dve sekciji sta odprla vabljena gosta s predavanji o BCD tehnologiji za pamet-

na močnostna vezja (C.Cini, ST, Milano) in tandemskih amorfnih silicijevih sončnih celicah (J.Furlan, FER, Ljubljana).

V okviru 29.Simpozija o sestavnih delih in materialih so tri vabljena predavanja in ostali referati pokazali trende in rezultate raziskav na področju elektronskih sestavnih delov in materialiov. Delo je bilo razdeljeno na štiri sekcije : Debele plasti, Karakterizacija, Tanke plasti in Materiali in komponente. Prvo sekcijo je odprl vabljeni gost E.Gramegna s predavanjem o keramičnih in poliimidnih materialih za multičip module. Ostali avtorji so poročali o raziskavah debeloplastnih materialov in tehnologij za različne uporabe, od senzorjev do perovskitnih katod za oksidne gorilne celice.

V sekciji karakterizacija je vabljeno predavanje M.Johnsona (IBM, Zürich) obravnavalo uporabo rasterske tunelske mikroskopije za karakterizacijo polprevodnikov.

Sekcija o materialih in elektronskih sestavnih delih pa se je pričela z vabljenim predavanjem A.Williamsa (University of Birmingham, UK) o magnetih na osnovi kovin prehoda in redkih zemelj ter njihovi tehnologiji in uporabi. Drugi referati v slednji sekciji so obravnavali npr. kondenzatorje na osnovi polimernih kompozitov, trde ferite, varistorje, nove uporabe LED....

Sekcija o tankih plasteh je med drugim obsegala referate o tankoplastnih piroelektričnih detektorjih, o novih metodah meritve električne upornosti in o sol-gel postopkih za pripravo tankih filmov.

Čeprav je bilo na letošnji konferenci MIEL-SD manjše število udeležencev kot prejšnja leta pa so bili stiki med udeleženci zelo živahni in koristni, kar se je pokazalo pri razpravah o referatih ter tudi pri organiziranih družabnih srečanjih.

21st INTERNATIONAL CONFERENCE ON MICROELECTRONICS, MIEL'93
29th SYSMPOSIUM ON DEVICES AND MATERIALS, SD'93
September 29 - October 1, 1993, Bled, Slovenia

MIEL-SD'93 has united two meetings with long traditions: the 21st International Conference on Microelectronics and the 29th Symposium on Devices and Materials. It was organized by MIDEM, the Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia, and was held at Bled, Slovenia, from September 29th to October 1st. This year, as well, these conferences have provided an opportunity for experts from all over the Europe to meet and discuss new developments in the fields covered by the Society. However, due to political events in this part of the world, the international character of the meeting has been lost to some extent. It is one of the major goals of the MIDEM Society to reestablish it in the future.

The MIEL conference was divided into six sessions: Integrated Circuits, Amorphous Silicon Devices, Device Physics, Modeling, and Technology. Due to increasing importance of education in the field of microelectronics, a new section on Education has been added this year. We hope that the addition of this section has encouraged and stimulated the understanding of microelectronics among non-specialists. The papers presented at the conference included recent results of research in semiconductor technology, processing, process and device modeling, and new designs of semiconductor devices and circuits.

Two sessions were opened by invited speakers. Dr.C.Cini from ST, Milano, has presented new trends in mixed bipolar-CMOS-DMOS smart power IC technology. Dr.J.Furlan from Faculty of Electrical and Computer Engineering, Ljubljana, talked about tandem amorphous silicon solar cells.

The introductory lectures and symposium papers of the 29th Symposium on Devices and Materials SD-93 presented the trends in the research on electronic materials and components. They were grouped in four sessions, i.e. Session on Thick Films, Session on Thin Films, Session on Materials and Components, and Session on Characterization. First session, Thick Films, started with invited paper on ceramic and polyimide materials for multichip modules presented by Mr.E.Gramegna from DuPont Electronics, Geneva. Other papers reported mainly on investigation of thick film materials for different applications ranging from sensors to perovskite cathodes for solid oxide fuel cells. The invited paper in "Characterization" session, given by Dr.M.Johnson, discussed the use of tunnel microscopy in the characterization of semiconductors. The sessions on "Thin Films" and "Materials and Components" were opened with introductory lecture on rare earth transition metal magnets given by Dr.A.Williams from University of Birmingham, UK. Other contributions dealt with capacitors, magnets and multilayer varistors in "Materials" session and mostly with sol-gel prepared thin layers in "Thin Films" session.

Although there were fewer participants than last year, this year's conference succeeded in innitiating fruitful technical discussions among participants during sessions, as well as new friendships during organized social events.

Podajamo seznam vseh udeležencev letošnje konference MIEL-SD'93 (This is a list of all MIEL-SD'93 Conference participants):

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ESSDERC 93
European Solid State Device Research Conference

The Conference was held from 13th to 16th of september in Grenoble, France. As each year a large number of participants took part and it was impossible to attend every article presented since there were parallel sessions.

Very interesting thing to notice was that many papers were presented as joint efforts between universities and industry.

Here are summaries of some of the most interesting papers covering mostly VLSI and mixed technologies.

1. D.Antoniadis, MIT, Physics and Technology for MOSFETs at 0.1 micron and Below, INVITED PAPER

2. W.H.Arnold, AMD, The New Limits of Optical Litography, INVITED PAPER

These two papers were invited and really show where the industry is heading. 0.5 micron is big ! Now it is possible to do 0.05 micron effective channel length and gate oxide of 35 Angstroms !

The first paper dealt with the effects of these small dimensions in the physics of the devices and the second with pattern definition and practical aspects such as cost. For example at present good step and repeat aligners cost about $ 2 million and for the future $ 10 million and this will not bring the 0.1 micron in production! This kind of numbers are a very convincing reason for a small companies to stay out of these kind of applications i.e. Memories and Micros.

3. K.Goser et al., University of Dortmund, Germany (other authors from Siemens - Munich), Mechanisms of Hot Carrier Degradation of Analog Device Parameters in N-MOSFETs

Devices from 1 - 5 micron gate length were checked. Stress in the drain region with thin gate oxide is not so important because it does not effect the output characteristics, but in the channel region such degradation is very important. There are two conditions possible: a) High drain voltage with low gate voltage and b) High drain voltage with high gate voltage.

In conclusion it is clear that high drain voltages can be a problem and to reduce the problem drain extensions would greatly help. Also thin gate oxide can be a problem for degradation; 200 Angstroms oxide was used and the devices were not bad.

A comment to this result is also that one could use thicker gate oxides and longer channel lengths where higher voltages are required (analog part of an IC) and thin gate oxide and short channel lengths where speed is required such as in the digital part of an IC.

4. J.A.Power et al, National and Analog Devices, Ireland, Generation of MOS Model Parameters Covering Statistical Process Variations

The paper is a result of long and tedious work with the aim to arrive to the set of worst/best case conditions for SPICE parameters to allow for better precision with circuit simulations.

5. K.Rodde, Matra MHF, France, CMOS Technology for System Integration: Constraints and Modular Process, INVITED PAPER

The author described the approach of process modules for system integration rather than technology integration. For example they integrate Digital circuits with DRAM or SRAM, also possible EPROMs and analog circuits by adding passive components. So in effect they just integrate standard MOS technologies only. Such a typical process has in production 18 masks.

6. D. Doyle et al, Analog Devices B. V., Ireland, ABCMOS3: A High Precision, High Speed, Modular BiCMOS Process for Analog/Digital Applications

In the paper authors claim modularity of the process. The paper outlined a method that offers high performance devices. The process is modular to make it possible to include or remove process modules depending on cost vs. performance requirements.

The main process is 12 masks, with double level metal. Bipolars can be added with five more masks. High precision poly-poly capacitors require two independent masks. They use burried layer and EPI approach.

7. B.C.Johnson, Motorola, The Future of High Density Packaging

This was very interesting paper. As performance of the devices and ICs are improved the overall performance is now limited by the package and stray effects of the package metal, bonds etc. Motorola is now starting to pay attention more and more in the package design and technology in the same way as in wafer processing. More and more the techniques used in wafer processing will also be used in package fabrication. The trend in packaging is from multi layer PC boards that are good for clock rates of up to 80 MHz to flip chip/photonics and wafer scale integration for system clock rates of over 1000 MHz.

8. H.G.Pomp et al, Philips Research labs, 0.25 micron CMOS with N_2O Nitrided Gate Oxides

The new idea now is that as the gate oxide gets very thin it can support very low voltages and is relatively unreliable. For this reason several companies are trying to use some nitride with the oxide. In the old days we used a sandwich of oxide and nitride under the gate but this introduced many problems, so the new idea is to introduce the nitride together during the oxidation. In this paper a two step oxidation is done first only with oxygen and then with N_2O and 1% nitride in the oxide is obtained. The final gate oxide is 75 Angstroms. The lifetime data for a change in threshold of 0.1 V was greater than 10 years for worst case condition and better than conventional gate oxides.

There were two other papers on this subject with different approaches for the oxidation steps. This is a good possibility for very thin gate oxides below 100 Angstroms.

Compiled from several sources

EPE - 5th European Conference on POWER ELECTRONICS AND APPLICATIONS

Od 13. do 16. septembra letos je bila v Brightonu, angleškem Portorožu, peta evropska konferenca o močnostni elektroniki in aplikacijah. Zaradi izredno visoke kotizacije (380 £) sem se udeležbi mislil odpovedati kljub sprejetemu članku z naslovom "Breakdown voltage of elliptic PN junctions". Premislil sem si v zadnjem trenutku, ker mi je evropska organizacija EPE plačala celotno kotizacijo, poleg tega pa mi je omogočila brezplačno udeležbo na enodnevnem seminarju o SPICE simulaciji v močnostni elektoniki (Using PSPICE in Power Electronics Simulation). To sem dosegel po daljšem dopisovanju z EPE in z veliko sreče, da sem to počenjal iz Toulousa, saj je bila finančna pomoč predvidena le za raiskovalce iz manj razvitih (lessfavoured) področij držav evrpske gospodarske skupnosti, kamor je spadala tudi regija Midi- Pyrénées.

Konferenca EPE (European Power Electronics) se je leta 1991 združila s konferenco MADEP (Materials Power Electronics) ter obdržala ime prve. Tako je nastala izredno velika konferenca, ki dejansko pokriva vsa področja močnostne elektronike: od fizike močnostnih elementov, izdelave in vgradnje v module, do kontrolnih enot, generatorjev in vseh mogočih gonilnikov (drives). In vse to tako na nivoju teoretičnih raziskav, simulacij in modeliranja, kakor tudi meritev in konkretnih aplikacij. Zanimivost konference je poseben način predstavitev prispevkov, ki večinoma potekajo kot razprave ob posterjih, čemur pravijo Dialogue Session. Avtor dobi na razpolago približno 2 m široko nišo, v katero postavi poster, na voljo pa ima še mizico in stole, kar mu omogoča miren razgovor in razpravo z vsakim zainteresiranim udeležencem. Take razprave in srečanja pa so navadno tudi najbolj plodovita. Širino in velikost konference najbolje ilustrira osem knjig referatov, od katerih je prva namenjena samo popolnemu seznanu člankov, povzetkom in štirim vabljenim predavanjem, v ostalih pa so referati. S svojim prispevkom sem sodeloval v sekciji

Materials and Devices, ki je v bistvu prenešena konferenca MADEP in zajema vse, kar se tiče močnostnih elementov v elektroniki. Največ referatov obravnava tematiko preklopov. Raziskujejo tako elemente, ki omogočajo čim hitrejše preklope ob čim manjših izgubah, kot tudi modele, ki bi zadovoljivo opisovali izhodne karakteristike močnostnih elementov za simulacijo vezij (SPICE simulacije). Dasiravno tiristorji in GTO ostajajo edina izbira za močnostne aplikacije za visoke napetosti in tokove pa v srednjem razredu močno napredujejo FET-krmiljeni elementi (MOSFET, IGBT, MCT). Izkazalo se je, da se preklopna moč teh elementov podvoji vsake dve do tri leta in je v primeru tiristorja in GTO že dosegla teoretično mejo, ki jo bo mogoče preseči le z uporabo novih materialov, kot na primer s silicijevim karbidom (SiC).

Glavne lastnosti in izboljšave močnostnih elementov v prihodnosti kaže tabela 1:

ELEMENTI	GLAVNE LASTNOSTI	IZBOLJŠAVE
diode	• specifične potrebe glede na aplikacije • aplikacije omejene z delovanjem diode	• optimizacija dinamičnih lastnosti (dI/dt)
GTO	• nizka cena na enoto toka	• zmanjšanje dinamičnih izgub • višje zaporne napetosti • serijsko povezovanje
IGBT	• FET krmiljeni element • max. površina 20-22 mm^2	• (modularno) paralelno povezovanje • zvišanje zaporne napetosti
Integrirani močnostni elementi	• specifične aplikacije • celotna aplikacija na čipu	• močno povečanje števila aplikacij

Poleg tega bodo v bodočnosti pomembni tudi "posebni elementi":

- optično krmiljeni tristorji za visoko napetostne aplikacije (10 kV)
- RC-GTO, ki bi združeval GTO in antiparalelno diodo na istem čipu, vendar z različno življensko dobo nosilcev
- MCT, ki trenutno velja za idealni element za preklope
- Smart-power elementi, ki poleg močnostnega vsebujejo dodatne elemente za kontrolo delovanja (senzor temperature, napetosti, toka, di/dt, dV/dt)
- elementi na silicijevem karbidu (SiC), ki omogočajo delovanje elementov pri višjih temperaturah, napetostih in tokovih ter nižjih izgubah.

Konferenca EPE se je tudi zaradi močne podpore industrije izkazala kot izredno cenjena in zanimiva za vse tiste, ki imajo opravka z močnostno elektroniko, posebno še z aplikacijami na tem področju.

Pri avtorju članka je interesentom na voljo ogled materiala s seminarja PSPICE, zbornika abstraktov in zbornika sekcije Materials and Devices.

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Peta evropska konferenca o uporabi metod za analizo površin in faznih mej (ECASIA 93)

V Cataniji na Siciliji je bila od 4.-8. oktobra 1993 že peta evropska konferenca z razmeroma dolgim imenom, navedenim v naslovu. Tisti, ki se ukvarjamo z metodami za preiskavo površin, že dlje časa vemo, da je to konferenca, ki pritegne vse najpomembnejše strokovnjake s tega področja v Evropi; zaradi njenega visokega znanstvenega in strokovnega nivoja pa so vedno v velikem številu prisotni tudi Američani in Japonci, ki imajo to področje tudi najbolj razvito. Konferenca je bila organizirana tako, da je okrog 500 udeležencev predstavljalo 435 prispevkov v obliki predavanj ali v poster sekcijah. Zastopana so bila naslednja področja (tu navedena po abecednem redu, če bi bila pisana v angleščini): adhezija, profilna analiza, interpretacija podatkov in kvantitativno vrednotenje, študij okolja, tehnike slikanja, metalurgija, mikroelektronika, optoelektronika, polimeri, radiacijski učinki, senzorji, superprevodniki, uporaba sinhrotrona, razvoj novih tehnik, tanke plasti in prevleke, tribologija in umetniška dela. Za posamezna področja sta organizacijski in znanstveni odbor konference organizirala osemnajst vabljenih predavanj.

Kot je že v navadi, je bilo v okviru konference organiziranih tudi več tečajev (delavnic), specializiranih za posamezne metode, kot so: AES, XPS, SIMS, TEM, STM/FM, RBS, ERD, NRA in druge. Vse najpomembnejše svetovne firme so pripravile razstavo opreme in najnovejših dosežkov, založba Wiley pa razstavo knjig in revij z zgoraj navedenih področij preiskav površin in faznih mej.

Primerjava s prejšnjima dvema konferencama ECASIA, ki sta bili pred štirimi leti v Antibesu, Francija in pred dvema letoma v Budimpešti, Madžarska, jasno pokaže hiter razvoj na tem področju (tako po naraščajočem številu udeležencev, kot po visokem strokovnem nivoju prispevkov). To ne preseneča, če vemo, da je prav uporaba metod za preiskavo površin nujen pogoj za raziskavo in razvoj novih večplastnih struktur in kompozitnih materialov za elektroniko, mikroelektroniko, metalurgijo, kemijo, strojništvo. V zadnjem času pa se te metode vse več uporabljajo tudi v medicini in drugje.

In kakšne so smeri razvoja? Več jih velja omeniti. Veliko pozornost je vzbudilo plenarno predavanje prof. G. Margaritondoja, ki je govoril o velikih možnostih uporabe sinhrotrona Elettra (v Trstu so prav v tednu ECASIA-93 napravili prve preizkuse s centralnim žarkom sinhrotrona). Zanimive so možnosti uporabe fotoelektronske holografije, elektronske spektroskopije z ultravisoko energijsko ločljivostjo in vrstične (rastrske) fotoemisijske spektroskopije. Povečal se je obseg preiskav z vrstično tunelsko mikroskopijo (STM), ki nudi, pred nekaj leti še neslutene, možnosti za strukturno in kemijsko karakterizacijo površin na atomarni ravni. Metoda SNMS se je razvila v tem pogledu, da za ionizacijo nevtralnih atomov in molekul uporablja laserski ali elektronski curek s čimer dosežejo občutljivost metode reda ppb. Nekateri avtorji so v svojih predavanjih pokazali tridimenzionalne slike, dobljene z ionskim mikroanalizatorjem. S 3D slikami, ki jih naredijo tako, da površino vzorca analizirajo v kombinaciji z ionskim jedkanjem, dobijo kvalitativni vpogled v porazdelitev elementov v teh dimenzijah vzorca. Več firm je prikazalo izboljšano računalniško pogramsko opremo za avtomatsko vodenje preiskav in zbiranje podatkov ter njihovo obdelavo.

Glede na udeležbo naših strokovnjakov na zadnjih konferencah ECASIA lahko sklenemo, da je to področje v Sloveniji v stagnaciji. Na letošnji konferenci ECASIA-93 je bil prisoten en udeleženec iz Slovenije in en Slovenec na delu v italijanski instituciji. Vzroka za tako stanje v Sloveniji sta predvsem dva: (1) raziskovalna oprema za tovrstne preiskave je draga, (2) strokovnjaki za to področje morajo praviloma imeti interdisciplinarno znanje, ki si ga lahko pridobijo šele po daljšem času in z delom na tujih institucijah z novejšo opremo. Slovenski raziskovalni inštituti in v prihodnosti oživljeno slovensko gospodarstvo bodo zato morali v bodoče naročati preiskave z zgoraj omenjenimi metodami v tujini. S tem bo seveda izgubljena avtonomnost pri preiskavah in pridobivanju novih patentov. Izgleda pa, da v tem prehodnem obdobju slovenska družba tovrstnih znanj in uslug ne potrebuje. Tudi avtor tega sestavka je daljši čas in tudi še v začetku leta 1993 prejemal osebni dohodek enak prejemku vratarja na istem institutu, kjer je zaposlen (IEVT).

Ni naključje, da je bila večina dosedanjih petih konferenc ECASIA organizirana v najbolj razvitih evropskih državah. TAko bo tudi naslednja konferenca ECASIA-95, za katero je organizator že pripravil prvo informacijo, od 9. do 13. oktobra 1995 v Montreux- ju v Švici.

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9. MEDNARODNA KONFERENCA O TANKIH PLASTEH, ICTF 9

Na Dunaju je bila od 6. do 10. septembra 1993 na Univerzi za ekonomijo 9. mednarodna konferenca o tankih plasteh (International Conference on Thin Films). Organiziralo jo je avstrijsko vakuumsko društvo (OEGV) v imenu Mednarodnega združenja za vakuumsko znanost, tehniko in uporabe (International Union for Vacuum Science, Technique and Applications, IUVSTA).

Strokovni del konference sta odprla J. Mannhart (IBM, Švica) ter K. Takayanagi (Tokio Institute od Technology, Materials Science and Engineering. Japonska) s plenarnima "Electric Field Effect in High-Tc Thin Films" ter "Surfactant Epitaxy: Nucleation and Growth Investigated by High Resolution TEM and STM".

V knjigi povzetkov je navedenih 293 prispevkov avtorjev iz 39 držav. Delo je bilo razdeljeno na 13 skupin. Porazdelitev ustnih prispevkov in posterjev po teh skupinah je prikazana v razpredelnici.

Če iz tabele ocenjujemo madnarodno dogajanje na področju tankih plasti, lahko rečemo, da je največ raziskav usmerjeno v osnovne lastnosti le-teh. Sledijo raziskave načinov nanosa, raziskave plasti za mikroelektroniko in magneto-optiko, analitske tehnike za površine in tanke plasti ter študije rasti. Med uporabniško usmerjenimi raziskavami je poleg že omenjenih raziskav plasti za mikroelektroniko in magneto-optiko največ zanimanja za trde in zaščitne prevleke, sledijo pa prevleke in večplastne strukture za rentgensko, UV, vidno in IR področje. Za polovico je manjše število

Delovne skupine na konferenci ICTF 9 Dunaj, 6. - 10. 9. 1993		število ustnih predstavitev	število posterjev	skupaj
T1	Osnovne raziskave rasti tankih plasti	21	10	31
T2	Osnovne lastnosti tankih plasti	21	27	48
T3	Spreminjanje tankih plasti z z ionskimi curki ter s plazmo	8	7	15
T4	Analiza površin in tankih plasti	13	18	31
T5	Postopki nanosa	13	21	34
T6	Visokotemperaturne superprevodne tanke plasti	7	6	13
T7	Organske in polimerne tanke plasti	6	8	14
T8	Sončne celice in snovi	8	5	13
T9	Trde in zaščitne prevleke	16	13	29
T10	Prevleke in večplastne strukture za X, UV, vidno ali IR uporabo	13	7	20
T11	Tankoplastna tipala	3	4	7
T12	Tanke plasti za mikroelektroniko in magneto-optične tanke plasti	16	16	32
PD	Zamujeni ustni prispevki	4		4
	SKUPAJ	149	142	291

raziskav na drugih, predvsem uporabnih področjih, kot so spreminjanje plasti z ionskimi snopi in plazmo, organske in polimerne plasti, visokotemperaturne superprevodne plasti ali sončne celice in snovi.

V okviru konference so organizatorji podelili nagrado "Max Auwaerter", imenovano po znanem raziskovalcu fizike in tehnologije tankih plasti ter ustanovitelju tovarne Balzers. Dobil jo je R. Wiesendanger za izjemno študijo površinskih defektov, domen in magnetnih struktur s pomočjo vrstične tunelske mikroskopije (Scanning Tunneling Microscopy, STM), opravljeno na univerzi v Baslu, Švica.

Podelitev nagrade skupaj z že omenjenim plenarnim predavanjem dokazuje, da je STM trenutno eno najbolj odmevnih področij raziskav. Drugo plenarno predavanje je bilo s področja visokotemperaturnih superprevodnikov, ki je v začetku devetdesetih let eksplodiralo, do danes pa se je že umirilo in se oblikovalo tako kot druga področja tankih plasti. Morda bo večji razmah temu področju dalo čisto sveže odkritje, da je meja superprevodnosti pod visokim tlakom lahko premaknjena nad 150 K.

Pri osnovnih raziskavah tankih plasti se s povečevanjem sposobnosti računalnikov opazno uveljavlja simulacija, ki je predstavljena na televizijski način. Vseeno pa so pogoji simulacije močno poenostavljeni, saj je to edini način, da je izračun končan v smiselnem času. Če na primer tridimenzionalno opazujemo dogajanje 500 atomov podlage med naparevanjem, naprševanjem, jedkanjem ali implantacijo, je število spremenljivk ogromno in moramo njihovo število optimazirati. G. Betz z Dunaja je prikazal simulacijo rasti tankih plasti ob različnih energijah vpadlih delcev. Na koncu je povedal, da simulacija ustreza rasti plasti s hitrostjo velikostnega reda m/s.

Med konferenco je v hali pred predavalnicama predstavljajo okrog 15 razstavljalcev svoje izdelke in tehnologije. Ta, ne razkošna razstava je potrjevala trditev organizatorjev, da so morali zaradi zmanjšanega števila sponzorjev kraj konference iz dunajskega centra premakniti na Univerzo za ekonomijo. Kljub visoki udeležnini (5800 ATS za navadne udeležence in 2850 ATS za študente) so bili natisnjeni le povzetki prispevkov, v revijah pa bo objavljeno le neznano majhno število prispevkov. Organizatorji so visoko udeležnino skušali upravičiti tudi z družabnimi dogodki in sicer s sijajno večerjo v slavnostni dvorani dunajske mestne hiše kot tudi s koncertom v dunajski koncertni hiši. Zdi se, da jim je uspelo.

Slovenija je bila na konferenci dostojno zastopana, saj imamo na spisku udeležencev 10 sodelujočih (za primerjavo: Češka 4, Madžarska 6, Francija 10, Italija 11, Švica 13, ZDA 19, Rusija 20, Avstrija 22, Japonska 29, Nemčija 46, itd.). Visoke številke udeležencev iz močnejših držav pričajo, da je konferenca uspela. Naslednja mednarodna konferenca o tankih plasteh bo v Salamanci v Španiji.

mag. Andrej Cvelbar
IJS
Jamova 39, Ljubljana

44. POSVETOVANJE O METALURGIJI IN KOVINSKIH GRADIVIH TER 1. POSVETOVANJE O MATERIALIH

V dneh 6. - 8. oktobra 1993 sta v hotelu Bernardin v Portorožu potekali v naslovu navedeni posvetovanji.

Pripravili in izvedli so ju:

- Inštitut za kovinske materiale in tehnologije
- Slovensko društov za materiale
- Slovensko kemijsko društvo: sekciji za keramiko in polimere
- Društvo za vakuumsko tehniko Slovenije

Finančno in moralno podporo je dalo Ministrstvo za znanost in tehnologijo Republike Slovenije.

Udeleženci so prišli z univerz, inštitutov in iz tujine ter iz industrije. Skupno jih je bilo nad 300 in so se od srede do petka zbirali na naslednjih sekcijah:

- metalurgija in kovinska gradiva
- sodobne tehnologije in materiali
- keramika, steklo, ognjevarna gradiva, kompoziti
- matematično modeliranje in računalniška simulacija procesov in tehnologij
- vakuumska tehnika
- tanke plasti
- polimerni materiali
- tribologija in propad gradiv
- tehnološki odpadki in varovanje narave
- sodobne toplotne obdelave.

Predstavljenih je bilo 176 prispevkov, od tega 94 govornih in 82 posterskih. Predavanja so potekala delno celo v dveh dvoranah vzporedno. Udeleženci so predavali o svojih dosežkih, zvečer pa so bili predstavljeni postri. Prva dva dneva so nekateri domači in tuji proizvajalci oz. njihovi zastopniki (RADEX Austrija, GIBA Avstrija, LEICA Avstrija, KLOCKNER Nemčija, ZWICK Nemčija, FISONS ZDA, SCAN Preddvor, TEAM-TRADE, Kamnik, IEVT Ljubljana) razstavljali opremo in pomožna sredstva za raziskave, razvoj in proizvodnjo. Predstavili so se še nemška založba SPRINGER, Slovensko društvo za materiale in Društvo za vakuumsko tehniko Slovenije.

Pomen skupne izvedbe dveh konferenc je v tem, da so prvič skupaj nastopili vsi strokovnjaki z različnih področij materialov in tehnologij (metalurgi, keramiki, kemiki, vakuumisti ...), ki so doslej delovali vsak zase. Praksa nam kaže, da novi časi v novem gospodarskem in političnem okolju zahtevajo nove drugačne načine sodelovanja; posamezno slovensko strokovno društvo ne uspe organizirati svojega nacionalnega kongresa, ker je pač premajhno, lahko pa se veže na podobne tuje konference in celo postane organizacijski servis za tuje strokovnjake, ali pa si najde svoj krog med strokovnjaki manjših narodov (npr. 3 dežele, skupnost Alpe-Jadran...) ali pa si poišče doma primerno tehnično "druščino" in goji domačo strokovnost malo manj ozko kot doslej. Izgleda, da je ta slednja varianta še najboj smiselna, vsaj portoroška izkušnja nam kaže tako. Udeležencev je bilo veliko in bili so si edini, da je bilo zanimivo in da bodo v prihodnje spet prišli.

Edino, kar - v smislu obstoja in razvoja prisotnih tehničnih strok - ni bilo povsem razumljivo, je vprašanje, zakaj glede na zanimivo vsebino ni prišlo več udeležencev iz proizvodnje; predvsem predstavniki s področja kovinskopredelovalne industrije, vakuumske in plinske tehnike ter izdelovalci polimerov in keramike so bili zelo redki. Zdi se, da ni zaupanja v domači znanstveno- razvojni potencial. Morda bi v prihodnje lahko poskrbeli še za kakšno novo obliko (so)delovanja, ki bi pritegnila aktiviste iz industrije.

Za vzpodbudo nam rabijo lahko mnogi lepi in pogumni nastopi mladih raziskovalcev, ki jih je bilo veselje poslušati. Želimo, da bi se znali postaviti za stroko, oglašati se v javnosti, dvigati nivo inženirskega stanu in pomagati organizirati delo na svojem strokovnem področju tako, da bo skupnosti kar največ koristilo.

Na posvetovanju so posebej ocenjevali prispevke novih raziskovalcev, ki pripravljajo magisterije in doktorate. Za priznanje so bili izbrani najboljši na naslednjih štirih področjih:

- **kovinski materiali** - Erika Bricelj: Vpliv deformacije na nukleacijo Nb (C,N), Železarna Jesenice
- **keramika** - Marko Rozman: Hidrotermalna sinteza feritov, Iskra Feriti
- **polimeri** - Miro Huskič: polimerizacija metilmetakrilata s PVC- ksantatnim mikroiniciatorjem
- **vakuumska tehnika** - Vinko Nemanič: Vakuumska ploskovna izolacija-kovinska alternativa ekološko oporečnim izolacijskim penam, IEVT

Predsednik posvetovanja prof F. Vodopivec jim je zagotovil izplačilo manjše denarne nagrade.

Zadnji dan dopoldne je v pristnosti direktorja Slovenskih železarn dr. A. Ocvirka in predstavnikov vlade potekala še javna razprava o stanju in obstoju naše jeklarske industrije, ki pa ni bila toliko uspešna, kot so si organizatorji želeli.

Skrbni organizatorji z Inštitutom za kovinske materiale in tehnologije na čelu so udeležencem ob prihodu pripravili knjigo abstraktov in bodo vse pravočasno oddane prispevke tudi natisnili v posebni številki revije "Kovine, zlitine, tehnologije", vendar le tistim, ki so poravnali kotizacijo.

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PREDSTAVLJAMO PODJETJE Z NASLOVNICE

The CMP Service

Bernard Courtois

This paper is about the CMP Service (Circuits Multi-Projects). CMP aims at providing Universities, Research Laboratories and Industries with the possibility to have their integrated circuits projects fabricated. The Service has started in 1981. Presently, customers are serviced for a CMOS double layer metal technology (DLM), 1.5 μm, 1.2 μm, and 1.0 μm, a CMOS double layer polysilicon / double layer metal (DLP/DLM), 1.2 μm, a bipolar technology, a digital GaAs .8 μm, a BiCMOS 1.2 μm and for Multi-Chip Modules fabrication. There are almost 20 runs per year. The paper details the Service, including some basic principles, some history, the descriptive formats, etc... A few examples of circuits fabricated for Educational and Research purposes are also briefly presented.

1. Introduction

A large number of complex technological operations are required for integrated circuit fabrication, but circuits are cheap, due to the fact that most of those operations are repetitive. Each processed wafer of silicon is cut into hundreds of dice. For some of the slowest and costliest operations, "batches" of hundreds of wafers are processed together. That means that tens of thousands of circuits are fabricated simultaneously. By this high number, industry can tolerate yields sometimes as low as 10 %. For non collective operations, such as test and packaging, operations are highly automated, using mass production techniques. All these very expensive techniques, aimed primarily at mass production, seem out of reach for research and educational centers for integrated circuit design. However the design of a circuit by students must be pursued to its conclusions, which means fabrication, but a student will only require a few chips and mass production is not necessary.

The basic idea of a multiproject chip or wafer is to collectively process circuits that are different and dissimilar. High fabrication costs can then be shared. To do so, a great number of elementary circuits are put side by side, to be reproduced on the wafer. The fabrication yield must excellent. Indeed circuits cannot be tested before being sent back to the designer.

CMP aims at providing Universities and Research Laboratories the possibility to have their integrated circuits fabricated. CMP has been started in 1981. Since 1981, CMP has been servicing 60 French Universities and Research Centers. 30 Centers from 20 foreign Countries have also been served. CMP has established official cooperation agreements with several of those Centers or Countries. CMP has experience from using 10 commercial semiconductor houses for mask making and processing, on NMOS, CMOS and bipolar technologies. More than 1000 circuits have been manufactured. Currently, CMP offers 22 runs a year. Complexity of the runs has been up to 73 different designs on a run (650 mm^2 of prototyping) and up to chip complexity of 100 000 transistors. The Service provides a minimum of 20 copies of the circuit (chips are untested) including 5 packaged samples (more on request).

2. A bit of history

The history of CMP cannot be dissociated from LUCIE and from the leadership of F. ANCEAU. In the late 70s, Universities had no CAD tools available to design integrated circuits. The Computer Architecture Group thus designed a graphical editor LUCIE, made available in 1979 - 1980. LUCIE has been the way to design circuits, and consequently the input to maskers to fabricate the first circuits. Next, LUCIE has been complemented by text editors, cell assemblers, etc.. and widely distributed to Universities (20 French Universities and 15 Foreign Universities on 13 different hardware platforms) and other inputs have been defined. But it should be stressed that this rudimentary CAD tool has been the way to get started in VLSI design and the way to first prototypes. The output format of LUCIE was used as exchange format by several research laboratories to connect their home- made CAD tools to the CMP Service.

Since many specific procedures, interfaces, etc... were necessary to go from the design data to prototypes, many people contributed, voluntarily, to this achievement: engineers and researchers from CNET / France Telecom, UCL in Louvain la Neuve, LAAS, LETI, Matra Harris Semiconductors, NANOMASK,... .

The first support came from a group named GCIS, a National entity grouping CNRS (The National Council for Scientific Research), CNET / France Telecom and LETI of the French Nuclear Research Center to fabricate the first circuits. Next, both CNRS and the Ministry for Education provided each one Engineer, and CMP was recognized as a National Center for chip fabrication in 1984. In 1986 the National Committee for Microelectronics Education (CNFM) decided to buy and to distribute widely industrial CAD software, like SOLO 1000 and SOLO 2000 from ES2. This decision was the start of a large improvement of designs for Education. Today,

CMP is supported by the Ministry for Education through CNFM, by the Ministry for Research through CNRS (Engineering Sciences) and the Ministry for Industry which supports CNFM. It is hosted by the TIMA Laboratory (research Laboratory on microelectronics).

3. Development

Several periods may be distinguished.

1981-1982: launching CMP

1981: The first chip, named MPC81 and containing three circuits was processed in June 1981 in cooperation with UCL (Université Catholique de Louvain), at Louvain La Neuve in Belgium. A second one , containing 5 circuits, was processed later. Masks were made with a mechanical photocomposer reading paper tapes !

1982: In March 1982, MPC82 had 27 projects coming from 11 Laboratories or Universities. The masks were made this time with an Electron Beam Generator, by Micromask, California, USA. Fabrication was made at the CNET, with a NS technology. Circuits were back to the designers in October 1982.

1983-1984: development of NMOS, launching CMOS

1983: In April 1983, the MPC 83 concentrated 48 circuits (25 from students and 23 from researchers). Mask making was made by Nanomask (France) and processing by CNET with the new NMOS L3 technology they had just developed. Circuits were distributed in November 1983.

1984: Three MPC projects have been processed in 1984: 2 projects in NMOS and one in CMOS. The two NMOS 1984 projects have been realized at CNET using the same technology. The two NMOS projects have collected 70 circuits on the whole (24 Educational circuits and 46 Research circuits). Each of them lasted a little more than 4 months. As for the preceeding project, half of the wafer was used by CNET circuits and half by MPC circuits.

The 84 CMOS project has been the first project processed with a CMOS technology, available from MATRA HARRIS SEMICONDUCTORS. 9 circuits on the whole have participated to this project ; 6 research circuits and 3 education circuits.

1985-1986: development of CMOS

1985: In 1985, two MPC projects have been launched; one in NMOS technology, and the other in CMOS technology.

The 85-NMOS MPC project has been realized, for the first time, at Thomson EFCIS company. This project was realised in 14 weeks, and 40 circuits were collected (half Research, half Education).

The 85 CMOS MPC project was realized at Matra Harris Semi-conducteurs, with a new technology: Saji5, gate of 2 microns , 2 metal levels. This project was the first project realized in CMOS 2 microns 2 metal levels technology. 32 circuits have been designed (14 research circuits and 18 education circuits). One of the objectives of the project was to offer the users an advanced technology. Two sets of design rules have been elaborated: one set of "tiny" rules, very close to the technology rules, and one set of "large" rules which allowed to accept the 1984 CMOS circuits with a minimum of transformations. The delay of this project has been about 9 months.

1986: two MPC projects were realized in 1986, similarly to the 1985 projects: one in NMOS technology at Thomson EFCIS and the second in CMOS at MHS. 52 circuits were part of the NMOS project, launched at the end of February. The turnaround time was 17 weeks and the circuits could have been tested at the end of June 1986.

73 circuits were part of the CMOS project, grouped in 26 macro-circuits of 7x7 mm. The turn around time was 5,5 months. The importance of the participation showed the necessity to increase the frequency of CMOS projects.

1987-1989: abandon NMOS, increase the frequency of CMOS runs

1987: four MPC projects were launched, regrouping an amount of 87 circuits. The first run was realized at Matra-Harris-Semi-Conducteurs, the other ones at European Silicon Structure. The turn around time varied from 4 to 5 months. Because of direct writing, from the C87-3 MPC run, a Design Rule Checker was systematically run on each circuit by the CMP before manufacturing. A new set of MPC design rules was set up in November 1986 and used for the ES2 design rules.

1988: five MPC projects were launched, regrouping an amount of 95 circuits and a total area of 879 mm^2. The five runs were realized at European Silicon Structure. The turn around time varied from 3,5 to 4,5 months from the data tape to the packaged parts.

1989: five runs have been organized, using the CMOS DLM 2 µm thechnology.

1990: more CMOS runs, introduction of bipolar

1990: In 1990, 9 runs have been organized: 5 in 2 µm CMOS DLM, 3 in 1.5 µm CMOS DLM, and the Service has opened a bipolar process facility. The total prototyped surface has been the double of what it was in 1989.

1991-1993: strong expansion and diversification

1991: a service using the 2 μm CMOS DLP/DLM from AMS has been opened. This service has been open to Universities, Research Laboratories, and Industries. A total of 14 runs has been realized. Also, the 1.2 μm CMOS DLM from ES2 has been opened and the production of the 2 μm from ES2 has been stopped. A total of 1.713 mm^2 have been prototyped, compared to 1.259 in 1990, and to 617 in 1989 (despite the use of thinner technologies).

1992: a total of 22 runs has been organized. The 1.2 μm CMOS DLP/DLM from AMS has been introduced, and the .8 μm GaAs from TCS (VITESSE process) is launched. CMP also introduced a Multi-Chip Modules service, using the DASSAULT ELECTRONIQUE capabilities.

1993: a BiCMOS 1.2 μm process is started. This process is fully compatible with the CMOS DLP/DLM 1.2 μm process.

4. Descriptive formats

Designers may use any CAD system, provided they submit the description of the circuit in a format accepted by CMP. The usual format is GDS2. CIF format produced by some design systems is also possible. EDIF is also agreed. Other formats have to be agreed prior to submission.

5. Design rules and CAD software

In the past, CMP used to allow 2 sets of design rules: a set of portable design rules and the foundries design rules. Today only foundries design rules are considered by the designers. They are those of the ECPD15, ECPD12 and ECPD10 CMOS from ES2, the CAE and BAB from AMS, the H-GaAs II from TCS and the Polyuse design data from TCS. CMP also distributes libraries and design kits when available, and even defines some design kits in cooperation with some CAD vendors and manufacturers: AMS and TCS design kits to be used under CADENCE, or COMPASS, ... As a focal point, CMP also distributes information on configuration files, converters, etc.. designed by some University, hence another University interested in that faculty may get it.

CMP has also available the back-end procedures to take directly designs issued from some CAD software like SOLO 1400 from ES2. Usually, the turn around time is 12 weeks from submission to delivery of the packaged circuits. The submission of a circuit implies that a testing report is sent back to CMP for publishing in the Annual Report.

6. Testing and packaging

To help the designers to test their circuits, a small series of low-cost probe equipment had been initially built using parts from several sources. Next CNFM decided to buy centrally ATE equipment in 1988.

Recommendations in view of packaging are available. Currently, the packages supported are as follows:

DIL	16	28	40	48	pins
CLCC		68	84		pins
PGA	84	100	120	144	pins

7. CMP service costs

Circuit production is billed according to the technology and according to the function and origin of the circuits submitted.

Some examples are:

- 700 FF/mm^2 for the 1.5 μm DLM CMOS from ES2
- 900 FF/mm^2 for the 1.2 μm DLM CMOS from ES2
- 1000 FF/mm^2 for the 1.0 μm DLM CMOS from ES2
- 1600 FF/mm^2 for the 1.2 μm DLM/DLP CMOS from AMS
- 2300 FF/mm^2 for the 1.2 μm BiCMOS from AMS
- 2700 FF/mm^2 for the .8 μm digital GaAs

8. Operations since 1981

CMP has served many Institutions since 1981, for a number of technologies. Table I depicts the Institutions, and Table II depicts the runs which have been fabricated.

9. A few examples

Below are briefly presented two circuits designed for Education and Research purposes.

The circuit detailed in picture 1 is a circuit designed for Educational purpose. This circuit is a distancemeter with a precision of 1 cm between 0 and 10 meters. The circuit has been designed by 2 students under guidance of G. BOUVIER, Professor at ENSERG. It has been fabricated by CMP on the 1.5 μm CMOS process from ES2.

The circuit detailed in picture 2 is a circuit designed for Research purpose. The circuit is a RAM designed with BIST (Built-in Self Test) capabilities. It implements the marching algorithm proposed by MARINESCU with low area overhead. The circuit has been designed by O. KEBICHI under guidance of M. NICOLAIDIS from TIMA

Laboratory. It has been fabricated by CMP on the 1.2 µm CMOS process from ES2.

10. Conclusions

It has been recognized that students and researchers must be provided with the possibility to have their circuits fabricated. From its inception in 1981, CMP has been successful and it expanded very much, particularly during the last years. The success is partly due to the basic principles which have been governing the choices of the Service: used **industrial** and **advanced** process lines. Indeed, to select University process lines to fabricate the circuits does not allow for good regularity and high yield (necessary because the circuits are not tested before to be returned to the designers). Advanced processes are more and more necessary because of the need of very skilled designers and because CAD industrial software is more and more available to Universities instead of University CAD software. Since new versions of CAD software come with libraries on advanced processes, there is no choice but to use advanced processes. For the years to come, it is expected that the cooperation between Education - Research - Industry will be facilitated by the fact that chip fabrication is not restricted to Educational or Research circuits.

11. Bibliography

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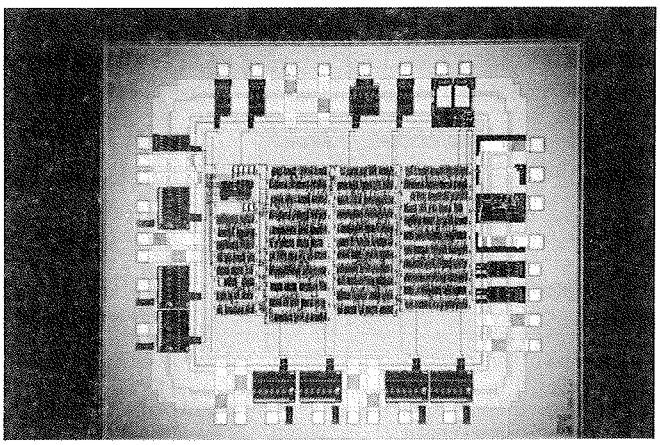
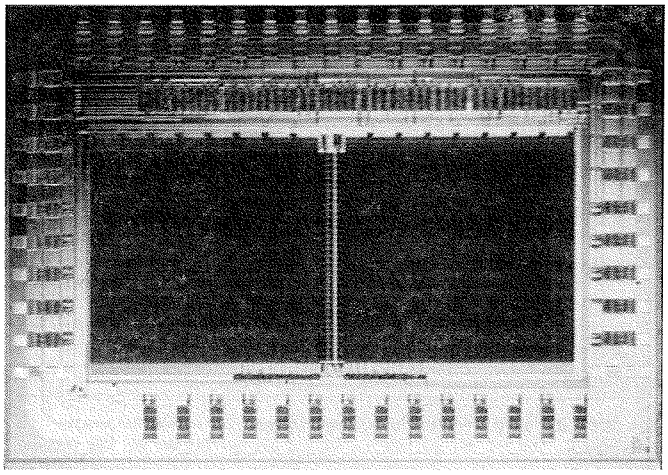


Picture 1: Educational circuit (distancemeter)



Picture 2: Research circuit (BISTed RAM)

FRANCE	TOWN
Etablissement Technique Central de l'Armement (ETCA)	Arcueil
Ecole Nationale Supérieure de Micro Mécanique	Besançon
Ecole Nationale d'Ingénieurs de Brest (ENIB)	Brest
Ecole Nationale des Télécommunications de Bretagne	Brest
Ecole Nationale Supérieure d'Electronique et ses Applications	Cergy Pontoise
Ecole Supérieure d'Electricité	Gif sur Yvette
Ecole Nat. Sup. d'Electron. et de Radio Electricité	Grenoble
DEA de Microélectronique	Grenoble
Ecole Nat. Sup. d'Ingén. Electriciens	Grenoble
Institut Universitaire de Technologie	Grenoble
Conception de Systèmes Intégrés	Grenoble
Techniques de l'Informatique, des Math. de la Microélec. et de la Microscopie Quantitative	Grenoble
Labo. Traitement d'Images et de Rec. des Formes	Grenoble
Unité de Génie Matériel (Laboratoire Génie Informatique)	Grenoble
Institut Supérieur d'Electronique du Nord	Lille
Ecole Centrale de Lyon	Ecully
Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier	Montpellier
Institut de Rech. Enseign. Sup. Techn. et Electron.	Nantes
Ecole Sup. d'Ing. en Electrotech. et Electronique	Noisy le Grand
Institut d'Electronique Fondamentale	Orsay
Laboratoire de Recherche en Informatique	Orsay
Laboratoire de l'Accélérateur Linéaire	Orsay
Ecole Polytechnique	Palaiseau

Centre de Microélectronique de Paris Ile de France (CEMIP)	Paris
Labo. de Méthodes et Archi. de Syst. Informatiques	Paris
Institut de Programmation	Paris
Ecole Nat. Sup. des Télécommunications	Paris
Ecole Normale Supérieure	Paris
Institut Supérieur d'Electronique de Paris	Paris
Laboratoire de Physique Nucléaire et de Hautes Energies	Paris
Université Pierre & Marie Curie, Dept d'Electronique	Paris
Institut Nat. de Recherche en Inform. et Automat.	Roquencourt
Ecole Supérieure d'Electricité	Cesson Sévigné
Institut de Rech. en Informat. et Syst. Alnatoires	Rennes
Université Louis Pasteur	Strasbourg
Lab. d'Electronique et de Physiques des Systèmes Instrumentaux (LEPSI)	Strasbourg
Ecole Nationale Supérieure d'Electronique et de Radioélectricité de Bordeaux (ENSERB)	Talence
Laboratoire de Microélectronique (IXL)	Talence
Ec. Nat. Sup. d'Electronique d'Electrotechnique d'Infor. et d'Hydraulique de Toulouse (ENSEEIHT)	Toulouse
Laboratoires d'Autom. et d'Analyse des Systomes (LAAS)	Toulouse
Institut National Sciences Appliquées (INSA)	Toulouse
Institut Universitaire de Technologie, Dept GEII	Toulouse
Ecole Nat. Sup. d'Electricite et de Mécanique	Vandoeuvre les Nancy
Université des Sciences et Techniques de Lille	Villeneuve d'Ascq
Laboratoire d'Informatique Fondamentale de Lille	Villeneuve d'Ascq
Institut de Physique Nucléaire	Villeurbanne
Institut National Sciences Appliquées	Villeurbanne

FOREIGN COUNTRIES	TOWN	COUNTRY
Commissariat aux Energies Nouvelles	Algiers	ALGERIA
Universidad Federal do Rio Grande do Sul	Porto Alegre	BRAZIL
Laboratorio de Sistemas Integraveis, EPUSP	Sao Paulo	BRAZIL
University of Science & Tech. of China	Beijing	CHINA
Universidad del Valle	Cali	COLOMBIA
Instit. für Matem. Maschin.& Datenverarbei.	Erlangen	GERMANY
National Technical University of Athens	Athens	GREECE
Technical University of Budapest	Budapest	HUNGARY
Laboratorium Elecktronika	Bandung	INDONESIA
Technion Israel Institute of Technology	Haïfa	ISRAEL
Politecnico di Torino	Torino	ITALY
Universita di Pisa	Pisa	ITALY
Universita di Roma	Roma	ITALY
Institute of Electron Technology	Warsaw	POLAND
Warsaw Univ. of Techn. (Inst. Mikroelek. Optoelek.)	Warsaw	POLAND
Inst. de Engenharia de Sistemas e Computad.	Lisbon	PORTUGAL
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Universidad Politecnica de Catalona	Barcelona	SPAIN
Universidad Politecnica de Madrid	Madrid	SPAIN
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Universidad de Cantabria	Santander	SPAIN
Centre Suisse d'Electronique et de Microtechnique S.A	Neuchatel	SWITZERLAND
Ecole Polytechnique Fédérale	Lausanne	SWITZERLAND
Eidgenoessische Technische Hochschule	Zurich	SWITZERLAND
Ecole Nat. des Sciences de l'Informatique	Tunis	TUNISIA
Bournemouth Polytechnic	Bournemouth	UNITED KINGDOM
University of London VLSI Consortium	London	UNITED KINGDOM
University College London	London	UNITED KINGDOM

Table I - Institutions having submitted circuit(s) to CMP
France: 47
Foreign Countries: 30
Total: 78

Date	Manufact	Techno	Gate mic	λ mic	Instit	Cir Res	Cir Edu	Cir total	Tot area
81	UCL	UCL	-	4	1	7	1	8	-
82	CNET	NMOS/NC	4.5	3	10	15	12	27	39.106 λ^2
83	CNET	NMOS/L3	3.15	2.25	18	25	23	48	62.106 λ^2
84Feb	CNET	NMOS/L3	3.15	2.25	15	15	28	43	72.106 λ^2
84Mar	MHS	CMOS/Saj4	3.5	2.25	8	3	6	9	18.106 λ^2
84Oct	CNET	NMOS/L3	3.15	2.25	12	9	18	27	48.106 λ^2
85Mar	THOMS	NMOS/hm1	3.5	2.5	10	19	21	40	50.106 λ^2
85June	MHS	CMOS/Saj5	2	1 & 2	11	18	14	32	203.106 λ^2
86Feb	THOMS	NMOS/hm1	3.5	2.5	13	37	16	53	122.106 λ^2
86June	MHS	CMOS/Saj5	2	1 & 2	22	34	39	73	657.106 λ^2
87Feb	MHS	CMOS/Saj5	2	1&1.5 & 2	16	22	18	40	192.106 λ^2
87June	ES2	ECDM20	2	1	10	10	2	12	65 mm^2
87Oct	ES2	ECDM20	2	1	8	10	5	15	157 mm^2
87Dec	ES2	ECDM20	2	1	8	10	9	19	224 mm^2
88Feb	ES2	ECDM20	2	1	9	13	17	30	222 mm^2
88Apr	ES2	ECDM20	2	1	8	7	3	10	78 mm^2
88June	ES2	ECDM20	2	1	7	22	1	23	249 mm^2
88Nov	ES2	ECDM20	2	1	13	32	1	33	330 mm^2
89Feb	ES2	ECDM20	2	1	12	22	14	36	190 mm^2
89Apr	ES2	ECDM20	2	1	6	8	4	12	108 mm^2
89June	ES2	ECDM20	2	1	8	14	1	15	119 mm^2
89Oct	ES2	ECDM20	2	1	7	13	4	17	126 mm^2
89Dec	ES2	ECDM20	2	1	8	6	6	12	74 mm^2
90Jan	ES2	ECDM20	2	1	2	0	33	33	296 mm^2
90Feb	ES2	ECDM20	2	1	10	7	31	38	276 mm^2
90Mar	ES2	ECPD15-1	1.5	-	3	3	0	3	24 mm^2
90May	ES2	ECDM20	2	1	10	10	11	21	220 mm^2
90July	ES2	ECDM20	2	1	6	7	1	8	124 mm^2
90Sept	ES2	ECDM20	2	1	9	6	6	12	145 mm^2
90Sept	ES2	ECPD15	1.5	-	4	3	1	4	58 mm^2
90Nov	TCMS	Polyuse L12	-	-	1	0	4	4	51 mm^2
90Dec	ES2	ECPD15	1.5	-	3	0	6	6	59 mm^2
91Feb	ES2	ECDM20	2	1	10	15	27	42	357 mm^2
91Feb	ES2	ECPD15	1.5	-	6	5	7	12	141 mm^2
91Apr	TCMS	Polyuse L12	-	-	4	0	8	8	102 mm^2
91Apr	ES2	ECPD15	1.5	-	2	0	18	18	268 mm^2
91Apr	AMS	CBE	2	-	1	0	2	2	9 mm^2
91May	ES2	ECPD12	1.2	-	6	3	5	8	160 mm^2
91June	ES2	ECPD15	1.5	-	6	2	5	7	141 mm^2
91July	ES2	ECDM20	2	1	10	9	8	17	240 mm^2
91July	TCMS	Polyuse L12	-	-	1	0	1	1	13 mm^2
91Sept	AMS	CBE	2	-	1	0	1	1	3 mm^2
91Oct	ES2	ECPD12	1.2	-	2	5	0	5	70 mm^2
91Nov	ES2	ECPD15	1.5	-	4	2	5	7	104 mm^2
91Nov	AMS	CBE	2	-	1	1	0	1	11 mm^2
91Dec	ES2	ECPD12	1.2	-	4	7	1	8	76 mm^2
92Jan	ES2	ECPD15	1.5	-	3	2	2	4	124 mm^2
92Jan	AMS	CBE	2	-	3	1	3	4	26 mm^2
92Feb	ES2	ECPD12	1.2	-	7	3	15	18	266 mm^2
92Feb	ES2	ECPD15	1.5	-	6	2	13	15	168 mm^2

cont'd

Date	Manufact	Techno	Gate mic	λ mic	Instit	Cir Res	Cir Edu	Cir Indus	Cir total	Tot area
92Feb	TCMS	Polyuse L12	-	-	2	0	2		2	26 mm^2
92Feb	AMS	CAE	1.2	-	1	0	1		1	12 mm^2
92Mar	TCMS	Polyuse L12	-	-	2	0	3		3	38 mm^2
92Mar	AMS	CBE	2	-	1	0	1	0	1	28 mm^2
92Apr	ES2	ECPD12	1.2	-	4	0	4	0	4	155 mm^2
92Apr	AMS	CBE	2	-	1	1	0	0	1	7 mm^2
92May	ES2	ECPD15	1.5	-	5	4	6	0	10	156 mm^2
92May	AMS	CAE	1.2	-	2	1	4	0	5	15 mm^2
92Jun	ES2	ECPD12	1.2	-	4	0	5	0	5	261 mm^2
92Jul	ES2	ECPD15	1.5	-	7	1	10	0	11	138 mm^2
92Jul	AMS	CAE	1.2	-	2	1	2	0	3	11 mm^2
92Jul	AMS	CBE	2	-	2	0	2	0	2	41 mm^2
92Aug	TCMS	Polyuse L12	-	-	2	0	2	0	2	26 mm^2
92Sept	ES2	ECPD12	1.2	-	4	1	4	0	5	164 mm^2
92Oct	ES2	ECPD15	1.5	-	6	2	5	0	7	114 mm^2
92Oct	AMS	CAE	1.2	-	5	5	4	0	9	40 mm^2
92Nov	ES2	ECPD12	1.2	-	1	2	0	0	2	21 mm^2
92Nov	AMS	CBE	2	-	1	1	0	0	1	6 mm^2
93Jan	ES2	ECPD12	1.2	-	5	1	3	1	5	134 mm^2
93Feb	ES2	ECPD15	1.5	-	7	0	14	0	14	111 mm^2
93Feb	ES2	ECPD12	1.2	-	9	1	20	0	21	459 mm^2
93Feb	AMS	CAE	1.2	-	3	2	4	0	6	41 mm^2
93Feb	TCS	Polyuse L12	-	-	2	0	2	0	2	26 mm^2
93Mar	AMS	CBE	2	-	1	0	1	0	1	4 mm^2
93Mar	TCS	HGaAsII	0.8	-	6	6	0	2	8	94 mm^2
93Apr	TCS	Polyuse L12	-	-	1	0	3	0	3	38 mm^2
93Apr	TCS	Polyuse L12	1.2	-	2	2	2	0	4	53 mm^2
93Apr	AMS	CAE	1.2	-	2	2	2	0	4	43 mm^2
93May	ES2	ECPD12	1.2	-	6	4	3	1	8	71 mm^2
93Jun	ES2	ECPD15	1.5	-	5	1	11	0	12	157 mm^2
93Jun	AMS	CAE	1.2	-	4	2	5	0	7	50 mm^2
93Jun	TCS	HGaAsII	0.8	-	10	10	0	8	18	124 mm^2
93Jul	ES2	ECPD12	1.2	-	10	2	10	1	13	133 mm^2
93Jul	ES2	ECPD10	1.0	-	3	2	1	1	4	102 mm^2
93Aug	AMS	CAE	1.2	-	2	0	0	2	2	10 mm^2
93Aug	AMS	BAB/CAE	1.2	-	7	9	2	2	13	70 mm^2
TOTAL 86 Projects										
1160 circuits: 527 Research circuits 615 Education circuits 18 Industrial circuits										

Table II - History of CMP projects

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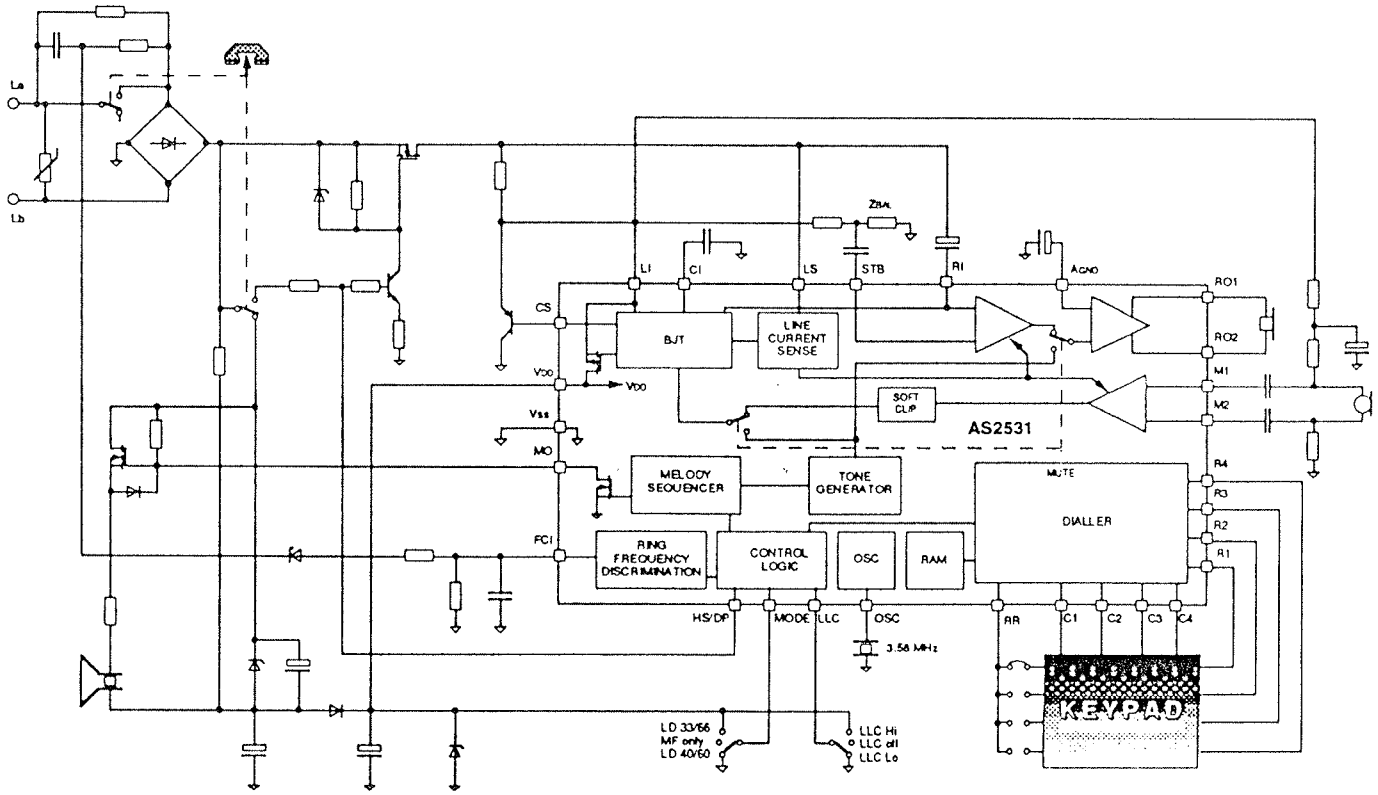
VESTI

NOVE KOMPONENTE

SINGLE CHIP TELEPHONE WITH 14 NUMBER REPEPERTORY DIALLER

AMS (Austria Mikro Systeme International) announces the imediate availability of the first CMOS single chip telephone in the world with a new speech transmission circuit with repertory dialler, melody generator and ringer all on a single chip: the AS2531, an integrated circuit that performs all the functions required of a medium range high performance electronic telephone.The advantage of this new ASIC is that it drastically reduces the external component count to about 40 as copared to about more than 200 in the average telephone set!The device incorporates LD/MF repertory dialling functions, melody generation, ring frequency discrimination and an advanced speech circuit. Additionally to the basic functions, the speech circuit includes soft clipping. The AS2531 also incorporaters a volume control for the earpiece.During on-hook the repertory number store is maintained with less than 0.1 μA-the device has an operating range from 13 mA to 100 mA but can operate down to as low as 5 mA with somewhat reduced performance. An on chip power on reset assures corect start-up. Furthemore, no battery is required. The device features a 31 digit last number redial and a 14 number repertory store.Furtheore, a unique double Wheatstone Bridge makes the adjustement of the return loss (AC impedance) and side tone riple since these two parameters are fully independent of each other.Since the RFI sensitivity has been minimized by the consequent use of CMOS technology no expensive coils are needed. The AS2531 allows an easy adaptation to a wide variety of different,international PTT requirements without changing the PCB of telephone. This is provided by built-in versaltillity and preprogramed options.The AS2531 is now available in 28 pin DIP, PLCC or SOIC packages.



Complete Single Chip Telephone

Fig. 1: Complete Single Chip Telephone

Customer Conformity

As a customer oriented ASIC company it felt natural for the telecom design team at AMS to be in compliance with customer wishes during the design phase of the AS2531.

High Degree of Integration

The AS2531 combines two desirable features which are normally contrary each other, high integration and flexibillity. The high integration is the reasonable consequence for complying with the deand for low overall costs.The flexibillity is necessary to allow the telephone manufacturer to utilize his own design philosophy, to put his own label on the telephone and to adapt it to different and ever changing market demands.

System on Chip

The consequent combination of high integration and versatillity allows the telephone manufacturer to cut design tie and effort. Designing with AS 2531 means:

- Short development time
- Easy and uncomplicated design effort
- And easily changeable to new PTT or market demands

Universal Operating Procedures

The AS 2531 is bilingual communication at your finger tips- worldwide. The operating procedures of the AS2531 are made out of consideration for system independency and constistency, -for improved user comfort. It literally works in any language.

Speech on AS2531-Sounds Great

The speech transmission quality is an often neglected feature. On the AS2531 it is the most vital feature. The AS2531 incorporates soft clipping, both in the transmit and in the receive path. The fast attack tie and slower decay time prevents unpleasant distortion via the side tone when the line conditions are bad.

The very fast attack time of the soft clipping is provided on the AS2531 allowing it to cope with the high dynamics of speech where the amplitude changes rapidly over a wide range.

The overdrive range of the soft clipping is high for handling very high signals from the microphone. This is especially important when using electret michrophones, since they do not have the acoustical limitation as the dynamic transducers have.

Most speech circuits have a hard clipping limitation on the receiver not to avoid acoustic shock only but also to avoid harsh distortion.

Low noise

The noise level of the AS2531 is well below the hardest PTT requirement, i.e. less than -75 dBmp on the line terminals as well as on the receive outputs.

Line Loss Compensation

Some PTTs require that the line loss (caused by long lines) should be compensated by increasing the gain of both the transmit and the receive path with decreasing line current. This line regulation is a pin option on the AS2531.

Volume Control

The VOL key provides a 4 dB boost of the receive gain, which is convenient for long lines with poor reception signals and for hard hearing people. The AS2531 also incorporates +/- keys as an alternative to the VOL key allowing the user to set the volume of the receiver from -4 dB to +6 dB in 2 dB steps. The volume setting will be reset to normal by next off-hook.

(Source: AMS pressinformation, AS23, June 1993.)

ULTRA FAST SILICON TRANSISTOR

A silicon transistor that can switch on/off at room temperature was recently reported by UC/Berkeley graduate students. The previous record for a silicon transistor, reported in 1988, matched this speed at liquid nitrogen temperature but at room teperature switched at only 56 GHz.

The new transistor also operates at only 1.5V. The students reported their success in two papers at the International Electron Devices Meeting in San Francisco last December. They worked in the UC/Berkley Microfabrication Lab under the direction of Chenming Hu and Ping K. Ko, professors of electrical engineering. The new transistors are similar to the conventional MOSFETs used in most IC chips today, but are much smaller and built on silicon-on-insulator material. Results descrided so far have been for n-type MOSFET circuits.

The Berkley team also fabricated CMOS circuits that switch in 25 ps at 3.3 V and 17 ps at 5 V - faster than a 28 ps record reported several months ago by Toshiba for CMOS circuits on conventional silicon wafers. The research team also is experimenting with a hybrid combination of MOSFETs and bipolar transistors that have been able to operate at 0.5 V.
(Reference: Solid State Technology, March 1993.)

INFO 93

U Zagrebu je u vremenu od 19. - 23.10. 1993.godine održan 25. međunarodni sajam INFORMACIJSKE TEHNOLOGIJE. To je najznačajnija priredba ove vrste u Hrvatskoj, a održava se već dvadeset i peti puta. U pet paviljona zagrebačkog Velesajma bio je predstavljen izbor modernih proizvoda informatičke tehnologije. Izložbeni program sajma INFO 93 obuhvaćao je: računarske sustave, osobna računala, radne stanice, periferijsku opremu, telekomunikacisku opremu, opremu za umrežavanje, mikrofilsku opremu, audiovizualnu opremu, informacijske sustave. Također je bila prikazana primjena računala u proizvodnji, specijalizirana primjena računala, primjena računanala projektiranju i cjelovito vođenje proizvodnje pomoću računala. Uz izložbu je održan niz seminara, stručnih predavanja i prezentacija. Na sajmu je učestvovalo više od 470 firmi, koje su izložile proizvode iz 22 države iz Amerike, Azije i Evrope. Inozemne kompanije bile su predstavljene, najvećim dijelom, preko svojih distributora i zastupnika u Republici Hrvatskoj. Asortiman izložaka izabran je prema trenutačnoj potražnji na hrvatskom tržištu.

POSLOVNE NOVOSTI

RAZDIOBA SVJETSKOGA TRŽIŠTA POLUVODIČA

Prema istraživanjima koja je provela firma "Dataquest" kompanija INTEL zauzela je 1992.godine prvo mjesto na svjetskome tržištu poluvodiča s udjelom od 7.7% ukupne svjetske prodaje. INTEL je ostvario prodaju u iznosu od 5,06 milijardi US dolara. Godinu dana ranije INTEL je zauzimao treće mjesto, ali je zahvaljujući porastu prodaje za 26% izbio na prvo mjesto. Deset najvećih kompanija zauzima približno 54% svjetskoga tržišta. Gledajući regionalno japanske kompanije zauzimaju 43% svjetskoga tržišta, sjevernoameričke 41%, a sve ostale 16%. Rang lista deset najvećih pokazana je u tablici.

Rang 1992.	Rang 1991.	Kompanija	Iznos prodaje Milijardi $	Udio na tržištu %
1	3	Intel	5,06	7.7
2	1	NEC	4,98	7.6
3	2	Toshiba	4,76	7.3
4	4	Motorola	4,63	7,10
5	5	Hitachi	3,90	6,0
6	6	Texas Instruments	3.05	4,7
7	7	Fujitsu	2,58	3,9
8	8	Mitshubishi	2,31	3,5
9	10	Philips	2,11	3,2
10	9	Matshushita	1,99	2,9

Među 10 najvećih samo je jedna evropska firma, Philips, i to na devetom mjestu.

MEMORIJA S NAJMANJIM ĆELIJAMA

Hitachi i Texas Instruments dogovorili su zajednički razvoj nove 256-Mbit-ne DRAM. Dogovor obuhvaća sklopovski razvoj, razvoj proizvodne tehnologije i pakovanje. Za proizvodnju nove komponente koristiće se nova tehnologija, razvijena u Hitachiju, koja omogućuje izradu ćelija manjih od svih dosadašnjih. Uz geometriju 0.4 μm može se napraviti ćelija površine 1.28 μm što je 30% manje po bitu od dosadašnjih ćelija.

BELGIJA

EASTERN EUROPE TECHNOLOGY Report is an up-to-date reference that details more than 700 leading sources of know-how, including addresses, phone, fax, and telex numbers; names of key personnel; details of research budgets and staffing; and authoritative summaries of research activities.

Price: US$ 850. More information is available from DPG Communications Ltd., 4 Rue de la Presse, 1000 Brussels, Belgium; ph:+32 2 217 850; fax +32 2 736 8898.
(From "Solid State Tehnology", March 1993)

ISRAEL
WEINZAN INSTITUTE OF SCIENCE

Researchers recently demonstrated a simple room-temperature procedure for making a transistor. The technique, in which a high electric field is applied across a homogenous piece of semiconductor, requires no impurity implantation or heat-curing steps. It was initially applied to the experimental semiconductor matrial copper indium selenide. The aproach is not yet sufficiently

refined for producing the microscopic transistor components of ICs, nor has it been applied to silicon. It was emphasized that practical use for microelectronic devices is not assured and in any case, is many years away. The researchers use electric fields to break down the uniform space distribution of component ions of the semiconductor, avoiding the need to introduce foreign ions. Stable charge distributions formed in the material resemble those obtained with normal doping processes. (From "Solid State Tecnology", march 1993.)

SEMI SETS UP RUSSIAN CENTRE

SEMI has set up Microelectronic Technology Centre in Russia, to be used for demonstrating production equipment, and providing training in a small clean room.SEMI got a $ 500000 grant from US governement to set up the centre. It has to match this sum over the next three years.

"There are benefits of this agreement for both US and Russian-based companies," says Paul Davis, director of SEMI Europe, who led a trade mission to Russia in 1991.

"There is some excellent technology in the former Soviet Union. This agreement will help us facilitate the interchange of production technology between the Russian and US semiconductor industries. To see the benefit for US industry, one only has to look at the long-term potential of this area as an electronic market."

The Microelectronic Centre will, at least initially, only be open to US companies to benefit directly from it, because of the US goverment's financial involvement. SEMI hopes that it can attract additional finance from elsewhere, which could allow it to open up the MTC to non-US companies.

"In addition to creating market opportunities for US companies, The Microelectronics Technology Centre will stimulate industry in Russia as well," says SEMI president William Reed. "We are pleased to begin this partnership with the Department of Commerce and serve as a focal point of US semiconductor industry activities in Russia. We hope the result of this agreement will provide a large boost to trade and investment within the former Soviet Union."
(From European Semiconductor april 93.)

SIGN OF CHANGE FROM JAPAN

"Japanese semiconductor manufacturers would be wise to take the short-term approach to bussiness if they are to prosper in the future." This was a key point made by Seichi Denda of Konica Corp., the keynote speaker at the recent Semicon/Japan exhibit. This startling advice was based in part upon what Denda reffered to us the four myths of the semiconductor business. These myts are: (1) market growth will continue forever, (2) investment will always pay, (3) achieving a large market share is most important according to learning curve theory, and 4) that plants should be kept operating.

In particular, Denda pointed out, the learning curve theory has been one of the principle guidelines for Japanese manufacturers. This theory indicates that because similar technology is involved and because the market is growing, that the more you make, the lower the cost, as a result, the larger the market share. Denda noted that these factors are no longer true and so the learning curve theory may no longer be appropriate. He also noted that because of this change, the long range philosophy that has typified the Japanese approach may have to be abandoned. In this situation, semiconductor production may have to be managed with rather short range considerations, just like other simple products and as a result a Japanese may be forced to have short term vision. It is this idea that is closer to what is called the "U.S. policy maker".

An important factor that is affecting the semiconductor marketplace, said Denda, is that the semiconductor is now basically a commodity and no longer a speciality product. This fact must affect how management views the product when making decisions. Also a factor is that the capital required to product to larger DRAMs is surpassing the should level of investment. In Denda's opinion, because the semiconductor industry has entered a slow growth phase, that the large investment days are over and it is now necessary to change investment policies with the new pattern being expected to be a moderate one.

As one other example of change, Denda pointed out that the classical "Silicon Cycle" in which the memory generations evolved every three years has now changed to where the peak sales of 4Mb DRAMs peakink from 4-5 years after 1Mb sales with this cycle probably stretching even further for future generations. Because some manufacturers are reporting large deficits, capital investment has been cut as much as 30% by many, R&D investments have been reduced to 10% of sales, and R&D departments have been restructured. Emphasis has now been placed upon cost saving measures! These are just a few of the observations made by Denda, and indeed indicate sign of change in Japan. Signs that should be carefully considered by all in the industry when making plans for the future.

THINK GLOBALLY, EUROPE

(Prenosimo u cijelosti "Think globally, Europe" autor kojega je Willem D. Maris direktor AMS Litography B.V. nadajući se da će članak biti zanimljiv čitaocima našega časopisa. Članak je objavljen u časopisu "Solid State Technology" od marta 1993)

European semiconductor companies have strong roles to play in world market, despite recent dire predictions. Europeans now understand that cornering their native market is not the key to success. Tuday's markets are

global-not regional-so dominating the European semiconductor market will not ensure worldwide success. To be globally competitive, companies must think and act beyond their own geographic markets.

Some have argued that Europe's semiconductor industry must conglomerate into one gigantic,self-reliant keiretsu or become an industrial colony of the USA or Japan. But vertical integration and mergers are not necessarily the best solution to the long-term challenges of survivability in a rapidly changing industry.

To be successful, Europeans must be active at all levels of worldwide business - in researching and developing new processes and products, and in pushing technologies into new applications. Individual companies no longer have the resources to go it alone in all of these areas and across all geographic markets. There is, however, a viable tactic at our disposal: global alliances.

European companies must aggressively pursue, attract, and participate in strategic alliances with companies based outside Eurpope. The working models are evident in such international pairings as AMD and Fujitsu, TI and Hitachi, NEC and AT&T, and even multinational alliance among IBM, Toshiba, and Siemens. Today's growing roster of successful partnership even includes associations between formerly fierce competitors. Why? Because companies are finding strategic alliances to be vital resources. International partnerships capitalize on the strenghts of each partner to maintain a competitive place in a world where access to new information is increasingly widespread and instantaneous. To think anything less than globally is literarlly to let the world's markets pass you by.

Manufacturers must find ways to deliver products that are universally acceptable and competitive. This takes familiarity with and commitment to all markets - a near-impossible assigment for a single company. Alliances are not limited to "horizontal" partnerships between manufactures in the same industry with complementary technologies; "vertical" alliances between semiconductor producers and capital equipment suppliers have also borne great success. From ASM lithography's own experience, we benefited greatly from the design inputs and feedback received from our key strategic partners in developing the PAS 5500 steppers.

Industry consortia ranging from the US-based SEMATECH to Europe's international JESSI program serve invaluable roles in keeping the lines of communication open between IC makers and equipment manufacturers. These programs are true working partnership beetwen users and suppliers of wafer-fab technology.

There has been talk of forming an European version of SEMATECH, which would be very beneficial for all levels of Europe's semiconductor industry. An European version of organization would have implications on global scale, because the likely sharing of information between US and European groups would benefit from both..

The competitiveness concerns of IC manufacturers and capital equipment suppliers are inextricably linked. As Dr. Nico Dekkers of JESSI pointed out the recent TEC 92 conference in Grenoble, of the 2700 man years that JESSI invested in R&D work in 1992, one-fourth of that valuable tie was directed at equipment and materials programs. As Dr. Dekkers says, "Considering the fact that IC, sales worldvide are roughly 10 times those of equipment and materials, (JESSI's) attention to equipment and materials seems large. This is a clear reflection, however, of the fact.... that new IC proccess generations fully rely on new equipment generations."

Suppliers and users of process equpment must work hand-in-hand to receive maximum, reciprocal benefits from a working partnership. For example, open communication of each partner's needs and capabilities has helped minimize risk in making the multimillion-dollar decision required to bring new products to market.

Strategic partnering is the best tactic available to European companies - and companies around the world, for that matter - striving to succeed in our increasingly competitive global industry. And European partners have much to offer: markett access into the European Economic Community, shared data from consortia research, and geographic and cultural ties with the next great emerging market, Eastern Europe.

Europe indeed has a place in the world semiconductor market, but it must think globally and adapt to strategic alliances.

FAR EAST LAGS IN RF-ID DEVELOPMENT

Neither the Koreans nor Japanese have invested heavily in the radio-frequency identifier market.

Tokyo-based electronics gianst NEC Corp. and Fujitsu Ltd., for example, do not manufacture RF-IDs. NEC purchases them from Sony Corp., also of Tokyo, and other firms for inclusion in the systems it provides, including:

- a Post Office Management System installed at the New Tokyo Post Office, in which RF-IDs are used at the gate of the pickup/delivery trucks, the system can program the routing of trucks as a function of job assignment.
- building security systems where gates open automatically when an individual carrying an RF-ID approaches.

Researchers at **Hyundal Electronics Industries Co., Ltd., Samsung Electronics Co.,** and **Texas Instruments Korea**, all based in Seoul, say their companies have no plans to pursue RF- ID.

Electronics, feb. 93

RF-ID: a new market poised for oxplosive growth

Though the new radiofrequency identification (RF-ID) market is in its infancy, many semiconductor and system vendors are bracing for explosive growth over the next several years.

David Slinger, general manager of Texas Instruments Registration and Identification Systems (TIRIS) North American Operation for Dallas-based Texas Instruments Inc., says the U.S. market is worth less than US$50 million, but it is growing rapidly.

Representatives at Hughes Aireraft Co. in Los Angeles agree, pegging the U.S. RF-tag market at $40 million and readers at $120 million. Worldwide, they estimate both are worth nearly $480 million and predict that the market will grow at 22% per year over the next few years.

AIM, the Automation Identity Systems Manufacturers and Suppliers Association, sets the West European market for all. identification systems, (including barcode-based systems) at about US$2 billion in 1990. Of that, RF-based systems had roughly $100 million (which includes nearly $21 millon for Germany alone) in 1990.

Nevertheless,RF systems are growing faster than the average. Holger Franksen, at Siemens' Automation Group in Nuremberg, Germany, figures that West Europe's RF systems market grew to $125 million in 1992. In Germany alone, sales reached $31 million last year, he estimates.

If all applications for RF-IDs were taken up, the total market today would be worth more than $6 billion, asserts Noel Middleton, European business manager for TIRIS, at Bedford, England.

Middleton predicts TIRIS will contribute $180 million to TI's total sales by 1995 and more than $1 billion by the year 2000. "Sales have doubled each year since TIRIS formed as a business within TI", Middleton says, and he sees no indication that the progress will slow.

Electronics, feb. 93

DISSECTING AN RF-IDENTIFIER

A radio-frequency identifier is a complex set of circuits that must sell for a low price and operate on very small voltage. Ron Courtois, director of sales and marketing at ABB GAFO Inc., a mixed signal ASIC vendor in San Diego, Dalif., says the circuit demands no external components except an antenna coil.

In operation, Courtois says an incoming RF burst provides power to run the circuit nad contains commands for the circuit itself. From the RF burst, a bridge circuit rectifies the incoming RF and charges a capacitor.

A regulator holds the voltage across the capacitor at a constant 2 V to power the chip. The logic on board the device interprets the command extracted from the RF burst. If the command is interrogating the identifier, the logic simply reads a number from the on-board EEPROM nad transmits a reponse.

If the transmission is changing information on the identifier, the logic on board stores the new information into the on-board EEPROM memory. A voltage pump increases the 2 V to 15 V to program the nonvolatile memory.

Electronics, feb. 93

AMERICAN SPECIALIST PREISES SUCCESSFUL AMS MODEL

Lewis H. Young, noted Editorial Director of the leading publication in the field of electronics in the USA- "Electronics Business", Cahners Publishing, highly praises the proven semiconductor model of Austria Mikro Systeme International AG (AMS) in his lead article. Under the heading "AMS designs a new model for a semiconductor company" Young describes the successful model of the company in his three page critical analysis and remarks: "The concept is based on a highly focused strategy, a customer-orented organizaton motivated mainly by creative freedom, and a determination to be profitable".

Young sees the main reasons for the success of the AMS strategy in the well-aimed orientation of the company and in the:

- clear mission and vision of the management;
- ideal size of the company;
- high technological competence in the field of analogue/digital ASICs;
- quick translation of ideas into decisions or production;
- effectiveness of the design team;
- financial stability of the company and
- the fact that AMS combines "under one roof" an integrated facility.

AMS, the only Austrian IC manufacturer and listed on the Vienna Stock Exchange and the SEAQ in London since July 1993, has further strengthened its top position with its innovative products and services in the semiconductor market: AMS is leading in the European market: No. 1 in the field of cell based mixed analogue/digital ASICs (application specific integrated circuits).

A M S
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A-8141 Unterpremstaetten, Austria
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*Tel (03136) 500-0**

TEHNOLOŠKI PROCES ZA 50 V COS NA TAIWANU

"Holtek Microeletronics Inc" u Hsinču u zajednici s "Electronics Research & Service Organization" (ERSO), koja je u vlasništvu vlade, razvijaju 50- volt COS procesnu tehnologiju za industrijsku upotrebu.

50-voltni CMOS je bitni dio u televiziji visoke rezolucije i kod LCD pokazivača. Očekuje se da će tržište za 50-V CMOS sklopove porasti do 1995. godine na US$ 240 miliona s US$ 80 miliona koliko je bilo 1990. godine. Na Taiwanu smatraju da je bitno usvojiti ovu tehnologiju, jer je Japan i USA već posjeduju.

TAIWAN GOVERNMENT CONSIDERS AID TO 16M DRAM VENTURE

The government's attitude toward financing a state-of-the- art semiconductor facility is crucial to Taiwan's prospect in sharing the future market of 16-Mbit dynamic random acces memory.

In view of the potential competition from other Asian countries, the Hsinchu-based Texas Instruments-Acer Inc. (TI-Acer) is planning to invest US$92 million in 1993, with 50% of the funding from the Taiwan governent, to expand its Hsinchu 4-Mbit DRAM facility. It aims to increase monthly capacity to 15,000 wafers by the end of this year, and to introduce the 0.5-micron 16-Mbit DRAM technology in Taiwan. This is the first part of TI-Acer's US$300 million 1993-1995, investment plan proposed late in 1992.

Stan Shih, chairman of the board of TI-Acer, says the time is running out for Taiwan to "catch the train" which Japan, South Korea, and even Singapore are alredy aboard, all with certain degree of help from local governments. Without the government aid, Ti-Acer is unlikely to carry out the plan on-time alone, and a delay may put Taiwan at disadvantage, he says. Taiwan's Ministry of Economic Affairs has looked into Ti-Acer's request, but has not reached conclusion.

The Dallas-based TI, a major stockholder of TI-Acer, is building a 16- Mbit DRAM plant in Singapore with the help of tax breaks and preferential price in land ascquisition. The Hewlett-Packard Co. of Palo Alto, Calif., and Tokyo's Canon Corp. contribute to the Singapore venture, which is expected to be complete by the end of this year.

EVROPA R&D JESSI TAKES STOCK, SEEKS EXTENSION OF PROGRAMS

Jessi, the Joint European Submicron Silicon program, appears to be right on course and scoring remarkable results. To garantee its continued success, Raimondo Paletto, chairman of the Jessi board, is appealing to the European Community to step up funding the program.

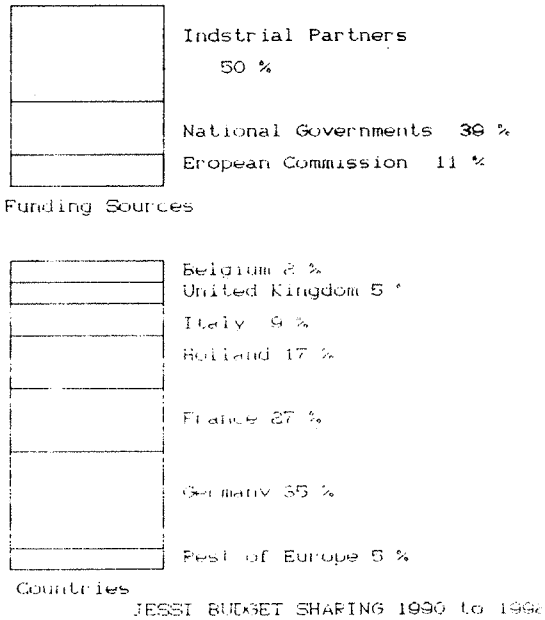
Paletto is also urging the EC to extend the program beyond 1996, the year it is now scheduled to end.

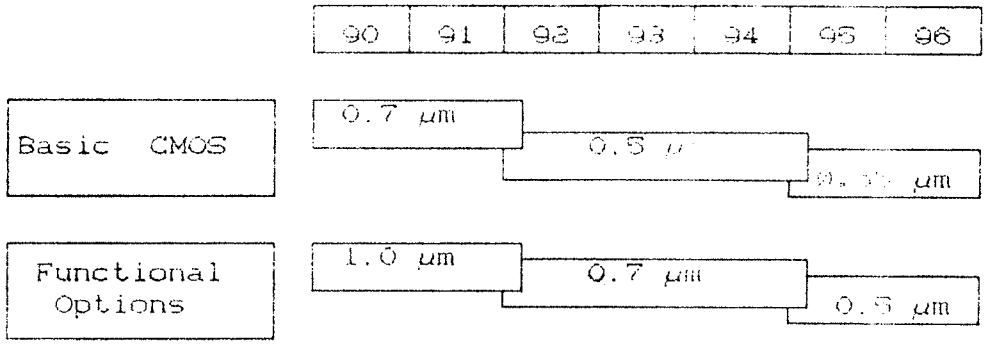
In supporting his appeal for an extension, Paletto points out that microelectronics will top its potential at the end of this decade. Microelectronics, he adds, will push many new prodcts that Jessi has identified and will be pulled by upcoming market demands. Forecast see electronics technology dominanting every other industrial sector in Erope by the year 2000.

Since 1990, the year that Jessi got underway, until the end of 1992, program funding amounted to about US$1x10^9, with 50 percent contributed by industry, 3 percent by the national governments, and 11 percent by the EC (see graph, "Jessi budget sharing"). In 1992, the first year of Jessi's main phase, funding came to roughly $460x10^9.

Among the milestones the program has reached to date are the development of 16-Mbit DRAMs, 16-Mbit EPROMS and other innovative circuits. Jessi has also made available 0.7-micron CMOS technology (see graph, "Jessi CMOS logic program outline"). A smaller version of a 4-Mbit DRAM uses 0.65 micron design rules. In addition, an 8-inch manufacturing process was started.

Meanwhile, in Jessi's ADEQUAT (Advanced Development for Quarter Micron CMOS Technology) project, which started in August 1992, more than 100 re-





JESSI CMOS LOGIC PROGRAM - Outline

searchers are working on 0.25-micron technology, the prerequisite for future systems on chip.

NOVA TEHNOLOGIJA ČINI SILICIJ BRŽIM OD GALIUM ARSENIDA

Stručnjaci iz "Siemens, Central Research Laboratories" iz Minhena referirali su na "International Solid State Conference" o novim ultra brzim silicijskim sklopovima. Sklopovi su namijenjeni za primjenu u optičkim i satelitskim komunikacijama i visokofrekventnoj instrumentaciji.

Za proizvodnju ovih ultrabrzih elemenata koristi se t. zv. SEG (Selective Epitaxial Technology) postupak, već ranije razvijen u Siemensu. Drugi važan činilac je poboljšana tehnika za optimalizaciju projektiranja ultra brzih sklopova koja je razvijena na "Ruhr University in Bochum" u Njemačkoj.

SEG postupkom postiže se smanjenje debljine baze tranzistora, a samim time i vremena prolaza. Elementi su također karakterizirani vrlo malom potrošnjom snage. Na primjer pet stepeni djelitelj frekvencije, koji radi na 16 GHz troši u prvome stupnju dijeljenja samo 8 mW. U usporedbi s galijum arsenidnim sklopovima ovi silicijumski sklopovi znatno su brži. Na primjer brzina demultipleksora je 40 Gb/s prema 27 Gb/s za GAs sklop. Siemens silicijski multipleksor ima brzinu 34 Gb/s prema 30 Gb/s kod GAs multipleksora.

S ovim novim sklopovima stručnjaci Siemens-a i Ruhr univerziteta pomaknuli su granice brzina za silicij u nove visine. Oni su pokazali da se dobro uvedeni, jeftini, laki za rukovanje silicijski materijal može koristiti za ekstremno brze sklopove, te da nije uvijek potrebno ići na skupi, nezgodni za procesiranje galijum arsenid ili indium fosfid.

Vijesti je pripremio
Miroslav Turina

KOLEDAR PRIREDITEV 1994

FEBRUAR

01.02.1995
DEUTCHES ISHM SEMINAR ON MCMS AND COB
Göppingen, Germany

28.02. - 0.0. 1994
EDAC - ETC EUROASIC 94 The European Design & Test Conference - Exibition
PARIS, France
(info.B. Courtois, Grenoble, tel. 76 57 45 00)

MAREC

14.03. - 2.03. 1994
CEBIT 94
HANNOVER, Germany
(info. PAGAT PLUS tel. (061) 266 369)

23.03. - 24.03.1994
5th MICROELECTRONICS SALON
Paris, France

APRIL
9th Annual Gethering KOREMA
ZAGREB, Hrvatska
(info. 85 41 611 944 Ext. 127)

MAJ
23.05. - 27.05. 1994
Mipro 94
OPATIJA, Hrvatska
(info. 385 51 211 051)

JUNIJ
06.06. - 08.06. 1994
MICROTECH 94
Anugrana, Italy

12.06. - 15.06.1994
TTFS 94 (WORKSHOP ON THICK AND THIN SENSORS AND THEIR APPLICATIONS IN EKOLOGY
Szklaska Poreba, Poland

MIDEM
Society for Microelectronics, Electronic Components and Material
Dunajska 10, 61000 Ljubljana
SLOVENIJA

22nd INTERNATIONAL CONFERENCE ON MICROELECTRONICS, MIEL'94
30th SYMPOSIUM ON DEVICES AND MATERIALS, SD'94

Dear Sirs,

MIEL-SD is an international conference organised by MIDEM, Slovenian Society for Microelectronics, Electronic Components and Materials. MIEL-SD used to be a Yugoslav microelectronics conference with strong international participation, especially of neighbouring countries. After the collapse of former Yugoslavia, MIEL has continued its program as an international conference providing opportunity for experts from all over the Europe to meet and discuss new developments in the field of microelectronics, electronic components and materials.

We expect that the conference may be of importance especially as a gathering of industrial and academic microelectronics laboratories of the surrounding regions such as Alpe-Adria countries including Italy, Austria, Switzerland, Hungary, Slovakia, Croatia, Slovenia, ...

Therefore, we propose a new initiative for a get-together of representatives of microelectronics companies and laboratories at the next MIEL-SD Conference where their research and development achievements would be presented.

The region Alpe-Adria, although a developed technological area, comprises several countries that in the past had no significant relations despite the small distances between their microelectronics research and development centres. Besides, following the major political changes that have occurred in some countries bordering on the European Community, new possibilities for co-operation, joint ventures and even ownership have lately arisen.

It is the intention of the MIEL-SD Conference to organise presentations of microelectronics labs and enterprises in order to get acquainted with the work of similar groups and establish new contacts. The presentations will be organised following afternoon sessions with regular scientific contributions. The speaker will be given 15 minutes to present his research group, company or specific project. Before we definitely introduce this concept into regular Conference, we would like to know whether You may be interested in this kind of additional presentation.

Therefore, You are kindly requested to reply to this letter if Your group or Company should be interested in such a presentation and if you were willing to present your activities. Any other suggestions will also be appreciated.

Organising Committee of the MIEL-SD Conference. Contact person:

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For Your information: this year the Conference will take place from September 28 to 30 in one of Slovenian tourist resorts. Besides regular papers given by participants, several prominent experts from Europe will present invited papers as an introduction to different sessions such as Integrated Circuits, Amorphous Silicon Devices, Device Physics, Modelling, Technology, Education, Characterisation, Thick Films and Thin Films. Official language of the Conference is English.

NAVODILA AVTORJEM

Informacije MIDEM je znanstveno-strokovno-društvena publikacija Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale-MIDEM. Časopis objavlja prispevke domačih in tujih avtorjev, še posebej članov MIDEM, s področja mikroelektronike, elektronskih sestavnih delov in materialov, ki so lahko:

izvirni znanstveni članki, predhodna sporočila, pregledni članki, razprave z znanstvenih in strokovnih posvetovanj in strokovni članki.

Članki bodo recenzirani.

Časopis objavlja tudi novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter druge relevantne prispevke.

Strokovni prispevki morajo biti pripravljeni na naslednji način

- 1. Naslov dela, imena in priimki avtorjev brez titul.
- 2. Ključne besede in povzetek (največ 250 besed).
- 3. Naslov dela v angleščini.
- 4. Ključne besede v angleščini (Key words) in podaljšani povzetek (Extended Abstract) v angleščini.
- 5. Uvod, glavni del, zaključek, zahvale, dodatki in literatura.
- 6. Imena in priimki avtorjev, titule in naslovi delovnih organizacij, v katerih so zaposleni.

Ostala splošna navodila

1. V članku je potrebno uporabljati SI sistem enot oz. v oklepaju navesti alternativne enote.

2. Risbe je potrebno izdelati s tušem na pavs ali belem papirju. Širina risb naj bo do 7.5 oz. 15 cm. Vsaka risba, tabela ali fotografija naj ima številko in podnapis, ki označuje njeno vsebino. Risb, tabel in fotografij ni potrebno lepiti med tekst, ampak jih je potrebno ločeno priložiti članku. V tekstu je potrebno označiti mesto, kjer jih je potrebno vstaviti.

3. Delo je lahko napisano in bo objavljeno v kateremkoli jugoslovanskem jeziku v latinici in v angleščini.

Uredniški odbor ne bo sprejel strokovnih člankov, ki ne bodo poslani v dveh izvodih.

Avtorji, ki pripravljajo besedilo v urejevalnikih besedil, lahko pošljejo zapis datoteke na disketi (360 ali 1,2) v formatih ASCII, wordstar (3.4, 4.0), wordperfect, word, ker bo besedilo oblikovano v programu Ventura 2.0. Grafične datoteke so lahko v formatu HPL, SLD (AutoCAD), PCX ali IMG/GEM.

Avtorji so v celoti odgovorni za vsebino objavljenega sestavka. Rokopisov ne vračamo.

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Elektrotehniška zveza Slovenije
Dunajska 10, 61000 Ljubljana

UPUTE AUTORIMA

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izvorni znanstveni članci, predhodna priopćenja, pregledni članci, izlaganja sa znanstvenih i stručnih skupova i stručni članci.

Članci će biti recenzirani.

Časopis također objavljuje novosti iz struke, obavijesti iz radnih organizacija, instituta i fakulteta, obavijesti o akcijama društva MIDEM i njegovih članova i druge relevantne obavijesti.

Stručni članci moraju biti pripremljeni kako slijedi

- 1. Naslov članka, imena i prezimena autora bez titula.
- 2. Ključne riječi i sažetak (najviše 250 riječi).
- 3. Naslov članka na engleskom jeziku.
- 4. Ključne riječi na engleskom jeziku (3Key Words) i produženi sažetak (Extended Abstract) na engleskom jeziku.
- 5. Uvod, glavni dio, zaključni dio, zahvale, dodaci i literatura.
- 6. Imena i prezimena autora, titule i naslovi institucija u kojima su zaposleni.

Ostale opšte upute

1. U prilogu treba upotrebljavati SI sistem jedinica od. u zagradi navesti alternativne jedinice.

2. Crteže treba izraditi tušem na pausu ili bijelom papiru. Širina crteža neka bude do 7.5 odnosno 15 cm. Svaki crtež, tablica ili fotografija treba imati broj i naziv koji označuje njen sadržaj. Crteže, tabele i fotografije nije potrebno lijepiti u tekst, već ih priložiti odvojeno, a u tekstu samo naznačiti mjesto gdje dolaze.

3. Rad može biti pisan i biti će objavljen na bilo kojem od jugoslavenskih jezika u latinici i na engleskom jeziku.

Autori mogu poslati radove na disketama (360 ili 1,2) u formatima tekst procesora ASCII, wordstar (3.4. i 4.0), word, wordperfect pošto će biti tekst dalje obraden u Venturi 2.0. Grafičke datoteke mogu biti u formatu HPL, SLD (AutoCAD), PCX ili IMG/GEM.

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Za sadržaj članaka autori odgovaraju u potpunosti. Rukopisi se na vraćaju.

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original scientific papers, preliminary communications, reviews, conference papers and professional papers.

All manuscripts are subject to reviews.

Scientific news, news from the companies, institutes and universities, reports on actions of MIDEM Society and its members as well as other relevant contributions are also welcome.

Each contribution should include the following specific components:

- 1. Title of the paper and authors' names.
- 2. Key Words and Abstract (not more than 250 words).
- 3. Introduction, main text, conclusion, acknowledgements, appendix and references.
- 4. Authors' names, titles and complete company or institution adress.

General information

1. Authors should use SI units and provide alternative units in parentheses wherever necessary.

2. Illustrations should be in black on white or tracing paper. Their width should be up to 7.5 or 15 cm. Each illustration, table or photograph should be numbered and with legend added. Illustrations, tables and photografphs are not to be placed into the text but added separatelly. Hower, their position in the text should be clearly marked.

3. Contributions may be written and will be published in any Yugoslav language and in english.

Authors may send their files on formatted diskettes (360 or 1,2) in ASCII, wordstar (3.4 or 4.0), word, wordperfect as text will be formated in Ventura 2.0. Graphics may be in HPL, SLD (AutoCAD), PVX or IMG/GEM formats.

Papers will not be accepted unless two copies are received.

Authors are fully responsible for the content of the paper. Manuscripts are not returned.

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Slovenia

К

Капацитивност, еквивалентна топлинска 2.4.7
Капацитивност (на полупроводнички елемент), топлинска 2.4.5
Коефициент (на полупроводник) Холов 2.1.24
Кукиште, температура 2.5.1

Л

Лавински напон 2.1.17
Лавински пробив (на полупроводнички PN–спој) 2.1.16
Лебдечки напон 2.4.2
Легиран спој 2.1.8

Н

Напон, Зенеров 2.1.20
Напон, инверзен 2.4.1
Напон, лавински 2.1.17
Напон, лебдечки 2.4.2
Напон, пробивен 2.4.3
Насока (на PN–спој), директна 2.3.3
Насока (на PN–спој), инверзна 2.3.4
Насочувачка диода, полупроводничка 2.2.5
Насочувачка диода со контролиран лавински пробив 2.2.12
Насочувачка диода со лавински пробив 2.2.11
Насочувачки блок, полупроводнички 2.2.6
Носител 2.2.11
Носители (во некоја област на полупроводникот), основни 2.1.12
Носители (во некоја област на полупроводникот), споредни 2.1.13
Носител (на електрицитет) 2.1.11

О

Одводник на пренапони, селенски 2.2.21
Осиромашен слој 2.1.14
Основни носители (во некоја област на полупроводникот) 2.1.12
Отпорност, еквивалентна топлинска 2.4.8
Отпорност (на полупроводнички елемент), топлинска 2.4.4

П

Полев транзистор 2.2.16
Полупроводник 2.1.1
Полупроводник од I–тип 2.1.5
Полупроводник од N–тип 2.1.3
Полупроводник од P–тип 2.1.4
Полупроводник, примесен 2.1.2
Полупроводничка диода 2.2.2
Полупроводничка насочувачка диода 2.2.5
Полупроводнички елемент 2.2.1
Полупроводнички насочувачки блок 2.2.6
Премин (спој) 2.1.6
Преодна топлинска импеданса 2.4.9
Приклучок (на полупроводнички елемент) 2.3.1
Примесен полупроводник 2.1.2
Пробивен напон 2.4.3
Пробив (на инверзно поларизиран PN–спој) 2.1.15
Пробив (на полупроводнички PN–спој), Зенеров 2.1.19
Пробив (на полупроводнички PN–спој), лавински 2.1.16
Пробив (на полупроводнички PN–спој), топлински 2.1.18

С

Селенски одводник на пренапони 2.2.21
Сигнална диода 2.2.9
Складирање, температура 2.5.2
Слој, осиромашен 2.1.14
Спој, дифундиран 2.1.9
Спој, извлекуван 2.1.10
Спој, легиран 2.1.8
Спој, PN 2.1.7
Спој (премин) 2.1.6
Споредни носители (во некоја област на полупроводникот) 2.1.13

Т

Температура, виртуелна 2.5.4
Температура, внатрешна еквивалентна 2.5.4
Температура на кукиштето 2.5.1
Температура на складирање 2.5.2

Тиристор 2.2.18
Топлинска импеданса за импулсна струја 2.4.10
Топлинска импеданса, преодна 2.4.9
Топлинска капацитивност, еквивалентна 2.4.7
Топлинска капацитивност (на полупроводнички елемент) 2.4.5
Топлинска отпорност, еквивалентна 2.4.8
Топлинска отпорност (на полупроводнички елемент) 2.4.4
Топлинска шема, еквивалентна 2.4.6
Топлински фактор на намалување на граничната моќност на дисипација 2.5.3
Транзистор 2.2.13
Транзистор, биполарен 2.2.14
Транзистор, полев 2.2.16
Транзистор, униполарен 2.2.15
Транзистор, фото 2.2.17
Тунел–диода 2.2.7
Тунелирање, ефект 2.1.21
Тунелирање (низ PN–спој) 2.1.22

Ќ

Ќелија, фотонапонска 2.2.20
Ќелија, фотопроводна 2.2.19

У

Униполарен транзистор 2.2.15

Ф

Фактор на намалување на граничната моќност на дисипација, топлински 2.5.3
Фото–диода 2.2.8
Фотоелектричен ефект 2.1.25
Фотонапонска ќелија 2.2.20
Фотонапонски ефект 2.1.26
Фотопроводна ќелија 2.2.19
Фото–транзистор 2.2.17
Фреквенција, гранична 2.6.1

Х

Холов ефект 2.1.23
Холов коефициент 2.1.24

Ш

Шема, еквивалентна топлинска 2.4.6

TERMINOLOŠKI STANDARDI

3.4 Abecedni seznam izrazov u slovenskem jeziku

B

Bipolarni tranzistor 2.2.14

D

Difuzijski spoj 2.1.9
Drsna napetost 2.4.2

E

Ekvivalentna toplotna kapaciteta 2.4.7
Ekvivalentna toplotna upornost 2.4.8
Ekvivalentno toplotno vezje 2.4.6
Elektroda (polprevodniškega elementa) 2.3.2

F

Fizikalni izrazi 2.1
Fotodioda 2.2.8
Fotoelektrični pojav 2.1.25
Fotonapetostna celica 2.2.20
Fotonapetostni pojav 2.1.26
Fotoprevodna celica 2.2.19
Fototransistor 2.2.17

H

Hallov koeficient (polprevodnika) 2.1.24
Hallov pojav 2.1.23

I

Inverzna napetost 2.4.1
Inverzna smer (PN-spoja) 2.3.4
Izrazi za mejne vrednosti in karakteristike 2.4

K

Karakteristike 2.6
Krmiljena plazovna usmerjalna dioda 2.2.12

L

Legirani spoj 2.1.8

M

Manjšinski nosilec (v polprevodniškem področju) 2.1.13
Mejna frekvenca 2.6.1

N

Napetost plazovnega preboja 2.1.17
Nečistotni polprevodnik 2.1.2
Nosilec elektrine 2.1.11

O

Osiromašeni sloj 2.1.14

P

Plazovna usmerjalna dioda 2.2.11
Plazovni preboj 2.1.16
PN-spoj 2.1.7
Poljski transistor 2.2.16
Polprevodnik 2.1.1
Polprevodnik tipa I 2.1.5
Polprevodnik tipa N 2.1.3
Polprevodnik tipa P 2.1.4
Polprevodniška dioda 2.2.2
Polprevodniška komponenta 2.2.1
Polprevodniška usmerjalna dioda 2.2.5
Polprevodniški element 2.2.1
Polprevodniški usmerjalni stavek 2.2.6
Preboj (inverzno polariziranega PN-spoja) 2.1.15
Prebojna napetost 2.4.3
Prehodna toplotna impedanca 2.4.9
Prepustna smer (PN-spoja) 2.3.3
Priključek (polprevodniškega elementa) 2.3.1

R

Referenčna dioda 2.2.3

S

Selenski omejevalnik prenapetosti 2.2.21
Signalna dioda 2.2.9
Splošni izrazi 2.3
Splošni izrazi in definicije 2
Spoj 2.1.6
Stabilizacijska dioda 2.2.4

T

Temperature 2.5
Temperatura okrova 2.5.1
Temperatura skladiščenja 2.5.2
Temperaturni razbremenitveni faktor 2.5.3
Termični preboj (polprevodniškega PN-spoja) 2.1.18
Tiristor 2.2.18
Toplotna impedanca pri impulznem obratovanju 2.4.10
Toplotna kapaciteta (polprevodniškega elementa) 2.4.5
Toplotna upornost (polprevodniškega elementa) 2.4.4
Transistor 2.2.13
Transistor na poljski pojav 2.2.16
Tunelska dioda 2.2.7
Tunelski pojav 2.1.21
Tunelski proces (v PN-spoju) 2.1.22

U

Unipolarni transistor 2.2.15
Unitunelska dioda 2.2.10

V

Večinski nosilec (v polprevodniškem področju) 2.1.12
Virtualna temperatura 2.5.4
Vlečeni spoj 2.1.10
Vrste elementov 2.2

Z

Zaporna napetost 2.4.1
Zaporna smer (PN-spoja) 2.3.4
Zenerska napetost 2.1.20
Zenerski preboj (polprevodniškega PN-spoja) 2.1.19

4 Seznama v tujih jezikih

4.1 Abecedni seznam izrazov v angleškem jeziku

A

Alloyed junction 2.1.8
Avalanche breakdown (of semiconductor PN junction) 2.1.16
Avalanche rectifier diode 2.2.11
Avalanche rectifier diode, controlled 2.2.12
Avalanche voltage 2.1.17

B

Backward diode 2.2.10
Bipolar transistor 2.2.14
Breakdown (of a reversebiased PN junction) 2.1.15
Breakdown (of a semiconductor PN junction), avalanche 2.1.16
Breakdown (of a semiconductor PN junction), thermal 2.1.18
Breakdown (of a semiconductor PN junction), Zener 2.1.19
Breakdown voltage 2.4.3

C

Capacitance, equivalent thermal network 2.4.7
Capacitance, (of a semiconductor device), thermal 2.4.5
Carrier 2.1.11
Carrier (in a semiconductor region), majority 2.1.12
Carrier (in a semiconductor region), minority 2.1.13
Case temperature 2.5.1
Cell, photoconductive 2.2.19
Cell, photovoltaic 2.2.20
Charge carrier (carrier) 2.1.11
Constant, Hall 2.1.24
Controlled avalanche rectifier diode 2.2.12
Cut-off frequency 2.6.1

D

Depletion layer 2.1.14
Device, semiconductor 2.2.1
Diffused junction 2.1.9
Diode, avalanche rectifier 2.2.11
Diode, backward 2.2.10
Diode, controlled avalanche rectifier 2.2.12
Diode, photo 2.2.8
Diode, semiconductor 2.2.2
Diode, semiconductor rectifier 2.2.5
Diode, signal 2.2.9
Diode, tunnel 2.2.7
Diode, unitunnel 2.2.10
Diode, voltage reference 2.2.3
Diode, voltage regulator 2.2.4
Direction (of a PN junction), forward 2.3.3
Direction (of a PN junction) reverse 2.3.4

E

Effect, Hall 2.1.23
Effect, photo-electric 2.1.25
Effect, photovoltaic 2.1.26
Effect, tunnel 2.1.21
Electrode (of a semiconductor device) 2.3.2
Equivalent thermal network 2.4.6
Equivalent thermal network capacitance 2.4.7
Equivalent thermal network resistance 2.4.8
Extrincic semiconductor 2.1.2

F

Field-effect transistor 2.2.16
Floating voltage 2.4.2
Forward direction (of a PN junction) 2.3.3

G

Grown junction 2.1.10

H

Hall coefficient (of a semiconductor) 2.1.24
Hall constant 2.1.24
Hall effect 2.1.23

I

Impedance, transient thermal 2.4.9
Impedance under pulse conditions, thermal 2.4.10

UDK 621.3:(53+54+621+66),ISSN0352-9045 Informacije MIDEM 23(1993)1,Ljubljana

R.Ročak: Sodelovanje društva MIDEM s sorodnimi društvi	2	R.Ročak: Collaboration of Society MIDEM with similar Societies
ZNANSTVENO STROKOVNI PRISPEVKI		PROFESSIONAL SCIENTIFIC PAPERS
Zvonko Fazarinc: Efekti drugega reda v bipolarnih tranzistorjih	3	Zvonko Fazarinc: Second Order Effects in Junction Bipolar Transistors
D.Resnik, U.Aljančič, D.Vrtačnik, S.Amon: Gladkost anizotropno jedkane površine (100) silicija	10	D.Resnik, U.Aljančič, D.Vrtačnik, S.Amon: Surface Smoothness of Anisotropically Etched (100) Silicon
A.Zalar, F.Pimentel, S.Hofman, D.Kohl, P.Panjan, B.Praček: Študij termične tvorbe silicidov v večplastni strukturi Ni/Cr/Si	17	A.Zalar, F.Pimentel, S.Hofman, D.Kohl, P.Panjan, B.Praček: A Study of Thermally Formed Silicides in a Ni/Cr/Si Multilayer Structure
A.Živić, Z.Živić: Rdeča feritna tehnologija - sanje ali resničnost	21	A.Živić, Z.Živić: Red Ferrite Technology - Dream or Reality
L.Koller, M.Jenko, E.Perman: Korozijska obstojnost vakuumsko kromanega železa za miniaturne hermetične releje	27	L.Koller, M.Jenko, E.Perman: Corrosion Resistance of Vacuum Chromized Iron Parts for Hermetical Relays
M.Valant, D.Suvorov, D.Kolar: Mikrovalovni keramični materiali	32	M.Valant, D.Suvorov, D.Kolar: Microwave Ceramic Materials
J.Pirš, B.Marin, S.Pirš: Prikazovalnik na osnovi feroelektričnih tekočih kristalov in polimernih gelov	38	J.Pirš, B.Marin, S.Pirš: Ferroelectric Liquid Cristal-polymer gel Displays
Janez Benda: Metaloksidni (ZnO) varistorji	43	Janez Benda: Metal Oxide (ZnO) Varistors
PRIKAZI DOGODKOV, DEJAVNOSTI ČLANOV MIDEM IN DRUGIH INSTITUCIJ		REPRESENT OF EVENTS, ACTIVITIES OF MIDEM MEMBERS AND OTHER INSTI TUTIONS
Miloš Kogovšek: Industrijska lastnina	50	Miloš Kogovšek: Industrial Ownership
Marija Trontelj: Nacionalni center za mikrostrukturno in površinsko analizo	52	Marija Trontelj: National Center for Microstructural and Surface Analysis
Zlatko Bele: Testni center MIKROIKS	53	Zlatko Bele: MIKROIKS Test Center
KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA		CONFERENCES, COLLOQUYUMS, SEMINARS, REPORTS
M.Kosec: ICECM '92	56	M.Kosec: ICECM'92
M.Hrovat: Konferenca MICROTECH'93	57	M.Hrovat: MICROTECH'93 Conference
PREDSTAVLJAMO PODJETJE Z NASLOVNICE		REPRESENT OF COMPANY FROM FRONT PAGE
SIQ - Slovenski institut za kakovost in meroslovje	61	SIQ - Slovenian Institute of Quality and Metrology
Prikazi magistrskih del, leto 1992	65	Ms. Abstracts, Year 1992
VESTI	71	NEWS
Vabilo za sodelovanje, MIEL-SD 93	76	Announcement and Call for Papers, MIEL-SD 93
TERMINOLOŠKI STANDARDI	79	TERMINOLOGICAL STANDARDS
MIDEM prijavnica		MIDEM Registration Form
Slika na naslovnici: Slovenski institut za kakovost in meroslovje - Detalj preskusa zdržljivosti zagonskih kondenzatorjev		Front page: Slovenian Institute of Quality and Metrology - Detail of Endurance Test of a.c. Motor Capacitors

UDK 621.3:(53+54+621+66),ISSN0352-9045 Informacije MIDEM 23(1993)2,Ljubljana

R. Ročak: Zaostreni kriteriji ali zmanjšanje državnih sredstev za razvoj	94	R. Ročak: Restrictive Criteria or Reduction of State Means for Development
ZNANSTVENO STROKOVNI PRISPEVKI		PROFESSIONAL SCIENTIFIC PAPERS
S. Smedley: Načrtovanje BiCMOS vezij z uporabo lateralnih pnp bipolarnih tranzistorjev. Model in nekaj primerov uporabe	95	S. Smedley: BiCMOS Circuit Design Using the Lateral PNP. A Model and some Circuit Applications
S. Starašinič, J. Trontelj: Šumne lastnosti vezij SC	99	S. Starašinič, J. Trontelj: Noise Behavior of SC Circuits
P. Jamnik: Iskrin elektronski števec energije: Enočipni merilni modul na osnovi Hallovega efekta	104	P. Jamnik: The Iskra Solid State Energy Meters: A single chip measuring module based on the integrated Hall effect sensor
R. Osredkar: Postopki planarizacije s centrifugalnim nanašanjem siloksanskih stekel	107	R. Osredkar: Spin-on-glass Planarization of Device Topography
M. Mozetič, M. Kveder, A. Pregelj, A. Paulin: Vodikova plazma	112	M. Mozetič, M. Kveder, A. Pregelj, A. Paulin: Hydrogen Plasma

VSEBINA LETNIKA 1993 CONTENT - VOLUME 1993

I. Belič, L.I. Belič: Visokotemperaturna metalizacije, model za izračun zrn keramike in integranularnega volumna med zrni keramike	117	I. Belič, L.I. Belič: High Temperature Metallization. Alumina Grains and Intergranular Volume Modelling
J. Ficzko, A. Dobnikar: Logične nevronske mreže za problem razpoznavanja znakov	123	J. Ficzko, A. Dobnikar: Logical Neural Networks for a Character Recognition Problem
UPORABA POLPREVODNIŠKIH IN MIKROELEKTRONSKIH KOMPONENT		APPLICATION OF SEMICONDUCTOR AND MICROELECTRONIC COMPONENTS
J. Žmavc: Identifikacijska kartica	128	J. Žmavc: Identification Card
Hitre in ultrahitre diode iz programa Iskre SEMICON	130	Fast and Ultrafast Diodes from Iskra SEMICON
PRIKAZI DOGODKOV, DEJAVNOSTI ČLANOV MIDEM IN DRUGIH INSTITUCIJ		REPRESENT OF EVENTS, ACTIVITIES OF MIDEM MEMBERS AND OTHER INSTITUTIONS
T. Tekavec: Osnovna pravila mednarodnega sistema ocenjene kakovosti elektronskih elementov (IECQ)	132	T. Tekavec: IECQ System
R. Ročak: Znanstveno raziskovalni projekti iz polja ELEKTRONSKE KOMPONENTE IN TEHNOLOGIJE v Sloveniji za leto 1993	137	R. Ročak: Scientific Projects in Slovenia for year 1993, Research Field ELECTRONIC COMPONENTS AND TECHNOLOGIES
D. Križaj: Pismo iz Toulousa		D. Križaj: La Lettre de Toulouse
KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA		CONFERENCES, COLLOQUYUMS, SEMINARS, REPORTS
D. Vrtačnik: SEMICON EUROPA '93	139	D. Vrtačnik: SEMICON EUROPA '93
PREDSTAVLJAMO PODJETJE Z NASLOVNICE		REPRESENT OF COMPANY FROM FRONT PAGE
Laboratorij za mikroelektroniko na Fakulteti za elektrotehniko in računalništvo v Ljubljani	140	Laboratory for Microelectronics on Faculty of Electrical and Computer Engineering in Ljubljana
PRIKAZI DOKTORATOV, LETO 1992	141	PhD ABSTRACTS, YEAR 1992
VESTI	146	NEWS
TERMINOLOŠKI STANDARDI	157	TERMINOLOGICAL STANDARDS
MIDEM prijavnica	163	MIDEM Registration Form
Slika na naslovnici: Laboratorij za mikroelektroniko na Fakulteti za elektrotehniko in računalništvo v Ljubljani: Integrirano vezje za miniaturni celični telefon		Front page: Laboratory for Microelectronics on Faculty of Electrical and Computer Engineering in Ljubljana: ASIC for miniature cellular telephone

UDK621.3:(53+54+621+66),ISSN0352-9045 Informacije MIDEM 23(1993)3,Ljubljana

R.Ročak: Kriza na Vzhodu, ozdravljenje na Zahodu	172	R.Ročak: Crises in the East, Recovery in the West
ZNANSTVENO STROKOVNI PRISPEVKI		PROFESSIONAL SCIENTIFIC PAPERS
Z.Fazarinc: Algoritmi za večdimenzionalno računalniško analizo polprevodnikov iz osnovnih fizikalnih principov	173	Z.Fazarinc: Algorithms for Multi-dimensional Analysis of Semiconductors Derived from First Principles
R.Osredkar: Termična obdelava poliimidnih umetnih smol za uporabo v mikroelektronskih tehnologijah	183	R.Osredkar: Polyimide Resin Curing in Microelectronic Applications
A.Žnidaršič: Nova generacija Mn-Zn feritov za močnostne aplikacije	186	A.Žnidaršič: A New Generation Mn-Zn Ferrites for Power Applications
M.Jenko: Raziskave segregacije antimona na površini neorientirane elektro pločevine z metodo AES	190	M.Jenko: AES Investigation of Surface Segregation of Antimony in Non Oriented Electrical Sheets
D.Donlagić, J.Koprivnikar, V.Matko: Princip senzorjev na osnovi oscilatorske diferencialne strukture	196	D.Donlagić, J.Koprivnikar, V.Matko: Differential Ocsillator Sensors
J.Skvarč: Avtomatski sistem za analizo slike TRACOS	201	J.Skvarč: Automatic Image Analysis System TRACOS
D.Gradišnik, D.Đonlagić: Laserski merilnik debeline s statistično obdelavo rezultatov	206	D.Gradišnik, D.Donlagić: Laser Thickness Measurer with Statistical Processing of Measurement
UPORABA POLPREVODNIŠKIH IN MIKROELEKTRONSKIH KOMPONENT		APPLICATION OF SEMICONDUCTOR AND MICROELECTRONIC COMPONENTS
C.Heberling: ASICs - kako izbrati optimalno rešitev	212	C.Heberling: ASICs - Selecting the Optimum Solution
J.Varl, J.Žmavc: Elektronsko vezje za mini časovni števec	214	J.Varl, J.Žmavc: ASIC for Mini Timer
Supresorske diode iz programa Iskre SEMICON	215	Suppressor and Limiter Diodes from Iskra SEMICON
KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA		CONFERENCES, COLLOQUYUMS, SEMINARS, REPORTS
A.Pregelj: Tečaj osnove vakuumske tehnike	220	A.Pregelj: Seminar on Basic Vacuum Technology
A.Pregelj: Prvo srečanje vakuumistov Slovenije in Hrvaške	220	A.Pregelj: First Meeting of Slovene and Croat Vacuum Societies

VSEBINA LETNIKA 1993 CONTENT - VOLUME 1993

PREDSTAVLJAMO PODJETJE Z NASLOVNICE		REPRESENT OF COMPANY FROM FRONT PAGE
Austria Mikrosysteme International	220	Austria Mikrosysteme International
VESTI	222	NEWS
TERMINOLOŠKI STANDARDI	229	TERMINOLOGICAL STANDARDS
MIDEM prijavnica	235	MIDEM Registration Form
Slika na naslovnici: "Integrirana vezja po naročilu za ves svet". Austria Mikro Systeme International GmbH, AMS, je firma, ki se je specializirala za razvoj in proizvodnjo integriranih vezij po naročilu (ASIC) in standardnih integriranih vezij za specifično uporabo (ASSP). Firma zaseda posebej močan položaj na trgu vezij za telekomunikacije, avtoelektronike in industrijske elektronike.		Front page : "ASICs for the World". Austria Mikro Systeme International GmbH, AMS, specializes in the development and production of application specific integrated circuits (ASICs) and application specific standard products (ASSPs). The company is in a strong position within the market segments telecommunications, automotive and industrial electronics.

UDK621.3:(53+54+621+66),ISSN0352-9045

Informacije MIDEM 23(1993)4,Ljubljana

I.Šorli: Društvo MIDEM in njegove dejavnosti	244	I. Šorli: MIDEM Society and its Activities
ZNANSTVENO STROKOVNI PRISPEVKI		PROFESSIONAL SCIENTIFIC PAPERS
MIEL-SD 93 VABLJENA PREDAVANJA		MIEL-SD 93 INVITED PAPERS
M.B.Johnson, H.W.M.Salemink: Rasterska tunelska mikroskopija presekov heteroslojnih polprevodnikov: Atomska ločljivost, sestava, fluktuacije in dopiranje	245	M.B.Johnson, H.W.M.Salemink: Cross-Sectional Scanning Tunneling Microscopy on Heterostructures: Atomic Resolution, Composition, Fluctuations and Doping
C.Cini: Mešana bipolarna - CMOS - DMOS tehnologija za pametna močnostna integrirana vezja	253	C.Cini: Mixed Bipolar-CMOS-DMOS Smart Power IC Technology
J.Furlan, W.Kusian, G.Conte: Tandemske amorfne silicijeve sončne celice	259	J.Furlan, W.Kusian, G.Conte: Tandem Amorphous Silicon Solar Cells
A.J.Williams, I.R.Harris: Magneti kovin prehoda in redkih zemelj: proizvodnja, lastnosti in uporaba	264	A.J.Williams, I.R.Harris: Rare Earth-Transition Metal Magnets: Their Processing, Properties and Applications
J.W.Ciognani, E.Gramegna, M.Wiegand: Pregled trenutnega stanja razvoja keramične in poliimidne tehnologije za multičip module	272	J.W.Ciognani, E.Gramegna, M.Wiegand: An Overview of Recent Developments in Ceramic and Polyimide Technologies for Multichip Modules
M.Maček: Pregled sodobnih postopkov mokrega čiščenja silicijevih rezin	275	M.Maček: A Review of Advanced Wet Cleaning
UPORABA POLPREVODNIŠKIH IN MIKROELEKTRONSKIH KOMPONENT		APPLICATION OF SEMICONDUCTOR AND MICROELECTRONIC COMPONENTS
J.Novak: Mikroelektronika v službi natančnega merjenja pomikov in zasukov. Integrirano vezje RLX 12510	284	J.Novak: Use of Microlectronic Technology for Exact Position and Shaft Measurements. RLX 12510 Integrated Circuit
KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA		CONFERENCES, COLLOQUYUMS, SEMINARS, REPORTS
M.Slokan, I.Šorli: 21.Mednarodna konferenca o mikroelektroniki, MIEL'93 in 29.Simpozij o elektronskih sestavnih delih in materialih, SD'93, 29.09. - 01.10.1993, Bled, Slovenija	285	M.Slokan, I.Šorli: 21st International Conference on Microelectronics, MIEL'93 and 29th Symposium on Devices and Materials, SD'93, 29.09. - 01.10.1993, Bled, Slovenia
ESSDERC 93	288	ESSDERC 93
D.Križaj: EPE - 5.evropska konferenca o močnostni elektroniki in njeni uporabi	289	D.Križaj: EPE - 5.th European Conference on Power Electronics and Applications
A.Zalar: ECASIA 93 - 5.evropska konferenca o uporabi metod za analizo površin in faznih meja	290	A.Zalar: ECASIA 93 - 5.th European Conference on Application for Surface and Interface Analysis
A.Cvelbar: ICTF 9 - 9.mednarodna konferenca o tankih plasteh	292	A.Cvelbar: ICTF 9 - 9th International Conference on Thin Films
A.Pregelj: 44.posvetovanje o metalurgiji in kovinskih gradivih ter 1. posvetovanje o materialih	293	A.Pregelj: 44th Symposium on Metallurgy and Metal Compounds and 1st Symposium on Materials
PREDSTAVLJAMO PODJETJE Z NASLOVNICE		REPRESENT OF COMPANY FROM FRONT PAGE
CMP servis	294	CMP Service
VESTI	301	NEWS
KOLEDAR PRIREDITEV	309	CALENDAR OF EVENTS
TERMINOLOŠKI STANDARDI	310	TERMINOLOGICAL STANDARDS
MIDEM prijavnica	315	MIDEM Registration Form
VSEBINA LETNIKA 1993	318	CONTENT - VOLUME 1993
Slika na naslovnici: CMP - Multičip servis; GaAs rezina z digitalnimi integriranimi vezji z minimalno razsežnostjo 0.8 μm izdelano v firmi TCS		Front page: CMP - Multi-Projets Circuits; 0.8 μm digital GaAs wafer from TCS

VSEBINA LETNIKA 1993 — CONTENT - VOLUME 1993

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UGODNA PONUDBA RABLJENE OPREME IN KEMIKALIJ

Po zelo ugodni ceni in pod ugodnimi pogoji nudimo naslednjo rabljeno opremo:

1. *Pe za temperaturno obdelavo vzorcev, Tempress M280*
2. *Kemino odporna jedkalna postaja z enim koritom, MicroAir*
3. *Delovna postaja z laminarnim pretokom zraka, 4", 6" in 8", MicroAir*
4. *Sistem za temperaturno staranje integriranih vezij, Marin Controls, System 25*
5. *Naparjevalnik za zlato in aluminij na silicijevih rezinah, MIPOT*
6. *Merilnik TOC (Total Organic Carbon) v vodi, Anatel A-100P*
7. *Elipsometer, Rudolph AutoEL III*
8. *Detektor vodika z ustrezno elektroniko in sondami, Auer*
9. *Avtomatski detektor arsina in fosfina, Matheson M8040*
11. *Roni detektor strupenih plinov, Dr(ger*
12. *572 Bayard Alpert Ionization Gauge*
13. *Avtomatski in roni poravnalnik rezin (FLAT FINDER), H_2CO*
14. *istilnik plinov, Matheson 460 z vloki*
15. *Merilnik upornosti vode s sondo, Balsbaugh 900*
16. *Kemikalije in plini po seznamu*

V kolikor se zanimate za katerega od natetih izdelkov nas, prosim, pokliite!!!