UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 3 ◦1994

Strokovno društvo za mikroelektroniko elektronske sestavne dele in materiale

Časopis za mikroelektroniko, elektronske sestavne dele in materiale
Časopis za mikroelektroniku, elektronske sastavne dijelove i materijale
Journal of Microelectronics, Electronic Components and Materials

INFORMACIJE MIDEM, LETNIK 24, ŠT. 3(71), LJUBLJANA, september 1994

INFORMACIJE MIDEM 3 ° 1994

INFORMACIJE MIDEM	LETNIK 24, ŠT. 3(71), LJUBLJANA,	SEPTEMBER 1994
INFORMACIJE MIDEM	GODINA 24, BR. 3(71), LJUBLJANA,	SEPTEMBAR 1994
INFORMACIJE MIDEM	VOLUME 24, NO. 3(71), LJUBLJANA,	SEPTEMBER 1994

Izdaja trimesečno (marec, junij, september, december) Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale.
Izdaja tromjesečno (mart, jun, septembar, decembar) Stručno društvo za mikroelektroniku, elektronske sastavne dijelove i materiale.
Published quarterly (march, june, september, december) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Glavni in odgovorni urednik
Glavni i odgovorni urednik
Editor in Chief
mag. Iztok Šorli, dipl.ing.,
MIKROIKS d.o.o., Ljubljana

Tehnični urednik
Tehnički urednik
Executive Editor
Janko Colnar,
MIDEM, Ljubljana

Uredniški odbor
Redakcioni odbor
Executive Editorial Board
Doc. dr. Rudi Babič, dipl.ing., Tehniška fakulteta Maribor
Dr.Rudi Ročak, dipl.ing., MIKROIKS d.o.o., Ljubljana
mag.Milan Slokan, dipl.ing., MIDEM, Ljubljana
Zlatko Bele, dipl.ing., MIKROIKS d.o.o., Ljubljana
Miroslav Turina, dipl.ing., Zagreb
mag. Meta Limpel, dipl.ing., MIDEM, Ljubljana
Miloš Kogovšek, dipl.ing., Iskra INDOK d.o.o., Ljubljana

Časopisni svet
Izdavački savet
International Advisory Board
Prof. dr. Slavko Amon, dipl.ing., Fakulteta za elektrotehniko in računalništvo, Ljubljana, PREDSEDNIK
Dr. Jean-Marie Haussonne, C.N.E.T. Centre LAB, Lannion
Dr. Marko Hrovat, dipl.ing., Inštitut Jožef Stefan, Ljubljana
Prof. dr. Zvonko Fazarinc, dipl.ing., CIS, Stanford University, Stanford, USA
Dr. Marija Kosec, dipl.ing., Inštitut Jožef Stefan, Ljubljana
Prof.dr.Drago Kolar, dipl.ing., Inštitut Jožef Stefan, Ljubljana
RNDr. DrSc. Radomir Kužel, Charles University, Prague
Dr. Giorgio Randone, ITALEL S.I.T. spa, Milano
Prof.dr. Stane Pejovnik, dipl.ing., Kemijski inštitut Boris Kidrič, Ljubljana
Dr. Wolfgang Pribyl, SIEMENS EZM, Villach, Österreich
Dr. Giovanni Soncini, University of Trento, Trento
Prof.dr. Janez Trontelj, dipl.ing., Fakulteta za elektrotehniko in računalništvo, Ljubljana
Dr. Anton Zalar, dipl.ing., IEVT, Ljubljana
Dr. Peter Weissglas, Swedish Institute of Microelectronics, Stockholm

Naslov uredništva
Adresa redakcije
Headquarters
Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 61000 Ljubljana, Slovenija
(0)61 - 316 886

Letna naročnina znaša 7000,00 SIT, cena posamezne številke je 1750,00 SIT. Člani in sponzorji MIDEM prejemajo Informacije MIDEM brezplačno.
Godišnja pretplata iznosi 7000,00 SIT, cijena pojedinog broja je 1750,00 SIT. Članovi i sponzori MIDEM primaju Informacije MIDEM besplatno.
Annual subscription rate is DEM 100, separate issue is DEM 25. MIDEM members and Society sponsors receive Informacije MIDEM for free.

Znanstveni svet za tehnične vede l je podal pozitivno mnenje o časopisu kot znanstveno strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinanci rajo Ministrstvo za znanost in tehnologijo in sponzorji društva.
Scientific Council for Technical Sciences of Slovene Ministry of Science and Technology has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials.
Publishing of the Journal is financed by Slovene Ministry of Science and Technology and by Society sponsors.

Znanstveno strokovne prispevke objavljene v Informacijah MIDEM zajemamo v:
* domačo bazo podatkov ISKRA SAIDC-el, kakor tudi
* v tujo bazo podatkov INSPEC
Scientific and professional papers published in Informacije MIDEM are assessed into:
* domestic data base ISKRA SAIDC-el and
* foreign data base INSPEC

Po mnenju Ministrstva za informiranje št.23/300-92 šteje glasilo Informacije MIDEM med proizvode informativnega značaja, za katere se plačuje davek od prometa proizvodov po stopnji 5 %.

Grafična priprava in tisk
Grafička priprema i štampa
Printed by
BIRO M, Ljubljana

Naklada
Tiraž
Circulation
1000 izvodov
1000 primjeraka
1000 issues

UDK621.3:(53+54+621+66),ISSN0352-9045 Informacije MIDEM 24(1994)3,Ljubljana

VSEBINA CONTENT

ABOUT STATE STIMULATIONS OF R&D IN SLOVENIA

In the last issue of the Journal the data on Slovenian state stimulation for the study of young researchers was published. Ministry for Science and Technology of Republic Slovenia is financing also other aspects of R&D activities in Slovenia.

First of all Ministry is financing completely the fundamental research and the public scientific and research institutes. To the research institutes Ministry is paying 75% of the cost of a R&D project which is ordered by at least two companies or if the research is performed by a mixed group composed of researchers from an institute and research department of a company at maximum 50% relation, 50% of the project cost for the projects ordered by a company if this company guaranties the transfer of the project result in the industrial application.

Ministry is covering 50% of an R&D project cost to a company in the case of a research group with researchers from two different companies and 25% if the researchers are from only one company. For hired researchers the Ministry covers 50% of the labour cost for these researchers.

50% of the interests for the bank loans for R&D equipment and infrastructural investments are also subject of Ministry stimulation. A company can get 50% of labour cost for a new Phd applicant in the company for the first year of employment, and 25% for the second year.

Ministry is willing also to finance a part of cost for technology centres or parks.

In spite of all goodwill of the Ministry there is a question if enough money for the need of Slovenian R&D is available. In any case the actual experience of the applicants for the state stimulation in Slovenia shows that any bigger industrial project can expect drastically financial reduction by a lack of financial 7 possibilities.

Great surprise in the R&D area was caused by the Slovenian Ministry of Finance. This Ministry interprets the R&D activity as a technical service with a 5% tax on income (financing). So, the money given by the Ministry of Science and Technology is in 5% value immediately taken by the tax office. Although logic for state income this is an absurd. All proclamations of state incentives for R&D expenses of a company are false. In the balance tax declaration the company can detract the R&D expenses but in this case this can not be accounted for as company's outcome, on the other hand it can not be detracted.

And what is the sense of such tax stimulation? It will be interesting to learn something on this subject from other countries. I am asking our members from abroad to give a comment or their experience on the subject.

MIDEM Society President
Dr. Rudolf Ročak

UDK 621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 24(1994)3, Ljubljana

GLASS ON SILICON TECHNOLOGY FOR OPTICAL INTERCONNECTIONS AND OPTOELECTRONIC HYBRID INTEGRATION

A. Fincato, S. Lorenzotti, P. Nugent,G. Parafioriti and G. Randone,
Italtel, Central Research Laboratories
Castelletto di Settimo Milanese, Milano, Italy

Key words: optoelectronics, glass on silicon, optical interconnections, optoelectronic integrations, hybrid integrations, optical communications, optical telecommunications, information processing, optical guides, self aligning procedures, cost reduction

Abstract: Optoelectronic integration has been widely recognised as a very important step to further increase the competitiveness of optical technologies in communication and information processing. Despite the impressive development effort on a monolithic technology, based on semiconductor InP and GaAs substrates, which has been carried out until now with quite promising feasibility results, it is still quite far in its present implementation from being suitable for economic product development. Therefore, a less ambitious target may be set by choosing an hybrid approach, where optical interconnects can be realised on a specific substrate and active components (Lasers and PINs) are mounted on this substrate by a die attach process, eventually aligned to the optical guides with self aligning procedures. The Glass on Silicon technology developed by Italtel, which will be described in this paper, is an example of this approach, and could be applied very quickly to the development of specific components and modules for optical telecommunications system, with many clear advantages in terms of cost reduction and mass production capability, with the support of very efficient CAD tools for the design of complex, multifunctional optical subassemblies[1]

Tehnologija stekla na silicijevem substratu za izvedbo optinih povezav in optoelektronske hibridne integracije

Ključne besede: optoelektronika, steklo na siliciju, povezave optične, integracije optoelektronske, integracije hibridne, komunikacije optične, telekomunikacije optične, procesiranje informacij, vodi optični, procedure samonastavljive, zmanjšanje stroškov

Povzetek: Veliko ljudi že priznava optoelektronsko integracijo kot zelo pomemben korak k povečanju konkurenčnosti optičnih tehnologij v komunikacijah in obdelavi informacij. Navkljub prepričljivemu razvoju monolitne tehnologije na osnovi polprevodniških InP in GaAs substratov, ki je potekal do sedaj z obetajočim uspehom, je le-ta na sedanji stopnji razvoja že dokaj daleč od tega, da bi bila primerna za razvoj ekonomičnega proizvoda. To pomeni, da si v tem trenutku lahko zastavimo manj ambiciozen cilj, to je hibridni pristop, kjer optične povezave izdelamo na specifičnem substratu, dodamo pa aktivne komponente (laserje in PIN diode) v čip obliki, ki jih pritrdimo na ta substrat in poravnamo z optičnimi vodniki s samonastavljivimi poravnalnimi postopki. Tehnologija stekla na siliciju, ki jo je razvila firma ITALTEL, in ki jo opisujemo v tem prispevku, je primer takega hibridnega pristopa. To tehnologijo lahko hitro uporabimo za razvoj specifičnih komponent in modulov za optične telekomunikacijske sisteme z jasnimi prednostmi glede zmanjševanja stroškov in možnosti velikoserijske proizvodnje ob uporabi zmogljivih CAD orodij za načrtovanje zamotanih večfunkcijskih optičnih podsestavov.

1. INTRODUCTION

Packaging and assembly processes still make up a large part of the manufacturing cost in the fabrication of optoelectronic components and subsystems. Besides high cost, which is limiting the penetration of optical fibres in the distribution network, available technologies do not efficiently support the batch fabrication of complex optical interconnection schemes, which are increasingly needed for optical switching and multiwavelength networks in order to become practical applications. Monolithic integrated optics has been considered for a long time a main research and development road to overcome these difficulties, by considering the analogy with the microelectronics case. Unfortunately, until now, encouraging results are still largely confined to laboratory feasibility, due to the intrinsic complexity and low yields of the required technologies, which put the economic convenience of the huge investments needed to implement a true high volume manufacturing capability for optical integrated circuits somewhat at risk. Even from a conceptual point of view, it became clear that a fundamental difference exists between integrated optics and electronic integrated circuits: for a VLSI chip only one basic building block is required (a silicon transistor), which relies on a well known and mature substrate technology; instead, the substrate for an integrated optic device may be chosen from a large variety of options (GaAs, InP, Silicon, glass, $LiNbO_3$, to mention the most popular choices), and the building blocks may include light sources and photodetectors, optical waveguides,

[1] This paper is the second of a series, which will be presented in MIDEM during 1994, concernig advanced topics in optical technologies and systems. The first contribution has been devoted to optical amplifiers and the last one will discuss a specific application to multiwavelength transport networks

passive optical components and light modulators, each one realised with a specific design and technology, generally with very limited, or none at all, mutual process compatibility. Therefore, apart from a very limited number of cases (the PIN photodetector with integrated FET preamplifier, for instance), the performance of integrated optoelectronic devices is generally worse than their discrete assembled equivalent version. In fact, elementary optical functions integrated on a monolithic chip are far less optimised due to process compatibility reasons, with respect to the same functional result achieved with discrete devices.

By considering the above aspects, a more realistic and practical approach than monolithic integrated optics may be based on the choice of a substrate material optimised for optical passive waveguide fabrication, on which discrete active optoelectronic devices may be mounted by a suitable hybrid assembly procedure and easily selected for a specific application. In our case, a silica layer deposited on a silicon substrate by a chemical vapour deposition technique was selected for waveguide formation; on the same silicon substrate, well known dry and wet etching, dielectric and metallic thin films deposition processes and photolithography can be used for waveguide patterning and metallic mounting pads formation. The final result is an hybrid assembly platform, suitable for a large variety of optical and electrical interconnection schemes and micromechanical alignment for efficient optical coupling, which could give to the photonic applications the same flexibility in product development, which was allowed by the introduction in the electronic design and manufacturing by the well known printed circuit board.

The Glass on Silicon technology (GoS), which will be described in the following, has been developed by Italtel in cooperation with AT&T-Bell Laboratories, during a two years joint development agreement which has been just terminated in June 1994. In the framework of this agreement, Italtel holds a full manufacturing license for products based on the glass on silicon process technology, including those processes which were originally developed by AT&T alone. Most of the work described in this paper has been carried out by a joint team from ATT and Italtel, in the ATT- Microelectronic and Bell Laboratories research facilities, in Breinigsville (PA) and Murray Hill (NJ).

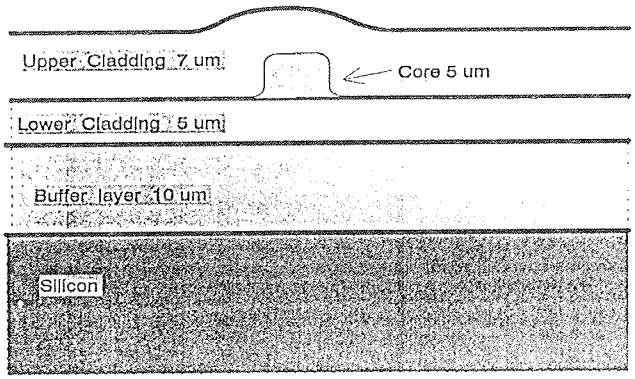


Fig. 1: *Cross-section of silica waveguide grown on Silicon substrate*

2. GLASS ON SILICON TECHNOLOGY

2.1 Waveguide deposition

A typical waveguide structure is formed on a 4" silicon substrate 0.5 mm thick; a 10 μm thick SiO_2 buffer layer is deposited first, by an high pressure oxidation process (High Pressure Oxidation, HIPOX), to avoid any optical leakage into the silicon substrate. The first cladding layer of the planar waveguide (5μm, P doped SiO_2) is deposited next, by a low pressure chemical vapour deposition, followed by a 1000°C annealing for densification and to remove the residual stress in the layer. The core waveguide layer (5μm) is then deposited by a similar process; the required refractive index for the core layer is controlled by varying the Phosphor doping and the deposition temperature. The silicon wafer is then processed through a photolithography and a dry etching process for two dimension rectangular waveguide patterning, followed by a 900°C annealing which rounds the waveguide corners and improves the layer optical characteristics. Finally, an upper cladding layer is deposited, which completes the waveguide structure (Fig. 1)

The waveguide shape is roughly a semi-circle, with a 5μm diameter; the refraction index step is of the order of 0.5 %, and intrinsic losses as low as 0.01 dB/cm have been measured; other typical waveguide parameters are reported in Table 1.

Table 1: Glass on Silicon waveguide parameters

index of refraction step, Δn/n (%)	0.5
core size diameter (μm)	5
waveguide loss (dB/cm)	0.03
fiber coupling loss (dB)	0.1
bend radius (mm)	15
coupler excess loss (dB)	0.2
Coupling length (mm)	2 ± 0.3

2.2 Wafer processing and micromachining

In addition to the waveguide fabrication, other wafer processes have been developed, in order to obtain a number of basic building blocks for a flexible implementation of complex functionalities. Most of these processes are readily available with little or no modifications from silicon microelectronics technology, and can be implemented on high throughput processing machines. In particular, current development work is under way on 4" silicon wafers, but all the machinery is already equipped with jig adapters suitable for handling 6" wafers. In addition to the already mentioned CVD process,

which will use two 4-stack BTU furnaces for doped SiO_2 and polysilicon deposition, standard processing facilities include Reactive Ion Etching, Plasma Enhanced CVD, for thick and low temperature oxide deposition, dielectric and metal thin film sputtering and metal deposition equipment.

Micromachining of the silicon substrate by using selective and anisotropic wet etching allows to reach submicron fabrication tolerances for the creation of 3D features on the substrate (steps, recesses, holes and V-grooves for instance), which may be used as mechanical references for self- alignment of various optical components (lasers, photodetectors and optical fibres) with the waveguides grown on the substrate. A few simple results already achieved in this area will be described below, as a good example of the potential of this process technology. It should be noted that, since the etching depth generally required for these applications is an order of magnitude larger than in the microelectronic case, little or no help is available from established specific silicon technology, and therefore new process development has been carried out.

2.3 Packaging

Packaging issues have always been a critical factor in optical and optoelectronics devices development, in particular with respect to cost targets and volume production capability. Therefore, an important long term objective for the GoS technology is to achieve complete automation in the assembly and packaging procedures, in particular without any need for active alignment for optical coupling; as a necessary condition for high production volume and low manufacturing cost. While substantial development work is still required to achieve this goal, some guidelines have already been established and tested with an encouraging degree of success; in particular:

1. a batch procedure has been defined, by a selective metallisation scheme, which allows the self-positioning of a semiconductor chip (Laser or photodetector) on the silicon substrate during the die attach, with better than 1 μm tolerance in position and less than 10 mrad misalignment of the chip edge with respect to a selected direction, starting with a relatively loose tolerance of the initial placing (20- 30μm in position, and 20° - 30° degree for the chip edge)

2. a quite complex procedure has been developed to etch a 45° degree mirror for vertical extraction of optical radiation from planar waveguides; in combination with the above process 1., then it has been possible to self-align a PIN photodetector directly with the waveguides by a batch process at the wafer level, as a good example of a truly hybrid optical integration.

3. a simple and economic lid cover technology has been developed to fabricate by etching specific recesses in Silicon to be placed in correspondance with chip positions on the substrate. The lid cover is then mounted in place by a selective die attach process on the hybrid optical circuit to achieve an high optical and electrical crosstalk immunity. The lid also allows for an hermetic seal of active devices and reduces outside electromagnetic interference. Moreover, most of the remaining work on the hybrid circuit (the fiber attachement for instance) can be carried out with delicate components on the circuit well protected and safeguarded, in such a way as to achieve high yield in testing and packaging operations.

4. the use of a plastic housing, allowed in conjunction with the hermetic silicon lid, as a final package, may further reduce the cost and increase the possibility of using different standard packages while mantaining the quality and reliability level mandatory for telecommunication applications.

The above mentioned steps clearly indicate that the glass on silicon technology holds the potential for achieving a breakthrough in optoelectronic assembly and packaging technologies; in particular, the intrinsic high yield batch process technology could be used to obtain a very low cost high volume production capability for simple devices (A packaged laser or photodetector), or to achieve an industrial standard for manufacturing complex multifunctional optoelectronic modules, with high yield and reasonable cost. A simple sketch of the potential described above is illustrated in fig. 2, which refers to a bidirectional optical transceiver, capable of using two carrier wavelengths for sending and receiving data signals simultaneously on the same optical fibre; all the functions described in fig.2, with the exception of the integral mounting of the laser source, are already available as engineered building blocks for the implementation of GoS hybrid integrated optic devices.

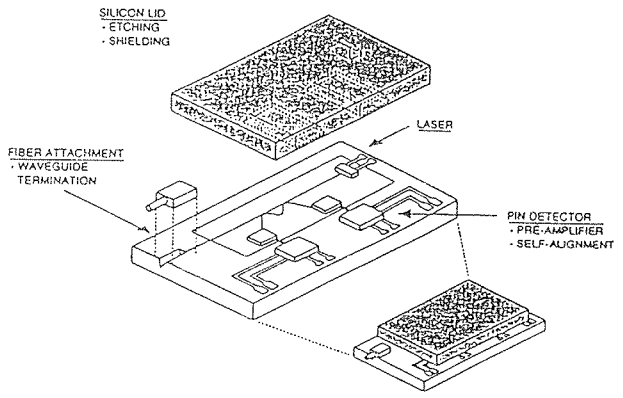


Fig. 2: Example of a Glass on Silicon integrated optoelectronic module

3. PASSIVE COMPONENTS DESIGN

Key functions in integrated optic devices are supported by passive optical components; in fig. 2 for instance the wavelength demultiplexing function, by which the incoming wavelength is sent to the photodetector, is implemented by the use of a planar waveguide structure well known in classical optics as a Mach-Zehnder interferometer. Complex passive components may be realised starting from several elementary optical elements: the straight and curved waveguide are the simplest examples of elementary passive optical component together with 3 db Y couplers and splitters. It should be noted that the bending radius of a curved waveguide is a critical design parameter [1,2], since (for a fixed refractive index step between core and cladding in the waveguide) the radiation losses increase exponentially with decreasing bend radius. Therefore a compromise should be found between the optical circuit dimensions and the acceptable radiation losses; in our case, a bend radius of 15 mm is sufficient to keep radiation losses below 0.1 dB/cm. An important development issue therefore is how to increase the refractive index step in the guiding structure. Typical measured losses as a function of the bending radius for a curved waveguide are reported in fig.3, and the advantage of a higher index step may be clearly seen.

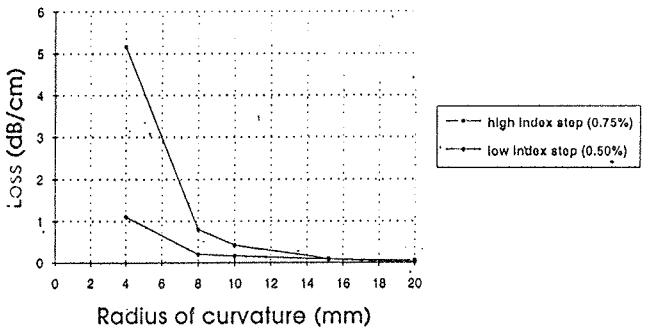


Fig. 3: Bend losses of curved waveguides measured at the 1550 nm wavelength (TM mode)

Even with simple elements it is possible to design quite complex optical interconnection schemes, which may offer relevant advantages in terms of quick design, simple manufacturing, reliable operation and very low cost. An example is shown in fig 4, which illustrates a 2 X 4 splitter for four fibre ribbon cable, designed and developed by Italtel for the Italian Public Operator TELECOM Italia, to be used in Passive Optical Network field trials, currently under way in Turin and Rome.

The integrated splitter will replace a bulky and fragile distribution box using fused fibre couplers and fusion splices manually assembled. It is interesting to note the use of waveguide intersections, which does not causes any measurable signal cross-talk, provided that the intersection angle is higher than a minimum value, which

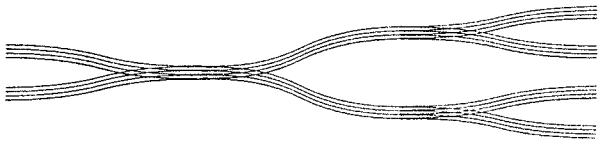


Fig. 4: 2X4 splitter for ribbon cable

depends on waveguide parameters (around 30° degrees for this specific example)

3.1 Directional couplers

When two waveguides come into close proximity (at a distance of the order of magnitude of the guided wavelength) for a certain length, an energy transfer takes place between the waveguides; the effect is the optical equivalent of the directional coupling well known to microwave engineers, and is controlled (Fig. 5) by the operating wavelength, the coupling length L, and the waveguides spacing d. In a directional coupler the input and output waveguides should be single mode while the central zone should be bimodal at the wavelengths of

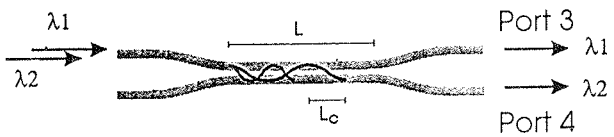


Fig. 5: Schematic of a directional coupler

interest. Due to the small branching angle, light is adiabatically coupled from the input branch into the double waveguide section. The two modes excited at a particular wavelength have different effective refractive indices and thus propagate at different velocities in this section. As these two modes interfere with one another the energy in the central zone oscillates from one waveguide to the other as the resulting phase difference between the two modes changes. Taking account of the distributed coupling in the input and output sections , this phase difference is given by:

$$\Delta\phi = \Delta\phi_{\text{central zone}} + \Delta\phi_{\text{branching zones}} = \Delta\beta\, L + \int \Delta\beta\, dz \qquad (1)$$

By ignoring the second term in this equation we can derive an expression for the coupling length in the central zone:

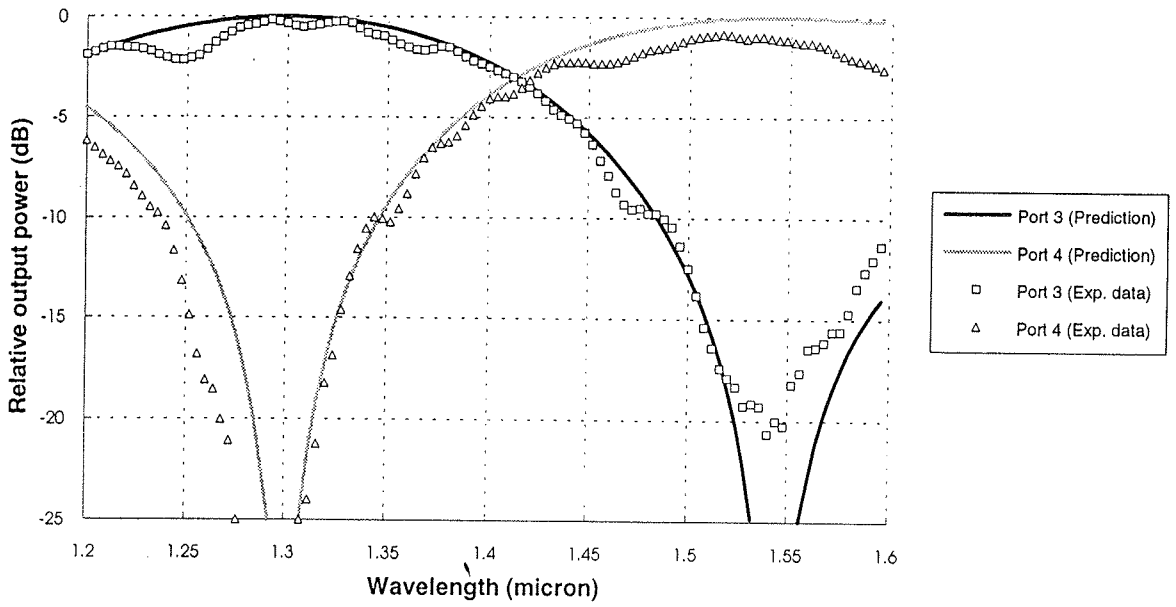


Fig. 6: Design prediction and experimental results of a WDM

$$L_c(\lambda) = \frac{\lambda}{2\left(n_{00} - n_{01}\right)} \qquad (2)$$

Multi/demultiplexing between two wavelengths may be achieved by choosing the length of the two waveguide section to be an even multiple of L_c at one wavelength and an odd multiple of L_c at the other.

The spectral characteristics of a directional coupler WDM are shown in fig.6, where excellent agreement is obtained between design prediction and experimental results.

3.2 Wavelength Division Multiplexers

The directional coupler principle can be used in a more complex structure (Fig. 7) based on two input ports, two 3-dB directional couplers, and a central section where one of the waveguide is longer by ΔL, in order to give a wavelength dependent phase shift between the two arms, and two output ports. The resonance conditions required for the multi/demultiplexing of two specific wavelengths are (at the output of the interferometer):

$n(\lambda 1).\ \Delta L = m.\ \lambda 1$

$n(\lambda 2).\ \Delta L = (m \pm 0.5).\ \lambda 1$

where $n(\lambda)$ is the refractive index and m is an integer.(the order of the interferometer).

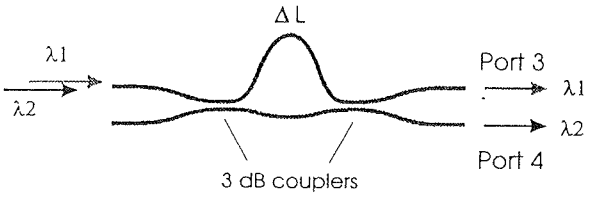


Fig. 7: Mach-Zehnder interferometer

The power from the input port divides between the two output ports in such a way that a specific wavelength can be adressed to each port. Therefore, the transmission characteristic of the Mach Zehnder interferometer allows the realisation of a wavelength division multiplexer or demultiplexer (WDM) where many optical carriers are being transmitted on a single fibre in a transmission network. While this principle was well known and applied for quite a long time, the new opportunity offered by the glass on Silicon technology is the full support from a computer aided design capability, which directly generates the photolitographic masks needed to implement the required design, with high accuracy and reproducibility. Moreover, the use of CAD tools would make it relatively easy to implement complex structure starting from more simple building blocks already designed and tested; for example, a four channel multiplexer, shown

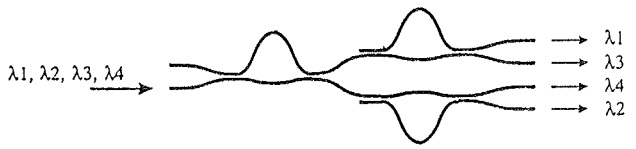


Fig. 8: Four channel WDM schematic

in fig. 8, is composed of three Mach Zehnder interferometer elements. The power from the input port divides among the four output ports, as a function of the selected wavelengths. the spectral characteristic of the four channels WDM is shown in fig.9.

The precise differences in path length required for the multiplexer design is easily controlled by the the mask fabrication process. With normal tolerances available in microelectronic masks, it would be possible to design multi channel WDM with channel spacing as low as 0.1 nm, the only limitation in channel number being the available wafer size.

The Mach-Zehnder interferometer is a basic building block in the design of a variety of optical control functions based on the splitting and combining of optical beams, normally as a function of their wavelength, which is controlled by the different optical length of the two interferometer arms. If this difference could be varied externally, a tuning capability would be added to the interferometer. In the case of devices built on an electrooptic material such as $LiNbO_3$, this effect is achieved by applying an electric field. In the GoS case, similar results has been experimentally demonstrated by NTT by using a thermo-optic effect [3]. In practice, a thin film NiCr strip heather is metallised on top of one interferometer arm, whose optical path length can be controlled by a thermorefractive effect due to current heating of the NiCr strip. Even if this effect is relatively slow, with response time of the order of milliseconds, it can be very useful in the development of complex multiwavelength networks as it would provide an economic solution to many wavelength control and routing problems, where only low speed processing capability is generally needed.

3.3 Multifunctional devices

More complex passive optical devices are at present under study to be implemented in the GoS technology; two examples will be shortly described here in order to give a simple demonstration of the potential of the approach. Both devices have already been tested in terms of feasibility in the ATT and NTT Laboratories.

With glass on silicon technology it is possible to implement waveguide patterns of NxM star couplers [4,5,6] (N and M up to 256) as shown in fig 10. The input power from any one of the 256 channel waveguides in the input array is radiated to a slab region and received by the output array. The uniformity of the optical power distri-

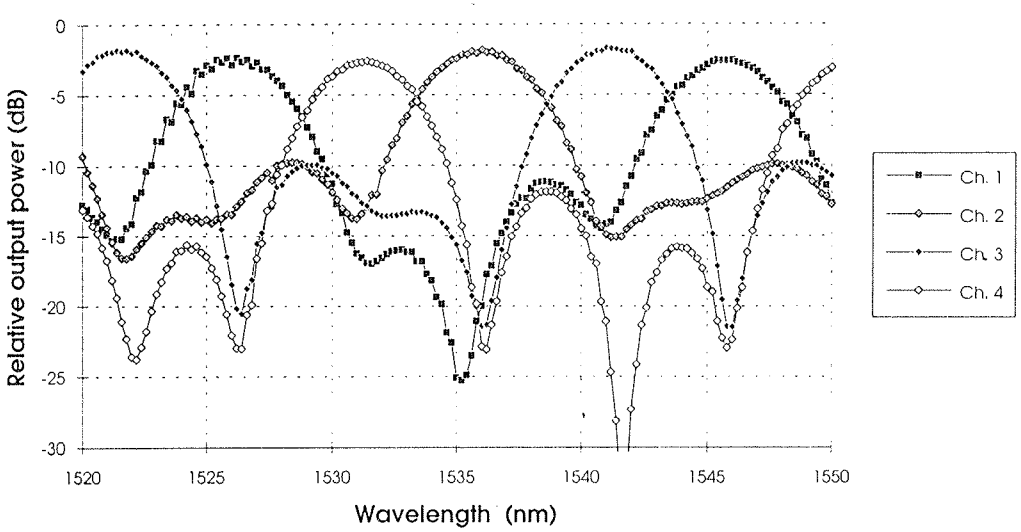


Fig. 9: Measurement of a 4 channel WDM with 5 nm channel spacing

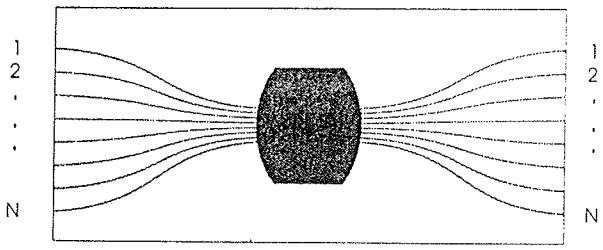


Fig. 10: NxN star coupler

bution was obtained by optimising the coupling conditions between adjacent waveguides in the input waveguide array. This device has the added advantage of being wavelength independent if properly designed.

Another complex device which has been realized using this technology is the NxN ($N \leq 8$)switching matrix, as developed by NTT [7] and illustrated in fig 11.

This device allows the routing of an optical signal to any one of N output fibres. The routing is realised using a composition of N^2 elementary switches each of which is based on a symmetric Mach-Zehnder interferometer thermally tuned by an electrode. Both arms of the interferometer are of equal length (no geometrical path difference) and the optical path difference is varied by modifying the effective refractive index in one of the two arms by means of the thermooptic effect. This effect is generally slow ($\approx$ 1 ms) but still quick enough for most routing applications.

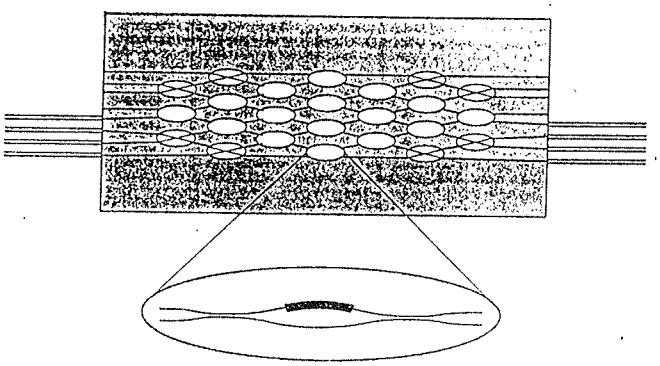


Fig. 11: NxN switching matrix

4. HYBRID ACTIVE INTEGRATED COMPONENTS

Assembly of active devices, such as lasers and photodetectors, on the Silicon substrate, with self alignement features with respect to passive elements (Fibres and planar waveguides) is another critical step to achieving a practical optical integration capability. Therefore, two basic processes have been established to develop the elementary building blocks for such functions.

4.1 Integrated photodetector (PIN-PAC)

The basic version of the integrated photodetector consists of a PIN photodiode mounted on a silicon submount and coupled to an optical fibre pig-tail (fig. 12).

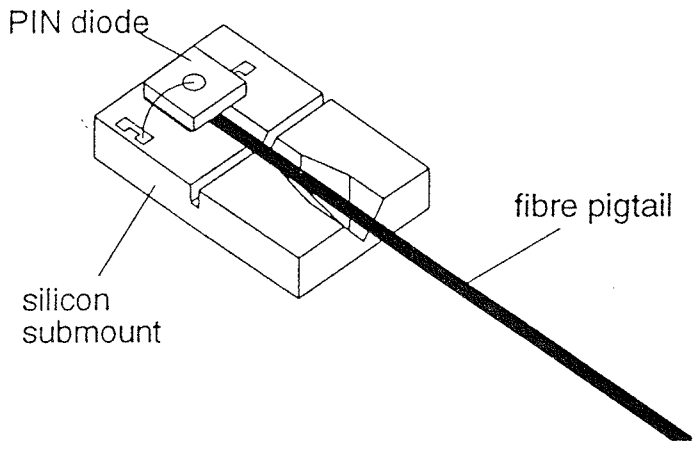


Fig. 12: PIN-PAC integrated photodetector

The basic characteristics of the PIN-PAC are:

1. the use of a 45° degree mirror to reflect the incoming light from the fiber pig-tail to the bottom illuminated photodetector soldered above it .

2. the use of anisotropic etching through a thick SiN or SiO_2 mask to form deep "V-grooves" in the Silicon substrate to house and fix the fibre pig-tail, with process reproducibility capable of achieving a 1μm tolerance in the position of the fibre, without any active alignement procedure.

3. the use of a particular metalisation pattern on the Silicon substrate and on the photodiode which makes possible the self-centering of the photodiode die with respect to the turning mirror position during the die-attach soldering process. This process can be done in a single step at the wafer level for hundreds of PIN devices simultaneously.

Therefore the PIN-PAC device is made without the need for individual optical alignement; the process is suitable to achieve both high production volume and very low cost. The assembly shown in fig 12 is a discrete device, which offers a very competitive trade-off between performance, cost and overall quality, with respect to currently available standard alternatives. In the case of an integratable photodetector, a similar but somewhat more complex process technology has been developed, in which the turning mirror is directly etched in the glass waveguide. In conclusion, the optical receiver function can be considered fully available for an hybrid integration in a Glass on Silicon optical IC.

4.2 Integrated photoemitter (Laser-PAC)

Intermediate results have been achieved so far in the case of the optical transmitter. A similar structure for a discrete device (Laser-PAC) (Fig. 13) has been developed, which already offers distinct advantages in terms of performance and manufacturing procedures with respect to standard laser modules, (the use of an integral microheather for the soldering of a metallized fibre pig-tail to the silicon submount, for instance) but still requires an active alignement procedure. Moreover, the Laser-PAC structure is not suitable for hybrid integration, even if a very simple coupling procedure can be used to join a fibre pig-tail of a few millimeters from the Laser-PAC to a "V-groove" on a separate Silicon substrate.

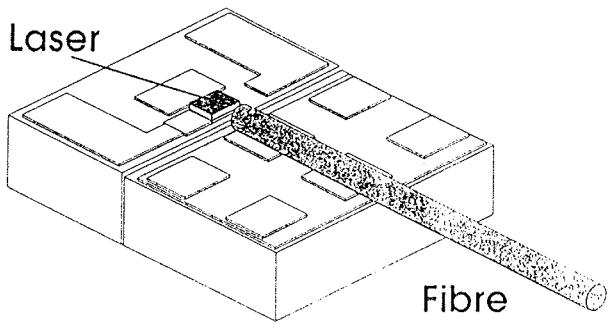


Fig. 13: Laser PAC

5. OPTOELECTRONIC MODULES APPLICATIONS

While most of the effort under way on the Glass on Silicon program is still focused on implementing process technology, and on achieving a good control of design tools and characterisation of basic building blocks described above, a few optoelectronic module prototypes have already been developed for specific applications, by using a combinations of available active and passive optical functions

5.1 Integrated optical transmitter and front-end receivers

The compact and reliable structure of PIN-PAC and Laser-PAC is ideally suited for realising an hybrid optoelectronic IC, by mounting on the same substrate, or on a ceramic support, the required electronic circuits. In the case of the receiver, the structure (fig.14) includes a PIN-PAC photodetector and a custom IC for preamplifier, AGC and clock recovery functions:

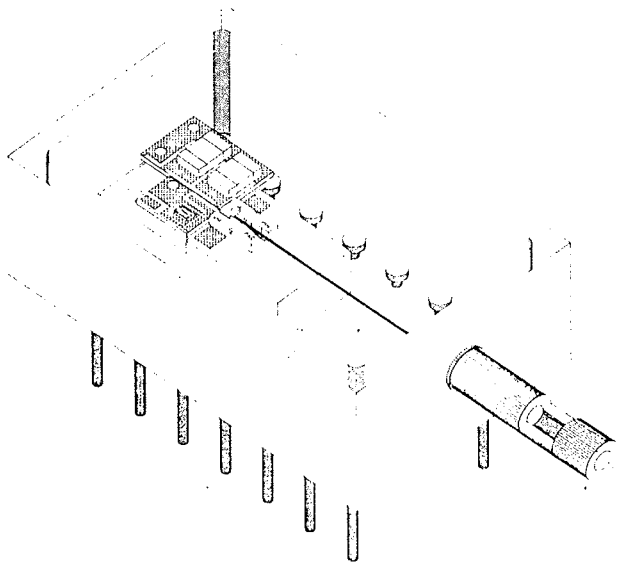


Fig. 14: SDH receiver

Housing is provided by a 2 x 1 cm package with a pig-tail. The transmitter includes a Laser-PAC mounted on a ceramic substrate with a custom IC for laser driver and supervisory and control functions, in the same housing as above. Both units' specifications are compatible with STM1 Synchronous Digital Hierarchy standard for 155 Mbit/s operation. For stand alone PIN- PAC and Laser-

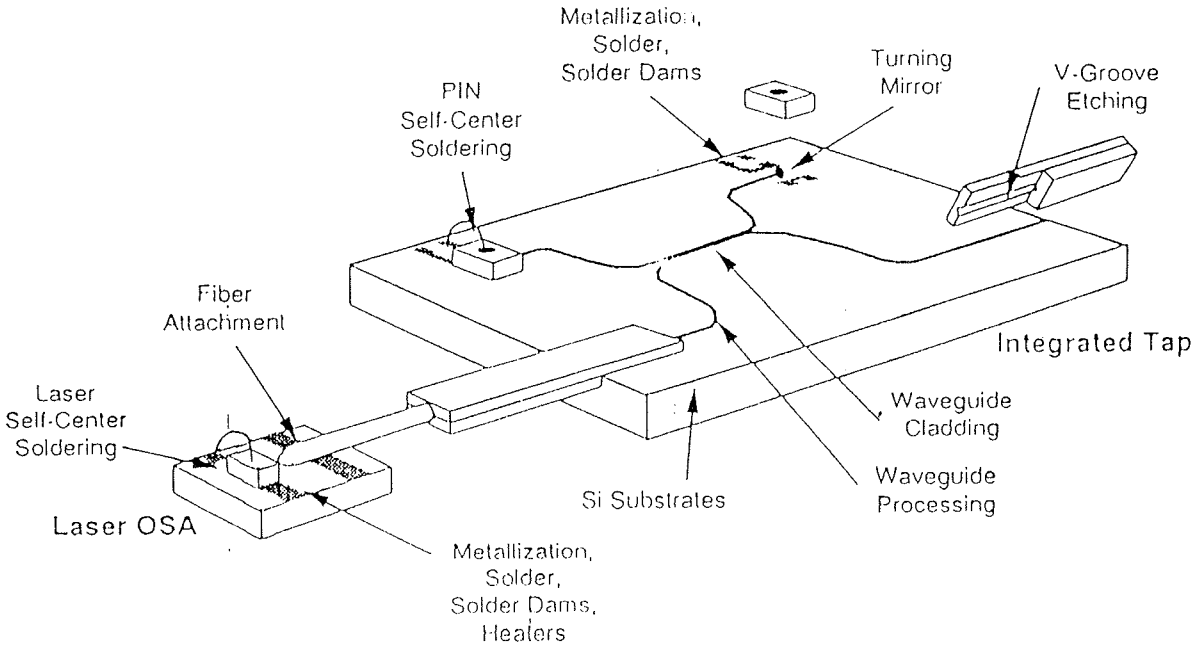


Fig. 15: Bidirectional operating module

PAC devices bandwidths in excess of 1 GHz have been measured, essentially identical to the laser and PIN original bandwidth characteristics.

5.2 Bidirectional optical transceiver

Bidirectional transmission of two carrier wavelengths on the same optical fibre has been considered by several RACE projects to be a viable solution for reducing cost in the implementation of the Broadband Access Network. Bidirectional transmission may be considered as a specific case of WDM principle, and therefore the development of an integrated bidirectional module has been chosen as a significant test vehicle to validate the Glass on Silicon technology with respect to the process capability of hybrid integration of several functions. At present, these functions are the wavelength demultiplexing, the monitor photodiode, the line receiver photodiode, the "V-groove" coupling of the output/input optical fibre and do not include the laser transmitter. A Laser-PAC equipped with a very short (a few mm) pig-tail can be coupled to a "V-Groove" etched into the module. The structure of the bidirectional module (apart from the transmitter side), is very similar to the scheme illustrated in fig. 2, and it is shown in fig. 15.

The optical bidirectional link is equipped with two complementary transceivers for each line termination. In particular data from the network (upstream) side should be transmitted at 1300 nm wavelength and data from the customer access (Downstream) side at 1500 nm wavelength. Also the data rate may be asymmetrical. (622 MBit/s upstream and 155 MBit/s downstream)

The WDM function is realised by a Mach-Zehnder interferometer, which provides enough isolation from optical cross-talk (>20 dB) to achieve the required Bit Error Rate on the line terminal; one of the WDM branches also provides the signal for the monitor photodiode. Electronics functions (Laser driver, PIN preamplifier and control circuitry) are realised with bare IC chips, mounted near the optoelectronic module on a ceramic thin film substrate. Layout design to mount these ICs directly on the Glass on Silicon substrate is under study, in particular to evaluate electrical cross-talk problems. The hybrid integrated circuit, including electronic functions, is housed in a 24 pin Dual in Line package.

6. CONCLUSIONS

Features of a new approach to the development of hybrid integrated optical circuits have been presented, taking into account material deposition processes, packaging and assembly aspects, and preliminary results on prototype design and characterisation. Main achievements reported to date include the simulation and design of several passive optical components, whose performance has been experimentally tested with good overall results. A sufficient set of CAD rules and basic building blocks have been established and experimentally assessed to make possible quick end efficient design of more complex functionalities. On the other hand, the high degree of process reproducibility, tested with good statistical accuracy, makes us confident that the technology is sufficiently stable and controlled to allow a pilot production line deployment, which would be in full operation by mid 1995. To our knowledge, this is the first industrial initiative in Europe for a product development which may lead to a significant breakthrough in the field of optoelectronic component manufacturing and optical communication system technology.

ACKNOWLEDGMENTS

The Authors wish to acknowledge the work done by all the Colleagues of the GoS Group, and in particular the outstanding contribution to the results described here given by S. Doneda, G. Iseni and G. Preve.

REFERENCES

/1/ "New technology for reduction in cost and size of silica guided wave component", K.Imoto and A.Hori, Electronics Letters Vol.28 No.17, 13th August 1992.

/2/ "Optimum planar bends", C.Dragone, Electronics Letters Vol.29 No.12, 10th June 1993.

/3/ "A four channel optical waveguide multi/demultiplexer for 5 GHz spaced optical FDM transmission", Kyo Inoue et al, Journal of Lightwave Technology Vol.6 No.2, February 1988.

/4/ "Efficient multichannel integrated optics star coupler on silicon", C.Dragone et al, IEEE Photonics Technology Letters Vol.1 No.8, August 1989.

/5/ "Efficient NxN star couplers using Fourier optics", C.Dragone, Journal of Lightwave Technology Vol.7 No.3, March 1989.

/6/ "Efficient NxN star couplers based on Fourier optics", C.Dragone, Electronics Letters Vol.24 No.15, 21st July 1988.

/7/ "Silica based optical matrix switch with intersecting Mach-Zehnder waveguides for larger fabrication tolerances", M.Kawachi et al, OFC/IOOC '93.

A. Fincato, S. Lorenzotti, P. Nugent, G. Parafioriti and G. Randone,
Italtel, Central Research Laboratories
Castelletto di Settimo Milanese,
Milano, Italy
tel. + 39 4388 7320
fax + 39 4388 7989

Prispelo (Arrived): 15.08.94 *Sprejeto (Acepted): 20.09.94*

UDK 621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 24(1994)3, Ljubljana

A MULTILAYER CHIP VARISTOR: THE FUTURE IN THE LOW VOLTAGE TRANSIENT SUPPRESSION
Part I: Fabrication and Characteristics

Z. Živič
KEKO, Žužemberk, Slovenia

Keywords: voltage transients, protective devices, protection components, SMT, surface mount technology, multilayer chip varistors, MLV chip varistors, ZNO varistors, thin sheet laminating technology, ceramic technology, leakage currents, surge currents, response times, nonlinear coefficients, surge absorptions, electrical breakdowns, fabrication processes, electrical properties

Abstract: A low voltage ZnO multilayer chip varistor for surface mounting was developed using tape casting and green sheet laminating ceramic technology. Differently sized chip varistors with breakdown voltage ranging from 4 V to 100 V were realised, featuring low leakage current, high nonlinear coefficient in a wide current range, very high surge current withstand capability (> 2000 A) and response time shorter than 5 ns. Very good stability on repetitive pulse of high amplitude and high energy level was also recorded. All these characteristics make multilayer chip varistor a very promising low voltage protection device.

Večplastni čip varistor: Prihodnost zaščite proti prehodnim pojavom in napetostnim sunkom
I del: Izdelava in lastnosti

Ključne besede: pojavi prehodni napetostni, naprave zaščitne, elementi zaščitni, SMT tehnologija montaže površinske, MLV chip varistorji večslojni, chip varistorji, ZNO varistorji, tehnologija nalivanja plasti tankih, tehnologije obdelave keramike, tokovi uhajavi, tokovi udarni, časi odzivni, koeficienti nelinearni, absorpcije udarov, preboji električni, procesi proizvodni, lastnosti električne

Povzetek: Nizko napetostni ZnO večplastni čip varistor za površinsko montažo je bil razvit s pomočjo keramične tehnologije nalivanja tankih plasti. Narejeni so čip varistorji različnih dimenzij, s prebojnimi napetostmi v obsegu od 4 V do 100 V, z naslednjimi lastnostmi: nizki tok puščanja, visoki nelinerni koeficient v širokem tokovnem področju, sposobnost absorpcije tokovnih sunkov višjih od 2000 A in čas odziva krajši od 5 ns. Zelo dobra stabilnost proti tokovnim sunkom visoke amplitude ter visokih energij je tudi bila ugotovljena. Vse te lastnosti kažejo da je večplastni čip varistor zelo obetavna nizko napetostna zaščitna komponenta.

1. Introduction

Electronic and electrical circuits can be subject to severe and sudden impulse voltage transients generated by lightning, switching and electrostatic discharge accumulated on the human body.

A contemporary development in the field of electronics and especially microelectronics requires miniaturised, highly integrated and low power consumption devices. As a result of this, the requirements for reducing device sizes and operation at low voltages are becoming extremely important for all electronic components including protective or surge absorbing devices.

Namely, lowering of the device geometrical dimensions, or scaling down principle, is widely used to improve CMOS IC's performances as: speed, density, complexity, reliability and cost. The dimension lowering is followed by operating voltage lowering as well. At the same time, internal protection devices built into IC's (typically containing monolithic connected diffused resistor with two or four Zener diodes) have been reduced in size to minimise their impact on speed and circuit area. Therefore, protection efficiency of the internal protection decrease, so CMOS IC's become more sensitive to damage or malfunctions caused by supply voltage transients and electrostatic discharges.

As a solution, electronic designers can either overspecify the circuits or use external protection. Final stability and quality of systems as well as economic balance call for the use external protection, not only of the whole systems or subsystems but of the individual sensitive components as well.

Transient voltage overstress protective devices can be divided into three categories: filters (R-C, R-L-C, etc.), crowbars such as gas discharge tubes or thyristors and low voltage clamps like varistors and Zener diodes. As

* - This paper presents a part of the results accomplished within the project titled "Multilayer Electronic Ceramic Components", no. B-669, which was partially financially supported by Slovene Ministry of Science and Technology from 1991-93.

far as low voltage surface mount devices are concerned only multilayer chip varistor (MLV) and Zener diode will be discussed. Both exhibit the necessary voltage - current relationship: at low voltages the current is very small, but when the applied voltage exceeds some predefined value (threshold), the device impedance decreases drastically and dissipates the excess energy which would be absorbed by the active component being protected. A ZnO MLV as well as Zener diode have this property although the operating physical principles and technology are different as shown in Table 1.

Both planar Si processing technology and pn-junction physics as a basis of Zener diode functioning are very well covered in literature[1,2]. Shallow pn- junction depletion region directs the operation of Zener diode. Its breakdown mechanism is tunnelling and avalanche multiplication one. Zener diode breakdown voltage is regulated by the depletion layer width, i.e. by the charge carrier concentration on both sides of pn-junction as well as by its geometry. When the diode is in breakdown, the greatest part of the energy is dissipated exactly in the shallow depletion layer.

In the case of varistor the physical model of its operation is not so 'clear', which will be one of the subjects of the discussion to follow.

Table 1: General differences between Zener diodes and multilayer varistor

General Characteristics	Zener Diode	MLV
Basic material	Si	ZnO
Structure	Monocrystal	Polycrystal
Physical mechanism	Tunneling & avalanche multiplication	Thermoionic emission & hot carrier injection effect
Barrier type	Abrupt junction	Double Shotky barrier
Technology	Planar Si	Ceramic - thin sheet laminating

2. Fundamental Characteristics of ZnO Varistors

2.1. Basic material

While Zener diode is semiconductor component made on monocrystalline Si, varistor is polycrystalline semiconductive electronic component on ZnO. Semiconducting ZnO of wurzite crystallographic structure is basic varistor material amounting to more than 90 % wt. This structure is relatively 'open' allowing easy building-in of dopants and influencing the nature of defects and diffusion mechanism[3]. The most common defect in ZnO is the metal ion in the open interstitial site, leading to a nonstochiometric metal excess N-type semiconductor with band gap of 3.3 eV. Within the band gap there are donor and acceptor levels occupied by thermally induced intrinsic defects as shown in Fig. 1.

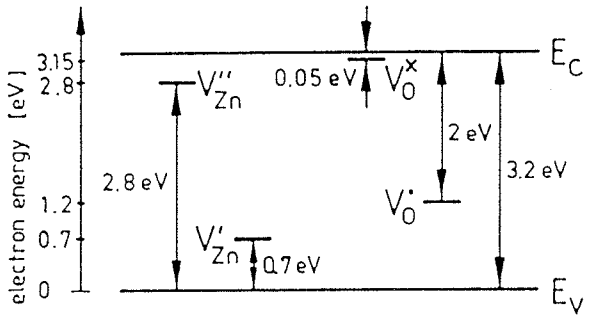


Figure 1: Energy - band diagram of ZnO[3]

2.2. Varistor Microstructure

Varistor is realised by homogenisation of ZnO powder with the oxide additives of Bi, Sb, Mn, Co, Cr, Ni, Al, etc. Forming of such a composite is performed by one of the ceramic procedures (dry pressing for example). After sintering, final polycrystalline ceramic structure, characterised by unique grain boundary properties that contribute to the nonlinear I-V varistor characteristics is obtained. As the flow of the electric current is controlled by electrostatic potential barrier of the grain boundaries, its electrical activity and microstructure can be adapted to provide the desired special properties of the material. For this reason many material scientists have been extensively studied ZnO varistor mictrostructures, especially those of the grain boundaries[4-6]. Their main concern was to investigate various crystalline phases, their

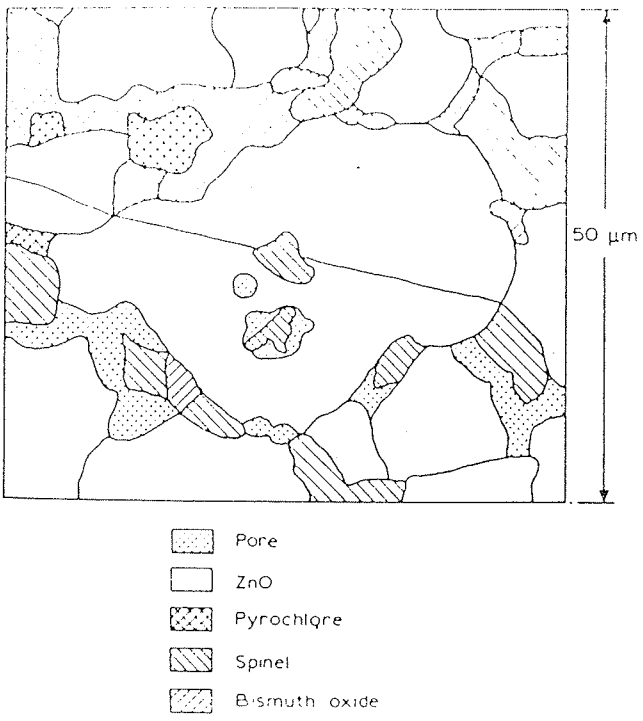


Figure 2: Actual structure of ZnO varistor[7]

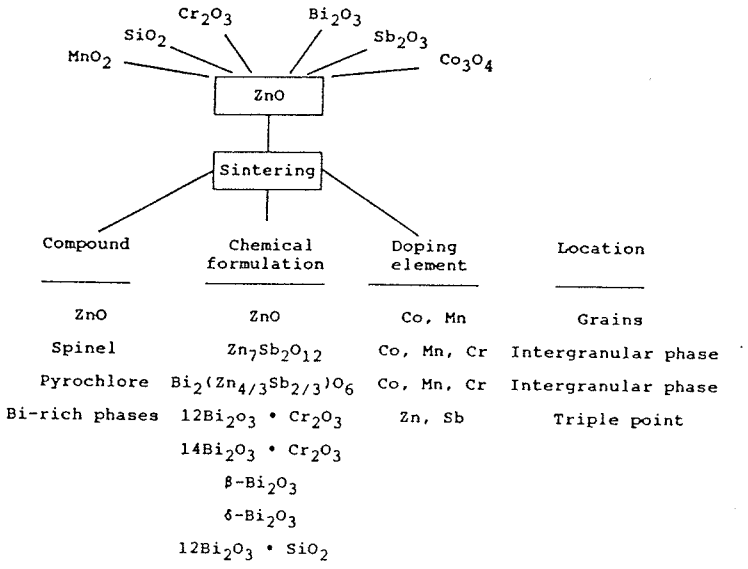


Figure 3: Microstructural components of the ZnO varistor[8]

chemical formulation and dopants in various phases comprised in varistor structure on the one hand, and their influence on electrical characteristics on the other hand. Schematic view of the real ZnO varistor microstructure is shown in Fig. 2., which illustrates ZnO grains surrounded by spinel, pyrochlore and several Bismuth phases including intra- and intergranular porosity. The major findings of the microstructure analyses are summarised in Fig. 3.. When the grain is etched out with acid, intergranular phases appear as a three dimensional network, which is electrically conductive under certain conditions (high field, high temperature, etc.)

Microstructural study resulted in a vary important conclusion. The primitive varistor or basic building block of a ZnO varistor is a boundary between two grains, being formed during sintering. Different chemical elements and ZnO intrinsic defects are being distributed during sintering so that the grain boundary region becomes highly resistive ($R_{gb} \approx 10^{12}$ Ωcm) and the grain interior highly conductive ($R_g \approx$ 1-10 Ωcm). Abrupt conductivity change on the grain boundary suggests the existence of the potential barrier and the depletion layer on both sides of the boundary inside the ZnO grain. It should be pointed out that each grain boundary in doped ZnO shows a nonlinear I-V characteristics, except in the cases, where one of the grains has high symmetry (e.g. basal plane), showing special electrical properties[4]. Several studies have indicated the presence of a thin (<20Å) and homogeneous layer of Bi[3,9] and excess oxygen at the grain boundary[10] as shown in Fig.4.

The role of Bi in grain boundary activation is very interesting. On the one hand, no varistor effect is obtained without Bi doping. On the other hand Bi concentration at the grain boundary stays unchanged in the cases of postsintering annealing or electric loading, when I-V

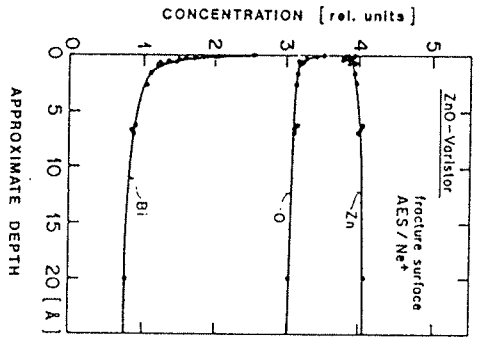


Figure 4: ZnO varistor grain boundaries AES chemical analysis[10]

characteristic in the prebreakdown region changes its shape[10]. Similarly, no correlation has been found between net charge stored at the grain boundary and Bi concentration. That's why it is generally assumed that absorbed Bi ions create some intrinsic interface defects which are capable of capturing an excess electron.

Unlike Bi ions, O ions are completely mobile[10], their concentration on the grain boundary being in the direct correlation to the I-V characteristic change, i.e. to the potential barrier height and the net charge stored at the grain boundary[11].

2.3. Varistor Physics

Several physical models have been proposed in the past to explain conductive mechanism in varistor[12,13]. Their inadequacy was in the fact that they could explain just

some of the experimental results. Advances in microstructural analysis at the atomic level and a wide range of electrical and spectroscopical measurement techniques helped Pike[14] to establish the most comprehensive model, being later refined by Greuter and Blatter[11,15].

The model is based on the fact that a net interface charge at the grain boundary results from the trapping of an excess electron (or hole) by the appropriate interface states. The interface charge Q_i is screened by the ionised bulk defects N_o, associated with intrinsic defects such as Zinc interstitial or Oxygen vacancies, in order to establish the overall charge neutrality. Visualising this process in an energy band diagram corresponds to the formation of a double Schottky potential barrier at the grain boundary as shown in Fig. 5. The current flowing across the grain boundary is controlled by the applied bias and the temperature dependent height of the potential barrier $\varnothing_b$ (V, T). Solving the Poisson equation, several authors[12,13,14] obtained that the potential barrier height is 0.9-1.0 eV. It should be pointed out that an increase in Q_i results in a larger $\varnothing_b$, whereas a higher N_o reduces $\varnothing_b$. Applying thermoionic emission model, current flow through the grain boundary can be described by the equation:

$$J = A T^2 \exp\left(-(e\varnothing_s - \in_n)/kT\right) (1 - \exp(-eV/kT)),$$

where A is a constant containing Richardson's constant, $\in_n = E_c - E_f$ and V is the applied voltage.

The existence of the following four current components on the interface is obvious: the thermally emitted electrons travelling from the left to the right and backwards (being suppressed by the factor exp(-eV/kT)) and small current of the electrons being trapped and remitted from the interface states. The two last currents are responsible for the updating of Q_i, and actually control the main current flowing over the barrier[15].

When a bias is applied to the junction (V< 3 V), $\varnothing_b$ will rapidly decay for a fixed Q_i. However, if through the lowering of $\varnothing_b$ new empty interface states can be filled, Q_i increases and $\varnothing_b$ is efficiently stabilised keeping the leakage current low. This is usually referred to as a pinning of b by the interface states. The strong pinning leads to a concentration of the voltage drop within a 1000Å wide region on the positively biased side of the junction. Near the top of the barrier, electric fields as high as 1 MV/cm can build up. Under this condition some electrons can get enough kinetic energy (became "hot") to create minority carriers by means of the impact ionisation. The holes created in this way, diffuse back to the interface ($\tau_t < 10^{-10}$ s), partly compensate Q_i and abruptly lower $\varnothing_b$ initiating the breakdown. Energy-band diagram of "hot" electron-hole induced varistor breakdown, different trajectories of "hot" electrons and the creation by impact ionisation are shown in Fig. 6.

As the optical-phonon scattering at low energies (0.1-0.4 eV) is the dominant loss mechanism in ZnO, a high starting field near the interface is the most important to overcome this critical energy range. On the basis of the

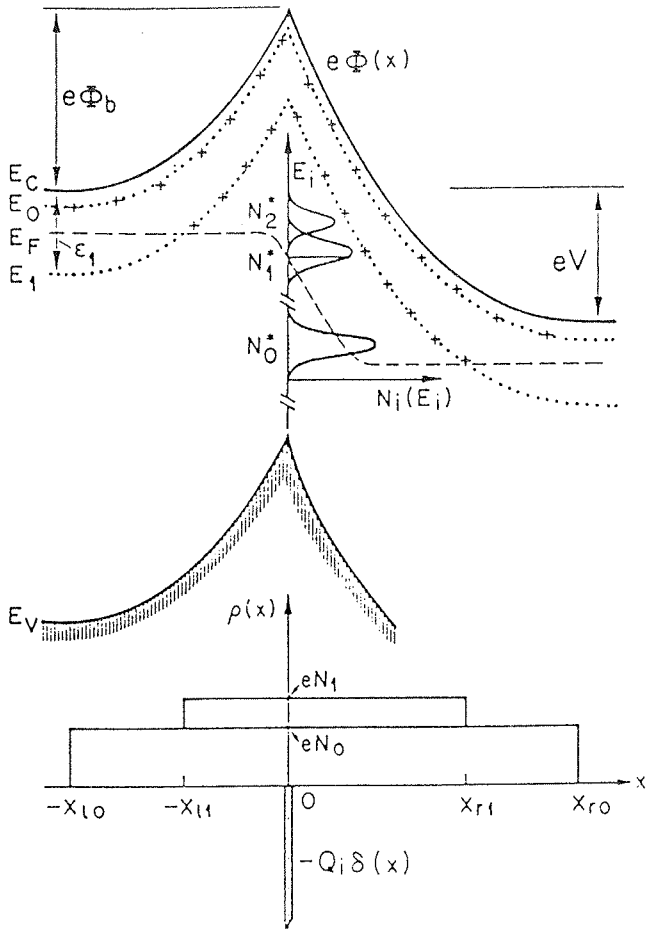


Figure 5: Double Schottky barrier at a negatively charged grain boundary[11]

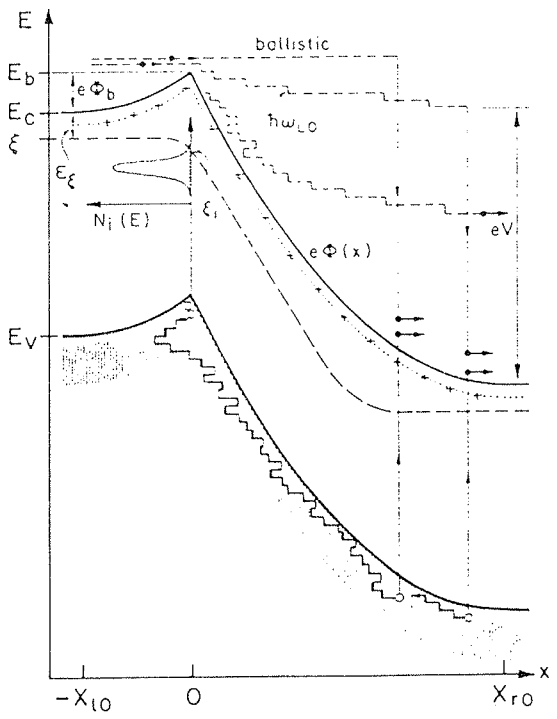


Figure 6: Energy-band diagram of a grain boundary barrier illustrating the hole induced breakdown[14]

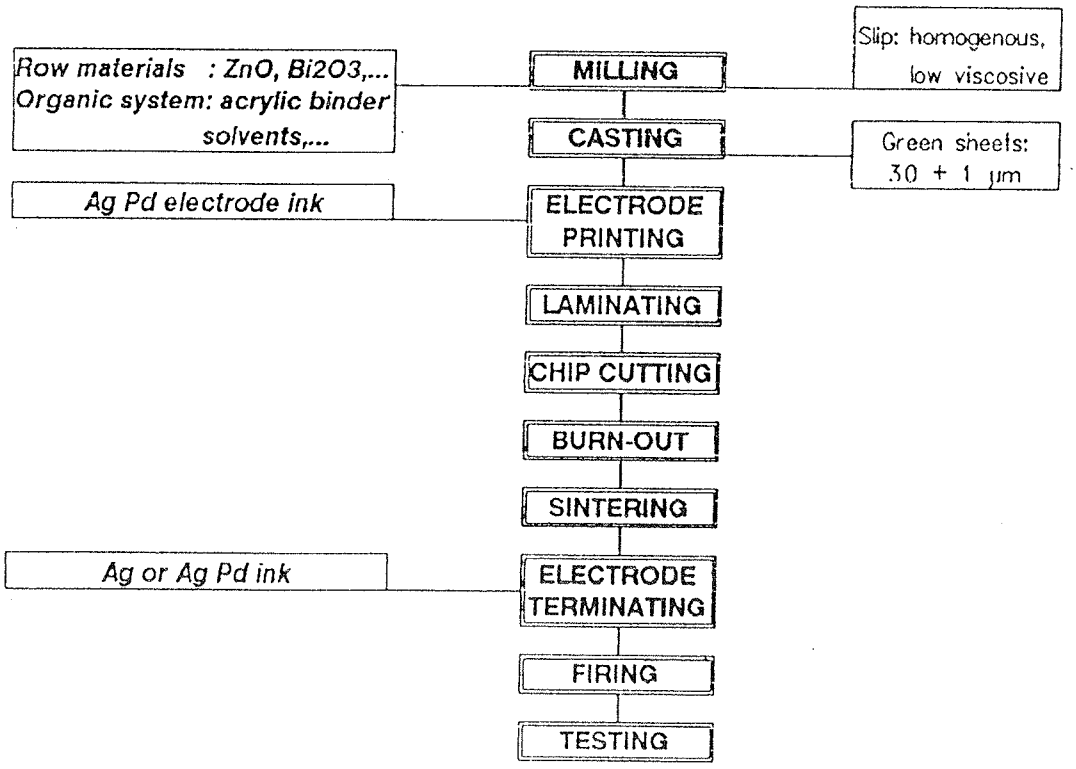


Figure 7: MLV fabrication process steps

data on threshold energy for electron-hole pair creation in ZnO ($E_{th} \approx 3.7$ eV) and the yield of the hole production and using the described model Greuter et. al.[15] estimated single grain boundary junction breakdown to be $V_b = 3.3\text{-}3.8$ V, which is in a very good agreement with the experimental results.

Besides, "hot"-electron-hole induced avalanche breakdown model can explain most basic experimental observations such as: high coefficient of nonlinearity ($\alpha > 40$) and its dependence on doping, small negative signal capacitance at large bias, voltage overshoot effect under the excitation with fast pulses, electroluminescence phenomena observed at grain boundaries and many other[11].

3. Multilayer Chip Varistor

Ceramic tape casting and especially green sheet lamination technology have been very intensively developing during the last twenty years, in the first place owing to the development of the multilayer ceramic capacitor and hybrid integrated circuit substrates. These technologies set the basis for the development of the multilayer chip varistor.

Although the first article was published by Shohata et. al.[16] in 1981 there has been little published about this new protection component, which became commercially available not more than two years ago.

3.1. Technology

3.1.1. Fabrication Process

Green sheet lamination process applied in presented MLV production experience is shown in Fig. 7. Varistor processing was based on fine particle high purity ZnO and other dopants. They were mixed in a nonaqueous system based on an acrylic binder in a ball mill for 15-20 h. The homogeneous low viscosity ceramic slip was tape cast into 30-100 µm thick sheets. Tape cutting was followed by AgPd internal electrode screen printing and their stacking into 10 x 10 cm large green ceramic blocks. Ceramic blocks were then laminated and cut into chips sized 2.5 x 1.5 mm, 3.2 x 2.5 mm and 5.7 x 5.0 mm, which are popular SMD dimensions. After binder burn out, chips were sintered in an air atmosphere furnace at the temperature of 950-1100°C. Finally, external AgPd electrodes were attached and fired to make contact with comb-like inner electrodes as shown in Fig. 8.. Fig. 9 illustrates the outside view and final dimensions of realised chips while Fig. 10 shows optical microscope photographs of the microstructure of the cross sectioned MLV.

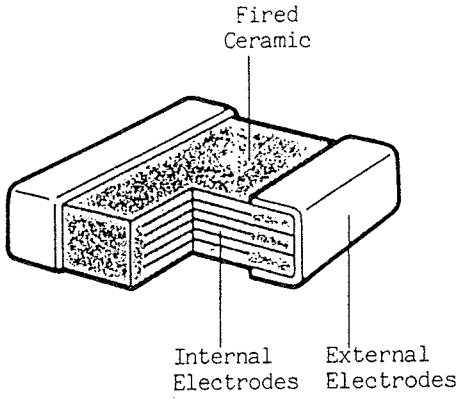


Figure 8: A cross sectional illustration of a MLV

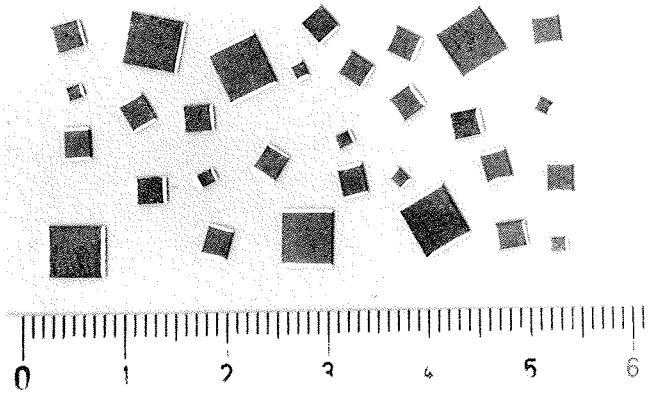


Figure 9: Outside view of differently sized MLVs

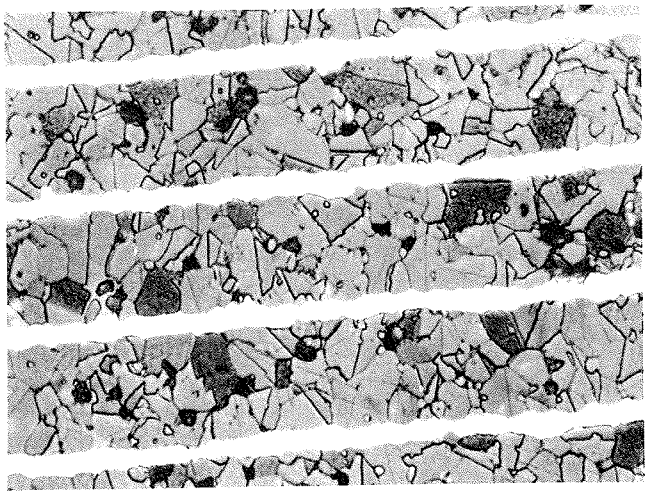


Figure 10: Microstructure photographs of a cross section of an MLV

3.1.2. Varistor Compositions

Shohata et. al.[17] concluded that the utilisation of Bi_2O_3 in MLV ceramic system is not possible because it easily reacts with any metal used for internal electrodes, destroying the multilayer structure. That's why, instead Bi_2O_3, they especially developed and suggested the usage of borosilicate-lead-zinc glass. Microstructural analysis of the ceramic- electrode interface[18] showed increased concentration of Bi in the case of low sintering temperatures (950°C), while at higher temperatures (1100°C) a lamelar reaction product, identified as $PdBi_2O_4$, was observed only in the "pockets" of a melt at the interface. TEM/EDS studies of the interface confirm that the reaction layer is neither continuous nor monophase. Due to that and opposite to the statements in [17], it was shown in [19] and it will be shown in this paper that usage of Bi_2O_3 is possible in varistor system without consequences either to the electrical characteristics or varistor reliability. Having this in mind, special varistor composition was designed[20,21], comprising ZnO (>92 wt %) and oxide additives such as Bi_2O_3, MnO, CoO, Sb_2O_3, etc. As the composition presents one of the design parameters, the care was also taken of the fact, that some differences exist in the case of the bulk varistors and MLV, the final ceramic layer thickness being both small and comparable to the grain size in the later. Two such examples are illustrated in Fig. 11. and Fig. 12.. They show the dependence of nonlinearity coefficient and specific voltage on sintering temperature in the case of MLV (layer thickness ≈ 17 μm) and bulk varistor (d ≈ 1 mm), realised with the same composition.

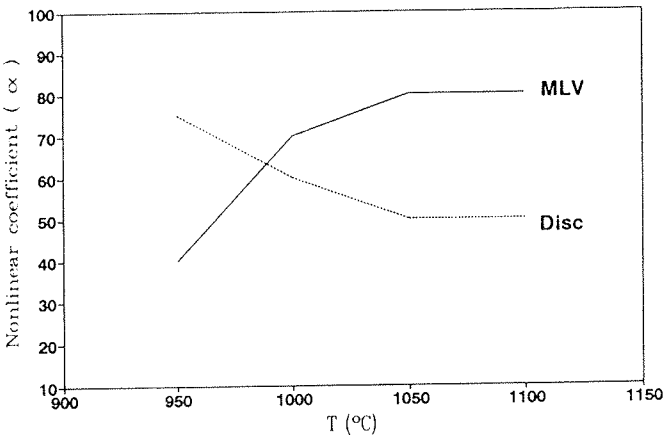


Figure 11: Nonlinear coefficient - α Versus sintering temperature

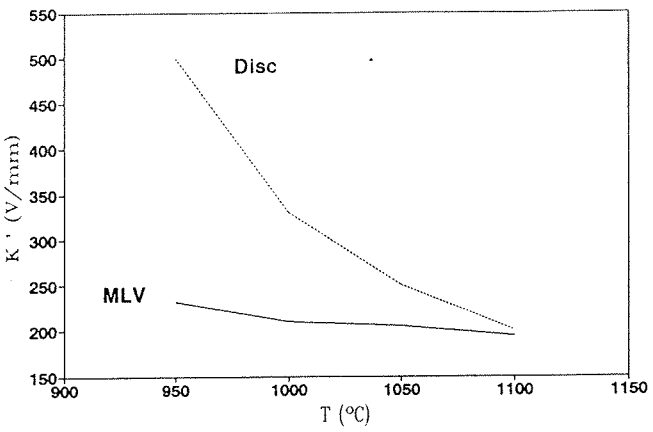


Figure 12: Specific voltage versus sintering temperature

3.1.3. Ceramic Foil

Presently, it is possible to use two processes for thin ceramic foil formation: extrusion & stretching process and doctor-blade tape casting process. We applied both processes to form varistor ceramic foil. The results of the second process will be shown in this paper. Nonaqueous tape casting system, containing acrylic binder, solvents, defloculants, plasticiser and some other additives, was used, enabling formation of homogeneous, stabile, low viscosity slurry, during homogenisation of varistor ceramic system. After homogenisation, the slurry travels on the carrier surface beneath the blade of the knife, that controls the thickness of the out-coming layer. When the solvent evaporates, the fine solid particles coalesce into a relatively dense flexible film that may be stripped from the carrier surface in a continuous sheet. Foils obtained in such a way have good mechanical firmness (enabling simple manipulation) and no pin hole defects. Besides, in the whole range of thicknesses no "skin" effect has been observed as illustrated in Fig.

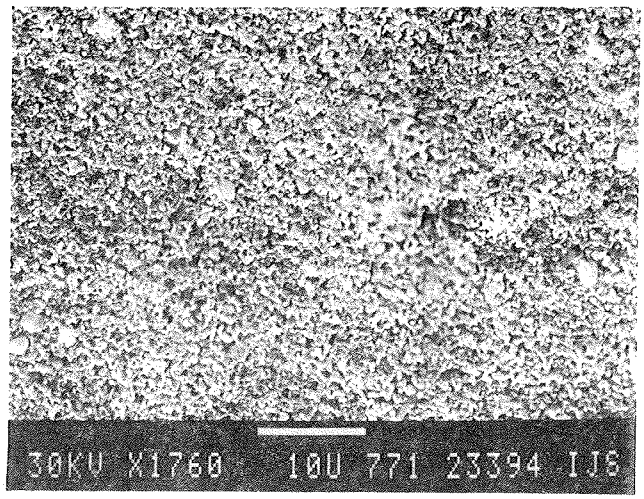


Figure 13: SEM photograph of the tape cast foil surface

13., showing the appearance of the surface of the varistor tape cast foil.

3.2 Chip Design and Structure

Based on considerations in #2.3. the overall varistor breakdown voltages could be calculated as n x 3.6 V, n being the mean number of grain boundaries along the shortest linear path between electrodes. Following this principle a low voltage MLV can be designed combining the ratio of the ceramic foil thickness and ZnO grain size. However, this procedure is limited by the opposing requirements for certain electrical characteristics, processing and surface mount technology.

Fig. 14. shows the breakdown voltages (at 1 mA) dependencies on sintering temperature with green sheet thickness as a parameter, while Fig. 15. shows the photograph of a) 4 V and b) 56 V sectioned MLV at the same magnification.

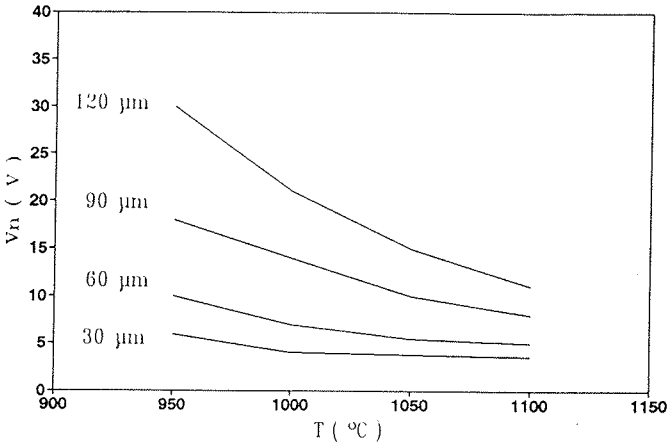


Figure 14: Breakdown voltage versus sintering temperature for different sheet thicknesses

As seen in Fig. 8. inner electrodes are set parallel to each other, where each second electrode is displaced to the same side, so that one group of electrodes is electrically connected to the end termination on one side and the other to the end termination on the other side of the chip. This finger- or comb-like electrode structure enables optimum usage of material volume and shows the whole array of other advantages. Inner electrodes

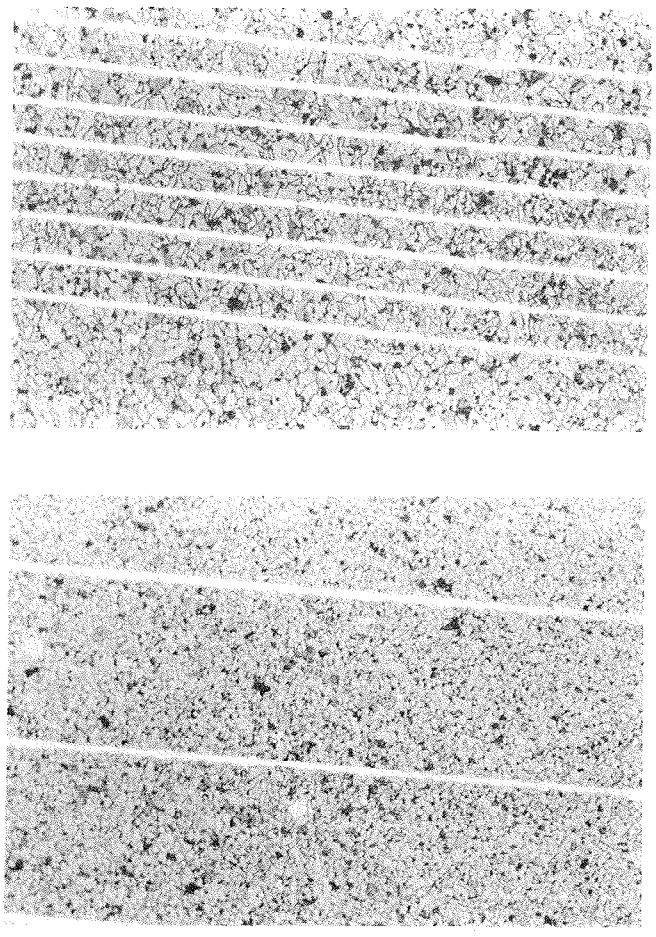


Figure 15: Photograph of cross-sectioned 4 V and 56 V MLV

are encircled with varistor ceramics, so that there are no parasitic structures between adjacent electrodes, meaning that there are no paths causing surface leakage currents or enabling flash-over breakdown. Moreover, this way of electrode design enables their relatively large active surface with respect to chip volume. This is especially evident when compared with the bulk varistor. This electrode disposition enables very uniform current and energy volume distribution, avoiding "hot" spots in the structure, which is of great importance when stability and reliability are concerned.

Beside inner electrode surface, their periphery is important as well. Being very long it facilitates peripheral electrode current injection, similarly as with high current power transistors and acts as an "amortiser" of extremely high current surges.

Being good heat conductors inner electrodes have dual positive role. In the case of ambient heating, they minimise large temperature differences between chip sides, helping uniform microstructure formation and prevent defect diffusion and electrical characteristic degradation. In this case they act as ideal internal heaters. On the other hand, during internal heating due to DC, AC or pulse loading, they conduct heat outwards and act as coolers. This provides fast varistor heat dissipation through the volume, shifting failure mechanism toward higher temperatures. This is one of the reasons that MLV is the only varistor capable of operating at +125°C, whereas the maximum operating temperature of other varistors is +85°C.

3.3. Electrical Properties

3.3.1. Current-Voltage Characteristics

MLVs with breakdown voltage in the range from 4 V to 100 V were realised in the above described way. It should be emphasised, that 4 V breakdown is practically, the lowest theoretically possible breakdown in ZnO varistor (see #2.3.). Achieved result illustrates that, it is possible to realise controllable microstructure, such, that in the cross section between the adjacent large surface electrodes there is only one grain boundary on the average, i.e. the whole structure acts as one large equivalent monobarrier.

Fig. 16 a) and b) shows symmetrical AC I-V characteristics of 4 V and 56 V varistor respectively. The sharp breakdown knee is typical for these high devices with a clearly defined threshold voltage. This is even more evident in Fig. 17, presenting measured I-V relationships. Wide current range measurements were provided using DC technique up to 10 mA and the pulse (8/20 μs) technique above this value. In both cases characteristics show distinct difference between the prebreakdown and breakdown region, which extends over six (for 4 V MLV) to seven (for 56 V MLV) orders of magnitude of current. Typical values of the nonlinear coefficient α measured

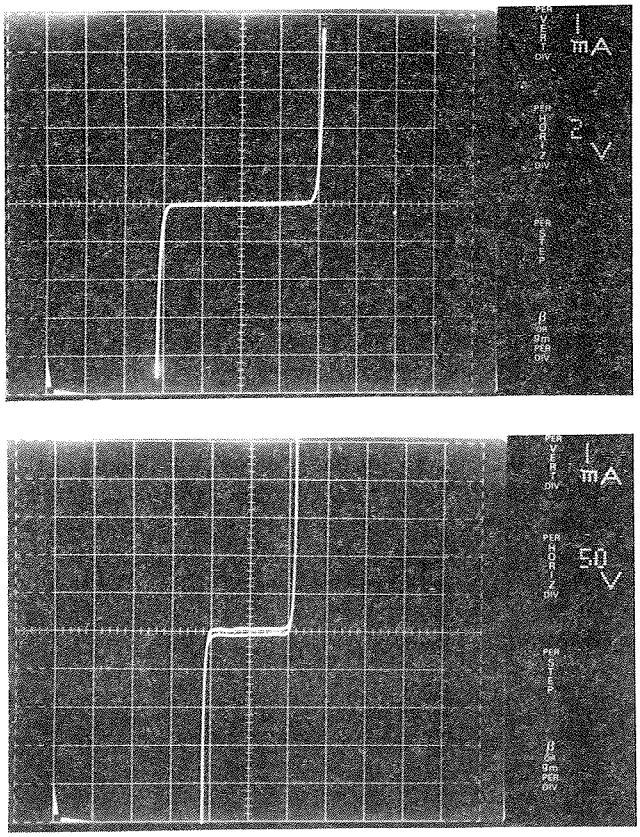


Figure 16: AC current-voltage characteristics of the a) 4 V and b) 56 V MLV

by the ALPHA meter in the current range from 1-10 mA usually exceeds 25 and in some cases reaches values over 50. It is especially important that α has so high value within the whole breakdown region. Fig.18. illustrates the example of 33 V MLV (5.7 x 5.0 mm), where α has the value >15 in the current range up to 1000 A, above which its value decreases and correlates with upturn region on the I-V characteristics. Protection level coefficient, defined as the ratio of clamping voltage for any specified current and the breakdown voltage at 1 mA, has the value < 2.5 up to the current value of 1000 A, increasing for the higher currents. It means that MLV provides very effective protection in the wide current range.

In the prebreakdown region MLV shows very low leakage current (typically < 5 μA), meaning at the same time, a low DC watt loss upon steady state operating voltage, typically set between 75-85 % of the threshold voltage. Although the leakage current increases with temperature, as shown in Fig. 19., for the case of 4 V MLV measured at V_{dc} = 3 V, it holds relatively low value even for the temperatures as high as +125°C, enabling its normal operation in that temperature range as well (see #3.2.). The linear relationship between current and temperature in semilogarithmic scale confirms the thermoionic emission mechanism, i.e. the validity of physical model described in #2.3.. The measured threshold voltage temperature coefficient is much lower than 0.01 %/°C in the temperature range from +25°C to +85°C.

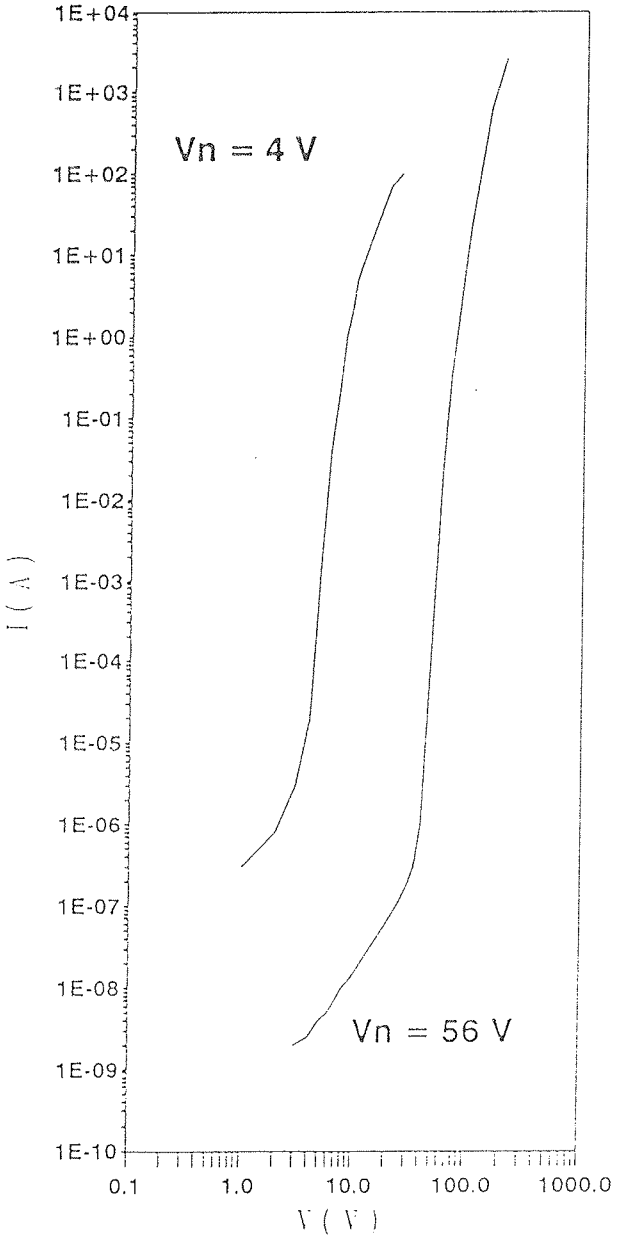


Figure 17: Current-voltage characteristics of 4 V (3.2 x 2.5 mm) and 56 V (5.7 x 5.0 mm) MLV

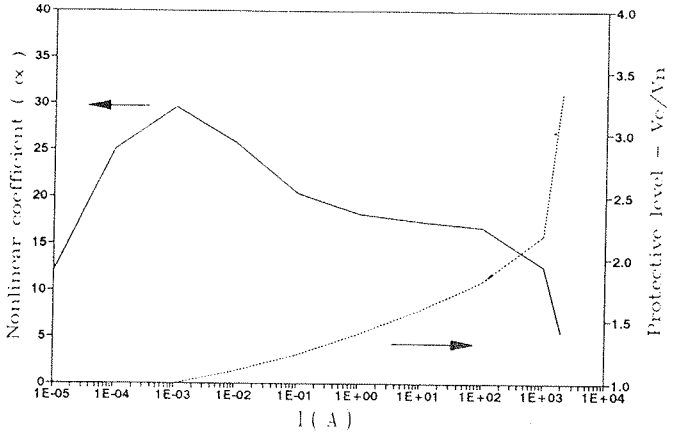


Figure 18: Nonlinear coefficient-α and protective level versus current

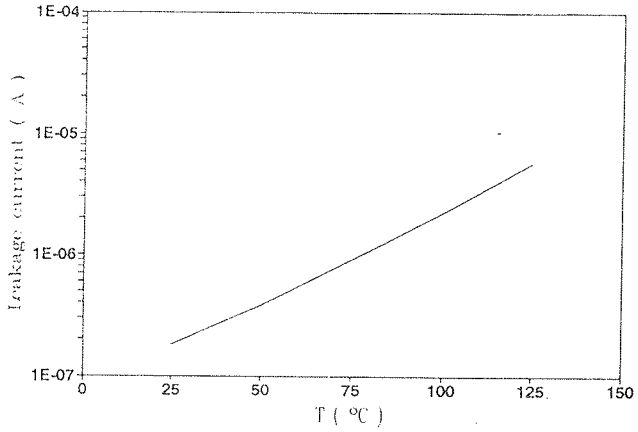


Figure 19: Temperature dependence of DC stand-by current (V_{dc} = 3 V) of the 4 V MLV

3.3.2. Capacitance and Response Time

Dielectric constant of ZnO is relatively small (≈ 10), while the effective dielectric constant of the varistor ceramics is about 100 higher as the consequence of intergranular barriers and their nature (see #2.3.). Capacitance of MLV with different breakdown voltages measured at 1 kHz, ranged from 0.5-40 nF, depending on the chip dimensions, layer thickness and their number. MLV capacitance is relatively stable over a wide frequency range, up to 1 MHz, as shown in Fig. 20.. The same figure shows bell shaped frequency-loss factor characteristics with the minimum value typically at 10 kHz. , The capacitance temperature change, in the temperature range from +25° to +85°C, is < 15 %.

Such a medium MLV capacitance value, which to a certain extent can be designed is especially desirable in specific applications to be discussed in the Part II: Advantages and Applications.

MLV chip has very low inductance, typically < 1.5 nH. The voltage response overshoot effect, being controlled by inherent parasitic lead inductance, is typically not observed in the case of 8/20 μs pulse, as illustrated in Fig. 21.. This figure shows 54 V pulse response charac-

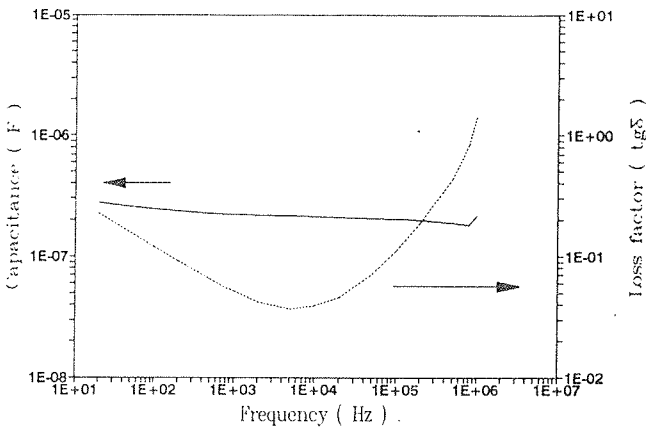


Figure 20: Capacitance and loss factor variation with frequency of the 8 V MLV

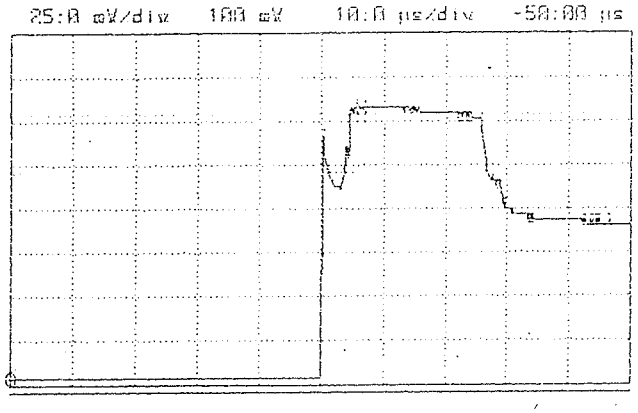


Figure 21: Pulse absorption characteristics of 33 V MLV (8/20 µs, 20 A; Hor. : 10 µs/div, Ver. : 351 x 25 mV/div)

teristics of a 33 V MLV after triggering with 20 A of 8/20 µs pulse. Our present equipment has enabled us to estimate the response time of MLV to be definitely < 5 ns, being adequate for protection in electrostatic discharge environment.

3.3.3.Stability and Reliability

MLV stability and reliability are especially important regarding the fact that it is intended to be protective device. To estimate its stability and reliability a number of tests were performed. The result of high current amplitude and high energy surge withstand capability tests are shown in Fig. 22 and 23.. Standard surge pulse shapes of 8/20 µs and 10/1000 µs were used. The relative threshold voltage change is plotted as a function of the number of surges. It is evident in Fig. 22. that in the case of 8/20 µs pulse threshold voltage increases somewhat faster during the first 10 surges, the change being slower afterwards. The change is lower than 5 %, even after 500 surges. The value of this result can be fully evaluated, having in mind that threshold voltage change of 33 V standard 20 mm disc varistor is higher than 10 % already after 100 to 150 surges. Similar results were obtained in the case of 10/1000 s pulse as shown in Fig. 23. It illustrates excellent stability of MLV

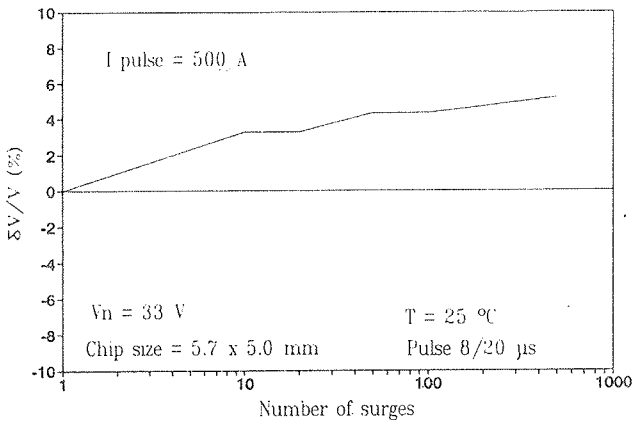


Figure 22: Repetitive pulse capability (30 s between pulses)

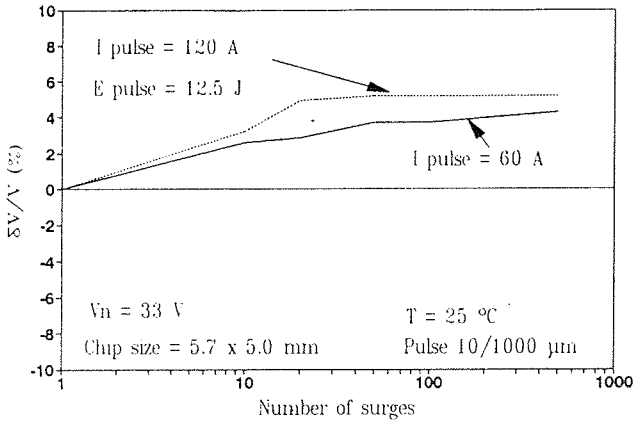


Figure 23: High energy repetitive pulse capability (30 s between pulses)

even in the case of 12.5 J pulses. During this test 33 V MLV was cumulatively absorbing the energy of more than 6 kJ in the period of 4 h, without substantially changing its characteristics. Similar threshold voltage change in the cases of different MLV pulse loading, suggests activation of the same failure mechanism, with no regard to the pulse duration or its shape.

As, varistors are, generally speaking, very sensitive to DC loading in the prebreakdown region, a continuous power dissipation life test was performed on 4 V MLV. The DC applied voltage was higher than the threshold voltage, i.e. the 4 V MLV was subjected to a 10 mA and 30 mA current. A stability that can not be obtained with any low voltage disc varistor is apparent in Fig. 24. Even after 80 min of loading with current of 30 mA, the threshold voltage change was not higher than 15 %. This result, as well as all the others, again confirms the consideration in #3.2. and proves the possibility of realising of a very homogeneous and ordered mictrostructure by means of thin ceramic layer technology.

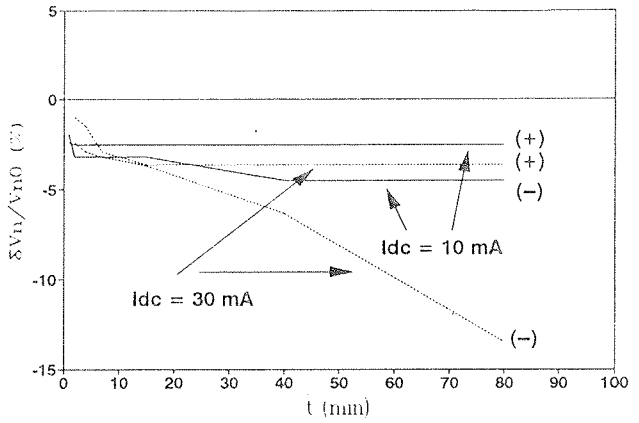


Figure 24: Continuous power dissipation life test of 4 V MLV. The marks (+) and (-) indicate the Vn change in the same and the opposite polarity with DC bias.

4. Conclusion

A low voltage MLV was developed using tape casting and green sheet lamination technology. Obtained electrical characteristics showed that the utilisation of Bi_2O_3 is possible in MLV ceramic system. Namely, MLV has high nonlinearity coefficient in the whole breakdown range, i.e. low clamping level, providing high protection efficiency. It was also shown that with respect to its planar surface MLV can withstand pulse density loading higher than 7000 A/cm^2, being far higher than in any protective device known today. Besides, leakage current in prebreakdown region has relatively small value even in the temperature range around +125°C. Very low inductance of chip MLV enables response time shorter than 5 ns, eliminating to a great extent voltage response overshoot effect.

Life test results, and especially repetitive pulse capability tests show MLV excellent capability to withstand great number of short high voltage surges as well as long high energy surges. Practically all static and dynamic characteristics as well as MLV stability lead to the conclusion that and MLV is favourable low voltage protective device.

Acknowledgement

The author would like to thank Dr. M. Kosec, Dr. M. Trontelj and Prof. Dr. D. Kolar and D. Ročak from the Institute Jožef Stefan in Ljubljana for helpful discussions and advice and the colleague and spouse A. Živič for encouragements and many valuable suggestions throughout this work as well as to all colleagues from KEKO for their support.

References

1. S. M. Sze, "Physics of Semiconductor Devices", Wiley, N. Y. 1981, pp.63-133

2. A.S. Grove, "Physics and Technology of Semiconductor Devices", Wiley, N. Y. 1967, pp.1-208

3. F. A. Kröger, "Chemistry of Imperfect Crystals ", Wiley, N. Y. 1974, Vol. 2, p. 752

4. D. R. Clarke, "The Microstructural Location of the Intergranular Metal RROxide Phase in a Zinc Oxide Varistor", J. Appl. Phys. 49 (4), pp. 2407- 11, 1978

5. A. T. Sauthanam, T. K. Gupta, W. G. Cavison, "Microstructural Evaluation of Microcomponent ZnO Ceramics", Appl. Phys., 50 (2), pp. 852-59, 1979

6. J. Wong, W. G. Morris, "Microstructure and Phases in Nonohmic ZnO-Bi2O3 Ceramics", Am. Cer. Soc. Bull. 53, pp.816, 1974

7. A. Lagrange, "Present and Future of Zinc Oxide Varistor", El. Cer., Ele sevier, London, 1991, pp.1-27

8. T. K. Gupta, "Application of Zinc Oxide Varistors", J. Am. Cer. Soc. 73(7), pp. 1817-1840, 1990

9. E. Olsson, G. L. Dunlop, R. Osterlund, "Interfacial Barriers to Electrical Conduction in ZnO Varistor Materials", Proc. of the Sec. int. Varistor Conf., pp.65-72, Schenectady, N. Y. Dec. 5-6, 1988

10. F. Greuter, G. Blater, M. Rossinelli, F. Stucki, " Conduction mechanism in ZnO Varistors : An Overview", Proc. of the Sec. Int. Varistor Conf., pp. 31-53, Schenectady, N. Y. Dec. 5-6, 1988

11. F. Greuter, G. Blater, "Electrical Properties of Grain Boundaries in Polycrystalline Compound Semiconductors", Semic. Sci. Technol. (5), pp. 111-137, 1990

12. L. M. Levinson, H. R. Philip, "ZnO Varistors - A Review", Cer. Bull. 65 (4), pp. 639-646, 1986

13. R. Einziger, "Metal Oxide varistors", Ann. Rev. Mater. Sci. 17, pp. 299- 321, 1989

14. G. E. Pike, "Electronic Properties of ZnO Varistors : A New Model", Mater. Res. Sci. Proc. 5, pp. 369-78, 1982

15. F. Greuter, G. Blater, "Current Control by Electrically Active grain Boundaries ", Proc. of the Int. Symp. of Polycrystalline Semiconductors - Grain boundaries and Interfaces, pp. 302-314, Malente, Germany, Avg. 29- Sept. 1988

16. N. Shohata, T. Matsumuka, K. Utsumi, T. Ohno, "Properties of Multilayer ZnO Ceramic Varistor", pp.349-358, in Advances in Ceramics, Vol. 1, Ed. L. M. Levinson, Am. Ceram. Soc., Columbus, OH, 1981

17. N. Shohata, M. Nakanishi, K. Utsumi, "Multilayer Ceramic Chip Varistor", pp.329-337 in Advances in Ceramics, Vol. 3, Ed. L. M. Levinson, Am. Ceram. Soc., Columbus, OH, 1989

18. M. Trontelj, Z. Živič, G. Dražič, Z. Samardžija, "The Microstructure of a Multilayer Varistor", Proc. of Conf. MIEL-SD'93, Bled, Sept. 1993, pp.143-148

19. Z. Živič, M. Kosec, "Properties of a 4 V Multilayer Varistor ", Proc. of Conf. MIEL-SD'92, Portorož, Sept. 1992, pp.419-424

20. Z. Živič, "Universal Composition for Varistor Production", Pat. No. 9200421, Slovene Patent Bureau, LJubljana, 1992

21. Z. Živič, "Low Leakage Current Varistor Composition", Pat. No. 9300426, Slovene Patent Bureau, Ljubljana, 1993

Zoran Živič, M.S.E.E.
KEKO, d.d.
Ceramic Capacitor Factory
Grajski Trg 15
68360 Žužemberk
Slovenia
tel. + 386 68 87 230
fax + 386 68 87 315

Prispelo (Arrived): 15.08.94 ***Sprejeto (Accepted): 20.09.94***

PLANAR LC OPTICAL SWITCH FOR OPTICAL COMMUNICATIONS

J. Pirš, S. Kopač, R. Lukač and B. Marin
Jožef Stefan Institute, Ljubljana, Slovenia

Key words: optical communications, optical switches, LC planar technology, liquid crystals, LC, nematic liquid crystals, electronical fields, refractive indexes, optical waveguides

Abstract: A planar electrooptical light switch and crossbar interconnection network specifically designed for optical fiber communications is described. It is based on the use of the homogeneously aligned nematic liquid crystals acting as the active elements for light beam splitting and redirecting. Several possibilities based on electrically controlled birefringence in nematic LC are described and the estimate on the dimensional limitations based on the calculations of the electric control field are given. The presented LC optical crossbar can be addressed electrically and can be miniaturized. This makes it particularly interesting anywhere where large number of interconnecting switching of optical light signals is required (i.e. telephone centrals,...)

Planarno tekoče kristalno optično stikalo za optične komunikacije

Ključne besede: Komunikacije optične, stikala optična, LC tehnologije planarne, LC kristali tekoči, LC kristali tekoči nematični, polja električna, količniki lomni, valovodi optični

Povzetek: Opisano je planarno tekočekristalno optično stikalo, ki je posebej primerno za optične komunikacije. Stikalo uporablja homogeno urejeno plast tekočega kristala, ki se mu z električnim poljem lahko spreminja lomni količnik - električno kontrolirana dvolomnost. Opisane so različne možnosti uporabe tega efekta v nematskih tekočih kristalih.Na osnovi izračuna električnega polja znotraj tekočekristalne celice je podana ocena maksimalnih možnih dimenzij takega optičnega stikala. Prednosti tekočekristalnega optičnega stikala so predvsem v majhnih dimenzijah in možnosti električnega krmiljenja z nizkimi napetostmi, zato je posebej zanimiv za uporabo povsod, kjer je zahtevano veliko število optičnih stikalnih elementov (npr. telefonske centrale,...)

INTRODUCTION

A number of different technical solutions using liquid crystals for switching the light signals between different optical fibers has been made so far[1,2,3,4]. They are based on different electrooptic mechanisms in liquid crystals from electrically controlled refractive index variations causing light coupling between optical waveguides[5], total light reflection[6], electrically controlled birefringence and electrically controlled light scattering[7]. Most of these solutions require the use of expensive optic elements (prisms, polarization beamsplitters,..), their construction is nonplanar and they cannot be miniaturized.

In this paper we propose a construction of an LC switching device based on the fact that LC itself can be used as a waveguide as first pointed out by Giallorenzi et al.[9] and later by M.Kawachi et al.[4]. Moreover, using a light, the electrically controlled birefringence of LC can be used to generate electrically induced light guide be-

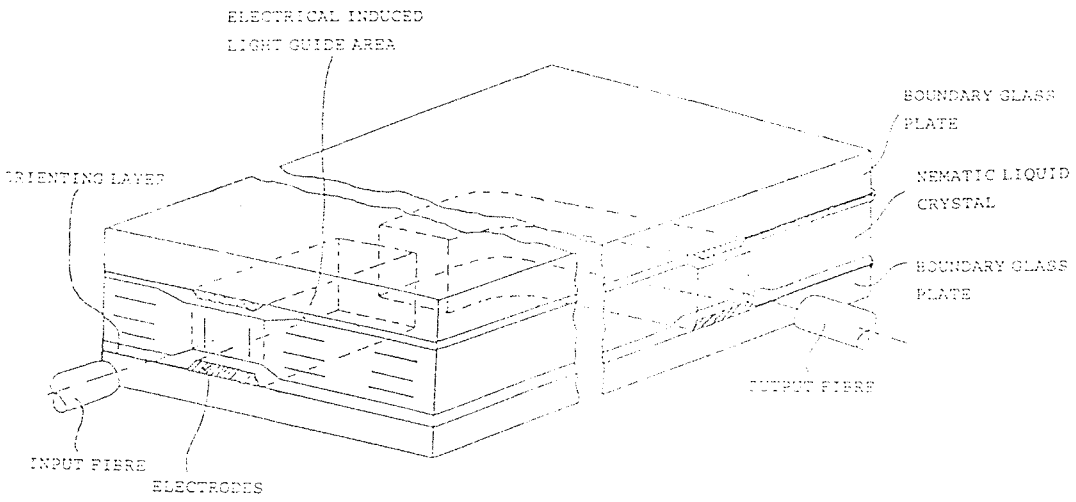


Figure 1: Schematic presentation of the electrically induced optical waveguide in the homogeneously aligned nematic LC

tween the properly shaped electrodes (see Fig. 1) in a standard, homogeneously aligned nematic LC cell.

If the polarization of the propagating light is perpendicular to the boundary glass plates of the homogeneously aligned nematic LC (positive dielectric anisotropy!) cell, than the applied electric field between the electrodes on the boundary plates causes, that the refractive index (n_e) of the LC between the electrodes becomes greater than in the area without the electrodes as well as greater than the refractive index of the boundary glass plates. So the conditions for optical waveguiding are met and an electrically induced waveguide is formed within the LC layer between the electrodes. The difference between the ordinary and extraordinary refractive index determines the numerical aperture of this waveguide and imposes the limitations on its maximum curvature.

With the appropriate design of the electrodes different electrooptical switching devices can be made consisting of several electrically induced optical LC waveguide segments. So electrooptical directional elements, crosspoints and even a complex matrix of such switches can be made (see Fig. 2, 3, 6).

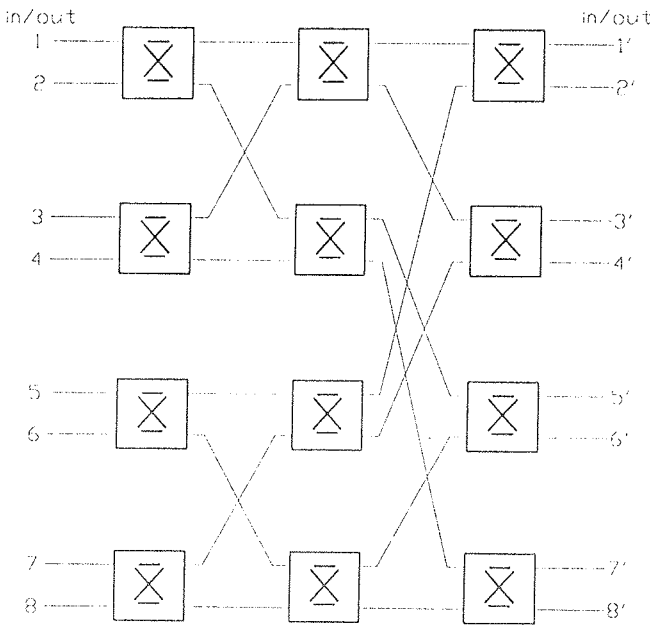


Figure 3: LC matrix 8x8 crossbar switch

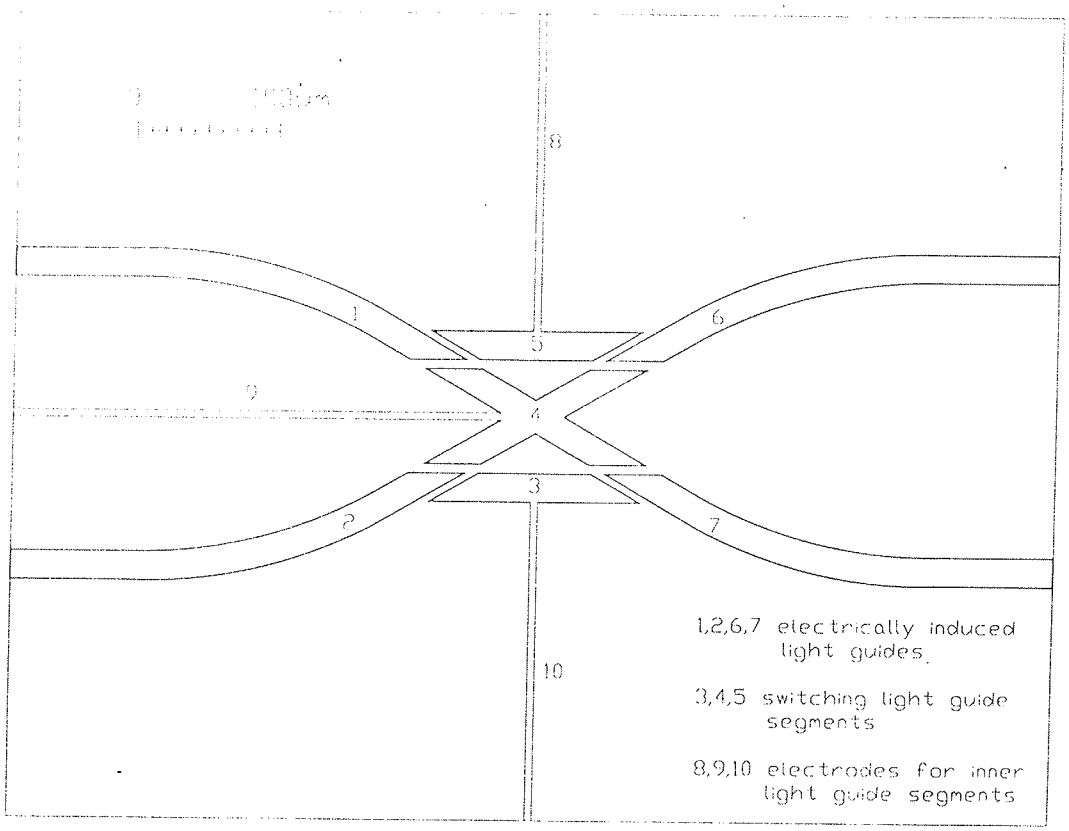


Figure 2: 2x2 Optical cross-bar switch

EXPERIMENTAL

The concept of electrically induced optical waveguide switches was verified by means of different homogeneously aligned LC cells with appropriate electrode configurations. The cells were made in a more less conventional way. ITO covered glass plates were used. After photolithografic formation of the required electrode pattern, the glasses were covered with thin Nylon orienting layer and rubbed to provide for the homogeneous orientation. Ten micron thick cells were made and filled with F.Hoffmann-La Roche nematic liquid crystal ROTN 0530 (n_o=1.513, n_e=1.718). The following electrode patterns were used:

1.Half plane electrodes - determination of the angle of total reflection (see Fig. 4a,b,c)

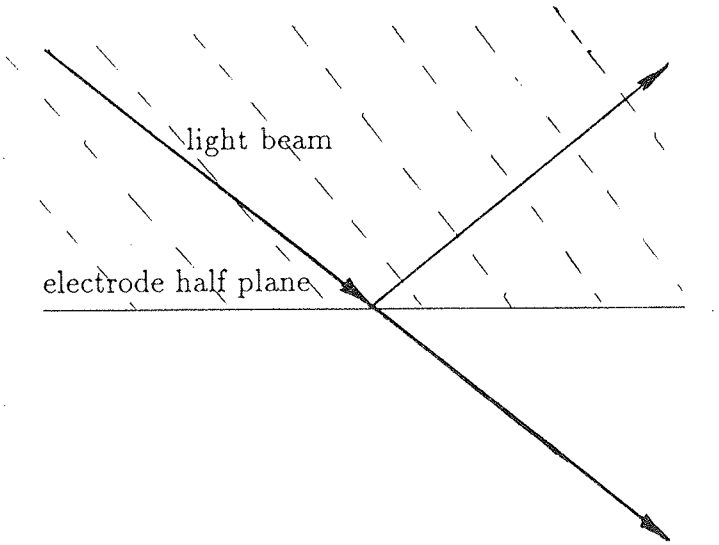
2.Straight 50-micron wide lines - basic concept of the electrically induced optical waveguide; numerical aperture determination (see Fig. 5)

3.Directional switch (see Fig. 6a,b,c) - evaluation of the switching performances, light losses, etc...

The signal light beam was simulated by a He-Ne laser that was coupled to the LC optical switch by a focusing lens and a precision x-z stage. The traveling of the light signal within the LC optical switch was monitored by observing the light scattered by the order parameter fluctuations under the low amplification microscope by means of the CCD camera coupled to a PC computer.

RESULTS AND DISCUSSIONS

The results of the evaluation of the electrically induced optical waveguide switch concept are shown on figures 4 through 6.



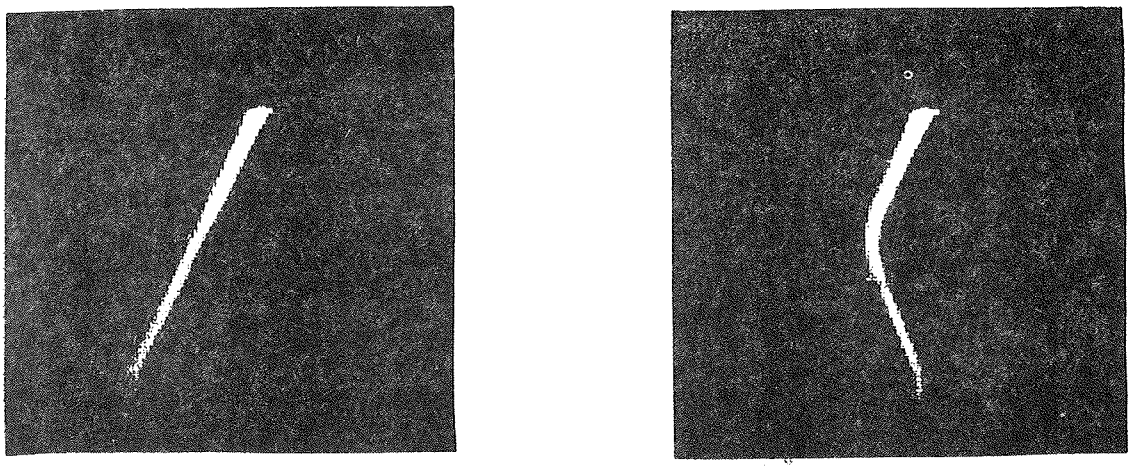


Figure 4: Signal light beam reflection on the electrically induced "refractive index barrier":
a.) Schematic presentation of the light beam and half plane electrodes
b.) Signal light beam propagation without electric field
c.) Signal light beam reflection at the electrically induced refractive index barrier

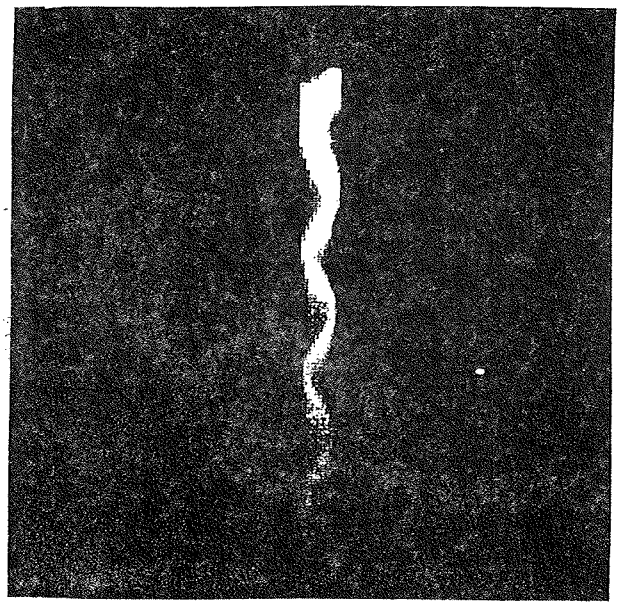


Figure 5: Electrically induced optical waveguide: the signal light beam is traveling along 50 μm wide straight LC waveguide. Since the incidence angle is different from zero but smaller than the one determined by the angle of total reflection, the light beam is reflected back and forth, but stays within the waveguide.

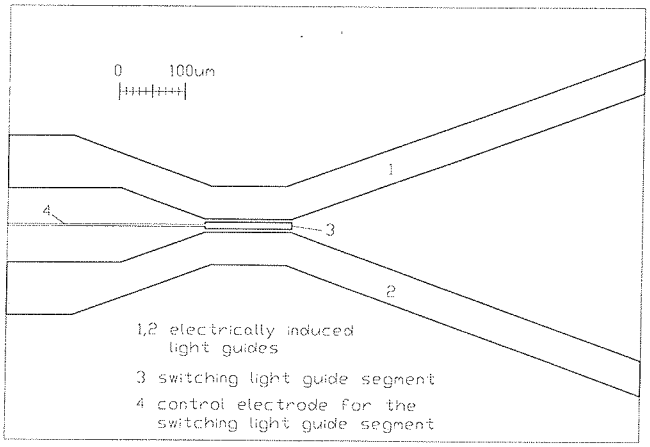
In order to evaluate the limitations and performances of this optical signal switching concept, a detailed computer analysis of the average refractive index variations based on the computer simulation of the nematic director fields within the LC optic waveguide switch was made. The refractive index was calculated for the birefringent medium according to the formula:

$$n_{ef}(\Theta) = \frac{n_e\, n_o}{\sqrt{n_o^2 + \left(n_e^2 - n_o^2\right)\sin^2\Theta}}. \qquad (1)$$

The nematic director fields were obtained as a result of the numerical solution of the relaxation equation for the director fields:

$$\gamma \frac{\partial}{\partial_t} n_i = k\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}\right) n_i + \Delta\varepsilon E_i \sum_{j=1}^{3} E_j n_j + \lambda n_i\,, \qquad (2)$$

where E is the electric field, $\Delta\varepsilon$ dielectric anisotropy and λ is a normalization constant.



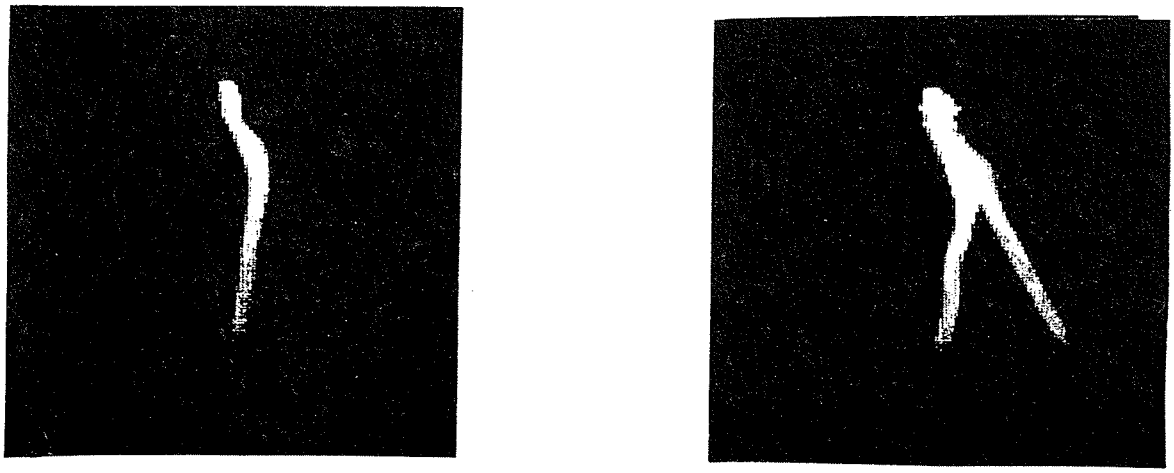


Figure 6: LC optical directional switch:
a.) Schematic presentation of the electrode pattern
b.) Signal light beam propagation with the switching segment turned off
c.) Signal light beam propagation with the switching segment turned on

This relaxation equation was coupled to the equation for the electric field:

$$E = -\text{grad}V; \quad \text{div}(\underline{\varepsilon}(x,y)\,\text{grad}V(x,y)) = 0, \qquad (3)$$

where:

$$\underline{\varepsilon} = \begin{bmatrix} \epsilon_{\perp} + \Delta\epsilon n_x^2 & \Delta\epsilon n_x n_y \\ \Delta\epsilon n_x n_y & \epsilon_{\perp} + \Delta\epsilon n_x^2 \end{bmatrix}$$

in LC and $\underline{\varepsilon} = \varepsilon_0$ outside.

Assuming strong anchoring conditions at the boundary surface, this relaxation equation was solved numerically using SOR method (Simultaneous over-relaxation)[10]. The results for a segment (Fig. 7) between two parallel electrically induced wave guides are shown on the Fig. 8 and Fig. 9.

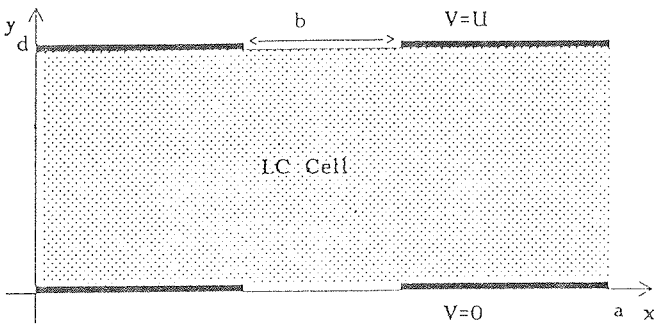


Figure 7: Shematic presentation of the waveguide segment

These results, which are also well confirmed by the experimental data (see Fig 4, 5, 6), clearly show, that:

1. The electrically induced waveguides are well separated if the electrode distances are more than two LC cell gaps apart. In this case one cannot expect much of the crosstalk between them.

2. If the electrodes are closer than one LC cell gap apart, the light signal passes from one waveguide to another almost without any light loss.

3. The switching waveguide segments of the LC light switch have to be wider than two LC cell gaps and should be located closer than one cell gap to assure good switching.

The anisotropy of the refractive index ($n_e - n_o$) in modern nematic LC materials can be as high as ≈ 0.25. This

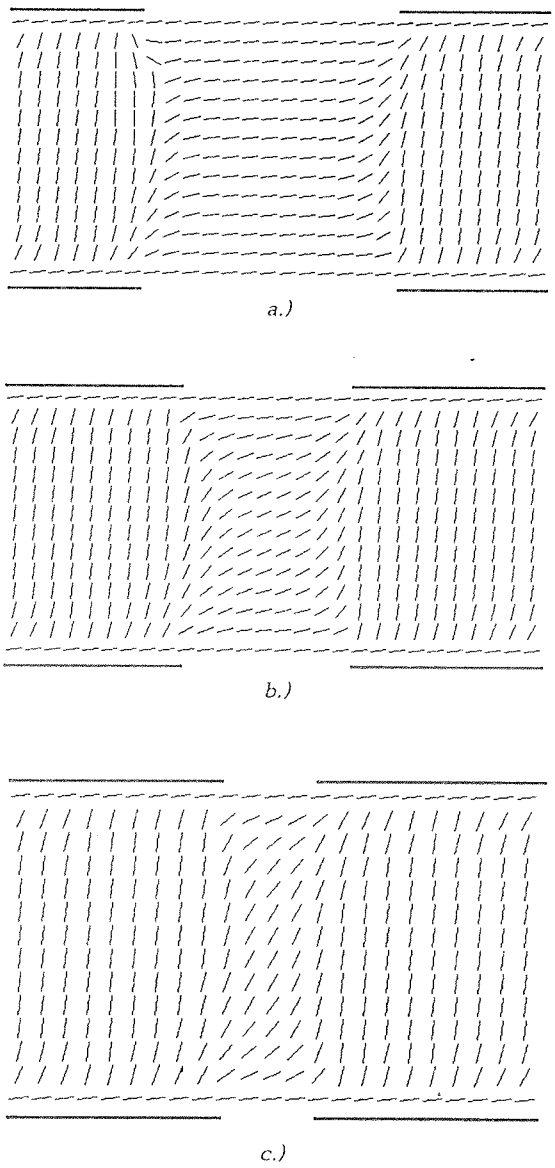


Figure 8: Plot of the director fields for different spacing of the electrodes:
a.) spacing is equal to four LC cell gap
b.) spacing is equal to two LC cell gaps
c.) spacing is equal to one LC cell gaps

imposes a limit to the maximum curvature of the electrically induced optical waveguides. So an optical crossbar switch (Fig. 2) has to be ≈ 200 μm long. Since order parameter fluctuations in nematic LC are causing relatively strong light scattering (light loss!), the area of the total optical switching array is limited to 600x600 μm. This means that the 8x8 switch array (Fig. 3) is the maximum, that one can expect from the nematic optical switches as described in this paper.

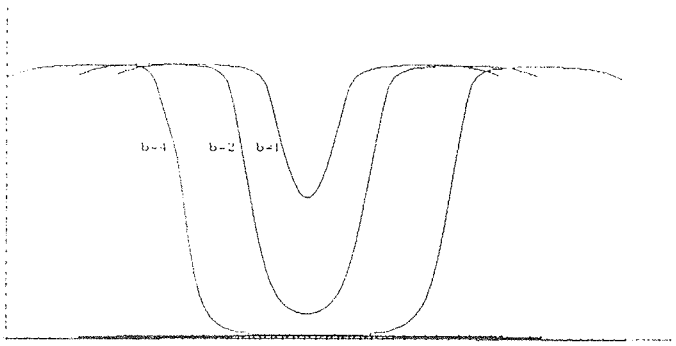


Figure 9: Plot of the refractive index between the electrodes for different electrode spacings (b): b=1 LC cell gap, b=2 LC cell gaps, b=4 LC cell gaps

REFERENCES

1. M.R.Meadows, M.A.Handschy, N.A.Clark, Appl.Phys.Lett., 54, 1394 (1989)

2. R.A.Kashnow, C.R.Stein, Appl.Opt., 12, 2309 (1973)

3. Y.Fujii, Appl.Opt. 28, 4968 (1989)

4. M.Kawachi, N.Shibata, T.Edahiro, Jap.J.Appl.Phys, 21, L162 (1982)

5. US patents: 4,720,174, 4,278,372, 4,773,136

6. US patents: 4,385,799, 4,720171, 4,737,019

7. US patents: 4,775,038, 4,478,494

8. R.Blinc, J.W.Doane, B.Marin, I.Muševič, J.Pirš, S.Pirš, S.Žumer, S.Kopač: "Liquid crystal light valve array optical cross-bar", US pat appl.# 289 476

9. Gialorenzi et al. "Liquid crystal waveguide", US Patent 3,963,310

10. W.H.Press, B.P.Flannery, S.A.Tenkolsky, W.T.Vetterling, Numerical Recipes (Cambridge Univ.Press, New York, 1989)

Janez Pirš, Samo Kopač,
Renato Lukač and Bojan Marin
Jožef Stefan Institute, Jamova 39,
61111 Ljubljana, Slovenia
tel. + 386 61 125 91 99
fax + 386 61 126 10 26

Prispelo (Arrived): 01.09.94 *Sprejeto (Accepted): 20.09.94*

SENZORJI TLAKA REALIZIRANI S POMOČJO DEBELOPLASTNE TEHNOLOGIJE

S. Šoba, D. Belavič, M. Hrovat*, B. Pavlin, A. Simončič
Iskra Hipot d.o.o., Šentjernej, Slovenija
* Institut Jožef Stefan, Ljubljana, Slovenija

Ključne besede: senzorji tlaka, senzorji piezoupornostni, senzorji industrijski, mikroelektronika, tehnologije debeloplastne, pretvorniki tlaka, senzorji multipleksni, NTC termistorji, inovacije tehnološke, doravnavanje, doravnavanje lasersko, tolerance ozke

Povzetek: Zastavljeni namenski cilj razvojnega projekta - povečanje tržnega deleža na področju senzorjev tlaka - je dosežen. Razvili smo skupino industrijskih senzorjev tlaka. Posebej bi omenili multiplex senzor in družino senzorjev ter pretvornikov za različna tlačna področja. Poleg tega smo osvojili različna znanja in razvili nove tehnološke postopke, ki so uporabni tudi za druge izdelke. Poudarili bi tehnološke inovacije pri debeloplastnem senzorju sile, doravnavanju debeloplastnih NTC termistorjev do ozkih toleranc in zapiranja mehansko občutljivih debeloplastnih vezij v plastična ohišja.

Pressure Sensors Realized by Thick Film Technology

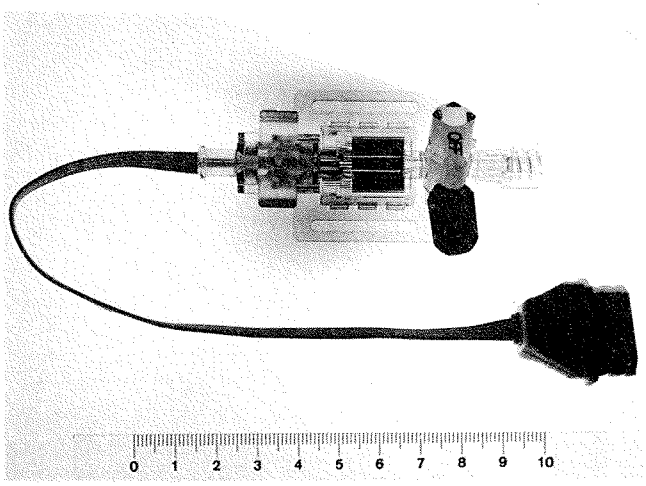
Keywords: pressure sensors, piezoresistive sensors, industrial sensors, microelectronics, thick film technologies, pressure transducers, multiplex sensors, NTC termistors, techological innovations, trimming, laser trimming, narrow tolerances

Abstract: The purpose of research and development project - an increased pressure sensor market share - has been achieved. The group of industrial pressure sensors (multiplex sensor, the family of sensors and transducers for different pressure etc.) was developed. The various "know-how" were acquired and new technological processes usable also on other fields, have been developed. As examples thick film strain gauge, laser trimming of thick film NTC thermistors to narrow tolerances and encapsulation of stress sensitive thick film circuits could be mentioned.

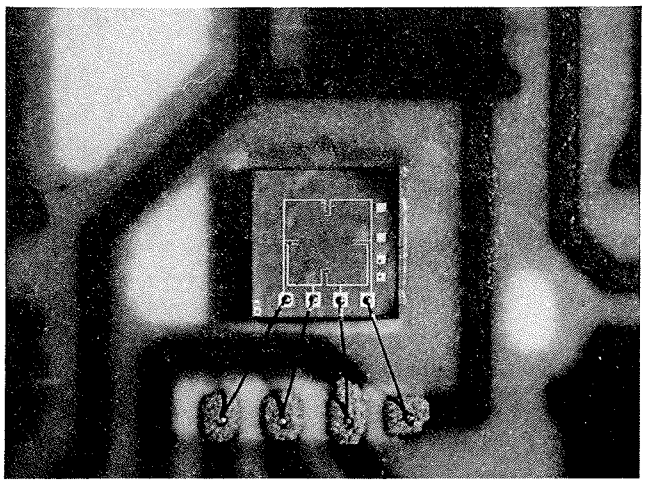
Uvod

V letih 1991 - 1993 je potekal projekt "Senzorji tlaka realizirani s pomočjo debeloplastne tehnologije", ki ga je z 20% deležem sofinanciralo Ministrstvo za znanost in tehnologijo Republike Slovenije. Naročnik projekta je bila ISKRA HIPOT, Tovarna elektronskih elementov in opreme, d.o.o., Šentjernej, Trubarjeva 7, izvajalci projekta pa Institut Jožef Stefan in Iskra Razvojno raziskovalni inštitut IEZE RO HYB Šentjernej ISKRE HIPOT. Projekt je bil zastavljen na podlagi uspešne realizacije in redne velikoserijske proizvodnje senzorja za merjenje krvnega tlaka za enkratno uporabo (slika 1).

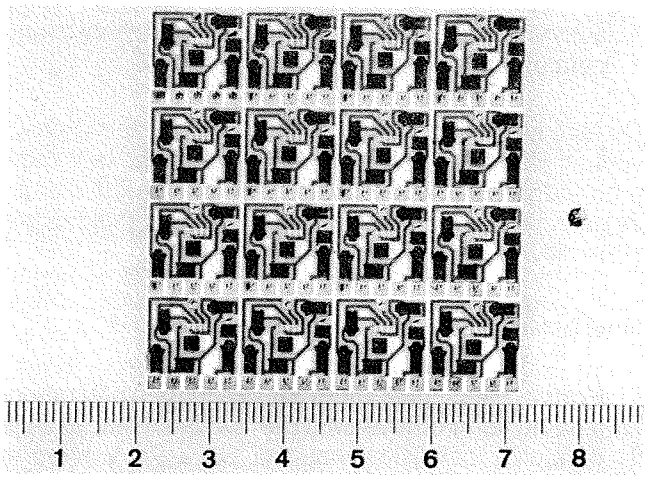
Omenjeni senzor je aplikacija piezoupornostnega silicijevega senzorja tlaka (slika 2) na debeloplastnem kompenzacijskem vezju, narejenem na keramičnem substratu (slika 3). Dobro obvladovanje proizvodnje senzorja krvnega tlaka je dajalo utemeljeno podlago za razmišljanje o uporabi podobne in še bolj dodelane tehnologije za razvoj novih izdelkov s področja senzorjev tlaka. Zastavljen je bil projekt, čigar končni cilj je bil



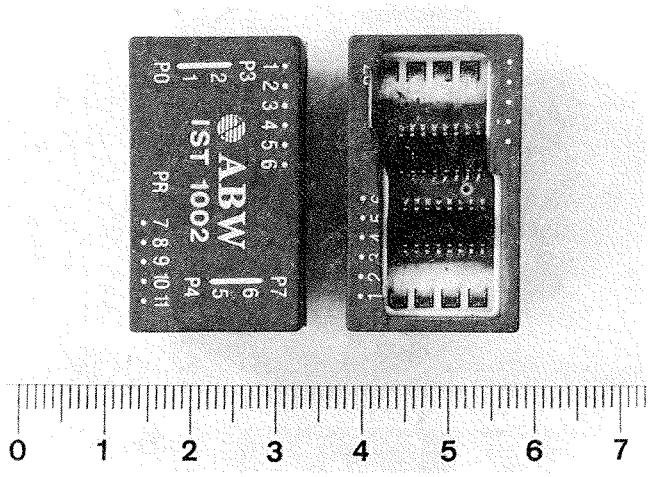
Slika 1: Senzor za merjenje krvnega tlaka za enkratno uporabo



Slika 2: Piezoupornostni silicijev senzor tlaka na debeloplastnem kompenzacijskem vezju



Slika 3: Keramična ploščica s 16 piezoupornostnimi silicijevimi senzorji tlaka na debelo- plastnem kompenzacijskem vezju



Slika 4: Multiplex senzor (modul z 8 silicijevimi senzorji tlaka za tlačno področje do 1 bar in dvema 4-kanalnima CMOS multiplexerjema)

razširiti tržni delež na področju senzorjev tlaka. Na podlagi analize trga smo se odločili za naslednje segmentne cilje projekta:

- industrijski senzorji in pretvorniki z uporabo debeloplastne tehnologije
- kompenzirani senzorji tlaka za uporabo v procesni industriji v različnih izvedbah
- aplikacije senzorjev in pretvornikov za uporabniška vezja
- debeloplastni senzor sile z različnimi aplikacijami
- medicinski senzorji tlaka (možganski senzor tlaka, senzor krvnega tlaka nove generacije

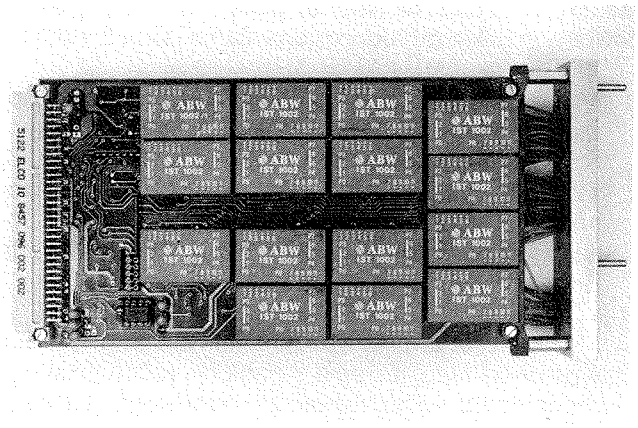
Predstavljamo rezultate raziskovalnega dela, ki se kažejo v *osvojitvi novih trgov, novih proizvodih in novih proizvodnih postopkih, tehnoloških inovacijah in patentih.*

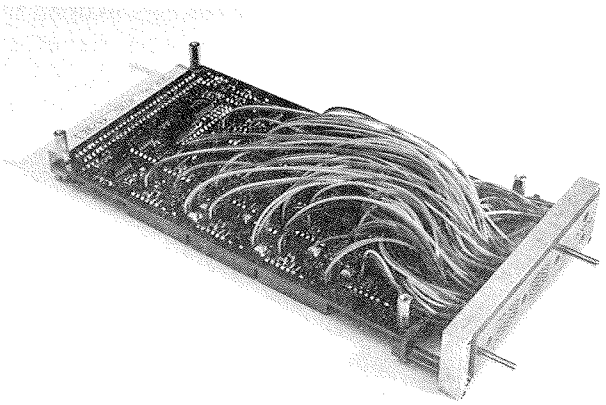
Predstavitev rezultatov projekta

Rezultate projekta lahko uvrstimo v tri skupine glede na doseženo stopnjo uporabe in prenosa v proizvodnjo. V prvi skupini predstavljamo raziskovalne dosežke iz vseh segmentnih ciljev projekta, ki so prišli v redno proizvodnjo in ki jih uspešno tržimo. S temi izdelki je bila dosežena

Osvojitev novih trgov

Na področju **industrijskih senzorjev** je bil za proizvod multiplex senzor narejen kompleten razvoj proizvoda od ideje do tržne realizacije. Proizvod je v redni proizvodnji. Multiplex senzor je aplikacijsko vezje, ki se sestoji iz 8 silicijevih senzorjev tlaka za tlačno področje do 1 bar in dveh 4-kanalnih CMOS multiplexerjev (slika 4). Namenjen je uporabi v sistemu, kjer je potrebno hitro preletavanje točk merjenega pritiska. Krmiljenje (CMOS logika) in kompenzacija

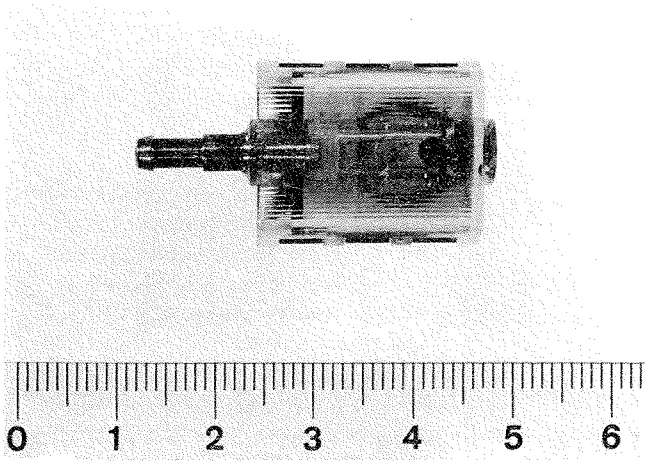




Slika 5,6: Plošča s 15 moduli multiplex senzor s skupno 120 senzorji tlaka; plošča vključno z vsemi cevkami in priključki

merjenih vrednosti iz senzorjev se opravlja računalniško oz. mikroprocesorsko.

Za kupca smo razvili tudi ploščo s tiskanim vezjem, na katerem je 15 modulov multiplex senzor s skupno 120 senzorji tlaka. Tiskano vezje je načrtovano tako, da

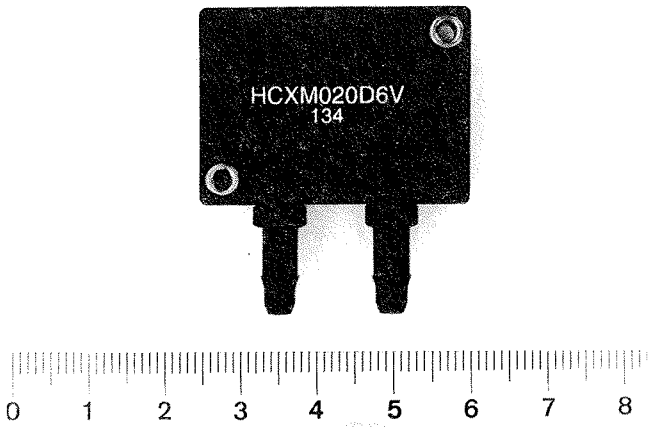


Slika 7: Senzor tlaka za diferencialni tlak 0-1bar oz. 0-5bar

omogoča hitro preletavanje vseh senzorjev in zapis meritev v računalnik. Tudi to ploščo vključno z vsemi cevkami in priključki redno proizvajamo (slika 5, slika 6).

Na področju **kompenziranih senzorjev** *tlaka* za uporabo v procesni industriji je v redni proizvodnji senzor tlaka za diferencialni tlak 0-1bar oz. 0-5bar (slika 7). Gre za sorazmerno cenen kompenzirani senzor narejen iz podobnih materialov kot velikoserijski senzor krvnega tlaka. Senzorski element tega senzorja je na sliki 2.

Med **kompenziranimi pretvorniki tlaka** za uporabo v procesni industriji smo s pomočjo računalniškega modeliranja vezja razvili za nemškega partnerja družino pretvornikov tlaka v tlačnem področju 20mbar - 5bar (20mbar, 50mbar, 100mbar, 350mbar, 1bar, 2bar, 5bar - vsi relativni in 1bar absolutni). Vsi pretvorniki so v redni proizvodnji (slika 8). Skupna za vse pretvornike je enaka napajalna napetost (najmanj 4.8V) in enak električni odziv (0.5 - 4.5V) glede na izbrano tlačno področje in majhno ter robustno ohišje. Vsi pretvorniki so kompenzirani v temperaturnem področju 0 - 70°C.

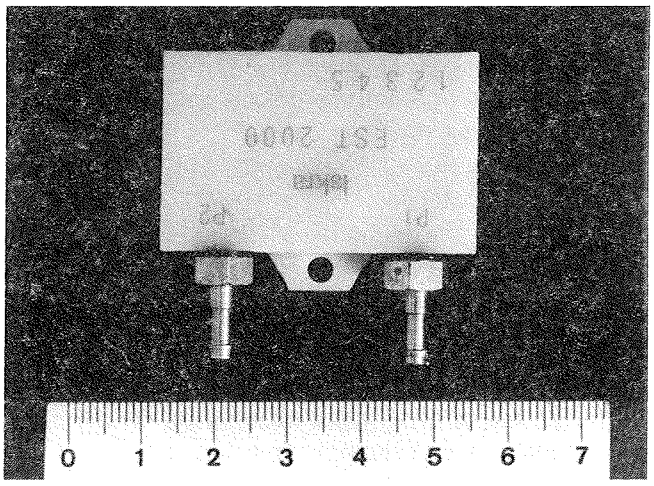


Slika 8: Družina pretvornikov tlaka v tlačnem področju 20mbar - 5bar (20mbar, 50mbar, 100mbar, 350mbar, 1bar, 2bar, 5bar - vsi relativni in 1bar absolutni)

Od faze ideje do prototipa so bili razviti naslednji proizvodi, ki jih iz različnih razlogov zaenkrat še ni v redni proizvodnji, nekatere rezultate iz razvoja teh izdelkov pa že uporabljamo v drugih proizvodih iz redne proizvodnje senzorjev.

Novi proizvodi in novi proizvodni postopki

Pretvornik tlaka 0-150mbar je podoben prej omenjenemu kompenziranemu pretvorniku tlaka, le da je narejen s cenejšimi materiali (slika 9). V njem je uporabljen senzor, ki ga uporabljamo za velikoserijsko proizvodnjo krvnega tlaka. Namenjen je uporabi v izdelku za trg široke potrošnje.



Slika 9: Pretvornik tlaka 0-150mbar

V okviru projekta smo imeli nalogo razviti tudi *senzor sile* za tehtnico z merilnim obsegom od 10 g do 3 kg in točnostjo +-2% polnega obsega. Glede na zahteve smo razvili in izdelali prototipe senzorja sile ter jih testirali in izmerili njihove lastnosti.

Medicinski senzor tlaka - nova verzija glede na obstoječega v redni proizvodnji. Za ta senzor so bila v sodelovanju z domačim partnerjem razvita vsa orodja za ohišje, izboljšani pa so bili postopki zapiranja mehansko občutljivega senzorskega dela.

Možganski senzor tlaka - z miniaturnim silicijevim senzorjem v kovinskem ohišju. Namen pri tem senzorju je bil ohraniti čim več dobrih lastnosti senzorja krvnega tlaka ob hkratni maksimalni miniaturizaciji vezja.

V toku izvajanja projekta je prišlo do razvoja več tehnološko različnih postopkov, ki predstavljajo

Tehnološke inovacije

tehnologija izdelave relativnih kompenziranih senzorjev tlaka v področju pritiskov 100 - 5000 mbar, 0

-70°C v debeloplastni tehnologiji z uporabo piezoupornostnega silicijevega senzorja tlaka;

tehnologija izdelave pretvornikov tlaka v področju pritiskov 20 - 5000 mbar, 0 -70°C, v debeloplastni tehnologiji, z različnimi aktivnimi izhodi (0-5V, 0-12V, 4-20mA, itd.);

tehnologija zapiranja mehansko občutljivih debeloplastnih vezij v plastično ohišje;

tehnologija izdelave medicinsko atestiranega konektorja in kalibracijske tipke na medicinskem senzorju tlaka za enkratno uporabo;

patentiran postopek laserskega doravnavanja debeloplastnih NTC termistorjev do ozkih toleranc;

tehnologija izdelave senzorja sile na osnovi piezoupornostnega efekta debeloplastnih uporov z dopustno deformacijo 1000 μm/m. Možne so aplikacije elementa senzorja sile za merilno področje od 10g - 500kg (odvisno od nosilnega elementa) oz. za meritev pritiska od 1 bar navzgor, odvisno od dimenzij membrane.

ZAKLJUČEK

Zastavljeni cilj projekta - povečanje tržnega deleža na področju senzorjev tlaka - je dosežen. Na področju medicinskih senzorjev smo najmanj ohranili tržni delež navkljub povečani konkurenci. Uspešno pa smo vstopili v trg industrijskih senzorjev, za večji prodor na ta trg pa moramo vzpostaviti redno velikoserijsko proizvodnjo industrijskih senzorjev, kar planiramo za leto 1995. Naročila za te senzorje že imamo.

Rezultati projekta so plod skupnega dela raziskovalnega dela raziskovalcev Instituta Jožef Stefan, Iskra RRI IEZE RO HYB in ISKRA HIPOT Tovarna hibridnih vezij,d.o.o. Del rezultatov je že prenešen v proizvodnjo, del rezultatov je pripravljen za prenos v proizvodnjo. Prenos rezultatov v proizvodnjo je delo raziskovalcev Iskre Hipot.

BIBLIOGRAFIJA

Objave:

Marko Hrovat, Darko Belavič, Aleš Markošek, Slavko Bernik, "Lastnosti" kombinacij NTC in debeloplastnih uporovnih past, IJS delovno poročilo, DP- 6284, 1991

Marko Hrovat, Darko Belavič, Stojan Šoba, Aleš Markošek, Thick film resistor materials for strain gauges, Proc. 20th Int. Conf. on Microelectronics / 28th Symp. on Devices and Materials MIEL-SD 92, Portorož, 1992, 343-348

Marko Hrovat, Darko Belavič, Aleš Markošek, Characteristics of thick film NTC/resistors combinations, Proc. 20th Int. Conf. on Microelectronics / 28th Symp. on Devices and Materials MIEL-SD 92, Portorož, 1992, 355-358

Marko Hrovat, Darko Belavič, Aleš Markošek, Overlapping of thick film NTC thermistors and resistors: a way to optimise laser trimming of narrow tolerance NTC thermistors, Hybrid Circuits, (32), (1993), 16-20

Marko Hrovat, Darko Belavič, Stojan Šoba, Thick film resistors for strain gauges fired on multilayer dielectrics, Proc. 21st Int. Conf. Microelectronics MIEL-93 / 29th Symp. on Devices and Materials SD-93, Bled, 1993, 91-95

Marko Hrovat, Darko Belavič, Silvo Mojstrovič, A new approach to laser trimming of thick film NTC thermistors, Proc. 21st Int. Conf. Microelectronics MIEL-93 / 29th Symp. on Devices and Materials SD-93, Bled, 1993, 97-101

Patent:
Marko Hrovat, Darko Belavič, Aleš Markošek, Postopek laserskega doravnavanja debeloplastnih NTC termistorjev do ozkih toleranc pod 1%, Št. patenta P - 8300417

Stojan Šoba, dipl. ing.
Darko Belavič, dipl. ing.
Božidar Pavlin, ing.
Alojz Simončič
Iskra Hipot d.o.o.
68310 Šentjernej
Tel.: +68 42020, Fax +68 42 370

dr. Marko Hrovat, dipl. ing.
Institut Jožef Stefan
61000 Ljubljana, Jamova 39
Tel.: +61 1259 199, Fax.: +61 219 385

Prispelo (Arrived): 01.09.94 ***Sprejeto (Accepted): 20.09.94***

TESTNE KARTICE - POMEMBEN DEJAVNIK PRI TESTIRANJU DANAŠNJIH KOMPLEKSNIH MIKROELEKTRONSKIH VEZIJ

Z. Bele
MIKROIKS d.o.o., Ljubljana, Slovenija

Ključne besede: mikroelektronika, vezja mikroelektronska, IC vezja integrirana, preskušanje vezij, kartice preskusne, BLADE kartice preskusne, EPOXY kartice testne, sonde preskusne, konice sond, impedance karakteristične, prilagajanje impedanc, rezine polprevodniške, preskušanje rezin, vernost signalov

Povzetek: Članek podaja problematiko testnih kartic pri testiranju kompleksnih mikroelektronskih vezij in osnovne značilnosti obeh izdelavnih tehnologij.

Probe Cards - an Essential Factor in Testing of Today's Complex Integrated Circuits

Key words: microeletronics, microelectronic circuits, integrated circuits, IC, circuit testing, testing cards, BLADE testing cards, EPOXY testing cards, testing probes, probe needles, characteristic impedances, impedance matching, semiconductor wafers, wafer testing, signal fidelity

Abstract: In the paper, main technical characteristics,advantages and disadvantages of two main probe card types are presented. BLADE probe cards are more robust while EPOXY probe cards are less susceptible to different noise, their characteristic impedance can be easier matched, as well as they can be built with more pins.
Company MIKROIKS d.o.o. is a manufacturer of BLADE and EPOXY type probe cards. At the same time these probe cards are used in its test center for R&D and production testing of LSI and VLSI integrated circuits on silicon wafers.

UVOD

Testne kartice postajajo, čeprav velikokrat neupravičeno zapostavljene, bolj in bolj ključnega pomena pri testiranju današnjih kompleksnih mikroelektronskih vezij, ko se le-ta nahajajo še na rezini. S hitrim naraščanjem stopnje integracije in hitrosti delovanja teh vezij, postaja obvladovanje izdelave in ustreznega vzdrževanja testnih kartic imperativ, če želimo zagotoviti zares kvalitetno testiranje mikroelektronskih vezij na rezini. Tega se zavedamo tudi v podjetju Mikroiks, ki v svojem Testnem centru v Stegnah obvladuje tako tehnologijo izdelave obeh tipov testnih kartic (BLADE, EPOXY), kot njihovo vzdrževanje in uporabo tako za lastne potrebe kot tudi za zunanje naročnike.

OSNOVNI PARAMETRI TESTNIH KARTIC

Osnovni parametri testnih kartic so:

- tip testne katice
- vernost signala
- šum na napajalnih sponkah
- vrsta materiala konic
- pritisk konic na kontaktne blazinice in sila na konico
- kontaktna upornost

Tip testne kartice

V splošnem ločimo dva tipa testnih kartic: BLADE in EPOXY.

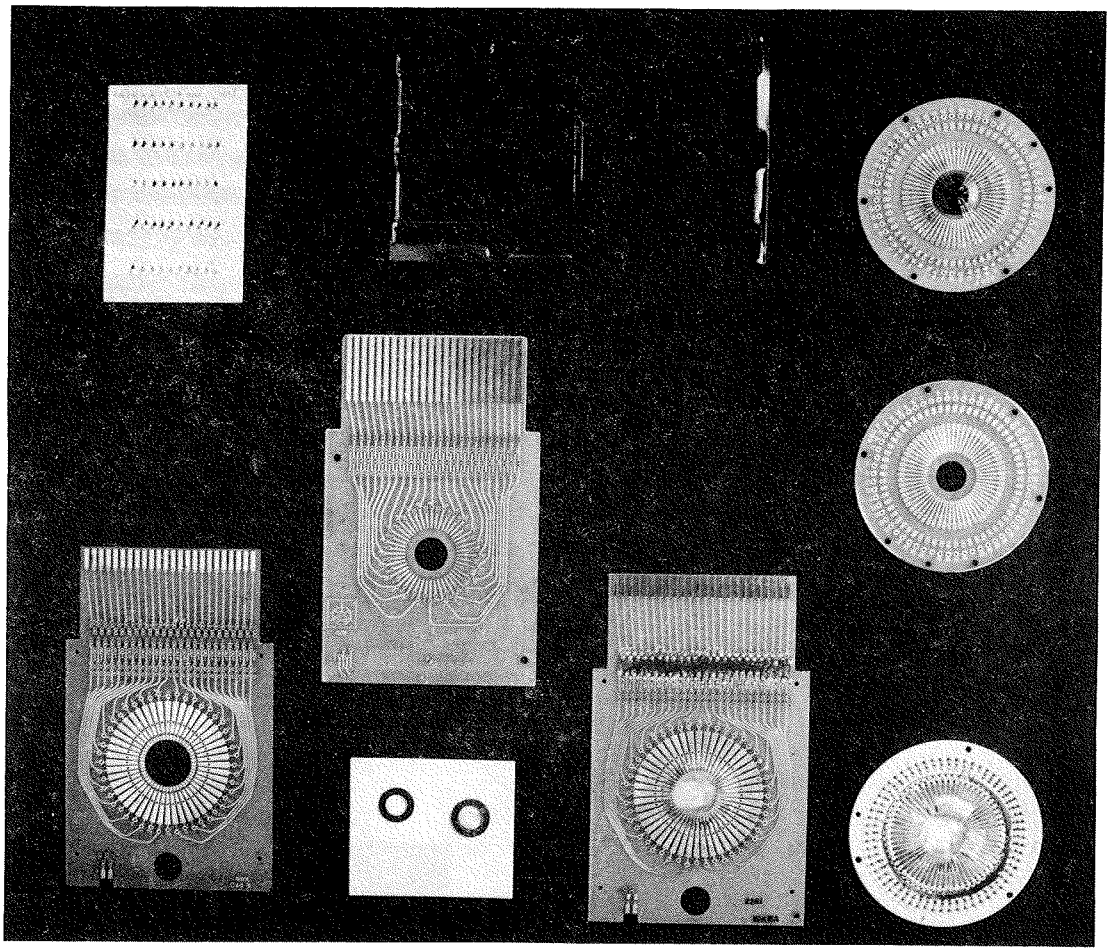
Testne kartice obeh tipov, ki jih izdelujemo v Testnem centru Mikroiks in njihovi sestavni deli so prikazani na sliki 1.

Pri testnih karticah tipa BLADE gre za posebno oblikovane konice, ki se posamično prispajkajo na nosilno tiskano ploščico, seveda tako, da s predpisano silo sedejo točno na kontaktne blazinice mikroelektronskega vezja, ki ga testiramo. Pri karticah tipa EPOXY pa najprej konice, ki imajo obliko navadnih iglic na koncih ustrezno ukrivimo in nato pritrdimo na poseben obroček z epoxy lepilom. Tudi pri teh morajo seveda biti konice zelo natančno pozicionirane na kontaktne blazinice testiranega vezja.

V zadnjem času vedno bolj prevladujejo testne kartice tipa EPOXY zaradi nekaterih bistvenih prednosti, ki jih imajo v primerjavi s karticami tipa BLADE, kot so:

- bistveno manjša susceptibilnost za motnje. BLADE konice namreč delujejo kot majhne antene, ki sprejemajo RF šum tako od svetilnih teles kot raznih instrumentov in podobno. Še pomembneje pa je, da so kapacitivnosti med prevodnimi linijami na tiskani ploščici za BLADE testne kartice tudi do 1.5-krat

Informacije MIDEM 24(1994)3, str. 182-186



Slika 1: Testne kartice tipa BLADE in EPOXY

večje kot pri EPOXY kartici in to še merjeno brez pritrjenih konic.

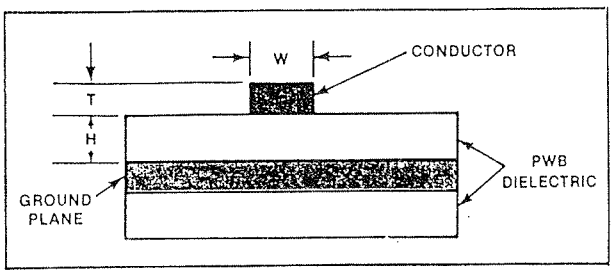
- možnost prilagoditve impedanc. Zaradi neuniformne širine prevodnih linij pri BLADE karticah je prilagoditev impedanc pri teh karticah praktično nemogoča.
- EPOXY testne kartice potrebujejo bistveno manj opreme za popravilo in vzdrževanje (za BLADE testne kartice potrebujemo npr. posebno postajo).
- bistveno večja gostota konic. BLADE kartice so omejene na maksimalno 60 konic, pretežno zaradi prostorskih omejitev pa tudi upogibanja same tiskane ploščice.
- z EPOXY testnimi karticami je moč testirati vezja s precej bolj kompleksnimi vzorci kontaktnih blazinic.
- večja stabilnost samih konic.

Kljub temu pa imajo predvsem zaradi fleksibilnosti izdelave in lažjega vzdrževanja v posameznih primerih prednost testne kartice tipa BLADE.

Vernost signala

Testna kartica ima zelo pomemben vpliv na vernost signala med testnim sistemom in testiranim mikroelektronskim vezjem. Prvi moment je vsekakor impedančna usklajenost oz. neusklajenost med testno kartico in testnim sistemom, kar lahko povzroči refleksijo signala. Refleksija signala na adresnih in/ali urinih sponkah pa lahko povzroči, da testni sistem merjeno vezje izloči kot slabo. Amplituda reflektiranega signala je odvisna od velikosti neusklajenosti karakteristične impedance med testnim sistemom in testno kartico ter frekvence oz. frekvenčne vsebine signala. Glede na to, da gre razvoj mikroelektronskih vezij v smeri vedno hitrejših vezij, postaja ta problem akutnejši, rešitev pa je v čim večji usklajenosti karakterističnih impedanc testnega sistema in testne kartice. Karakteristična impedanca Z_0 prevodne linije na testni kartici je odvisna od dimenzij te linije (višina, širina), oddaljenosti linije od ozemljitvene površine in dielektrične konstante osnovnega materiala (glej sliko 2 !).

Odvisnost karakteristične impedance in kapacitivnosti med prevodno linijo in ozemljitveno površino od širine prevodne linije prikazujeta sliki 3 in 4. Iz omenjenih

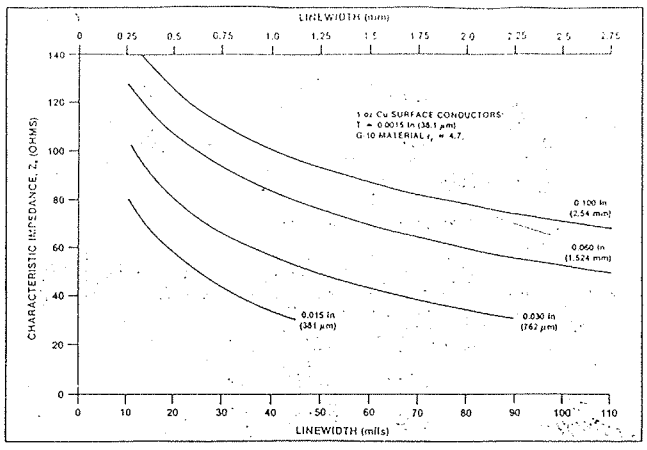


$$Z_0 = \frac{87}{\left[\varepsilon_r + 1.41\right]^{1/2}} \ln\left[\frac{5.98\,H}{0.8\,W + T}\right]$$

kjer so:

Z_0 ... Karakteristična impedanca v ohmih
ε_r ... dielektrična konstanta osn. materiala (PWB)
W,H,T ... dimenzije prevodne linije

Slika 2: Karakteristična impedanca prevodne linije na tiskani ploščici

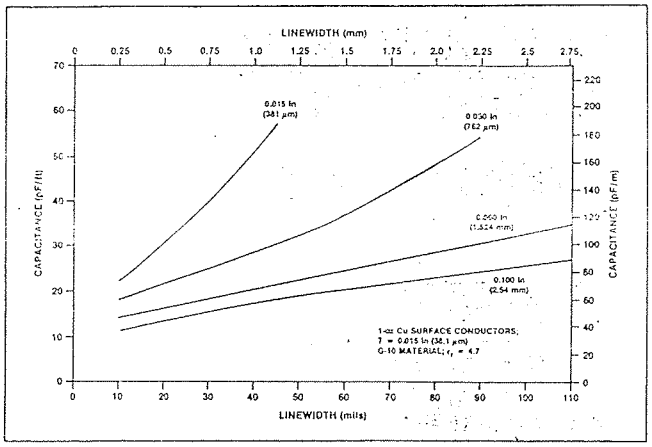


Slika 3: Karakteristična impedanca kot funkcija širine linije, $\varepsilon_r = 4.7$, $T = 38.1\ \mu m$

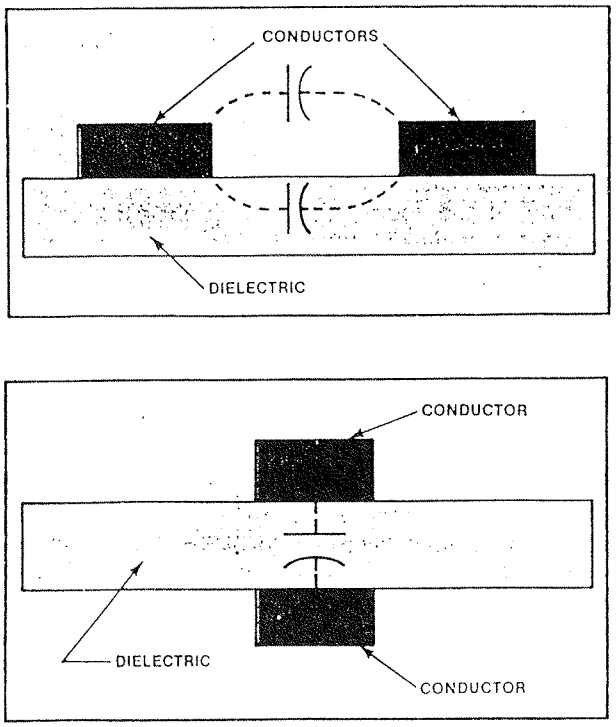
krivulj lahko enostavno določimo potrebne parametre za določeno karakteristično impedanco.

Drugi degradacijski faktor za vernost signala je vsekakor presluh med dvema prevodnima linijama, bodisi sosednjima ali prekrivajočima, zaradi kapacitivne povezave, kot je to prikazano na sliki 5.

Presluh med prekrivajočima linijama lahko učinkovito znižamo ali celo odpravimo z vmesno ozemljitveno



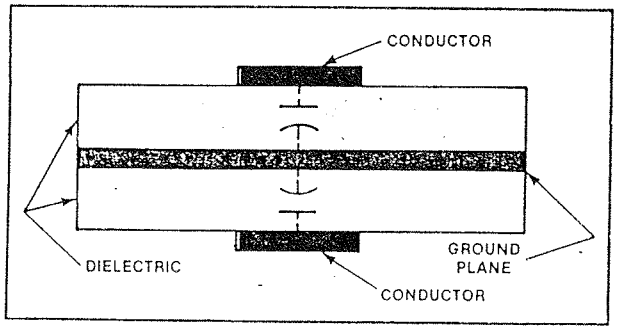
Slika 4: Kapacitivnost med prevodno linijo in ozemljitveno površino kot funkcija širine prevodne linije, $\varepsilon_r = 4.7$, $T = 38.1\ \mu m$

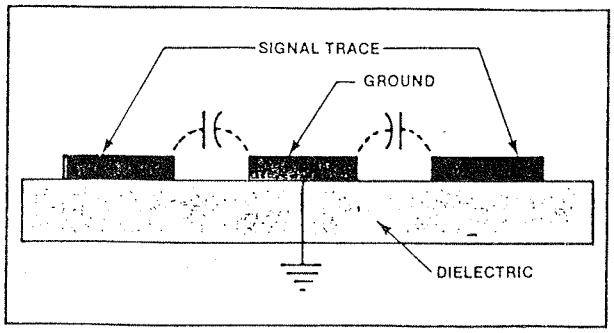


Slika 5: Kapacitivna povezava med sosednjima linijama (zgoraj) in prekrivajočima se linijama (spodaj)

površino, katera tudi precej poenostavi impedančno prilagoditev in zmanjša prehodne efekte na ozemljitveni sponki (slika 6 zgoraj).

Stranski presluh med sosednjima linijama pa lahko zmanjšamo, če povečamo (čim bolj je možno) razdaljo med obema linijama, ali še bolje, če med vsako signalno linijo vstavimo še ozemljitveno linijo (slika 6 spodaj).





Slika 6: Odprava presluha med linijama

Seveda sta obe rešitvi prostorsko omejeni.

Najboljši učinek pa seveda dosežemo s kombinacijo prve in tretje rešitve.

Šum na napajalni in ozemljitveni sponki

V splošnem je ta problem najteže rešljiv, vsekakor pa je eden najpomembnejših. Šum je večji, čim večja je hitrost vezja. Pri današnjih vezjih pa gre trend ravno v tej smeri. Primer vezij, pri katerih je ta problem še poudarjen so npr. dinamična spominska vezja, pri katerih je generacija šuma pogojena predvem z nabijanjen in praznenjem notranjih kapacitivnosti. Pri teh vezij lahko opazimo tudi zelo hitre tokovne konice reda nekaj 100 mA na napajalni in ozemljitveni sponki, kar vsekakor pomeni precejšnja nihanja napajalnih napetosti v vezju.

Poleg primernega načrtovanja izdelave testne kartice pa je relativno enostaven način odprave šuma na napajalnih sponkah uporaba "bypass" kondenzatorja. Vrednost takega kondenzatorja je izkustveno v območju med 0.001 in 0.1 μF, njegovo točno vrednost pa je najbolje določiti na podlagi opazovanja signala in efekta "bypass" kondenzatorja na širokopasovnem osciloskopu.

Vrsta materiala za konice

Konice za testne kartice so v splošnem iz treh vrst materiala: volframa, zlitine baker-berilij (Cu-Be) ali paladija. Daleč največ uporabljan material je volfram, ki ima nekaj pomembnih prednosti nasproti Cu-Be in paladiju. Predvsem je izredno odporen proti oksidiranju in zelo trden, kar pomeni daljšo življensko dobo konic. Njegova največja pomankljivost pa je v relativno visoki kontaktni upornosti. Volframova konica zaradi svoje strukture med testiranjem "pobira" silicijev oksid s kontaktnih blazinic tako, da lahko kontaktna upornost preseže 5 ohmov, kar lahko občutno vpliva na kvaliteto testiranja in seveda izplen rezine. Nasprotno ima Cu-Be izredno nizko osnovno kontaktno upornost, ki pa se praktično ohranja med testiranjem, saj se silicijev oksid nanj ne prijemlje. Je pa bistveno mehkejši kot volfram, kar pomeni, da potrebujejo testne kartice s konicami iz tega materiala več vzdrževalnih posegov pa tudi njihova življenska doba je precej krajša. Po drugi strani pa je to moč kompenzirati z večjim in ponovljivejšim izplenom na račun nižje kontaktne upornosti.

Pritisk na kontaktne blazinice in sila na konico

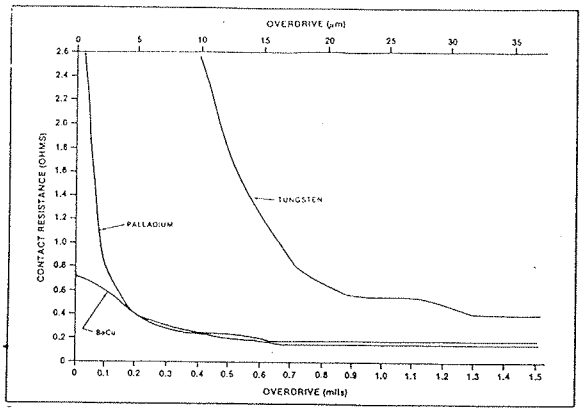
Pritisk na kontaktne blazinice ima vsekakor velik vpliv na izplen pri testiranju. Od njega je odvisno, kako dober kontakt ustvarimo med konico in kontaktno blazinico, pri tem pa ne sme priti do morebitnega preboja zelo tanke aluminijeve plasti, ki tvori kontaktno blazinico. Velikost pritiska določata tako dodatni pomik mizice navzgor (overtravel) od točke, ko konice dotaknejo rezino, kakor tudi površina oz. premer same konice.

Sila na samo konico pa je odvisna od vrste materiala iz katerega je konica, dolžine vrha konice in dodatnega pomika.

Kontaktna upornost

Kot že rečeno, kontaktna upornost je predvsem odvisna od vrste materiala iz katerega je konica in dodatnega pomika (overtravel). Pri tem je seveda dodatni pomik omejen, saj če je prevelik poškoduje površino kontaktne blazinice, zaradi upogibanja pa lahko konica celo zleze izven kontaktne blazinice.

Obstajajo posebni izračuni, s pomočjo katerih je moč kar se da točno določiti potrebni dodatni pomik, ki je običajno med 50μm in 100μm.



Slika 7: Odvisnost kontaktne upornosti od dodatnega vertikalnega pomika mizice

Odvisnost kontaktne upornosti od dodatnega pomika za tipično konico premera 50μm in dolžine 500μm podaja slika 7.

Osnovne značilnosti tehnologij izdelave testnih kartic v Testnem centru Mikroiks

Osnovne značilnosti obeh tehnologij, ki jih uporabljamo pri izdelavi testnih kartic v Testnem centru Mikroiks so:

a) Tehnologija EPOXY:

- material konic: volfram (99. 99%)
- razdalja med konicama: 0. 005" (127μm)
- velikost kontaktne blazinice: 0. 0025"-0. 0030" (63.5 - 76.2 μm)
- sila na konico: 2-4 g/mils (2-4 g/ 25.4 μm)
- planarizacija: +- 0. 0007" (17.8 μm)
- premer konice: 0. 0015"-0. 0025" (38.1 - 63.5 μm)
- oblika vrha konice: raven
- dolžina konice: 0. 007"+-0. 001" od krivine (177.8 ± 25.4 μm)
- tiskane ploščice:
  C48-1 (dolžina 4. 5" (114.3 mm), 48 konic, pravokotna)
  C70-1 (dim. 4. 5"X7. 35" (114.3 x 186.7 mm), 70 konic, pravokotna)
  C70-2 (premer 2" (50.8 mm), 70 konic, okrogla)

b) Tehnologija BLADE:

- material konic: volfram (99. 99%)
- razdalja med konicama: 0. 005" (127 μm)
- velikost kontaktne blazinice: 0. 0025"-0. 0030" (63.5 - 76.2 μm)
- sila na konico: 2-4 g /mils (2-4g/ 25.4 μm)
- planarizacija: +- 0. 0007" (17.8 μm)
- premer konice: 0. 0015"-0. 0025" (38.1 - 63.5 μm)
- oblika vrha konice: raven
- dolžina konice: 0. 007"+-0. 001" od krivine (177.8 ± 25.4 μm)
- tiskane ploščice:
  C48-1 (dolžina 4. 5", (114,3 mm), 48 konic, pravokotna)

ZAKLJUČEK

Testne kartice postajajo vedno pomebnejši dejavnik pri testiranju kompleksnih mikroelektronskih vezij, saj lahko pomembno vplivajo na kvaliteto testiranja s tem pa prek izplena na celotno stroškovnost izdelave vezja. Zato so proizvajalci mikroelektronskih vezij praktičo prisiljeni temu segmentu posvečati vedno več pozornosti, tako v smislu vlaganj v vedno bolj sofisticirano opremo za izdelavo in vzdrževanje testnih kartic in tudi kadre, ali pa se posluževati profesionalnih uslug specializiranih firm za to področje.

Zlatko Bele, dipl. ing.
Mikroiks d. o. o.
Dunajska 5
61000 Ljubljana
tel. + 386 61 312 898
fax + 386 61 319 170

Prispelo (Arrived): 01.09.94 ***Sprejeto (Accepted): 20.09.94***

KARAKTERIZACIJA V VAKUUMU NAPARJENIH TANKIH PLASTI Al NA Si REZINE*

B. Praček
Inštitut za elektroniko in vakuumsko tehniko, Ljubljana, Slovenija

Ključne besede: mikroelektronika, tehnologija polprevodniška, plasti tanke, rezine silicijeve, naparevanje vakuumsko, nanašanje aluminija, oksidacija termična, AES Auger spektroskopija elektronska, C-V metoda kapacitivno napetostna, interferometrija

Povzetek: Nanašanje tankih plasti aluminija na silicijeve rezine je pomemben del polprevodniške tehnologije. V članku so podani rezultati karakterizacije tankih plasti aluminija s spektroskopijo Augerjevih elektronov v kombinaciji s C-V metodo in interferometrijo. Prikazani rezultati so dobljeni s preiskavo šestih karakterističnih vzorcev. Tanka plast aluminija je bila nanešena na tri vzorce z elektronskim curkom, na preostale tri pa z indirektnim uporovnim ogrevanjem na volframski spirali. Na enem vzorcu iz obeh skupin je bila pred nanosom plasti aluminija, na silicijevih rezinah s termično oksidacijo izdelana samo tanka plast silicijevega dioksida. Na drugih dveh je pred nanašanjem Al plasti z difuzijo bora izdelan np spoj ter na preostalih dveh z difuzijo fosforja pn spoj. Debelina, kemična sestava in elektronske lastnosti tako naparjenih plasti aluminija se najbolj razlikujejo pri tistih plasteh, ki so nanesene na silicijev dioksid, zaradi redukcije tega z aluminijem. Prav tako smo ugotovili, da so Al plasti nanešene z elektronsim curkom veliko boljše v pogledu gibljivih in negibljivih nabitih delcev, katere vnašajo v silicijev dioksid.

Characterization of Thin Al Films Deposited on Si Substrates**

Key words: microelectronics, semiconductor technology, thin films, silicon wafers, vacuum evaporation, aluminium deposition, thermally grown silicon oxide, AES, Auger electron spectroscopy, capacitance-voltage method, interferometry

Abstract: For a long time vacuum evaporation of thin aluminium films has been a constitutive part of semiconductor technology. This article presents some results on characterization of these films by Auger electron spectroscopy, capacitance-voltage and interferometric methods. The results presented have been obtained by examining six characteristic samples. On three of them aluminium has been evaporated by electron beam technique; other tree were coated with aluminium by evaporation from tungsten spiral. In each group of samples one of samples has been previously covered with thermally grown silicon oxide; the second two samples have been doped by boron and the third two by phosphorus. The thickness, chemical composition and electronic properties of these films are different; films deposited on the silicon dioxide show the most prominent differences because of the reduction of silicon dioxide by aluminium. Also, it has been confirmed that electron beam evaporated samples show better characteristics concerning the contents of fixed and mobile charges in the underlining silicon dioxide.

1. UVOD

Vakuumsko naparjene plasti aluminija so že dolgo nepogrešljiv sestavni del polprevodniške tehnologije. Dobro nanašanje in legiranje, dobra električna prevodnost, možnost fotolitografskega postopka in nizka cena so zelo zaželjene lastnosti v proizvodnji polprevodnikov. Aluminij se uporablja tako za vmesne plasti kot tudi za kontaktiranje. Uporabne lastnosti nanesenih plasti aluminija bodo odvisne od njihove končne kemične sestave in strukture. V članku podajamo rezultate karakterizacije tankih plasti aluminija, ki so nanesene v vakuumu z dvema različnima metodama: naparevanjem iz volframske špirale in nanašanjem s pomočjo elektronskega curka.

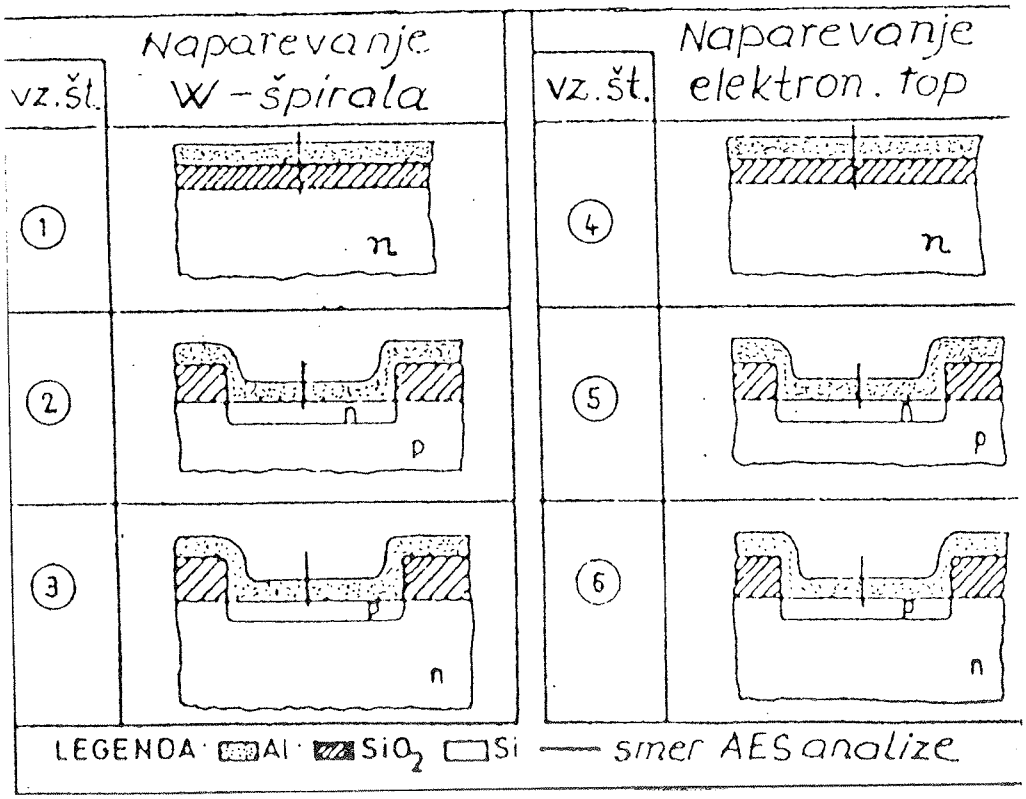
2. EKSPERIMENTALNO DELO

2. 1. Izdelava vzorcev

Vsi vzorci so izdelani na podlagah iz silicijevih rezin z orientacijo <111> in premera 2". Silicijevi podlagi sta bili za vzorca št.1 in št.4 termično oksidirani do debeline silicijevega dioksida okoli 0.4 μm in sta bila n tip z upornostjo 3-5 ohm cm. Plast aluminija je na vzorec št.1 naparjena iz volframske spirale na vzorec št.4 pa je nanesena z elektronskim curkom. Vzorca št.2 in št.5 sta izdelana na silicijevih rezinah p-tipa z upornostjo, ki je znašala 3-5 ohm cm, ki sta bili termično oksidirani do debeline silicijevega dioksida okoli 1 μm. Z fotolitografskim postopkom sta bili najprej pri obeh v oksidni plasti izdelani odprtini, sledil je postopek dopiranja s fosforjem in nato nanašanje aluminija. Plast aluminija je na vzorec št.2 naparjena iz volframske spirale na vzorcec št.5 pa nanešena z elektronskim curkom. Podlaga za vzorca št.3 in št.6 sta bili silicijevi rezini n-tipa s površino pripravljeno na enak način kot za vzorca št.2 in št.5, le da je po izdelavi odprtin v plasti silicijevega dioksida sledilo dopiranje z borom pred nanašanjem aluminija. Na vzo-

* Prispevek je bil objavljen že v prejšnji številki Informacij MIDEM, 2(94), vendar ga ponovno objavljamo in se opravičujemo avtorju zaradi napak, ki so se prikradle med tiskom prejšnje številke.

** This article has already been published in the last issue of Informacije MIDEM, 2(94). Due to some unfortunate mistakes which appeared in the text during printing, we are publishing it again with our apologies to the author.



Slika 1: Shematski prikaz prereza vzorcev

rec št.3 je plast aluminija naparjena iz volframske spirale, na vzorec št.6 pa je Al plast nanešena z elektronskim curkom. Shematski prikaz preseka na opisani način izdelanih vzorcev z označeno smerjo AES profilne analize kaže slika 1.

2. 2. Profilometrične meritve in optična karakterizacija

Meritve s profilometrom so pokazale, da je na vseh šestih vzorcih debelina nanešenih plasti aluminija dokaj enaka in da znaša okoli 0.4 μm. Prav tako so meritve pokazale, da sta debelini termično izdelanega silicijevega dioksida na podlagah vzorcev št.1 in št.4 pred nanašanjem aluminija, znašali okoli 0.38 μm. Preiskave z optičnim mikroskopom pri 500 kratni povečavi niso pokazale bistvenih razlik v izgledu in strukturi plasti.

2. 3. AES karakterizacija

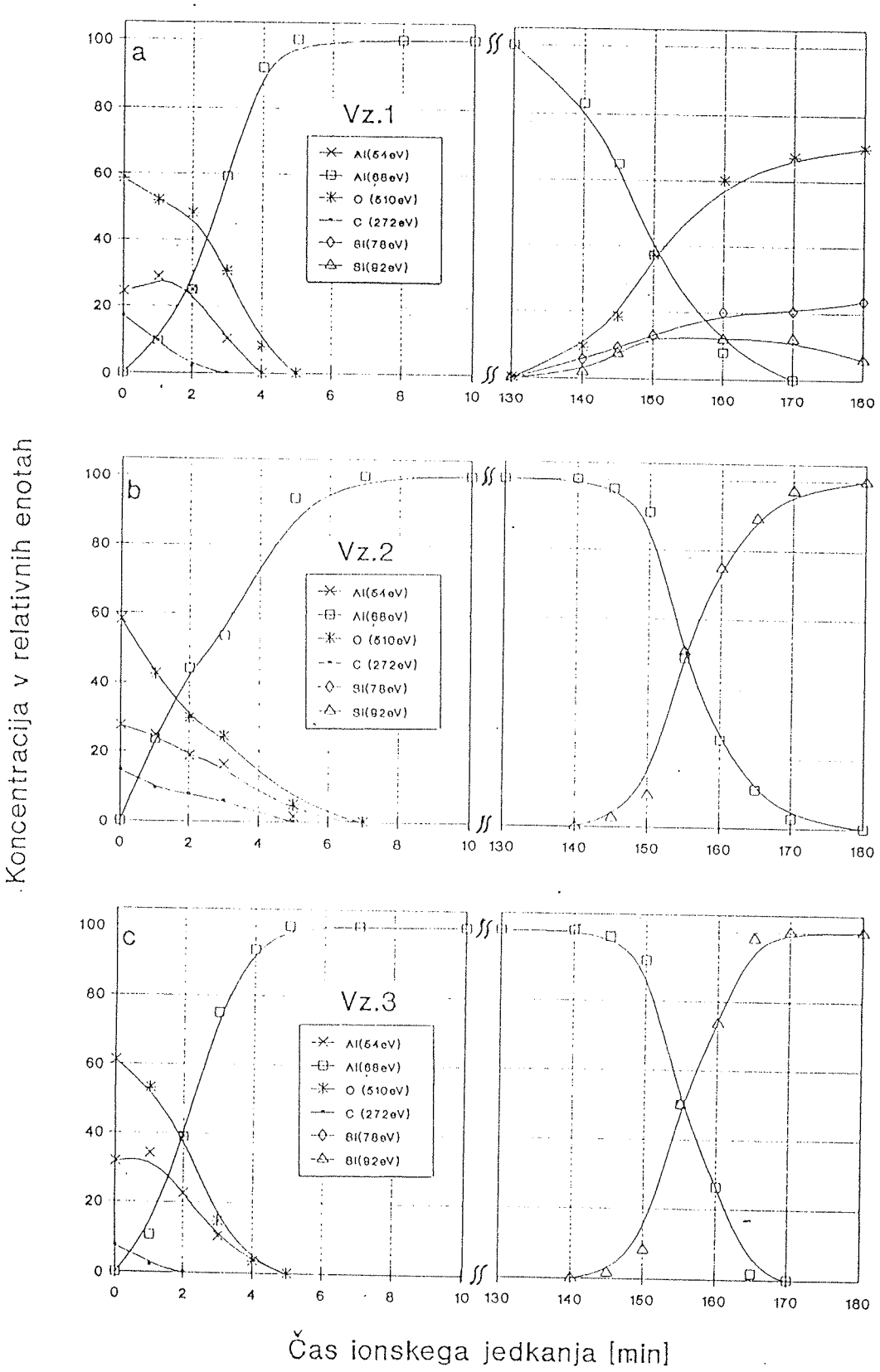
Vzorce smo pritrdili na nosilec vzorcev z nagibom 60 kotnih stopinj in jih ugradili v spektrometer Augerjevih elektronov (Phisical Electronics Ind. SAM 545 A). Za analizo smo uporabili statični curek primarnih elektronov energije 3 keV in tok elektronov 0.5 μA. Vzorci so jedkani z dvema sovpadajočima curkoma ionov argona z energijo 1 keV, ki sta rastrirala na površini 5mm x 5mm pri vpadnem kotu 47 kotnih stopinj. Hitrost jedkanja Cr/Ni standarda je bila okoli 3 nm/min. Podatki dobljeni iz spektrov Augerjevih elektronov, posneti med profilno analizo, so uporabljeni za izdelavo profilnih diagramov prikazanih na slikah 2 in 3. Na ordinati diagramov je nanesena koncentracija v relativnih enotah in na abscisi čas ionskega jedkanjav minutah. V legendi diagramov je za vse detektirane elemente označeno pri kateri energiji se v spektru Augerjevih elektronov nahaja njihov vrh.

3. REZULTATI IN DISKUSIJA

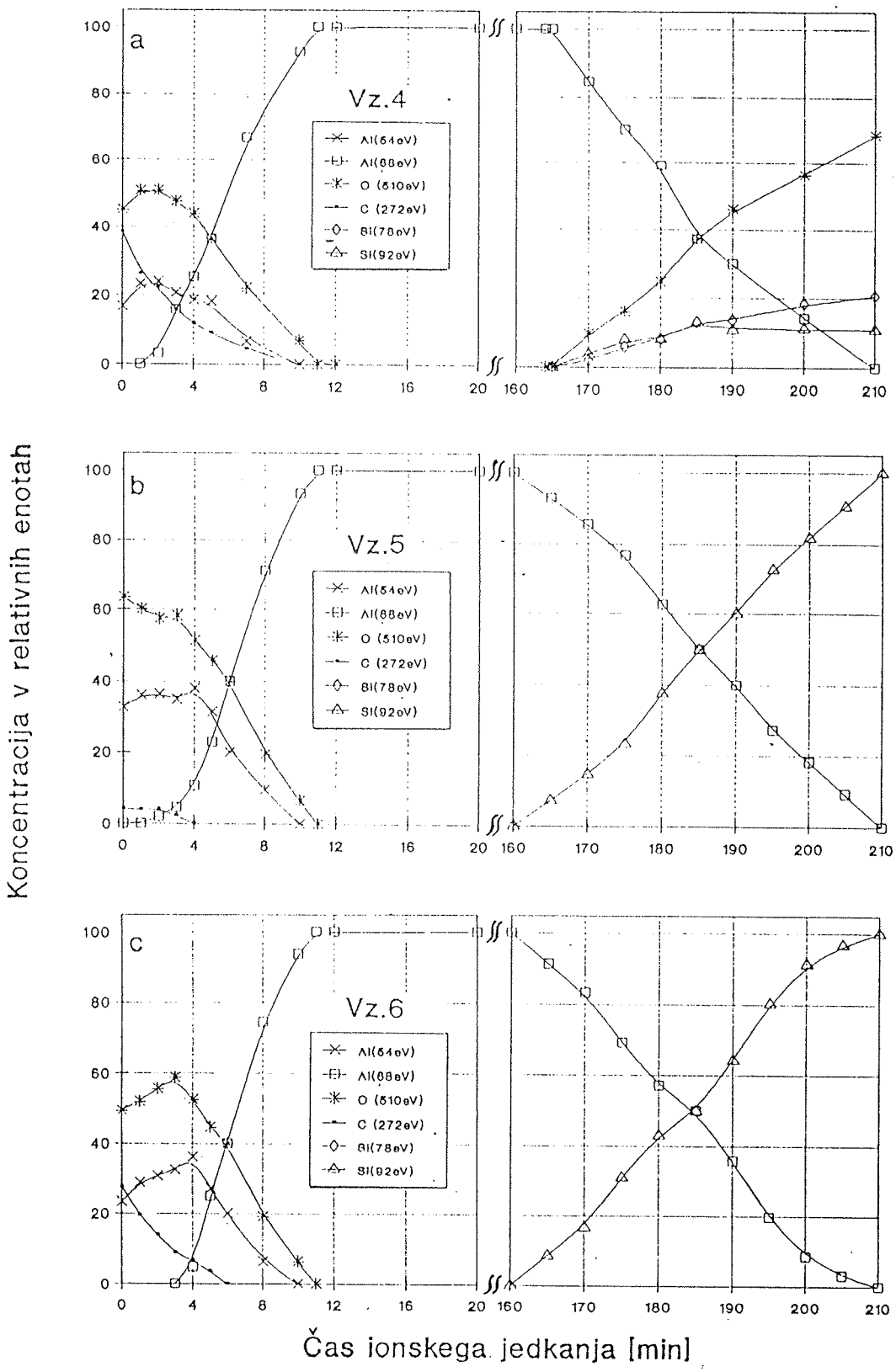
3.1 Rezultati AES profilne analize

Profilni diagram vzorca št.1 (slika 2a), prikazuje koncentracijski profil 0.4 μm debele plasti aluminija, ki je bila naparjena iz volframske spirale na 0.38 μm debelo plast silicijevega dioksida. Na površini Al plasti se nahaja tanka oksidna plast debela okoli 9 nm (okoli 3 min jedkanja). Augerjev vrh pri energiji 54 eV, ki pripada aluminiju vezanemu v Al_2O_3 ne zaznamo več že po štirih minutah jedkanja. Na površini in deloma tudi v tanki oksidni plasti najdemo kot kontaminacijo manjšo koncentracijo ogljika. Vse do 130-te minute jedkanja se nahaja plast čistega aluminija (Augerjev vrh pri energiji 68 eV), ko se že pojavijo vrhovi: Si(78eV), ki pripada siliciju vezanemu v SiO_2, vrh Si(92eV) pripada elementarnemu siliciju in vrh kisika O(510eV). Fazno mejo med Al in SiO_2 dosežemo po 150-tih minutah jedkanja (debelina okoli 0.45 μm).

V profilnem diagramu vzorca št.2 (slika 2b), je prikazan koncentracijski profil 0.4 μm debele plasti aluminija, ki je bila naparjena iz volframske spirale na silicijevo rezino dopirano z fosforjem. Nastala oksidna plast na površini tega vzorca je približno enake debeline (okoli 9nm) kot na vzorcu št.1, le da je meja med Al oksidom in kovino manj izrazita. Krivulja vrha Al(54eV), ki pripada oksidir-



Slika 2: Profilni diagram vz.1(a), vz.2(b) in vz.3(c)



Slika 3: *Profilni diagram vz.4(a), vz.5(b) in vz.6(c)*

anemu aluminiju namreč počasneje pada s časom jedkanja in izgine šele po 7-mih minutah jedkanja. Enaka ugotovitev velja tudi za koncentracijo ogljika. Po 140-tih minutah ionskega jedkanja se pojavi vrh elementarnega Si(92eV). Fazno mejo med čisto plastjo Al in Si dosežemo po 155-tih minutah jedkanja (okoli 0.46 μm). Fosforja kot dopanda pa nismo zaznali zato, ker je njegova koncentracija pod mejo občutljivosti AES metode.

Profilni diagram vzorca št.3 (slika 2c), kaže profil 0.4 μm debele plasti aluminija, ki je bila naparjena iz volframske spirale na silicijevo rezino dopirano z borom. Na površini vzorca št.3 je nastala oksidna plast aluminija, ki je po sestavi in izgledu meje med oksidom in kovino bolj podobna tisti na vzorcu št.1. Oksidna plast na vzorcu št.3 je tanjša (okoli 7nm) od plasti na vzorcih št.1 in 2 in vsebuje najnižjo koncentracijo ogljika. Čas ionskega jedkanja, ko zaznamo pojav elementarnega Si(92eV) in čas, ki je potreben, da dosežemo fazno mejo Al/Si pa je polnoma enak kot pri vzorcu št.2. Zaradi koncentracije, ki je pod mejo detekcije ne zaznavamo bora.

Profilni diagram vzorca št.4 (slika 3a), predstavlja profil 0.4 μm debele plasti aluminija, ki je bila z elektronskim curkom nanešena na 0.38 μm debelo plast silicijevega dioksida. Opazimo, da je na površini tega vzorca oksidna plast debela okoli 18 nm (6 min jedkanja). Na površini in tudi globlje vsebuje oksidna plast veliko koncentracijo ogljika. Po 165-tih minutah jedkanja zaznamo vrhove Si(78eV), Si(92eV) in O(510eV). Fazno mejo med Al in SiO_2 dosežemo po 185-tih minutah jedkanju (okoli 0.56 μm).

Profilni diagram vzorca št.5 (slika 3b), predstavlja profil 0.4 μm debele plasti aluminija nanešene z elektronskim curkom na silicijevo rezino dopirano z fosforjem. Na površini vidimo približno enako debelo oksidno plast (okoli 18 nm) kot je tista na vzorcu št. 4. Koncentracija ogljika pa je na površini in v oksidni plasti tega vzorca najmanjša. Vrh elementarnega Si(92eV) se pojavi po 160-tih minutah jedkanja, fazno mejo med Al in Si pa dosežemo po 185-tih minutah jedkanja (okoli 0.54 μm).

Profilni diagram vzorca št.6 (slika 3c), kaže profil 0.4 μm debele plasti aluminija, ki je bila z elektronskim curkom nanešena na silicijevo rezino dopirano z borom. Koncentracijski profil tega vzorca je zelo podoben profilom vzorcev št.4 in 5 (slika 3b in 3c) le da je koncentracija ogljika v približno enako debeli oksidni plasti nekoliko manjša kot pri vzorcu št.4

3. 2. CV karakterizacija

Vzorca št.1 in št.4 smo uporabili tudi za meritve količine gibljivih in negibljivih nabitih delcev s pomočjo TBS metode (1). Vzorec št.1 na katerega je bila 0.4 μm debela plast aluminija naparjena iz volframske špirale na 0.38 μm debelo plast SiO_2 je v oksidu vseboval Q = 3.41 x 10E11 q/cm^2 negibljivih in Q = 5.37 x 10E11 q/cm^2 gibljivih nabitih delcev. Vzorec št.4 na katerega je bila 0.4 μm debela plast aluminija nanešena z elektronskim curkom na 0.38 μm debelo plast SiO_2, pa je v oksidu vseboval Q = 2.05 x 10E11 q/cm^2 negibljivih in Q = 1.83 x10E11 q/cm^2 gibljivih nabitih delcev.

3. 3. Diskusija rezultatov

Znano je, da se na površini aluminija takoj po nanašanju v vakuumu, tvori tanka plast Al_2O_3 (2). Proces oksidacije površine poteka v dveh fazah: prva je kemisorbcija kisika in na to kemična reakcija, ki tvori oksid. Vsi z AES metodo analizirani vzorci so imeli na površini nastalo tanko oksidno plast aluminija, kjer smo razen aluminija in kisika ugotovili različno vsebnost ogljika. Debelina tankih oksidnih plasti na površini aluminija, ki je bil naparevan iz volframske spirale je približno dvakrat tanjša od tistih na katere je aluminij nanašan z elektronskim curkom. Razlike so posledica večih vzrokov: razlike v sestavi preostalih plinov pri nanašanju v vakuumu in razlike v energiji delcev, ki prihajajo na podlago (nekaj eV pri naparevanju iz W-spirale in nekaj deset eV pri nanašanju z elektronskim curkom) (3). Kot smo pričakovali so oksidne plasti na vzorcih št.1, 2 in 3, ki so bili istočasno v vakuumskem sistemu in naparevani iz W-spirale približno enake debeline (okoli 9 nm). Dvakrat debelejše (okoli 18 nm) so nastale oksidne plasti na vzorcih št.4, 5 in 6 ko je Al nanašan z elektronskim curkom. Debeline plasti Al so medsebojno enake na tistih vzorcih ko je nanašan na enako podlago in na enak način (vz. št.2 in št.3 ter vz. št.5 in št.6). Vrh elementarnega silicija Si(92eV), katerega zaznamo na fazni meji med Al in SiO2 tako pri vzorcu št.1, kot pri vzorcu št.4 je posledica redukcije SiO_2 z aluminijem (4). Daljši časi jedkanja plasti Al, ki so na podlago nanešene s pomočjo elektronskega curka, v primerjavi s časi jedkanja plasti Al naparevanega iz volframske špirale lahko pojasnimo s tem, da imajo plasti nanašane z elektronskim curkom bolj kompaktno strukturo zaradi večje energije delcev ko prihajajo na podlago in se zato počasneje jedkajo (5). Pri vzorcih, kjer je plast Al nanašana z elektronskim curkom smo opazili, da je manj izrazita tudi fazna meja med Al in podlago. Plasti, ki jih nanašamo z elektronskim curkom imajo verjetno tudi zaradi tega boljšo adhezijo na podlago. Kot smo pričakovali, to so potrdile tudi CV meritve, je bolj primerno nanašanje Al z elektronskim curkom tudi zato, ker daje manjše količine nabitih delcev v silicijevem dioksidu pod plastjo Al.

4. ZAKLJUČEK

Rezultati preiskave šestih tipičnih vzorcev plasti aluminija nanesenih na različno obdelane podlage na silicijevih rezinah so pokazali, da med plastmi Al, ki so naparjene iz W-spirale in tistimi, ki so nanešene s pomočjo elektronskega curka obstojajo razlike v kemični sestavi površin in faznih mej Al/Si-rezina in tudi v elektronskih lastnostih. Na plasteh aluminija, ki so naparjene iz W-spirale so nastale tanjše in manj kontaminirane oksidne plasti. Postopek nanašanja iz W-spirale povzroča tudi večjo količino gibljivih in negibljivih nabitih delcev v SiO_2

plasteh pod nanešenim aluminijem. Plasti Al, ki so nanešene z elektronskim curkom imajo bolj kompaktno strukturo kar kaže daljši čas ionskega jedkanja enako debelih plasti. Na površini Al z elektronskim curkom nanešenega Al nastajajo sicer debelejše oksidne plasti, nekoliko večja pa je tudi kontaminacija z ogljikom. V plasti SiO_2, ki se nahaja pod plastjo Al pa se zato nahaja manjša količina gibljivih in negibljivih nabitih delcev.

5. LITERATURA

(1) D. M. Petković, Zbornik referatov simpozija o elektronskih sestavnih delih in materialih, Ljubljana (1980), p.247

(2) M. Bujor, L. A. Larson and H. Poppa, J. Vac. Sci. Technol., 20(3), (1982), P.392

(3) Y. E. Strausser and K. S. Majumder, J. Vac. Sci. Technol., 15(2), (1978), p.238

(4) D. Pramnik, A. N. Saxena, S. State Technology, Jan. 1983, p.127

(5) E. Zinner, J. Electrochem. Soc., May (1983), p.199C

B. Praček, dipl.ing.
IEVT
Teslova 30
Ljubljana
tel. + 386 61 123 13 41
fax. + 386 61 263 098

Prispelo (Arrived): 16.05.94 ***Sprejeto (Accepted): 10.06.94***

ELEKTRONSKE KOMPONENTE

VISOKOVOLTNI ALUMINIJASTI ELEKTROLITSKI KONDENZATOR

Proizvajalci elektronskih komponent za audio in video naprave so visokovoltni elektrolitski kondenzator za 350 V delovne napetosti začeli zamenjevati s kondenzatorjem delovne napetosti 385 V. Ob tem so zahteve po življenski dobi 2000 ur in temperaturni kategoriji -40°C do +85°C povsem nekaj normalnega, ki jih zahtevajo že vsi kupci v svetu. Poleg tega se pojavlja še zahteva posebne izvedbe priključnih ušesc, to je "SNAP IN" izvedba. Prvo povpraševanje po takih kondenzatorjih smo dobili iz tovarne Gorenje, v letu 1992 pa še iz Češke, Nemčije in Francije. To je bil glavni razlog za našo odločitev, da naredimo nov korak na področju proizvodnje visokovoltnih aluminijastih elektrolitskih kondenzatorjev. Zato smo se odločili za razvoj visokovoltnega aluminijastega elektrolitskega kondenzatorja (ELKO) za nazivno napetost 385 V za temperaturno območje delovanja od -40°C do +85°C z življensko dobo 2000 ur. Kondenzator se uporablja v napajalnih modulih, v proizvodnji audio in video naprav ter v merilni in regulacijski tehniki.

Za izvedbo naloge smo celoten projekt razdelili na tri faze, ki so obsegale naslednja poglavja dela:

1. faza:

a) sinteza delovnega elektrolita
b) konstrukcija zvitka
c) določitev tesnilnih materialov
d) konstrukcija ohišja
e) izdelava laboratorijskih vzorcev
f) interni preizkus

2. faza:

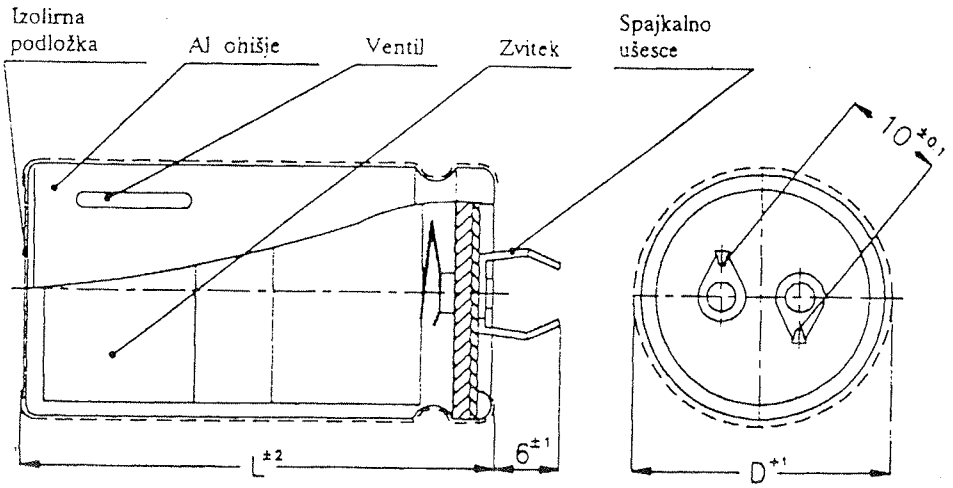
a) optimiziranje Al ELKO
b) izdelava novih laboratorijskih vzorcev
c) izvajanje poskusov laboratorijskih vzorcev
d) izdelava vzorcev za interni tipski preizkus
e) interno testiranje tipskih vzorcev

3. faza:

a) razvojna dokumentacija za poskusno proizvodnjo ELKO
b) tehnološka dokumentacija za poskusno proizvodnjo
c) tehnološke preureditve
d) poskusna proizvodnja
e) izdelava vzorcev za tipsko preizkušanje
f) testiranje tipskih vzorcev
g) izdelava dokumentacije za redno proizvodnjo
h) izdelava zaključnega poročila

1. faza:

Najprej smo se lotili izdelave delovnega elektrolita in laboratorijskih vzorcev, da smo lahko določili osnovne električne parametre ELKO. Na osnovi tega smo določili materiale za izdelavo zvitka (Al folije) in materiale za tesnenje. Vzporedno smo konstruirali tudi izvedbo ohišja. S tem so bili izpolnjeni osnovni pogoji za izdelavo vzorcev za interni laboratorijski preizkus.



Slika: *Kostrukcija ELKO v "SNAP-IN" izvedbi*

2. faza:

Na osnovi rezultatov 1. faze dela smo opravili določene korekture pri delovnem elektrolitu in pri izbiri Al anodnih folij. Preizkusili smo tudi nov tip Al ohišja z ventilom na steni stročnice. Napravili smo vzorce v "SNAP-IN" izvedbi in opravili interni tipski preizkus. V obeh fazah je potekala izdelava zvitkov na napravah redne proizvodnje. Ostalo kot: sinteza delovnega elektrolita, impregnacija, montaža in električna obdelava pa smo opravili v laboratoriju. Na ta način smo izdelali po 50 kosov vsake vrednosti 60 μF, 100 μF, 150 μF in 220 μF. Začeli pa smo se pripravljati tudi na redno proizvodnjo.

Konstrukcija ELKO v "SNAP-IN" izvedbi je prikazana na sliki.

3. faza:

Izdelali smo dokumentacijo za poskusno proizvodnjo in izvedli določene tehnološke preureditve na napravah za impregnacijo, montažo in električno obdelavo. Na ta način smo brez večjih investicijskih vlaganj začeli s poskusno proizvodnjo. Na proizvodnih linijah smo izdelali 300 kosov vsake vrednosti. Vzorce smo preizkusili na življenski dobi 2000 ur pri napetosti 385 V in temperaturi +85°C.

Rezultati preizkusov so pokazali, da vzorci ustrezajo naslednjim zahtevam:

DIN 45910 T12
IEC 384-4
CECC 303000

Redna proizvodnja:

Na osnovi teh rezultatov smo izdelali kompletno dokumentacijo za redno proizvodnjo. Ustreznost vzorcev so potrdili tudi naši kupci iz Gorenja in na Češkem. Zaradi velikega povpraševanja smo začeli z redno proizvodnjo in v letu 1993 izdelali 45.000 kosov 220 μF/385 V. Na osnovi naročil pa predvidevamo za leto 1994 350.000 kosov redne proizvodnje.

Matija Zdešar dipl. ing.
ISKRA ELEKTROLITI
Proizvodnja elektrolitskih kondenzatorjev, d.o.o.
Mokronog, Stari trg 36

PREDSTAVLJAMO PODJETJE Z NASLOVNICE

KEKO

Grajski Trg 15, Žužemberk, Slovenia
tel. (+386 68) 87-230,
faks (+386 68) 87-315

Tradicija na področju proizvodnje keramičnih elektronskih komponent se pričenja v Žužemberku leta 1960, ko se v obratu Iskre začnejo proizvajati keramični disk kondenzatorji. Na podlagi stalnega razvoja tovarne v programskem in statusnem smislu obstaja danes KEKO delniška družba, ki v svojih programih ponuja široko paleto:

- keramičnih enoplastnih in večplastnih kondenzatorjev (SLC in MLC),
- pozitivno temperaturno odvisnih uporov (PTC termistor),
- enoplastnih in večplastnih napetostno odvisnih uporov (varistorjev) in
- konstrukcijo in izdelavo opreme za proizvodnjo navedenih elementov in opreme po naročilu

Z navedenimi programi dosegamo trenutno 10 mio DM letne prodaje od tega prek 80 % na zahodnih trgih. Distribucijo opravljamo prek prodajne mreže distributerjev in agentov kot tudi z direktnimi kontakti.

Naše komponente se uporabljajo tako v širokopotrošnih izdelkih kot tudi v sistemih telekomunikacij, avtomobilske industrije, krmiljenja, skratka na vseh področjih uporabe elektronike.

V KEKO obvladujemo v osnovi dve keramični tehnologiji - prašno tehnologijo suhega stiskanja in tehnologijo nalivanja keramičnih plasti. To nam omogoča proizvodnjo širokega spektra keramičnih komponent, kakršnega lahko nudijo le redke firme v svetu. Druga prednost tovarne je lastna izdelava opreme za proizvodnjo omenjenih keramičnih komponent. To nam omogoča nenehno izboljšavo tako opreme, njene avtomatizacije, kakor tudi tehnologije ter razvoj kvalitativno novih komponent ali komponent po naročilu. Takšne rezultate omogoča le interdisciplinarno delo naših izredno kakovostnih inženirjev vseh tehničnih strok, kakor tudi uspešno sodelovanje s strokovnjaki z Inštituta Jožef Stefan in Kemičnega inštituta Boris Kidrič na področju fizikalno-kemičnih analiz materialov ter komponent.

Naši osnovni cilji so:

- postati konkurenčni po kakovosti, spektru komponent ter ostalih komercialnih merilih na evropskem trgu ter v ZDA in trajno obstati na teh trgih

- razširitev proizvodnega programa v smeri SMD večplastnih elektronskih keramičnih komponent, kot so PTC, NTC ter mikrovalovne komponente

Najstarejši program je program enoslojnih keramičnih kondenzatorjev (SLC), ki jih proizvajamo s tehniko suhega stiskanja do 12 mio. kosov na mesec. Pri nekaterih vrstah SLC kondenzatorjev (serije cevnih, skoznih, trapeznih) smo med zadnjimi proizvajalci v Evropi. Za zaščitne ter kondenzatorje proti motnjam imamo pridobljene VDE, CSA, S, N, D ter FI ateste.

Izdelek večplastni keramični kondenzator je novejši predstavnik v verigi keramičnih elektroskih elementov in je logično nadaljevanje programa klasičnih enoplastnih kolutastih kondenzatorjev. Element je tehnološko zahtevnejši in ima, v primerjavi z drugimi predstavniki v družini keramičnih kondenzatorjev, nekaj bistvenih prednosti. Ena glavnih je vsekakor miniaturizacija dimenzij in hkratno doseganje visokih kapacitivnosti. Večplastni keramični kondenzator je sestavljen tako, da predstavlja seštevek množice kondenzatorjev z izredno tankimi dielektričnimi plastmi. Na ta način se doseže relativno zelo visoke kapacitivnosti tudi na miniaturnih dimenzijah. Način vgradnje elektrod v keramični čip zagotavlja visoko zanesljivost elementa ter dobro izolacijo in zaščito pred zunanjimi vplivi. S proizvodnjo teh kondenzatorjev smo začeli pred približno desetimi leti. Ker je MLC kot izdelek tehnološko zelo zahteven, smo tehnologijo in proizvodne zmogljivosti dograjevali postopno. Večina opreme je bila izdelana v sami tovarni. Sedaj imamo zanesljivo in avtomatizirano proizvodno linijo s kapaciteto okrog 10 mio kosov mesečno.

Asortiman izdelkov s področja MLC je relativno širok. V osnovi obstajata dve izvedbi: izvedba "SMD čip", namenjena za vgradnjo v vezja s površinsko montažo ter izvedba z žičnimi kontakti, namenjena za vgradnjo v klasična tiskana vezja. Nadalje se asortiman deli glede na keramične mase z različnimi temperaturnimi karakteristikami: NP0, 2R1 (X7R) in 2F3 (Z5U). Tudi spekter nazivnih delovnih napetosti je obširen. Izdelujemo kondenzatorje standardnih napetosti 50 in 100 V, srednjenapetostne kondenzatorje 20-500 V ter visokonapetostne kondenzatorje 1-10 kV. Glede na dimenzije, izdelujemo vse najpogostejše dimenzije, ki so standardizirane v mednarodnih standardih. Poleg kondenzatorjev s področja standardnih MLC lahko na željo strank izdelamo tudi elemente s specialnimi lastnostmi ali zahtevami.

Trenutno poteka razvoj nižjenapetstnih večplastnih kondenzatorjev na dielektričnih plasteh debeline 5-10 μm, kar pomeni dvakrat, oziroma štirikrat tanjše plasti v primerjavi z dosedaj standardnimi plastmi. To nam bo omogočalo za ravno tolikokrat povečati obseg najvišjih kapacitivnosti, zmanjšati dimenzije in hkrati znižati proizvodne stroške. Osnova za te kondenzatorje je nova tehnologija, ki jo razvijamo skupaj z nizozemsko firmo DSM. Predvidevamo, da bo poskusna proizvodnja stekla v začetku leta 1995. Razvoj v smeri miniaturizacije se bo na tej tehnologiji nadaljeval tako, da bo v končni fazi mogoče uporabljati dielektrične plasti okrog 1 μm.

Temperaturno odvisen upor, oz. termistor je kpt elektronski pasivni element poznan že od začetkov elektronike. Razdeljen je na negativno odvisen upor oz. NTC in pozitivno temperaturno odvisen upor oz. PTC. Pravo veljavo v elektroniki dobiva šele v zadnjem obdobju, ko se njegova uporabnost močno širi v področje zaščit, senzorjev in dodatno PTC upori na področje grelcev. Temu je vsekakor prispeval razvoj termistorjev v smislu večjih temperaturnih odvisnosti, skratka dizajniranju karakteristik s ciljem približati se uporabnosti v čim širšem pomenu besede.

V KEKO se je razvoj PTC termistorja pričel z odkupom določene faze razvoja od Iskre Feriti in prenos v KEKO v letih 89-90. Nadaljni razvoj tehnologije proizvodnje PTC termistorjev je pripeljal danes do proizvodnje 10 mio kosov letno, kar se trži 95 % na zahodne trge. Glavne uporabe so na področju grelcev in senzorjev. Nastopajo v glavnem v obliki kolutov in ploščic premerov od Ø2 do Ø25 mm z metaliziranimi elektrodami. Trenutno dosegamo nazivne upornosti od 60 Ωcm do 10 kΩcm in Curiejeve temperature od 70°C do 250°C, kar omogoča od nekaj W do desetin W disipirane moči, odvisno od dimenzije grelnega telesa.

V uporabi kot grelec omogoča PTC termistor priklop direktno na omrežno napetost in temperaturo površine. S tem se minimizira regulacijska vezja in razne termo zaščite ter eventuelne vžige, kot je problem pri uporovnih grelcih. Vsekakor predstavlja PTC termistor elektronski element, ki si bo obdržal svoje področje uporabe in se s svojim razvojem še okrepil na področju zaščite in senzorike.

Najnovejši program, ki smo ga pred štirimi leti samostojno začeli razvijati je program zaščitnih komponent - varistorjev. Zahvaljujoč dinamičnemu razvoju in tehnološko bogatemu okolju KEKA smo uspeli razviti že 7 različnih zaščitnih komponent z varistorsko funkcijo, ki obsegajo tako enoslojne kakor tudi večplastne komponente.

Ena od prvih serij, ki smo jo pričeli proizvajati je serija standardnih disk varistorjev CV. Z njo pokrivamo široko napetostno področje od 18-1000 V, pri čemer je njihova zdržljivost na tokovne udare v obsegu od 100-6500 A. Izdelujemo 5 standardnih velikosti (5, 7, 10, 14, 20 mm). Trenutno smo v fazi pridobivanja CSA, UL in VDE atestov.

Druga serija v okviru enoslojnih varistorjev je SV serija specialnih, kvadratnih , ožičenih, v epoksi zalitih varistorjev, predvidenih za srednjenapetostno območje (100-1000 V), z zdržljivostjo na tokovne udare v osegu od 400-12000 A. Ta serija ima dve veji. Eno tvorijo standardni tipi, ki jih izdelujemo v 7 standaradnih velikostih (5, 7, 10, 14, 18, 20 mm). Standardni del SV serije je načrtovan z namenom da zamenja standardne, na tržišču običajne disk varistorje, nudeč kupcu boljše elek-

trične lastnosti (nivo zaščite, tok puščanja, zdržljivost na tokovne udare, itn.) na nominalno manjših dimenzijah. Ena od naših posebnosti, po kateri smo edini na svetovnem trgu, so varistorji s karakteristikami po željah naročnika, ki tvorijo drugo vejo SV serije. Kupec lahko sam ali z našo pomočjo dizajnira optimalni varistor z minimalnimi dimenzijami tako, da zadovolji svojo specifično aplikacijo. Kupec se tudi lahko odloči, da ima standardne električne parametre na nestandardni obliki in v dimenzijah, ki najbolj ustrezajo predvidenem ohišju. Naša popolna strokovna pomoč je kupcu vedno na razpolago.

V večplastni tehnologiji izdelujemo dve seriji izdelkov: nizkonapetostne ZV varistorje ter AV "automotiv" varistorje. Oba izdelka nudimo v "SMD čip" in ožičeni izvedbi. ZV varistorji pokrivajo napetostno območje od 4-50 V, z zdržljivostjo na tokovne udare v obsegu od 25-1000 A. V Evropi smo prvi in edini proizvajalec, ki v svojem proizvodnem programu ima 4 V varistor, ki predstavlja optimalno zaščito sodobnih CMOS in BiCMOS integriranih vezij z napajalno napetostjo do 3 V. AV varistorji so predvideni za napetostno območje, ki se pojavlja v avtoelektroniki (12, 14 V) in za izredno visoko zdržljivost na tokovne udare (500-4000 A) ter energetske obremenitive (2-100 J) in so zato idealna zaščita za elektronske sisteme v vozilu.

Posebno vrsto kvalitativno novih zaščitnih komponent predstavljajo komponente z dvojno zaščitno funkcijo VARICONi, ki ščitijo proti napetostnim sunkom in visokofrekvenčnim oziroma radiofrekvenčnim motnjam. Imamo dve seriji VARICON-ov. MV serija je predvidena za napetostno območje od 4-50 V in ima kapacitivnosti v obsegu od 10-100 µF, kar ščiti občutljiva elektronska vezja proti napetostnim sunkom ter visokofrekvenčnim motnjam. OV serija je predvidena za napetostno področje avtoelektronskih aplikacij in ima kapacitivnosti v obsegu od 0.17-1.5 µF.

Serijo, s katero zaokrožujemo naš spekter zaščitnih komponent, tvorijo visoko energetski ZOV varistorji za močnostne aplikacije, ki pokrivajo napetostno območje od 200-1000 V z zdržljivostjo na tokovne udare v obsegu od 15000-70000 A. Izdelujemo jih ali kot metalizirane bloke namenjene za montažo pri uporabniku ali v epoksirani izvedbi s kovinskimi priključki. V okviru standardne veje ZOV serije ponujamo 4 velikosti (25, 32, 40, 60 mm) ZOV varistorjev. Drugo vejo ZOV varistorjev predstavljajo varistorji s karakteristikami po željah naročnika, pri katerih so dosegljivi tudi višji nivoji zdržljivosti na tokovne udare (do 100000 A).

Program izdelave opreme za proizvodnjo elektronskih keramičnih komponent smo razvijali od samega začetka. Prvotni impulz so bile lastne potrebe firme. Pozneje, ko smo z razširitvijo tipov opreme pokrili vse operacije tehnologije nalivanja dielektričnih plasti smo postali tržno zanimivi. Do sedaj smo opremo ter tehnologijo nalivanja dielektričnih plasti tržili na Kitajskem, v Belorusiji ter v Indiji.

Sesutje ruskega trga v preteklih letih je pomenilo hud udarec za proizvodnjo opreme in tudi za ekonomiko tovarne v celoti.Lastno znanje na izdelavi opreme, kakor tudi na vseh ostalih programih je prispevalo preokretu tovarne v smislu optimiranja lastnih rezerv brez odpuščanja delavcev in doseganju svetovnih tržnih zahtev. Opiranje na lastne kadre nam je dalo osnovo za uspeh, da smo za proizvodnjo opreme v obdobju pol leta poiskali nadomestne trge in znova dosegli ekonomiko tovarne, ki nam omogoča lažje prebroditi težave pri vključevanju v svetovne trge in transformacijo tovarne v postopkih lastninjenja.

PROIZVODNI PROGRAM

KERAMIČNI KONDENZATORJI				
MLC	**Vp Serija** - Srednjenapetostni	**HV Serija** - Visokonapetostni		
Kapacitivni obseg	1 pF to 3.3 µF	100 pF to 470 µF		
Nazivna napetost	50,V 100 V, 200 V, 300 V, 500 V	1-10 kV		
Temperaturna karakteristika	NP0, X7R, Z5U	NP0, X7R		
Izvedba	Radialno ožičeni ali čipi	Čip		
Zaščita	Epoksi			
Pakiranje	Razsuti ali trakani	Razsuti		
SLC	**K Serija** - Disk	**KV Serija** - Visokonapetostni	**KZ Serija** - Zaščiteni	**KM Serija** - Proti motnjam
Kapacitivni obseg	0.56 pF do 18 nF	2.2 pF do 10 nF	33 pF do 4.7 nF	1 nF do10 nF
Nazivna napetost	10 V, 500 V	1-10 kV	400 V/50 Hz	250 V/50 Hz
Temperaturna karakteristika	Tip 1, Tip 2	Tip 1, Tip 2	Tip 2	Tip 2 (X1, Y)
Zaščita	Durez	Durez	Durez/epoksi	Durez/epoksi
Pakiranje	Razsuti ali trakani	Razsuti ali trakani	Razsuti ali trakani	Razsuti ali trakani
Atesti			VDE	VDE, CSA, S, N, D, FI
	T Serija - Trapezni	**S Serija** - Skozni	**C Serija** - Cevke	
Kapacitivni obseg	2.2 pF to 3.9 nF	5.6 pF to 2.7 nF	0.6 pF to 1.8 pF	

Nazivna napetost	500 V	350 V	500 V
Temperaturna karakteristika	Tip 1, Tip 2	Tip 2 (X1, Y)	Tip 1
izvedba	čip	Aksialno ožičeni	Radialno ožičeni
Pakiranje	Razsuti	Razsuti	Razsuti

VARISTORJI			
SLV	**CV Serija** - Disk	**SV Serija** - Standardni	**SV Serija** - Po naročilu
Napetost praga	18 V do 1000 V	100 V do 1000 V	100 V do 1000 V
Najvišji tokovni impulz	100 A do 6500 A	400 A do 12000 A	> 5500 A/cm^2
Najvišji energetski impulz	0.3 J do 200 J	2.2 J do 280 J	> 400 J/cm^3
Zaščita	Epoksi	Epoksi	Epoksi
Pakiranje	Razsuti ali trakani	Razsuti ali trakani	Razsuti ali trakani
Atesti	C-UL, VDE v testiranju		
MLV	**ZV Serija** - Nizkonapetostni	**AV Serija** - Avtomobilski	
Napetost praga	4 V do 33 V	18 V, 22 V, 27 V, 33V	
Najvišji tokovni impulz	25 A do 1000 A	250 A do 4000 A	
Najvišji energetski impulz	0.05 J do 6.0 J	1 J do 45 J	
Izvedba	Radialno ožičeni ali čipi	Radialno ožičeni ali čipi	
Zaščita	Epoksi	Epoksi	
Pakiranje	Razsuti ali trakani	Razsuti ali trakani	
Močnostni	**ZOV Serija** - Standardni	**ZOV Serija** - po naročilu	
Napetost praga	200 V do 1000 V	200 V do 1000 V	
Najvišji tokovni impulz	15000 A do 40000 A	> 5500 A/cm^2	
Najvišji energetski impulz	140 J do 1100 J	> 400 J/cm^3	
Izvedba	Metalizirana ploščica ali zaščiten	Metalizirana ploščica ali zaščiten	
Zaščita	Epoksi	Epoksi	
Pakiranje	Razsuti	Razsuti	
VARICON	**MV Serija** - Nizkonapetostni	**OV Serija** - Avtomobilski	
Napetost praga	4 V do 33 V	18 V, 22 V, 27 V, 33 V	
Najvišji tokovni impulz	50 A do 250 A	1000 A	
Najvišji energetski impulz	0.05 J do 1.3 J	3.2 J do 6.0 J	
Kapacitivni obseg	10 do 100 nF	0.47 do 1.5 µF	
Zaščita	Epoksi	Epoksi	
Pakiranje	Razsuti ali trakani	Razsuti ali trakani	

POZISTORJI		
Grelci	**Visokonapetostni**	**Nizkonapetostni**
Naziva temperatura	70°C do 220°C	40°C do 80°C
Nazivna upornost	200 Ω do 1700 Ω	4 Ω do 25 Ω
Največja dovoljena napetost	160 V, 240 V, 260 V	30 V, 50 V
Izvedba	Metalizirane tablete	Metalizirane tablete
Pakiranje	Razsuti	Razsuti
Pretokovna zaščita	**High voltage**	
Naziva temperatura	60°C	
Nazivna upornost	1200 Ω to 3500 Ω	
Največja dovoljena napetost	360 V	
Izvedba	Radialno ožičeni	
	Epoksi ali brez	
Pakiranje	Razsuti	

KEKO d.d., Grajski trg 15, 68360 Žužemberk, SLO, tel. (+ 386 68) 86-230, fax (+ 386 68) 87-315

KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA

NATO Advanced Workshop on "Advances in Ceramic MCM and High Performance Electronic materials" 21. - 23. 5. 1994, Islamorada, Florida, USA

Udeležil sem se konference oz. delavnice (workshop) o (predvsem) keramičnih multichip modulih (MCM) in materialih za elektroniko, ki sta jo sponzorirala NATO in ISHM (International Society for Hybrid Microelectronics). Konferenca je trajala tri dni, od 21. do 23. maja v hotelu Cheeca Lodge na otoku Islamorada, kakih 150 km južno od Miamija. Delo je potekalo v naslednjih sekcijah:

- Keramični MCM
- Uporaba keramičnih MCM
- Debeloplastni senzorji
- Načrtovanje in modeliranje
- MCM - "mešane" tehnologije
- "Napredni" (advanced) debeloplastni materiali

Udeleženci:

Združene države Amerike	31
Francija	4
Nemčija	4
Velika Britanija	3
Madžarska	2
Poljska	2
Švedska	2
Avstrija	1
Belgija	1
-Češka	1
Italija	1
Litva	1
Slovaška	1
Slovenija	1
Španija	1

V poročilu bom na kratko opisal vsebino nekaterih zanimivejših predavanj, na razpolago pa je zbornik razširjenih povzetkov. Zbornik referatov bo izšel predvidoma v prvi polovici naslednjega leta.

Multi Chip Moduli (MCM) so komponente z zelo visokim številom funkcij, pri katerih se na večplastne substrate z veliko gostoto povezav pritrdi gole silicijeve tabletke. Multichip moduli imajo precej prednosti pred konvencionalno inkapsuliranimi silicijevimi tabletkami z velikim številom vhodov/izhodov (single chip modules), predvsem v primerih, ko primanjkuje prostora v vezju in, če je takt ure "hiter". Nekateri predavatelji so povedali, da bodo za zahtevne aplikacije postali MCM nujno potrebni, ker zaradi naraščajočega števila transistorjev na silicijevih tabletkah in hitrosti "delovanja" konvencionalne tehnologije ne bodo več ustrezale zaradi predolgih povezav.

Ena od prednosti MCM pred ASIC (Application Specific Integrated Circuits) je v hitrejšem designu MCM. Pri ASIC traja načrtovanje tudi do dve leti, v MCM pa se povežejo obstoječe tabletke. ASIC je v velikih količinah lahko precej cenejši in bolj funkcionalen, vendar je za izdelke pomembnejši kratek čas razvoja. Gostota komponent je lahko podobna na MCM in pri ASIC, pri tem pa se lahko v MCM kombinirajo tudi različne polprevodne tehnologije, na primer silicij in GaAs.

Na konferenci so obravnavali predvsem keramične MCM. Za začetek bom na kratko definiral "osnovne tipe" Multi Chip Modulov, izdelanih v različnih tehnologijah:

MCM-L so zahtevna večplastna tiskana vezja z linijami minimalne širine, to je navzdol do 25 μm.
* Relativna cena: 1

MCM-D so moduli, ki imajo nanešene tankoplastne večplastne kovinske povezave (večinoma aluminij ali baker), ločene s polimernim ali napršenim tankoplastnim (SiO_2) dielektrikom. Kot substrat se največ uporablja Al_2O_3 ali silicij. Silicij dobro prevaja toploto, njegov temperaturni razteznostni koeficient pa je seveda isti kot razteznostni koeficient silicijevih tabletk. V tem primeru se del elektronike izdela lahko že na substratu. Ta tip MCM omogoča največje gostote komponent oz. funkcij.
* Relativna cena - Al_2O_3 : 3
* Relativna cena - silicij: 8

MCM-C so "keramični" hibridi visoke gostote, navadno večplastni keramični substrati, v katerih je tudi prek 50 nivojev prevodnika, ali pa kompleksna debeloplastna večplastna vezja. Večplastni keramični substrati so narejeni iz zelenih folij, potiskanih s prevodnimi linijami in so lahko na osnovi Al_2O_3 ali AlN z višjo toplotno prevodnostjo (HT- MCM-C - keramični MCM z visoko temperaturo žganja) ali pa na osnovi kristalizirajočih stekel (LT- MCM-C - keramični MCM z nizko temperaturo žganja). V sam substrat

so lahko vgrajeni, v glavnem v primeru keramike s temperaturo žganja pod 1000°C, tudi upori ali kondenzatorji.
* Relativna cena: 2

Moja (povsem osebna!) ocena je, da bodo zaradi njihove visoke cene, kljub neizpodbitnim prednostim, MCM uporabljani še precej časa predvsem za vojaške in vesoljske aplikacije. Mimogrede, še anekdota iz uvoda članka o MCM; avtor je napisal, da, če isto vezje, izdelano v večplastni debeloplastni tehnologiji, imenuje večplastno vezje, bo zanj dobil 100$, če pa ga imenuje Multi Chip Modul, pa 1000$.

Več avtorjev je predstavilo uporabo MCM za uporabo v satelitih, tako komunikacijskih kot "opazovalnih", ki morajo spraviti velike količine podatkov. Zahteve po spominu v nekaterih primerih presegajo nakaj 100 Gbit, predvsem za geostacionarne satelite. MCM začenjajo tako po karakteristikah (lahki, kompaktni in odporni na sevanje) kot po številu podatkov, ki jih lahko "spravijo", tekmovati z magnetnimi spomini (trakovi ali diski) ali optičnimi diski. Njihova prednost je predvsem v tem, da so brez gibljivih delov. Bodoči trendi so, kot so podali nekateri avtorji, med ostalim tudi tridimenzionalno zlaganje MCM drugega na drugega ali drugega poleg drugega tako, da dobimo tridimenzionalno "škatlico" - MCM cube - z visoko volumsko, ne samo ploskovno gostoto funkcij, ki še vedno zavzame majhen del površine plošče, na kateri se montira. N. Sinnadurai (Middlesex University, Anglija) je v svojem prispevku povedal, da bi morali predvsem za "vesoljske" aplikacije pretestirati in uporabljati organske polimerne zaščitne materiale, zaradi nizkih dielektričnosti in predvsem zaradi nižje teže tako enkapsuliranih MCM, čeprav to nasprotuje sedanji filozofiji o uporabi hermetičnih, to je kovinskih ali keramičnih ohišij. Omenil je zahtevo za te vrste aplikacij, to je nobene odpovedi v 25 letih.

A. M. Hirscherg (Coors Electronic Package Comp., ZDA) je zatrdil, da so keramični MCM trenutno najbolj razviti. Ta razvoj je bil financiran večinoma od komercialnih firm, medtem ko je vlada vlagala denar v glavnem v razvoj MCM-D in MCM-L. Prednosti MCM-C so predvsem v tem, da se lahko "zgradi" veliko število, tudi prek 100, prevodnih nivojev. Omenil je MCM na osnovi AlN z 93000 povezavami (vias) med nivoji in 800 m (skoraj kilometer!) pokopanih, to je zapečenih v keramičen substrat, prevodnih linij. H. Hentzell (IMC, Švedska) je govoril o MCM na tako imenovanih aktivnih ali pametnih (smart) substratih. Pri teh MCM je substrat silicijeva ploščica, na kateri so poleg povezav izdelani tudi logika in spominski elementi, zato je potrebno pritrditi manj silicijevih tabletk. Na ta način lahko zmanjšajo dimenzije MCM za več kot 50% v primerjavi s pasivnimi substrati, na katerih so samo povezave. Povedal je, da bi se teoretično lahko spravila vsa elektronika na silicijev substrat, vendar bi vezje postalo tako kompleksno, da bi bili izkoristki nesprejemljivo nizki. (Pripombe; pred nekaj leti je vojska oz. letalstvo Združenih držav pripravilo projekt za razvoj takih integriranih vezij, pri čemer bi bile posamezne tabletke velike tudi do 50 mm - wafer scale integration -, vendar ga zaradi problema izkoristka niso izpeljali. Še prej, v drugi polovici osemdesetih let, je imel isto idejo Sinclair, izumitelj in proizvajalec hišnih računalnikov, od katerih je bil verjetno najbolj znan in prodajan Spectrum).

W. K. Jones (Florida Int. University, ZDA), D. Lambert (Bull SA, Francija) in E. Bihler (IBM, Nemčija) so govorili o "mešanih" MCM, kjer se na večplastnih keramičnih substratih izdela večplastne tenkoplastne strukture na osnovi polimerov kot izolatorjev in bakra oz TiW/Au kot prevodnika (kombinacija MCM-C in MCM-D tehnologije). Pri tem da keramična podloga trdnost in dobro odvajanje toplote, polimerni dielektrik pa omogoča višjo frekvenco signalov zaradi nizke dielektričnosti. Nekaj referatov je poročalo o karakteristikah debeloplastnih uporov ali kondenzatorskih dielektrikov, ki so pokopani in žgani v večplastnih keramičnih strukturah. Zanimiva (in nenavadna) je bila uporaba laserja za "risanje" prevodnih linij na AlN keramiki, o čemer je poročal Z. Illyefalvi-Vitez (Technical University of Budapest, Madžarska). AlN razpada na aluminij in dušik, ko je obsevan z laserjem. Po poti laserskega žarka se pod primerno nastavitvijo parametrov laserja Al izloči na površini keramike in tvori tenkoplastno prevodno sled s plastno upornostjo do 200 mohm/ . Širina teh linij je, vsaj teoretično, omejena samo z ostrino fokusa laserskega žarka. (Pripomba: to je isti efekt, ki otežuje lasersko doravnavanje debeloplastnih uporov na AlN substratih. Kovinski Al, ki lahko ostane v rezu, do neke mere kratko sklene prerezan del upora, kar povzroči nestabilnost uporovne vrednosti). G. Harsanyi (Univerza v Budimpešti, Madžarska) je obravnaval probleme zaradi elektromigracije v večplastnih MCM. Migracijo kovinskih ionov skozi dielektrik povzroča vlaga, ki lahko ostane na vezjih ali pa je absorbirana v polimerih. Ta problem se bo verjetno še poslabšal, ko bodo namesto CFC topil za čiščnje ostankov organskih fluksov po spajkanju začeli uporabljati topila na osnovi vode za vodotopne flukse.

V sekciji o debeloplastnih senzorjih je bil predstavljen tudi naš referat, ki je obravnaval preiskave komercialnih debeloplastnih materialov z namenom, da bi našli materiale z optimalno kombinacijo karakteristik za uporabo v senzorjih temperature (termoelementi, narejeni z debeloplastnimi prevodniki) in upogiba (debeloplastni upori z visoko odvisnostjo spremembe upornosti od deformacije). R. Dell'Acqua (MiTeCo, Italija) in S. Mergui (Florida University, ZDA) sta prikazala pregled debeloplastnih senzorskih materialov tako na osnovi keramike kot organskih polimerov. Poudarjena je bila predvsem potreba po večji zanesljivosti, ponovljivosti in ceni, pristopni za splošno uporabo. L. J. Golonka (Technical University of Wroclaw, Poljska) je poročal o debeloplastnem elektrolitskem sonzorju za detekcijo žveplovega dioksida. Trdni elektrolit je bil K_2SO_4, referenčna elektroda pa Ag/Ag_2SO_4/. M. Somora (Technical University of Kosice, Slovaška) je poročal o uporabi debeloplastnih uporovnih materialov na osnovi RuO_2 za sekundarne temperaturne senzorje za zelo nizke temperature, pod 1 K. J. Minalgiene (Hibridas Enterprise, Litva) in S. Achmatowicz (Institute of Electronic Materials Techn.,

Poljska) sta predstavila razvoj fotoobčutljivih debeloplastnih materialov, ki omogočajo s postopki foto litografije izdelavo zelo gostih večplastnih vezij z ločljivostjo prevodnih linij pod 50 μm in lukenj (vias) v dielektriki okrog ali pod 100 μm. Pri tem razvoju sodelujejo trije "vzhodni" inštituti iz Litve, Ukrajine in Poljske, poleg tega pa še firma Mozaik Technology Ventures iz Anglije. (Pripomba: take materiale je firma Du Pont ponudila prvič že v sedemdesetih letih pod imenom FODEL, nato pa ponovno pred okrog tremi leti. Ker pri omenjenem razvoju teh materialov sodeluje tudi S. Muckett - firma Mozaik iz Anglije -, ki je "povezana" z Electro Science Labs., znanim proizvajalcem debeloplastnih materialov, sklepam, da bo te materiale po končanem razvoju pričela prodajati ESL).

Dr. Marko Hrovat, dipl. ing.
Institut Jožef Stefan
Jamova 39, 61000 Ljubljana

VESTI, NEWS

KOREA'S SEMICON INDUSTRY WILL CONTINUE STRONG GROWTH

The Seoul based **Korea Semiconductor Industry Association (KSIA)** predicts **the industry will show a healthy 37% growth over 1993, reaching US$7.24 billion** this year. Last year, it registered $5.26 billion in sales, a 61% increase over the previous year.

"Among the U.S. dealers, Korean DRAMs are recognized as No. 1 in terms of quality and price," said Kim Chi-Luck, KSIA's president. This reputation, he added, should enable Korean chip makers to enjoy a favorable business environment, for some time to come. Also, he said, the Korean makers' **strong commitment to mass production could give them an edge over Japanese rivals,** especially in the memory business, where the key selling point is low unit price.

Kim dismissed the possibility that trade friction with foregin countries could result from a sharp rise in exports, "because Korean memory producers do not sell their products under production cost and do not have a monopoly in over-seas markets".

To avoid other possible trade conflicts, Korea's government is preparing details of the Korea Chip Protection Law enacted last year and is studying ways to improve the tariff structure in the sector, Kim said.

He also noted that KSIA and its counterparts in the U.S. and European Union have agreed to eliminate tariffs on semiconductor devices and equipment for five years after the Urugay Round Tariff accord. He said the pact should increase the industry's exports.

Electronics, March 1994

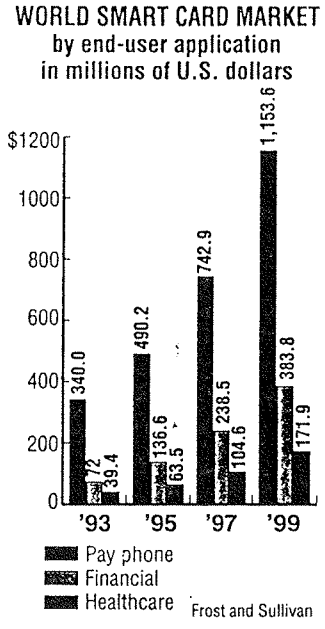
TI Europe attacks electronic money chip market with encryption protocol

Texas Instruments Europe is challenging market leaders **SGS Thomson Microelectronics SA** of Paris and **Motorola Inc.** of Schaumburg, Ill., in an effort to capture half Europe's sales of electronic money microcontroller chips. The chips are used in financial transaction cards which enable banks and credit card firms to identify the legitimate user through a personal code that is scanned before any payment is authorized.

The Villeneuve Loubet - based firm has been working with Paris' **Schlumberger SA** to develop the non-volatile EPROM memory chip family that is the basis of its pay card technology in which secure data encryption is a key element, said Sghaier Noury, TI's microcontroller manager for Europe.

He said that **within 18 months, TI will have a new, even more sophisticated encryption protocol ready that will provide a higher degree of security for the user.**

"Data encrypted transaction is going to be the driving force in tomorrow's payments cards," said Noury. "The business person is becoming increasingly nomadic. Just as he wants to use his mobile phono wherever he



The smart card markers for pay phone, financial and healthcare applications will grow at compound annual growth rates of 22%, 32.5% and 27.6%, respectively, according to Girish Rishi, a senior analyst at Frost and Sullivan Market Intelligence in Mountain View, Calif.

happens to be, he needs to access confidential data - from an office database or his personal bank account - at any time or place. That's why encryption is so important."

He added, "The pay card market is developing much faster in Europe then elsewhere. (The U.S. market) has regarded a switch to the microprocessor-memory chip on a 'smart card' (from magnetic strip cards) as too costly. But now, losses due to forgery are so huge that the mood is changing."

Electronics, March 1994

Semiconductors allow 25-GHz transit frequencies

The semiconductor group of Munich-based **Siemens AG** has introduced a new process technology named B6HF, which allows transit frequencies of more than 25 GHz. Unitl now these extremely high frequencies were a domain of gallium arsenide (GaAs).

B6HF offers gate delay times of 25 picoseconds at 1.2 microAmperes and 70 ps at 100 µA. In this technology, **structures of 0.8 - microns can be realized with noise factors of 1.1 dB at 1.8 GHz,** making them suitable for fiber-optic transmission systems running at 10 Gbits/s.

The effective emitter width is said to be 0.4 micron.

"B6HF is the only silicon technology in the world that offers a transit frequency of more than 25 GHz," said Rolf-Juergen Bruess, head of marketing for communications ICs at Siemens.

The company plans to develop ECL gate arrays with complexities of 3.000 and 6.000 gates this year.

Siemens handles its bipolar B6HF process on its CMOS process lines. Except for the precipitation of the Epi layer, the B6HF process is fully compatible to the 0.8 - micron CMOS process.

Electronics, March 1994

Siemens sees high demand for communications ICs

Communication ICs for mobile communications, trunk switches, public branch exchanges and integrated services digital networks (ISDN) have become leading sellers in the Munich headquarters of **Siemens AG's** semiconductor group.

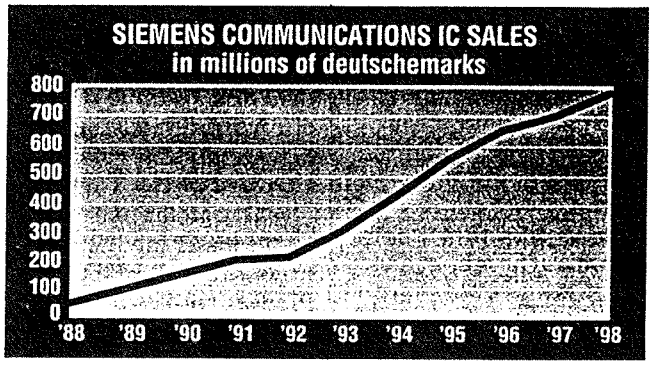
While other divisions of the semiconductor group struggle to make a profit, the communications ICs division has been in the black since the last fiscal year (ending in September), said Rolf- Juergen Bruess, senior marketing manager of communication ICs at Siemens. He said that **within the last two years, the company's communications ICs sales will have more than doubled to DM400 million (US$235 million) by the end of this fiscal year.** "Our strong growth is based on our structural strength," Breuss asserted. "There is no other manufacturer who offers such a broad spectrum of communications ICs."

Siemens will sell more than 500.000 chip sets for global system for mobile communications (GSM) standard terminals and between 25 to 30 million high-frequency ICs this year. **Due to the high demand for third-generation GSM ICs, there are shortages in this sector.**

Within the next four to five years Siemens plans to get a GSM market share of 17%. At the beginning of 1996, the next GSM chip set generation will be presented to the market. The whole GSM phone will then consist of only tree high-frequency ICs and two digital ICs, plus EEPROM and RAM.

Another major growth market is in digital European cordless telephones (DECT), where Bruess expects a steep increase by mid- 1994:**"1995 will be the year of DECT. We are preparing to sell 250.000 DECT chip sets per month next year."**

The trunk switch, PBX and ISDN chip markets are also good business for the German semiconductor manufacturer. It expects to sell "several houndreds of thousand" of its IEC-Q, a single-chip solution for the ISDN-U interface with echo cancellation. The demand seems to be higher than Siemens' delivery capacity, and Bruess wants to expand the IEC-Q production volume to several million units per year in 1995. However, even though Bruess reports an "annual increase of more than 500% in chips for ISDN PC cards," the IEC-Q is not used for ISDN but mainly for digitally added main line (DAML) applications, which enable the transmission of two phone calls via one twisted pair cable.



Electronics, March 1994

Sanyo solar cell sets efficiency standard

Sanyo Electric Co. Ltd of Osaka is expanding its expertise in solar technology on two fronts - advanced technology and consumer marketing.

At the cutting-edge of solar-energy conversion technology, Sanyo has announced what it claims to be the world's most efficient solar cell - a 1-cm-square, thin-film device of polycrystalline silicon that has achieved an energy conversion rate 8.5%. When the device is used

in conjunction with conventional amorphous silicon cells, the conversion ratio can be increased to 13%. Sanyo said **the technology used is capable of a conversion ratio of as much as 20%,** but further development is needed.

Already developed and ready for shipment next month are Sanyo solar power generation panels for the Japanese residential market.

The shipping date is timed to coincide with a 1994 Japanese government subsidy program for homeowners upgrading their homes to solar power. Up to half the upgrade costs will be shouldered by the Japanese taxpayer.

A typical system costs approximately Y6 million (US$57.000). That includes solar cell module, solar inverter, electric power distribution panel, switches, installation hardware and dual kilowatt-hour meters: one to record power consumption, the other to track surplus power generation. Since passage of a 1992 law, surplus power can be sold by the homeowner to the local power company. Similar laws have been in effect in the U.S. for a number of years.

Electronics, March 1994

AMS joins ESPRIT Project "FAB 2000"

Austria Mikro Systeme International, together with ES2 in France, GEC-Plessey in the UK, Gressi of France and Siemens Germany will participate in the joint European ESPRIT project "FAB 2000", the aim of which is to develop new and refined fabrication methodologies for next generation of application specific integrated circuits to be implemented by the year 2000. The ultimate goal is to guarantee the competitiveness of the European semiconductor industry into the next century.

Although all the participants of the ESPRIT project come from full member states of the European Union (Austria will be full member as of January 1, 1995 after a resounding yes to join the EU), AMS has also been invited because of its profound IC manufacturing experience since the company is one of the few European semiconductor manufacturers that houses all necessary fabrication facilites "under one roof": Research and development, design, mask lithography, wafer fabrication, assembly and test.

Dr. Humbert Noll, head of the AMS research and development department:"As a result of the participation in the ESPRIT project AMS will provide highly specialized and valuable know-how and thus further strengthen its leading position in the field of mixed analogue/digital integrated circuits."

For more information, call: Schloss Premstätten
A-8141 Unterpremstätten, Austria
Telex 312547 ams a
FAX (03136) 52 501, 53 650
*(03136) 500-0**
Dr. Conrad Heberling, ext. 277

Microtip technology: the LCD market's next leader?

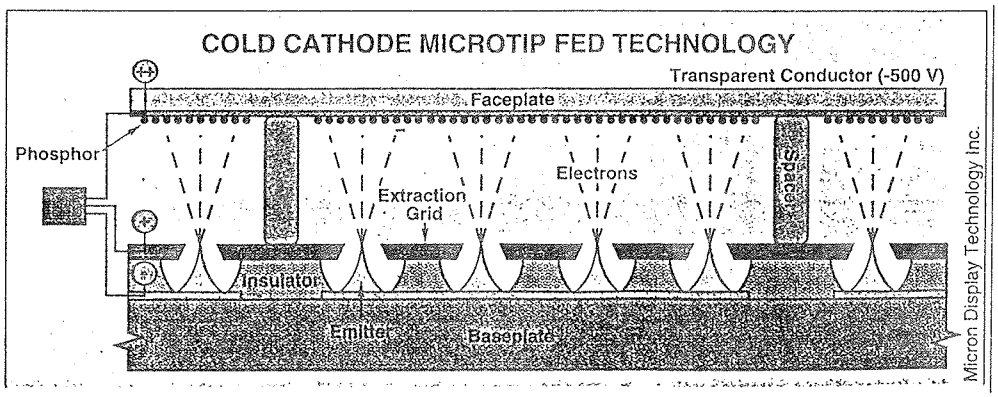
Microtip technology proponents hail the field-emission display (FED) technology as a high-performance, lightweight, low-power consumption FPD.

Pixel International of Rousset, France, is an active advancer of microtip technology, originally developed by **Laboratoire d'Electronique de Technologies et d'Instrumentation (LETI)** of France.

"Based on the preliminary work of Pixel and LETI, (microtip) is outstanding," said David Mentey, director of display industry research with **Stanford Resources Inc.** in San Jose, Calif. "It's sort of the dark horse (FDP technology) right now."

Pixel has lincensed its technology to **Futaba Corp.** of Mobara, Japan and **Texas Instruments Inc.** of Dallas.

Mentley also cited microtip work done by Boise-based **Micron Display Technology Inc.** It has three patents for cold-cathode FEDs, with 15 patents pending for its

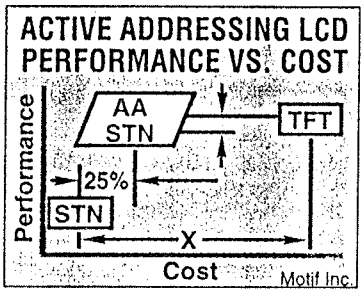


Micron's FEDs consist of a series of arrays composed of sets of cold-cathode FE devices (spindt emitters) opposing a phosphor- coated transparent plate-the space between the arrays and the plate has been evacuated. The spindt emitters are activated, and electrons are accelerated from the cold-cathode devices toward the phosphor-coated plate, which serves as an anode and has a positive voltage relative to the spindt emitter arrays. The phosphor is then induced into luminescence by electrons bombarding the phosphor surface, just as with conventional cathode ray tubes.

technology (see illustration). Micron estimates that a 10-inch, 50 fL, full-color FED would consume less than 5 watts of power.

Electronics, April 1994

MOTIF BRIDGES AM/PM LCD GAP



Motif Inc. of Wilsonville, Ore., is producing prototypes of its "active addressing" (AA) LCD technology and may begin production for OEMs by 1995, said Thomas Mills, marketing manager for Motif, a joint venture of **Motorola Inc.** in Schaumburg, Ill., and **In Focus Systems Inc.** of Tualatin, Ore. He said units will be evaluted in late Q2 or early Q3.

AA applies electrical signals to LCDs in a way that, Motif says, improves response time and contrast without limiting resolution or display size: **AA-LCDs enable STN-LCDs to nearly achieve the performance of TFT-LCDs at a reduced cost** (see chart). AA-LCD signals all pixels constantly and simultaneously using AA-ICs located off screen - cicuit complexity is in silicon to simplify manufacture.

The initial development phase of AA-LCD targeted high-end use, such as notebook computers. In March, In Focus announced it will inject new capital into the venture - US$ 1.5 million to $3.5 million - to cover ongoing costs, increase plant capacity and begin development of a second-phase AA-LCD for handheld game, entertainment and wireless applications.

Electronics, April 1994

EU alliance hopes to crack LCD market

A consortium of European companies, led by **Flat Panel Display**, a subsidiary of **Philips NV** of Eindhoven, have allied in a European Union Esprit program to develop ferroelectric LCD technology.

The companies - **Thomson-LCD, Thomson Consumer Electronics, Sagem, IBM France, DRA, Merck** and **Barco** - hope to improve the EU's dismal position in the the market for liquid crystal devices, components and sub-assemblies for panels.

The project aims to develop a customized integrated circuit, a touch input system and a ferroelectric LCD which, when combined, **will provide a low-cost, low-power module for use in a series of information technology products.**

The project is using two key advantages of ferroelectric technology: memory, the ability to retain an image with no power, and extremely low voltage.

Use of the memory capability will reduce the power consumption of the display and greatly prolong battery life. The use of low voltages will reduce both the size and cost of the ICs used in the drive electronics. These two key advantages make the proposed display modules ideally suited for a wide range of new and emerging portable IT products.

The project will also try to provide analog gray levels on ferroelectric LCDs, so the display can be used in video applications. Analog gray scale has not yet been sucessfully demonstrated in a passive ferroelectric LCD.

The project was launched in January 1994 and is expected to take two years to complete.

Electronics, April 1994

Hyundai begins construction of 64M DRAM plant

In mid-July, **Hyundai Electronics Industries Co.** of Seoul began construction of an 8-inch wafer fabrication plant for 64-Mbit dynamic random-access memory, in Ichon, Korea.

A US$ 1.24 billion investment, the plant is projected to be completed in June 1995. Featuring 0.35 micron process rules and a Class 1 cleanroom with less than 0.05 micron particles, the plant will be optimized for the production of 64-Mbit DRAMs. However, it will produce 16-Mbit DRAMs until late 1996 or 1997, when the market for 64-Mbit DRAMs is expected to mature. When the plant is completed, Hyundai's combined monthly production capacity of 16- Mbit DRAMs will reach 9.9 million units.

Hyundai expects to ship $930 million worth of 16-Mbit DRAMs to take 11% of the world's market share next year.

Electronics, July 1994

KOLEDAR PRIREDITEV 1994

SEPTEMBER

28.09.-30.09.1994
22nd INTERNATIONAL CONFERENCE ON MICROELECTRONICS, MIEL '94
30th SYMPOSIUM ON DEVICES AND MATERIALS, SD '94
TERME ZREČE, Rogla, Slovenija
(Info.: Meta Limpel, Tel.: 386 61 312 898)

OCTOBER

04.10.-06.04.1994
FIRST EUROPEAN DEPENDABLE COMPUTING CONFERENCE
Berlin, Germany
(Info.: Dr.David Powell, Tel.:(33) 61 33 62 87)

04.10.-07.10.1994
ESREF '94
5th EUROPEAN SYMPOSIUM ON RELIABILITY OF ELECTRON DEVICES, FAILURE
PHYSICS AND ANALYSIS
Glasgow, Scotland
(Info.: G.M.Brydon, Tel.: 44 604 408647)

10.10.-11.10.1994
BIPOLAR/BICMOS CIRCUITS & TECHNOLOGY MEETING
Minneapolis, MN, USA
(Info.: John S.Shier, VTC Inc., Tel.:(612)853-3292)

10.10.-13.10.1994
INTERNATIONAL CONFERENCE ON COMPUTER DESIGN:VLSI IN COMPUTERS & PROCESSORS
Cambridge, MA, USA
(Info.: IEEE Computer Society, Tel.:(202) 371-0101)

11.10.-13.10.1994
INTERNATIONAL DISPLAY RESEARCH CONFERENCE
Monterey, CA, USA
(info.: Ralph Nadel, Pallisades Institute (212) 620-3379)

16.10.1994
GALLIUM ARSENIDE RELIABILITY WORKSHOP
Philadelphia, PA, USA
(info.: Antony Immorlica, GE Co., (315) 456-3514)

16.10.-19.10.1994
GALLIUM ARSENIDE INTEGRATED CIRCUITS SYMPHOSIUM
Philadelphia, PA, USA
(Info.: Donald D'Avanzo, Hewlett-Packard, CA, Tel.: (707) 577-2644)

31.10.-04.11.1994
INTERNATIONAL CONFERENCE ON COMPUTER AIDED DESIGN
Santa Clara, CA, USA
(Info.: IEEE Computer Society, Tel.: (202) 371-0101)

NOVEMBER

14.11.-16.11.1994
TOPICAL CONFERENCE ON THE SYNTHESIS & PROCESSING OF ELECTRONIC MATERIALS
San Francisco, CA, USA
(Info.: Tim Anderson, Tel.: (904) 392-0881)

15.11.-16.11.1994
SEMICONDUCTOR MANUFACTURING CONFERENCE & WORKSHOP
Cambridge, MA, USA
(Info.: Margaret Bachmeyer, Tel.: (202) 457-9584)

DECEMBER

05.12.-09.12.1994
INTERNATIONAL CONFERENCE ON PHOTOVOLTAIC ENERGY CONVERSION
Waikoloa, HI
(Info.: Dennis J.Flood, Cleveland, Ohio, Tel.: (216) 433-2303)

NAVODILA AVTORJEM

Informacije MIDEM je znanstveno-strokovno-društvena publikacija Strokovnega društva za mikroelektroniko, elektronske sestavne dele in materiale-MIDEM. Časopis objavlja prispevke domačih in tujih avtorjev, še posebej članov MIDEM, s področja mikroelektronike, elektronskih sestavnih delov in materialov, ki so lahko:

izvirni znanstveni članki, predhodna sporočila, pregledni članki, razprave z znanstvenih in strokovnih posvetovanj in strokovni članki.

Članki bodo recenzirani.

Časopis objavlja tudi novice iz stroke, vesti iz delovnih organizacij, inštitutov in fakultet, obvestila o akcijah društva MIDEM in njegovih članov ter druge relevantne prispevke.

Strokovni prispevki morajo biti pripravljeni na naslednji način

- 1. Naslov dela, imena in priimki avtorjev brez titul.
- 2. Ključne besede in povzetek (največ 250 besed).
- 3. Naslov dela v angleščini.
- 4. Ključne besede v angleščini (Key words) in podaljšani povzetek (Extended Abstract) v angleščini.
- 5. Uvod, glavni del, zaključek, zahvale, dodatki in literatura.
- 6. Imena in priimki avtorjev, titule in naslovi delovnih organizacij, v katerih so zaposleni.

Ostala splošna navodila

1. V članku je potrebno uporabljati SI sistem enot oz. v oklepaju navesti alternativne enote.

2. Risbe je potrebno izdelati s tušem na pavs ali belem papirju. Širina risb naj bo do 7.5 oz. 15 cm. Vsaka risba, tabela ali fotografija naj ima številko in podnapis, ki označuje njeno vsebino. Risb, tabel in fotografij ni potrebno lepiti med tekst, ampak jih je potrebno ločeno priložiti članku. V tekstu je potrebno označiti mesto, kjer jih je potrebno vstaviti.

3. Delo je lahko napisano in bo objavljeno v kateremkoli jugoslovanskem jeziku v latinici in v angleščini.

Uredniški odbor ne bo sprejel strokovnih člankov, ki ne bodo poslani v dveh izvodih.

Avtorji, ki pripravljajo besedilo v urejevalnikih besedil, lahko pošljejo zapis datoteke na disketi (1.2 ali 1.44) v formatih ASCII, wordstar (3.4, 4.0), wordperfect, word, ker bo besedilo oblikovano v programu Ventura 2.0. Grafične datoteke so lahko v formatu HPL, SLD (AutoCAD), PCX ali IMG/GEM.

Avtorji so v celoti odgovorni za vsebino objavljenega sestavka. Rokopisov ne vračamo.

Rokopise pošljite na naslov

Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 61000 Ljubljana

UPUTE AUTORIMA

Informacije MIDEM je znanstveno-stručno-društvena publikacija Stručnog društva za mikroelektroniku, elektronske sestavne dijelove i materijale - MIDEM. Časopis objavljuje priloge domaćih i stranih autora, naročito članova MIDEM, s područja mikroelektronike, elektronskih sastavnih dijelova in materijala koji mogu biti:

izvorni znanstveni članci, predhodna priopćenja, pregledni članci, izlaganja sa znanstvenih i stručnih skupova i stručni članci.

Članci će biti recenzirani.

Časopis također objavljuje novosti iz struke, obavijesti iz radnih organizacija, instituta i fakulteta, obavijesti o akcijama društva MIDEM i njegovih članova i druge relevantne obavijesti.

Stručni članci moraju biti pripremljeni kako slijedi

- 1. Naslov članka, imena i prezimena autora bez titula.
- 2. Ključne riječi i sažetak (najviše 250 riječi).
- 3. Naslov članka na engleskom jeziku.
- 4. Ključne riječi na engleskom jeziku (3Key Words) i produženi sažetak (Extended Abstract) na engleskom jeziku.
- 5. Uvod, glavni dio, zaključni dio, zahvale, dodaci i literatura.
- 6. Imena i prezimena autora, titule i naslovi institucija u kojima su zaposleni.

Ostale opšte upute

1. U prilogu treba upotrebljavati SI sistem jedinica od. u zagradi navesti alternativne jedinice.

2. Crteže treba izraditi tušem na pausu ili bijelom papiru. Širina crteža neka bude do 7.5 odnosno 15 cm. Svaki crtež, tablica ili fotografija treba imati broj i naziv koji označuje njen sadržaj. Crteže, tabele i fotografije nije potrebno lijepiti u tekst, već ih priložiti odvojeno, a u tekstu samo naznačiti mjesto gdje dolaze.

3. Rad može biti pisan i biti će objavljen na bilo kojem od jugoslavenskih jezika u latinici i na engleskom jeziku.

Autori mogu poslati radove na disketama (1.2 ili 1.44) u formatima tekst procesora ASCII, wordstar (3.4. i 4.0), word, wordperfect pošto će biti tekst dalje obraden u Venturi 2.0. Grafičke datoteke mogu biti u formatu HPL, SLD (AutoCAD), PCX ili IMG/GEM.

Urednički odbor će odbiti sve radove koji neće biti poslani u dva primjerka.

Za sadržaj članaka autori odgovaraju u potpunosti. Rukopisi se na vraćaju.

Rukopise šaljite na adresu:

Uredništvo Informacije MIDEM
Elektrotehnična zveza Slovenije
Dunajska 10, 61000 Ljubljana
Slovenija

INFORMATION FOR CONTRIBUTORS

Informacije MIDEM is professional-scientific-social publication of Professional Society for Microelectronics, Electronic Components and Materials. In the Journal contributions of domestic and foreign authors, especially members of MIDEM, are published covering field of microelectronics, electronic components and materials. These contributions may be:

original scientific papers, preliminary communications, reviews, conference papers and professional papers.

All manuscripts are subject to reviews.

Scientific news, news from the companies, institutes and universities, reports on actions of MIDEM Society and its members as well as other relevant contributions are also welcome.

Each contribution should include the following specific components:

- 1. Title of the paper and authors' names.
- 2. Key Words and Abstract (not more than 250 words).
- 3. Introduction, main text, conclusion, acknowledgements, appendix and references.
- 4. Authors' names, titles and complete company or institution adress.

General information

1. Authors should use SI units and provide alternative units in parentheses wherever necessary.

2. Illustrations should be in black on white or tracing paper. Their width should be up to 7.5 or 15 cm. Each illustration, table or photograph should be numbered and with legend added. Illustrations, tables and photografphs are not to be placed into the text but added separatelly. Hower, their position in the text should be clearly marked.

3. Contributions may be written and will be published in any Yugoslav language and in english.

Authors may send their files on formatted diskettes (1.2 or 1.44) in ASCII, wordstar (3.4 or 4.0), word, wordperfect as text will be formated in Ventura 2.0. Graphics may be in HPL, SLD (AutoCAD), PCX or IMG/GEM formats.

Papers will not be accepted unless two copies are received.

Authors are fully responsible for the content of the paper. Manuscripts are not returned.

Contributions are to be sent to the address:

Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 61000 Ljubljana,
Slovenia

2.2 Usmerjalne diode

1	2	3	4
2.2.1	Splošni izrazi		
2.2.1.1	• Direktni (propusni) smer • Propusni (direktni) smjer • Директна насока • Prepustna smer	147–0/IC–1.1 • Forward direction • Sens direct	Smer trajnega enosmernega toka, v kateri ima polprevodniška dioda manjšo upornost.
2.2.1.2	• Inverzni (nepropusni) smer • Zaporni (inverzni) smjer • Инверзна насока • Zaporna smer, inverzna smer	147–0/IC–1.2 • Reverse direction • Sens invers	Smer trajnega enosmernega toka, v katerem ima polprevodniška dioda večjo upornost.
2.2.1.3	• Grana ispravljačkog bloka (sloga) • Grana ispravljačkog sloga • Гранка на исправувачки блок • Veja usmerjalnega stavka	147–0/IC–1.3 • Rectifier stack arm • Bras d'un bloc de redressement	Del usmerjalnega stavka, ki je priključen med dva priključka in ima lastnost, da prevaja tok pretežno samo v eni smeri. Opomba: Veja usmerjalnega stavka, sestavljena iz ene ali več diod, vezanih zaporedno, vzporedno ali zaporedno-vzporedno, da delujejo kot enota. To pomeni, da je veja usmerjalnega stavka lahko celotni usmerjalni stavek ali samo njegov del.
2.2.1.4	• Anodni priključak, anoda (poluprovodničke ispravljačke diode ili ispravljačkog bloka) • Anodni priključak, anoda poluvodičke ispravljačke diode ili ispravljačkog sloga	147–0/IC–1.4 • Anode terminal (of a semiconductor rectifier diode or rectifier stack) • Borne d'anode (d'une diode de redressement á semicondicteurs ou d'un bloc de redressement)	Priključek, v katerega teče prepustni tok iz zunanjega tokokroga.

1	2	3	4
	• Анoден приклучок (на полупроводничка насочувачка диода или на насочувачки блок) • Anodni priključek (polprevodniške usmerjalne diode ali usmerjalnega stavka)		
2.2.1.5	• Katodni priključak, katoda (poluprovodničke ispravljačke diode ili ispravljačkog bloka) • Katodni priključak, katoda poluvodičke ispravljačke diode ili ispravljačkog sloga • Катоден приклучок (на полупроводничка насочувачка диода или на насочувачки блок) • Katodni priključek (polprevodniške usmerjalne diode ali usmerjalnega stavka)	147–0/IC–1.5 • Cathode terminal (of a semiconductor rectifier diode or rectifier stack) • Borne de cathode (d'une diode de redressement à semiconducteurs ou d'un bloc de redressement)	Priključek, iz katerega teče prepustni tok v zunanji tokokrog.
2.2.2	Izrazi, ki se nanašajo na mejne vrednosti in karakteristike		
2.2.2.1	• Direktni (propusni) napon • Propusni (direktni) napon • Директен напон • Prepustna napetost	147–0/IC–2.1 • Forward voltage • Tension directe	Napetost, ki nastane na priključkih zaradi prehoda toka v prepustni smeri.

1	2	3	4
2.2.2.2	• Vršni radni inverzni (nepropusni) napon • Vršni radni zaporni (inverzni) napon • Врвен работен инверзен напон • Temenska delovna zaporna napetost, temenska delovna inverzna napetost	147–0/IC–2.2 • Crest (peak) working reverse voltage • Tension inverse de crête	Največja trenutna vrednost zaporne napetosti, ki nastane na polprevodniški usmerjalni diodi ali veji usmerjalnega stavka, izključojoč vse ponovitvene in neponovitvene prehodne napetosti.
2.2.2.3	• Periodični vršni inverzni (nepropusni) napon • Periodični vršni zaporni (inverzni) napon • Периодичен врвен инверзен напон • Ponovitvena temenska zaporna napetost, ponovitvena temenska inverzna napetost	147–0/IC–2.3 • Repetitive peak reverse voltage, maximum recurrent reverse voltage • Tension inverse de pointe répétitive	Največja trenutna vrednost zaporne napetosti, ki nastane na polprevodniški usmerjalni diodi ali veji usmerjalnega stavka, vključojoč vse ponovitvene in izključojoč vse neponovitvene napetosti.
2.2.2.4	• Neperiodični vršni inverzni (nepropusni) napon • Neperiodični vršni zaporni (inverzni) napon • Непериодичен врвен инверзен напон • Neponovitvena temenska zaporna napetost, neponovitvena temenska inverzna napetost	147–0/IC–2.4 • Non-repetitive peak reverse voltage, peak transient reverse voltage • Tension inverse de pointe non répétitive	Največja trenutna vrednost neponovitvene prehodne zaporne napetosti, ki nastane na polprevodniški usmerjalni diodi ali na veji usmerjalnega stavka. Opomba: Ponovitvena napetost je navadno funkcija vezja in povečuje izgubno moč elementa. Neponovitvena prehodna napetost se navadno pojavi zaradi zunanjega vzroka in lahko predpostavimo, da njen učinek popolnoma izgine, preden pride do naslednje prehodne napetosti.
2.2.2.5	• Konstantni (jednosmerni) inverzni (nepropusni) napon • Konstantni (istosmjerni) zaporni (inverzni) napon • Постојан инверзен напон • Trajna (enosmerna) zaporna napetost, trajna (enosmerna) inverzna napetost	147–0/IC–2.5 • Continuous (direct) reverse voltage • Tension inverse continue permanente	Vrednost trajne napetosti, priključena na diodo v zaporni smeri.

1	2	3	4
2.2.2.6	• Direktna (propusna) struja • Propusna (direktna) struja • Директна струја • Prepustni tok	147–0/IC–2.6 • Farward current • Courant direct	Tok, ki teče skozi diodo v smeri manjše upornosti.
2.2.2.7	• Srednja direktna (propusna) struja • Srednja propusna (direktna) struja • Средна директна струја • Povprečni prepustni tok	147–0/IC–2.7 • Mean forward current • Courant direct moyen	Povprečna vrednost prepustnega toka v celotni periodi.
2.2.2.8	• Periodična vršna direktna (propusna) struja • Periodična vršna propusna (direktna) struja • Периодична врвна директна струја • Ponovitveni temenski prepustni tok	147–0/IC–2.9 • Repetitive peak forward current • Courant direct de pointe répétitif	Temenska vrednost toka v prepustni smeri, vključojoč vse ponovitvene prehodne toke. Opomba: Razmerje tega toka in povprečne vrednosti toka v prepustni smeri dobimo s faktorjem, ki je odvisen od vezja in od oblike vala napajalne napetosti.
2.2.2.9	• Udarna neperiodična direktna (propusna) struja • Udarna neperiodična propusna (direktna) struja • Ударна (непериодична) директна струја • Udarni (neponovitveni) prepustni tok	147–0/IC–2.10 • Surge (non-repetitive) forward current • Courant direct non répétitif de surcharge accidentelle	Kratkotrajen impulz toka v prepustni smeri z določeno valovno obliko.
2.2.2.10	• Inverzna (nepropusna) struja • Zaporna (inverzna) struja • Инверзна струја • Zaporni tok, inverzni tok	147–0/IC–2.11 • Reverse current • Courant inverse	Celotni tok, ki teče skozi diodo, ko se nanjo pritisne označena zaporna napetost.

1	2	3	4
2.2.2.11	• Ukupni gubici snage • Ukupni gubici • Вкупни загуби на моќност • Celotna izgubna moč	147–0/IC–2.12 • Total power loss • Pertes totales en puissance	Vsota izgub, ki nastane pri podanih pogojih zaradi toka v prepustni in zaporni smeri.
2.2.2.12	• Udarna inverzna disipacija (ispravljačkih dioda s lavinskim i prinuđenim lavinskim probojem) • Udarni zaporni gubici (ispravljačkih dioda s lavinskim i prisilnim lavinskim probojem) • Ударна инверзна дисипација на моќност (кај насочувачки диоди со лавински пробив и насочувачки диоди со контролиран лавински пробив) • Udarna zaporna izgubna moč (plazovnih in krmiljenih plazovnih usmerjalnih diod)	147–0B/IC–2.13 • Surge reverse power dissipation (of avalanche and controlled avalanche rectifier diodes) • Puissance de surcharge accidentelle dissipée en inverse (des diodes de redressement à avalanche et des diodes de redressement à avalanche contrôlée)	Izgubna moč diode kot posledica trenutne preobremenitve pri delovanju v zaporni smeri.
2.2.2.13	• Disipacija u direktnom smeru, propusna disipacija (ispravljačkih dioda s lavinskim i prinudenim lavinskim probojem) • Propusni gubici ispravljačkih dioda s lavinskim i prisilnim lavinskim probojem • Директна дисипација на моќност (кај насочувачки диоди со лавински и контролиран лавински пробив) • Prepustna izgubna moč (plazovnih in krmiljenih plazovnih usmerjalnih diod)	147–0B/IC–2.14 • Forward power dissipation (of avalanche and controlled avalanche rectifier diodes) • Puissance dissipée en directe (des diodes de redressement à avalanche et des diodes de redressement à avalanche contrôlée)	Izgubna moč diode pri delovanju v prepustni smeri.