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Reducing the Length of the Test Sequence for Analog Test Signal Generation

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Abstract. In this paper we introduce a novel test signal generation method for the analog systems based on the SVM (support vector machine). Considering a circuit whose output signals cannot be classified with linear hyperplanes (i.e., the circuit has only small parametric faults), the responses of the normal instances are similar to those of the faulty instances, then the traditional test generation methods have difficulty generating the test signals. However, the SVM provides an effective result. Then we compress the test signals by measuring the Euclidean distance of different sample vectors obtained by the circuit instances in the feature space of SVM. It can reduce the length of the test sequence and save the cost of hardware and software in testing. A large number of experiments confirm that this method can ensure correct compression rates and precision of the test generation.

Keywords: analog system, support vector machine, fault, test signal generation

Zmanjšanje dolžine testnega zaporedja pri analognih vezjih

V članku je predlagan nov pristop pri testiranju analognih vezjih z metodo podpornih vektorjev. Pri vezjih, ki imajo le manjši del parametričnih napak, zaradi česar posledično ne moremo klasificirati izhodnih signalov z linearnimi ravninami, je odziv vezja z napako zelo podoben odzivu pravilnega vezja. Z uporabo predlagane metode lahko povečamo učinkovitost testiranja. Dolžino testnega zaporedja zmanjšamo z izračunom Evklidove razdalje med odzivom vezja na vhodne testne vektorje in s tem prihranimo pri času testiranja. Eksperimentalni rezultati na testnih vezjih potrjujejo pravilnost in točnost predlagane metode.

1 INTRODUCTION

Testing analog systems is difficult due to its complex transfer relation [1]. A key tool to facilitate analog systems testing is test signal generation [2-3]. Test signal generation is first introduced in digital systems testing. It generates test signals for the device under test (DUT), hence is a key component in automatic test equipments [4-6].

It is notable that analog test signal generation [7] differs from classic digital test signal generation. The fault models in digital circuits talk about 0-1 faults, delay faults, and bridge faults; while the fault models in analog circuits talk about continuous ranges of time and values [8-10].

The faults occurred in an analog system can be categorized into catastrophic faults (hard faults) and parametric faults (soft faults) [11]. The catastrophic faults are those that deviate significantly from the DUT normal specifications [12]. The parametric faults, however, deviate much less. Such subtlety of the parametric faults results in a highly mixed sampled space, which necessitates a non-linear classification [13]. Unfortunately, to our best knowledge, the current test signal generation methods [14-19] use a linear classification, hence, cannot effectively distinguish the parametric faults.

Long and Wang et al. introduced a test signal generation method in [17]. It is based on Support Vector Machine (SVM), a method of classifying small samples based on the statistical learning theory [20]. This method is proven to be efficient in dealing with our highly nonlinear classification problem.

However, if we use SVM for test signal generation directly, every *circuit instance* (a "circuit instance" is an instance of the DUT; it can be normal or has certain parametric fault(s)) that may need a unique test signal. Meanwhile, the test sequence for a DUT is constructed by concatenating the test signals of all circuit instances. As parametric faults may result in a huge number of circuit instances, the final test sequence may be too long, causing unaffordable test time cost.

To address this problem, in this paper, we propose a test signal reduction method which is based on measuring sample vectors' Euclidean distances in the SVM feature space.

The rest of the paper is organized as follows: Section II introduces the background on the SVM-based test signal generation method in [17]. Section III proposes

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our method on reducing the test sequence length and evaluates the method with the simulations. Section IV concludes the paper.

2 BACKGROUND

The test signal generation method in this paper works in three steps (see Fig. 1):

1) Construct the sampled space by sampling the impulse responses (a.k.a. *impulse response vector*) of the training circuit instances. These training circuit instances are *simulated* circuit instances which can be normal or faulty. The normal training circuit instances are labeled "passed"; while the faulty ones are labeled "failed". *Note, to simplify narration, in the rest of the paper, "faults" always refer to "parametric faults" unless explicitly denoted.*

2) Classify the sampled space to derive a hyperplane that divides the impulse responses of the "passed" training circuit instances from those of the "failed".

3) Obtain the test signals from the classification hyperplane found in step *2)*.

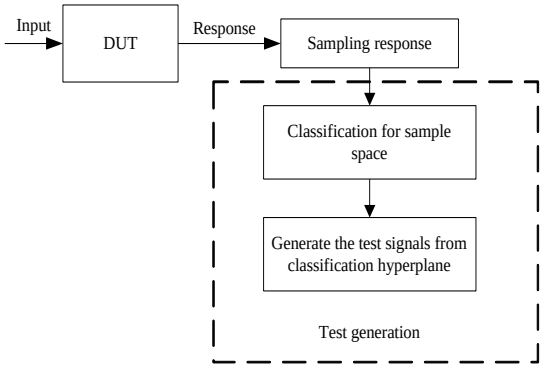

Figure 1. Test signal generation process

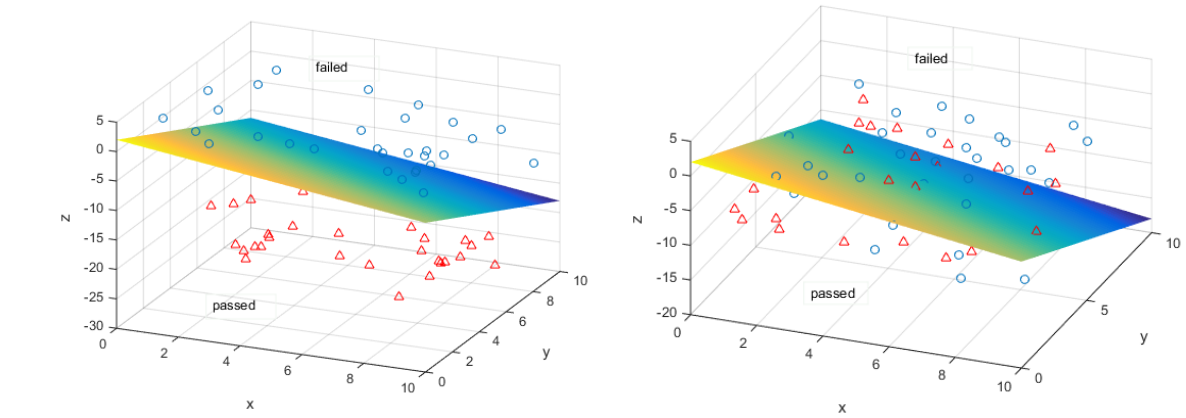

Figure 2. Linear classification accuracy: (a) slightly mixed sampled space (b) highly mixed sampled space

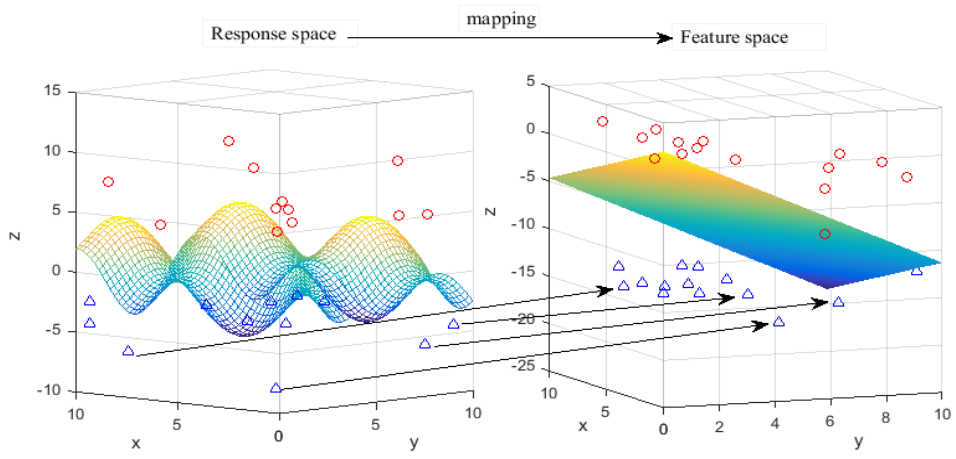

Figure 3. Basic idea of SVM

As mentioned above, in a constructed sampled space, the impulse response vectors of the "passed" and "failed" circuit instances can often be highly mixed, due to the subtlety of the parametric faults.

Such mixture is hard to classify with linear classification algorithms. This is illustrated by the comparison shown in Fig. 2 (a) and (b): with the same amount of the linear classification effort, the mis-classification rate rises as the sampled space becomes more mixed.

The drawback of the linear classification necessitates the use of non-linear classification [21]. A well-known efficient non-linear classification method is SVM [22, 23]. It applies the so-called kernel functions [18] to map a highly mixed sampled space to a higher-dimension feature space and then partition the training sets with an optimal (with maximized border margin) hyperplane, as illustrated in Fig. 3.

According to the related work [24], we apply SVM to classify the highly mixed sampled space with a hyperplane. Once this hyperplane is available, we generate the test signals using the test signal generation method of [17] .

In our test signal generation, the classification process job is to partition the sampled space with a proper hyperplane. This hyperplane serves as a basis for the test signal generation. Therefore, the classification accuracy can strongly effect the precision of our test signal generation. We choose SVM to achieve a high classification accuracy, considering the responses of the normal circuits are similar to those of the circuits with small parametric faults. After executing the classification process with SVM, we use an algorithm of the test signals generation to obtain the test signals from the classification hyperplane.

3 COMPRESSION OF THE TEST SIGNALS

3.1 Analysis

The SVM-based test signal generation can deal with the highly mixed sampled space (see Fig. 2(b)), but we know that each training circuit instance needs its unique test signal. It means that a test signal cannot be used to test more than one circuit instance (i.e., one kind of faulty/normal circuit). If there are hundreds of training circuit instances, we must generate the same number of the test signals. Then the test sequence (i.e., the concatenation of all the generated test signals) becomes too long when there are too many training circuit instances.

In practice, an analog system may have a huge number of the potential parametric faults, which correspond to the same number of the training circuit instances, and hence an unacceptably long test sequence. We need to find ways to compress the test sequence.

In this section we propose a method to test the multiple training circuit instances with a single test signal. This will reduce the total number of the test signals and shrink the test sequence.

Our heuristics run as follows. As described above, the SVM maps the sample vectors of a highly mixed sampled space to a higher-dimension feature space to simplify classification. Thus, from the perspective of classification, two sample vectors of the sampled space can be approximated as one, if they are close enough in the mapped feature space. In other words, a test signal can test several training circuit instances, if these instances sample vectors are close enough in the higher-dimension feature space. In this way, we can reduce the number of the test signals.

Formally, SVM uses the kernel functions to map the sampled space to the feature space defined by $K(\cdot,\cdot)$. Let H_p and H_q be the sample vectors for two different impulse responses, respectively. The SVM method maps H_p (H_q) in the sampled space to a new vector F_p (F_q) in the feature space.

Let F_{pi} denote the *i*-th element of F_p in the feature space. Then we have

$$F_{pi} = K(H_i, H_p), \qquad i \in N_{SV} \tag{1}$$

where H_i ($i \in N_{SV}$) is a support vector. The dimension of F_p is the number of the support vectors.

In the same way, F_{qi} denotes the *i*-th element of F_q in the feature space, so

$$F_{qi} = K(H_i, H_q), \qquad i \in N_{SV} \ . \tag{2}$$

The dimension of F_q is also the number of the support vectors.

Then the Euclidean distance between F_p and F_q is

$$d(F_p, F_q) = \sqrt{\sum_{i \in N_{sv}} (F_{pi} - F_{qi})^2} \ . \tag{3}$$

If F_p is close enough to F_q, i.e., $d(F_p, F_q) \approx 0$, then

$$F_{pi} - F_{qi} \approx 0, \quad i \in N_{sv} . \tag{4}$$

This implies

$$a_i y_i (F_{pi} - F_{qi}) \approx 0, \quad i \in N_{sv} . \tag{5}$$

Consequently

$$\begin{aligned} & t(H_p) - t(H_q) \\ &= \sum_{i \in N_{sv}} a_i y_i K(H_i, H_p) - \sum_{i \in N_{sv}} a_i y_i K(H_i, H_q) \\ &= \sum_{i \in N_{sv}} a_i y_i F_{pi} - \sum_{i \in N_{sv}} a_i y_i F_{qi} \\ &\approx 0. \end{aligned} \tag{6}$$

According to reference [17], the test signal for H_p is

$$c_p = t(H_p) \times (H_p{}^T)^{-1} . \tag{7}$$

If we use c_p to test H_q, then

$$t_{c_p}(H_q) = c_p \times H_q{}^T = t(H_p) \times (H_p{}^T)^{-1} \times H_q{}^T \ . \tag{8}$$

Here, $t_{c_p}(H_q)$ is the value of t in [17] when we use c_p to test H_q.

According to Equation (6), $t(H_p) \approx t(H_q)$, hence Equation (8) can be transformed into

$$t_{c_p}(H_q) \approx t(H_q) \times (H_p{}^T)^{-1} \times H_q{}^T . \quad (9)$$

Thus, if in addition to the requirement that F_p and F_q are close enough, H_p and H_q are also close enough. It is because that $d(F_p, F_q) \approx 0$ can result in Equation (4). Every element of F_p derived from a support vector is almost equal to an element of F_q derived from the same support vector. For every support vector, Equation (4) must be tenable to meet the situation $d(F_p, F_q) \approx 0$, so $H_p \approx H_q$ comes into existence with the highest probability. A large number of experiments in Section III can validate this highest probability. Then Equation (9) can be transformed to

$$t_{c_p}(H_q) \approx t(H_q) . \quad (10)$$

This means we can use c_p instead of c_q to test H_q, given F_p and F_q are close enough, and H_p and H_q are close enough. Thus we can reuse the test signal for multiple sample vectors. This will shrink the length of the final test sequence.

Then the first step for reducing the length of the test sequence is to measure the Euclidean distance of different sample vectors. The distance measurement is performed in the feature space, after mapping the response space to the feature space by SVM. The second step for reducing the length of the test sequence is to find the sample vectors whose Euclidean distance is small. To simplify narration, in the rest of the paper, we will use "close" to show the meaning of "small Euclidean distance". Then we can use the test signal of one sample vector to test other close sample vectors, for reducing the number of the test signals and the length of the test sequence. The next section will show the process of reducing the length of the test sequence.

3.2 The process of compression

Suppose that the original sampled space is $S=(H_1,\cdots H_i,\cdots H_n)$, where H_i is a sample vector for an impulse response. Suppose our SVM maps S into $F=(F_1,\cdots F_i,\cdots F_n)$ in the feature space. Per our design described in the previous subsection, for any two close enough sample vectors H_i and H_j in S, if their corresponding feature space vectors F_i and F_j are also close enough, then they can share the same test signal.

Thus, if we define the following distance metric

$$d_{ij} = d(F_i, F_j) , \quad (11)$$

where $d(\cdot,\cdot)$ is the Euclidean distance, we can then cluster the vectors $\{H_i\}$ in S according to d_{ij}. Once clustering is done, we pick only one vector from each cluster to construct a new sampled space S_{new} to replace S. S_{new} is the compressed subspace, as it has less vectors.

Then we use the SVM-based test signal generation method [17] to generate the test sequence for S_{new}, and use this test sequence to test the un-compressed sampled space S. The length of the test sequence for S_{new} is longer than S, because the number of the sample vectors in S_{new} is less then S. Then the compression can be achieved.

Formally, the above compression algorithm runs iteratively. In the ith iteration (i = 1, 2, …), we do the following three steps:

1) $S_{new} = (H_1, H_2, \ldots, H_i)$. If i achieves the last H in S, then halt.

2) Check all remaining vectors $H_{i+1}, H_{i+2}, \ldots$, in S one by one. If and only if a vector H_j has a distance $d_{ij} > th\_dis$ from H_i, then H_j is appended to the end of S_{new}. Here d_{ij} is defined by Equation (11), and th_dis is the threshold distance for clustering.

3) Let S_{new} become the new S, and sequentially re-number the subscripts of vectors in S, so that the kth vector in S becomes the new H_k.

The process of constructing S_{new} is illustrated in Fig. 4.

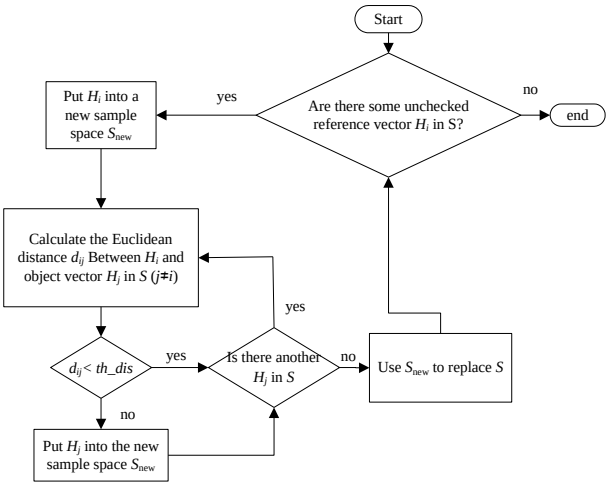

Figure 4. Process of constructing compressed subspace S_{new}

3.3 Examples

Without the loss of generality, we use the circuits in Fig. 5 to show the performance of the SVM-based test signal generation method, with compressing the test sequence. The example circuits include a two-pole active filter, three-pole active filter and five-pole active filter. Normal and faulty circuit instances can be built by assigning the normal and faulty parameters to the components. For a "normal" circuit, all the parameters fall inside their respective ranges of tolerance. A number of experiments for the circuits in Fig. 5 validate the inference from Equation (9) to (10).

We can acquire many sample vectors from the circuit shown in Fig. 5, and construct a sampled space. Each sample vector is obtained by sampling the impulse response of a circuit instance. The length of each sample vector is set to 30, so the sample vector can be written

as (h[0], h[1],⋯, h[28] , h[29]). In the training set, each sample vector is labeled as 'passed' or 'failed' according to the circuit specifications. The testing set classifications are derived by comparing the output response to a threshold derived from the hyperplane coefficients, following the SVM-based test signal generation method of [17].

Fig. 6 shows the misclassification rates for the circuits in Fig. 5 with the SVM-based test signal generation method. For the "passed" ("failed") population, the misclassification rate is defined as the ratio of the number of wrongly classified "passed" ("failed") instances to the number of the instances labeled as "passed" ("failed") [14]. The misclassification for the total population is calculated by summing the misclassification for the "passed" and "failed" population. Fig. 6 shows the performance of the test signal generation method of [17] with the proposed method (see Section III.A and B) in this paper. The corresponding sampled spaces are S_1~S_5 for the circuit in Fig. 5 (a), (b), and (c), respectively. *Note, S_1~S_5 are the label of the sampled spaces for the circuit in Fig. 5, so S_i indicates a different space when refer the different circuit.* S_1~S_5 in Fig. 6 are then compressed by our proposed method.

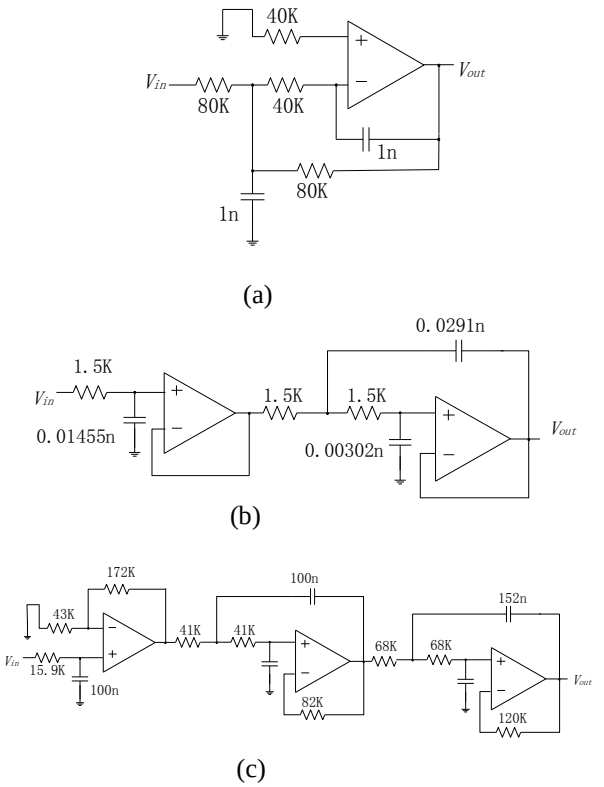

Figure 5. Example circuits: (a) two-pole active filter (b) three-pole active filter (c) five-pole active filter

Fig. 6 shows that the total misclassification rate for the training set of S_1 is 1.34% , and for the testing set of S_1 is 1.56%, when Fig. 5 (a) is the circuit under test. The total misclassification rates for S_2 ~S_5 , derived from Fig. 5(a), Fig. 5(b) and Fig. 5(c) are shown in Fig. 6, too. According to Fig. 6, the SVM-based test signal generation method [17] achieves low misclassification rates, hence ensures the precision of the test signal generation.

Table 1, on the other hand, evaluates the effectiveness of our proposed test signal set compression method.

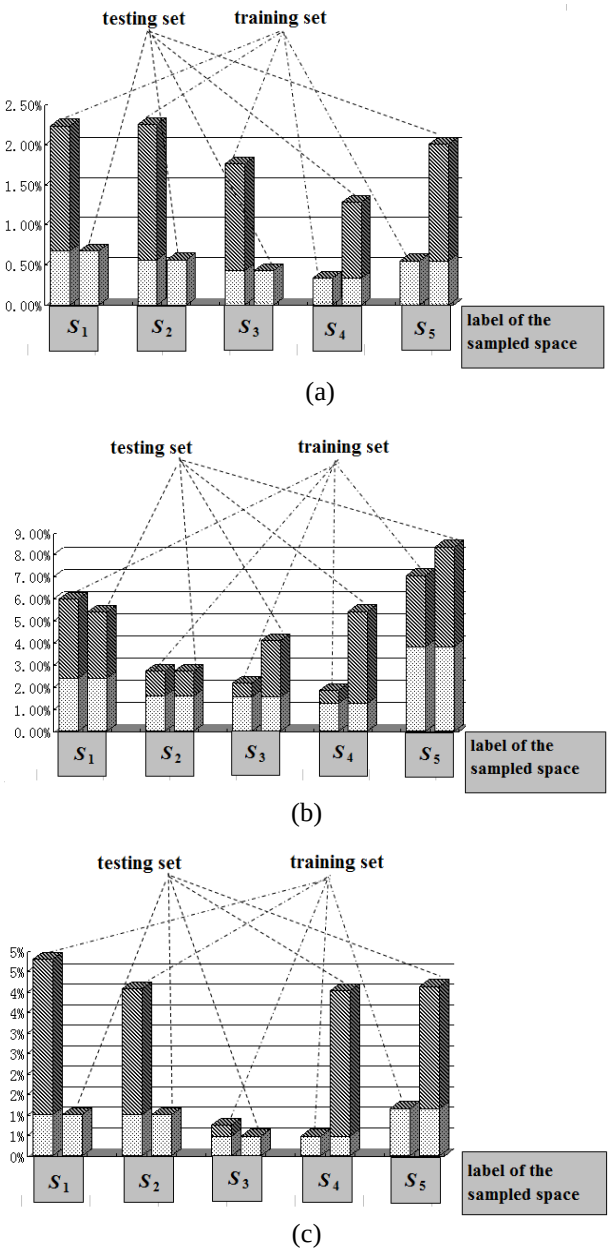

Figure 6. Misclassification rates for the circuits in Fig. 5 when using the SVM-based Test Signal Generation Method of [17] after compression: (a) Misclassification rates for Fig. 5(a); (b) Misclassification rates for Fig. 5(b); (c) Misclassification rates for Fig. 5(c).

Table 1. Test signal compression effectiveness

Label of the sampled space	Fig. 5 (a)		Fig. 5 (b)		Fig. 5 (c)	
	Compression rate of the test signal	Correct compression rate	Compression rate of the test signal	Correct compression rate	Compression rate of the test signal	Correct compression rate
S_1	36%	100%	16.25%	99.5%	29.67%	100%
S_2	29.2%	100%	16.84%	99.74%	32.8%	100%
S_3	24.75%	100%	15.68%	99.73%	34.71%	100%
S_4	21%	100%	16%	99.75%	24.67%	100%
S_5	31.2%	100%	16.22%	99.19%	32.8%	100%

Let S and S' be the sampled space before and after the compression. Let |TestSigSet(S)| be the number of the test signals for sampled space S. The compression rate means Compression Rate = 1 – |TestSigSet(S')| / |TestSigSet(S)|. Hence, a bigger compression rate of the test signal set means a less number of the test signals needed.

Let |CirInsSet(S)| be the number of all the circuit instances for S, and |CorrectClassifiedCirInsSet(S)| be the number of all the correctly classified circuit instances for S.

The correct compression rate refers to |CorrectClassifiedCirInsSet(S)| / |CirInsSet(S)| when we use the test signals of S' to test all the circuit instances in S. Table 1 confirms that our proposed method of compressing the test signal set can ensure high correct compression rates meanwhile shrinking the test signal set.

4 CONCLUSION

In this paper we proposed an effective test signal set compression method for the SVM-based test signal generation method. The SVM-based test signal generation method is effective in dealing with the non-linearity classification, when a large number of the parameter faults occurs. However, its resulted test signal set is too big. In our proposal, we measured the distance of different sample vectors in the feature space of SVM to find similar/redundant test signals. By replacing the similar test signals with one test signal, the test signal set can be compressed. Our simulations showed our proposal can effectively reduce the test signal set, while ensuring highly correct compression rates.

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