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Obnovitev članstva v strokovnem društvu MIDEM in iz tega izhajajoče ugodnosti in obveznosti

Spoštovani,

V svojem več desetletij dolgem obstoju in delovanju smo si prizadevali narediti društvo privlačno in koristno vsem članom.Z delovanjem društva ste se srečali tudi vi in se odločili, da se v društvo včlanite. Življenske poti, zaposlitev in strokovno zanimanje pa se z leti spreminjajo, najrazličnejši dogodki, izzivi in odločitve so vas morda usmerili v povsem druga področja in vaš interes za delovanje ali članstvo v društvu se je z leti močno spremenil, morda izginil. Morda pa vas aktivnosti društva kljub temu še vedno zanimajo, če ne drugače, kot spomin na prijetne čase, ki smo jih skupaj preživeli. Spremenili so se tudi naslovi in način komuniciranja.

Ker je seznam članstva postal dolg, očitno pa je, da mnogi nekdanji člani nimajo več interesa za sodelovanje v društvu, se je Izvršilni odbor društva odločil, da stanje članstva uredi in **vas zato prosi, da izpolnite in nam pošljete obrazec priložen na koncu revije.**

Naj vas ponovno spomnimo na ugodnosti, ki izhajajo iz vašega članstva. Kot član strokovnega društva prejemate revijo »Informacije MIDEM«, povabljeni ste na strokovne konference, kjer lahko predstavite svoje raziskovalne in razvojne dosežke ali srečate stare znance in nove, povabljene predavatelje s področja, ki vas zanima. O svojih dosežkih in problemih lahko poročate v strokovni reviji, ki ima ugleden IMPACT faktor.S svojimi predlogi lahko usmerjate delovanje društva.

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A NEW APPROACH IN TESTING ANALOG-TO-DIGITAL CONVERTERS

Martin Kollár

Technical University of Košice, Slovakia

Key words: testing ADC, integral non-linearity, differential non-linearity.

Abstract: This paper describes a new approach in testing static parameters of analog-to-digital converters (ADCs). The input of an ADC to be tested is connected to a generator of saw-tooth impulses. In comparison to ordinary approaches, the measured decision levels are not related to zero potential but to the decision levels of an additional ADC, which is of same type as tested ADC. Approximating principle-based test system, with a digital-to-analog converter (DAC) in the feedback, measures these differences, which are in the extreme case in the range of a few least significant bits (LSB) of tested (additional) ADC. It has been proposed a special algorithm, to which output codes of tested and additional ADC enter, to control this DAC, which output is added through a resistive divider to the input of additional ADC. By using this approach, there are no special requirements on the precision of input saw-tooth impulse generator and precision of the obtained integral non-linearity (INL), differential non-linearity (DNL) characteristics mainly depends on DAC used. It was also shown that using 8 bit DAC the precision is in the range of a few hundredths of LSB. By simulations with MATLAB, the theoretical considerations are verified.

Nov pristop k preizkušanju analogno-digitalnih pretvornikov

Kjučne besede: testiranje analogno-digitalnih pretvornikov, integralna nelinearnost, diferencialna nelinearnost

Izvleček: V prispevku opisujemo nov pristop k preizkušanju statičnih parametrov analogno-digitalnih pretvornikov (nadalje ADC) Vhod pretvornika, ki ga želimo preizkusiti, priklopimo na generator impulzov. V nasprotju s standardnim pristopom, kjer merjene nivoje primerjamo z ničelnim potencialom, jih v našem primeru primerjamo z drugim pretvornikom istega tipa kot ta, ki ga preizkušamo. Če upeljemo testni sistem tako, da dodamo digitalno-analogni pretvornik (DAC) v povratni vezavi, je ta sposoben meriti razlike, ki so v skrajnem primeru v območju zadnjega pomembnega bita (LSB - Least Significant Bit) testiranega (dodatnega) pretvornika. Predlagamo poseben algoritem, kjer izhodne kode testiranega in dodatnega pretvornika peljemo v DAC, katerega izhod preko uporovnega delilnika vrnemo nazaj v dodatni ADC. Pri takem pristopu točnost generatorja vhodnih impulzov ni pomembna in sta integralna in diferencialna nelinearnost odvisni predvsem od uporabljenega DAC pretvornika. Pokažemo, da je, če uporabimo 8 bitni DAC, točnost v območju nekaj stotink LSB. Teoretična predvidevanja smo potrdili s simulacijo z MATLABom.

Introduction and motivation

The price of mixed-signal integrated circuits is dominated by the ever-increasing testing cost of the analog blocks and converters. In particular, the full test of an ADC implies the determination of two kinds of parameters, the static errors linked to some deviations of the converter transfer function, and the dynamic features expressing the distortion and noise of the converted signal introduced by the converter. Static errors are generally deduced from a histogram-based test /1/ lying on a statistical analysis of the occurrence frequency for each output code, while dynamic parameters are usually evaluated from the spectral distribution of the converted signal, computed using a Fast Fourier Transformation (FFT) /2/.

Although the principles of both the static and dynamic tests have been well elaborated /1-3/ more work remains to be done on its feasibility issues. The test methods have been originally proposed under the assumption that the input source of reference signal is without uncertainties.

Let us assume that the full scale (FS) of a tested 12 bit ADC is in the range of a few V. Then the LSB will be in the range of a few mV. Since, the precision of signal generator should be at least two orders higher than LSB of ADC being tested /3/, in this case the generator absolute error should be in the range of a few hundredths of mV. A serious problem appears here because if it will be 16 bit ADC, the generator absolute error should be in the range of a few thousandths of mV.

To avoid such requirements on high precision of input generator a new approach will be presented in the following part of this letter. Originality consists in that all measurements of decision levels of tested ADC are not related to zero potential but to decision levels of an additional ADC. Thus, if this additional ADC is of same type as that to be tested, the maximal measured values will be in the range of a few LSB of tested ADC.

To be more detailed, let us assume a tested and additional ADC with an element of transfer characteristic according to Fig.1. By using an ordinary approach the voltages V_1, V_2 are measured in relation to zero potential, while using a new approach the voltages V_1',V_2' are measured in relation to a decision level output code i of an additional ADC. The voltages in both approaches have to be generated with the same absolute error. However, using new approach the acceptable relative error can be much greater than that in the ordinary approach.

The principle of this new method including also a possible hardware realization is depicted in the following sections.

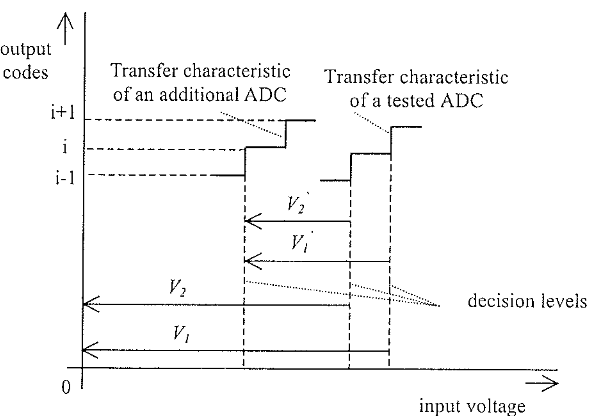


Figure 1. Principle of a new approach in testing ADCs

Principle of the new method

Fig. 2 shows a complete scheme of test system. As it can be seen the output codes of additional and tested ADC are processed in a microprocessor (µP). Also DAC, which output voltage through a precise resistive divider R_2/R_1 is added to input of tested ADC, is controlled by µP. According to Fig.1, by increasing input voltage from saw-tooth impulse generator, because of given transfer characteristics, the output code *i* at first will be generated by additional ADC and then with a time delay by tested ADC. However, by adding a voltage from resistive divider R_2/R_1 which is smoothly greater than V_2 the output code *i* at first will be generated by tested ADC and then with a time delay by additional ADC.

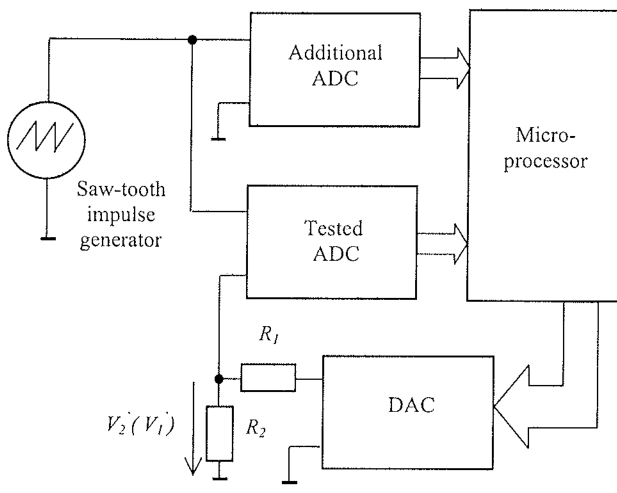


Figure 2. Block diagram of new test method

To achieve very short time of measurement of voltage difference V_2' approximating principle based conversion can be used. For example, by using 8 bits DAC the saw-tooth impulse must be generated 8 times by input generator. During the first impulse is only done a decision whether difference voltage is positive or negative. In case that it is positive value which means that output code *i* at first will be generated by additional ADC and then with a time delay by tested ADC, the voltage at resistive divider output will be set to FS/2, where FS is a full scale of DAC relating to resistive divider output. During the second impulse is tested by µP whether additional or tested ADC at first generates output code *i*. In case that again at first additional ADC generates output code *i*, the output voltage of resistive divider will be set to FS/2+FS/4. In opposite case this voltage will be set to FS/2-FS/4. Thus the output voltage of resistive divider is approximately set during the following six cycles. The approximating principle of conversion is well known /4/ therefore here only its summary is made.

In the same manner difference voltage V_1' is measured. Since, in this case the measurement is related to decision level of output code *i* from additional ADC and to decision level of output code *i*+1 from tested ADC, µP tests during each cycle, which one from these output codes is generated as first. From measured V_1', V_2' DNL of output code *i* is calculated using formula /4/

$$DNL(i) = \frac{\left(V_1' - V_2' - LSB\right)}{LSB} \quad (1)$$

where LSB is value of ideal least significant bit of tested (additional) ADC.

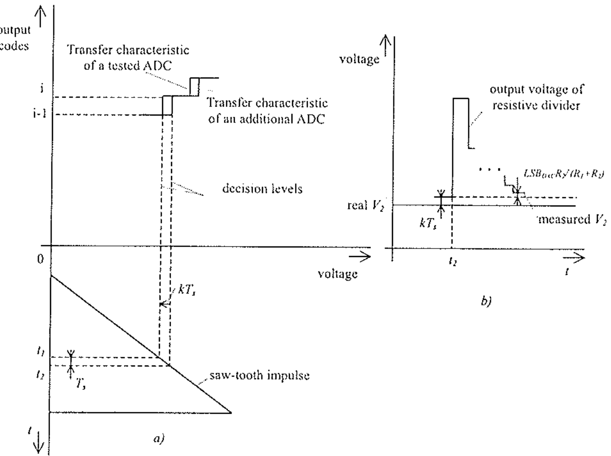


Figure 3. Precision of measured V_2'

From (1) it is clear that the precision of calculated DNL is determined by precision of measured V_1', V_2'. Fig.3a shows an example when the difference between actual decision levels of output code *i* of tested and additional ADC is smoothly lower than kT_s, where *k* is slope of saw-tooth impulse and T_s sampling period. In the moment t_1 output code *i*-1 is at output of additional and tested ADC, while in the moment t_2 it will be output code *i*. In this case, it is not possible to decide whether by tested or additional ADC at first was generated output code *i*. Thus, instead to be decreased, the output voltage of DAC will be increased about value FS/2^n, where *n* is actual step of approximating con-

version. In the remaining conversion steps this voltage will be increased but with the resolution $LSB_{DAC}.R_2/(R_1+R_2)$, where LSB_{DAC} is least significant bit of DAC, shown in Fig3b. Therefore the maximal error of measured $V_2^{'}$ is given by formula

$$\Delta_{V_2^{'}} = |kT_s| + \left| \frac{R_2}{(R_1+R_2)} LSB_{DAC} \right| \quad (2)$$

Since the same error is for measured $V_1^{'}$, the maximal error of measured DNL is given by formula

$$\Delta = 2\left(|kT_s| + \left| \frac{R_2}{(R_1+R_2)} LSB_{DAC} \right| \right) \quad (3)$$

If nominal parameters are such that kT_S is about hundredths of LSB, then an extreme change of slope about 100 % reflects to error $2kT_S$ and thus does not influence markedly the resultant precision.

Measurement of INL and DNL characteristic

It is described in previous section, the difference voltages $V_1^{'}, V_2^{'}$ have to be measured to obtain DNL in given output code *i*. In this section, an algorithm is described by using of which the complete INL and DNL characteristic is obtained passing the full scale of tested and additional ADC *s* times, where *s* is the number of bits of DAC used. By assuming that

$$\overline{DNL} = \begin{pmatrix} DNL\left(-\frac{N}{2}\right) \\ \cdot \\ \cdot \\ \cdot \\ DNL\left(\frac{N}{2}-1\right) \end{pmatrix} \text{ and } \overline{INL} = \begin{pmatrix} INL\left(-\frac{N}{2}+1\right) \\ \cdot \\ \cdot \\ \cdot \\ INL\left(\frac{N}{2}\right) \end{pmatrix}, \quad (4)$$

where *N* is the number of output codes of tested (additional) ADC we can write that

$$\overline{DNL} = \left(\overline{V}_1^{'} - \overline{V}_2^{'}\right) / LSB - \overline{E}, \quad (5)$$

where

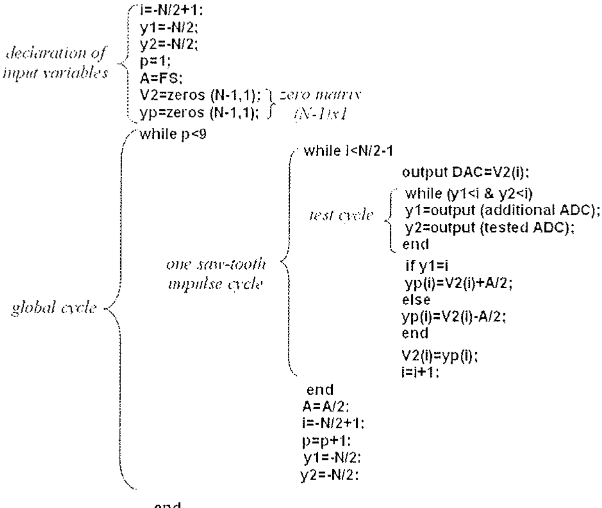
$$\overline{V}_1^{'} = \begin{pmatrix} V_1^{'}\left(-\frac{N}{2}\right) \\ \cdot \\ \cdot \\ \cdot \\ V_1^{'}\left(\frac{N}{2}-1\right) \end{pmatrix}, \quad \overline{V}_2^{'} = \begin{pmatrix} V_2^{'}\left(-\frac{N}{2}\right) \\ \cdot \\ \cdot \\ \cdot \\ V_2^{'}\left(\frac{N}{2}-1\right) \end{pmatrix} \text{ and } \overline{E} = \begin{pmatrix} 1 \\ \cdot \\ \cdot \\ \cdot \\ 1 \end{pmatrix}_{(N-1)x1}, \quad (6)$$

and

$$\overline{INL} = \begin{pmatrix} 1 & 0 & 0 & . & . & . & 0 \\ 1 & 1 & 0 & . & . & . & 0 \\ & & & . & . & & \\ & & & . & . & & \\ & & & . & . & & \\ 1 & 1 & 1 & . & . & . & 0 \\ 1 & 1 & 1 & . & . & . & 1 \end{pmatrix} \overline{DNL} \quad (7)$$

Then, for example, because $INL(i) = \sum_{r=-N/2}^{i-1} DNL(r)$ it could seem that maximal error of INL(i) is $\Delta|-N/2-i+1|$. However, it should be noted that maximal error of DNL in (3) does not represent the systematic error, but the maximal value of random signal with rectangular probability of distribution and zero mean /4/. Therefore, the maximal error of measured DNL remains in the range of a few hundredths of LSB. This fact will be verified by simulation with MATLAB in the following section.

To measure vector $\overline{V}_2^{'}$ the following algorithm is to be implemented to µP.



At the beginning the variables are declared. Into variable **A** the full scale **FS** of DAC is saved and zero column matrix **V2**, **yp** are defined. The algorithm contains a global cycle with two embeded cycles. During the test cycle, whether output code **i** is at first generated by tested or additional ADC is tested. If, for example, the output code **i** is at first generated by additional ADC the output of DAC will be enlarged about *A/2* (at the beginning *A=FS*) and this value is saved into element **V2(i)**. Then, **i** is incremented about 1 and this procedure will repeat. Thus, from one saw-tooth impulse cycle vector $\overline{V}_2^{'}$ after 1st step of conversion will be obtained. Then, the variable **A** will be decreased in half and i will be set to -N/2+1. The whole procedure will repeat. The result will be vector $\overline{V}_2^{'}$ after 2nd step of conver-

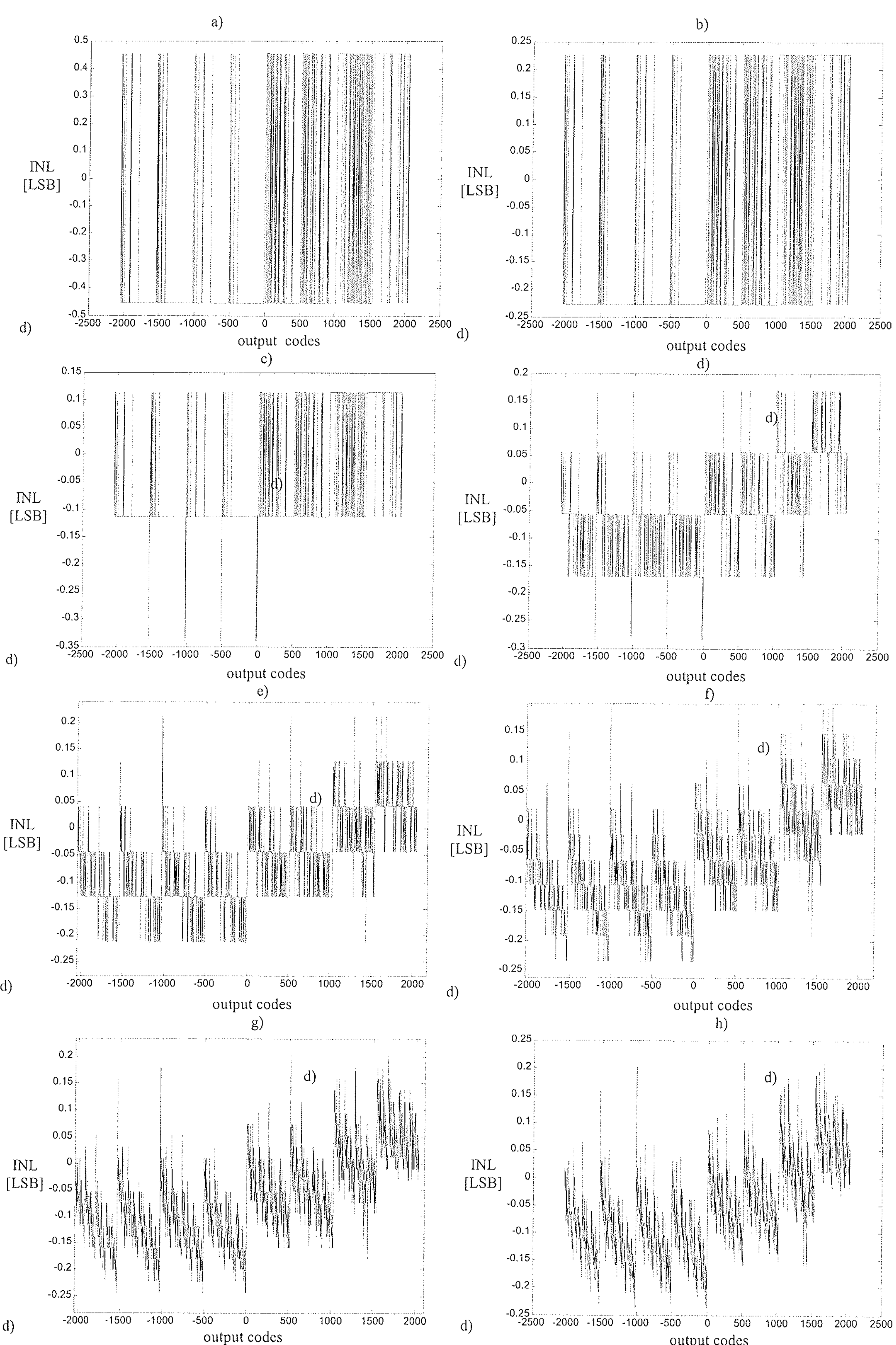
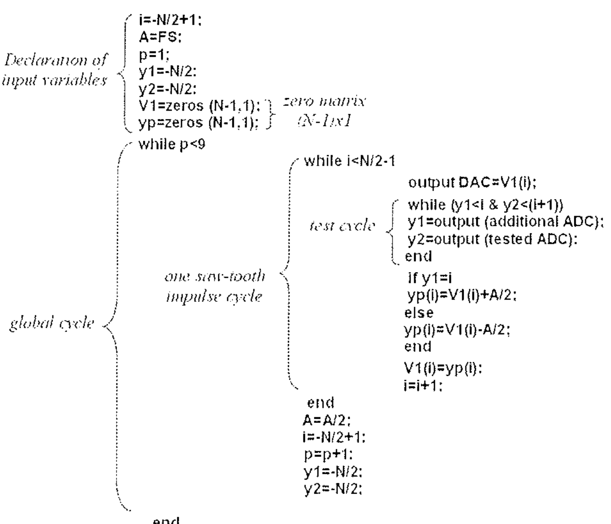


Figure 4. INL characteristic after: a)1st, b)2nd, c)3rd, d)4th, e)5th, f)6th, g)7th, h)8th step of conversion

sion. The number of steps of conversion depends on number of bits of DAC. In above algorithm the number of steps is 8 because 8 bit DAC is being used.

To measure vector $\vec{V_1}$ the following algorithm is to be implemented to μP.



```
Declaration of input variables:
  i=-N/2+1;
  A=FS;
  p=1;
  y1=-N/2;
  y2=-N/2;
  V1=zeros (N-1,1);   } zero matrix
  yp=zeros (N-1,1);   } (N-1)x1
global cycle:
while p<9
  one saw-tooth impulse cycle:
  while i<N/2-1
    output DAC=V1(i);
    test cycle:
    while (y1<i & y2<(i+1))
      y1=output (additional ADC);
      y2=output (tested ADC);
    end
    if y1=i
      yp(i)=V1(i)+A/2;
    else
      yp(i)=V1(i)-A/2;
    end
    V1(i)=yp(i);
    i=i+1;
  end
  A=A/2;
  i=-N/2+1;
  p=p+1;
  y1=-N/2;
  y2=-N/2;
end
```

As it can be seen, the only difference is in test cycle, where it is tested whether at first will be generated output code **i** by additional ADC or output code **(i+1)** by tested ADC.

The complete INL and DNL characteristic can be obtained by means of equations (5),(7).

Results of simulation

The test system according to Fig.2 was simulated in MATLAB. 12 bit ADC in PC-LAB-1200 was used as tested. Its transfer characteristic was obtained by using histogram-based test method /4/. For simplicity, 12 bit ADC with ideal transfer characteristic was used as additional. The parameters of saw-tooth impulse were as follows: k= 4.10^2 V.s^{-1}, V_{max}= 9 V and V_{min}= -9 V. The output voltage from DAC ranged from -8 to 8 V, the resistive divider ratio was 1/1000 and sampling period T_s of the system was 10^{-7} s.

INL characteristics calculated by means of (5) and (7) from vectors $\vec{V_1}$, $\vec{V_2}$ after given steps of conversion are shown in Fig.4. The resultant INL characteristic is shown in Fig.4h. The difference between this characteristic and that ideal (obtained by using histogram-based test) is shown in Fig.5. As it can be seen the maximal error is equal to −0.014 LSB.

Very interesting was to study the dependence of this error on precision of input saw-tooth impulse generator. The slope of the saw-tooth impulse was changed from 4.10^2 to 8.10^2 V.s^{-1} and results of simulation showed maximal error equal to −0.033 LSB. In spite of such extreme error of input saw-tooth impulse generator the error of measured INL remains in the range of a few hundredths of LSB.

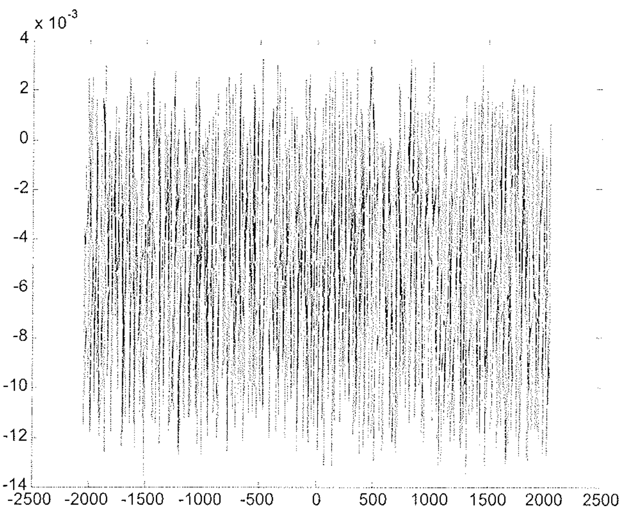


Figure 5. Absolute error of measured INL

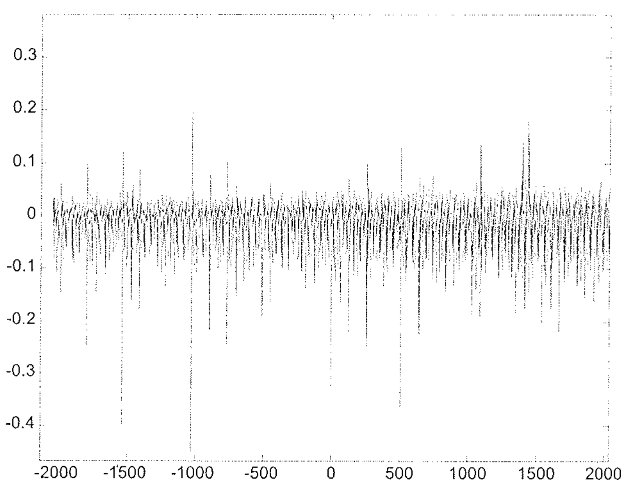


Figure 6. Resultant DNL characteristic of tested ADC

Other source of uncertainty that could be taken into account is the resistive divider. However, because, on the present the resistive dividers with relative error 0.01 % are standardly produced, this source of uncertainty can be omitted. Also as to DAC, if its maximal INL and DNL is a few LSB_{DAC} at the output of resistive divider it is error only a few hundredths of LSB using 8 bit DAC. By using DAC with higher number of bits the situation can be only better.

The resultant DNL characteristic calculated by means of (5) is shown in Fig.6 and corresponding absolute error is in Fig.7.

As to test time, because k= 4.10^2 V.s^{-1}, V_{max}= 9 V, V_{min}= -9 V, the sampling period is 10^{-7} s and measurement range of tested ADC is to be passed 8 times to measure voltage vector $\vec{V_1}$, and 8 times to measure vector $\vec{V_2}$ using 8 bit DAC, its value is 0.72 s.

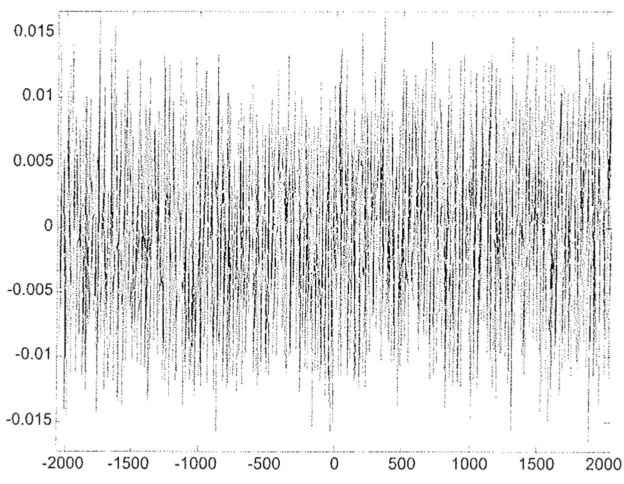


Figure 7. Absolute error of DNL

Conclusions

A new approach in testing ADCs has been presented. In comparison to ordinary approaches, decision levels of tested ADC are not measured to zero potential but to the decision levels of an additional ADC. Thus, there are not special requirements on precision of input signal generator. It has been shown that the precision of measured INL and DNL characteristic is in the range of a few hundredths of LSB. Very interesting is knowledge that the test system is immunized in face of input generator extreme errors.

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Acknowledgements

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SEED AND POLYNOMIAL SELECTION ALGORITHM FOR LFSR TEST PATTERN GENERATOR IN BUILT-IN SELF-TEST ENVIRONMENT

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Abstract: Testing integrated circuits is of crucial importance to ensure a high level of quality of product functionality. Testing a digital circuit involves applying an appropriate set of input patterns to the circuit and checking for the correct outputs. The conventional approach is to use an external tester (automatic test equipment - ATE) to perform the test. Built-in self test (BIST) techniques have been developed in which some or all test functions are incorporated on the chip. In today's integrated circuits, BIST is becoming increasingly important as designs become more complicated and the density of VLSI circuits increases. The BIST approach offers economic benefits, reuse of logic circuits as well as some significant opportunities in hierarchical testing. On the other hand, the classical testing approach and the use of automatic test equipment is becoming a less important part in the testing process. In this paper, we give an overview of BIST methods and present some advanced new BIST solutions for testing combinational circuits. We propose an algorithm for seeding the LFSR-based test pattern generators. We achieved nearly 100% test fault coverage for a given test lengths. Our method can be used for both test-per-scan and test-per-clock BISTs. The goal of the proposed method is to minimize the test lengths through suitable selection of initial seeds, to minimize hardware overhead and achieve sufficiently high fault coverage. While semi-random generated test cubes are additionally completed by deterministically calculated test vectors, the achieved fault coverage is very high. The experiments were made on ISCAS85 (ISCAS89) benchmark circuits /7/.

Algoritem za izbiro semena in polinoma generatorja testnih vzorcev LFSR za vgrajeno samotestiranje

Izvleček: Testiranje digitalnih vezij je bistvenega pomena, da bi zagotovili visoko stopnjo funkcijske zanesljivosti ter kakovosti proizvedenega vezja. Pri postopku testiranja na vhodne priključke vezja privedemo določen nabor testnih vektorjev in preverjamo pravilnost odzivov na izhodnih priključkih. Pri klasičnem načinu testiranja v ta namen uporabljamo testne naprave (ATE). Metode, pri katerih se del testiranja izvede znotraj samega vezja, se vedno bolj uporabljajo in prevzemajo pomembno vlogo pri testiranju sodobnih vezij. Današnje tehnologije omogočajo visoko gostoto vezij in dostopnost do testnih priključkov je vedno bolj otežena. Problem dostopa in zmanjšanja odvisnosti od uporabe dragih naprav ATE je mogoče rešiti z uporabo vgrajenih testnih metod BIST. Razen ekonomskih ima BIST še vrsto drugih prednosti, kot je pouporaba testnih modulov in možnost za izvedbo hierarhičnega testiranja. V članku predstavimo osnove vgrajenega testa BIST in nov pristop k testiranju kombinacijskih logičnih vezij. Podan je algoritem za ugotavljanje najprimernejšega semena in polinoma iz določene končne množice psevdonaključnih generatorjev za generiranje naključnih testnih vektorjev. Z izbranim naborom testnih vektorjev zagotovimo visoko stopnjo pokritja napak z minimalno potrebno testno dolžino. Metodo lahko uporabimo za dva načina izvedbe testa (TPC in TPS). Cilj predlagane metode je sistematično določanje primerne začetne vrednosti (semena), kot tudi vrste polinoma za psevdonaključni generator. Naključne generatorje izberemo tako, da bi jih lahko realizirali z najmanj dodatnimi elementi. Skrajšati želimo potrebni čas za samo izvedbo testa s predpostavko, da bi dosegli čim višje pokritje napak. Naključno dobljen nabor testnih vektorjev primerjamo z deterministično izračunanimi testnimi vektorji. Eksperimenti so prikazani na standardnem naboru primerljivih vezjih iz družine ISCAS85 (ISCAS89) /7/.

1. Introduction

Testing of integrated circuits is of crucial importance in ensuring a high level of quality in product functionality. The increasing complexity of VLSI systems makes testing a challenging task. Considering that testing represents a key cost factor in the production process (a proportion of up to 70% of total product cost), an optimal test strategy can offer a substantial competitive advantage in the market of the semiconductor and electronics industry /27/. Testing effects areas of manufacturing as well as engineering and design. The time and cost are the two main considerations in IC design and production process /17/.

As the density of VLSI circuits increased, it became attractive to integrate dedicated test logic on a chip /2/. Built-in self-test (BIST) techniques enable an integrated circuit (board, system) to test itself. BIST techniques offer a great economic benefit compared to the traditional testing. When testing is built into the hardware, it has ability of being not only fast and efficient but also reusable /18/. Furthermore, BIST offers the capability for hierarchical testing where BIST circuit perform test on chips, boards, and the entire system without external, expensive automatic test equipment /20/. Another important consideration is that BIST allows an IC to be tested at its normal operating speed /2/. Figure 1 illustrates the testing process with classical and basic BIST approach. The basic BIST architecture requires the addition of three hardware blocks to the circuit under test (CUT): a pattern generator, a response analyzer, and a test controller /1/.

For simpler applications the deterministic test patterns are stored in an on-chip ROM instead of using a pattern generator. Since this method requires high storage overhead it leads into a non-practical solution /4/. Instead of pre-

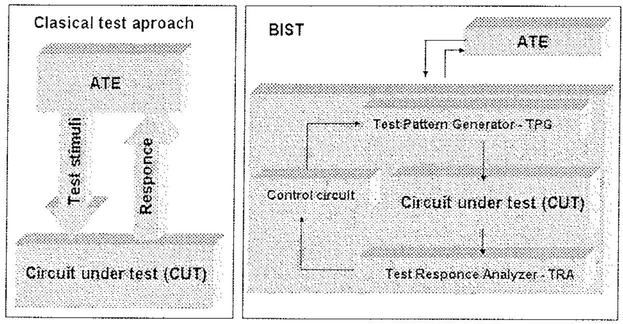


Figure 1: Classical and BIST testing scheme.

calculated test vectors a linear feedback shift registers (LFSR) is generally preferred for pattern generation /1/, /2/,/13/. It is able to generate a pseudo-random test patterns with low hardware overhead (easy and cheap to generate).

However, several circuits contain random pattern resistant (r.p.r.) faults which limit the performance of BIST /19/. For background, the r.p.r. faults are faults with low detectability, and therefore require a very long testing time to achieve the appropriate test coverage. While r.p.r. faults are known to be implicated in insufficient fault coverage levels, the selection of the appropriate pseudo-random test pattern generator has been extensively investigated for enhancing fault coverage levels /31/,/22/. A pure pseudo-random test could be very long, hence too expensive in terms of time, to obtain the highest possible fault coverage. Moreover, it is not always guaranteed that the highest possible fault coverage will be achieved even with extremely long pseudo-random test pattern sequence.

A variety of solutions have been suggested to solve this problem /2/. A common method is to modify the circuit by test point insertion (control, observation point), or to redesign it to make it testable via random patterns /25/. Modifying the CUT is rarely a desirable option because of performance degradation and for intellectual property reasons /18/. Another technique is to test with weighted pseudo-random sequences, where the random patterns are biased using additional logic to increase the probability of detecting the r.p.r. faults /13/.

Another widely investigated approach in BIST is the so called mixed-mode testing method /11/. In this BIST technique the circuit is tested in two phases. In the first phase, pseudo-random patterns are applied to cover easy to detect faults /11/. In the second phase, deterministic test patterns are applied to cover the remaining faults. The mixed-mode BIST can be performed in several variations. One is to apply the deterministic patterns from a tester while another way is to store the deterministic patterns in an on-chip ROM. Storing, however, requires a large amount of hardware overhead. As an alternative with lower memory requirements seeds can be stored on the external tester.

Next significant innovation in mixed-mode testing came with the introduction of mapping logic /22/. The idea is to identify patterns in the original generated set that don't detect any new faults and map them by hardware into deterministic patterns.

The other mixed-mode approach is presented as "bit-fixing" method /24/. The deterministic test cubes are embedded in the pseudo-random sequence of bits /8/. Logic is added at the serial output of the LFSR to alter the pseudo-random bit sequence, so that it contains deterministic patterns that detect the r.p.r. faults. This is accomplished by "fixing" certain bits in the pseudo-random test sequence. The method provides 100% fault coverage, but with high hardware overhead.

Wunderlich et.al proposed another mixed-mode technique called the "bit-flipping method" /29/. To avoid storing the deterministic patterns on the chip, the authors show that it is sufficient to alter just a few bits of the general pseudo-random sequence. The efficiency of this scheme relies on the fact that relatively small amounts of the generated pseudo-random patterns are useful for fault detection while others are candidates for altering. Moreover, as a deterministic test pattern usually contains many unspecified bits, there is a very high possibility that one of the ineffective patterns can be modified at just a few bit positions so that it becomes compatible with a previously computed deterministic pattern. Results are provided to show that this scheme represents the most area-efficient solution to-date /29/.

Another possible way to enhance low detectability of the r.p.r. faults is to select the seed very carefully. Several procedures to select seeds have already been studied /5/,/6/,/10/,/14/,/16/. Bayraktaroglu et al. examined the pseudo-random pattern generator structure and selection approaches /5/,/6/. Lempel et al. proposed an LFSR seed-selecting algorithm that used the theory of discrete logarithms /16/. In Fagot et al.'s study /10/, fault simulation computes an efficient LFSR seed which outputs the test sequence including a test cube. To reduce test application time, Ichino et al. used a reseeding method and reverse order simulation /16/.

In this paper we propose a BIST technique that selects the type of LFSR test pattern generator (TPG) and appropriate seed (initial state) to improve random-pattern test quality. The idea is to find a minimal possible set(s) of pseudo-random generated tests to achieve the highest possible test coverage within specified time constraints. An additional effort was invested to embed the test and keep the hardware overhead as low as possible. We consider that the size of the LFSR, its primitive feedback polynomial, and the length of generated test are a priori known. The proposed method is intended to produce a one-seed test sequence of a given length that achieves the highest possible stuck-at fault coverage. The main feature of this technique is a minimal requirement for the additional hardware to cover as many r.p.r. faults as possible. The goal of the presented method is an efficient test pattern generator which guarantees nearly 100% test fault coverage. Furthermore, the proposed technique minimizes the test ap-

plication time, test generation time, and hardware requirements. For most tested circuits we reached a reasonable fault coverage. When these techniques are applied to a mixed-mode BIST such as reseeding, bit-flipping or bit-fixing, the number of additional circuits is generally reduced. With a minor modification of the proposed software the seed-selection methods can be applied not only to typical LFSRs but also to other types of test pattern generators such as Cellular Automata. /29/.

The paper is organized as follows. In next section, we describe the construction methods of LFSR test pattern generator. Two basic BIST techniques are then described. In section 3, we briefly present some necessary definitions. In section 4, we introduce the proposed method for generating an efficient one-seed LFSR test sequences. Experiments performed on ISCAS 85 benchmark circuits are presented and discussed in section 5. Concluding remarks are given in section 6.

2. Test pattern generator implementations

The main disadvantage of the classical testing approach is that the purchase price of test equipment (ATE) is very high /31/. For built-in self testing one must be able to generate and apply test patterns internally. By applying BIST, we can eliminate the need for ATE /1/,/2/,/13/. Figure 2 illustrates a basic BIST implementation. The method relies on embedding some extra elements to the circuits like test pattern generator and test response analyzer. In this paper we will primarily focus on the problem of built-in generation of test patterns.

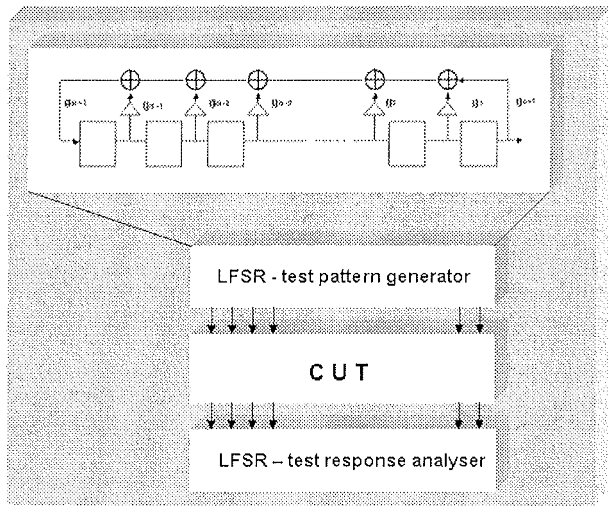


Figure 2: *Basic BIST implementation to CUT.*

The test sets can be stored in chip ROM but in the case of larger circuits this is an impractical and costly solution. LFSRs are commonly used as test pattern generators that generate pseudo-random patterns. These circuits are autonomous in the sense that they have no inputs except for clocks. Each cell is assumed to be a clocked D flip-flop. The LSFRs are cyclic as they go through a fixed sequence of states. The output sequences (patterns) generated by such circuits are also cyclic. The patterns could be also encoded into seeds by solving a linear system of equations, which is an algebraic representation of the linear expansion of the LFSR /15/.

The behaviour of a linear feedback register is completely determined by the feedback coefficients $g_0, g_1, .., g_m$ where g_i is a binary constant, and $g_i = 1$ implies that a connection exists, while $g_i = 0$ implies that there is no connection. A sequence of numbers $g_0, g_1, .., g_m$ can be associated with a polynomial called the generator function G(x), defined in equation (1).

$$G(x) = g_0 + g_1 x^1 + g_2 x^2 + ... + x^m \quad (1)$$

Since the feedback coefficients determine the polynomial of this LFSR, they need to be set to certain combinations to realize a specific desired polynomial. The LFSR goes through a cyclic i.e. periodic sequence of states and the output sequence is also periodic. The maximum length of this period is 2^m-1, where m is the number of stages. The characteristic polynomial associated with a maximum length sequence is called a primitive polynomial. If the feedback polynomial is primitive then the output sequence has the same random properties and is called pseudo-random. In many cases pseudo-random patterns perform well for testing but may also lead to reduced fault coverage due to linear dependencies /1/.

There are two established realizations of characteristic polynomials in Figure 3. The Fibonacci implementation consists of a simple shift register in which a binary-weighted modulo-2 sum of the taps is fed back to the input. On the other hand, the Galois implementation consists of a shift register the contents of which are modified at every stage by a binary-weighted value of the output stage. The choice of LFSR generators, configuration of feedback taps and applied seeds (initial values) can make an enormous difference in the efficiency of testing and in achieving the required test coverage for a particular CUT. When implemented in hardware, modulo-2 additions are performed with XOR gates. The Galois form is generally faster than the Fibonacci one due to the reduced number of gates in the feedback loop, thus making it the favoured form /13/.

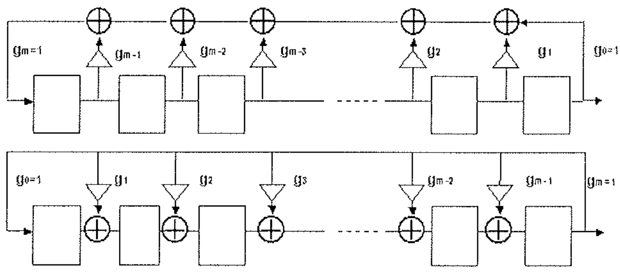


Figure 3: *Fibonacci and Galois implementation of LSFR.*

Figure 4 illustrates pseudo-random patterns generated with Fibonacci and Galois type of polynomial. For experimental purposes we implemented both types of generators in the software. The example shows an LFSR of size m = 4 with feedback connections at g_4 and g_3. The feedback taps are specified as lfsr "/4,3/g" for the Galois form, and lfsr "/4,3/f" for the Fibonacci form. The left side of Figure 4 shows the output sequence behavior of the Fibonacci implementation with a primitive Fibonacci field. The non primitive cyclic form in our example are obtained when the feedback taps of the polynomial are specified as lfsr "/4,2,1/f" for the Fibonacci or lfsr "/4,2,1/g" Galois form.

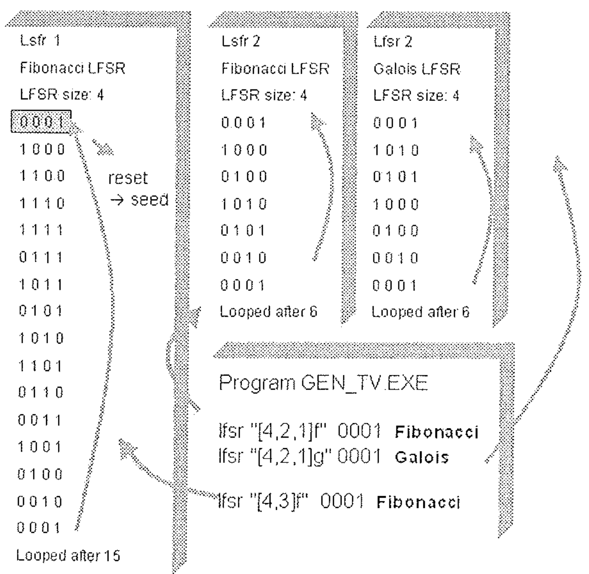
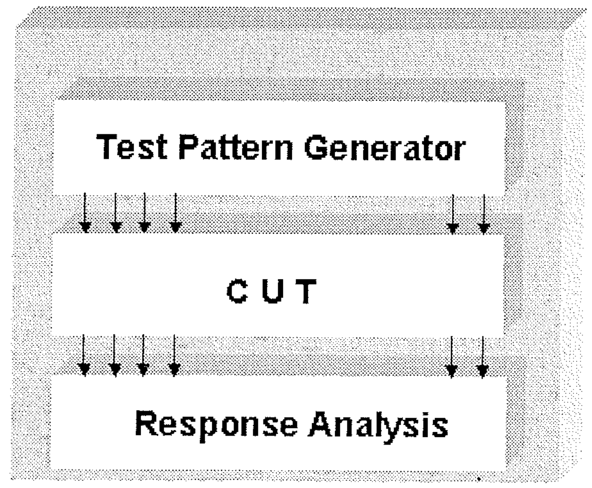


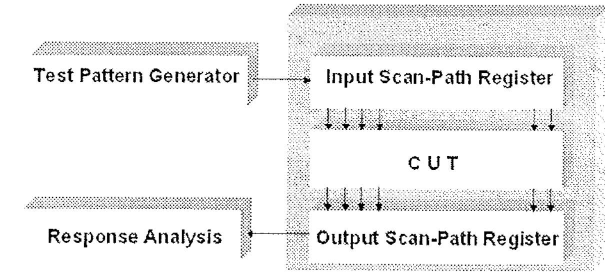
Figure 4: *Examples of primitive and non primitive sequence generation.*

BIST techniques, as shown in Figure 5, are classified into two categories: test-per-clock and test-per-scan /2/. In the test-per-clock BIST (Figure 5(a)), a test vector is applied and its response is captured every clock cycle. In the test-per-scan BIST (Figure 5(b)) a test vector is applied and its response is captured into the scan chains only after the test is scanned into the scan chains. A scan cycle is defined as the number of clock cycles required to shift the vector into a serial register of the serial scan paths (whichever is larger) plus one or more normal mode clocks. The test-per-scan approach is generally much slower than the test-per-clock approach. The two approaches involve distinct hardware structures and trade-offs.

We propose an algorithm for selecting a seed that can achieve target fault coverage with minimum test length for a given set of polynomials. Additionally, we propose an algorithm for seed selection that can achieve maximum fault coverage for a given test length and for a given set of polynomials. In other words, the number of undetected faults is reduced to a minimum. The proposed algorithm considerably improves pseudo-random testing without the need to change circuits in the CUT.



(a) Test-per-clock



(b)Test-per-scan

Figure 5: *Basic BIST techniques*

3. Preliminary details and definitions

We define the notation where F is the set of modeled faults in the CUT. In this paper we consider single stuck-at faults. Let |F| represent the number of elements in a set. Then a fault coverage of C % by a test pattern sequence means that |F| x C /100 faults are detected by this sequence. F_T denotes the set of faults that are detected by test pattern T.

Let T be an input test pattern generated from an m-stage LFSR, where m is the number of primary inputs to the CUT. When the LFSR outputs T_0 as the first test vector, then the sequence of outputs proceeds as follows: T_0, T_1, T_2, ..., T_{m-1}, T_0... Similarly, for seed T_1 the LFSR output sequence is: T_2, T_3, ..., T_{m-1}, T_0, T_1, T_2... In general, when the seed is T_i, the *j-th* test pattern is T_{i+j} (mod m).

To model the required test length we define a function $L(T_i, N_g)$ where N_g is a total number of faults detected for a selected seed T_i. N_g denotes the target number of detected faults, and $N_g \leq |F|$. Function $L(T_i, N_g)$ can be estimated or computed by fault simulations. For a given CUT there is at least one seed that detects N_g faults with a minimum test length. We search for this as the minimum test length seed $T_{i\,min}$. It is always possible to find at least one such seed.

4. The proposed approach

When performing pseudo-random testing using an LFSRs as test pattern generators, the fault coverage that can be obtained is limited by the presence of random resistant faults in the CUT. To evaluate the detection hardness of these faults, we need to use a measure that represents the difficulty level for a random pattern to detect a given fault. Computing the fault detection probability is a hard problem. Generally, the higher the number of patterns detecting a given fault, the easier this fault is detected. In our method, we measure the quality of the generated test after each test vector is applied to the CUT.

A pattern generator based on an LFSR generates a test pattern sequence after a seed has been set. We first applied the method to the test-per-clock BIST structure, where the CUT is a combinational circuit. Once an LFSR seed is selected, the succeeding output test sequence is uniquely determined. A binary vector from the *m*-stage LFSR is regarded as an element T_i ($0<i<2^m-1$) from Galois Field (GF) (2^m), where T is a primitive element from GF (2^m) and i denotes the index.

Figure 6 shows a three pillar example of the seed selection procedure. First we select one of LFSR generators with a starting seed T_i. We first consider that the length L of the generated test sequences is set. Then we start to generate a fixed number of pseudo-random test vectors. With a fault simulator /21/ we measure the success of generated test vectors after each new generated and applied test vector. The first pillar represents the result for test set with seed T_i. The bright frames in the pillar contain the *useful test vectors*. Those cover one or more faults in the CUT. The dark frames contain *unuseful* ones (no new faults were found by a specific test vector). By comparing those three pillars, we suppose a seed that generates a test cube that covers more faults then any other. Unfortunately, it is not only the number of successful test vectors in a cube that is important, but also how many faults are covered by them. Figure 7 describes this situation, where the cubes were rearranged by a fault coverage C (%). The seed T_{i+n} is the most successful selection with the highest achieved fault coverage. However, the generated test vectors for seed T_{i+m} contains more *useful* test vectors, but test vectors for seed T_{i+n} in a set are more effective.

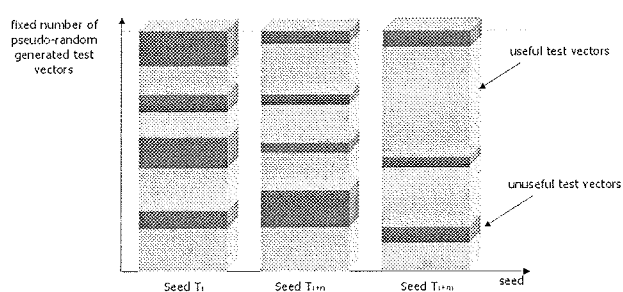


Figure 6: *Fixed generated number of test sets with different seeds.*

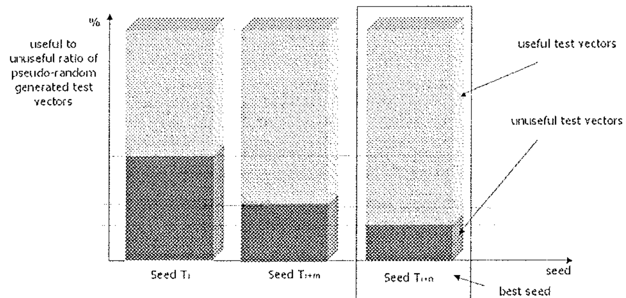


Figure 7: *Ordered pillars by effectiveness.*

Next, we assume that the test-per-clock BIST has been used in the C17 circuit, which is one of the ICSAS'85 benchmark circuits. This circuit has five primary inputs and two outputs. An example of the best seed calculation procedure is given in figure 8. For a given polynomial

Name of the circuit	c17							
Number of primary inputs	5							
Number of primary outputs	2							
Number of gates	6							
Level of the circuit	3							
Polinomial	Seed	Test patte	Fault cove	Collapsed	Detected f	Undetecte	Memory	CPU
[5,1]	10000	17	100.000	22	22	0	168112	0.000
[5,1]	01000	16	100.000	22	22	0	168112	0.010
[5,1]	00100	15	100.000	22	22	0	168116	0.010
[5,1]	00010	14	100.000	22	22	0	168116	0.016
[5,1]	10001	13	100.000	22	22	0	168116	0.000
[5,1]	11000	12	100.000	22	22	0	168116	0.000
[5,1]	01100	11	100.000	22	22	0	168120	0.001
[5,1]	00110	10	100.000	22	22	0	168120	0.010

Figure 8: *The best seed calculation procedure for minimal required number of test patterns according to complete fault coverage of C17 with polynomial /5,1/.*

$P(X)=x^5+x+1$ and the starting seed T_0 (10000) the fault simulation returns 100% fault coverage of C17 after 17 generated test vectors. If we calculate the required test length to achieve the target coverage (in our case 100%), we next increment the starting seed by one and a function $L(T_i, N_g)$ returns 16 test vectors for all 22 faults. Starting with a seed 00110, we achieve the same (100%) fault coverage with shorter test length of only L=10 pseudo-random generated test vectors, which is the minimum function for the proposed polynomial and the seed $T_{i\ min}$ is 00100.

Figure 9 shows the differences in fault coverage when we implement different polynomials. We found that the implementation of specific polynomial as pseudo-random pattern generator can be very successful for some circuits while another type of polynomial returns weak results. Therefore, it is important to try more than one polynomial.

For a large circuit a seed calculation through a complete space of all possible test vectors is an NP-hard problem, therefore we have to be satisfied with approximations. It is important for the first step to make a realistic estimation of realistic test length. In the second step we can then begin with the estimation of the shortest test length $L_{min}(Ti, Ng)$. Figure 10 shows an example where the fault coverage of L=100 pseudo-random generated tests were simulated. For a given seed T_j the possible fault coverage (FC) of 88% after applied 58 pseudo-random generated test vectors was achieved. The rest (number) of test vectors are only unusable ones in window of 100 pseudo-random test vectors (PRTV). The great benefit of our technique is the possibility for exact calculation of the lower bound of those testing windows which are able to reach the target fault coverage for a specific circuit.

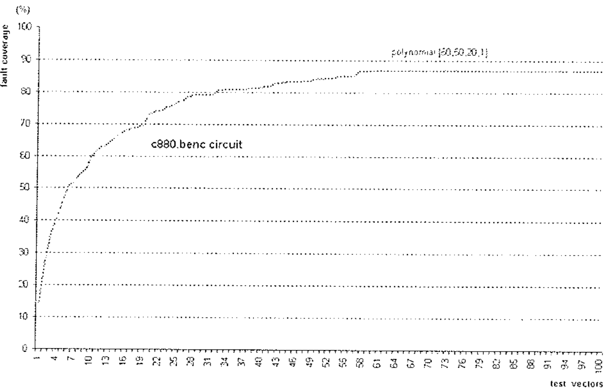


Figure 10: Coverage/number of generated test vector ratio for c880.bench

5. Experimental results

The method to reduce the pseudo-random test length described in this paper was applied to ISCAS 85 benchmark circuits. We considered the test-per-clock BIST structure. The size of each LFSR is equal to the number of primary inputs in each circuit. The characteristic polynomial of each LFSR is a primitive feedback polynomial. Fault simulation in each circuit was performed using FSIM simulation tool

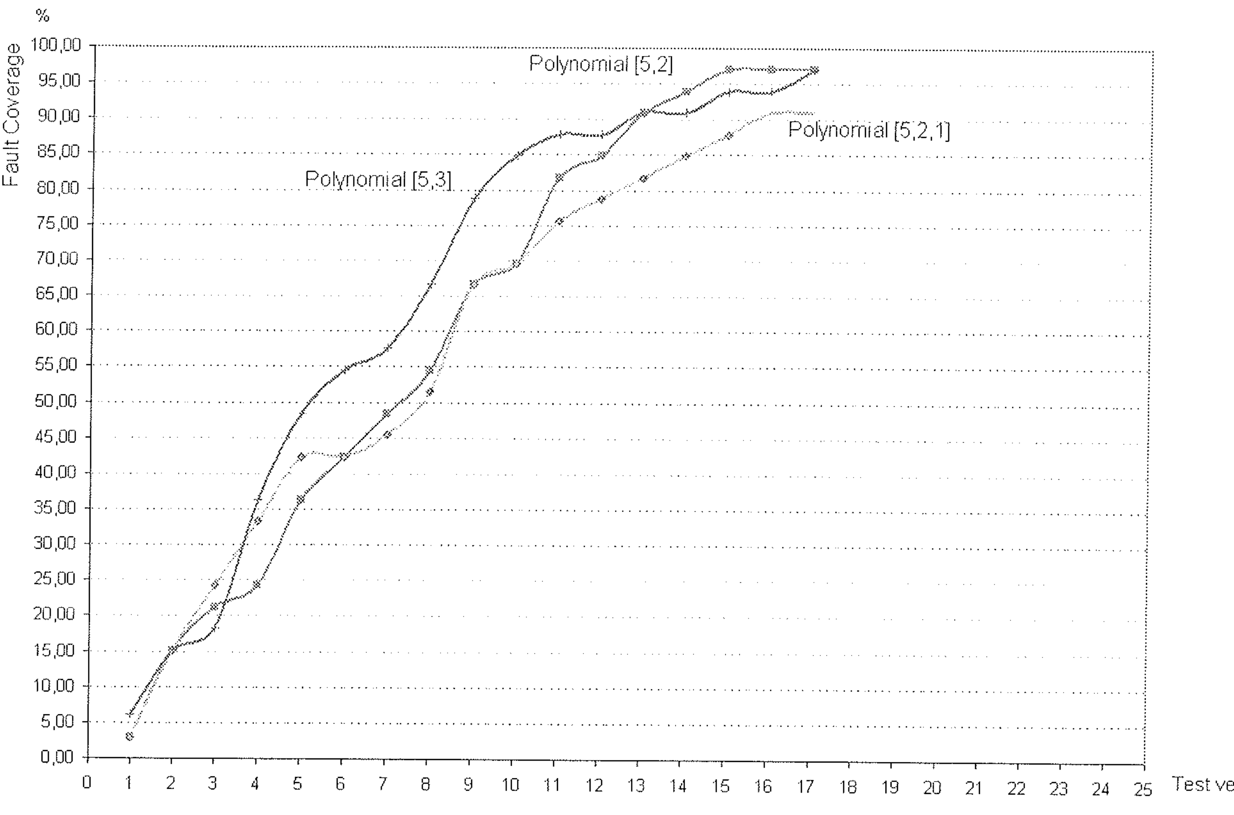


Figure 9: Polynomial discrepancy

/21/. The computer we used is PC based platform with 1 GHz Pentium Processor.

First, we select a seed that could achieve the minimum test length to cover the highest possible number of detectable faults in a particular benchmark circuit. Next, we search for suitable polynomial for a circuit. First polynomial in the database is a polynomial with the lowest possible number of feedbacks. Then we progressively increase the number of feedbacks for each additional polynomial in the base. The number of selected polynomials differs and depends on the size and complexity of a circuit. For example, we used 20 different polynomials for C880 circuit and only three polynomials for C7552 circuit. In the next step we randomly select the first seed and determine the fixed test length TSL for each test sequence. Further on, we determine the distance to the next seed and the total number of generated test sequences for each individual polynomial in database. The number of selected seeds, i.e. the number of test sequences, depends on the number of inputs in the tested circuit and ranges between a few hundred and few thousand for each polynomial. With the simulator, we calculate the achieved fault coverage for each generated test sequence, for each polynomial and seed. Next step is a determination of the average (AVR_FC %) and maximum fault coverage (M_FC %) for the specific test set. The results give us the information, which polynomial, seed and test length are the most suitable for a tested circuit.

The results are given in Table 1. The first column indicates the circuit name. The second and the third column give the number of primary inputs (# PI) and primary outputs (# PO), respectively. The fourth column gives the number of detectable faults (# F) in a circuit. The fifth column reports the chosen length of the generated test sequences (TSL). Columns six and seven give the average fault coverage (AVR_FC in %) and maximum achieved fault coverage (M_FC in %) according to the selected test length. The CPU time (in seconds) needed for the complete process of generating a one-seed LFSR test sequence is in the last column. For each circuit, an average of 15 different primitive feedback polynomials were evaluated. The results in table 1 show the performances obtained with the proposed method to compute the most successful LFSR seed and the best polynomial. By comparing our results to previously published results /23/,/10/, we conclude that for most tested circuits our results were comparable or even better. Computational effort is much more difficult to compare because of different equipment used in former reports.

In the second step of the algorithm, the goal was to find the shortest test sequence according to selected polynomial and starting seed. We used the outcome of first step of the algorithm, i.e. the best suited polynomial and the best seed. The seed is then used as initial seed in the second step of procedure. For each new generated test vector a fault coverage is computed by the fault simulator.

Table 1: Test results according to selected test lengths for ISCAS 85 circuits

Circuit	# PI	# PO	# F	TSL (10^3)	AVR_FC (%)	M_FC (%)	CPU (s)
c432	36	7	524	5	98,696	99,237	322,69
				10	98,993	99,237	5398,50
				50	99,135	99,237	29073,51
c499	41	32	758	1	98,697	98,945	519,56
				5	98,725	98,945	12702,11
				100	98,945	98,945	19800,47
C880	60	26	942	1	94,286	99,894	529,02
				5	99,5	100	1022,55
				10	99,753	100	1495,23
C1355	41	32	1574	1	96,215	99,238	1180,11
				5	97,343	99,942	3100,21
C1908	33	25	1879	1	95,268	97,765	141624,00
				10	99,487	99,521	384374,12
				50	99,519	99,521	15500,98
C2670	233	140	2747	5	84,526	88,278	191052,19
				10	84,748	90,462	358931,22
C3540	50	22	3428	1	94,278	95,362	7906,16
				5	95,829	96,004	13000,01
C5315	178	123	5350	5	69,907	98,897	6 h
				10	98,897	98,897	4008
C6288	32	32	7744	500	99,561	99,561	1008,09
				1	99,561	99,561	1579,15
C7552	207	108	7550	10	94,188	96,768	7 h
				50	96,467	96,927	13 h

Table 2: Average test results according to selected test lengths for ISCAS 85

Circuit	# PI	# PO	# F	# AVR_TL	AVR_FC (%)	MIN_TS	M_FC (%)
C17	5	2	22	11	100,00	5	100
C432	36	7	524	611	98,413	353	99,24
C499	41	32	758	793	98,820	512	98,95
C880	60	26	942	14353	98,272	1024	100,00
C1355	41	32	1574	2060	97,059	1760	99,49
C1908	33	25	1879	3502	99,071	3296	99,31
C2670	233	140	2747	> 100000	92,111	99999	95,413
C3540	50	22	3428	9949	95,920	4160	96,004
C5315	178	123	5350	512	98,061	483	98,897
C6288	32	32	7744	62	99,330	64	99,561
C7552	207	108	7550	> 100000	96,026	14432	97,007

When the desired fault coverage is achieved, the procedure ends and the last generated test vector determines the intermediate achieved test length. For each polynomial, we randomly select 1.000, 5.000, 10.000 and 100.000 test sets on average. Then, we calculate minimal test length (MIN_TS) for the highest fault coverage (FC %), average test length (# AVR_TL) and average fault coverage (AVR_FC). We found out that the majority of tested circuits the average and minimal number of test vectors are very close. For some circuit, i.e. C880, we calculate the minimal test length of 1024 generated test vectors to achieve 100% of fault coverage. To achieve the average of 98,272 % fault coverage we need 14.353 test vectors in average.

In Table 2, we compare the fault coverage provided by our method and the best fault coverage of random selected seed test sequence. The first column has the circuit name. The second and the third columns give the number of primary inputs (# PI) and the number of primary outputs (# PO). The fourth column gives the number of detectable faults (# F) in each circuit. Columns five and six give the average test length (# AVR_TL) and the average achieved fault coverage (AVR_FC in %) according to the selected set of seeds. In column seven we report the shortest achieved test length. The highest possible fault coverage achieved according to minimal test length is in the last column.

6. Conclusion

In this paper, we proposed a technique for selecting the LFSR TPG seed in order to achieve the highest fault coverage with a given set of characteristic polynomials. In our research we can conclude that different characteristic polynomials can return a different best possible seed to reach the expected fault coverage. The test length (total number of generated pseudo-random test patterns) differs more than 1 against 10 for some circuits being tested. To compute the best seed for the largest circuits in the test (C7552) we need 13 h of computational time. Note that for large circuits the applicability of the method depends on two user constraints. The first one is the computational effort one is willing to spend. The second one is the test length of the test sequence one is willing to allow. Comparing to the results of other authors we can conclude that our technique is fast enough to deal with combinational circuits of great size and with a large number of primary inputs. Furthermore, the proposed seed/polynomial selection can be applied not only as conventional BIST but also in mixed mode BIST such as those with reseeding, mapping, and bit-fixing.

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DESIGN AND ANALYSIS OF THE ON CHIP INTEGRATED DATA INTERFACES FOR ASIC ADOPTING I^{2}C AND SPI PROTOCOL

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Key words: I^{2}C, SPI, ASIC, Serial synchronous data transmission, eeprom AT24CXX.

Abstract: Application specific integrated circuit design usually requires several input bits for trimming, for changing operating parameters or simply for storing information - such as a product version or a serial number. While reducing the size of the chip, we can not afford to waste silicon for several input pads. Therefore, to satisfy the compatibility issues, we normally have to use, or suitably adopt one of the available serial busses. They vary in protocol types, speed, reliability, complexity and number of wires required. In this article we will briefly introduce some of the most popular serial interfaces. Afterward we will focus on the SPI (Serial Peripheral Interface) and I^{2}C (Inter Integrated Circuit bus) serial protocols. For that purpose we will give some details about two different application specific integrated circuits that we recently designed for serial production. These two circuits have very similar input and output requirements, but they use different interface protocols. Complexity details and space requirements for the mentioned interfaces will be analyzed.

Načrtovanje in analiza podatkovnega vmesnika na integriranih vezjih po naročilu z uporabo I^{2}C in SPI standardov

Kjučne besede: I^{2}C, SPI, Integrirana vezja po naročilu, zaporedna sinhrona komunikacija, eeprom AT24CXX.

Izvleček: Načrtovanje integriranih vezij po naročilu je vse pogosteje povezano z zagotavljanjem možnosti sprotnega vplivanja na delovanje integriranega vezja in tudi možnostjo shranjevanja informacij v integriranem vezju - na primer verzija izdelka ali serijska številka. V ta namen je najbolj ekonomična uporaba zaporednega komunikacijskega vodila, saj zahteva malo vhodnih priključkov na integriranem vezju. Zaradi združljivosti z drugimi napravami, je priporočljivo uporabiti ali prilagoditi katerega izmed znanih serijskih vodil. Seveda pa se slednji med sabo zelo razlikujejo glede načina komunikacije, hitrosti, zanesljivosti, zapletenosti in številu povezav, ki jih potrebujemo za njihovo uporabo. V tem članku bomo na kratko predstavili nekaj najbolj popularnih serijskih protokolov. Bolj natančno pa si bomo ogledali SPI (Serial Peripheral Interface) in I^{2}C (Inter Integrated Circuit bus) načina povezav in to na primeru dveh integriranih vezij po naročilu. Vezji smo nedavno razvili za serijsko proizvodnjo in imata zelo podobne vhodno izhodne komunikacijske zahteve. Za izvedbo smo uporabili dva različna komunikacijske protokola. Primerjali bomo prostorsko zahtevnost in zapletenost izdelave komunikacijskih vmesnikov.

1. Introduction

Modern ASIC (Application Specific Integrated Circuit) design usually requires input capability of several information bits. This is necessary to achieve optimal operation or for storing desired information. Since the silicon chip should be as small as possible, we can not afford to use several pads for parallel communication. As the efficiency of the serial busses increases, the speed advantage of the parallel data transmission gets less important. Consequently, a serial transmission is perfectly suited to decrease the number of space consuming pads on the integrated circuit. The basic principle is that command codes and as well as data values are serially transferred to the integrated circuit. After that they are pumped into a shift register, where they can be available for internal parallel processing.

At the present time we have several serial communication standards available /1/. The most popular are USB (Universal Serial Bus), IEEE1394, SPI (Serial Peripheral Interface), I^{2}C (Inter Integrated Circuit bus), UART (Universal Asynchronous Receiver Transmitter) and CAN (Controller Area Network). Figure one presents an application overview of the mentioned serial protocols. Let us shortly present the most important features:

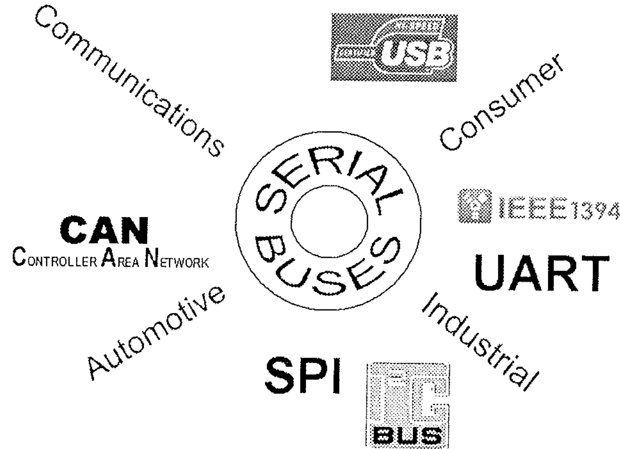


Figure 1: Overview of the most popular serial data busses.

- USB is still emerging standard, developed by Intel and Microsoft for connecting personal computers to peripherals. It uses four wires; two of them are power supply.
- UART is mainly used for asynchronous communications in computer world for speeds up to 1Mbits/s. Parity bit can be added for increased reliability. One wire for each direction of flow.
- CAN is one wire (differential) bus, developed by BOSCH and CIA for industry demanding environments, where high reliability is requested.
- IEEE 1394 is also still emerging standard - trademark of Apple. It uses four or six wires. Mostly used in computer or video applications where constant transfer rates with guaranteed bandwidth is required.
- SPI was developed for connecting peripherals to each other and to microprocessor. It is a four wire full duplex synchronous serial data link. Has no official specification.
- I^2C developed by Philips for communication between integrated circuits on printed circuits boards. Two bus lines are required.

In this article we will take a closer look to the SPI and I^2C serial bus. We recently designed and transferred into the production two different ASICs, with similar input and output requirements, but different interfacing protocols. One was SPI and the other was I^2C.

The SPI-bus is a four-wire (actually three-wire plus slave selects wires plus ground) synchronous serial communications interface, used by many microprocessor peripheral chips. It is standard across many Motorola microprocessors and other peripheral chips. It provides support for a low/medium bandwidth network connection amongst CPUs and other devices supporting the SPI. A synchronous clock shifts serial data in and out of the bus controller in blocks of 8 bits. SPI bus is a master-slave interface. Whenever two devices communicate, one is referred to as the "master" and the other as the "slave" device. The master drives the serial clock. When using SPI, data is simultaneously transmitted and received, making it a full-duplexed protocol. Motorola's names for the four signals are as follows: SCLK for serial clock, which is always driven by the master, MISO is master-in slave-out data, MOSI is master-out slave-in data and CS (chip-select) input is required to enable the slave. Every slave connected to bus needs separate chip-select signal line. There are also the extensions to SPI protocol such as for example QSPI (Queued Serial Peripheral interface) and MicrowirePLUS.

I^2C is a two-wire (plus ground) synchronous full duplexed serial interface standard defined by Philips Semiconductor in the early 1980's. The two active wires, SDA and SCL, are both bidirectional. Where SDA is the Serial Data line and SCL is the Serial Clock line. The interface typically runs at a fairly low speed (100 kHz to 400 kHz) form 1998 specifications also up to 3.2 mega baud. Each device on the bus has a unique address. A device that controls signal transfers on the line and also controls the clock frequency is the master. Device that is controlled by the master is slave. The master can transmit or receive signals to or from the slave, or control signal transfers between the two slaves. Bus supports more than one master on a single bus. To begin the communication, the master places the address of the slave, with which it intends to communicate, on the bus. All devices monitor the bus, to determine if the master device is sending their address. Only the device with the proper address communicates with the master. I^2C has also the acknowledgement mechanism to confirm data reception.

In next paragraph we will shortly describe our approach to the implementation of the SPI and I^2C bus, including some technical background for better understanding the complexity and the differences between the mentioned communication protocols. Later we will show our interface design approach and some area analyses of the implemented methods.

2. Implementation of the SPI interface on the ASIC1

Requests for the ASIC1 interface was to adopt SPI interface for writing, storing and reading eighty bits of information. This information is necessary for trimming DAC (Digital to Analog Converters) and for integrated circuit setup. Interface clock frequency should be up to 1MHz. Eighty bits are organized within ten differently addressed bytes. Since the purpose of previously mentioned bits is to fine trim the operation of the ASIC, these ten bytes of information should be available in parallel. The reason for this is to avoid erratic operation of the chip while trimming. In other words, by using a simple shift register particular fine trimming function would be set up to several undesired positions before the final shift. Therefore we actually need more registers and appropriate logic to perform the desired serial to parallel operations. Figure 2 presents block diagram of the ASIC 1 interface.

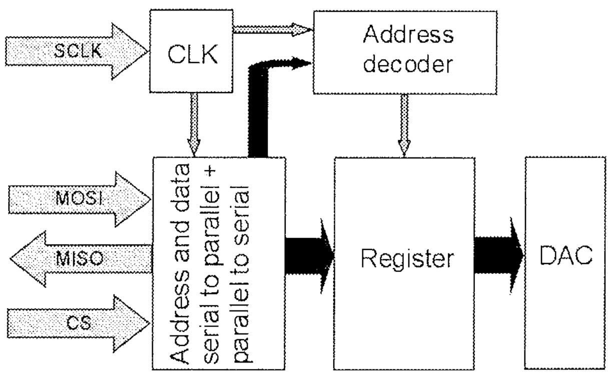


Figure 2: SPI interface block diagram for ASIC 1.

There is no official specification what exactly is SPI interface and what not, so there are no general rules for transitions where data should be latched. In practice there are used four different modes. Figure 3 presents an example of the SPI-mode 0 communication protocol where CPOL (Clock polarity) and CPHA (Clock phase) are both zero. Data on the MOSI and MISO lines are therefore valid on the rising edge of the clock. When chip select for slave device is low, writing instruction is followed by address and data bits.

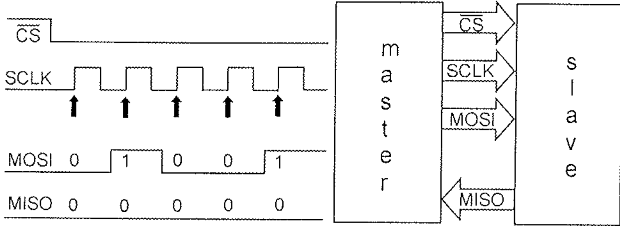


Figure 3: Example of the SPI communication protocol.

From the block diagram on figure 2 we can see, that such SPI interface design can be quite straight forward. There are very few extra blocks necessary. We require one address decoder, one clock multiplier and divider, some electronics for enabling and disabling register operations, eleven eight bit registers and two serial to parallel registers - one for address and one for data.

3. Implementation of the I^{2}C interface on the ASIC 2

Serial communication protocol for the ASIC 2 uses I^{2}C interface for reading fifty-six information bits that are also used for trimming DAC structures and setup the operation of the integrated circuit. This demand is quite close to that for the ASIC 1.

Communication must run between the ASIC 2 and the Atmel eeprom integrated circuit AT24CXX /3, 4/. When one IC that wants to talk to another, the communication procedure goes as follows:

- Wait until there is no activity on the I^{2}C bus. This is when SDA (data) and SCL (clock) wires are both high.
- Reserves the communication bus. All other ICs then wait for the clock and address to appear on the bus.
- Provides a clock signal. It will be used by all the ICs for the synchronization of the transfer. The data on the data wire is valid when clock wire switches from low to high.
- Places on the bus the unique binary address of the IC that it wants to communicate with.
- Puts appropriate bit on the bus, whether it wants to send or receive the information.
- Waits for the other IC to acknowledge the communication.
- After receiving acknowledge, it starts transferring data. After every eight bits of data, it waits for a new acknowledge.
- After all data is transferred, it sends stop bit to the bus.

Figure 4 presents the implemented sequence of protocol requirements for our purpose. Default eeprom address for AT24CXX is "1010" and additional three bits "000" are used for addressing different memory pages or different devices on the bus. If we use for example AT24C01 with 1K of memory, it has address "1010000". Reading starts at byte with address 0x01.

From figure 4 we can see, that we need besides fifty-six information bits also additional thirty-seven bits thanks to the communication protocol. Therefore we actually have to monitor bus clock for ninety-three bits. For that purpose we decided to use two decimal counters, one clock divider and multiplier, input data monitor, action select circuit and seven eight bit shift-parallel registers. Since the data, that is stored in seven eight bit registers also fine adjusts DAC structures, it is necessary to read them in parallel to avoid erratic operation. The same case was in section two while we discussed ASIC 1. Such ASIC 2 structure is generally presented on figure 5. We can easily see that there is extra complexity according to the ASIC 1 structure on figure 3.

At this time we must also mention the Philips's position, that all chips (IC, ASIC, FPGA, etc) that can talk to the I^{2}C bus must be licensed. It does not matter how this interface is implemented /1, 11/. Since we only perform reading

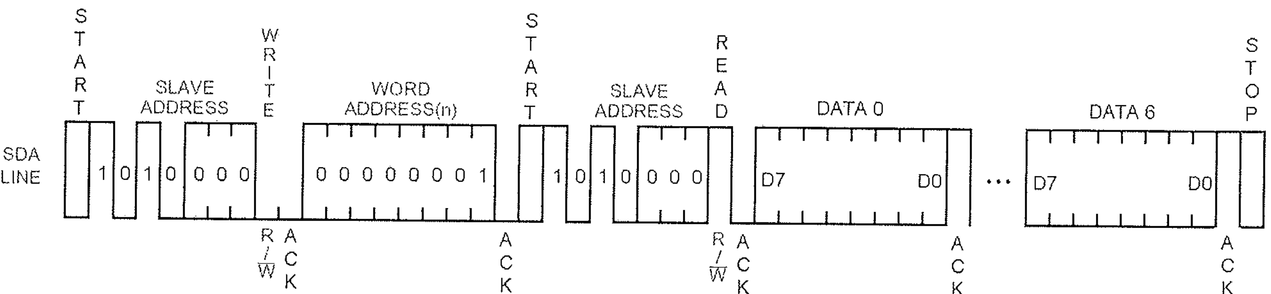


Figure 4: Communication procedure form AT24CXX to ASIC 2.

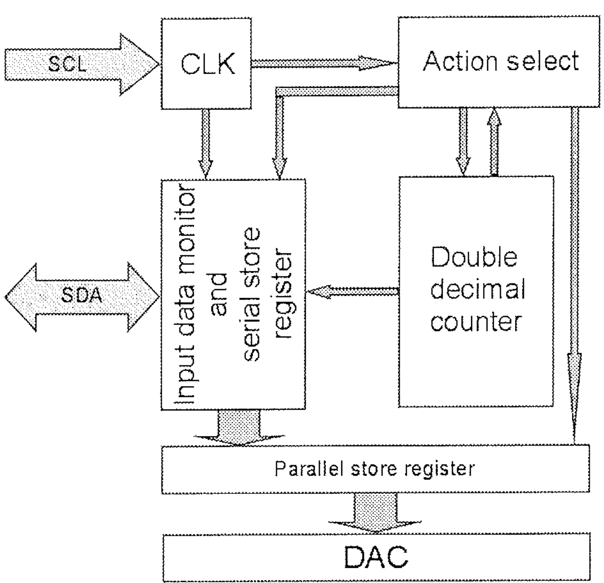


Figure 5: I^2C interface block diagram for ASIC 2.

from the eeprom, such license is already covered by eeprom manufacturer and is not additionally required for our ASIC 2.

4. Comparison of the implemented serial interfaces

Previously described interface approach on the ASIC 1 required for realization 3784 transistors occupying 0.1 mm^2, what represents 1.2 percent of the chip area. ASIC 2 required for the interface realization approximately 4696 transistors occupying 0.18 mm^2, what represents approximately three percents of the chip area.

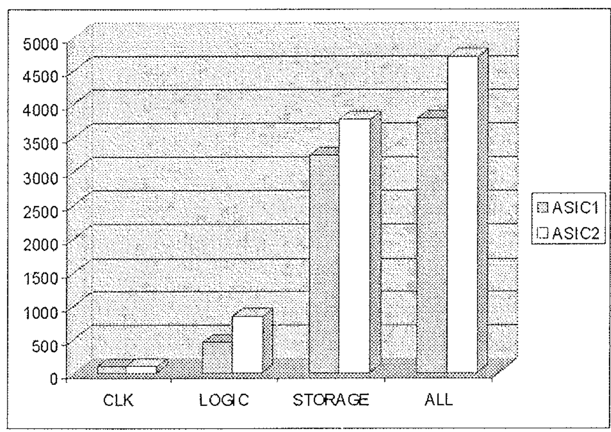
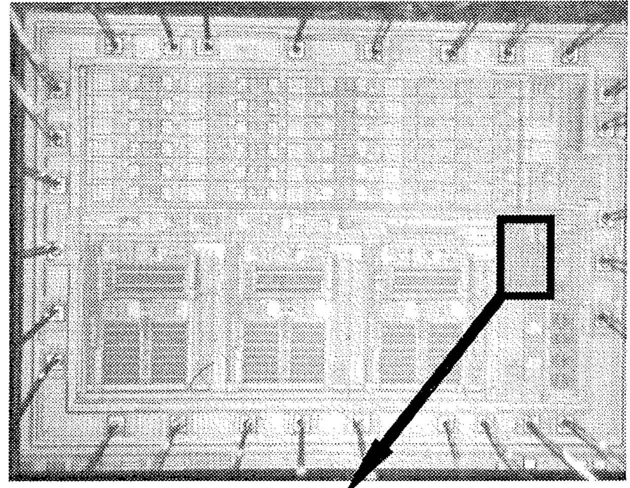


Figure 6: Number of transistors that were necessary for practical ASIC 1 and ASIC 2 interface realization.

Diagram on figure 6 presents the number of transistors that was used for realizing different interface tasks on ASIC 1 and ASIC 2. Realization of the auxiliary clock signals required almost identical number of transistors. It is also clear, that less communication wires required more digital logic gates for input stream processing. The reason for different number of necessary transistors for storage is due to the higher complexity of the I^2C. It requires some additional functions to be included in storage registers. The difference to consider is also the fact that ASIC 1 needs to store eighty bits in ten registers, while ASIC 2 needs to store fifty-six bits into seven registers.

On the other hand, the design of storage registers does not require a lot of designing time, since the same cells are frequently repeated. More demanding is the design and simulation of the interface logic. From figure 6 we can clearly see that choosing SPI interface requires less design effort. Our rough estimation is that necessary time to



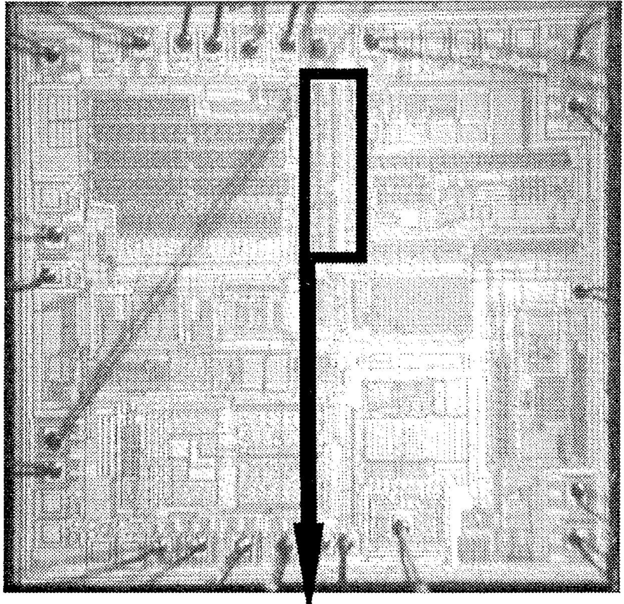


Figure 7: In scale comparison of the ASIC 1 and ASIC 2 with marked areas that are in use by serial interfaces.

incorporate and simulate SPI interface on the ASIC interface takes about half the time necessary for the I^2C interface simulation.

ASIC 1 is realized in 0.6um CMOS technology. It is designed to control 3D strain gauge probe and to process the strain gauge generated signals for 3D computer modeling purposes. ASIC 2 is realized in 0.8um CMOS technology and controls the closed loop current measurement sensor that consists from a full bridge built with MR sensors /12/. Figure 7 presents in scale comparison of the ASIC 1 and ASIC 2 with marked SPI and I^2C data interface areas.

Although both SPI and I^2C provide good support for communication with slow peripheral devices that are accessed intermittently, each of the mentioned communication ways has its own advantages towards each other. I^2C is best if we have just two signal lines to spare or if we need strong line drivers. If the clock speed should be faster than 400 kHz SPI is most likely better and simpler choice. SPI is also better suited for applications that are naturally suited as data streams while I^2C is better for communication with on-board devices that are accessed on an occasional basis.

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OPTIMAL DIMENSIONING OF COMPONENTS FOR A HIGH VOLTAGE FEEDTHROUGH

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Key words: components for power delivery, dielectric materials, dielectric strength, dissipation constant, feedthrough, high voltage applications, high voltage breakdown, RF power, RF power equipment, unbalanced load impedance

Abstract: The design of high voltage feedthrough components needs to satisfy mutually contradictory requirements. Selected geometries, dimensions, and materials of a high voltage feedthrough need to prevent voltage breakdown under worst case conditions, while size and weight are often constrained. The compact size requirement is less important in massive systems (distribution of electric energy), but it becomes critical with requirements of limited space and/or low mass. Both constraints, on size and weight, are crucial in RF power delivery systems for plasma processing in the semiconductor industry and in satellite-mounted instruments for space exploration, such as instruments for solar wind measurements. Expressions for optimal dimensioning of a high voltage feedthrough are derived in this paper for the case of delivering RF energy to a plasma chamber via an impedance matching network. Derived geometries and expressions are useful in design of high voltage feedthrougs in RF and other engineering areas (instruments for space exploration, instruments for high-energy physics experiments, X ray systems, systems for distribution of electric energy).

Določitev optimalne geometrije in izpeljava izrazov za dimenzioniranje komponent visokonapetostnega prehoda

Kjučne besede: dielektrični materiali, dimenzijska optimizacija, močnostne komponente, RF energija, RF močnostna oprema, neuglašena impedanca bremena, visokonapetostne komponente, visokonapetostni preboj

Izvleček: Konstruiranje komponent visokonapetostnih prehodov mora zadovoljiti izključujoče se zahteve. Velikosti in materiali komponent visokonapetostnega prehoda morajo preprečiti napetostni preboj pri najneugodnejših pogojih delovanja, in sistemske zahteve pogosto omejujejo velikost in maso visokonapetostnih komponent. Zahteva po majhnih dimenzijah in masah visokonapetostnih prehodov je manj pomembna v velikih sistemih, kot na primer pri distribuciji električne energije. Zahteva po majhnosti pa je kritična, kadar so dimenzije in masa celotne naprave vnaprej omejene. Kompaktne izmere in majhna masa visokonapetostnih sistemov sta elementarni zahtevi v a) konstrukciji sistemov za generiranje in dovajanje elektromagnetne energije v radijskem frekvenčnem (RF) območju za vzbujanje RF plazme za prizvodne procese v izdelavi mikroelektronskih vezij, in b) v konstrukciji satelitskih sistemov in instrumentov.

V tem prispevku so določene optimalne geometrije in so izvedeni izrazi, potrebni za optimalno konstruiranje visokonapetostnega prehoda pri dovajanju RF energije v plazemsko komoro preko sistema za impedančno prilagajanje. Izvedene geometrije in izrazi so uporabni za načrtovanje visokonapetostnih prehodov v RF tehniki in na drugih področjih (instrumenti za raziskovanje vesolja, instrumenti za eksperimentalno delo v visoko-energetski fiziki, roentgenski sistemi, distribucija električne energije).

1. Introduction

A universal problem in the design of RF power equipment is the transfer of RF power across equipment walls. Typical examples are energy transfer out of RF generators, into and out of matching networks, and into loads. At high powers, the physical design of such feedthroughs runs into the difficulty of satisfying mutually contradictory requirements. One requirement, related to voltage, is that there be sufficient separation between the center conductor and the wall. The other requirement, not fundamental but quite common, is that of over-all size reduction - which may limit the space available for the feedthrough. When the impedance is controlled, as out of a generator and into a matching network (the two being connected by a 50 Ohm cable), tested commercial solutions exist for different power ranges. It is at the interface of the loads (e.g., the RF plasma chamber) and matching networks /1,4/, that the RF and mechanical designers face the challenge of geometric optimization /3/. What makes this interface critical is the uncontrolled impedance of the load /2, 5/. For a given power, whose *maximal* value is known as the power rating of the generator P_{gen_rated}, and for variable load impedance, the voltages that may appear at the feedthrough can reach extremely high values. Hence, the feedthrough design voltages are not those expected in steady state operation, but those that may be generated by the worst transients, however short.

Thus, for a generator power rating P_{gen_rated} and maximal transient load impedance Z_{max} is

$$P_{gen_rated} > \frac{V_{eff_load}^{\;2}}{|Z_{max}|},$$

and the feedthrough *design* voltage (peak value) is

$$V_{max} = K\sqrt{2P_{gen_rated}|Z_{max}|}, \quad (1)$$

where K is the designer's safety factor.

Fortunately, the feedthrough design problem naturally splits into two parts. One is the optimization of conductor shapes, regardless of the required maximal voltage rating; the other is the selection of its overall dimension. The first part, which is pure physics, can be solved once for all for any type of feedthrough geometry - which is done in the present paper for an easily manufactured feedthrough. The second part depends on the application. Here, we only suggest guidelines.

2. Derivation of expressions for optimization of shapes and dimensions of conductors

We state the problem as follows:

For a given round hole opening of diameter D *in a cabinet wall determine the feedthrough shape that withstands the highest RF voltage if the dielectric is air.*

Here, D is the variable that characterizes the physical size of the solution (second part of the problem). As we shall see, it is proportional to V_{max}.

The mechanical feedthrough model is that of a cylindrical conductor (usually made of copper tubing) of diameter d passing at a right angle through the center of the hole. The support issue is irrelevant in principle, provided the corona paths along insulator surfaces are sufficiently long.

The voltage limit for this model is defined by the onset of arcing, which would take place between the center conductor and the wall over a distance (D - d)/2. As arcing begins at local ionization spots[1] when the dielectric field exceeds the medium's characteristic breakdown value, (about 1000 V/mm for dry air), the often quoted computation of electric fields as voltage divided by distance regularly leads to grossly under-designed feedthroughs. This is because the voltage over distance expression is valid only between parallel capacitor plates. In all other cases, we must use the exact definition of the electric field, which is the gradient of the potential function. This is particularly true near all edges. The edge of the window in a cabinet wall is the critical one for feedthroughs. It thus follows that all radii of curvature must be maximized, not only the distances between conductors. This is why we install into the window a tube of outer diameter D and wall thickness w, as shown in Figure 1. The length of this tube is not important. It can be optimized with respect to other considerations (e.g., mechanical structure). The optimal wall thickness w of the tube will be determined below.

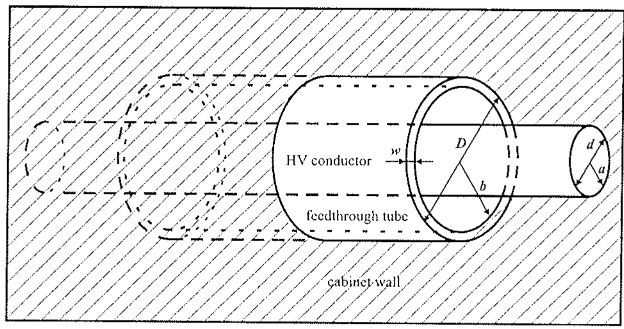

Figure 1 Tube-type high voltage feedthrough.

Disregarding for the time being the edge effects at the end of this tube, our first task is to determine the optimal diameter of the inner conductor in terms of hole opening of diameter D in a cabinet wall. To this end, we view the geometry as a cylindrical capacitor, whose inner electrode is of outer radius a = d/2 and outer electrode of inner radius b = (D - 2w)/2. Solving the Laplace equation for the space within the capacitor, i.e., $\nabla^2\Phi = 0$, the potential function $\Phi=\Phi\;(r)$ between the two conductors is

$$\Phi(r) = \frac{V}{\ln\left(\frac{b}{a}\right)}\ln\left(\frac{b}{r}\right).$$

The magnitude of the electric field is then $E = |\nabla\Phi|$, i.e.,

$$E = \left|\frac{\partial\Phi}{dr}\right| = \frac{-V}{r\ln\left(\frac{a}{b}\right)}.$$

Clearly, its maximal value is at the minimum value of r, which is $r = a$:

$$E_{max} = \frac{-V}{a\ln\left(\frac{a}{b}\right)}. \quad (2)$$

This value is to be minimized by properly selecting the ratio a/b. For a given b, we thus require $\partial E_{max}/\partial a = 0$.

1 *If the medium is not air, but a dielectric, the language may change from "arcing" to "punch through", but the arguments and the calculations are identical.*

$$\frac{dE_{\max}}{\partial a} = \frac{V}{\left(a^2 \ln\left(\frac{a}{b}\right)\right)^2}\left(\ln\left(\frac{a}{b}\right) + a\frac{b}{a}\frac{1}{b}\right) = 0,$$

which implies

$$\ln\left(\frac{a}{b}\right) + 1 = 0.$$

Hence, the solution is

$$a = b/e.$$

This establishes one relationship between D, d, and w:

$$d = \frac{D - 2w}{e}.$$

The next task is to determine the optimal value of w.

The following intuitive arguments give us a starting point: To minimize the field inside the capacitor, it is better to have a small value of w, as this leaves a greater spacing between the conductors. A thin wall, however, implies a small radius of curvature at the edge, namely $w/2$, as it is shown in case *C* in Figure 2. Hence, from the point of view of edge effects, it is better to have a thicker wall.

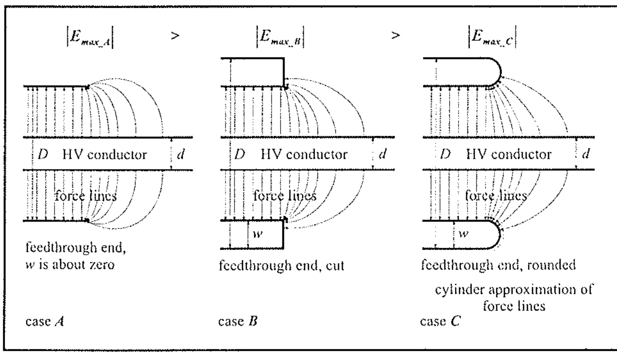

Figure 2 Ends of tube-type high voltage feedthroughs.

An exact solution to the problem of optimal wall thickness would also give us the optimal shape according to which the edge should be formed. Such a shape is not present in cases *A* and *B* in Figure 2 that are simple to manufacture. From the standpoint of machining, one would easily decide for either case *A* or case *B* in Figure 2.

Figure 2, case *C* is quite close to an exact solution. Additional computational and machining efforts of an exact solution of the optimal edge shape would hardly be justified by the marginal improvement. We thus assume that the edges terminate in a semicircular profile of radius $w/2$. For a heuristic estimation of the minimal value of $w/2$, we note that the density of force lines near the edge (but inside the cylinder) is equal to the density at the inner conductor divided by e. Hence, in a good approximation, we may increase the density of lines at the edge of the cylinder by a factor of e without degrading the voltage rating of the device, as suggest the geometries and force lines shown in dashed lines in Figure 2, case *C*. This occurs if we take the radius of curvature at the edge to be the radius of the inner conductor divided by e, i.e.,

$$w = d/e.$$

With the previous equation, this gives us the complete solution:

$$w = \frac{D}{e^2 + 2},$$

$$d = ew.$$

Numerically,

$$w = \frac{D}{9.39}, \tag{3}$$

$$d = \frac{D}{3.45}. \tag{4}$$

The next task is to relate the window's diameter D to the absolute maximum of peak RF voltage, V_{max}, (1) that could possibly appear on the conductor. The governing equation is (2). Combining it with relation (1), we get

$$E_{\max} = \frac{-V_{\max}}{a \ln\left(\frac{a}{b}\right)} = \frac{-K\sqrt{2P_{gen_rated}\left|Z_{\max}\right|}}{a \ln\left(\frac{a}{b}\right)}.$$

Substitution of $a/b = 1/e$ and

$$a = \frac{d}{2} = \frac{D - 2w}{2e} = \frac{e^2}{2e\left(e^2 + 2\right)}D$$

yields

$$E_{\max} = K\frac{2e\left(e^2 + 2\right)\sqrt{2P_{gen_rated}\left|Z_{\max}\right|}}{e^2 D}.$$

Expressing power in kW, all dimensions in meters, and taking $E_{max} = 10^6$ V/m, we finally get

$$D = K\frac{2\left(e^2 + 2\right)}{1000\,e}\sqrt{2P_{gen_rated}\left|Z_{\max}\right|} =$$

$$= 6.91\times10^{-3}K\sqrt{2P_{gen}\left|Z_{\max}\right|}.$$

Numerically,

$$D[\mathrm{cm}] = 0.7K\sqrt{2P_{gen_rated}\left[kW\right]\left|Z_{\max}\left[\Omega\right]\right|},$$

or

$$D[\mathrm{cm}] = 0.7K\,V_{\max}\left[\mathrm{kV}\right].$$

The safety factor K remains to be selected. For a 50 percent safety margin, for example, we would have $K = 1.5$, and hence, the simple rule of thumb

$$D[\text{cm}] = V_{\max}[\text{kV}] \ . \tag{5}$$

If V_{max} has already been estimated with a reasonable safety margin, one can take $K = 1$, which yields

$$D[\text{cm}] = 0.7\, V_{\max}[\text{kV}] \tag{6}$$

Thus, at least one centimeter of window diameter opening is required for every seven hundred volts of peak RF voltage. This assumes that the edge of the window is mechanically terminated with a tube that leads through the window in the equipment wall, Figure 1. The tube is to be made according to the optimal dimensions derived above. Any other dimensioning makes matters worse.

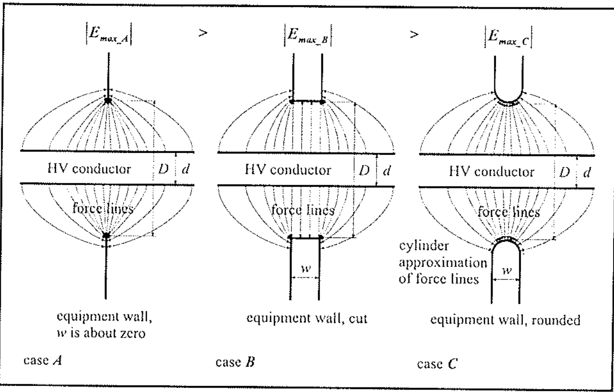

Figure 3 *High voltage feedthrough without a built-in tube.*

These results are for framed feedthroughs, which are often a natural mechanical solution regardless of voltage rating considerations. If the frame is not needed, however, its length may be reduced to the minimum, which is its wall thickness, w. It may then be implemented as an integral part of the housing wall, provided its edges are machined to a semi-circular profile, as illustrated in Figure 3, case C. The required opening D is then smaller, since it does not have to accommodate the frame. Geometries and force lines shown dashed in Figure 3 are identical to those in Figure 2, and so is the analysis. Results, i.e., modified design equations are:

$$d = \frac{D}{e}, \tag{7}$$

$$w = \frac{d}{e} = \frac{D}{e^2}, \tag{8}$$

$$D[\text{cm}] = 0.6\, K\, V_{\max}[\text{kV}]. \tag{9}$$

Cases A and B in Figure 3 would be simple to manufacture, but such geometries are inadequate for optimization of feedthrough dimensioning, since sharp edges imply intense local peaks in force line densities.

3. Worked out examples

Let us assume that the RMS voltage at full generator power in a matched condition is 2 kV. The peak voltage is then $2\times\sqrt{2}$, which can be conservatively rounded to 3 kV. Let us further assume that experience and computations indicate that in the case of worst transient mismatch the steady state voltage gets doubled, at most. Then, we may take V_{max} = 6 kV. Equations (6), (4), and (3) then yield

$$D = 0.7 * 6 = 4.2 \text{ cm},$$

$$d = \frac{4.2}{3.4} = 1.24 \text{ cm},$$

$$w = \frac{4.2}{9.4} = 0.45 \text{ cm}.$$

Hence, the smallest possible robust feedthrough requires a window opening of 4.2 centimeters, a center conductor 1.24 cm in diameter and a window frame of wall thickness 0.45 cm. Figure 1 shows the general appearance. Both ends of the tube are rounded as shown in Figure 2, case C. The length of the tube is arbitrary, and may be very short.

For a straight feedthrough, case C in Figure 3 (no separate tube), equations (9), (7) and (8) yield the solution

$$D = 0.6 * 6 = 3.6 \text{ cm},$$

$$d = \frac{D}{e} = 1.32 \text{ cm},$$

$$w = \frac{1.32}{e} = 0.49 \text{ cm}.$$

We see that the diameter of the center conductor and the thickness of the wall are essentially the same, but a much smaller opening is required. The trade-off is in the thickness of the housing wall, which must be 0.5 cm. It is also essential that the hole be smoothly milled to a semi-circular profile.

Finally, we must emphasize that this entire analysis refers to air as a dielectric. The supporting insulators are also assumed to be designed for a sufficiently long surface corona path. Clearly, a substantially more compact feedthrough is possible if the window and central conductor can be completely and tightly potted (no air gaps) in some appropriate structural dielectric. The relative geometry of the optimal solution remains the same, i.e., relations (7) and (8) are still valid, but equation (9) becomes

$$D[\text{cm}] = 0.6\frac{\varepsilon'}{r} K V_{\max}[\text{kV}], \tag{10}$$

where ε' is the dielectric's relative dielectric constant, and r its dielectric strength relative to air. We see that the die-

lectric constant ε' works against us, while the dielectric strength r is in our favor.

Example:

We consider the same problem as above, but with Teflon encapsulation. We have $\varepsilon' = 2.5$, and let us take r = 50 (which corresponds to a dielectric strength of 50 kV per millimeter). Then,

$$D = 0.6\frac{2.5}{50}V_{\max} = 0.03V_{\max} = 0.03*6 = 0.18\,\text{cm},$$

$$d = \frac{0.18}{e} = 0.066\text{cm}.$$

The minimal wall thickness (w = 0.024 cm) is irrelevant in this case, as any realistic housing wall would substantially exceed it in any event.

This example points to two issues not considered above:

1. The current carrying capability of the conductor. Clearly, the wire with a diameter of 0.6 mm in this example is probably unrealistic (unless the minimal impedance of the load is so high that the RF current is very small). However, it is the lesson that counts: Once a feedthrough design is completed, the conductor diameter, d, must be reviewed for its current carrying capability. At RF frequencies, the resistance must be computed accurately by taking the skin effect into account. If a larger diameter is called for, the window diameter D must be increased accordingly - either by redoing the mathematical analysis under the assumption of a given d, or, overconservatively, by preserving the geometric relations derived above (i.e., by taking $D = ed$).
2. The dissipation in the dielectric. If the dielectric were ideal, i.e., if its dissipation constant ε'' were zero, (as it is in air), the design equation (10) would suffice. With realistic dissipation constants, it is not. The reason is that at sufficiently high field strengths and frequencies, even for the smallest available ε'' (as in Teflon and Ultem), enough power is dissipated in the dielectric to heat it faster than it can cool. As the dielectric strength decreases with temperature /6/, thermal runaway and catastrophic failure immediately follow.

We extract the following lesson from these considerations:

In selecting a potting dielectric, aim at a minimal dielectric constant ε' and minimal dissipation constant ε'' It is a mistake to search for maximal dielectric strength r, as it is most unlikely that the dielectric strength of the cold dielectric will ever be a limiting design parameter.

4. Conclusion

At high voltages, the physical design of feedthroughs runs into the difficulty of satisfying mutually contradictory requirements. One requirement, related to voltage, is that there be sufficient separation between the center conductor and the wall. The other requirement is saving the equipment volume. The feedthrough design problem splits into optimization of shapes, in selection of materials and into calculation of dimensions.

Optimal feedthrough shapes and expressions for optimal dimensioning are derived in this paper. Our optimization suggests selection of materials with a low dielectric constant and with a low dissipation constant for potting dielectrics. It is most unlikely that the dielectric strength of the cold dielectric would be a limiting design parameter.

Acknowledgments

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ELEKTROKEMIJSKO IMPULZNO NANAŠANJE BAKRA V PROCESU IZDELAVE TISKANIH VEZIJ

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Kjučne besede: tiskano vezje, skoznja luknja, impulzno nanašanje, transport snovi, gostota toka, tokovni vir

Izvleček: Miniaturizacija električnih naprav narekuje razvoj večplastnih elektronskih tiskanih vezij z visoko integracijo komponent, zaradi česar se zmanjšujeta širina povezav in premer skoznjih lukenj na tiskanini. Nanašanje bakra na ta mesta postaja v procesu izdelave tiskanega vezja vedno bolj zahteven postopek, od katerega je odvisna kakovost in cena izdelka. Zlasti v primeru dimenzijsko zahtevnih oblik, kjer s klasičnim postopkom nanašanja ne moremo izpolniti zahtev kupca, se zato poslužujemo nove tehnologije elektrokemijskega impulznega nanašanja. Njene prednosti se kažejo v enakomernejšem nanosu in v njegovih izboljšanih mehanskih lastnostih. To dosežemo z izbiro ustreznih parametrov toka, preko katerih lahko vplivamo na kinetiko elektrodnih reakcij na način, ki je v članku principielno opisan. Nezaželen produkt napajanja elektrokemijskega procesa z impulznim tokom je kapacitivni vpliv dvojnega sloja, ki je odvisen od dinamike tokovnih impulzov. Zgolj z modifikacijo klasičnega enosmernega vira ne moremo zagotoviti ustrezne dinamike toka, zato smo predlagali novo topologijo impulznega tokovnega vira, na podlagi katere smo izdelali eksperimentalni model. Ob koncu so zbrani doseženi rezultati, ki omogočajo primerjavo enosmernega in impulznega postopka nanašanja bakra na zahtevnejša tiskana vezja.

Pulse plating in PCB manufacturing

Key words: PCB, via, pulse plating, mass transport, current distribution, pulse current source

Abstract: The continuing trend of miniaturization is driving PCB design more and more towards HDI and multi-layer boards. This means finer tracks, smaller holes and higher aspect ratios. As a consequence, the conventional acid-copper electroplating becomes very demanding and affects the performance and the price of the finished board. The ability to plate sophisticated boards is given by the use of pulse current instead of a DC. Since the pulse plating process takes place at higher current densities, a fine grain structure of the deposit can be obtained and hence the deposit porosity is reduced. Uniform deposit distribution is another advantage offered by the pulse technology. It should be noted, that current "shaping" represents only one way of influencing the complicated system which contains many other process parameters. To understand the interdependence of these parameters with pulse parameters qualitatively, a basic mass transport and its influence to the current distribution are described. Charging and discharging of the double layer, which is a side effect of the pulse plating, represents the main limitation of arbitrary pulse parameters setting. It can be reduced providing sufficient slopes of current pulses. Considering this, we also proposed a new topology of pulse current source and built an experimental model. At the end, the results of copper deposition obtained under bipolar pulse current conditions are collected and compared to the results obtained using conventional technology.

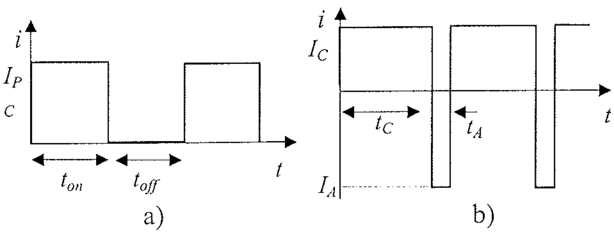
1. Uvod

Elektrokemijsko nanašanje kovin je proces, ki zahteva temeljito interdisciplinarno poznavanje metalurgije, kemije in močnostne elektronike. Prav slednja je v preteklem desetletju bistveno pripomogla k novim spoznanjem na področju nanašanja kovin na osnovne materiale s pomočjo moduliranega (impulznega) toka. Prednosti impulzne tehnologije nanašanja pred nanašanjem z enosmernim tokom se kažejo v izboljšanih mehanskih lastnostih in v enakomernejši porazdelitvi kovinskega nanosa po površini /1-4/. Tehnologija je v zadnjih letih deležna intenzivnega razvoja, kar je posledica stopnjevanja zahtevnosti industrijskih izdelkov. Posledično s klasičnim enosmernim postopkom nanašanja kovin ni mogoče zadostiti vsem postavljenim zahtevam. S tovrstnimi problemi se soočamo tudi v proizvodnji tiskanih vezij, kjer se zaradi visoke integracije elektronskih komponent na tiskanem vezju zmanjšujeta širina vezi in premer skoznjih lukenj, debelina vezja pa se povečuje. Izziv v procesu izdelave tiskanih vezij je nanašanje bakra v skoznje luknje s premerom, ki je manjši od 200 μm, in z razmerjem med debelino plošče in premerom skoznje luknje (AR - Aspect Ratio) vse tja do 20.

Pri nanašanju z enosmernim tokom je namreč porazdelitev gostote toka in s tem debelina nanosa proti sredini luknje izrazito neenakomerna. V primeru zahtevnejših tiskanih vezij so proizvajalci prisiljeni zmanjšati amplitudo toka, s katerim poteka proces bakrenja, in na ta način zagotoviti predpisano debelino (20 μm) kovinskega nanosa znotraj skoznjih lukenj. Ukrep je resda enostaven, vendar vpliva na količino dnevne proizvodnje, saj se skladno z zmanjšanjem amplitude toka podaljša trajanje postopka nanašanja.

Napredek na področju nanašanja kovin zagotavlja tehnologija nanašanja z impulznim tokom. Slika 1 kaže primer preprostega (katodnega) tokovnega impulza (a) in obliko impulza z anodno polarizacijo (b), kakršen se je uveljavil pri sodobnih procesih nanašanja bakra.

Kot bomo videli v nadaljevanju, lahko z amplitudnimi in časovnimi parametri toka vplivamo na porazdelitev gostote toka po površini tiskanega vezja in s tem na enakomernost ko-



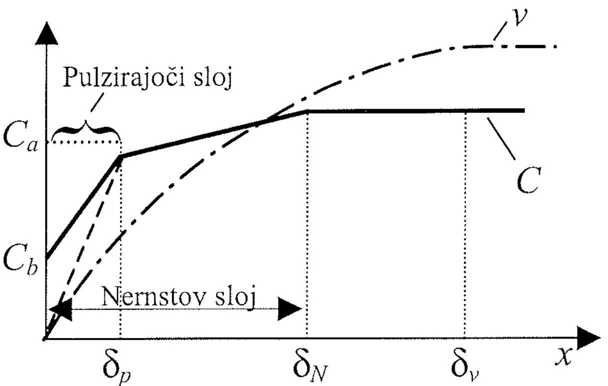
Slika 1. Oblika impulznega toka: a) preprosta, b) z anodno polarizacijo

vinskega nanosa. Zaradi številnih vplivnih veličin, ki nastopajo v procesu elektrokemijskega nanašanja (temperatura, vrsta elektrolita, vrsta kovine, intenzivnost mešanja, koncentracija organskih dodatkov...), je optimalne vrednosti parametrov smiselno določiti iz serije poskusov in meritev. Zato mora biti impulzni tokovni vir, s katerim napajamo proces, sposoben generirati tokovne impulze s parametri, nastavljivimi v širokem območju.

2. Fizikalno ozadje impulznega nanašanja kovin

Porazdelitev gostote toka na posameznih mestih tiskanega vezja (le-to v procesu nanašanja tvori katodo elektrolitske celice), je odvisna od geometrije sistema, prevodnosti elektrolita in elektrod ter od kinetike elektrodne reakcije. Na slednje imamo možnost vplivati preko parametrov električnega toka. Pri tem igra ključno vlogo poznavanje masnega transporta snovi, ki v elektrolitu poteka na tri načine: s konvekcijo, difuzijo in z migracijo. Za migracijo predpostavljamo, da bistveno ne prispeva k skupnemu transportu, zato jo bomo v nadaljevanju zanemarili. Transport snovi s konvekcijo poteka pod vplivom zunanjega mešanja elektrolita. Zaradi njegove viskoznosti, se ob katodi formira hidrodinamični sloj debeline δ_v, znotraj katerega hitrost gibanja elektrolita v upada (slika 2). Kovinski ioni tik ob površini katode se izločajo v obliki kovine, kar povzroči nastanek koncentracijskega gradienta (koncentracija ionov v smeri proti katodi pada). Transport snovi znotraj hidrodinamičnega sloja zato ne poteka zgolj s konvekcijo, temveč tudi z difuzijo. Za lažje razumevanje je smiselno razmere v okolici katode idealizirati, zato vpeljemo fiktivni parameter, Nernstov difuzijski sloj, debeline δ_N. Na ta način smo predpostavili mirujoč (stacionaren) difuzijski sloj, znotraj katerega poteka transport snovi zgolj z difuzijo, izven tega sloja pa prevladuje transport snovi s konvekcijo. Pravkar opisno dogajanje ustreza razmeram pri nanašanju z enosmernim tokom.

Sedaj predpostavimo napajanje procesa z impulznim tokom, pri čemer naj ima tok obliko pravokotnih impulzov trajanja t_{on} in s pavzo t_{off} (slika 1a). V tem primeru se znotraj Nernst-ovega difuzijskega sloja na strani katode formira dodaten pulzirajoči difuzijski sloj debeline δ_p, ki je precej tanjši od stacionarnega sloja. Koncentracija ionov znotraj novonastalega sloja pulzira s frekvenco tokovnih impulzov, minimalno vrednost na površini katode pa doseže ob koncu tokovnega impulza. Potek koncentracije kovinskih ionov C v odvisnosti od razdalje $\underline{x}$ od katode pri nanašanju z impulznim tokom kaže slika 2.



Slika 2: Potek koncentracije kovinskih ionov v odvisnosti od razdalje od katode

Nagib premice v pulzirajočem sloju je sorazmeren amplitudi impulznega toka

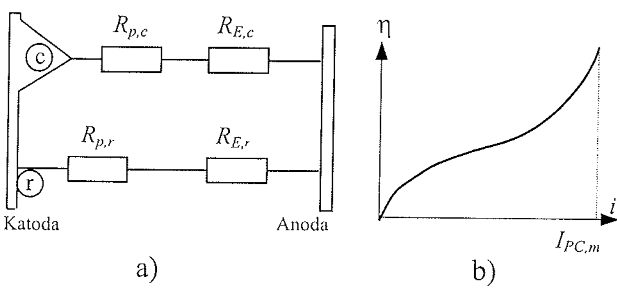
$$I_{PC} = -nFD_a \frac{C_a - C_b}{\delta_p}, \qquad (1)$$

pri čemer je n število elektronov na izločeni ion kovine, F je Faradeyeva konstanta, D_a pa je difuzijski koeficient. Na enak način lahko iz nagiba premice v stacionarnem difuzijskem sloju določimo srednjo vrednost impulznega toka, ki je ekvivalentna amplitudi toka pri nanašanju z enosmernim tokom. Amplitudi toka, pri kateri pade koncentracija ionov ob katodi na nič ob koncu tokovnega impulza, pravimo mejna vrednost toka $I_{PC,m}$. Iz slike 2 je razvidno, da je nagib premice v stacionarnem sloju, ki je značilen za nanašanje z enosmernim tokom, mnogo manjši od nagiba premice v pulzirajočem sloju ($\delta_p << \delta_N$). Zato je lahko amplituda tokovnih impulzov temu ustrezno večja, kar se odraža v finozrnati strukturi in posledično v izboljšanih mehanskih lastnostih kovinskega nanosa. Pri tem velja omeniti, da se trajanje impulznega postopka v primerjavi s klasičnim načinom nanašanja ne skrajša, saj srednja vrednost impulznega toka, od katere je odvisna hitrost izločanja kovine, ne sme preseči vrednosti, ki je določena z nagibom premice v stacionarnem sloju.

Dodatna prednost impulznega nanašanja, ki jo s pridom izkoriščamo v procesu izdelave tiskanih vezij, je možnost vplivanja na debelino pulzirajočega sloja (δ_p) in s tem, kot bomo videli v nadaljevanju, na porazdelitev gostote toka. Kako globoko se bo pulzirajoči sloj razširil v območje stacionarnega sloja, je namreč odvisno od trajanja tokovnega impulza t_{on}

$$\delta_p = \sqrt{2D_A t_{on}}. \qquad (2)$$

Problematiko neenakomerne porazdelitve gostote toka po površini katode si ponazorimo s sliko 3a, ki ilustrira model upornosti v galvanski kopeli. Katoda je namenoma nepravilnih oblik.

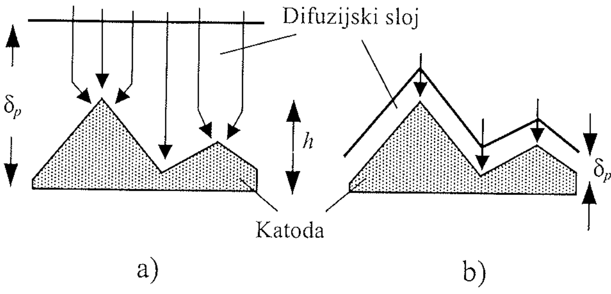


Slika 3: a) Model upornosti v galvanski kopeli; b) polarizacijska krivulja

R_E je upornost elektrolita, R_p pa je katodna polarizacijska upornost na stiku katoda-elektrolit, ki je definirana z naklonom polarizacijske krivulje. Indeksa »c« oz. »r« se nanašata na različni mesti na površini katode. Porazdelitev gostote toka izrazimo z Wagnerjevim številom (*Wa*)

$$Wa = \frac{R_P}{R_E} = \kappa \frac{d\eta}{di} \frac{1}{l}. \tag{3}$$

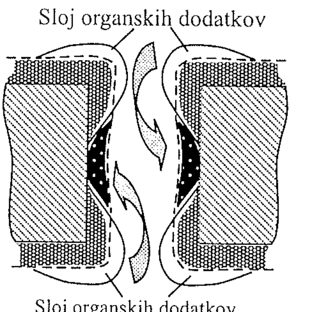
Večje kot je število *Wa*, enakomernejša je porazdelitev toka. V izrazu (3) je κ specifična prevodnost elektrolita, *l* pa je karakteristična dolžina galvanske kopeli. V odvisnosti od razmerja upornosti R_p in R_E ločimo tri karakteristične primere porazdelitve toka: primarna, sekundarna in terciarna tokovna porazdelitev. Pri impulznem nanašanju težimo k terciarni tokovni porazdelitvi, za katero je značilno, da je $R_E << R_p$. Slednje zagotovimo tako, da proces napajamo s tokom, katerega amplituda je reda velikosti mejne vrednosti toka $I_{PC,m}$. V tem primeru poteka ob katodi transport snovi z difuzijo, zato porazdelitev toka ni odvisna zgolj od kriterija (3), ampak tudi od debeline difuzijskega sloja. S tega stališča ločimo dva karakteristična primera, ki sta prikazana na sliki 4. V prvem (slika 4a) gre za tako imenovan mikroprofil, pri katerem je debelina pulzirajočega sloja δ_p večja od karakteristične dimenzije profila *h* (slika 4). Izpostavljeni deli katode se nahajajo na mestu difuzijskega sloja z večjo koncentracijo ionov, zato je gostota toka na teh mestih večja. Tokovnice v obliki puščic na sliki 4 prikazujejo porazdelitev toka vzdolž profila katode.

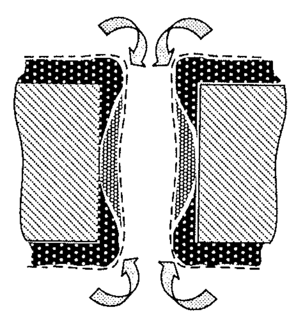


Slika 4: Vpliv difuzijskega sloja na terciarno porazdelitev toka: a) mikroprofil, b) makroprofil

Tipičen primer mikroprofila imamo pri nanašanju bakra v skoznje luknje z enosmernim tokom, in sicer, ko je dimenzija skoznjih lukenj reda velikosti debeline difuzijskega sloja. Le-tega pa določajo hidrodinamične razmere v galvanski kopeli. Situacijo, ko je debelina difuzijskega sloja manjša od karakteristične dimenzije profila, pa imenujemo makroprofil (slika 4b). V tem primeru difuzijski sloj sledi profilu vzdolž katode, zato izenačevalno vpliva na porazdelitev gostote toka in s tem na enakomerno debelino nanosa.

Iz povedanega je razvidno, da lahko v pogojih impulznega nanašanja z ustrezno modulacijo debeline difuzijskega sloja stanje mikroprofila prevedemo na makroprofil in s tem zagotovimo enakomerno porazdelitev toka. Pri tem igrajo odločilno vlogo amplitudni in časovni parametri impulznega toka. V proizvodnji tiskanih vezij se vse pogosteje srečujemo s skoznjimi luknjami z velikim AR. Zaradi slabih hidrodinamičnih pogojev znotraj luknje je konvekcijski transport snovi omejen, zato enakomerne porazdelitve toka v luknji ne moremo doseči zgolj z njeno prevedbo na makroprofil. Skrajni primer so slepe skoznje luknje, kjer imamo opraviti z omejenim pretokom elektrolita. Tovrstnim težavam se izognemo z uporabo impulznega toka z anodno polarizacijo (slika 1b), v kombinaciji z ustreznimi organskimi sredstvi (levelers), ki jih dodajamo v elektrolit. Trajanje negativnega impulza je bistveno krajše od pozitivnega, po amplitudi pa je do trikrat večji. V času negativnega impulza se del predhodno nanešenega bakra raztaplja, zato se koncentracija kovinskih ionov ob elektrodi poveča. Reakcija je burnejša na mestih s povečano gostoto toka, to pa je ravno tam, kjer je v fazi nanašanja izločanje kovinskih ionov intenzivnejše. Dodatna reakcija, ki se odvija v času negativnega (anodnega) tokovnega impulza, je transport molekul organskih dodatkov na mesta s povečano gostoto toka. Tam se formira zaščitni sloj, ki v fazi nanašanja zavira izločanje kovinskih ionov. S tega vidika lahko razdelimo trajanje pozitivnega impulza v dva intervala. V prvem se predhodno raztopljeni kovinski ioni izločajo na mestih z manjšo gostoto toka (sredina skoznje luknje). Zaščitni sloj molekul, ki preprečuje izločanje ionov, se v tem času raztaplja. Drugi interval pozitivnega tokovnega impulza pa nastopi v trenutku, ko se zaščitni sloj molekul v celoti raztopi, nakar se prične izločanje kovinskih ionov tudi na mestih s povečano gostoto toka. Pravkar opisan postopek izločanja kovinskih ionov na sredini in na robovih skoznje luknje kaže slika 5.





Slika 5: Mehanizem delovanja organskih dodatkov na primeru skoznje luknje

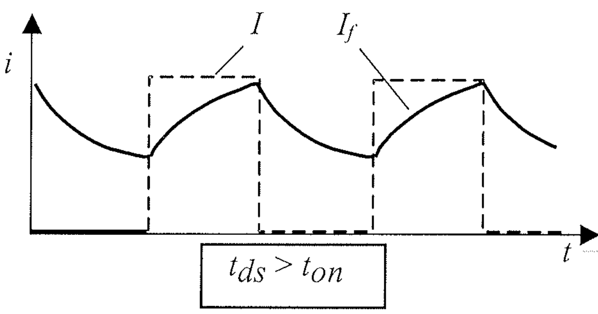
Če nekoliko posplošimo, poteka nanašanje bakra v skoznje luknje po pravkar opisanem postopku v treh fazah. V času negativnega impulza se na mestih s povečano gostoto toka kovinski baker raztaplja in se ob nastopu pozitivnega impulza izloči na mestih z manjšo gostoto toka (sredina skoznje luknje). Tretja faza nastopi proti koncu pozitivnega tokovnega impulza, ko se zaščitni sloj dodatkov raztopi, in se kovinski ioni izločajo na robovih luknje.

4. Vpliv kapacitivnosti dvojnega sloja

Na površini kovinske elektrode, ki je potopljena v elektrolit, se vzpostavi sloj negativne elektrine, ki tvori s slojem pozitivnih kovinskih ionov v elektrolitu električno nevtralnost obeh medijev. Ob delovanju zunanjega električnega polja se z izmenjavo električnega naboja med omenjenima slojema vzpostavi novo ravnovesno stanje. Potek potenciala znotraj slojev ustreza poteku potenciala v kondenzatorju, zato dvojni sloj ponazorimo s kapacitivnostjo C_{ds}. Tok v galvanski kopeli I je sestavljen iz Faradayeve komponente I_f, ki določa hitrost izločanja kovine, in iz kapacitivne komponente I_C za polnjenje kapacitivnosti C_{ds}.

$$I = I_F + I_C = I_F + C_{ds}\frac{d\eta_A}{dt}. \tag{4}$$

Izločanje kovine se prične šele, ko je dosežena napetost aktivacijskega potenciala (η_A), do katerega moramo napolniti C_{ds}. Pri nanašanju z enosmernim tokom to ne povzroča nevšečnosti, saj poteka polnjenje kondenzatorja le ob vklopu usmernika. Razmere pa se bistveno spremenijo pri napajanju procesa z impulznim tokom. Izločanje kovinskih ionov v obliki kovine se prične šele ko je dosežen aktivacijski potencial med elektrolitom in kovino. Zato moramo ob vsakem nastopu tokovnega impulza napolniti kapacitivnost dvojnega sloja na določen potencial. Čas polnjenja dvojnega sloja t_{ds} mora biti bistveno krajši od trajanja tokovnega impulza t_{on}. V nasprotnem primeru je oblika Faradayevega toka popačena, v skrajnem primeru celo izgubi impulzni značaj (slika 6).



Slika 6: Vpliv kapacitivnosti dvojnega sloja na obliko Faradayevega toka

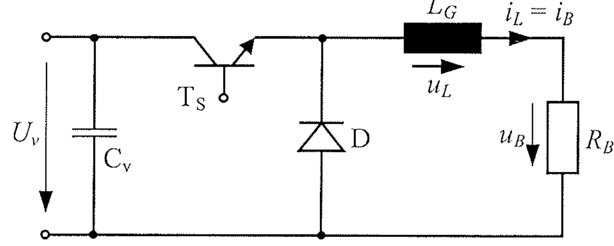
Podobne ugotovitve veljajo za praznjenje dvojnega sloja in trajanje pavze oz. negativnega tokovnega impulza. Metode za izračun časov polnjenja in praznjenja dvojnega sloja so podane v /4/.

Na zmanjšanje vpliva dvojnega sloja, ki nam onemogoča nastavitev poljubno kratkih časovnih parametrov impulznega toka, lahko vplivamo z učinkovitim mešanjem elektrolita in z izbiro ustreznega tokovnega vira. Ta mora biti sposoben generirati tokovne impulze z veliko strmino, kar bistveno pripomore k zmanjšanju kapacitivnega vpliva dvojnega sloja.

5. Visokodinamični impulzni tokovni vir

K snovanju topologije impulznega tokovnega vira smo pristopili z namenom postopnega uvajanja impulznega nanašanja bakra v proizvodnjo tiskanih vezij. Zahteve, ki jih mora vir izpolnjevati, so poleg velike strmine generiranih tokovnih impulzov še vzdrževanje konstantnega, od bremena neodvisnega toka med trajanjem impulza, majhna valovitost izhodnega toka v ustaljenem stanju, galvanska ločitev bremenskega tokokroga od napajalnega omrežja, možnost generiranja bipolarnih tokovnih impulzov in neodvisna nastavitev parametrov toka v širokem območju /5,6/. Z razvojem elementov močnostne elektronike nam je dana možnost izgradnje sofisticiranih pretvorniških naprav, ki delujejo v stikalnem režimu. Prednost tovrstnega pristopa je višji izkoristek in manjše dimenzije pretvornika. Slednje dopušča namestitev naprave v neposredno bližino galvanske kopeli, s čimer zmanjšamo potrebo po dolgih povezovalnih kablih, ki s svojo parazitno induktivnostjo znatno zmanjšujejo strmine generiranih tokovnih impulzov.

Sodobni procesni tokovni viri, ki so namenjeni aplikacijam v elektrokemiji, pogosto temeljijo na topologiji pretvornika navzdol. V območju moči do nekaj 10 kW je to najprimernejša oblika stikalnega pretvornika za napajanje bremena s konstantnim tokom. Principialno shemo pretvornika navzdol kaže slika 7.



Slika 7: Principialna shema pretvornika navzdol

Pretvornik je priključen na vir enosmerne napetosti U_v. Z ustreznim krmiljenjem stikala T_S vzdržujemo tok skozi gladilno dušilko L_G in breme R_B na želeni vrednosti /7,8/. Zaželena je čim manjša valovitost toka v stacionarnem delovanju

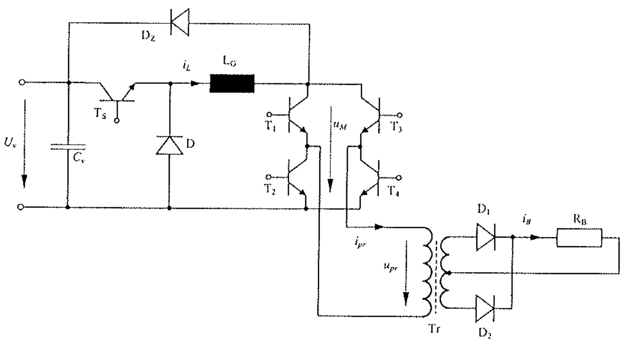
$$\Delta i_L = \frac{U_v}{4 \cdot L_G \cdot f_{st}}, \tag{5}$$

pri čemer je f_{st} frekvenca preklopov stikala. Pri generiranju impulznega toka nas poleg ustaljenega obratovanja zani-

majo tudi razmere v vezju med dinamičnim (impulznim) obratovanjem. Začetna strmina tokovnih impulzov znaša

$$\frac{di_L}{dt} = \frac{U_v}{L_G} \qquad (6)$$

in je odvisna zgolj od napajalne napetosti in induktivnosti gladilne dušilke. Iz primerjave enačb (5) in (6) ter ob upoštevanju, da je stikalna frekvenca f_{st} tranzistorja navzgor omejena, je razvidno, da je nemogoče zagotoviti zadostno strmino tokovnega impulza, ne da bi to vplivalo na povečanje valovitosti toka Δi. Zato je pretvornik s slike 7 neprimeren za generiranje tokovnih impulzov. Njegova pomanjkljivost izvira iz dejstva, da se gladilna dušilka nahaja v bremenskem tokokrogu. To smo upoštevali pri snovanju nove topologije impulznega tokovnega vira. Rešitev, ki jo v nadaljevanju predstavljamo, je prikazana na sliki 8. Pretvornik navzdol, ki nastopa v vlogi vhodnega pretvornika, smo povezali v kaskado s tokovnim razsmernikom. Ta je sestavljen iz tranzistorskega mostiča in transformatorja. Vhodni pretvornik generira konstantno vrednost enosmernega toka na način, kot je bilo predhodno opisano, s tokovnim razsmernikom pa ta tok pretvorimo v zaporedje tokovnih impulzov. Gladilna dušilka L_G je prestavljena iz bremenskega tokokroga v vmesni enosmerni tokokrog, zato na strmino tokovnih impulzov nima vpliva. Ker si pretvornika "delita" gladilno dušilko L_G, mora biti njuno delovanje časovno usklajeno.

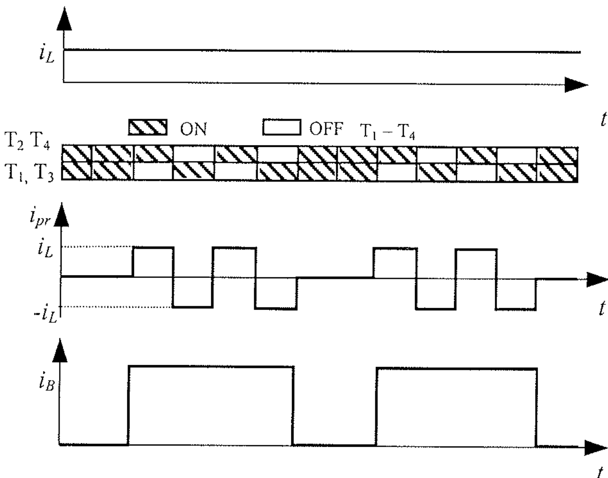


Slika 8: Predlagana topologija impulznega tokovnega vira

V ta namen deluje razsmernik v tako imenovanem kratkostičnem režimu (vsi tranzistorji T_1 do T_4 sočasno prevajajo) ali v razsmerniškem režimu (izmenoma prevajata tranzistorska para T_1-T_4 in T_2-T_3). Tok vmesnega tokokroga v nobenem primeru ne sme biti prekinjen. Delovanje pretvorniškega sklopa je razvidno s slike 9.

V kratkostičnem režimu obratovanja se tok vmesnega tokokroga zaključuje preko kratkosklenjenega tranzistorskega mostiča. Primarno navitje transformatorja je v tem primeru kratkostičeno, zato ni prenosa energije v sekundarni tokokrog in tok skozi breme je nič.

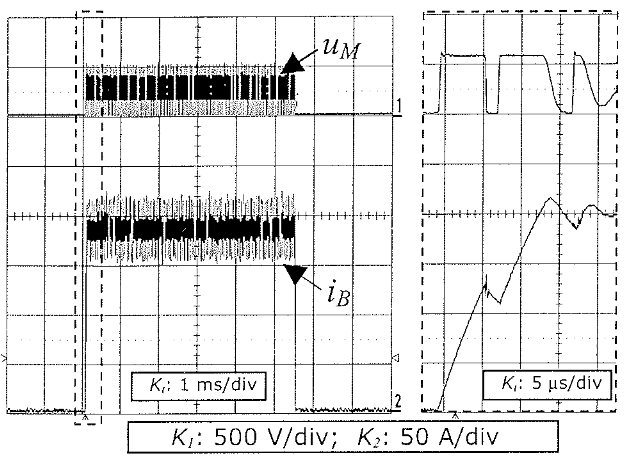
Razsmerniški režim obratovanja nastopi z izmeničnim proženjem diagonalanih parov tranzistorjev. Tok komutira v



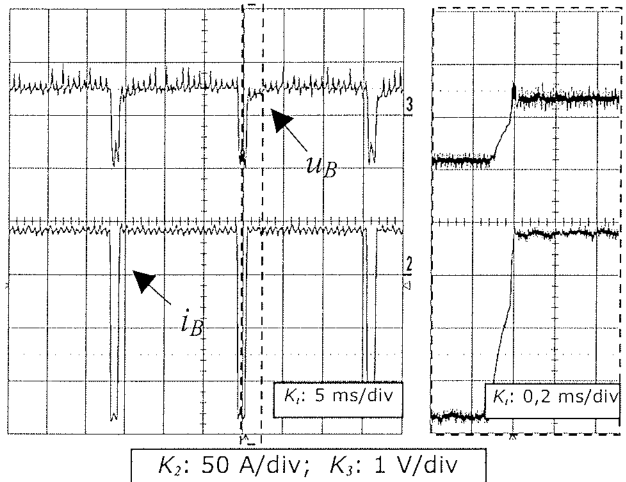
Slika 9: Pricipielno delovanje impulznega tokovnega vira

primarno navitje transformatorja in se z njegovo tokovno prestavo transformira v bremenski tokokrog. S tem sprožimo tokovni impulz skozi breme, ki ga prekinemo s ponovnim kratkostičenjem tokovnega razsmernika (kratkostični režim). Strmino tokovnih impulzov določa komutacija toka iz kratkostičnega tokokroga v primarno navitje, ki je odvisna od stresane induktivnosti transformatorja in parazitne induktivnosti povezav do bremena. Z načrtovano izgradnjo transformatorja /9/ in povezav tokovnega vira z bremenom lahko vpliv omenjenih induktivnosti zmanjšamo, ne moremo pa ga v celoti odpraviti. Komutacija toka v nobenem primeru ne more biti trenutna, zato je v vezju na sliki 8 dodana zaščitna dioda D_Z, preko katere speljemo v času komutacije del toka, ki ga primarno navitje ne more prevzeti. Na ta način omejimo napetost u_M na vrednost napajalne napetosti pretvornika. V nasprotnem primeru bi se na izhodu pretvornika navzdol inducirala prenapetost, ki bi ogrozila tranzistorje razsmernika.

Iz delovanja predlagane topologije je razvidno, da omogoča zgolj generiranje impulzov ene polaritete. Zato smo v eksperimentalnem modelu impulznega tokovnega vira zagotovili bipolarno obliko impulznega toka s protiparalelno vezavo dveh tokovnih virov s slike 8. Modularnost virov omogoča tudi vzporedno obratovanje, pri čemer je skupni tok enak vsoti prispevkov posameznega vira. Amplituda toka posameznega vira v modelu je neodvisno nastavljiva v območju od 0 do 200 A. Časovni parametri toka pa so nastavljivi v območju od 1 ms do 10 s za pozitivni impulz oz. v območju 100 µs do 10 ms za negativni tokovni impulz. Minimalna vrednost časovnih parametrov je pogojena z zmogljivostjo uporabljenega mikrokrmilniškega sistema, s katerim nadzorujemo delovanje modela. Oscilogrami v nadaljevanju prikazujejo karakteristične veličine eksperimentalnega modela impulznega tokovnega vira. Slika 10 kaže primer preprostega tokovnega impulza (I_B) in napetosti u_M na stikalih tokovnega razsmernika. Področje, ki je očrtano s črtkano krivuljo, je na desni strani prikazano povečano. Strmina tokovnega impulza znaša 15 A/µs.



Slika 10:Primer preprostega tokovnega impulza



Slika 11:Potek toka in napetosti v galvanski kopeli

Slika 11 kaže tok i_B in napetost u_B med elektrodama v galvanski kopeli med procesom impulznega nanašanja. Proces je bil napajan z eksperimentalnim modelom tokovnega vira.

9. Rezultati

Analizo impulznega nanašanja bakra v skoznje luknje smo izdelali v sodelovanju s podjetjem za proizvodnjo tiskanih vezij Intec Tiv iz Kranja. V raziskavo smo vključili vzorčne plošče s skoznjimi luknjami različnih premerov in dolžin. V elektrolit smo dodali najnovejšo serijo komercialno dostopnih organskih dodatkov proizvajalca Atotech. Pri ustvarjanju razmer v galvanski kopeli (temperatura, koncentracija dodatkov...) smo upoštevali priporočila proizvajalca. Razmerje amplitud katodnega in anodnega tokovnega impulza smo spreminjali med 1,5 in 3, razmerje časovnih parametrov pa med 5 in 15.

Za primerjavo smo nekatere tipe vzorcev vključili v obstoječo proizvodnjo tiskanih vezij, kjer poteka nanašanje z enosmernim tokom. Po končanem testnem nanašanju smo z razrezom vzorčnih plošč po sredini skoznje luknje pripravili metalurške obruse, primerne za nadaljnjo analizo. Podatki o posameznih vzorcih so zbrani v tabeli 1, od koder so razvidni rezultati nanašanja (debelina nanosa *d* na posameznih mestih luknje - A, B C in faktor *PTH*). Faktor *PTH* (Plate Through Hole) je podan v odstotkih, pove pa nam, kakšna je razsipna moč impulznega nanašanja na sredini skoznje luknje glede na debelino nanosa na njenih robovih. V praksi težimo k *PTH* = 100 %, kar pomeni, da je debelina kovinskega nanosa na sredini skoznje luknje enaka debelini nanosa na njenih robovih.

V raziskavo smo namenoma vključili tudi manj zahtevne vzorce z razmerjem AR = 2,6 in vzorce z AR = 10 oz. 12, ki jih srečamo v kompleksnejših tiskanih vezjih. V primeru vzorca št. 1 z AR = 2,6 se porazdelitev bakra znotraj skoznje luknje ni bistveno razlikovala od tiste, dobljene pri impulznem nanašanju. Prednost impulznega nanašanja pred nanašanjem z enosmernim tokom se je pokazala v primeru zahtevnejših vzorcev, kar je razvidno iz analize vzorcev pod zaporednima št. 2 in 3. Razmerje AR je v tem primeru znašalo 10. Nanašanje bakra v primeru vzorca pod zaporedno številko 2 smo izvršili po klasičnem postopku nanašanja z enosmernim tokom. Debelina nanosa na sredini skoznje

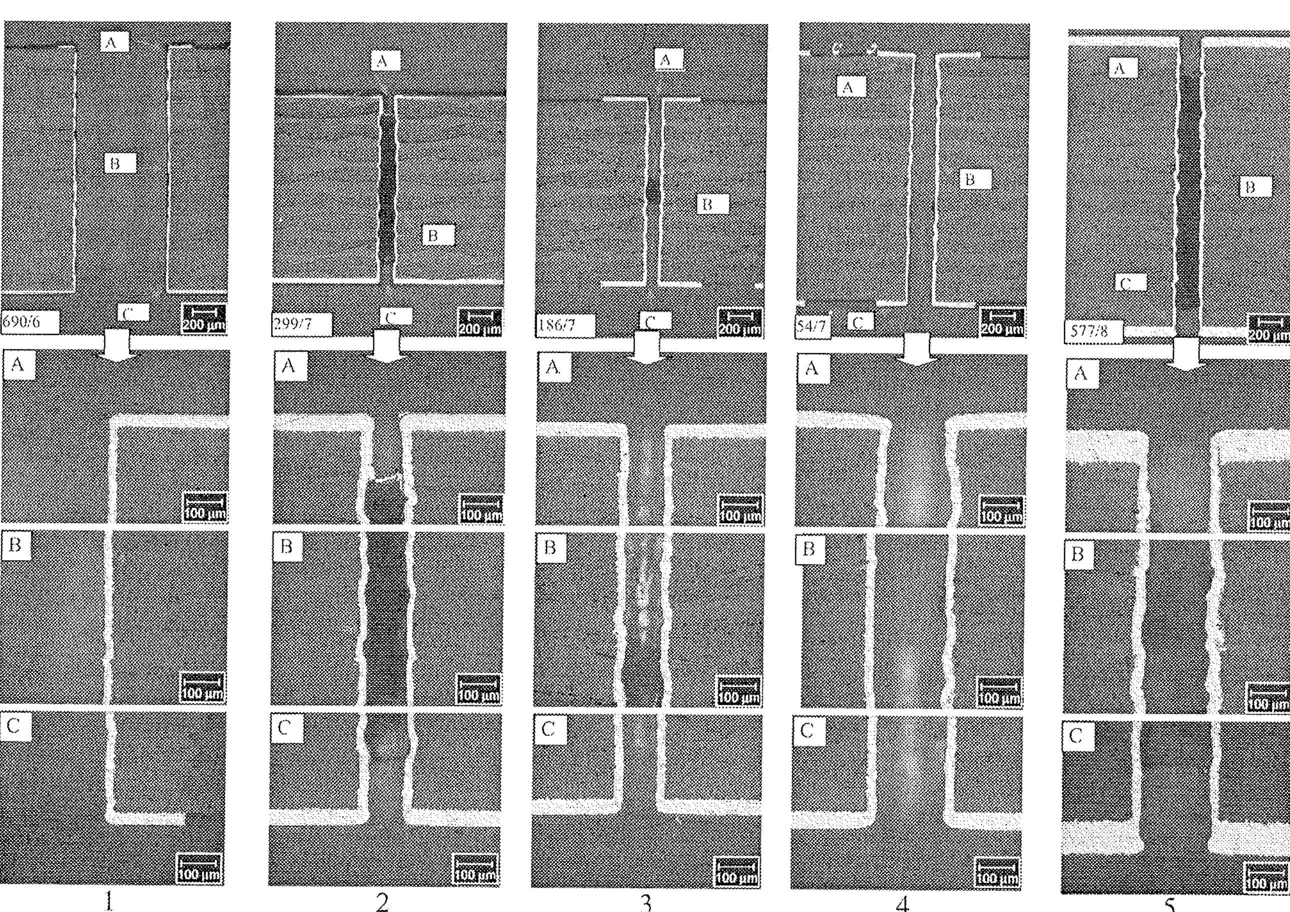
Tabela 1: Rezultati analize

Zap. št.	Oznaka vzorca	2R/D [mm/mm]	AR	Nanašanje	Debelina nanosa na posameznih mestih luknje *d* [µm]			*PTH* [%]
					A	B	C	
1	690/6	0,75/2,0	2,6	Impuzno Enosmerno	22,5	22,2	22,6	**98**
2	229/7	0,15/150	10	Enosmerno	24,2	16,5	25,6	**60**
3	186/7	0,15/150	10	Impulzno	24,4	22,1	24,4	**90**
4	54/7	0,2/2,0	10	Impulzno	21,7	24,1	24,5	**95**
5	577/8	0,2/2,4	12	Impulzno	24,1	28,8	24,1	**120**

luknje je občutno manjša od debeline na njenih robovih, kar priča o neenakomerni tokovni porazdelitvi. Faktor *PTH* je temu ustrezno majhen. Nasprotno lahko zaključimo za vzorec št. 3, pri katerem je nanašanje potekalo z impulznim tokom. Še večji *PTH* smo dosegli v primeru vzorca št. 4, kljub temu, da so bili parametri toka in AR lukenj enaki. Razlog za to pripisujemo večjemu premeru skoznje luknje in zato boljšim hidrodinamičnim pogojem v njej. Vzorec pod zaporedno številko 5 pa je obravnaval luknje z največjim AR. V tem primeru smo na podlagi serije poskusov določili parametre impulznega toka, s katerimi smo dosegli, da je debelina nanosa na sredini skoznje luknje celo večja od debeline nanosa na njenih robovih (*PTH* > 100%). Na podlagi te ugotovitve lahko zaključimo, da posameznim dimenzijam lukenj ustrezajo različni optimalni parametri toka. Zato je, zlasti v primeru tiskanih vezij z dimenzijsko široko paleto skoznjih lukenj, smiselno razdeliti nanašanje bakra v več korakov, znotraj katerih parametri toka ustrezajo posameznim dimenzijam lukenj, začenši z najzahtevnejšimi luknjami. Na metalurških obrusih iz tabele 1 smo izdelali mikroskopske posnetke skoznjih lukenj in njihovih detajlov. Posnetki so zbrani na sliki 12.

Zaključek

V članku smo predstavili novo tehnologijo elektrokemijskega nanašanju bakra, ki se počasi, a vedno bolj uveljavlja v procesu izdelave zahtevnih elektronskih tiskanih vezij. Opisani postopek se od klasičnega nanašanja z enosmernim tokom razlikuje v tem, da je tok impulzne oblike. Ta pristop omogoča v kombinaciji z ustrezno izbranimi parametri impulznega toka določene prednosti, ki se kažejo v izboljšanih mehanskih lastnostih in enakomernejšemu nanosu. Za razumevanje prednosti nanašanja z impulznim tokom smo podali fizikalno sliko masnega transporta snovi in porazdelitve toka v neposredni bližini elektrod. Predlagali smo topologijo impulznega tokovnega vira in izdelali eksperimentalni model. Slednji je služil napajanju galvanske kopeli, ki smo jo za potrebe raziskave impulznega nanašanja opremili z ustrezno sestavo elektrolita. Proces smo napajali s pravokotnimi tokovnimi impulzi s katodno in anodno polarizacijo. Raziskava je obsegala vzorčne plošče tiskanih vezij z različnimi dimenzijami skoznjih lukenj. Dobljene rezultate smo analizirali in primerjali z rezultati, dobljenimi v procesu enosmernega nanašanja. Poleg enakomernejšega nanosa v primeru zahtevnejših tiskanih vezij smo zlasti v primeru manj zahtevnih tiskanih vezjih opazili možnost za skrajšanje procesa nanašanja, ne da bi s tem bistveno vplivali na kakovost izdelkov. Kljub temu, da to ni bilo predmet raziskave, je ta ugotovitev pomembna predvsem s stališča serijske proizvodnje.



Slika 12:Metalografski posnetki vzorčnih obrusov

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SILICON-GLASS ANODIC BONDING

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Key words: anodic bonding, silicon, Pyrex glass, piezoresistive pressure sensor

Abstract: Piezoresistive pressure sensors test structures fabricated on the same silicon wafer were anodic bonded to Pyrex glass wafer and bonding characteristics were analyzed. Surface profiles of both, silicon and Pyrex wafer, were measured before and after bonding process using Taylor-Hobson Talysurf surface profiler. A simple test method for non-destructive in-situ evaluation of both, anodic bonding parameters and bond quality was introduced. Possible causes for thin silicon diaphragms deflection, detected after anodic bonding process, were analyzed and discussed.

Anodno bondiranje silicij - steklo

Kjučne besede: anodno bondiranje, silicij, Pyrex steklo, piezorezistivni senzor tlaka

Izvleček: Testne strukture piezorezistivnega senzorja tlaka so bile anodno zbondirane na rezino Pyrex stekla. Površinski profili obeh rezin pred in po bondiranju so bili posneti s Taylor-Hobson-ovim površinskim profilometrom. Vpeljana je preprosta metoda za nedestruktivno oceno bondirnih parametrov in kvalitete bonda, ki je uporabna tudi med samim tehnološkim procesom. Merilni rezultati na testnih strukturah s tanko silicijevo membrano kažejo ukrivljenost membrane po zaključenem bondirnem procesu. Raziskani so bili možni vzroki za takšno obnašanje testnih struktur.

1. Introduction

Since Wallis and Pomeratz /1/ first introduced anodic or electrostatic bonding in 1969, this technique became one of the basic steps in the fabrication of micro-electro mechanical systems (MEMS). Beside usage of anodic bonding for joining silicon wafer to glass wafer, several related techniques were developed in recent years such as anodic bonding using sputtered glass /2,3/, evaporated glass /4-6/ and spin-on glass /7/. These methods are used for vacuum packaging, hermetic sealing, and encapsulation of MEMS as well as fabrication of reference cavities for pressure and acceleration sensors.

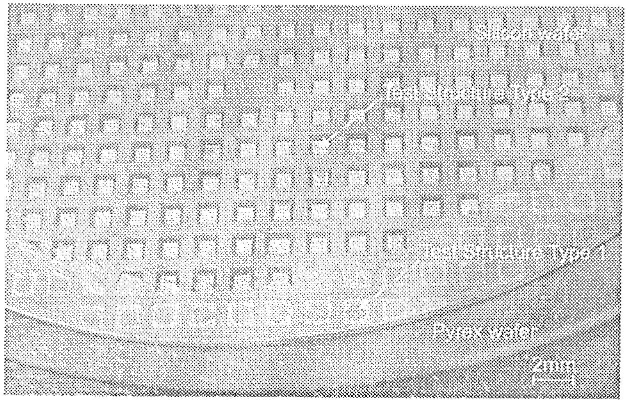

Figure 1: Pyrex wafer bonded to silicon wafer with piezoresistive pressure sensor structures (type2). Pressure sensors structures without diaphragm (type1) are located at the wafers edge

In this paper, 7740 Corning Pyrex glass wafers were anodically bonded to silicon wafers with pressure sensor structure (Fig.1). Among similar commercially available glasses, the main reason to choose 7740 Pyrex glass wafers in our case was their thermal expansion coefficient, well matched with silicon in a wide temperature range. In addition, relative low volume resistivity of 7740 Pyrex glass enables formation of reliable bond already at low applied voltage and temperature that could be essential in many applications. Despite the fact that the optimal solution is to bond silicon wafer directly to glass, silicon oxide as an intermediate layer was introduced in our case to analyze the effects during the bonding of structurized silicon wafers to flat Pyrex glass wafers.

Two different types of test piezoresistive pressure sensor structures fabricated on the same wafer were investigated. The only difference between both is that in the first structure anisotropic etching of diaphragm is not performed. These structures (type1), located in narrow area at the wafers edge (Fig.1), were used as the bond strength test structures based on the blade insertion technique /8-12/ to induce delamination. The second test structures (type2) were used to study fabrication of reference cavity under pressure sensor diaphragm.

2. Bonding mechanism

Bonding mechanism itself is not yet completely understood, but it is generally agreed that bonding is primarily due to the presence of mobile sodium ions in Pyrex glass. At elevated temperatures (yet below the softening point of Pyrex at 821 °C), positive sodium ions are mobile enough for Pyrex to behave like conductor (Fig.2).

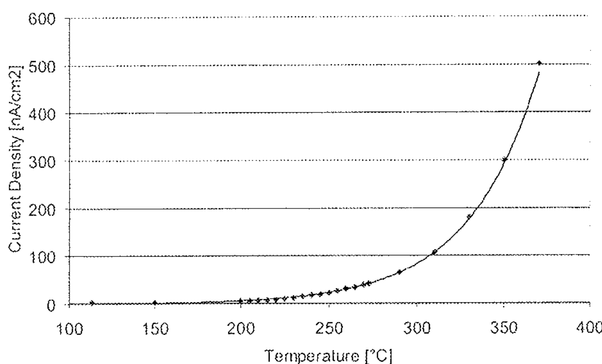

Figure 2: Steady state current density vs. temperature measured through 725μm thick 7740 Corning Pyrex glass wafer between two aluminium electrodes.

When a DC voltage (V) is applied across the silicon-glass sandwich (Fig.3a), sodium ions in glass are transported toward the cathode. The more strongly bounded negative oxygen ions in glass are left in glass adjacent to the silicon surface, forming negative space charge layer. This negative charge layer in glass, together with positive charge in silicon, creates a high electrostatic field across thin air gap between both surfaces. As a consequence, a strong electrostatic pressure pulls both wafers into intimate contact (Fig.3a). This effect can be easily observed during the bonding process on transparent Pyrex glass as the light grey interface between silicon and glass becomes dark grey.

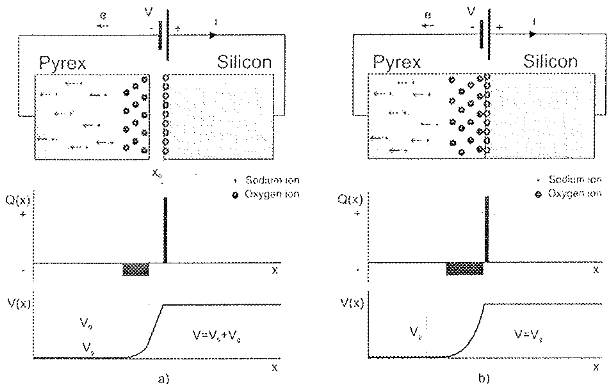

Figure 3: Charge and potential distribution during anodic bonding process: a) before and b) after intimate contact between silicon and Pyrex wafer

Once wafers are in intimate contact (Fig.3b), almost all of the applied voltage (V) is dropped across the narrow space charge layer in glass (V_g), resulting in extremely high field, strong enough to develop transport of oxygen ions to the bonding surface. As a consequence, irreversible Si-O-Si bonds in the interface, joining Pyrex and silicon, are presumed to occur.

3. Experimental

Test structures of silicon pressure sensors, fabricated on 3-inch, CZ grown, <100> crystallographic oriented, 20Ohmcm, n-type, 374μm thick, double side mechanically polished silicon wafers (details reported elsewhere /13/) were bonded to commercially available 4-inch, 725μm thick 7740 Corning Pyrex glass wafers (Figs.1,4). Before bonding, a thin layer of silicon nitride (70nm) - that covers thin silicon oxide (500nm) on the backside of test structure used for mask during diaphragm etching in KOH - was removed in RIE plasma etcher.

During etching of 20μm thick pressure sensor diaphragms, silicon wafer was placed to a holder that protects wafer front-side from aggressive KOH. Because of the holder sealing, a narrow region at the edge of silicon wafer backside was also protected from KOH etching. This is the reason why diaphragms near wafers edge are not etched (Fig.1). This un-etched region was used in our case for the non-destructive anodic bond strength characterization /15, 16, 17/.

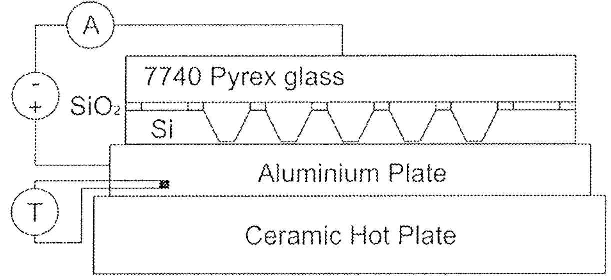

Figure 4: Anodic bonding process setup.

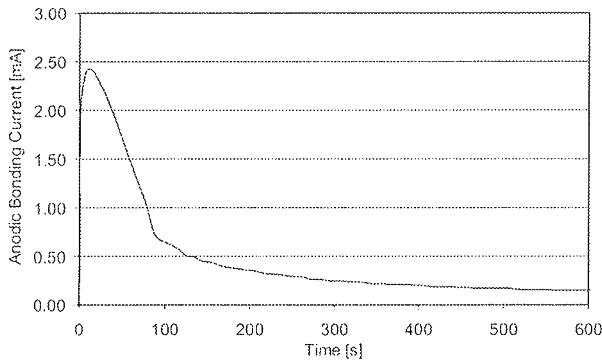

Figure 5: Typical anodic bonding current vs. time.

After surfaces of both wafers were characterized with Taylor-Hobson Talysurf surface profiler, they were cleaned with DI water and dried with nitrogen. As suggested by Resnik et al. /14/, both wafers were put into an intimate contact in cleanroom ambient at room temperature immediately after surface preparation to avoid particles that cause voids. Silicon-Pyrex structure was bonded together by applying high DC voltage (730V) at temperature 370°C in air atmosphere, using Cimarec hot plate with ceramic top (Fig.4).

Bonding temperature was monitored by thermocouple mounted in aluminium plate. Anodic bonding current was measured during bonding process and a typical result is shown in Fig.5. After bonding process, the surface was scanned again in the same areas as before, using the same Talysurf surface profiler setup.

4. Results & discussion

4.1 Structure without diaphragm (type 1)

Surface profiles (Figs. 6-11) of test structures without diaphragm from the wafer edge (Fig.1) were scanned with Talysurf in length of 1.7mm with speed of 0.5mm/s. Profiles were normalized, i.e. rotated till beginning and end of measured curve was in horizontal line.

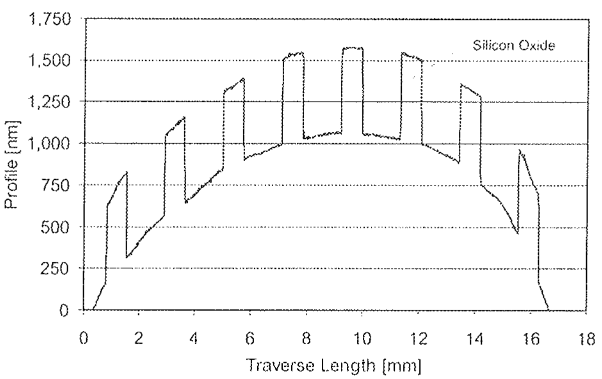

Figure 6: Surface profile of silicon wafer back-side covered with 500nm thin silicon oxide mask scanned at wafer edge before bonding. Diaphragms of pressure sensors at the wafers edge were not etched.

Before anodic bonding, silicon and Pyrex glass wafer were scanned on both sides (Figs.6-9). In Fig.6, surface profile of silicon wafer back-side is shown. Steps in this profile

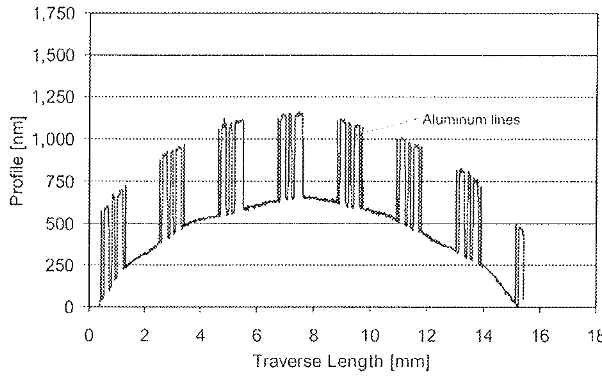

Figure 7: Surface profile of silicon wafer front-side scanned at wafer edge before bonding. Peaks represent 500nm thin aluminium metallization lines of single pressure sensor.

(Fig.6) originate in approx. 500nm thick silicon oxide square diaphragm mask (Fig.1), which is used here as anodic bonding strength test structure. Surface profile of silicon wafer front-side (before bonding) in Fig.7 also contains groups of steps, originating in approx. 500nm thick aluminium metallization lines of pressure sensor. Surface scan of Pyrex glass wafer both sides, front and back, before anodic bonding procedure are presented in Figs.8 and 9, respectively.

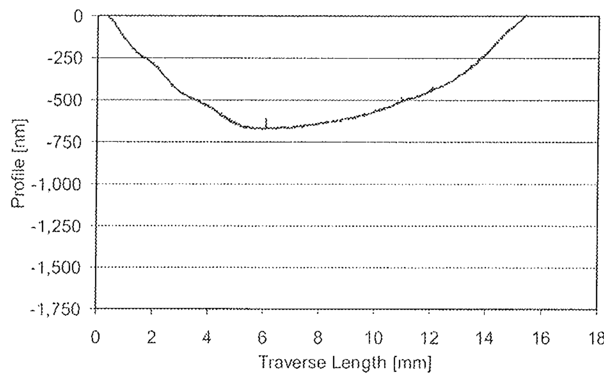

Figure 8: Surface profile of Pyrex glass wafer front-side before bonding.

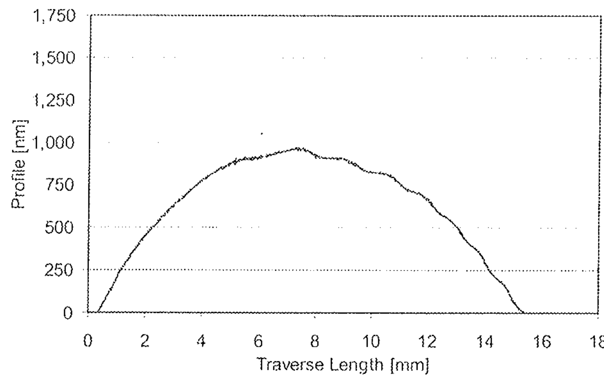

Figure 9: Surface profile of Pyrex glass wafer back-side before bonding.

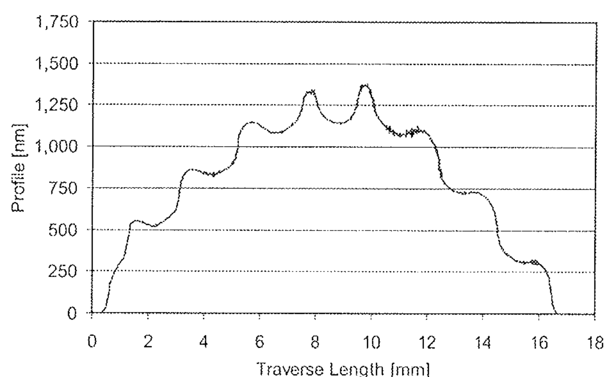

Figure 10: Surface profile of Pyrex glass wafer front-side after bonding.

After silicon and Pyrex wafers were anodically bonded together, with back-sides in contact, surface scans of bonded wafers front-sides were repeated in the same areas as before. Results are presented in Figs.10-11. In both figures, it is clearly seen again the modulated surface profiles with silicon oxide mask as before on Fig.6. Similar amplitudes of modulated surface profile were measured on both surfaces (240µm on Pyrex surface (Fig.10) and 260µm on silicon surface (Fig.11)).

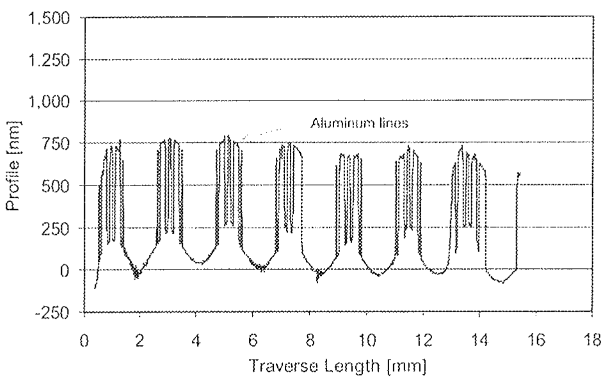

Figure 11: Surface profile of silicon wafer front-side after bonding.

Measured results clearly show that both, silicon and Pyrex wafer bend within test structure with silicon oxide mask. Bonding plane lies at 260nm from the interface between silicon and silicon oxide (Fig.12). From several measuring methods, the strength of the bond between two wafers of different material can be evaluated by technique developed on double cantilever cracking under constant wedging condition (Fig.13) /8-12/. In our case, both parameters, blade thickness (2h) and crack propagation (c) were substituted by thickness of thin silicon oxide mask (500nm) and by distance between mask and bonding point of both wafers at the centre of diaphragm (135µm in Fig.12), respectively.

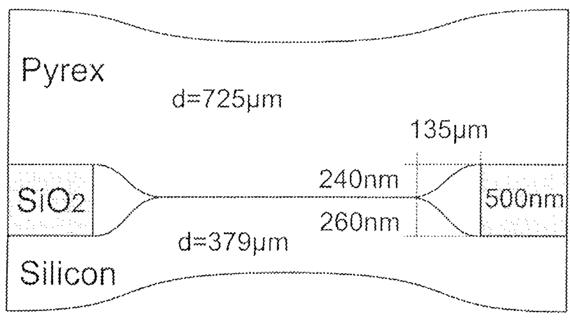

Figure 12: Cross-section of bond test structure with measured parameters

In contrast to silicon-silicon wafer bonding, in silicon-Pyrex anodic bonding, the distance *c* between mask and bond is easily determined by optical microscope. Because bonding within test structure occurs if bond energy is greater

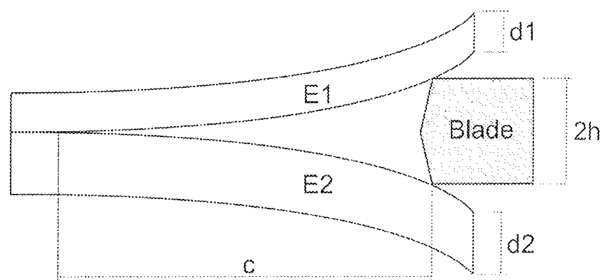

Figure 13: Double cantilever test geometry under wedging condition

than the value determined by blade technique, work of adhesion W_{AB} (per unit area) can be expressed as /12/:

$$W_{AB} \geq \frac{3h^2 E_{Si} d_{Si}^3 E_g d_g^3}{2c^4 (E_{Si} d_{Si}^3 + E_g d_g^3)} \approx 1.65 GPa\mu m \quad (1)$$

where $2h$ is silicon oxide mask thickness, c is distance between mask and bond, d_{Si} is thickness of silicon wafer, d_g is thickness of Pyrex wafer, and E_{Si} and E_g are Young's modulus of silicon and Pyrex, respectively. It is necessary to emphasize that the determined work of adhesion W_{AB} = 1,65GPaµm, represents a quantitative estimation of bond strength between silicon and Pyrex within the test structure. Therefore, the presented approach based on simple test structure can be used for in-situ non-destructive evaluation of both, anodic bonding process parameters and bond quality, as a comparative method on different parts of a single wafer, between wafers in one run and between different runs as well.

4.2 Structure with diaphragm (type 2)

Test structures with 20µm thick diaphragm were characterized in the same manner as structures without diaphragms. Surface profile scans of these structures are presented in Figs.14-17. Despite thin silicon diaphragm, no particular difference was observed in surface profile scan at the centre of silicon wafer front-side before bonding (Fig.14) compared to scan at the edge of silicon wafer shown in Fig.7. On the other hand, silicon wafer back-side profile in wafers centre before bonding (Fig.15) shows distinctive property of anisotropic etched silicon wafer. Etching depth of 354µm was measured in presented scan.

Compared to structures without diaphragms, no significant differences were obtained from surface scans of Pyrex glass either before or after bonding procedure. This is the reason why those scans are not presented here. Much more interesting results were found in surface scan of silicon wafer front-side after bonding procedure (Figs.16, 17). A magnified section of scanned profile in Fig.16 is presented in Fig.17.

After bonding procedure, deflection peaks in value of 500nm were measured on 20µm thin silicon diaphragms

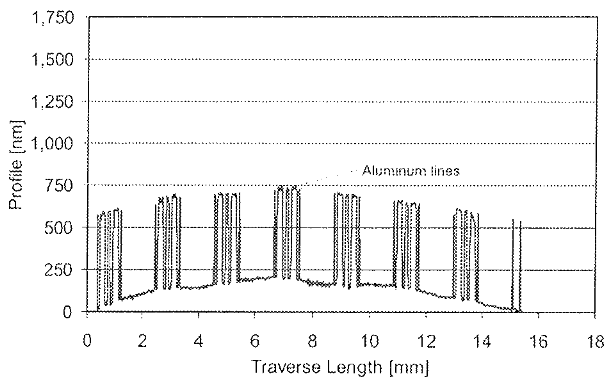

Figure 14: Surface profile of silicon wafer front-side scanned at wafer centre before bonding. Peaks represent 500nm thin aluminium metallization lines of single pressure sensor.

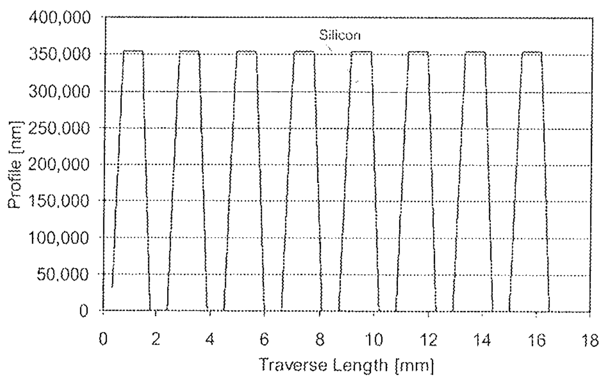

Figure 15: Surface profile of silicon wafer back-side scanned at wafer centre before bonding. Peaks represent 354µm thick anisotropic etched silicon wafer bulk.

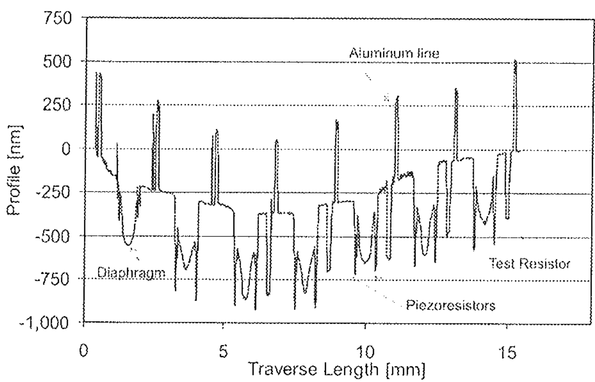

Figure 16: Surface profile of silicon wafer front-side scanned at wafer centre after bonding shows deflection of pressure sensor diaphragm.

(Figs.16, 17). This result was the reason for a further study of its origins. First, electrostatic pressure involved during anodic bonding procedure was investigated as the possible cause for mentioned deflection. In the first moment,

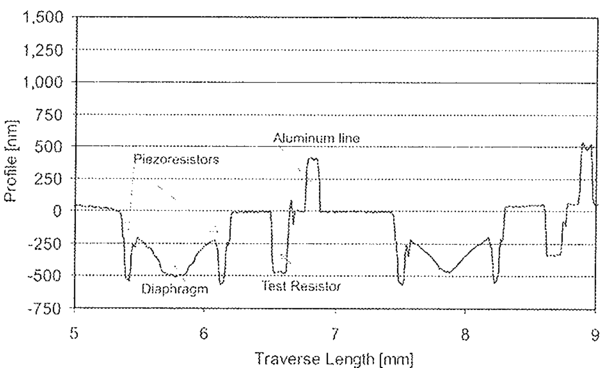

Figure 17: Zoom of surface profile of silicon wafer front-side scanned at wafer centre after bonding shows deflection of pressure sensor diaphragm.

when a high DC voltage is applied to the silicon-Pyrex structure, value of electrostatic pressure p under non-deflected diaphragm can be calculated from the following equation /18/:

$$p = \frac{1}{2}\varepsilon_0\varepsilon_r\frac{V^2}{h^2} \tag{2}$$

where V represents applied DC voltage (assuming neglectable depth of space charge layer in Fig.3), h is the distance between silicon diaphragm and Pyrex glass, ε_0 is permittivity of free space (the ideal vacuum), and ε_r is dielectric constant or relative permittivity of air (1,00059). Due to 354µm thick air gap h between silicon diaphragm and Pyrex glass, a value of 18.8Pa was determined for electrostatic pressure that press diaphragm toward glass during anodic bonding procedure. This amount of electrostatic pressure can easily be neglected.

Next, thermally induced mechanical stress as possible cause for diaphragm deflection was studied. As presented elsewhere /19/, thin silicon diaphragm could deflect at elevated temperature due to the mismatch of thermal expansion coefficients of thin layers that covers the diaphragm, despite the fact that the residual mechanical stress in diaphragm at room temperature could be neglected. However, this deflection disappears when such a structure is cooled down to room temperature. This is the reason that thermally induced mechanical stresses were also rejected as the cause for measured diaphragm deflection.

Finally, due to the fact that anodic bonding procedure was done at normal air pressure (10^5Pa), the main reason for diaphragm deflections, presented in Figs.16 and 17 was found in the well known gas equation:

$$\frac{p_1V_1}{T_1} = \frac{p_2V_2}{T_2} = const. \tag{3}$$

where p_1 represents air pressure, V_1 is reference cavity volume during anodic bonding procedure at elevated temperature T_1, while p_2 means pressure (vacuum) under thin diaphragm in reference cavity with volume V_2 at room tem-

perature T_2. Compared to reference cavity volume V_1, change of cavity volume V_2 due to the deflected diaphragm is neglectable in our case. Because both wafers, silicon and Pyrex, came into intimate (hermetic) contact at air pressure and temperature 370°C immediately after DC voltage was applied, pressure (vacuum) in reference cavity p_2 in value of 6.49kPa was determined from Eq.3. The same diaphragm deflection can be achieved, if pressure of 93,51kPa is applied on the diaphragm from above.

Using our laboratory computer simulator for thin silicon diaphragm deflections /20/, pressure above 500nm deflected thin silicon diaphragm was determined. Simulations for piezoresistive pressure sensor structure deflection show that such a diaphragm deflects for 500nm (maximal deflection in centre of diaphragm) in case when pressure of 77.88kPa is applied to its top surface.

Simulated result (77.88kPa) does not match with the result obtained from gas equation (93.51kPa). The reason for that could be oxygen generation during anodic bonding procedure, an assumption widely accepted in the literature /21,22/.

5. Conclusion

Test structures, based on piezoresistive pressure sensors were anodic bonded to Pyrex glass and analyzed. Surface profiles of both, silicon and Pyrex wafer, were measured before and after bonding process, using Taylor-Hobson Talysurf surface profiler. A simple test method for non-destructive in-situ evaluation of both, anodic bonding parameters and bond quality, was introduced. Anodic bond strength between 7740 Corning Pyrex glass wafer and silicon wafer was determined. Measured results on test structure without diaphragm unambiguously show bending of both, silicon and Pyrex wafer. Bond strength within test structures was evaluated by a new technique developed on double cantilever cracking under constant wedging condition. The proposed approach is appropriate for a simple, efficient quality control in anodic bonding process. Measured results on test structures with thin silicon diaphragm show diaphragms deflection after the anodic bonding process was performed. Possible causes for such behaviour were analyzed and discussed.

Acknowledgements

This work was supported by Ministry of Science, Education and Sport of Republic of Slovenia.

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PREDSTAVLJAMO PODJETJE Z NASLOVNICE
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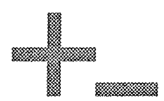
ISKRAEMECO 

Iskraemeco, 4000 Kranj, Savska loka 4, Slovenija
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V Iskraemecu uspešno združujemo izkušnje z inovacijami in novimi tehnologijami pri zadovoljevanju različnih potreb na področju merjenja in obračuna porabe električne energije. Po prodaji števcev se uvrščamo med največje na svetu, izdelke z našo blagovno znamko poznajo danes že v skoraj sto državah na vseh petih kontinentih. Iskraemeco je danes na trgu sistemski ponudnik opreme, svojo ponudbo pa razširjamo tudi na storitve s področja merjenja in obračuna energije. Odpiranje trga električne energije ponuja vrsto možnosti za nove izdelke in rešitve, ki so velik izziv za naše strokovnjake danes in tudi v prihodnje.

Začetek družbe Iskraemeco, d.d. sega v leto 1945, proizvodnja enofaznih elektromehanskih števcev teče v Kranju že od leta 1946. Mehansko tehnologijo smo nadgradili z elektronsko, leta 1975 smo začeli proizvajati elektronske precizijske števce. Do današnjega dne smo kupcem dobavili več kot 40 milijonov izdelkov, od tega skoraj 2 milijona v elektronski izvedbi. Leta 1986 smo postavili prvi sistem za merjenje in obračun električne energije. Ponosni smo na dejstvo, da so vsi izdelki iz našega programa plod lastnega znanja, zasnovani na številnih lastnih patentih.

Že po prvem desetletju delovanja smo svoje izdelke začeli prodajati na tuje, najprej le v nekaj držav, z leti pa po vsem svetu. Poleg izvoza končnih izdelkov smo se uspešno uveljavili tudi s prenosi tehnologije in s prodajo licence za proizvodnjo števcev na tujih trgih. Zadnjih deset let sledimo težnji po globalizaciji tako, da se uporabnikom na različnih trgih približujemo z ustanavljanjem lastnih podjetij in podjetij v mešani lasti.

Podjetji, ki ju vodita člana MIDEM med dobitniki priznanj Slovenske gazele 2004
Companies directed by two MIDEM members won Slovenska gazela 2004 award

KDO SO GAZELE?

Znameniti ameriški raziskovalec David Birch je pri raziskovanju, kako se ustvarjajo nova delovna mesta v ZDA, prišel do zanimivih ugotovitev, da kar dve tretjini rasti zaposlenosti prispevajo podjetja z manj kot dvajsetimi zaposlenimi. Pozneje je analiziral življenjski cikel podjetij in jih razdelil na tri kategorije: **miši, gazele** in **slone**.

Gazele so dinamična podjetja, ki hitro rastejo, se bliskovito razvijajo, intenzivno zaposlujejo in vedno držijo korak prednosti pred konkurenco.

Cilj dinamičnih podjetij ni preživeti, temveč uspeti. Največkrat so to majhna družinska podjetja, ki požrtvovalno gradijo in previdno izbirajo prve sodelavce, dokler ne začnejo bliskovito rasti. Takrat je pomembno predvsem dvoje: zagotavljati sredstva za bliskovito rast in enako hitro najti prave ljudi za nove naloge v podjetju.

Sposobnost gospodarstva, da raste in zaposluje, je močno odvisna od sposobnosti gospodarstva, da ustvarja gazele.

Slovenskih 500 najhitreje rastočih podjetij v generaciji 2003 je od leta 1998 do 2002 ustvarilo 7.940 novih delovnih mest. Leta 1998 je imela povprečna gazela 24 zaposlenih, leta 2002 pa že 40.

Prodaja se je v istem času v povprečju povečala za 4-krat, izvoz pa je v štirih letih zrasel kar za 5,5-krat.

Povprečno hitro rastoče podjetje je tako v letu 2002 prodalo za 1,5 milijarde tolarjev izdelkov ali storitev. Tretjino od tega v tujino. In na koncu leta je povprečni gazeli ostalo 60 milijonov tolarjev dobička.

Kipci zlata, srebrna in bronasta gazela 2004 podeljeni

6. oktobra smo v Cankarjevem domu razglasili letošnje tri zmagovalce Slovenske gazele 2004. Bronasta gazela je postalo kranjsko podjetje Don Don. Srebrni kipec je šel v roke ljubljanski hitro rastoči družbi Bioiks. Najbolj prestižni gospodarski kipec - zlato gazelo 2004 - pa je v žužemberški Keko Varicon odnesel Zoran Živić.

Keko Varicon

zlata gazela 2004

Podjetje Keko, v katerem sta delala Zoran in Angela Živić, je bilo leta 1995 tik pred zlomom. Zaposleni v Keku so zaradi izgube jugoslovanskih in ruskih trgov čakali le še na konec. Zoranu Živiću, ki je delal v razvojnem oddelku, pa je tik pred stečajem, uspelo pritegniti takratni Tehnološki sklad, ki je verjel v prihodnost Živićevih patentov. Sklad je obljubil, da bo v podjetje vložil 500 tisoč takratnih nemških mark. Keku pa je postavil pogoj, da ustanovi hčerinsko podjetje in vanj prenese nove perspektivne programe. Večinoma so bili ti takrat šele na papirju.

Tik pred stečajem je Keko res ustanovil podjetje Keko Varicom, Živić pa je prispeval svoje patente. Agonija družbe se je za zakonca Živić, ki sta prevzela vodenje na novo nastalega podjetja, šele pravzaprav začenjala. Prvi udarec je bil stečaj Keka, ki je bil ob ustanovitvi 45-odstotni lastnik podjetja. Drugi pa to, da je Tehnološki sklad (55-odstotni lastnik) Keku Vriconu odobril le 120 tisoč mark nepovratnih sredstev, razliko pa je nakazal v obliki kratkoročnega posojila. »Pa še od teh 120 tisoč mark smo jih sto morali takoj nakazati dobaviteljem, ker nam niso hoteli dobavljati materiala, če ne poravnamo dolgov Keka, ki je medtem šel v stečaj,« opisuje začetke Zoran Živić, direktor in solastnik Keka Varicona.

Kljub temu je podjetje leta 1995 začelo poslovati; imeli so 40 zaposlenih, program standardnih keramičnih kondenzatorjev, ki je delal izgubo, 20 tisoč mark in bili so brez pravih poslovnih prostorov. »Padale so stave, koliko mesecev, celo tednov bo podjetje sploh preživelo,« se spominja Živić. Rešili so jih, pravi, patenti za nove izdelke in trma, da se bodo že pretolkli in uspeli.

Zdaj je položaj podjetja, ki izdeluje najrazličnejše keramične zaščitne sestavne dele predvsem za avtomobilsko elektroniko, povsem drugačen. V družbi dela 150 ljudi. Odkupili in obnovili so proizvodne prostore in kupili precej nove proizvodne opreme. Vodilni pa se ubadajo predvsem s tem, kako izdelati vse, kar jim trg naroči. V osmih letih so nanj spravili 25 novih izdelkov. »Naše zaščitne keramične komponente se vozijo v mercedesu S in A pa v beemveju. Zelo ponosni smo tudi na to, da smo kraljevski dobavitelj Fiata kjer smo izrinili vse svetovne tekmece, saj italijanski avtomobilski proizvajalec vse zaščitne sestavne dele za elektroniko naroča pri nas.« Polovica izdelkov, ki jih izdelujejo, je unikatna. Vse, kar naredijo, izvozijo. Njihova konkurenčna prednost ni nizka cena, temveč kakovost in tudi do štirikrat krajši dobavni rok kot pri tekmecih. Pa seveda razvoj, patenti in s tem novi izdelki.

Tudi lastniška sestava podjetja se je pred leti ustalila. Živić je svoj vložek, šest patentov, štirje so patentirani v ZDA, dva pa v Evropi, leta 1998 spremenil v lastniški vložek in postal 29,5-odstotni lastnik podjetja, ki ga vodi. Preostali delež pa je iz rok Tehnološkega sklada najprej romal na SRD, nato pa je leta 2000 v podjetje vstopil sklad Horizonte venture.

Bioiks

srebrna gazela 2004

Čeprav ima Bioiks več kot 300 zaposlenih in je skoraj v središču Ljubljane, ga pozna presenetljivo malo ljudi. »Nimamo svoje spletne strani in tudi v promocijo čisto nič ne vlagamo.« pojasnjuje Rudi Ročak, direktor in solastnik podjetja. Kot menijo, promocije ne potrebujejo, saj imajo le dva strateška kupca - dve vodilni italijanski multinacionalki. Prva je Gambrodasco, ki ima pri dializnih aparatih 24-odstotni svetovni delež, druga pa Dideco, ki v kardiologiji obvladuje kar polovico svetovnega trga.

Razlog za njihovo rast je na prvi pogled preprost - Bioiks je rasel, ker sta rasli obe multinacionalki. Vendar pa je bila tekma za ta položaj predvsem z neposrednimi konkurenti zelo ostra. »Ena od multinacionalk je pred leti imela več kot deset dobaviteljev, danes sta od njih ostala le še dva. Posle preostalim smo prevzeli mi,« pojasnjuje direktor Ročak. Za uspeh so bili poleg cene pomembni kakovost, učinkovito upravljanje podjetja, prilagodljivost, izpolnjevanje rokov v dogovorjenem času, učenje na napakah in nenehen trening. Rast pa bo v prihodnje zaradi konkurence z vzhoda, predvsem Čehov, odvisna tudi od cenovne konkurenčnosti in od tega, kako hitro se bo povečevala produktivnost podjetja. »Proizvodnjo bomo zato še bolj avtomatizirali in opremili z najsodobnejšimi roboti, poleg tega se bomo še bolj usmerili v inoviranje,« razlaga Ročak. Sicer pa ima Bioiks še dve hčerinski družbi. Ena je Bioprod z blagovno znamko Pharmagena, ki bo po direktorjevih napovedih v prihodnjih letih še močno rasla. Drugo hčerinsko podjetje, Mikroiks, pa se ukvarja z distribucijo elektronskih komponent v Sloveniji in z inženiringom. Z njim je Rudi Ročak tudi začel podjetniško kariero.

Dr.Rudolf Ročak
ŠESTDESETLETNIK

Naš nekdanji dolgoletni predsednik in gonilna sila društva MIDEM, dr.Rudolf Ročak, praznuje visok jubilej

ČESTITAMO!!

Urednik časopisa me je zaprosil, da mu dam podatke za članek ob moji šestdesetletnici. Malo zaradi poslovne zasedenosti, malo zaradi lenobe, pa tudi že prihajajoče se pozabljivosti (čeprav sem na stvari, ki bi jih moral kdaj narediti, vedno rad pozabljal; le za pretekle dogodke sem imel vedno spomin, kot beli slon, tako vsaj pravijo). Namesto, da dam podatke, sem se odločil, da kar sam napišem nekaj o sebi. Ne bom vas moril z biografskimi podatki, niti s podatki poslovnega življenjepisa. Odločil sem se, da napišem nekaj o sebi v tesni zvezi z društvom MIDEM in njegovim časopisom Informacije.

Povezava med mano in društvenim življenjem se je začela daljnega leta 1978, ko sem se vrnil z dela v tujini, poln ambicij, da nekaj svojega, tam pridobljenega znanja, prenesem v takratno jugoslovansko okolje. V Zagrebu sem se vključil v organizacijo konference o mikroelektroniki, ki jo je organizirala sekcija za elektronske sestavne dele pri zvezi ETAN. To sicer ni bil moj prvi stik s kolegi te sekcije, saj sem pred tem enkrat obiskal to konferenco v Ljubljani, kot italijanski gost. Takratni podpredsednik sekcije magister Milan Slokan me je hitro uspel pridobiti za »hrvaškega poverjenika«, oziroma me potem predlagal za podpredsednika sekcije. Ko je po upokojitvi profesorja Janeza Dobejca sam postal predsednik, me je nekoč poslal v Muenchen, da ocenim in preverim takrat porajajočo se idejo, da jugoslovanske konference bolj internacionaliziramo. Po posvetovanju s kolegi iz mednarodnih krogov sem predlagal, da jugoslovanske konference postanejo predvsem konference z mikroelektronsko industrijsko usmeritvijo. Ta usmeritev se je vse do propada jugoslovanske mikroelektronike, ki se je začela v Sloveniji in nadaljevala potem še v Srbiji in na Hrvaškem pokazala kot dober »pogodek«. Ko sem se leta 1982 odločil, da v Ljubljani poskusim, pod vodstvom Ive Baniča, pomagati zagnati proizvodnjo takrat nastajajoče tovarne za mikroelektroniko v okviru Iskre, so me kolegi iz Jugoslavije, spet na predlog Milana Slokana izbrali za predsednika sekcije. Milan me je sicer predlagal še kot »Hrvata«, ki naj prevzame štafeto. Kolegi iz Srbije so se sicer kasneje jezili, ko so ugotovili, da sem prešel med Slovence, vendar so me kljub temu sprejeli, posebej Vlado Pantović iz Beograda, ki je nekako brzdal ambiciozne »mladiče iz Niša«. Ratko Krčmar iz Banja Luke in Petar Biljanović sta s svojo podporo omogočala izredno plodno društveno delovanje, ki je hitro preraslo v tak nivo, da se je začelo razmišljati o ustanovitvi samostojnega strokovnega društva. Ker se ni moglo takrat ustanavljati jugoslovanskih društev, ampak samo zveze republiških društev, kar pa nismo želeli, smo pristopili k majhnemu triku. Odločili smo se, da ob podpori Elektrotehniške zveze Slovenije (predvsem Drage Chvatala) ustanoviti strokovno društvo v najmanjši možni upravni enoti - občini Šiška v Ljubljani. Nekaterim se jo to zdelo čudno, vendar s statutom, ki je predvideval tudi regionalno organiziranost svojih članov (oblast pa ni mogla prepovedati ustavno pravico vseh državljanov Jugoslavije, da se včlanijo tudi v občinsko društvo) smo pridobili vse pomembne strokovne kolege iz cele Jugoslavije. Devetindvajsetega januarja 1986 leta smo imeli prvi občni zbor novega društva za mikroelektroniko, elektronske sestavne dele in materiale, MIDEM, ki je postal tudi kolektivni član EZS in zveze ETAN, sam pa predsednik društva. Ob razpadu Jugoslavije smo društvo nemudoma internacionalizirali. V Portorožu je naš češki kolega Radomir Kužel postal prvi član iz tujine. Na ta način smo se želeli prilagoditi novim

zgodovinskim dogodkom. Na žalost nam pa to ni ravno zelo dobro uspelo.

Še nekaj besed o razvoju strokovnega časopisa. Alojz Keber, ob pomoči Pavleta Tepine je prevzel urejevanje novega časopisa Informacije Midem, čez nekaj časa je njegovo delo nadaljeval novinar Janko Colnar, tiskanje pa je prevzel Biro M, ki ga tiska še danes. Nekaj po zaslugi moje takratne funkcije slovenskega koordianatorja za elektroniko, veliko pa s prevzemom urejevanja časopisa s strani kolege in prijatelja Iztoka Šorlija, smo časopis uspeli pripeljati do najvišjega nivoja med slovenskimi znanstvenimi revijami. Od zajemanja podatkov iz časopisa s strani INSPEC, smo z vztrajnostjo in trmoglavostjo, uspeli prodreti do zajemanja podatkov s strani ISI, kar je doslej največje priznanje časopisu. Zelo sem vesel, da po vseh teh letih časopis še vedno ima zavidljiv nivo. Upam, da ga to moje današnje pisanje ne bo kvarilo. Spomin na lasten prispevek v kreiranju društva MIDEM in profiliranju časopisa mi je eden od najlepših in najdražjih spominov.

Vsem kolegom, ki berejo ta časopis in so uspeli imeti potrpljenje priti s čitanjem do konca prispevka, želim lepe božične in novoletne praznike, pa še dobre želje za skorajšnjo dvajsetletnico društva.

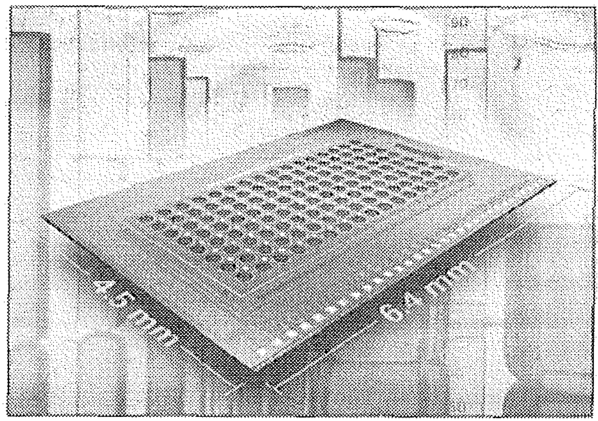
Ob koncu gospodnjega leta dva tisoč četrtega

Rudi Ročak

NOVICE
NEWS

German partners plan biochip future

THE Fraunhofer Institute for Silicon Technology (ISIT), Siemens and Infineon announced proposed development of electronic biochip technology along with their nomination for the German Federal President's Deutscher Zukunftspreis technology and innovation award.



The biochip co-operation was initiated by the federal government sponsored SIBANAT project. The three partners have produced an electronic DMA biochip that can be used to detect various carcinogenic viruses.

Siemens wants to implement a low cost "quicklab system" based on existing smart card production technologies. The system is intended for use in doctor surgeries, at the point of care and in clinical laboratories. The smart card would be inserted into a laptop-sized terminal for a fully automatic analysis.

Infineon is working on incorporating the electronic DNA biochips in desktop devices for diagnostics. This will enable complex DNA analyses to be carried out in medical practices, hospitals and other medical institutions faster and more cost-effectively than in the past.

Working together with its spin-off company eBiochip Systems, Fraunhofer ISIT is expanding the platform for biochemical measurement with low-density electrical biochips and low-cost portable devices. Typical applications will include monitoring of foodstuffs or identification of pathogens in the environment.

The Deutscher Zukunftspreis award will be made November 11, 2004. The first such award was made in 1997.

Progress on 65nm process

INTEL has built fully functional 70Mbit SRAM memory chips with more than 0.5bn transistors on a die area of 110mm^2 using a 65nm process. The transistor gates measure 35nm, 30% smaller than the lengths on the company's previous 90nm technology. Each SRAM memory cell has six transistors packed into an area of $0.57 \mu m^2$.

The process enhances the strained silicon first deployed at Intel's 90nm node. The second generation strain increases performance by 10-15% without increasing leakage. Conversely, leakage can be cut by four times at constant performance compared with 90nm transistors.

The reduced gate length and 1.2nm gate oxide thickness combine to provide improved performance and reduced gate capacitance. The reduced gate capacitance ultimately lowers a chip's active power. The new process also integrates eight copper interconnect layers and a "low-I<" dielectric. Intel has also implemented "sleep transistors" that shut off large SRAM blocks when they are not being used.

The 65nm semiconductor devices were manufactured at Intel's 300mm development fab (DID) in Hillsboro, Oregon, where the process was developed. More information on the 65nm logic will be presented at the International Electron Devices Meeting in December 2004.

SiGen takes uniaxial strain across wafer

SILICON GENESIS (SiGen) has successfully developed wafer-level uniaxial strained substrates. Until now, only local transistor-level uniaxial strain has been available, the company says. SiGen has called its wafer-level technique "Next-Generation Strain" (NGS).

Uniaxial strain avoids mobility degradation and the high defect levels associated with current silicon-germanium (SiGe) based biaxially strained silicon or strained silicon on insulator (s-SOI), says SiGen. Several chip manufacturers, including Intel and Texas Instruments, have demonstrated benefits of uniaxial strain at the local, transistor level. Intel pioneered the use of uniaxial strain-enhanced transistor technology and is already using it in its 90nm process. Francois J Henley, SiGen president and CEO, comments: "This new material offers the potential for significant mobility enhancements over SiGe-based biaxial strain wafer technologies and is compatible with local straining approaches since the strains are additive. It also features very low defect levels due to SiGen's use of its proprietary low-temperature processing technology. It can be directly integrat-

ed on silicon as an "epi-like' strained bulk wafer or on an insulator as a strained silicon-on-insulator wafer (s-SOI)."

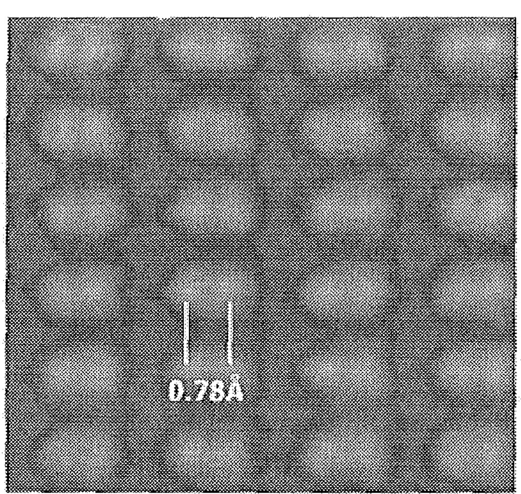
Dr Scott Thompson, Florida University associate professor and former Intel Fellow, adds: "Uniaxial strain is now being recognized as the preferred strain type for deep-submicron device applications, and its local variant has displaced global biaxial strain as the mobility enhancer of choice. Biaxial strain has been plagued with process integration issues such as high defect levels and germanium inter-diffusion, but more importantly is much less efficient in boosting PMOS transistor performance. Local uniaxial strain processes are already enhancing 90nm performance at many companies. The availability of a global uniaxially strained substrate can work with these existing approaches to substantially improve total transistor performance and has scaling advantages over local strain at the 45nm node and beyond."

Sub-Angstrom silicon imaging

OAK RIDGE US national laboratory scientists have used electron microscope aberration correction technology from Nion to directly image silicon at sub-Angstrom resolutions (Science, September 17, 2004). The transmission electron microscope (TEM) was able to image silicon crystal in the <112> orientation, showing the dumbbell spacing of Si column pairs of 0.78Å (78pm) using a 300 kV VG Microscopes HB603U scanning TEM (STEM).

Analysis of the power spectrum shows the presence of information down to 0.61Å. The imaging mode used was annular dark-field (ADF). Before correction, the optimum ADF resolution limit on the microscope used was 0.13nm. "We expect light columns to be visible in the presence of adjacent heavy columns and individual dopant or impurity atoms to be detectable within materials, at defects and interfaces, and on their surfaces," the authors write.

Although the wavelength of the electrons used in TEM imaging can be of the order of a few picometres (0.001 nm), spherical aberration limits resolution to about 0.15nm.



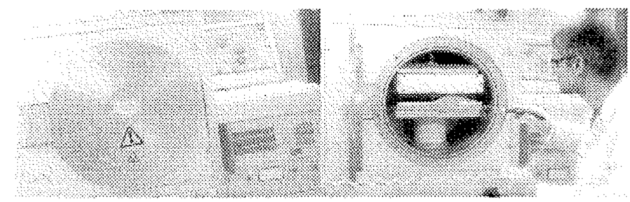
Nion's technology uses arrangements of magnetic lenses designed by computer to provide aberration correction.

The company works with many research organisations. In Bulletin 445, August 12, 2002, we reported work with scientists at IBM imaging gold atoms on a carbon substrate.

The US Department of Energy's Basic Energy Sciences division funded the development.

New plasma texturing process for solar cells

IMEC has developed a new plasma texturing technique for silicon solar cells, which has the potential to reduce the environmental impact of the production process while improving conversion efficiency. This technique can be applied to both standard multi-crystalline solar cells and thin-film silicon solar cells.



The new *solar cell plasma etching* system, *installed in IMECs solar cell pilot line.*

To produce efficient solar cells, it is essential to structure the starting wafer so that its front surface becomes rough. This surface texture ensures that reflection is lowered and that the light is obliquely coupled into the solar cell, resulting in an increased short circuit current. The traditional alkaline anisotropic etching technique for single crystalline silicon is not suitable for multicrystalline silicon, the standard low-cost material used in today's photovoltaic industry. An elegant solution consists in applying an isotropic texturing step in an acidic solution. This process, developed at IMEC and successfully transferred to its spin-off Photovoltech, sets the standard for texturing processes in the photovoltaic industry.

As the photovoltaic industry continues at a steady 30% growth rate, it is essential to develop processes that are environmentally sustainable in solar-cell mass production, and that can meet the new, more stringent environmental regulation that is bound to come into force in the future. This implies reducing water consumption and production of chemical waste. Moreover, the new processes should be applicable to very thin (200 μm or less) wafers with a high yield and should lead to higher solar cell performance.

All these aspects have led IMEC to start a research activity on plasma texturing. In collaboration with SECON, an Austrian company, a new system has been developed for solar-cell etching and texturing processes. The system is

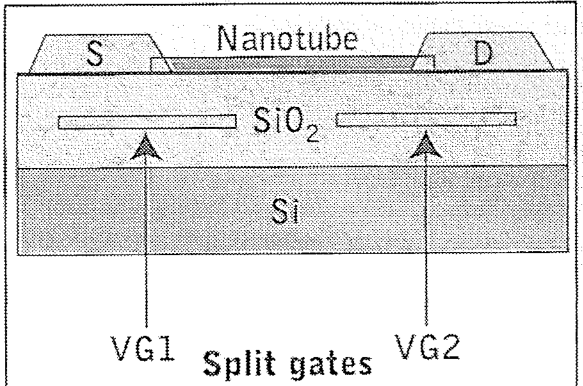
based on plasma generation using microwave antennas encased in ceramic rods, and on a fluorine-containing plasma chemistry. Previous attempts of other research groups to use a plasma process for texturing have shown limited success. Most of these attempts were based on reactive ion etching, a process involving heavy ion bombardment of the surface. This surface damage subsequently needs to be removed by a wet chemical etch, precisely the type of process we seek to replace. In IMECs process, the type of plasma generation combined with the selected chemistry ensures that no structural damage is created. Moreover, the process is mask-less and therefore much simpler and more straightforward than processes based on a prepatterned mask. Excellent and uniform results have been obtained at cell level, such as 15.6% efficient solar cells made on 10 x 10 cm^2 standard multicrystalline material. Those cells performed better in fact than the reference cells for which acidic isotexturing was used. Apart from the possible application as an alternative replacement in existing industrial solar-cell processes, this new plasma texturing technique is of particular interest for thin-film silicon solar cells that are expected to eventually replace bulk silicon solar cells. Indeed, IMEC's technique ensures that only a very small amount of silicon (the most costly component of a thin-film cell) is removed during the texturing step.

These results were presentee at the 19* European Photovoltaic Conference, which took place in Paris, from 7 to I I June 2004.

Electrostatics set up for nanotube p-n junction

GE Global Research Centre scientists have developed a carbon nanotube p-n junction diode based on electrostatic doping (Applied Physics Letters, JulyS, 2004). The single-wall tube is put between source-drain contacts on a silicon substrate. Underneath the tube in a silicon dioxide layer are two gates. These provide electrostatic fields that create different doping conditions (charge carriers) in the tube.

The researchers report forward conduction and reverse blocking characteristics - diode rectification behaviour. For low bias conditions, the characteristics follow closely the ideal diode equation with an ideality factor close to one.



Schematic diagram of carbon nanotube diode

Intel potrjuje Moorov zakon - Intel je dosegel pomemben mejnik v tehnologiji proizvodnje naslednje generacije mikroprocesorjev.

Z uporabo najnaprednejše 65-nanometrske (nm) tehnologije proizvodnje je podjetje proizvedlo 70-megabitne delujoče statične pomnilnike SRAM, ki gostijo več kot pol milijarde tranzistorjev. Ta dosežek je v skladu z Intelovim ciljem razvoja nove tehnologije proizvodnje vsaki dve leti, kar omogoča nadaljnje sledenje Moorovem zakonu.

Tranzistorji proizvedeni z novo 65-nm tehnologijo (nanometer je milijardni delec metra) imajo vrata (stikala, ki vklapljajo in izklapljajo tranzistor) velikosti 35 nm, in so torej za približno 30 odstotkov manjša kot vrata v starejši, 90-nm tehnologiji. Nova tehnologija proizvodnje omogoča povečanje števila tranzistorjev na procesorju, kar daje Intelu možnost za razvoj in proizvodnjo procesorjev z več jedri ter dodajanje novih zmogljivosti v bodoče izdelke, vključno z virtualizacijo in varnostnimi zmožnostmi. Intelova nova 65-nm tehnologija proizvodnje vključuje tudi več edinstvenih novosti za zmanjševanje porabe energije in izboljšanje delovanja. (aNET)