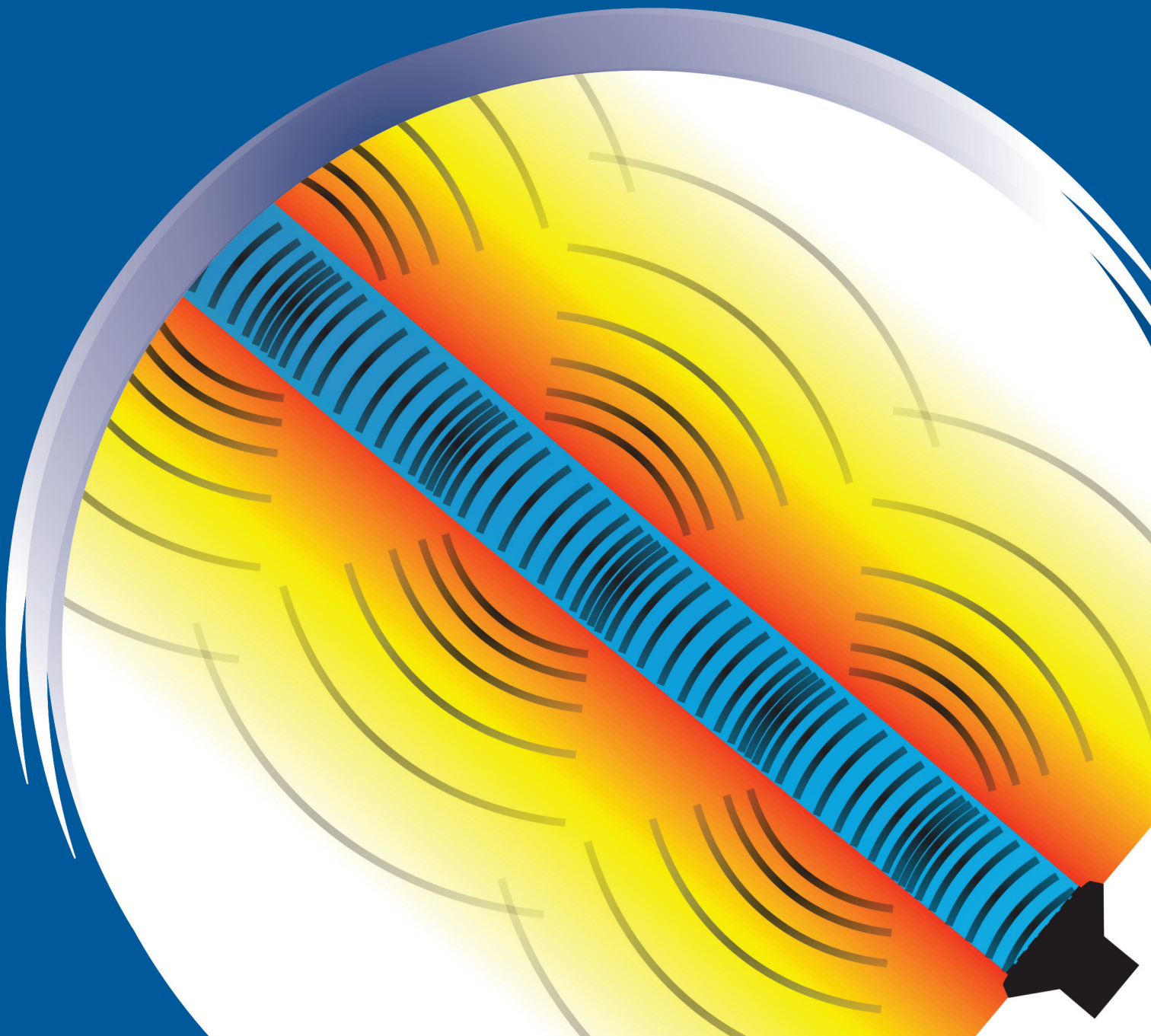
ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 49, No. 1(2019), March 2019

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 49, številka 1(2019), Marec 2019



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *1-2019*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 49, NO. 1(169), LJUBLJANA, MARCH 2019 | LETNIK 49, NO. 1(169), LJUBLJANA, MAREC 2019

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Headquarters | Naslov uredništva
Uredništvo Informacije MIDEM
MIDEM pri MIKROIKS
Stegne 11, 1521 Ljubljana, Slovenia
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Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 49, No. 1(2019)

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Original scientific paper
https://doi.org/10.33180/InfMIDEM2019.101

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 1(2019), 3 – 9

Prototyping of a High Frequency Phased Array Ultrasound Transducer on a Piezoelectric Thick Film

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Abstract: A process including virtual prototyping of a high frequency phased array ultrasound transducer on a piezoelectric thick film using a finite element method (FEM) is shown. Generated FEM models were based on PMN-PT (Pb(Mg1/3Nb2/3)O3-PbTiO3) thick films, made by sol-gel technique, with the thickness vibrational mode resonant frequency of each film being close to 28.5MHz. Ultrasound transducers with such characteristics, due to their size and high frequency, are suitable for use in small medical diagnostic tools intended for use in delicate and sensitive areas (for example in ophthalmology and dermatology). With respect to their size, the transducers should retain very good focusing, beam steering and other advantages that phased array layout offers. To ensure an optimal performance of the phased array ultrasound transducer on such a piezoelectric thick film, several electrode patterns were used and tested in FEM simulations with the end goal of getting best performance from the PMN-PT thick films. A 64-element configuration was shown to be a promising technological solution for ophthalmological ultrasound diagnostics.

Keywords: Phased Array, Thick Film, PzFlex/OnScale, High Frequency, PMN-PT

Izdelava prototipa visokofrekvenčnega faznega polja ultrazvočnih pretvornikov na debelo plastnem piezoelektriku

Izvleček: V članku je prikazan proces virtualne izdelave prototipa visokofrekvenčnega polja ultrazvočnih pretvornikov na debelo plastnem piezoelektriku na osnovi FEM metode. Generirani FEM modeli temeljijo na PMN-PT filmih, ki so narejeni na tehnologiji sol-gel in sicer z debelino z vibracijsko resonančno frekvenco blizu 28.5 MHz. Ultrazvočni pretvorniki teh dimenzij in frekvenc so primerni za uporabo v majhnih medicinski diagnostični opremi za uporabo v občutljivih območjih (npr. oftalmologija in dermatologija). Zaradi svoje majhnosti naj bi pretvorniki zagotavljali dober fokus in vodenje žarka. Za doseganje optimalnega delovanja so bili obravnavani bili številni vzorci faznega polja ultrazvočnih pretvornikov. Izkazalo se je, da je, za uporabo v oftalmologiji, najboljša kombinacija s 64 elementi.

Ključne besede: fazno polje, debele plasti, PzFlex/OnScale, visoka frekvenca, PMN-PT

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1 Introduction

In modern medicine ultrasound is still an important diagnostic tool, despite development of new and advanced diagnostic techniques. Ophthalmology is probably the most illustrative example: although optical diagnostic methods are more present in medical practices, in cases of blur of the eye caused by a trauma or a disease, ultrasound is still the best way to look inside the eye. Ultrasound ophthalmological instrumentation available on the market is generally based on vibrating piezoelectric bulk transducers generating a single ultrasound wave. Such technology limits the highest available frequency, the minimum focus depth, and the minimum plane-wave formation distance.

Imaging of anterior eye chamber is rather important since precursors of many eye diseases create in it. Due to their generally low ultrasound frequency, this front part of the eye cannot be probed with high resolution by present ultrasound diagnostic tools. Since the resonant frequency of piezoelectric material inversely depends on its thickness, implementation of thick piezoelectric films as ultrasound-source material would increase the frequency to tens or hundreds MHz range. For ophthalmology applications such frequencies are targeted ones, since they can enable to probe microstructures on distances of few millimeters from the transducer. Linear array of micro-transducers based on a piezoelectric film could improve the overall performance further, since, by tuning the phase of each micro-transducer ultrasound, the diagnostic ultrasound wave can be focused in a controllable way. Although many research efforts are taken to create such phase-tuned linear arrays [1-8], they still cannot be routinely created. The major difficulty is the preparation of high-quality piezoelectric films of thickness of few or few tens of micrometers convenient for such applications (problems with ultrasound cross-talk). Further, as resonant frequency of the film increases, the size of a single micro-transducer decreases to size that makes traditional mechanical cutting techniques inapplicable.

Recent studies show drawbacks of thinned bulk ceramics over piezoelectric films [9-11]: in the piezoelectric films higher vibration amplitudes can usually be present, with smaller hysteresis, and the films can produce higher energy densities with lower power requirements. Thick films of lead magnesium niobium titanate (PMN–PT) have superior piezoelectric and dielectric constants when compared to zinc-oxide (ZnO) and lead zinc titanate (PZT) [12-19], distinguishing them as the main candidates for high-frequency ultrasound transducers.

In this paper we show a finite element modelling (FEM) analysis of different configurations of metallic electrodes deposed on a thick piezoelectric film. Each electrode with the piezoelectric film beneath is considered as an ultrasound micro-transducer. The modelling is based on properties of PMN-PT film available in our laboratory and can be used for experimental realization of studied models.

2 Sample properties

The acoustically active basis for the FEM analysis presented here is a set of PMN-PT ($Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$) thick films. Films were deposited by screen-printing at the Jožef Stefan Institute, Ljubljana, Slovenia (details of film preparation are given on [20-22]). Fig. 1 shows a cross section of the film imaged by a FEI Apreo scanning electron microscope. The films thicknesses are around 30 μm, with the average grain size of 5 μm. For the electrical characterization we used a vector network analyzer Bode 100 of Omicron Lab. Fig. 2 gives the electrical impedance *Z* (top) and the phase angle ϕ (bottom):

$$\phi = arctan\frac{Im(Z)}{Re(Z)} \tag{1}$$

where Im(*Z*) and Re(*Z*) are the imaginary and real parts of the electrical impedance, respectively. The impedance is measured on the whole sample area. Due to structural homogeneity of the active layer (see Fig. 1), we assume that electrical properties are homogenous as well. It shows broad antiresonance-resonance peaks at 1.7 MHz and 28.5 MHz respectively, that indicates weak electromechanical coupling. Resonant frequency of 28.5 MHz is used in the FEM analysis presented later in the text. Models used for the FEM analysis are based on four samples of phased array ultrasound transducers on a piezoelectric thick films, all made with 16 electrodes. The layout of the samples is shown in Figure.3.

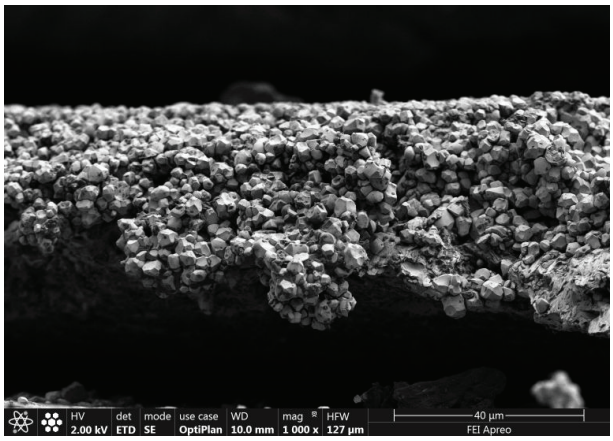


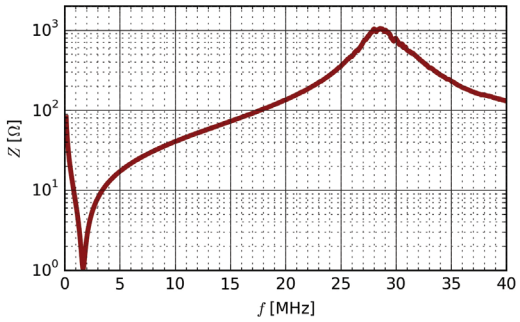
Figure 1: A scanning electron microscope image of the cross-section of the PMN-PT film.

The material properties of the phased array ultrasound transducer on a piezoelectric thick film and other geometrical parameters are given in Table.1.

Table 1: Phased array ultrasound transducer parameters.

Layer	Material	Function	Width	Length	Thickness
1	Al_2O_3	Substrate	5,4 mm	6,0 mm	3,0 mm
2	Au	Ground	5,4 mm	6,0 mm	10 μm
3	PMN-PT	Piezoelectric	5,4 mm	6,0 mm	30 μm
4	Al	Electrode	10 μm	4,0 mm	≤ 10 μm

a)



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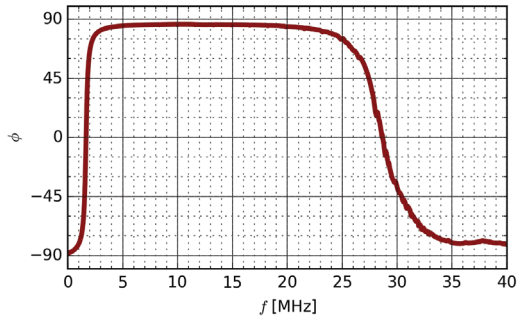


Figure 2: Frequency dependence of the electrical impedance (top) and the phase angle (bottom) of the tested PMN-PT film. Broad resonance-antiresonance frequency interval indicates weak electro-mechanical coupling.

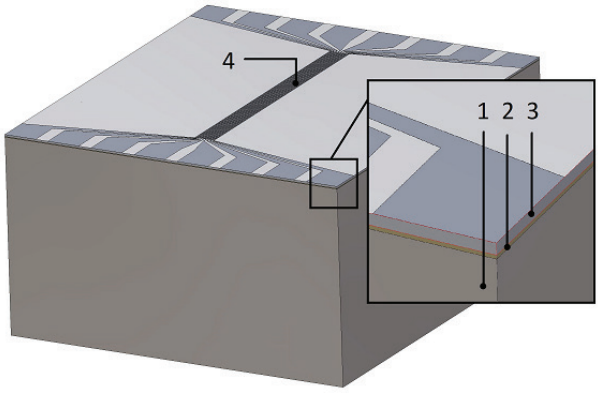


Figure 3: Phased array ultrasound transducer on a piezoelectric thick film layout

The main difference between the four models is in the electrodes arrangement. For example, the samples differ in pitch, aperture, etc. These parameters have critical influence on transducers performance; they are shown in Table 2.

Table 2: Electrodes arrangement on the transducer samples

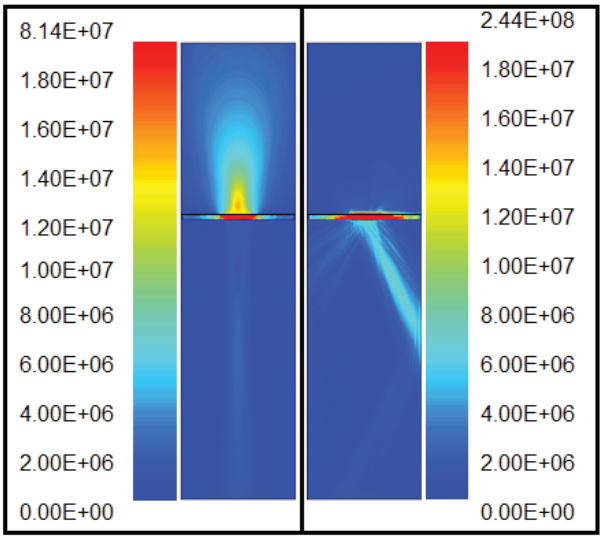
Wpassive	W	A	p	g	e
Sample 1	4 mm	0,310 mm	20 µm	10 µm	10 µm
Sample 2	4 mm	0.385 mm	25 µm	15 µm	10 µm
Sample 3	4 mm	0,460 mm	30 µm	20 µm	10 µm
Sample 4	4 mm	0,610 mm	40 µm	30 µm	10 µm

3 Results of fem analysis

2D model set-up is a multilayer structure with cross-section arranged in the same way as the model from Figure 3, while electrode-arrangement dimensions are as specified in Table 1.

Acoustic, piezoelectric, damping, dielectric and other properties of materials used are predefined in PzFlex material database [23].

A 2D model was set up to simulate the propagation of sound waves through a 3mm water column, with the central frequency being 28.5MHz and the amplitude peak being 100V. The analysis showed weak focus-



a) b)

Figure 4: Maximum acoustic pressure of Sample 1 configuration: a) focusing b) beam steering. Color scale values are in Pa, while model domain dimensions are 2x8 mm.

ing and good beam steering (25°) properties of these transducers. Bad focusing properties are visible in maximum acoustic pressure field graphic view (see Figure 4a), which shows a weak pressure field under the transducer and a lack of focus. The focusing of the passed array transducer was simulated by delaying the signal excitation on electrodes and the focal point was set to 3mm depth on the bottom of the water column, but the simulation results differ.

The weak focusing of the passed array transducer can be verified by calculating its near-field value, because the near-field gives the maximum depth for the usable focus for a given passed array configuration. Near-field values are given by the following equation:

$$N = \frac{D^2 f}{4c}[mm] \quad (2)$$

where:
$D = np$ [mm] for active phased array axis
$D = W$ [mm] for passive phased array axis
n - electrode number
W- passive aperture [mm]
f - frequency [Hz]
c - speed of sound through material [mm/s]

From Equation (2) it is calculated that the near-field value on the passive axis (i.e. the axis that cannot be focused) is N_p = 77.03mm, but the near-field value on the active axis, depending on a model, is N_{a1}=0.5mm (for p=20μm), N_{a2}=0.77mm (for p=25μm), N_{a3}=1.11mm (for p=30μm) and N_{a4}=1,97mm (for p=40 μm). Near-field values on the active axis clearly show weak focusing capabilities of the current transducer setup, which needs to be improved. Bad focusing properties also affect the beam steering because the beam dissipates and widens after the focal point.

The tested transducer setups have pronounced side lobes and there is a grating lobes formation at higher pitch values (30μm and 40μm). The side lobes are produced by an acoustic pressure leaking from probe elements at a different angle. Grating lobes are generated by the acoustic pressure due to even sampling across the probe element and they can be reduced by alternating the probe pitch, and keeping it below λ/2 value, if possible.

3.1 Modifying transducer setup

Referring to previously shown results, it is obvious that the main point of improvement is the focusing capability. Improvement of this capability can be done by modifying the electrodes arrangement. This can be done by increasing the electrode width (*e*) in some degree, because the electrode width affects the pitch (*p*) and the increasing of the electrode spacing (*g*) has an effect on the pitch. Changing pitch values is limited because it has a great impact on the grating lobes. The next option would be increasing the number of electrodes (n), which means going from 16 element phased array to 32 or 64 elements, and as well the electrode length should be corrected to balance the passive and active phased array axis. To limit the grating lobes, the pitch should be $p<\lambda/2$, but the general rule allows a pitch value up to $p<0.67\lambda$. Respecting this pitch limitation, near-field values are calculated for 32 and 64 elements electrodes configuration. The calculated values are shown in Table 3.

Table 3: Data calculated for different passed array transducer configurations.

n	p [μm]	e [μm]	g [μm]	A [mm]	W [mm]	Na [mm]	Rule
32	25	10	15	0.785	0.8	3.1	p<λ/2 (λ/2 =26 μm)
64	25	10	15	1.105	1.6	12.3	
32	30	10	20	0.94	0.96	4.4	λ/2<p<0.67λ
64	30	10	20	1.26	1.9	17.8	
32	35	15	20	1.1	1.12	6	p<0.67λ
64	35	15	20	1.58	2.2	24.2	

Values of the passive aperture (W) are now similar to the values of the active aperture (A) – they are chosen in this way to balance out the near-field values on the passive and active passed array axes (see Table 3).

3.2 Additional FEM analysis

Newly acquired electrode arrangement parameters on a phased array transducer must be verified by a FEM analysis software, so the additional FEM analysis was conducted with identical driving conditions (time function, frequency, voltage peak) as before. For additional analysis, two highlighted configurations from Table 3 are used for the 2D model setup. This is due to decent near-field values, which should mean that the transducers setups in this manner should have decent focusing depths.

The FEM analysis showed good focusing properties on chosen configurations (n=64, p=30μm and n=64, p=35μm). The analysis was set to simulate the 6mm focus in a 7mm high water column. The new configuration manages to successfully focus at the wanted depth, which is visible in the higher maximum acoustic pressure values around the wanted focusing depth (see Figure 5).

The 16 electrodes configuration produced higher-pressure values (see Figure 4) due to very long electrodes ($W_{passive}$ >> A) but focusing capabilities were poor. The 64 electrodes configuration produced smaller pressure values (Figure 5) but it had much better-focusing capabilities, and electrodes length was corrected on this configuration ($W_{passive}$ = A). It is important to mention that pressure values will also change with different focusing depths.

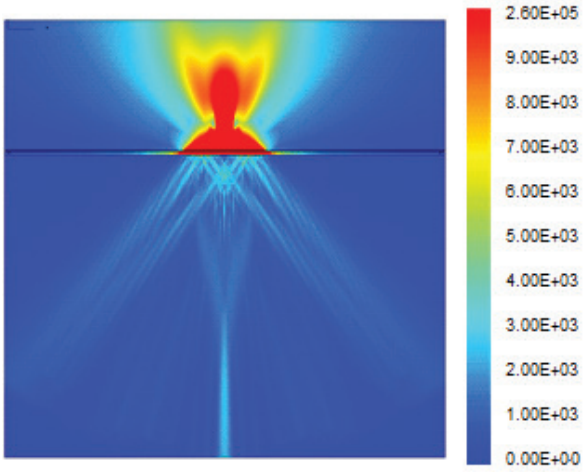


Figure 5: Maximum acoustic pressure of n=64, p=30 passed array transducer configuration. Color scale values are in Pa, while model domain dimensions are 10x10 mm.

This configuration also has a pronounced grating lobes formation because of a bit higher pitch value. To reduce this by keeping the pitch below λ/2 and to keep the focusing capabilities at least above 15mm it is necessary to further increase the electrodes number above, an already high, 64, compared to 16 electrodes at the start. Also with the 64 electrodes configuration, the transducer is still relatively compact in size, which brings benefits regarding possible applications.

The 64-electrodes configuration has better beam formation and better-focusing capabilities in comparison with 16 electrodes configuration. However, the sensitivity of both transducer configuration is poor. Due to a small pitch value (i.e., close electrode placement), which will provide a better beam formation and less scattering of the generated acoustic wave in water column, we have very pronounced crosstalk that affects transducers sensitivity in a way that reflections from barrier cannot be differentiated. This is visible on Figure 6, where each colored line represents the received signal of the one of 64 elements. The difference between frontwall and backwall of the barrier should be much more pronounced.

An increase of pitch value will result in more pronounced scattering of the acoustic wave, but with reduced crosstalk. To our estimate, pitch of 100 µm will lead to better transducer performance regarding the quality of acquired signals.

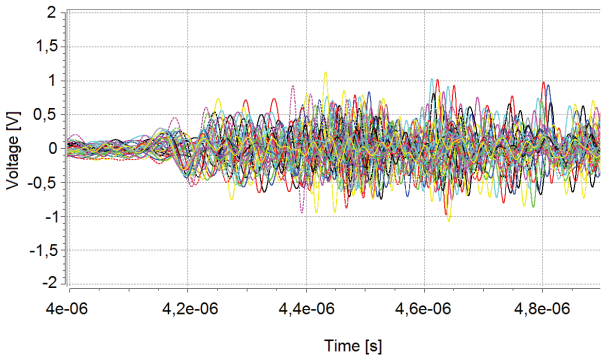


Figure 6: Crosstalk on received signal from a 0.450 mm thick barrier inside water column (for 64 electrodes configuration, pitch is 30 µm).

4 Conclusions

After conducted FEM simulations it is possible to conclude that the electrode pattern of considered transducers need at least 64 electrodes to obtain an optimal performance of a high-frequency miniature phased array ultrasound transducer on a PMN-PT thick piezoelectric film of central thickness mode vibration frequency of around 28.5MHz. If one considers potential applications of this kind of transducers, in ophthalmological diagnostic tools for example, it is shown here that weak and technically unusable phased array transducer properties of a 16-electrodes configuration cannot probe the front part of an average eyeball, with a diameter around 24 mm. The 64-electrode phased array configuration of a thick PMN-PT piezoelectric film of central thickness mode vibration frequency close to 30MHz could theoretically achieve a full depth ultrasound diagnostics coverage of an average human eye.

5 Acknowledgments

Ante Bilušić wish to thank to Dr Barbara Malič, Jožef Stefan Institute, Ljubljana, Slovenia for providing PMN-PT samples. This research was partially supported under the project MEMSplit, Contract Number: RC.2.2.08-0052, a project funded by the European Union through the European Regional Development Fund – the Operational Programme Regional competitiveness 2007 – 2013 (RC.2.2.08).

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https://support.onscale.com/hc/en-us/articles/360007367631-4-Materials.

Arrived: 31. 08. 2018
Accepted: 22. 01. 2019

Original scientific paper
https://doi.org/10.33180/InfMIDEM2019.102

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 1(2019), 11 – 18

A Memetic based Approach for Routing and Wavelength Assignment in Optical Transmission Systems

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Abstract: In optical networks, Routing and Wavelength Assignment (RWA) problem is one of the major optimization problems. This problem can be solved by different algorithms such as Genetic Algorithm (GA), Artificial Bee Colony (ABC), Ant Colony Optimization (ACO), etc. Shuffled Frog Leaping Algorithm (SFLA) is implemented in the proposed work, to solve the RWA problem in long-haul optical networks. The goal is to use minimum number of wavelengths and to reduce the number of connection request rejections. Cost, number of wavelengths, hop count and blocking probability are the performance metrics considered in the analysis. Various wavelength assignment methods such as first fit, random, round robin, wavelength ordering and Four Wave Mixing (FWM) priority based wavelength assignment are used in the analysis using SFLA. Number of wavelengths, hop count, cost and setup time are included in the fitness function. The SFLA algorithm proposed, has been analyzed for different network loads and compared with the performance of genetic algorithm.

Keywords: ACO, GA, RWA, SFLA

Memetični pristop za usmerjanje in dodeljevanje valovnih dolžin v optičnih prenosnih sistemih

Izvleček: V optičnih omrežjih je največji problem optimizacije usmerjanje in dodeljevanje valovnih dolžin. Problem je rešljiv z uporabo različnih algoritmov, kot so genetični algoritem (GA), umetna kolonija čebel (ABC) in optimizacija kolonije mravelj (ACO). V članku je, za reševanje problema RWA v optičnih omrežjih na dolgih razdaljah, implementiran algoritem mešanega žabjega skakanja (SFLA). Cilj je uporabiti najmanjše število valovnih dolžin in zmanjšati število zavrnitev zahtevkov za povezavo. Stroški, število valovnih dolžin, število preskokov in verjetnosti blokiranja so parametri analize uspešnosti. V analizi se z uporabo SFLA uporabljajo različne metode določanja valovnih dolžin, kot so prvo prileganje, naključno, krožno določanje valovnih dolžin in dodelitev valovne dolžine s štirimi valovnimi mešanji (FWM). Predlagani algoritem SFLA je bil analiziran za različne obremenitve omrežja in primerjan z učinkovitostjo genetičnega algoritma.

Ključne besede: ACO, GA, RWA, SFLA

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1 Introduction

In long-haul, high capacity communication networks, Optical systems and networks are vital. The optical data is routed at intermediate nodes, depending on their wavelength (Le et al 2005 and Bisbal et al 2004). Different optical components are used to regulate the data traffic and to direct it to the end user like optical splitters / combiners being used to separate the optical signals and collect them as they propagate through the network (Ramaswami & Sivarajan 2000). Wavelength based services like routing and grooming are the provided by optical networks. Transmission capacity and communication range are better in optical fiber communication (Vidmar 2001).Transferring more information with minimum equipment is the goal of an optical communication system (Batagelj 2014).

The capacity of optical system can be improved by Wavelength Division Multiplexing (WDM). These systems and networks make use of the features of optical fibers and WDM components. Different problems that persist in optical wavelength division multiplexing are optimal routing, traffic grooming and wavelength assignment, survivability and Quality of Service (QoS)

problems (Bhanjaa and Mahapatra 2013 and Adhya and Datta 2009). More computational time is involved in solving these problems using conventional methods (Wang et al 2014 and Triay et al 2010). Selecting a suitable path and allocating a available wavelength for an optical connection results in the problem called Routing and Wavelength Allocation (RWA) problem (Srinath & Janet 2013). To solve the RWA problem, which are in real- world optical networks, Multi-objective evolutionary algorithms based on swarm intelligence are used (Kavian et al 2013 and Largo et al 2012). Also Genetic Algorithm is used in many application due to less complex computation (Başak et al 2014). Shuffled Frog Leaping Algorithm is used to solve this RWA problem in the proposed research. Certain simpler or similar algorithms lead to poor performance or are too complex to be used. Therefore, a computationally feasible algorithm is used for a good performance of the network.

In this research paper, two optimization algorithms - genetic algorithm and shuffled frog leaping algorithm are used in the routing and wavelength assignment problem model. In variety of fields, Genetic Algorithm is used to solve many problems and hence comparison between these two algorithms are done. The simulation results and analysis are discussed and the conclusions of the study and possible future work are presented.

2 Routing and wavelength assignment

In dynamic routing and wavelength assignment, the requests for lightpath will arrive dynamically. Wavelength continuity constraint is that, on all the links in its path, a lightpath should use same wavelength. The time for which a lightpath and the required resources remain occupied is called as holding time. When the holding time expires, the resources allocated are made free and are made available to support other lightpath requests. The RWA model involves a network model, routing model, wavelength assignment model and an optimization algorithm (Bhanjaa et al 2013). Routing and Wavelength Assignment model with optimization is shown in Fig.1.

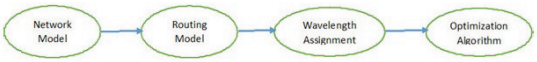

Figure 1: Block diagram of an RWA model with optimization

2.1 Network and Routing Model

A network which contains N number of nodes can be modeled as a graph NG(R,E), where E denotes the set of edges representing the connectivity between the nodes and R represents the set of nodes like routers or switches. It is assumed that the links between the nodes are bidirectional. National Science Foundation Network (NSFNET), Advanced Research Projects Agency Network (ARPANET) and European Optical Network (EON) are few standard network architectures currently in use.

One of the major problems in optical networking is Routing and Wavelength Assignment (RWA). The goal is to reduce the rejection of connection requests i.e. to maximize the number of optical connection. For every connection request, a particular route and a wavelength should be assigned. If wavelength converters are not used in the network, then same wavelength should be used throughout the path. Same optical link may be shared by two connections requests, if different wavelengths are provided (Bhanjaa et al 2012).
Fitness function to be maximized is given by

$$f_x = \frac{W_x}{\sum_{j=1}^{k_x-1} C_{gx(j),gx(j+1)}} + \frac{W_x}{\sum_{(i,j)\in E} H_{i,j}^x} + \frac{W_x}{T_x} \quad (1)$$

W_x is the free wavelength factor. The value of this factor is one, if same wavelength is available in all the links of path x or otherwise, zero. In the first term, the summation defines the total link cost of the path and similarly in the second term, the summation represents the total number of hops in the path. If link (i, j) is a part of path x, the variable $H^x_{i,j}$ takes the value of one and otherwise, it is zero. The set up time of the path x is represented by the variable T_x. Variable K_x represents the length of the x-th chromosome or number of memeplexes. The route is optimal when the objective function maximizes with the following constraints being satisfied.

$$\sum_{(i,j)\in E} I_{ij}^{lp} - \sum_{(j,i)\in E} I_{ij}^{lp} = 1, \text{ if i=S, lp ÎLP} \quad (2)$$

$$\sum_{(i,j)\in E} I_{ij}^{lp} - \sum_{(j,i)\in E} I_{ij}^{lp} = -1, \text{ if i=D, lpÎLP} \quad (3)$$

$$\sum_{(i,j)\in E} I_{ij}^{lp} - \sum_{(j,i)\in E} I_{ij}^{lp} = 0, \text{ if i≠S, i≠D, lpÎLP} \quad (4)$$

$$\sum_{\substack{i\neq j \\ (i,j)\in E}} I_{ij}^{lp} \leq 1, \text{ if i≠D, lpÎLP} \quad (5)$$

$$\sum_{\substack{i\neq j \\ (i,j)\in E}} I_{ij}^{lp} = 0, \text{ if i=D, lpÎLP} \quad (6)$$

$$\sum_{(i,j)\in E} I_{ij}^{lp} \leq h_0, \text{ for t ≤ T} \quad (7)$$

$$h_0 < \sum_{(i,j)\in E} I_{ij}^{lp} \leq (N-1) \text{, for t > T (8)}$$

Equations (2) to (6) represent the flow conservation constraint. Equations (7) and (8) represent the hop count constraint.

2.2 Wavelength Assignment Model

First fit and Random fit are the wavelength assignment techniques are the generally used techniques. First Fit method chooses the available wavelength with the lowest index whereas random fit method identifies the available wavelengths and chooses one amongst them in a random manner. For both the algorithms, O(w) is the complexity and w indicates the number of wavelengths. First Fit performs better than Random Fit. Other wavelength assignment techniques such as round robin technique, wavelength ordering technique and Four Wave Mixing aware wavelength assignment technique are also used for the analysis. One of many fiber nonlinear effects is a four-wave mixing (FWM) phenomenon (Batagelj et al 2004 and Batagelj & Vidmar 2002). When more than two wavelengths of light interact with each other while propagating through the medium, a spurious component is produced. Since the FWM crosstalk power will be more over the center of transmission window, in the FWM aware wavelength assignment technique priority is given to the wavelengths towards the edges of the transmission window. Complexity of this method is $O(N^3 \log^2 N)$, where N is the number of nodes in the network. In the fitness function proposed, Wx the free wavelength factor is updated after the wavelength assignment phase. In the wavelength assignment model, if the link (i, j) is used by the lightpath lp, the variable I_{ij}^{lp} assumes one else it assumes zero. Variable I_{ijw}^{lp} is the lightpath wavelength indicator. It shows whether the lightpath lp uses wavelength 'W' on link (i, j). Variable $I_{ijw}^{lp}(x,y)$ is the lightpath wavelength link indicator and this is one when the lightpath uses wavelength 'W' on link (i, j) between the nodes x and y. l(x,y) takes one if a physical link exists between the nodes x and y (Bhanjaa et al 2010).

The wavelength continuity constraints are

$$I_{ij}^{lp} = \sum_{w=0}^{W-1} I_{ijw}^{lp} \text{, } \forall \text{ (i,j)} \quad (9)$$

$$I_{ijw}^{lp(x,y)} \leq I_{ijw}^{lp} \text{, } \forall \text{ (i,j), } \forall \text{ (x,y) , } \forall \text{ w} \quad (10)$$

$$\sum_{i,j} I_{ijw}^{lp(x,y)} \leq 1 \text{, } \forall \text{ (x,y), } \forall \text{ w} \quad (11)$$

$$\sum_{w=0}^{W-1} \sum_{x} I_{ijw}^{lp(x,y)} l^{(x,y)} - \sum_{w=0}^{W-1} \sum_{x} I_{ijw}^{lp(y,x)} l^{(y,x)} = I_{ij}^{lp} \text{, y=j} \quad (12)$$

$$\sum_{w=0}^{W-1} \sum_{x} I_{ijw}^{lp(x,y)} l^{(x,y)} - \sum_{w=0}^{W-1} \sum_{x} I_{ijw}^{lp(y,x)} l^{(y,x)} = -I_{ij}^{lp} \text{, y=i} \quad (13)$$

$$\sum_{w=0}^{W-1} \sum_{x} I_{ijw}^{lp(x,y)} l^{(x,y)} - \sum_{w=0}^{W-1} \sum_{x} I_{ijw}^{lp(y,x)} l^{(y,x)} = 0 \text{, y≠i, y≠j} \quad (14)$$

3 Optimization algorithms

3.1 Genetic Algorithm

The flow involved in Genetic Algorithm is shown in Fig.2. Initial population is created and it works iteratively on this initial solution set. The algorithm converges to arrive on best solution (Kavian et al 2009).

Chromosome is the route or path encoded from source to destination. A sequence of nodes creates each chromosome and is generated based on the topology of a particular network. Each chromosome may be of different length and each of them encodes the path from the sender node S to the receiver node D. By random selection of solutions, initial population is created. The initial population has only one chromosome.

Position of the nodes in routing paths do not affect the crossover. One pair is randomly chosen and the crossing site of each chromosome is identified by the locus

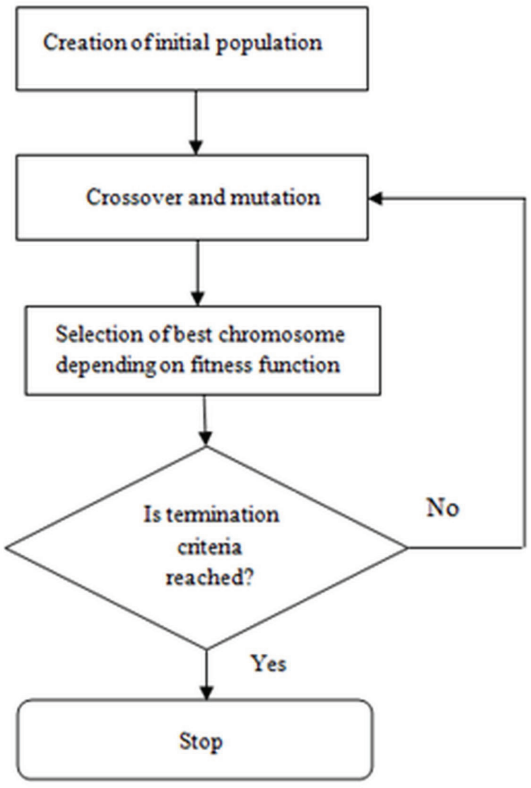

Figure 2: Flowchart of GA

of each node. The crossing points of two chromosomes may be different from each other (Ahn and Ramakrishna 2002). During mutation, the mutation site of the parent chromosome is chosen randomly. Based on the topology database, different path is chosen from the mutation site to the destination.

The fitness function is formulated as in equation (1) and is to evaluate the quality of the chromosomes.

3.2 Shuffled Frog Leaping Algorithm

Shuffled Frog Leaping Algorithm (SFLA) is a meta-heuristic algorithm inspired by nature. Novelty of this algorithm is its fast convergence speed (Hemalatha and Mahalakshmi 2017). Various other factors that cause latency or delay in the optical network at the physical layer are the optical fiber, optical amplifiers and other modules in the network out of which the propagation delay caused by the fiber is more predominant (Eržen and Batagelj 2015). Advantages of both the genetic-based memetic algorithm and the behavior-based Particle Swarm Optimization (PSO) algorithm are combined together in SFLA. SFLA combines the benefit of the local search tool of Particle Swarm Optimization (PSO) and the idea of mixing information from parallel local searches, to move towards a global solution (Muzaffar et al. 2006). In the SFLA, group of frogs that define possible solutions are referred to as population. These groups of frog are partitioned into several communities and are called as memeplexes. Each frog in the memeplexes perform local search. Behavior of each frog within the memplex influences the behavior of the other frogs and through a process of memetic evolution it is developed. After a certain number of memetic evolutions, the memeplexes are forced to mix together and through shuffling process, new memeplexes are formed. Until convergence criteria are satisfied, the local search and the shuffling processes continue. The flowchart of Shuffled frog leaping algorithm is illustrated in Fig.3 (Roshni et al 2016).

The steps involved are given as below:

a) SFLA involves a population 'P' of possible solution, defined by a group of virtual frogs(n).
b) Frogs are sorted in descending order based on their fitness and partitioned into subsets called as memeplexes (m).
c) Frog i is expressed as $X_i = (X_{i1}, X_{i2}, \ldots..X_{i3})$ where X represents number of variables.
d) Frogs with worst and best fitness are identified as X_w and X_b within each memeplex.
e) Frog with global best fitness is identified as X_g.
f) The frog with worst fitness is improved based on the following equation.

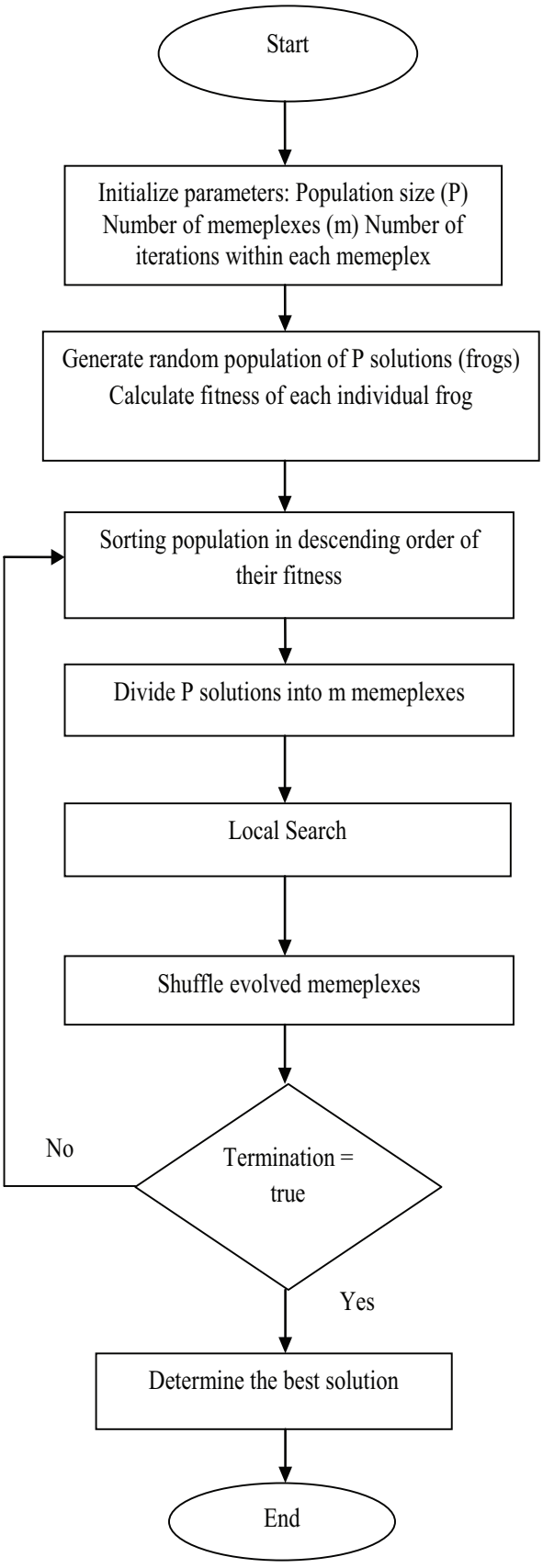

Figure 3: Flowchart of SFLA

D_i=rand() (X_b -X_w) (15)

X_{neww}=X_{oldw}+ D_i (16)

Rand() is a random number in the range of [0,1] (Muzaffar 2006).

D_i is the step size of i-th leaping frog and D_{max} is the maximum step size allowed. If the fitness value of new X_w is better than the current one, X_w will be accepted. Otherwise, the calculated step size of leaping frog D_i and new fitness X_{neww} are recomputed with X_b replaced by X_g. Further if no improvement is achieved, a new X_w is generated randomly. The update operation is repeated for specific number of iterations. After a predefined number of memetic evolutionary steps within each memeplex, the solutions of evolved memeplexes are replaced into new population. This is called shuffling process. Global information exchange among the frogs is promoted by the shuffling process. The population is then sorted in order of decreasing performance values and updates the population based on best frog's position, repartition the frog group into memeplexes and progress the evolution within each memeplex until the conversion criteria are satisfied (Samuel and Rajan 2014).

4 Simulation results

The optimization algorithms have been implemented using the software MATLAB. Simulations are carried out for a 14 node network having 21 bidirectional links similar to NSFNET network topology. The fitness against the execution time for the genetic algorithm and shuffled frog leaping algorithm with 4 number of channels fand a load of 10 Erlangs is shown in Fig.4. Number of hops, holding time and cost are the paramateres included in the fitness function. The shuffled frog leaping algorithm has a better fitness compared to the genetic algorithm.

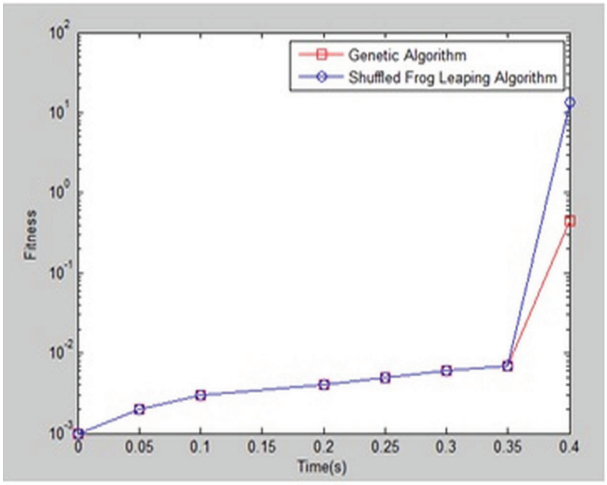

Figure 4: Fitness function of GA and SFLA

The mean blocking probability against number of generations for GA and SFLA with 4 number of channels fand a load of 10 Erlangs are shown in Fig.5 and 6 respectively. By comparing both the figures, its is clear that the blocking probability is lesser in SFLA than in GA. Among the three wavelength assignment techniques Round robin Technique has the least blocking probability.

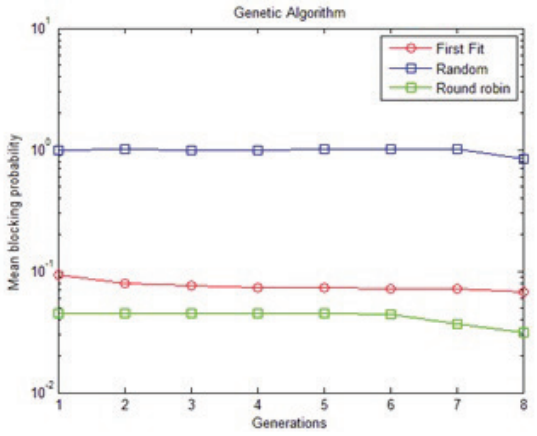

Figure 5: Mean blocking probability against number of generations using GA

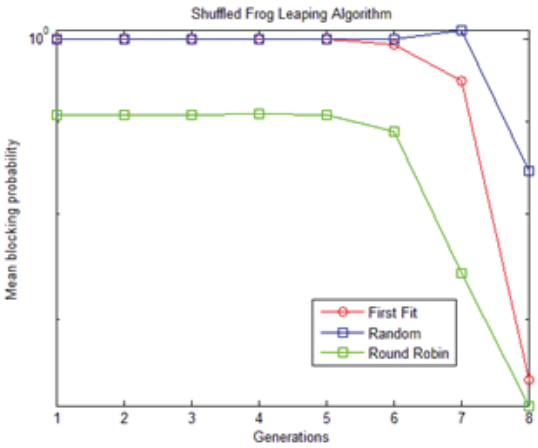

Figure 6: Mean blocking probability against number of generations using SFLA

For different wavelength assignment techniques first fit, random, round robin, wavelength ordering and FWM aware priority based wavelength assignment, the rate of convergence of genetic algorithm and shuffled frog leaping algorithm with 4 number of channels fand a load of 10 Erlangs is shown Fig.7. By randomly selecting an individual and choosing the best fitness

value, the graphs are plotted. The average fitness score decreases, as the generations increase. For both GA and SFLA with different wavelength assignment techniques, the average fitness score is approximately the same. Among all the wavelength assignment techniques, FWM priority based assignment has a better average fitness score.

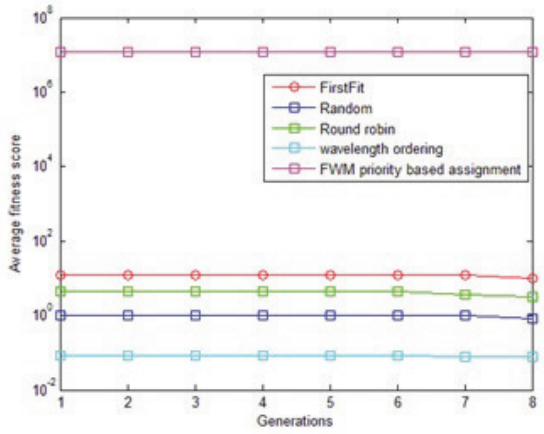

Figure 7: Average fitness score for GA and SFLA

The experimental results of mean execution time obtained for different wavelength assignment techniques First Fit, Random, Round Robin, Wavelength Ordering and FWM aware priority based wavelength assignment using GA and SFLA for various network load in Erlangs is as ahown in Table 1. The mean execution time (seconds)varies appropriately with the network loads and is observed that FWM aware priority based wavelength assignment technique requires very minimum mean execution time in both GA and SFLA algorithms for various network loads. When SFLA is compared with GA, SFLA requires minimum mean execution time for all the wavelength asignment techniques.

The imrpovements achieved in the mean execution time while using SFLA compared to GA is showm in Table 2. The experimental results are quantified using t-test to show the improvements in the proposed SFLA algorithm. The parameters t and p-value are dimensionless. The p-values obtained for all the wavelength assignment techniques are less than or equal to the level of significance value 0.05. This shows that the mean execution time is lesser for the proposed shuffled frog leaping algorithm compared to genetic algorithm.

5 Conclusions

One of the complex optimization problems in optical networks is Routing and Wavelength Assignment

Table 1: Mean Execution Time for different wavelength assignment techniques using GA and SFLA

Wavelength Assignment Techniques	Mean Execution Time for various network loads(Erlang) using GA in seconds					Mean Execution Time for various network loads(Erlang) using SFLA in seconds				
	0	0.7	2.0	3.3	4.6	0	0.7	2.0	3.3	4.6
First Fit	0.1200	0.0241	0.0537	0.1024	0.1029	0.1191	0.0232	0.0504	0.1019	0.1003
Random	0.3000	0.2462	0.2398	0.3071	0.3824	0.2987	0.2451	0.2369	0.3042	0.3736
Round Robin	0.1200	0.1543	0.1597	0.2002	0.2357	0.1198	0.1503	0.1513	0.2001	0.2227
Wavelength Ordering	0.0500	0.0049	0.0108	0.0297	0.0453	0.0490	0.0044	0.0097	0.0281	0.0404
FWM priority based Assignment	0.0050	3.873e-11	7.490e-11	2.0037e-10	3.01e-10	0.038	3.726e-11	7.329e-11	1.998e-10	2.92e-10

Table 2: T-test results showing improvements in Mean Execution Time in SFLA

Wavelength Assignment Techniques	Difference between Mean Execution Time for various network loads(Erlang) of SFLA and GA in seconds					Average in seconds	Standard Deviation in seconds	t	p-value
	0	0.7	2.0	3.3	4.6				
First Fit	0.0009	0.0009	0.0033	0.0005	0.0026	0.00164	0.001232	2.98	0.02
Random	0.0013	0.0011	0.0029	0.0029	0.0088	0.0034	0.003137	2.42	0.04
Round Robin	0.0002	0.004	0.0084	1e-04	0.013	0.00514	0.005557	2.07	0.05
Wavelength Ordering	0.001	0.0005	0.0011	0.0016	0.0049	0.00182	0.001766	2.31	0.04
FWM priority based Assignment	-0.033	1.47e-12	1.61e-12	5.7e-13	9e-12	-0.0066	0.014758	-1	-

(RWA) problem. In the proposed work, two optimization algorithms Genetic Algorithm and Shuffled Frog Leaping Algorithm are used to solve the problem. The fitness function minimizes the blocking probability, number of hops and cost. Basic wavelength assignment techniques such as first fit, random and round robin and also wavelength ordering and FWM aware priority based wavelength assignment are used to analyze the performance of the algorithms GA and SFLA.

Fitness value achieved is found to be better in SFLA compared to GA. The two optimization algorithms GA and SFLA are compared in terms of mean execution time, mean blocking probability and fitness score. The experimental results show that SFLA has better fitness score, less mean execution time and minimum mean blocking probability. Within the algorithm among various wavelength assignment techniques, FWM aware priority based wavelength assignment technique achieves better average fitness score and also less mean execution time. Time complexity of SFLA approach is lower compared to that of Genetic Algorithm and therefore some flexibility may be provided in the network design.

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Arrived: 12. 06. 2018
Accepted: 24. 12. 2018

Original scientific paper
https://doi.org/10.33180/InfMIDEM2019.103

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 1(2019), 19 – 23

Design of Low Power and Low Phase Noise Current Starved Ring Oscillator for RFID Tag EEPROM

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Abstract: Power dissipation of CMOS IC is a key factor in low power applications especially in RFID tag memories. Generally, tag memories like electrically erasable programmable read-only memory (EEPROM) require an internal clock generator to regulate the internal voltage level properly. In EEPROM, oscillator circuit can generate any periodic clock signal for frequency translation. Among different types of oscillators, a current starved ring oscillator (CSRO) is described in this research due to its very low current biasing source, which in turn restrict the current flows to reduce the overall power dissipation. The designed CSRO is limited to three stages to reduce the power dissipation to meet the specs. The simulated output shows that, the improved CSRO dissipates only 4.9 μW under the power supply voltage (VDD) 1.2 V in Silterra 130 nm CMOS process. Moreover, this designed oscillator has the lowest phase noise -119.38 dBc/Hz compared to other research works. In addition, the designed CSRO is able to reduce the overall chip area, which is only 0.00114 mm^2. Therefore, this proposed low power and low phase noise CSRO will be able to regulate the voltage level successfully for low power RFID tag EEPROM.

Keywords: CMOS, RFID, EEPROM, CSRO, power dissipation

Načrtovanje tokovno omejenga oscilatorja nizkih moči in nizkega faznega šuma za RFID EEPROM nalepke

Izvleček: Poraba moči CMOS IC je izredno pomembna pri napravah nizkih moči, posebej še pri spominu RFID nalepk. V spošnem, spomin nalepk, kot je elektronsko izbrisljiv in programirljiv EEPROM, potrebuje generator interne ure za reguliranje internega napetostnega nivoja. Poleg številnih tipov osclatorjev je v članku opisan tokovno omejen obročni oscilator (CSRO), saj zaradi omejitve toka, ki zmanjšuje porabo moči. Načrtan CSRO uporablja tri stopnje za doseganje specificirane porabe moči. Simuliran oscilator potrebuje 4,9 μW pri napajalni napetosti 1,2 V in realizaciji v 130 nm Silterra CMOS tehnologiji. V primerjavi z drugimi oscilatorji ima najnižji fazni šum -119,38 dBc/Hz in majhno površino 0,001144 mm^2. Predlagan oscilator je sposoben regulirati napetost EEPROM RFID nalepk.

Ključne besede: CMOS, RFID, EEPROM, CSRO, poraba moči

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1 Introduction

Radio frequency identification (RFID) is a detection system, where communications happen through radio waves to complete the data transmission/ reception process between the reader and tag [1]. In an RFID system, transponder contains an electronic microchip with three main blocks; like front-end digital baseband processor and the memory, where the product information's are stored inside the tag memory. The microchip is fabricated as a low power integrated cir-

cuit (IC), which employs a memory depending on the device features like ROM, RAM, non-volatile memory (EEPROM, Flash) and data buffers [2-4]. At present, a key design aspect for RFID transponder IC is the low power dissipation and low cost. Therefore, EEPROM is the most used tag memory, which is easily applicable to an RFID tag, DC-DC converter, SOC and FPGA system due to its advantages of low cost, low power and compatibility with the standard CMOS process [1].

In RFID, tag EEPROM, a clock driving circuit is required to maintain the internal voltage regulation. The clock signal in RFID systems is generated using a low power on-chip oscillator. In EEPROM, the oscillator is the major circuit that is required to generate a clock signal internally to regulate the voltages. Generally, the output frequency of the oscillator is a linear function of its control voltage. Therefore, the output frequency should be a function of the control voltages, which has a tunable range [5].

Among all the voltage-controlled oscillators (VCOs), current-starved ring oscillator (CSRO) has the popularity due to their easy integration. Moreover, this CSRO is an essential building block in EEPROM, which is commonly used in the clock generation. This internal clock generation is required to provide the input clock signals for voltage boost up the process. In addition, a very low current biasing source is required in CSRO to restrict the current flows in inverters inside the oscillation process to reduce the power dissipation [6].

This paper presents an improved CSRO circuit, which is suitable for the EEPROM voltage regulator in RFID tags. The design of a CSRO involves many important factors like frequency, power dissipation, chip area, phase noise etc [6]. Therefore, the design method of CSRO is discussed in this research, illustrates a three-stage CSRO. This paper is organized with the design method of the CSRO followed by the results and discussions. Finally, the comparison table is presented to show the better performance results compared to other research works.

2 Methodology

The memory of the RFID transponder requires a clock driving circuit to provide the clocks for the charge pump/voltage boost up circuit. The clock signal in EEPROM is generated using either the incoming carrier or an on-chip block [6]. Therefore, a ring oscillator is essential to get the low power on-chip and stable clock signals for RFID transponders memory performances. Moreover, a very low current biasing source is allowed through the inverters, which limits the current flow and reduces the power dissipation. A typical ring oscillator is constructed with a number of delay stages, where the output of the last stage feedback to the input of the first stage. In this scheme, the rings need to generate a phase shift of 2π, which should have the unity voltage gain in the oscillation frequency. In this research, a three-stage CSRO is proposed as shown in Figure 1, which follows the same operating phenomenon.

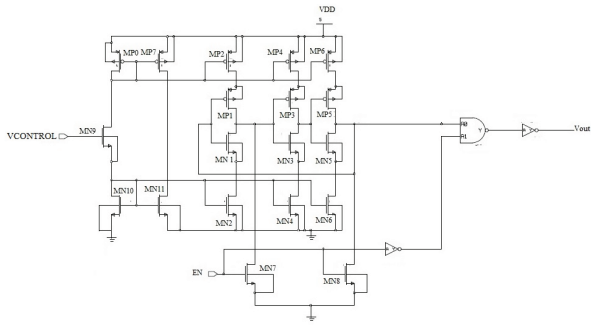

Figure 1: Schematic diagram of the proposed CSRO

MN1/MP2 is used to act as an inverter in the proposed design. On the other hand, MN2/MP2 acts as the mirror current source to limit the current flow through the inverter MN1/MP1. MP0, MP7, MN9, MN10 and MN11are required constructing a biasing circuitry for the oscillator. In this design, MP7/MN11 has the equal drain current, which is controlled by the input voltage VCONTROL and is mirrored to each level of the oscillator. In this proposed oscillator, an input pin EN is embedded with the main circuitry, which generates the reset signal for the chip. Moreover, when a power failure occurs from a certain level, this EN pin disconnects the chip. If the power supply voltage exceeds the required threshold, this EN pin generates a command signal to enable the chip operation. Therefore, the overall frequency of the proposed oscillator can be defined by the following equation.

$$f = \frac{1}{NT_D} = \frac{I_D}{NC_{equ}V_{DD}} \quad (1)$$

where, N is the stage number, T_D is the delay, C_{equ} is the single stage output equivalent capacitance, and VDD is the supply voltage.

In this proposed work, a three-stage CSRO is illustrated where some current starved inverters are involved to generate the oscillation frequency. In addition, to provide the bias current to the delay elements, an internal biasing circuitry with power switching in the conventional design is biased through this internal bias unit. This biasing circuitry delivers a range of control

voltages and helps to enhance the biasing voltage of the CSRO with maximum voltage variation, which ultimately elevates the sensitivity of the CSRO by engendering greater oscillation frequencies. On the other hand, designing a CSRO with frequency stability against temperature variation is another challenging task. Mostly, the threshold voltage in MOS transistors is one of the temperature dependent factors, which affects the oscillation frequency. As a result, to overcome this problem, the designed CSRO need to be controlled by a temperature independent source. Therefore, in this proposed design, a biasing unit is involved that generates the control voltage to the CSRO with minimum threshold voltage dependency and minimum temperature dependency.

3 Result and discussion

The proposed CSRO is designed and simulated in Mentor Graphics tool using Silterra 130 nm CMOS Process. To determine the operating frequency of the proposed CSRO circuit, the pre-layout simulated output frequency of the CSRO is shown in Figure 2. The operating temperature of the circuit is set to 27 ^{0}C.

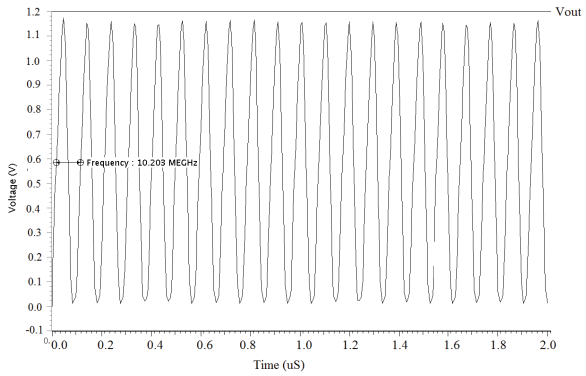

Figure 2: The simulated output of the proposed CSRO

From Figure 2 it is shown that, the proposed CSRO is achieved 10.2 MHz frequency when the control voltage is set to 1.2 V. The different transistor sizes of the proposed CSRO make it possible to get this desired frequency from the power supply voltage at 1.2 V. The operating temperature of the circuit is set to 27 ^{0}C. It is also illustrated from the figure that, the pre-layout simulation results also able to provide a full-swing oscillation signal with a supply voltage of 1.2 V.

To validate the proposed CSROs frequency range the design is simulated at different control voltages. Figure 3 shows the frequency deviation of the proposed CSRO circuit in terms of power supply deviations. Applying a range of power supply variation generates a frequency variation from 7 MHz to 11 MHz as shown in Figure 3. In this proposed design, it is observed that a non-linear relationship has been established due to the sensitivity of output frequency with respect to power supply variations. However, designing a CSRO with frequency stability against temperature variation is another challenging task

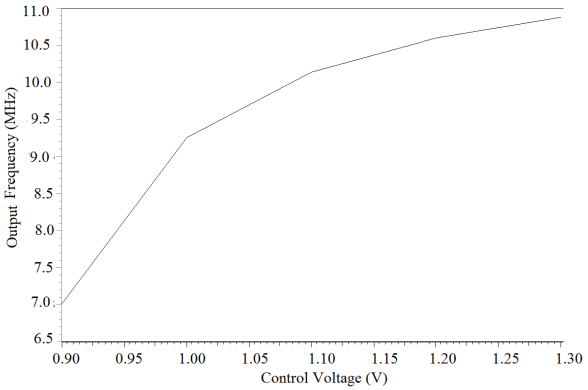

Figure 3: Tuning range of the proposed CSRO at 27 ^{0}C

As the improved CSRO is aimed to offer low power dissipation, the result shows that the power consumption of this design is only 4.9 µW. This result is superior to any recently published research works for RFID transponders memory clock generation. In our design, we have achieved a single side-band phase noise of −119.38 dBc/Hz at a 1MHz offset from the carrier as shown in Figure 4.

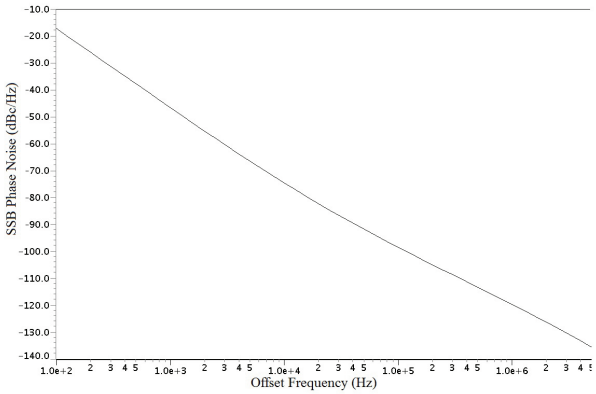

Figure 4: Single sideband (SSB) phase noise (PN) of the CSRO

In this design, a statistical analysis named Monte Carlo simulation is needed to calculate the impact of transistor and process variation mismatch. Therefore, a Monte-Carlo simulation with 100 runs is performed to validate the impacts. The results, shown in Figure 5, reveal that the designed current starved oscillator has an average frequency of 10.66 MHz with a standard deviation of 0.375 MHz.

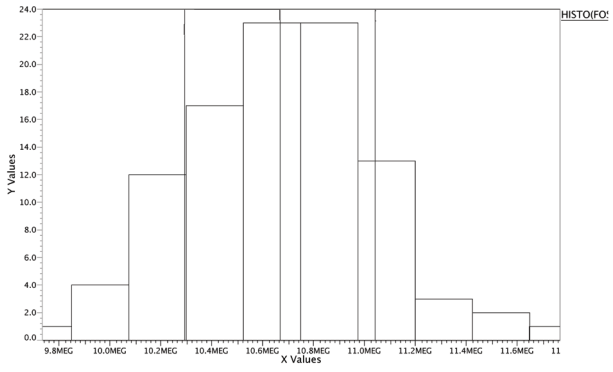

Figure 5: Monte Carlo simulations for oscillation frequency for ring oscillator

The principle of industry-oriented EDA tools (such as Mentor Graphics, Cadence, etc.) is expected to have the closest simulation result to the experimental result. Here, we have used Mentor Graphics to design, simulate, and draw the layout of our proposed design of CSRO. Therefore, the post-layout simulation will be expected to agree with the actual measurement result after IC fabrication. The layout design (Figure 6) has been sent for fabrication using standard 0.13 μm CMOS process including PADs and buffer circuit. A layout of the chip is shown in Figure 6, where the CSRO core occupies an area (without PADs) of 0.00114 mm^2. In this research, all the transistors have been placed in a way so that the mismatches and the area of the design can be reduced.

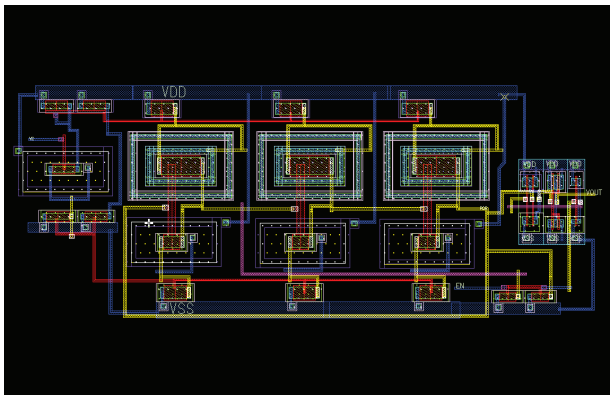

Figure 6: The layout of the proposed CSRO

Table 1: Performance comparisons of CSRO

References	Process (µm)	Power Supply (V)	Frequency (MHz)	P_{DC}, core (µW)	Phase noise (dBc/Hz)
[5]	0.13	1.3	28.2MHz-3.5GHz	590.88	-118@1MHz
[7]	0.18	0-1.8V	25.70 - 222.53	105.2	-
[8]	0.13	1.8	15.57	6000	-116.6@1MHz
[9]	0.18	1.8	1.02 GHz -3.99 GHz	7490	-80.17@ 1MHz
This Work	0.13	1.2	7-11	4.9	-119.38@1MHz

Table 1 summarizes the performance of the proposed CSRO along with other research works. In this research, a 10.2 MHz clock frequency is required to mitigate the requirements of the low power RFID tag EEPROM memory. Compared to all the research works shown in Table 1, the proposed CSRO has the lowest phase noise -119.38 dBc/Hz, which is the lowest compared to recently published research works with 10.2 MHz oscillation frequency. In addition, the proposed design has the lowest power dissipation only 4.9 µW compared to other research works, which makes the proposed design superior for low power applications. From the comparison in Table 1 it is found that, the proposed design has a small layout area, which eventually reduces the production cost.

In CMOS ring oscillators (single-ended or differential); a most common concern is the preferred method to generate better performance in terms of jitter, phase-noise, and total power dissipation. Single-ended CMOS ring oscillators phase noise and jitter are not strong functions of the number of stages [10-12]. However, the design is not done symmetrically or the design produces large noise, then a larger N will reduce the jitter. In general, the choice of the number of stages must be made based on several design criteria, such as 1/f noise effect, the desired maximum frequency of oscillation, and the influence of external noise sources.

4 Conclusion

An improved low power, low phase noise current-starved ring oscillator is presented in this research works. The design has only three inverter stages with the internal biasing method, which is required lower power, compared to other research works. The statistical analysis shows that the modified oscillator is able to produce the desired clock signal properly with different transistor sizing. Moreover, the comparison study shows that, the design has a lower phase noise -119.38 dBc/Hz@1 MHz offset from the carrier frequency. In addition, the simulated output shows that, the improved CSRO consumes only 4.9 μW power under supply voltage (VDD) 1.2 V in Silterra 130 nm CMOS process, which

is the lowest among previous research works. Finally, the working frequency for clock generation, which is 10.2 MHz and the small chip are make this proposed CSRO suitable for the voltage regulation of the low power application like RFID tag EEPROM.

5 Acknowledgements

The authors would like to express sincere gratitude to Universiti Kebangsaan Malaysia for supporting this research project through the GUP-2018-141 fund.

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Arrived: 08. 08. 2018
Accepted: 15. 01. 2018

Original scientific paper
https://doi.org/10.33180/InfMIDEM2019.104

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 1(2019), 25 – 32

Design and Performance Analysis of Hybrid SELBOX Junctionless FinFET

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Abstract: In this work, the performance of selective buried oxide junction-less (SELBOX-JL) transistor at a FinFET structure is analysed using numerical simulations. The proposed structure exhibits better thermal resistance (R_{TH}), which is the measure of the self-heating effect (SHE). The DC and analog performances of the proposed structure were studied and compared with the conventional and hybrid (or inverted-T) JLFinFETs (JLTs). The I_{ON} of the hybrid SELBOX- JLFinFET is 1.43x times better than the ION of the JLT due to the added advantage of different technologies, such as 2D-ultra-thin-body (UTB), 3D-FinFET, and SELBOX. The proposed device is modeled using sprocess and simulation study is carried using sdevice. Various analog parameters, such as transconductance (g_m), transconductance generation factor (TGF = g_m/I_{DS}), unity current gain frequency (f_T), early voltage (V_{EA}), total gate capacitance (C_{gg}), and intrinsic gain (A_0), are evaluated. The proposed device with a minimum feature size of 10nm exhibited better TGF, f_T, V_{EA}, and A_0 in the deep-inversion region of operation.

Keywords: Junctionless FinFET, Hybrid SELBOX-JLFinFET, Self heating, f_T, TGF.

Analiza zasnove in učinkovitosti hibridnega brezspojnega SELBOX FinFET-a

Izvleček: V članku je analiziran brezspojni SELBOX-JL transistor v FinFET strukturi. Predlagana struktura izkazuje boljšo termično upornost, ki je merjena preko lastnega segrevanja. DC in analogne lastnosti predlagan strukture so primerjanes konvencionalnimi in hibridnimi strukturami. Tok hibridnega SELBOX-JLFinFET je 1.43-krat boljši kot pri JLT zaradi uporabe drugačne tehnologije, kot je 2D ultra tanko ohišje, 3D-FinFET in SELBOX. Ocenjeni so številni parametri, kot je transkonduktanca, generacijski faktor transkonduktance, frekvenca tokovnega ojačenja, zgodnja napetost, skupna kapacitivnost vrat in osnovno ojačenje.

Ključne besede: Brezspojni FinFET, hibridni SELBOX-JLFinFET, lastno segrevanje, f_T, TGF.

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1 Introduction

Silicon on insulator (SOI) MOSFETs has numerous advantages over bulk MOSFETs such as low parasitics, better isolation, radiation hardness, improved speed, ability to operate at low V_{DD} and higher environmental temperatures [1, 2]. The improved gate control over the channel causes FinFETs to demonstrate reduced short channel effects (SCEs), such as drain-induced barrier lowering (DIBL), when compared to MOSFETs [3,4]. However, the performance of the conventional FinFETs is overshadowed by hybrid FinFETs by effective utilization of the device area. A higher drain current is attained in hybrid FinFET by employing the unused area in conventional FinFET. The added advantages of the SOI and ultra-thin body (UTB) technologies enable the hybrid FinFET to have more drain current for the same fin width (W_{fin}) and gate length (L_g) when compared to conventional FinFETs. Zhang et al. proposed hybrid FinFET [5] and was later explored by Fahad et al. in [6]. Subsequently, the impact of high-k symmetric and asymmetric spacer, fin shape, and temperature on the performance of the hybrid FinFETs were analyzed by Pradhan et al. [7,8,9,10]; and the effect of self-heating on the performance of hybrid FinFETs was studied by Nelapati et al.[11].

Continuous scaling of electronic devices led to the difficulty of having sharp doping profiles in inversion mode (IM) transistors. Consequently, this led to the invention of the transistor without junctions. Colinge et al. [12] demonstrated a junctionless transistor (JLT), which is free from the junction and any doping gradients. A

comparative study of SOI-JLT and bulk JLT was carried in [13]. SOI-JLT is better than the bulk JLT but lacks in thermal conductivity due to the presence of silicon dioxide as a buried oxide. Self-heating in SOI devices can be reduced by replacing silicon dioxide with better thermally conductive materials or by modifying the device structure [14, 15]. Narayanan *et al.* proposed a modified SOI device structure for reducing the self-heating effect [16]. In this structure, the buried oxide is patterned in the selective region under the source and drain, and not continuously, which is referred to as the SELBOX structure. Uzma *et al.* presented a comparative study of planar SELBOX and SOI junctionless transistors [17].

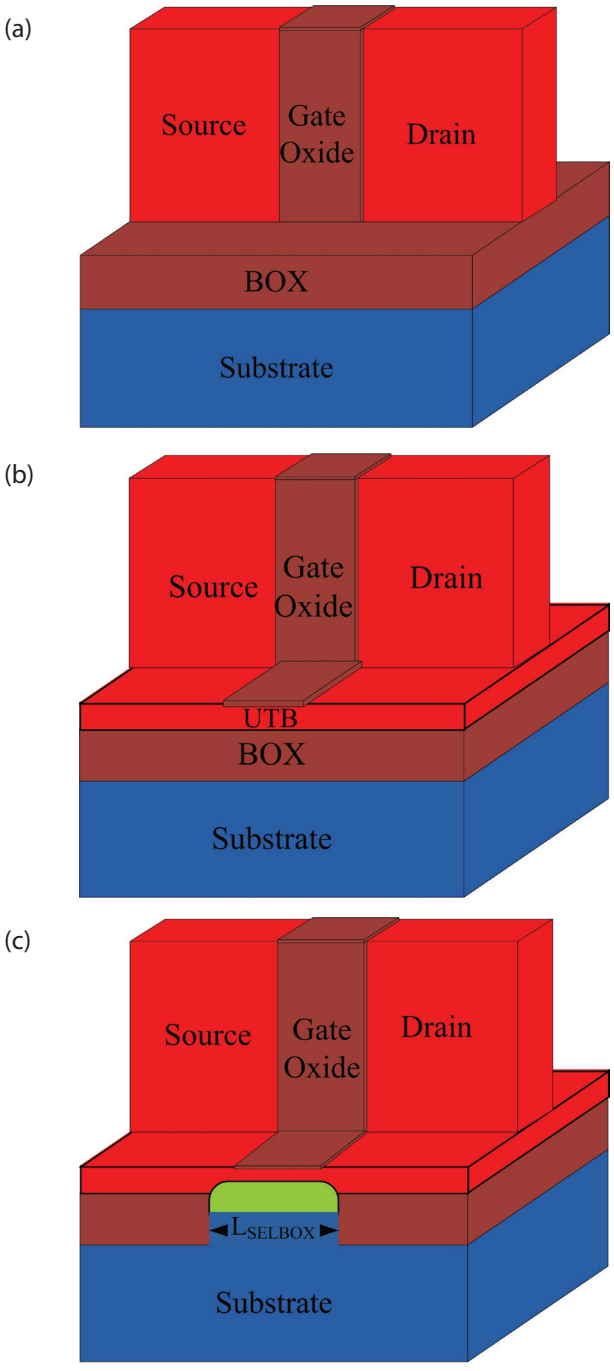

Figure 1: (a) Coventional JLT (SOI-JLT) (b) HJLT (c) HSJLT.

In this work, we analyzed the performance of hybrid SELBOX-JLFinFET (HSJLT), which is immune to self-heating and delivers higher drain current. The proposed structure adds the advantage of UTB, SOI technology, and SELBOX structure. Figure 1 depicts the 3-D view of conventional JLT, hybrid JLFinFET (HJLT), and HSJLT. The DC and analog performance of HSJLT are evaluated and compared with conventional and hybrid JLTs. The rest of the paper is organized as follows: Section 2 discusses the process flow of the proposed device and the simulation setup. Section 3 discusses the DC characteristics, self-heating effect, and analog performance of HSJLT and the comparison of simulation results with conventional and hybrid JLTs. The conclusions are drawn in Section 4.

2 Process flow and Simulation Setup

Figure 2 shows the process flow adopted for modeling the proposed HSJLT using sentaurus process (sprocess) [18]. Silicon material is defined as a substrate with underlying doping of boron ($5x10^{18}$ cm^{-3}). The insulating material, SiO_2, is deposited as a buried oxide on the selective regions by masking. The device structure after the BOX patterning is shown in Figure 2(a). The silicon material for the fin is deposited as shown in Figure. 2(b) with uniform doping of arsenic ($1x10^{19}$ cm^{-3}) and by masking, followed by etching the fin of the transistor is defined as shown in Figure. 2(c). HfO_2 is deposited as shown in Figure 2(d), which serves as the gate dielectric. Figure 2(e) shows the device structure after the deposition of the gate metal and spacer material. Finally, the metallization is carried for the contact of the source and drain, as shown in Figure 2(f).

Table 1 shows the device specifications and doping profiles of the three devices considered for the simulation. The OFF current (I_{OFF}), of the three devices shown in Figure 1, is adjusted to ≈ 1pA by tuning the gate metal work function (GWF). The GWF for conventional JLT, HJLT, and HSJLT is 4.72eV, 4.87eV, and 4.7eV, respectively. The GWF of HJLT is larger because the ultra-thin body transistor in hybrid devices will be turning on early when compared to fin transistor [6]. The GWF of HSJLT is smaller when compared to HJLT because the planar transistor's gate is depleted in HSJLT by both GWF and the depletion region formed by the oppositely doped substrate [19].

The sentaurus device (sdevice) is used to conduct device simulations [20]. Mobility degradation models,

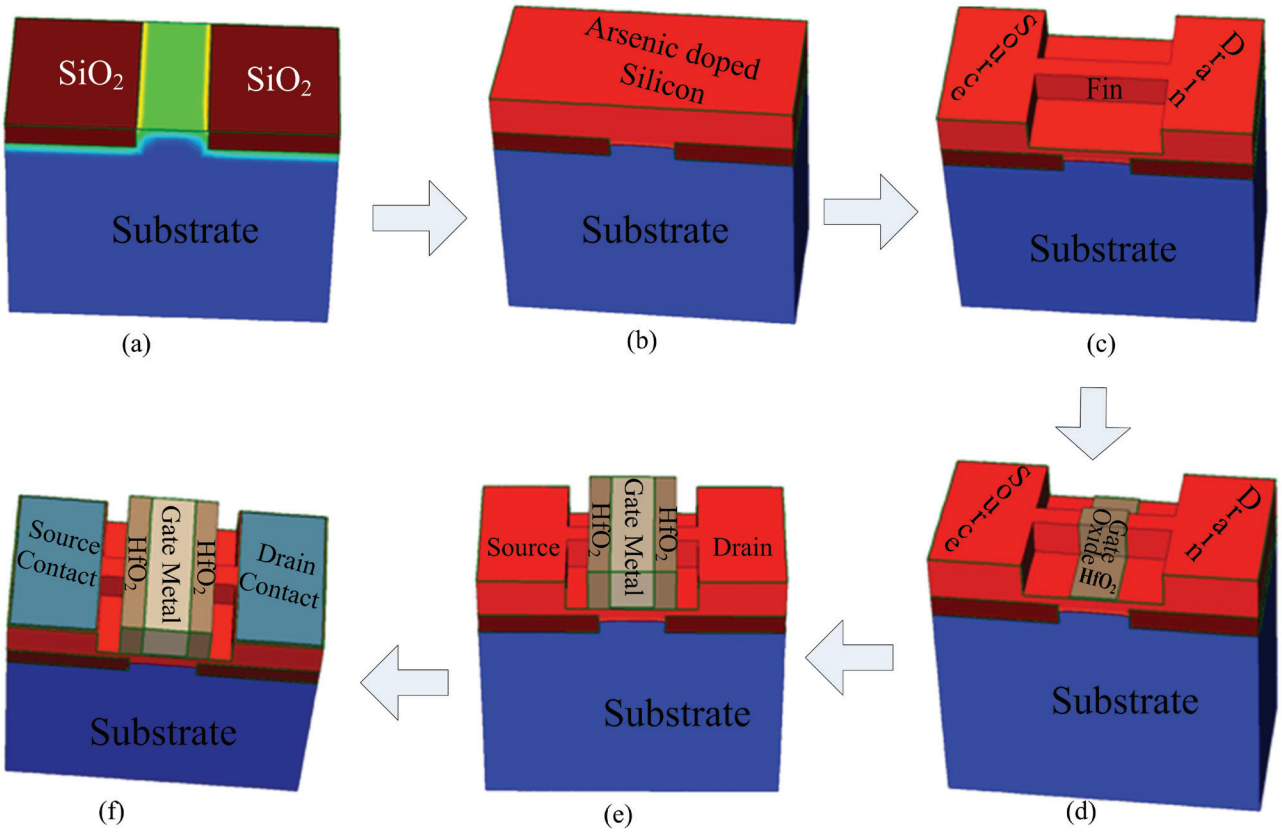

Figure 2: The process flow of the proposed HSJLT using Sprocess, device structure (a) after deposition of the buried oxide (b) after epitaxial growth of silicon for fin (c) after definition of the fin (d) after gate oxide (HfO_2) deposition (e) after gate metal and spacer deposition (f) after contact definition

such as transverse field (to account for degradation at interfaces), high field saturation (to account for velocity saturation effect), and doping dependence (to account for impurity scattering effect), are considered along with default carrier transport model for the device simulation. Shockley – Reed – Hall (SRH) recombination and Auger recombination models are included to account for the recombination of electrons and holes. Old-slotboom band-gap narrowing model is incorporated due to the high doping of the channel. The self-heating effect is accounted for by the inclusion of Auger recombination models, SRH (temperature dependent), and the thermodynamic model for carrier transport. The simulator is verified by the excellent fitting of transfer characteristics of SOI junctionless transistor with the experimental data presented in [12]. Figure. 3 shows the calibration of simulation results with experimental data.

Table 1: Device parameters and doping profiles.

Parameter	JLT	HJLT	HSJLT
Gate length (L_g)	20nm	20nm	20nm
Fin height (H_{fin})	20nm	Hfin–UTB = 16nm	Hfin–UTB = 16nm
Fin width (W_{fin})	10nm	10nm	10nm
Effect oxide thickness (EOT)	0.9nm (HfO_2)	0.9nm (HfO_2)	0.9nm (HfO_2)
Ultra-thin body (UTB) thickness	-	4nm	4nm
Spacer length	10nm (HfO_2)	10nm (HfO_2)	10nm (HfO_2)
Selbox length (L_{SELBOX})	-	-	10nm to 40nm
BOX thickness	10nm	10nm	10nm
Fin dopants (Arsenic)	1 X $10^{19}cm^{-3}$	1 X 10^{19} cm^{-3}	1 X 10^{19} cm^{-3}
Substrate dopants (Boron)	1 X 10^{15} cm^{-3}	1 X 10^{15} cm^{-3}	5 X 10^{18} cm^{-3}
Gate metal workfunction (GWF)	4.72eV	4.87eV	4.7eV

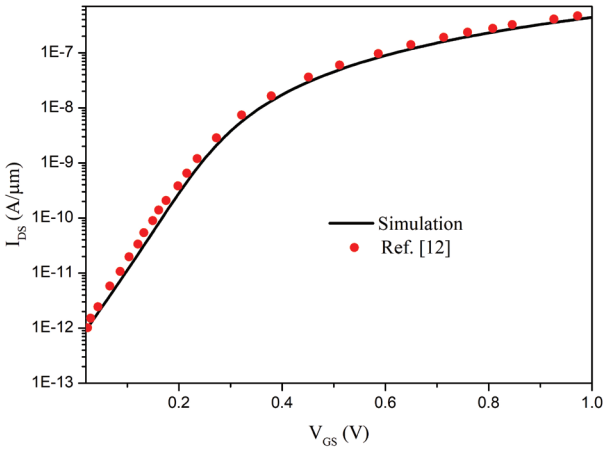

Figure 3: Calibration of I_{DS} – V_{GS} characteristics of the SOI junctionless transistor with the experimental data [12] at V_{DS} = 1V and L_g = 1μm.

3 Results and Discussions

Figure 4 shows a comparison of the transfer characteristics of the three device structures calibrated to the same I_{OFF}. Figure 4 shows that the HJLT and the HSJLT deliver maximum drain current due to the added advantage of UTB and fin structures. HSJLT delivers more drain current than HJLT because of the lower threshold voltage (V_{TH}) and low GWF.

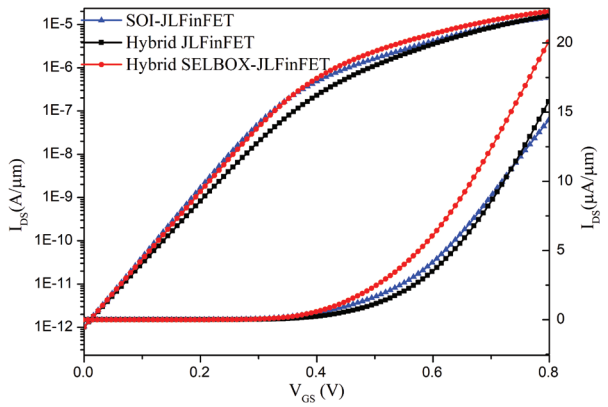

Figure 4: Comparison of transfer characteristics of SOI-JLFinFET, hybrid JLFinFET, and hybrid SELBOX-JLFinFET at L_{SELBOX} = 20nm, V_{DS} = 0.8V and calibrated to same I_{OFF} = 1pA.

3.1 DC performance of HSJLT

In this section, the DC performance of the HSJLT is studied for different SELBOX lengths (L_{SELBOX}) at the same V_{TH}. The variations of ON current (I_{ON}), I_{OFF}, sub-threshold slope (SS), DIBL, lattice temperature, and R_{TH} in HSJLT are presented for different L_{SELBOX} and compared with the conventional and hybrid JLTs.

Figure 5 shows the variation of I_{ON} with the increase in L_{SELBOX}. L_{SELBOX} is the gap between the edges of the BOX material shown in Figure 1(c). As L_{SELBOX} increases, the I_{ON} of the HSJLT decreases due to the penetration of the depletion region into the active area. HJLT is a particular case of HSJLT, in which the L_{SELBOX} is zero. In hybrid transistors, the conduction of current is due to UTB transistor and fin transistor, and the UTB transistor turns on earlier than the fin transistor [6]. For the same threshold voltage, the GWF required for HSJLT is lower than the HJLT due to the depletion region provided by the SELBOX structure. Comparatively low GWF of HSJLT makes its fin transistor to turn early when compared to the fin transistor of HJLT, due to which the I_{ON} is less in HJLT when compared to HSJLT for L_{SELBOX} being < 40nm.

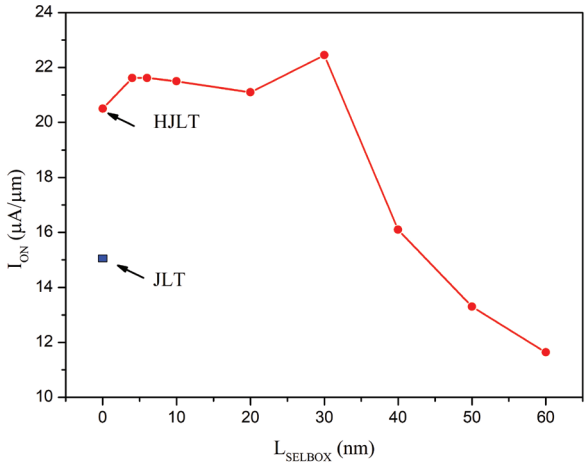

Figure 5: Variation of I_{ON} for different L_{SELBOX} of HSJLT at L_g = 20nm, V_{DS} = 0.8V, and V_{GS} = 0.8V.

Figure 6 shows the variation of I_{OFF} and I_{ON}/I_{OFF} for different L_{SELBOX}. I_{OFF} decreases as L_{SELBOX} increases due to the tight control of the GWF at the top and the depletion region at the bottom of the planar transistor [17].

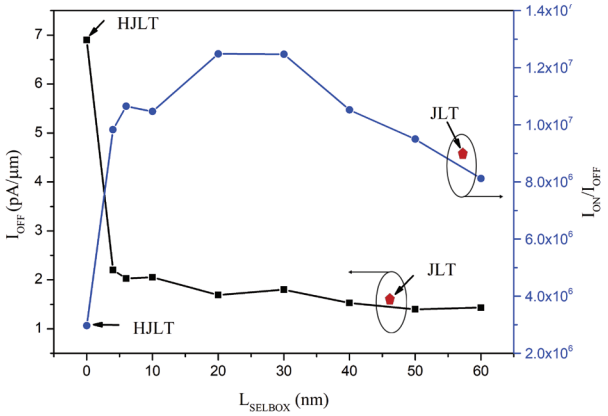

Figure 6: Variation of I_{OFF} and I_{ON}/I_{OFF} for different L_{SELBOX} of HSJLT at L_g = 20nm, V_{DS} = 0.8V.

Initially for L_{SELBOX} < 30nm, I_{ON}/I_{OFF} ratio increases with an increase in L_{SELBOX} and this ratio decreases for L_{SELBOX} > 30nm because I_{ON} drops significantly compared to I_{OFF}.

Figure 7 and Figure 8 show the variation of the SS and DIBL for different L_{SELBOX} of HSJLT. SS and DIBL decrease as the L_{SELBOX} increases due to the increase in gate control over the active region caused by an effective increase in the depletion region provided by the SELBOX at the bottom of the UTB transistor. SS and DIBL in HJLT are high because of non-uniform V_{TH} [6].

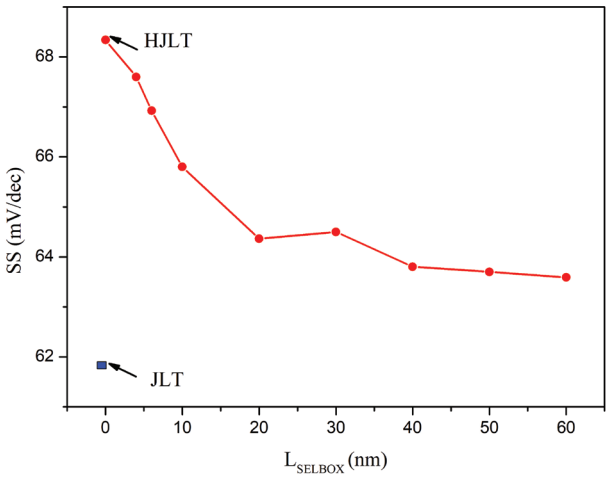

Figure 7: Variation of SS for different L_{SELBOX} of HSJLT at L_g = 20nm, V_{DS} = 50mV.

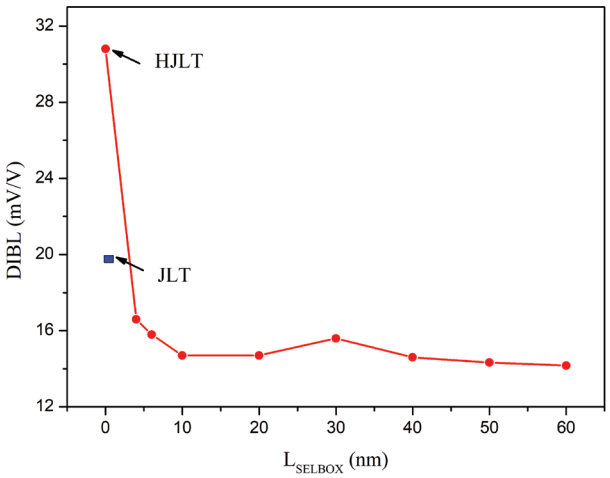

Figure 8: Variation of DIBL for different L_{SELBOX} of HSJLT at L_g = 20nm, $V_{DS,linear}$ = 50mV, $V_{DS,saturation}$ =0.8V.

Figure 9 and Figure 10 depict the variation of thermal resistance (R_{TH}) and lattice temperature for different L_{SELBOX}. Thermal resistance can be used to measure the immunity to self-heating of the device; more RTH, less immunity to self-heating. R_{TH} depends on the power dissipated ($P_{dissipated}$ = V_{DD} x I_D) and lattice temperature ($T_{lattice}$), as shown in Eq. (1). Thermal resistance and lattice temperature decrease with an increase in L_{SELBOX}. An increase in LSELBOX results in an increase in the cross - section area for heat to dissipate into the substrate. In conventional JLT, the lattice temperature is lower compared to hybrid SELBOX - JLTs due to the former transistor's low drain current.

$$R_{TH} = \frac{(T_{lattice} - 300)}{P_{dissipated}} \quad (1)$$

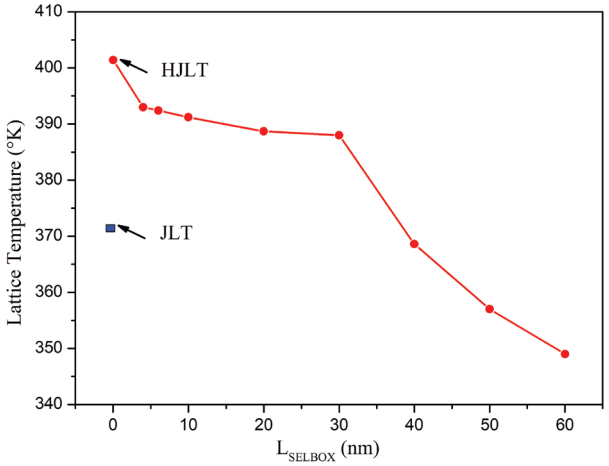

Figure 9: Variation of lattice temperature for different L_{SELBOX} of HSJLT at L_g = 20nm, V_{DS} = 0.8V, V_{GS} = 0.8V.

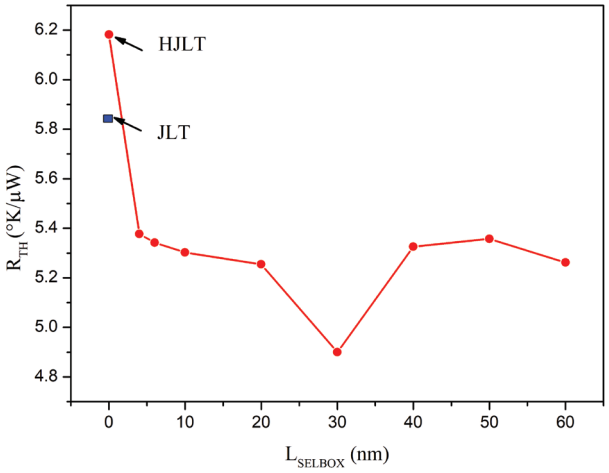

Figure 10: Variation of thermal resistance for different L_{SELBOX} of HSJLT at L_g = 20nm, V_{DS} = 0.8V, V_{GS} = 0.8V.

From the simulation results discussed in section 3.1, it can be observed that the HSJLT exhibits a better performance at $L_{SELBOX} \approx L_g$, i.e., 20nm. It exhibits high I_{ON}, improved DIBL, and low R_{TH} when compared to conventional JLT.

3.2 Analog Performance of HSJLT

This section presents the analog performance of HSJLT at L_{SELBOX} = 20nm. The analog figure of merits (FOM),

such as transconductance (g_m), unity gain frequency (f_T), transconductance generation factor (TGF), early voltage (V_{EA}), and intrinsic gain (A_0) of HSJLT, are compared with conventional and hybrid JLTs.

Figure 11 shows the transconductance variation concerning the change in the gate voltage of the three devices for the same I_{OFF}. The transconductance of HSJLT is higher than conventional and hybrid JLTs because of the high-low field mobility of the former transistor. The higher the g_m, the better the device's analog performance. Figure 12 shows the variation of the transconductance generation factor of the three devices with the change in I_{DS}. TGF is the measure of the efficiency of the transistor to convert the drain current into transconductance; it also indicates the region of operation of the device [21]. From Figure 12, it can be observed that HSJLT exhibits a higher TGF than conventional and hybrid JLTs at the same drain current when the devices are in moderate or strong inversion (i.e., I_{DS} > 1E-7 A/μm).

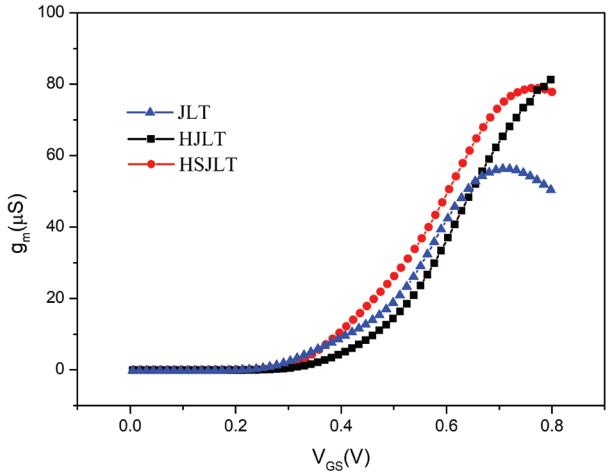

Figure 11: Transconductance variation of JLT, HJLT, and HSJLT with a change in the gate voltage.

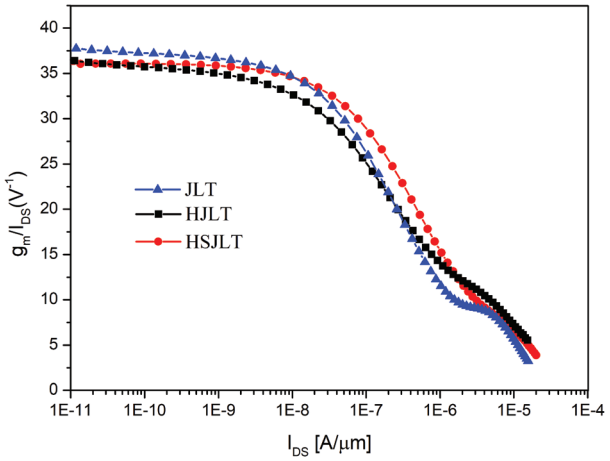

Figure 12: TGF as a function I_{DS}/(W/L) in JLT, HJLT, and HSJLT.

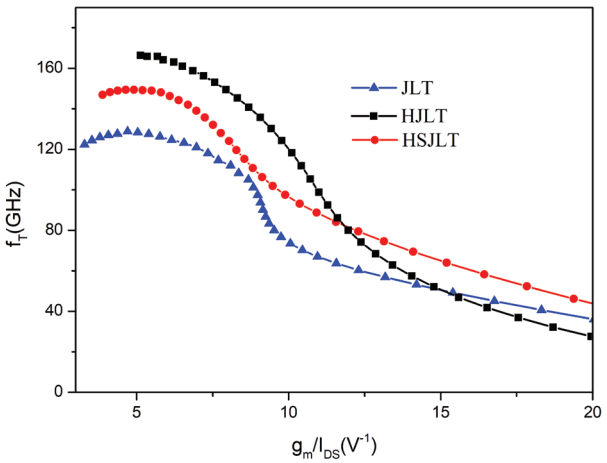

Figure 13: Variation of f_T as a function of TGF in JLT, HJLT, and HSJLT.

Figure 13 shows the variation of f_T as a function of g_m/I_{DS}. f_T depends on the total gate capacitance and transconductance, as shown in Eq. (2). HSJLT exhibits higher f_T than conventional JLT, but lower f_T than HJLT at moderate or strong inversion (i.e., g_m/I_{DS} < 10) due to the large gate capacitance of theHSJLT, as shown in Figure 14, and dipping of the transconductance. In deep-strong inversion (i.e., 10< g_m/I_{DS} >20), f_T of HSJLT is higher when compared to the other two devices because of higher g_m.

$$f_T = \frac{g_m}{2\pi C_{gg}} = \frac{g_m}{I_{DS}} \bullet \frac{I_{DS}}{2\pi C_{gg}} \quad (2)$$

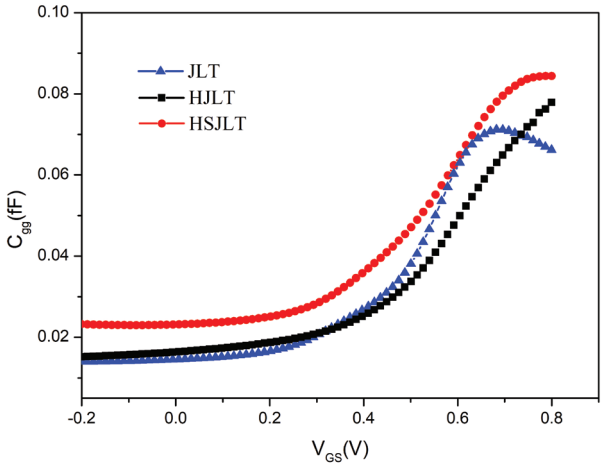

Figure 14: Gate capacitance dependence on the gate voltage in JLT, HJLT, and HSJLT.

Figure 15 shows the variation of early voltage (V_{EA}) as a function of TGF for JLT, HJLT, and HSJLTs. V_{EA} is the drain current - to - drain conductance (g_d) ratio and is an important analog performance metric as it determines the transistor's intrinsic gain if TGF multiplies it.

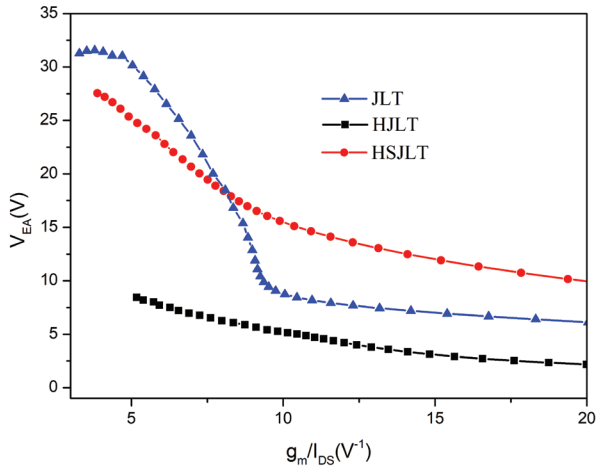

Figure 15: Early voltage dependence on the TGF in JLT, HJLT, and HSJLT.

It can be observed from Figure 15 that in a moderate or strong inversion region, conventional JLT has larger V_{EA} than the HSJLT, because of the low drain conductance of the conventional JLT. In a deep-strong inversion region, HSJLT exhibits higher V_{EA} than conventional JLT, due to the high drain current and nearly the same drain conductance as shown in Figure 16.

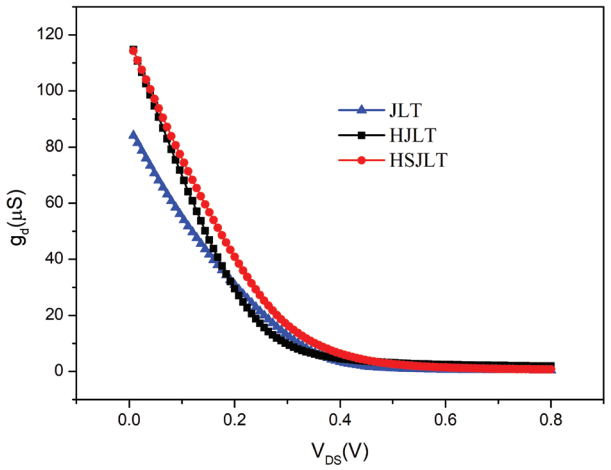

Figure 16: Drain conductance versus drain voltage of JLT, HJLT, and HSJLT.

Figure 17 shows the variation of intrinsic gain (A_0) as a function of TGF. Due to better transconductance generation factor and early voltage, conventional JLT provides high intrinsic gain compared to HSJLT in moderate or strong inversion region. HSJLT has a high intrinsic gain in the deep - strong inversion region than the other two devices.

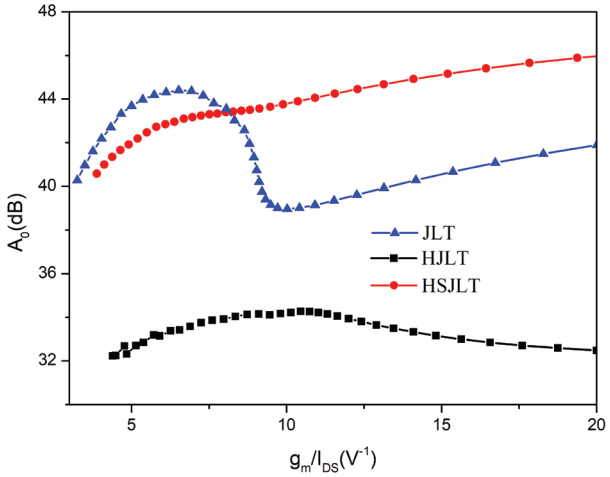

Figure 17: Variation of intrinsic gain in JLT, HJLT, and HSJLT as a function of TGF.

4 Conclusions

In this paper, the DC characteristics and the analog performance of the proposed HSJLT are presented. This paper illustrates the impact of variation in L_{SELBOX} of the proposed structure on the I_{ON}, I_{OFF}, SS, DIBL, and thermal resistance. It is found from the simulation results that the proposed device architecture shows better DC performance for $L_g \approx L_{SELBOX}$. Within the same device area, the proposed device delivers 1.43 times higher drain current compared to conventional JLT due to combined technologies (UTB, FinFET, SELBOX). Simulation results show that the hybrid SELBOX- JLFinFET exhibits better immunity to self-heating when compared to conventional and hybrid JLFinFETs. The analog figure of merits, such as TGF, early voltage, and intrinsic gain, is evaluated through the simulations. It can be concluded from the simulation results that the hybrid SELBOX-JLFinFET is an option for high-performance applications due to higher I_{ON} and it exhibits better g_m/I_D, f_T, V_{EA} and intrinsic gain than the conventional and hybrid JLFinFETs.

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Arrived: 01. 11. 2018
Accepted: 26. 03. 2019

Original scientific paper
https://doi.org/10.33180/InfMIDEM2019.105

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 1(2019), 33 – 42

Idle Noise Reduction of a Parametric Acoustic Array Power Driver

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Abstract: Parametric acoustic arrays (PAA) have progressed from specialized niche applications to commercially available audio solutions in the last two decades. Their primary advantage is their incredible directivity and their main disadvantage is low conversion efficiency of the primary ultrasonic waves into audible sound. This paper presents a noise analysis of a practical implementation of a directional audio system. The system is comprised of a modulator, a D-class audio amplifier, and an emitter consisting of 97 commercially available piezoelectric ultrasonic transducers. The designed system exhibited an uncomfortable level of idle noise at the maximum volume level. The analysis of the signal path and all the noise sources revealed that the most critical component was the modulator, and a solution was devised which provided a 16 dB improvement of the carrier to noise ratio.

Keywords: PAA, Parametric Acoustic Array, Directional Sound System, Ultrasonic, noise, PZT transducer

Zmanjšanje lastnega šuma ojačevalnika in modulatorja za parametrično akustično polje

Izvleček: Parametrična akustična polja (PAP) so se v zadnjih dveh desetletjih razvila od specialnih nišnih aplikacij do komercialno dostopnih avdio sistemov. Njihova poglavitna prednost je izredna usmerjenost zvoka, glavna slabost pa nizka učinkovitost pretvorbe primarnega ultrazvočnega valovanja v slišni zvok. V tem prispevku je predstavljena analiza šuma praktične realizacije usmerjenega avdio sistema. Sistem sestavljajo modulator, avdio ojačevalnik razreda D in ultrazvočni oddajnik, sestavljen iz sedemindevetdesetih komercialno dostopnih piezoelektričnih ultrazvočnih pretvornikov. Zasnovani sistem je pri maksimalni nastavitvi glasnosti oddajal neprijetno visok nivo lastnega šuma. Analiza signalne poti in vseh možnih virov šuma je pokazala, da je najbolj kritična komponenta analogni množilnik. Na podlagi analize smo zasnovali rešitev, ki je izboljšala razmerje med velikostjo nosilca in šuma za 16 dB.

Ključne besede: PAP, parametrično akustično polje, usmerjeni zvočni sistem, ultrazvočni, šum, PZT pretvornik

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1 Introduction

Parametric acoustic arrays (PAA) were first introduced by Westervelt in 1963 [1]. Due to their high directivity and almost non-existent side lobes, many applications have been developed using PAA ranging from underwater applications [2, 3], sediment exploration [4], communications [3, 5, 6], to medical applications [7]. In the last two decades, tremendous progress has been made in the field of PAAs in air to the point where there are multiple commercial solutions available for highly directive sound systems [8–10]. The two main challenges that each PAA system must overcome are the low conversion efficiency of the high frequency primary waves into secondary audible acoustic waves and the distortion of the desired signal. Since high ultrasound amplitudes are necessary to achieve the desired audio levels, noise can become a problem and care must be taken to keep it below the hearing threshold.

Conversion efficiency of the high frequency ultrasonic sound beam into audible sound is very low. To achieve sufficient volume of audible sound, the volume of the ultrasonic beam has to be very high and the signal source needs to be sufficiently powerful. The A and AB-class amplifiers are not very efficient, and therefore not well suited for this type of sound source. The D-class amplifiers with their high efficiency are a much better choice. The impedance of most ultrasonic transducers at resonant frequency has a very pronounced capacitive character, which requires a high reactive current in addition to the active current. The reactive current dramatically increases the losses of the linear power am-

plifiers of both classes. D-class amplifiers employ pulse width modulation (PWM), nearly lossless switches, and an appropriate filter to achieve the same results as linear amplifiers, but with much lower losses. These amplifiers feature high efficiency for resistive, reactive or combined loads. On the other hand, D-class amplifiers can introduce noise into the system [11], especially if the PWM frequency is not considerably higher than the bandwidth of the amplified signal.

We designed our own directional sound system based on double sideband amplitude modulation (DSB-AM) using low cost ultrasonic piezoelectric ceramic transducers. The first version of the system exhibited quite high idle noise which was particularly noticeable at the maximum volume setting. Our initial noise analysis and measurements of the PAA power driver have already been presented in brief at the 50th MIDEM conference [12]. In this paper an updated and more detailed account of the driver and its improvement is given. A short description of the operation principle of PAAs is followed by an overview of available ultrasonic transducers suitable for this purpose. Section 4 describes the electronics of the driver. Section 5 analyzes the noise performance of the electronics, and describes the changes made to the design. Measurement results and conclusions are given in the last two sections.

2 Operation principle

A parametric acoustic array is created by emitting an intense and highly directed ultrasonic beam consisting of a carrier wave and signal components introduced by one of the various modulation types [13]. The carrier interacts with other spectral components of the ultrasonic beam due to the nonlinearity of air at high acoustic sound pressure levels (SPL) and generates new spectral components along the ultrasonic beam.

These secondary waves contain audible spectral components related to the difference between the carrier and side bands. The nonlinearity of air also generates higher inaudible frequencies which are quickly absorbed due to the high absorption coefficient of air at high frequencies. Thus the ultrasonic source creates a beam of ultrasound which acts as a virtual array of sound sources (Fig. 1).

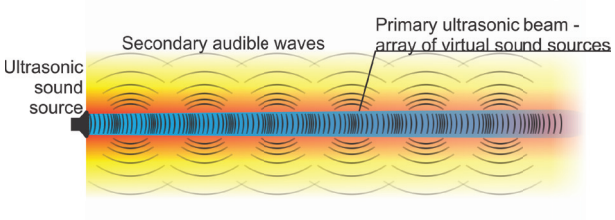

Figure 1: Visualization of the PAA.

Berktay devised a simple equation in 1965 [6] to describe the time dependent pressure of low-frequency secondary waves in the far-field

$$p(t') = p_0^2 \frac{\beta a^2}{16\rho_0 c_0^4 z\alpha_0} \cdot \frac{d^2}{dt'^2} E^2(t') \tag{1}$$

where $E(t')$ is the envelope of the modulated ultrasonic sound pressure, p_0 is the pressure source amplitude, β is the nonlinearity of the medium, which is 1.2 for air, a is the source radius, ρ_0 is the medium density, c_0 is the speed of sound in the medium, z is the distance from the source along the axis of the beam, α_0 is the sound absorption coefficient of the medium for the carrier frequency, and t' is retarded time

$$t' = t - z / c_0 \tag{2}$$

Ten years later Merklinger [14] upgraded Berktay's expression to account for nonlinear attenuation at higher ultrasound intensities. For SPL of the primary beam exceeding 120 dB, with 0 dB = 20 µPa, Merklinger's relation can be linearized to

$$p_s(t') \propto p_0 \frac{d^2}{dt^2} |E(t')| \tag{3}$$

whereby the less important constants have been omitted for the sake of clarity. According to (3) the level of secondary sound becomes linearly proportional to the second time-derivative of the envelope of the modulated ultrasound carrier. This linearized relation in combination with the simplicity of design is the reason that simple double sideband amplitude modulation (DSB-AM) is frequently used in PAAs for audio reproduction.

We can report that the perceived quality of sound reproduction we achieved using the DSB-AM was much better than expression (1) and the work of Yoneyama [15] would suggest. However, in the case of lower primary wave intensities the perceived sound is noticeably impaired, requiring nonlinear preprocessing of the envelope to compensate for the squaring in (1) as suggested in [13, 15]. Hearing tests using a computer generated square rooted envelope of speech and music demonstrated substantially improved quality of sound reproduction at the lower ultrasonic carrier levels. The designed driver is intended for louder reproduction, which requires a high ultrasound level of the carrier (SPL $\approx$ 120 dB), therefore simple DSB-AM is employed to minimize costs and the physical dimensions of the device. The high SPL of the carrier ensures that the airborne demodulation process is ruled by Merkliger's relation (3), which does not include the square of the

envelope waveform, and therefore does not cause high total harmonic distortion (THD).

3 Ultrasonic sound source

Ultrasonic sound waves in the air are usually generated by piezoelectric or electrostatic transducers. The commercially available electrostatic transducers we tested were not suitable for PAAs. Electrostatic transducers require high driving voltages with a high DC bias. The tested transducer achieved an SPL of 115 dB at 50 kHz at the highest combined voltage of 300Vpk-pk + 100 VDC.

The advantages of electrostatic transducers with respect to other types of transducers are wide bandwidth, insensitivity to overload, and a narrow beam angle. The drawbacks are high driving voltage and DC bias, their high price, and the small number of manufacturers.

Piezoelectric transducers use piezo ceramics or piezoelectric polymers in the form of thin foils. Only the ceramic transducers are commercially available, so the power amplifier has been designed for driving a variable number of commercially available piezoelectric transducers.

The mechanical construction of a piezoelectric ceramic transducer is shown in Fig. 2. The active element is a bimorph of Lead Zirconate Titanate (PZT) ceramics. The two PZT layers are poled differently [16], so that the applied voltage causes one layer to shrink while the other expands. The center of the bimorph disc is thus displaced vertically up or down depending on the polarity of the voltage. The mechanical properties of the materials used, as well as their physical dimensions, determine the resonant frequency and bandwidth of the transducer.

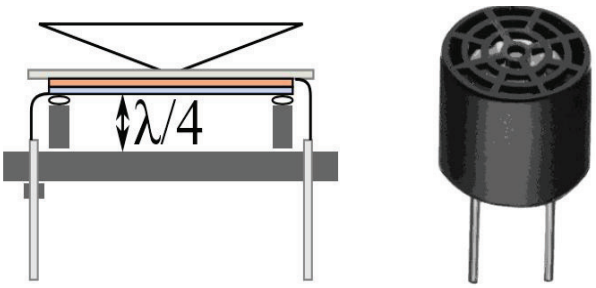

Figure 2: Cross-section and appearance of the utilized PZT bimorph transducer.

These transducers can continuously transmit an SPL of about 120 dB at 40 kHz when driven by 10 V_{RMS}. The PZT bimorphs we used have a small bandwidth and a maximum driving voltage of 20 V_{RMS}. Internal losses cause heat and mechanical fatigue which irreversibly destroy the weakest part of the transducer, namely the joint between the top metal plate and the acoustic cone. When the joint breaks, the light metal cone becomes loosened and the acoustic coupling between the transmitter and the air is lost. Such destruction alters the impedance at the electrical terminals of the transducer which can lead to an increase of the driving voltage if resonant filtering is used.

Both electrostatic and piezoelectric polymer film transducers are less sensitive to overloading and have a greater bandwidth than PZT bimorphs, but require high driving voltages. In addition, commercially available electrostatic transducers do not achieve the desired acoustic pressure level required for PAAs unless they are driven with very high voltages of 400 V_{PP}. Piezoelectric film transducers require lower driving voltages - typically about 100 V_{RMS} - to achieve a sufficient SPL of the ultrasonic carrier, but are not available as commercial components.

3.1 PZT bimorph electrical model

The structure of the PZT transducer shown in Fig. 2 is similar to the structure of a quartz crystal oscillator. Metallic electrodes on both surfaces of the PZT ceramics with very high permittivity ε_r form a physical capacitor C_p between the terminals. The electromechanical reaction of the piezoelectric disc, material losses and transmitted acoustic power are modeled by a serial RLC network. The electrical equivalent network of piezoelectric transducer is shown in Fig. 3. The parallel capacitance C_p is measured between the terminals at 1 kHz and is usually specified by the manufacturer along with other relevant data. The plot in Fig. 4 shows the measurement of the complex admittance $Y(f)$ of the PZT transducer used in the ultrasonic transmitter. The trajectory in the complex plane was measured with a HP 3589A spec-

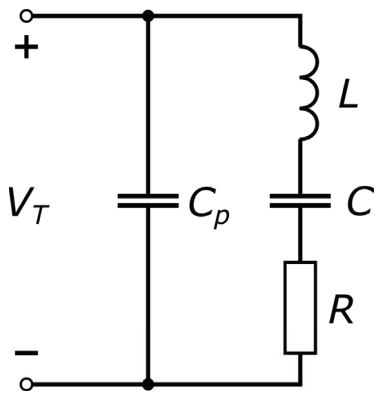

Figure 3: Equivalent electrical model of the PZT ceramic transducer

trum/network analyzer and an additional linear power amplifier which provided the required driving voltage of 10 V_{RMS}. Two sets of element values of the transducer electrical model (Fig. 3) are shown in Table 1. One set is obtained from the complex impedance plot from the datasheet [17], which was acquired using a test voltage of 1 V_{RMS}, the other is calculated from the measured plot shown in Fig. 4.

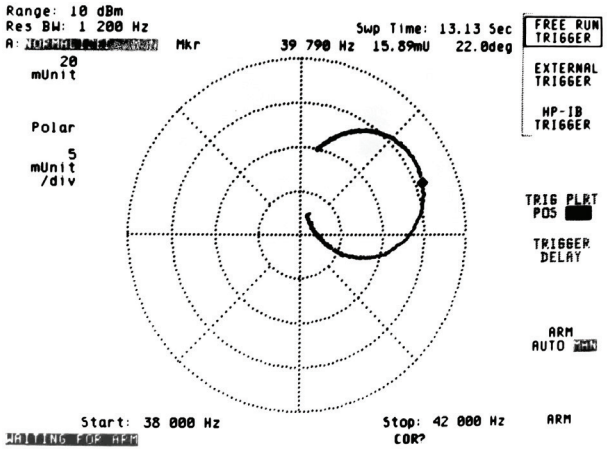

Figure 4: Vector plot of the transducer admittance $Y(f)$ from 38 kHz to 42 kHz (V_T = 10 V_{RMS})

Table 1: Equivalent circuit element values for Pro-Wave 400ST16P

Data source	V_T	C_p [nF]	R [Ω]	L [mH]	C [pF]
Data sheet	1 V_{RMS}	2.4	760	93	167
Measurement	10 V_{RMS}	1.9	665	81	197

Slight differences between the values are expected and come from device tolerances and different driving voltages. The actual operating point of the transmitter varies between 0 and 10 V_{RMS}, depending on the volume setting. The ultrasonic transmitter of the designed system shown in Fig 5 consists of 97 400ST16P piezoelectric transducers (Pro-Wave El. Corp.) arranged in a circle.

Figure 5: Photograph of the PZT ultrasonic transmitter

4 Modulator/amplifier

The modulator/amplifier system consists of (Fig. 6):
- Input amplifier and signal conditioner,
- Low THD 40 kHz quadrature oscillator,
- Integrated analogue multiplier with an adder,
- Differential output amplifier with a DC blocking filter,
- D-class power amplifier,
- LC output filter, and
- Power supply (not shown).

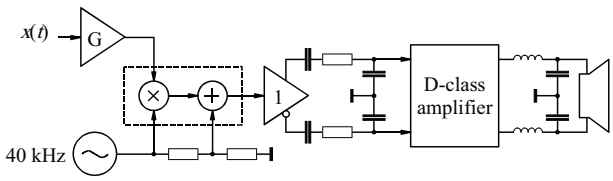

Figure 6: Main building blocks of the modulator/amplifier system

The amplitude of the input signal $x(t)$ is adjusted within the frequency range between 50 Hz and 20 kHz, by a two-stage preamplifier, shown as an amplifier with gain G in Fig. 6. If a stereophonic sound source is applied at the driver input, the two signals are added together in the first stage of the preamplifier. The ultrasonic carrier frequency is generated by a quadrature oscillator consisting of two low-noise operational amplifiers. This is a low cost solution with stable frequency that can be adjusted by a trimmer. The frequency drift of the 40 kHz carrier over the temperature interval ±30°C is within ± 150 Hz, which is much less than the specified center frequency tolerance Δf_0 = ±1 kHz of the selected PZT transducers. Amplitude stabilization is implemented according to the guide lines [18] for low harmonic distortion. The higher harmonic components lie far outside of the transmitting frequency band around the carrier but nonlinearity of the multiplier and action of switch mode power amplifier can generate intermodulation components in the AM signal frequency band.

The double sided AM which has proven to be suitable for PZT transducers is implemented by an AD633, which contains an analog four quadrant multiplier and an adder. The AM signal is obtained by adding the DSB modulated signal, which appears at the multiplier output to the carrier

$$y(t) = A\cos\omega_c t\,[1 + m\,x(t)] \tag{4}$$

where *A* is the carrier amplitude and *m* is the modulation index. The expression in brackets is the envelope function *E*(*t*), which is proportional to the instantaneous carrier amplitude.

A D-class power amplifier is used to avoid large heat sinks and the demanding power supply required by linear power amplifiers. The complex admittance $Y(\omega_C)$ of the transmitter at the carrier frequency, which is also the resonant frequency of PZT transducers, can be approximated by

$$Y(\omega_C) = \frac{n}{R} + j\omega_C n C_p \tag{5}$$

where *R* and C_p are the model parameters of Fig. 3 given in Table 1, while *n* is the number of transducers in the transmitter. The actual admittance of the load for *n* = *97* transducers at the carrier frequency of 40 kHz is $Y(\omega_C)$ = (146 + j46) mS, which corresponds to an impedance of 6.53 Ω ∠ -17.7°. This means that the current through the resistance, which reflects the acoustic load, is accompanied by the reactive current through the parallel capacitance of the transducer electrodes. This current, whose magnitude is roughly a third of the current through the acoustic load, has to be delivered by the output stage. If an AB-class amplifier would be used, it would dissipate 18 W just for the 10 V_{RMS} carrier at the output. This calculation was made for the supply voltages of ± 24V which would be required for achieving the maximum allowed transmitter voltage of 20 V_{RMS} at 100 % modulation.

D-class amplifiers are much more efficient than linear amplifiers, which usually operate in an AB-class, but require a low-pass output filter to suppress the spectral components repeated around multiples of the operating PWM frequency f_{PWM}. In the case of more usual applications, where the maximum signal frequency is 20 kHz, the PWM switching frequency of only 200 kHz in combination with an appropriate low pass filter could suffice. The highest frequency of the AM signal in this case is 60 kHz, which requires a higher switching frequency to achieve sufficient frequency separation between the base band and the first lower side band of the PWM signal.

In the implemented driver, a TAS5613A integrated switching amplifier with f_{PWM} = 400 kHz was used. The filter for the bridge tied load (BTL) topology is symmetrical with respect to ground in order to reduce the electromagnetic interference emissions (EMI) from the transmitter leads.

A simplified asymmetrical model of the output filter and the equivalent electrical model of the ultrasonic transmitter are shown in Fig. 7, where a clear distinction between the filter capacitors inside the driver and the transmitter model is made. The plot in Fig. 8 shows the electrical and acoustic frequency response, reflecting the voltage across the terminals and the resistor voltage, respectively.

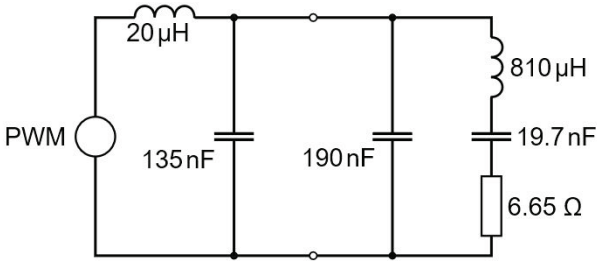

Figure 7: The output filter connected to the equivalent electrical model of the transmitter.

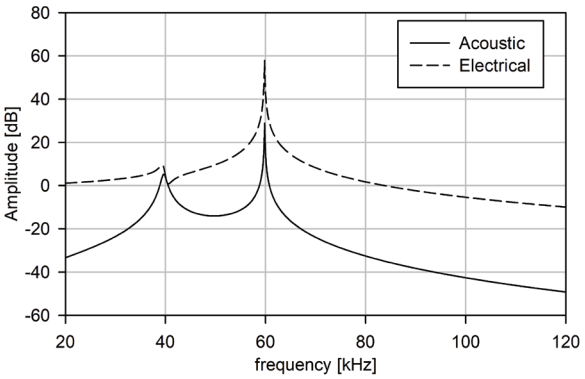

Figure 8: Frequency response of the loaded output filter.

Due to the capacitive nature of the load determined by C_p the frequency response |*H*(*f*)| of the filtering network has a second resonant peak in the spectral region above the base-band of the AM signal, which spans from 20 kHz to 60 kHz, and below the lower margin of the first mirror band at 340 kHz. This part of the spectrum does not contain any PWM spectral components. However, the shape of the acoustic transfer function modifies the noise power spectrum within the pass band of the signal and has an influence on the audible noise.

The BTL configuration of the switching amplifier, which doubles the output voltage swing compared to a single ended configuration, is achieved by inverting the signal at the input of one of the two amplifiers of the switching power driver. The differential output signals are AC-coupled to the switching amplifier as shown in Fig. 6. The inputs of the amplifiers are internally biased and the DC level is adequate providing there is no DC path to the input node. The network shown in the schematics performs much better than a coupling capacitor alone. The resistor in the signal path limits the input

current and adds a real pole in the frequency response of the coupling.

5 Noise source analysis

5.1 Noise analysis of the original system

The suitability of a simple AM and PZT bimorphs for a PAA directional sound system was verified by the hearing tests conducted on the system. The flaws of AM in PAAs mentioned in [13, 16] were not perceived for different audio signals, i.e., music, speech, etc., although high idle noise levels were noticed. Acoustic noise measurements in this particular case would be extremely demanding, because of the very large dynamic range required due to the very high ultrasonic carrier signal. The normal hearing SPL is roughly 40 to 50 dB below the ultrasonic carrier level and the perceivable noise SPL is estimated to be about 40 dB lower than that, depending on the background noise of the surroundings.

The noise spectrum range ($f_C - f_H$, $f_C + f_H$) modulates the carrier amplitude and thus demodulates as audible noise. As a measurable figure of merit we use the ratio between the power of the carrier and the noise, given by

$$CNR = 10\log\frac{C}{N} = 10\log\frac{A^2}{2\cdot S_n B} \tag{6}$$

where *C* is the carrier power, *N* is the in band noise power, *A* is the carrier amplitude, S_n is noise power spectral density, and *B* is the frequency bandwidth.

Within the PAA driver system (Fig. 6) each functional block generates noise that contributes to the final *CNR* at the transmitter. The two low noise JFET operational amplifiers TL071 used in the two-stage input preamplifier have an equivalent input noise of 4 μV from 100 Hz to 10 kHz and a constant noise density of $18\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ above 10 kHz. The contribution of the input noise current is negligible and is not taken into account.

Each of the two stages of the input preamplifier can be represented by the equivalent circuit shown in Fig. 9, where all the noise sources are joined into one equivalent input noise source. The equivalent input noise voltage consists of the amplifiers input noise and all the thermal noise sources:

$$u_{neq} = \sqrt{u_{nTL071}^2 + u_{nR}^2} \tag{7}$$

where u_{nTL071} represents input noise of the operational amplifier and u_{nR} all the thermal noise contributions. Contributions of all the thermal noise sources can be modeled by a single thermal noise source with noise voltage appropriate to the parallel connection of resistors R_1 and R_2 of Fig. 9:

$$u_{nR} = \sqrt{4kBT\frac{R_1R_2}{R_1+R_2}} \tag{8}$$

where *k* represents Boltzmann constant, *B* bandwidth and *T* temperature. Given the equivalent circuit in Fig. 9, the output noise can be calculated as:

$$u_{nout} = u_{neq}\frac{R_1+R_2}{R_1} \tag{9}$$

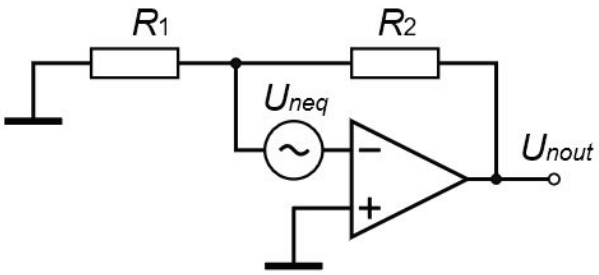

Figure 9: Equivalent circuit applicable to both stages of the input preamplifier.

The noise voltages and relevant data for the two-stage input audio signal conditioner are shown in Table 2.

Table 2: Input amplifier noise voltages (*B* = 20 kHz, *T* = 300 K).

Stage	1	2
R_1	5.0 kΩ	10.0 kΩ
R_2	4.7 kΩ	10.0 kΩ
Thermal input noise	0.9 μV	1.3 μV
Amplifier input noise	4.4 μV	4.4 μV
Equivalent input noise	4.5 μV	4.9 μV
Inverting gain	0.94	1
Output noise	8.7 μV	9.2 μV
Entire output noise	12.7 μV	

The most important noise source in this spectral region is the 1/f noise of the amplifier. Thermal noise is not significant because of the small bandwidth and low input resistances.

The oscillator generates the carrier signal (40 kHz, 3.3 V_{RMS}) and noise with significant noise density in the vicinity of the carrier:

$$c(t) = s_C(t) + n_C(t) \tag{10}$$

where $n_C(t)$ is the carrier signal noise and $s_C(t)$ is the ideal carrier signal:

$$s_C(t) = A \cdot \cos(\omega_C t) \tag{11}$$

The total noise power must be integrated over the 40 kHz band – carrier frequency $f_C \pm 20$ kHz. An equivalent noise voltage of 96 μV was obtained using LTspice and operational amplifier models provided by the manufacturer. This gives a *CNR* of 91 dB at the oscillator output. The result does not include harmonic components because they are outside the frequency range of interest.

The carrier and audio signal are multiplied together and divided by 10 V by the AD633 integrated circuit. The carrier signal is attenuated by a factor of 10 by a resistor divider and added to the product:

$$y(t) = \frac{x(t) \cdot c(t)}{10\ \mathrm{V}} + \frac{c(t)}{10} \tag{12}$$

Both the carrier and the signal each contain their own noise and the multiplication product from (12) contains multiple terms representing noise:

$$\begin{aligned} x \cdot c &= (s_X + n_X) \cdot (s_C + n_C) = \\ &= s_X s_C + s_X n_C + n_X s_C + n_X n_C \end{aligned} \tag{13}$$

where s_X is the ideal input signal, n_X is the signal noise, s_C is the ideal carrier signal, and n_C is the carrier noise. The term $s_X s_C$ is the desired signal, while all other terms represent noise. The product of both noises $n_X n_C$ is very small and can be neglected. When idle noise is considered, the signal is zero and therefore the product of the carrier noise with the signal $s_X n_C$ is also zero. The only term which contributes significantly to the idle noise at the output of the multiplier is the signal noise multiplied by the carrier signal $n_X s_C$, which scales and spreads the carrier noise over the pass-band frequency range $f_C \pm 20$ kHz. Taking into account the scaling factor of 1/(10 V) it contributes:

$$n_{DSB} = \frac{3.3\mathrm{V} \cdot 12.7\ \mu\mathrm{V}}{10\ \mathrm{V}} = 4.2\,\mu\mathrm{V} \tag{14}$$

After the multiplication of the signal with the carrier, the carrier signal attenuated by a factor of 10 is added, which contributes its own noise of 9.6 μV to the output signal. The AD633 itself generates noise with a constant spectral density of $0.8\ \mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ which results in 160 μV of noise within the 40 kHz bandwidth of interest. Particular noise source contributions, the entire output noise and the obtained *CNR* are summarized in Table 3.

Table 3: Multiplier noise sources (B = 40 kHz).

Multiplier output noise	4.2 μV
0.33 V carrier noise	9.6 μV
AD633 output noise	160 μV
Entire output noise	160.3 μV
CNR	66.3 dB

The differential output amplifier noise contributes a similar amount of noise as the first stage of the input amplifier (approximately 5 μV). Compared to the noise present in the signal at this stage it is insignificant and can be safely neglected.

The carrier and accompanying noise are amplified and additional uncorrelated noise is generated by the D-class TAS5613A power amplifier. The gain of the amplifier for a single channel is 22.4, but in the BTL configuration used in this case, the gain is 44.8. The amplitude of the carrier that appears on the transmitter in idle state at full volume is calculated to be 7.4 V_{RMS}, but in reality varies with temperature between approximately 7 and 8.5 V_{RMS}. Taking into account the transmitter impedance at 40 kHz, the calculated carrier voltage results in an apparent output power of 8.4 VA and effective output power of 8.0 W. This level was selected to ensure that the driving voltage never exceeds the limits of safe operation of the power amplifier and the piezoelectric transducers.

The only information the TAS5613 datasheet contains about noise is a THD+N (Total Harmonic Distortion and Noise) parameter expressed in percent. This means the noise and THD at the output depend on signal size. In this specific case, harmonic distortion is not important because the harmonic components lie outside the pass-band of the AM signal. It is possible to separate the THD and N portions of the THD+N parameter with the help of the datasheet. The THD+N parameter drops significantly above 10 kHz because the higher harmonic components of signals with a frequency above 10 kHz lie beyond the audio band. That means that for signals above 10 kHz only noise contributes to the THD+N parameter (Table 4).

By means of careful measurements a third kind of output noise was identified at the output of the power amplifier with the inputs AC-shorted by capacitors. This noise, which is not specified in the data sheet, was measured on the transmitter in the frequency range from 20 kHz to 60 kHz. Table 4 summarizes all the relevant parameters, noise contributions, final output noise and CNR at the transmitter terminals.

Table 4: Power amplifier noise voltages $V_o = C = 7.4\ V_{RMS}$, $P_L = 8.0$ W

THD + N (f > 10 kHz)	0.002% = $2 \cdot 10^{-5}$
Voltage gain	2 × 22.4
Amplified input noise	3.60 mV
Idle output noise (input shorted)	0.49 mV
Generated output noise (carrier)	0.15 mV
Entire output noise	3.63 mV
CNR	66.2 dB

The presented analysis of the sources and propagation of noise reveals that the most important source of noise is the multiplier. The data in Table 4 shows that the noise generated by the power stage is negligible in relation to the amplified input noise. The input and output signals have almost the same *CNR*.

The noise generated by each stage (except the power amplifier stage) is independent of the signal size unless the limits of a stage are exceeded. A general solution to the signal to noise ratio problem is to either decrease the noise or increase the signal amplitude. In this case, the most critical stage regarding generated noise is the AD633 multiplier. There is considerable headroom available with regard to signal size at this stage, while nothing can be done to reduce the noise generated by the AD633. Therefore, the solution would be to increase signal size before it is passed through the multiplier and reduced again just before the power amplifier stage.

5.2 Noise analysis of the improved system

In order to increase the *CNR* at the output of the multiplier, the voltage gain of the second stage of the input amplifier was increased from 1 to 10 and the oscillator output was connected to the summing input of the AD633 directly, without any attenuation to maintain the same modulation depth of the AM signal. The amplitudes of all signals involved are still below the saturation margins of the device. The multiplier output had to be attenuated by approximately a factor of 10 before it could be fed into the power amplifier in order to maintain the same signal levels as before. To achieve the attenuation, the capacitances of both DC blocking networks at the power amplifier input were changed. Due to the sparse value scales of the multilayer ceramic capacitors the capacitive voltage divider attenuates the output voltage to 13% instead of 10% in the pass band between 1 kHz and 1 MHz.

Had the multiplier been the only source of noise, this modification would have resulted in a 20 dB improvement of the *CNR*. Tables 5, 6 and 7 present the noise magnitudes for the input stage, the modulator and the power amplifier, respectively, of the improved system.

The results show that the *CNR* at the output of the modulator is indeed improved by 18.5 dB, however the *CNR* at the output of the power amplifier is slightly less improved, namely, by only 15.9 dB, since the noise generated by the power amplifier is not negligible anymore.

Table 5: Modified input amplifier noise voltages (B = 20 kHz, T = 300 K).

Stage	1	2
R_1	5.0 kΩ	1.0 kΩ
R_2	4.7 kΩ	10.0 kΩ
Thermal input noise	0.9 μV	0.55 μV
Amplifier input noise	4.4 μV	4.4 μV
Equivalent input noise	4.5 μV	4.4 μV
Inverting gain	0.94	10
Output noise	8.7 μV	48.4 μV
Entire output noise	99.6 μV	

Table 6: Multiplier noise sources (B = 40 kHz).

Multiplier output noise	32.9 μV
3.3 V carrier noise	96 μV
AD633 output noise	160 μV
Entire output noise	189 μV
CNR	84.8 dB

Table 7: Power amplifier noise voltages $V_o = C = 9.7\ V_{RMS}$, $P_L = 13.7$ W.

Amplified input noise	0.55 mV
Idle output noise (input shorted)	0.49 mV
Generated output noise (carrier)	0.19 mV
Entire output noise	0.76 mV
CNR	82.1 dB

6 Measurement results

The design of the analyzed system was focused on the demodulated sound quality, directivity and range. Actual hearing tests revealed the need for a detailed analysis of noise sources. The main difficulty of noise measurements in this particular case was the presence of the large but inaudible carrier. Spectral analyzers have a limited dynamic range, which makes it impossible to measure very small signals when large spectral components are present. To get around this problem, we performed noise measurements with the oscillator disconnected from the rest of the system.

In order to eliminate the on-board oscillator as a possible cause of audible idle noise, the ultrasonic transmitter was tested by using a linear power amplifier and two test signals. One test signal was generated with a function generator and the other by the quadrature oscillator of the designed system. No audible noise was perceived in either case at normal carrier levels.

Measurements were performed with an HP3589A spectrum analyzer. The results of the measurements and theoretical analysis are summarized in Fig. 10. Noise power was calculated from measured power spectrum densities over the frequency band from 20 kHz to 60 kHz. This band contains all frequencies that can modulate the amplitude of the ultrasonic carrier and demodulate into audible sound or noise.

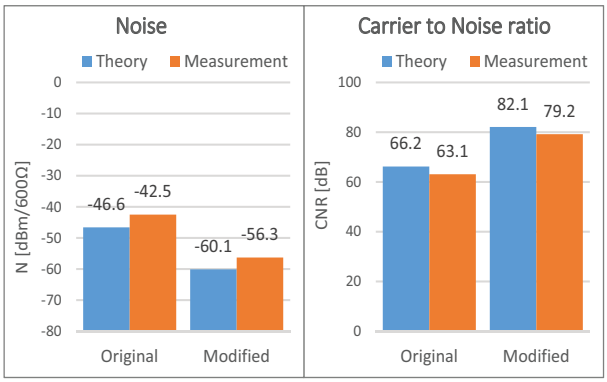

Figure 10: Theoretical and measured Noise (lower is better) and Carrier to Noise ratio (higher is better) before and after the modification.

The theoretical noise powers are lower than the measured ones in both the case of the original and the modified driver. This can be explained by the frequency response of the output filter shown in Fig. 8 which indicates that noise power density that appears on the transmitter terminals is amplified in certain frequency regions. The actual acoustic response is much more limited by the frequency response of the utilized PZT transducers.

The analysis as well as the experimental results revealed the main source of noise and enabled us to minimize its effect on the output signal without modifying the printed circuit board (PCB). This made it possible for the modification to be implemented on the existing production series. The improved version has considerably less perceptible idle noise as well as a slightly larger maximum volume.

7 Conclusions

The designed modulator amplifier system for a PAA resulted in good audio reproduction but exhibited noticeable acoustic noise when idle. We performed a noise analysis of the complete signal path and identified the analogue multiplier as the most significant source of the noise. This noise source is virtually independent of the signal levels, therefore higher signal levels at the multiplier input improve the output signal to noise ratio. The improvement of the device has been achieved by increasing the audio signal amplitude by a factor of 10 before it is fed into the modulator and by reducing it by approximately the same amount on the other side of the modulator. This change was possible without a PCB redesign and could therefore be implemented on the existing production series. The change has resulted in a 16 dB improvement in the *CNR*, which is enough to reduce the idle noise to an acceptable level.

8 Acknowledgments

The author would like to thank M. Ciglar of Ultrasonic d.o.o. for the financial support of the project, A. Levstek for many helpful discussions and S. Beguš for the use of an anechoic chamber.

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Arrived: 31. 03. 2019
Accepted: 15. 04. 2019

Original scientific paper
https://doi.org/10.33180/InfMIDEM2019.106

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 49, No. 1(2019), 43 – 50

Optimization of shunt capacitive RF MEMS switch by using NSGA-II algorithm and uti-liti algorithm

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Abstract: The present paper aimed at designing, optimizing, and simulating the RF MEMS Switch which is stimulated electrostatically. The design of the switch is located on the CoplanarWaveguide (CPW) transmission line. The pull-in voltage of the switch was 2V and the axial residual stress of the proposed design was obtained at 23MPa. In order to design and optimize the geometric structure of the switch, the desired model was extracted based on the objective functions of the actuation voltage and the return loss up-state and also the isolation down-state using the mathematical programming. Moreover, the model was solved by the NSGA-II meta-heuristic algorithm in MATLAB software. In addition, the design requirements and the appropriate levels for designing the switch were obtained by presenting the Pareto front from the beam actuation voltage and also the return loss up-state and isolation down-state. Finally, the RF parameters of the switch were calculated as S11=-2.54dB and S21=-33.18dB at the working frequency of 40GHz by extracting the appropriate parameters of the switch design through simulating a switch designed by the COMSOL Multiphysics software 4.4a and the advanced design system (ADS).

Keywords: RF switch MEMS; Genetic algorithm; uti-liti algorithm; Actuation voltage

Optimizacija šarazitne kapacitivnosti RF MEMS stikala z uporabo algoritmov NSGA-II in uti-liti

Izvleček: Članek predstavlja načrtovanje, optimizacijo in elektrostatično simulacijo RF MEMS stikala. Dizajn stikala je osnovan na CPW prenosni liniji. Za optimizacijo structure stikala so bile uporabljene objektivne funkcije aktuacije napetosti, povratnih izkub v vzbijenem stanju in izolativnosti v izklopljenem stanju. Model je bil rešen z NSGA-II metahevrističnem modelu v MATLABu. Izračunani RF parametri stikala pri delovni frekvenci 40 MHz znašajo S11=-2.54dB in S21=-33.18dB. Parametri so bili določeni s pomočjo COMSOL Mutiphysics programske opreme.

Ključne besede: RF MEMS stikala; generični algoritem; uti-liti algoritem; aktuacijska napetost

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1 Introduction

The Micro-Electromechanical System (MEMS) refers to a technological process used to create integrated systems and components of the complex (or the combination of the electrical and mechanical elements) [1]. In this regard, the MEMS switches are significantly considered due to their efficiency in areas such as fuzzy array systems and switching filters for wireless communication.[2] MEMS switches have low power consumption, very high isolation, very low insertion loss (the RF MEMS switches have the insertion loss of about 0.1 to 100 GHz) and high linear performance as compared to the diodes or FET switches[3]. However, the high actuation voltage and the high switching time are among the weaknesses of the MEMS switches. MEMS switches are of different types, in which series of switches (ohm connection) and parallel switches (capacitance) have various applications. In this sense, they can be used as an ohm (serial switches) and also the capacitive switch (shunt switches) using electrostatic, electromagnetic ,piezoelectric or thermal designs[3]. The electrostatic setup is usually used due to its power consumption

closed to zero, lower performance time, and smaller size [2]. MEMS switches can be used both on micro strip lines and CPW lines of the glass, silicon and GaAs substrates, which are capable of being operated in these configurations up to the frequency of 100 GHz. A dielectric layer has been used in contacting the switch with the transmission line to prevent corrosion and fatigue in metal-to-metal connection [2]. It is worth mentioning that important parameters should be considered in designing MEMS switches. These parameters include the electrostatic actuation voltage, isolation, transmission losses, and operating time[2]. Numerous studies have been conducted on the evaluation of the performance of MEMS switch and its important parameters. As a switch is presented in [4], the return loss of -5.6 dB and an isolation of -24.38dB are obtained from an output voltage of 3.04 V and at a frequency of 40 GHz, using the design of the experiment of. When a switch is presented in[5], the return loss of -3.1dB and an isolation of -15dB are obtained from an output voltage of 7V and at a frequency of 40GHz. When a switch is presented in[6], the return loss of -0.98 dB and an isolation of -17.9dB are obtained from an output voltage of 82V and at a frequency of 20 GHz. Besides, when a switch is presented in[7], the return loss of -0.68 dB and an isolation of -35.78dB are obtained from an output voltage of 23.6V and at a frequency of 40 GHz. Moreover, when a switch is presented in[8], the return loss of -0.8 dB and an isolation of -30dB are obtained from an output voltage of 25V and at a frequency of 40 GHz. Finally, when a switch is presented in [9], from an output voltage of 3V and at a frequency of 40 GHz, using the design of the experiment of. In the present paper, a suitable model was extracted for optimizing the multi-object in the target functions (voltage actuation and RF parameter) of the switch using the mathematical programming method. Then, the proposed model was solved using the NSGA-II[1] meta-heuristic algorithm. In addition, the proposed model was used to achieve a MEMS switch with low electrostatic actuation voltage and improved insertion loss and isolation by choosing the proper structures of width, length, and thickness and, also, using the Pareto front presented for the designed beam spring constant.

The present paper is organized as follows: Section 2 evaluates the switch performance. Section 3 examines the details of the model and presents the Pareto front solution set for the actuation voltage and return loss up-state and isolation down-state by solving the proposed model using the NSGA-II in MATLAB software and the uti-liti algorithm. Finally, section 4 simulates the desired switch using the COMSOL and ADS software and evaluates the necessary parameters such as actuation voltage, operating time, insertion loss and the isolation.

2 MEMS switches performance

2.1 Initial performance

Fig.1 illustrates a parallel MEMS switch. Which is located on the coplanar waveguide and includes two electrodes. The lower electrode is the central transmission line of the waveguide, while the upper electrode is a thin metal sheet, which is suspended on the lower electrode and connected to the lateral conductors of the coplanar waveguide. Further, the thin dielectric layer is covered on the lower electrode to prevent the metal-to-metal connection [10]. In the state up with the bridge in up position, the switch is OFF and shows insertion loss. ON state can be achieved by pulling down the beam in the down position through electro-static actuation. The isolation state is occurred especially when the bridge provides the ground for the float central capacitive area. The electrostatic actuation voltage of the capacitance switches is calculated according to the equation 1:[2]

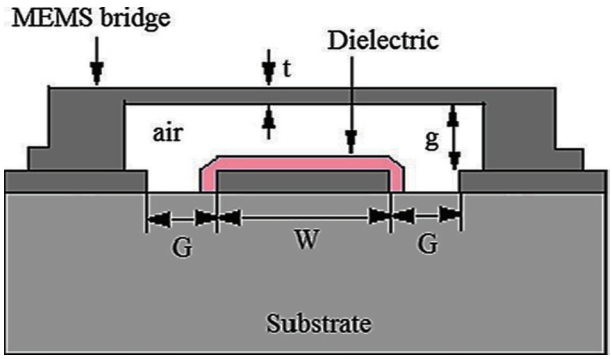

Figure 1: The schematic of the switch

$$V = V\left(\frac{2}{3}g_0\right) = \sqrt{\frac{8k}{27\varepsilon_0 A}g_0^{\,3}} \quad (1)$$

Where ε_0 represents the vacuum permittivity coefficient and indicates the air gap between the suspended bridge and the transmission line, the electrostatic actuation voltage is zero, and shows the beam spring constant. As shown in the equation, the distance ($g_0 = g_{gap}$ + thd) and the area of the switch (A) can be reduced in order to achieve a low spring constant. The S-parameters are first measured in the up-state position data (S_{11}) which is fitted to get the up-state capacitance of the switch. S_{11} is achieved using the equation 2. The S-parameters are first measured in the down-state position data (S_{21}) which is fitted to get the up-state capaci-

[1] *Non-dominated Sorting Genetic Algorithm-II*

tance of the switch. $S_{21}$is achieved using the equations 3 .[11]magnetostatic, piezoelectric, or thermal designs. To\\ndate, only electrostatic-type switches have been demonstrated at 0.1-100\\nGHz with high reliability (100 million to 10 billion cycles

$$S_{11}\left(\text{up state}\right) \simeq \frac{-j\omega c_u z_0}{2+j\omega c_u z_0} \Rightarrow$$

$$\Rightarrow \left|S_{11}{}^2\right| \simeq \frac{\omega^2 Z_0{}^2 \left(\varepsilon_0 Ww\right)^2}{4\left(g_{gap}+\left(\frac{t_d}{\varepsilon_r}\right)\right)^2} \tag{2}$$

$$S_{21}\left(\text{down state}\right) \simeq \frac{2}{2+j\omega c_d z_0} \Rightarrow$$

$$\Rightarrow \left|S_{21}{}^2\right| \simeq \frac{4t_d{}^2}{\omega^2 Z_0{}^2 \left(\varepsilon_0\, \varepsilon_r Ww\right)^2} \tag{3}$$

Where Z_0 implies the impedance of the transmission line which is equal to 50 Ohms, ω is the angular frequency and the C_u and C_d of the capacitor are in up-state and down-state and the C_u and $C_d$are achieved using the equations 4.1 and 4.2:

$$C_d = \frac{\varepsilon_0 \varepsilon r Ww}{t_d} \tag{4.1}$$

$$C_u = \frac{\varepsilon_0 Ww}{g_{gap}+\left(\frac{t_d}{\varepsilon_r}\right)} \tag{4.2}$$

3 RF MEMS switch design

3.1 Principles for mathematical programming

Mathematical programming is based on the problem modelling. In other words, the programming techniques are used to achieve the maximum efficiency and the right decision-making process in terms of optimization and efficiency. Generally, the research techniques in operation are categorized in accordance to observation, definition, modelling, model solving, and model implementing, which should be considered in order to obtain the results of the research. [12] in a mathematical programming technique, four main and important parts should be followed in order to create a proper model of the problem. The objective function, constraints, decision variables, and parameters are the principles for designing a model using the mathematical programming. The solution set of the objective function is called the Pareto front, which is an optimal vector dominating other vectors especially when no similar vectors can be found in the entire solution space.[12] In this sense, the vector is generally called the non-dominated answer, and the set of these points is called the Pareto Front[13]. In order to optimize RF switch MEMS, A multi-objective integer programming model is proposed. The proposed model includes three objective functions: minimizing the actuation voltage and minimizing the return loss up-state and maximizing isolation down-state. Descriptions of objective function, constraints, decision variables, and parameters of the mathematical model are presented in Table 1.

3.2 Objective functions

The objective functions are to minimize the actuation voltage, maximize the isolation and minimize the return loss as defined below:

- Minimizing the actuation voltage. The objective function for actuation voltage is based on the equation (1).
- Minimizing the return loss up-state for the best isolation. The objective function for return loss is based on the equation. (2).
- Maximizing the isolation down-state. The objective function for isolation is based on the equation (3).

The model presented in this paper is shown in equation 5.

Table 1: List of parameters , and decision variables

Parameters				
AL Young's modulus (E)	AL Poisson's ratio (v)	Switch thickness (t)	Frequency of operation (f)	Switch Width(w)
70GPa	0.32	0.877μm	40GHz	80μm
Decision variables				
Spring constant (k)	Switch Length (W)	Dielectric layer thickness (t_d)	Air gap (g_{gap})	

$$Actuation\,voltage:\ \min: Z1 = V = \sqrt{\frac{8k}{27\varepsilon_0 W w}\,g_0^{\,3}}$$

$$Return\,loss\,up-state: Min:\ Z2 = |S_{11}|^2 \simeq \frac{\omega^2 Z_0^{\,2}\left(\varepsilon_0 W v\right.}{4\left(g_{gap}+(\frac{t_d}{\varepsilon_r}\right.} \quad (5)$$

$$Isolation\,down-state: Max: Z3 = |S_{21}|^2 \simeq \frac{4t_d^{\,2}}{\omega^2 Z_0^{\,2}\left(\varepsilon_0\varepsilon_r W\right.}$$

subject.to:

$$\begin{cases} 1N/m \le k \le 1.4N/m \\ 150\mu m \le W \le 200\mu m \\ 1.1\mu m \le g_{gap} \le 1.4\mu m \\ 0.085\mu m \le t_d \le 0.11\mu m \end{cases}$$

3.3 Genetic algorithm

In order to solve the proposed multi-objective model and determine the decision variables, we used the NSGA-II algorithm. It is an evolutionary algorithm by which one is able to find sets of optimal solutions on Pareto-optimal fronts. It has been developed as an efficient algorithm to solve multi-objective optimization problems [14]. The best values for the algorithm's parameters are defined in Table 2.

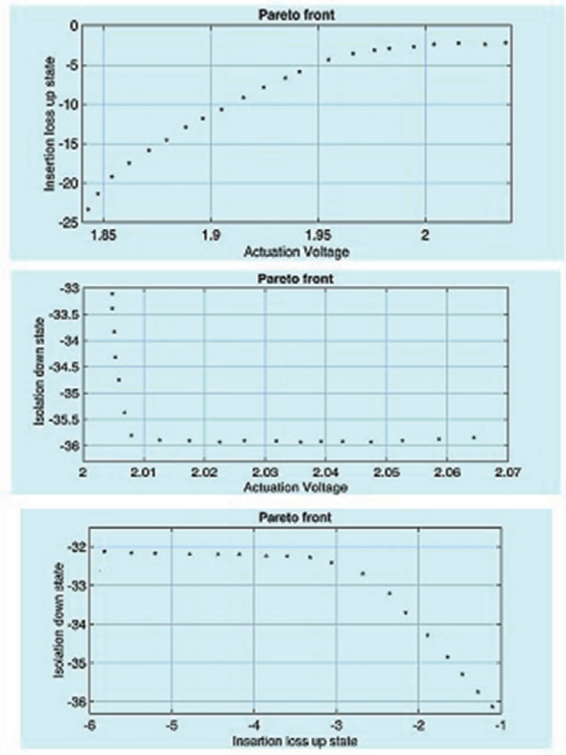

Figure 2: The visualization of the estimates of the Pareto front for the case study problem.

Table 2: Best parameters for NSGA-II algorithm

Population size	Number of iteration	Crossover probability (Pc)	Mutation (Pm)
250	500	0.8	0.25

After tuning the NSGA-II parameters, the model RF switch MEMS problem is solved in MATLAB software. The visualization of the estimates of the Pareto front for the case study problem is depicted in Fig. 2.

The values of target functions and variables are shown using the algorithm NSGA-II in Table 3.

Table 3: The values of target functions and variables

n	V	S_{11}	S_{21}	k	W	g_{gap}	t_d
1	1.981	-2.985	-32.417	1.333	199.841	1.115	0.094
2	2.03	-2.856	-33.209	1.442	199.956	1.109	0.087
3	1.421	-2.756	-34.110	1.214	199.969	1.118	0.085
4	2.032	-2.569	-33.593	1.389	199.946	1.121	0.084
5	2.051	-2.498	-33.124	1.398	199.898	1.131	0.091
6	2.026	-2.897	-34.459	1.445	199.995	1.141	0.93
7	1.996	-2.654	-34.158	1.498	199.972	1.131	0.087
8	2.019	-2.756	-33.275	1.245	199.964	1.115	0.088
9	2.015	-2.236	-34.163	1.469	199.997	1.154	0.091
10	2.062	-2.479	-33.231	1.326	199.963	1.112	0.087
11	1.992	-2.569	-33.195	1.213	199.979	1.104	0.084
12	2.113	-2.897	-34.189	1.335	199.854	1.106	0.088
13	2.057	-2.746	-34.356	1.456	199.897	1.109	0.087
14	2.067	-2.663	-34.237	1.364	199.964	1.103	0.086
15	2.042	-2.789	-34.187	1.287	199.985	1.110	0.088
16	2.034	-2.567	-33.598	1.251	199.932	1.113	0.089
17	2.031	-2.859	-34.320	1.199	199.987	1.112	0.087
18	2.019	-2.669	-33.365	1.203	199.935	1.155	0.092

3.4 Utiliti algorithm

It is clear that each set of the solutions represents a scenario for the development of a capacitance switch. Considering the same preference for the solutions obtained in the answer set, the approach based on the uti-liti of the target functions was used to find the optimal answer in such a way that each of the target functions has the least distance from the best value in the answer reported as the optimal one. In the approach used to select the answer from the set of solutions, the Equation 6.1 should be optimized in such a way that the Ui related to the uti-liti of the target function can be equal to Zi. Given the equations 6.2-6.5.[15], the uti-liti value is equal to the one for conditions in which each target function has its best value, while the uti-liti value is zero for conditions in which the target function has its worst possible value. [16]

$$\max \gamma \tag{6.1}$$

$$\gamma = \min\left(U_1, U_2, U_3\right) \tag{6.2}$$

$$U_1 = \left(\frac{Z_1^{max} - Z_1}{Z_1^{max} - Z_1^{min}}\right) \tag{6.3}$$

$$U_2 = \left(\frac{Z_2^{max} - Z_2}{Z_2^{max} - Z_2^{min}}\right) \tag{6.4}$$

$$U_3 = 1 - \left(\frac{Z_3^{max} - Z_3}{Z_3^{max} - Z_3^{min}}\right) \tag{6.5}$$

Table 4 presents the values related to the best, worst, and final values of the target function in the selected answer. According to the proposed uti-liti algorithm, the appropriate values for the actuation voltage and the return loss up-state and the isolation down-state values are equal to V=1.992V, S_{11}=-2.569dB, S_{21}=-33.195dB.

The optimal answer for the switch is obtained in row 11. According to the proposed algorithm, the optimal switch design is presented in the Table 5.

3.5 Switch spring constant

The spring constant presented in equation 7 is obtained with the design of spiral beams as shown in Fig.3[17]

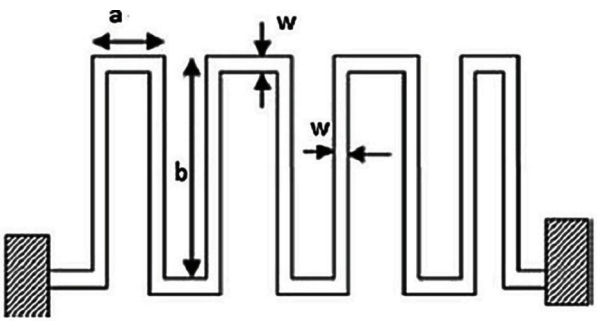

Figure 3: Spiral Beams Design

Table 4: Final value of the target function

n	V	S11	S21	U1	U2	U3	γ
1	1.981	-2.985	-32.417	0.1907514	0	1	0
2	2.03	-2.856	-33.209	0.1199422	0.17223	0.612145	0.119942
3	1.421	-2.756	-34.110	1	0.305741	0.170911	0.170911
4	2.032	-2.569	-33.593	0.117052	0.555407	0.424094	0.117052
5	2.051	-2.498	-33.124	0.0895954	0.6502	0.653771	0.089595
6	2.026	-2.897	-34.459	0.1257225	0.11749	0	0
7	1.996	-2.654	-34.158	0.1690751	0.441923	0.147405	0.147405
8	2.019	-2.756	-33.275	0.1358382	0.305741	0.579824	0.135838
9	2.015	-2.236	-34.163	0.1416185	1	0.144956	0.141618
10	2.062	-2.479	-33.231	0.0736994	0.675567	0.601371	0.073699
11	1.992	-2.569	-33.195	0.1748555	0.555407	0.619001	0.174855
12	2.113	-2.897	-34.189	0	0.11749	0.132223	0
13	2.057	-2.746	-34.356	0.0809249	0.319092	0.050441	0.050441
14	2.067	-2.663	-34.237	0.066474	0.429907	0.108717	0.066474
15	2.042	-2.789	-34.187	0.1026012	0.261682	0.133203	0.102601
16	2.034	-2.567	-33.598	0.1141618	0.558077	0.421645	0.114162
17	2.031	-2.859	-34.320	0.1184971	0.168224	0.068071	0.068071
18	2.019	-2.669	-33.365	0.1358382	0.421896	0.535749	0.135838

Table 5: Optimal switch design

n	V	S11	S21	U1	U2	U3	γ
11	1.992	-2.569	-33.195	0.174855	0.555407	0.619001	0.174855
Variables							
k		W		ggap		td	
1.213		199.979		1.104		0.084	

$$k_z = \left[\left[\frac{\left(8N^3a^3\right)+\left(2Nb^3\right)}{3EI_x}+\frac{abN\left[3b+(2N+1)(4N+1)a\right]}{3G_j}\right]-\right.$$
$$\left.-\left[\frac{Na^2\left[\left(\frac{2Na}{El_x}\right)+\frac{(2N+1)b}{G_j}\right]^2}{2\left(\frac{a}{El_x}+\frac{b}{G_j}\right)}-\frac{Nb^2}{2}\left(\frac{a}{G_j}+\frac{b}{El_x}\right)\right]^{-1}\right] \quad (7)$$

Table 6 presents the parameters of equation (7).

Table 6: The parameters of the equation (7)

Primary meander length (a)	Secondary meander length (b)	Beam with	Shear module (G_j)
4.5µm	45µm	1.7µm	E/(2(1+ν))
x-axis moment of inertia (Ix)	z-axis moment of inertia (Iz)	Polar moment of inertia (Ip)	Torsion constant (J)
$wt^3/12$	$wt^3/12$	Ix+Iz	$0.413I_P$

4 Designed switch analysis

After optimizing the suggested switch using the genetic algorithm and uti-liti algorithm presented in the previous sections, the electrical and mechanical properties and the efficiency of the RF MEMS parallel switch are optimized and simulated using COMSOL Multiphysics 4.4a and Advance Design System (ADS). Finally, the response provided by the parallel switch is reviewed.

4.1 Electro-Mechanic Analysis

The design and the optimization of the switch were investigated. The proposed design was simulated in the COMSOL software. The boundary conditions used in this design include fixing the end of the beam, applying zero voltage to the dielectric subsurface, applying the bias voltage to the membrane surface, applying symmetry conditions, using boundary load conditions to the beam subsurface to prevent infinite displacement error, and applying the boundary conditions of the electrical DC voltage on the switch level. Fig.4 illustrates the simulation results of the designed optimal switch. It is observed that applying the actuation voltage of 2V to the surface of the membrane causes a displacement of 1.1 µm and reaches the transmission line voltage to zero. Figs.4.a and 4.b illustrate the results obtained from the displacement and the axial residual stress. The axial residual stress resulting from applying the voltage to the switch surface is equal to σ=23MPa.

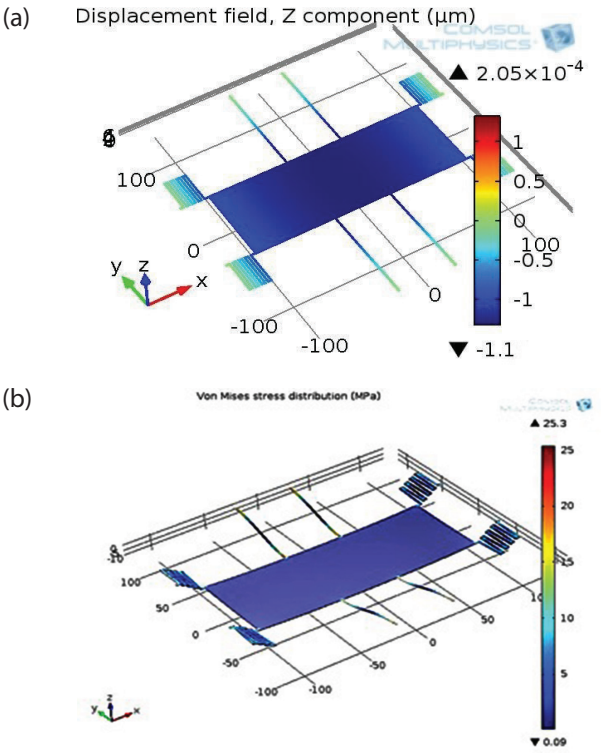

Figure 4: (a) Z-displacement distribution and (b) Von Misses stress distribution

4.2 Switch operation time and capacitor variations

The switch operation time which is highly dependent on the voltage is applied to the beam membrane. The response time is about 29.6µs by designing an optimal

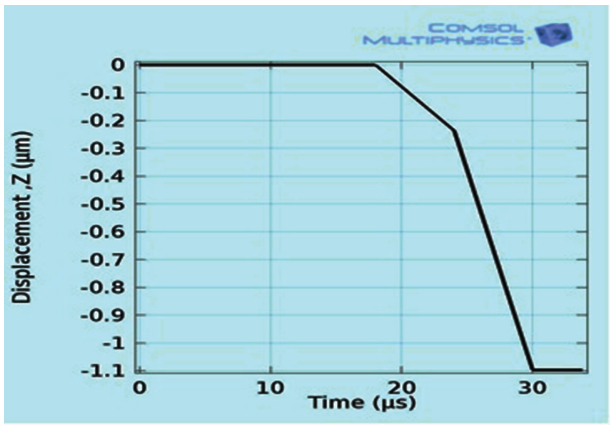

Figure 5: Simulation of the optimized RF-MEMS switch in time domain. Membrane's movement

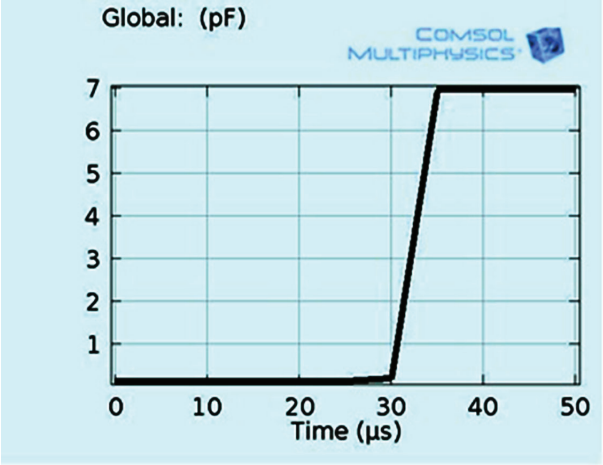

Figure 6: Capacitances of switch-on and switch-off

switch and applying the electrostatic actuation voltage as illustrated in Fig.5. Besides, it is possible to obtain the quickest answers by increasing the actuation voltage. As a result, the amount of capacitor is obtained at about 7pF after applying the electrostatic actuation voltage to the switch. When the electrostatic actuation voltage is cut off, the value of the capacitor is equal to 0.1 pF as shown in Fig.6.

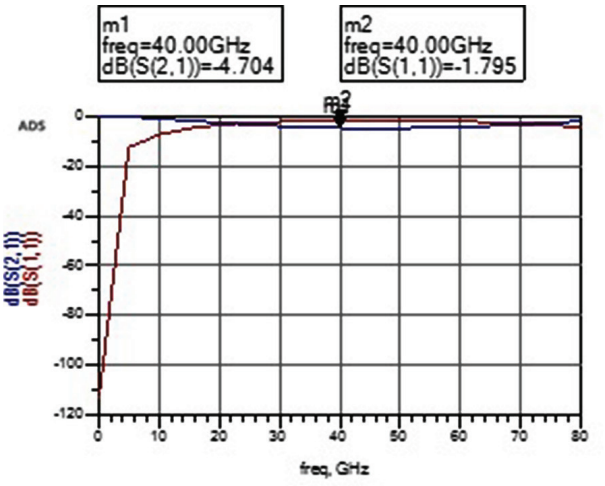

Figure 7: S-parameters of switch-up state

4.3 RF switch parameters

The electromagnetic analysis of the designed optimal switch is performed using the advance design system for wireless Communications software and equations 2 and 3. In addition, the index of dispersion (S parameter) is simulated. As illustrated in Fig.7, when the electrical voltage is not applied to the switch and the switch is off, the return loss is S_{11}=-2.54dB at the frequency of 40 GHz. Additionally, after applying the actuation voltage to the membrane surface and turning on the switch, the isolation is S_{21}=-33.18dB at the frequency of 40 GHz as shown in Fig.8.

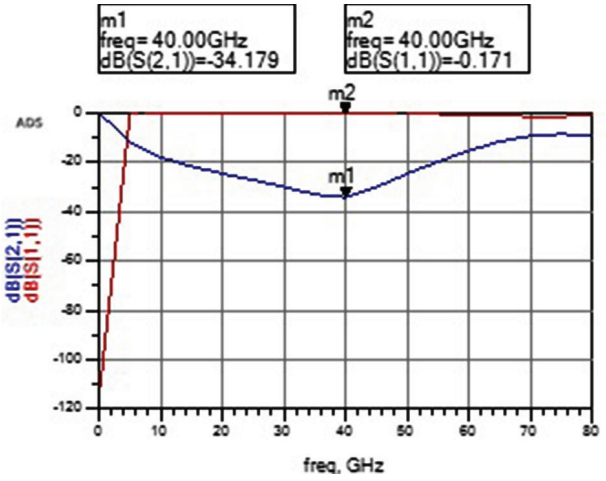

Figure 8: S-parameters of switch-down state

5 Results

The present paper developed a multi-objective model for determining the actuation voltage and insertion loss up-state and isolation down-state of an aluminium switch using a mathematical programming technique. The proposed model was solved by using the NSGA-II meta-heuristic algorithm and uti-liti algorithm. By extracting the Pareto solution set, the actuation voltage and insertion loss up-state and isolation down-state

Table 7: Comparison of developed capacitive RF-MEMS switches

	[5]	[6]	[7]	[8]	[9]	[4]	This work
V	7V	82V	23.6V	25V	3V	3.04V	2V
K	0.27N/m	-	1.43N/m	-	0.65N/m	1. 3N/m	1.213N/m
g_{gap}	1.1μm	-	3μm	3μm	2.2μm	1.397μm	1.1μm
t_d	Sio, ε_r=3.9	Sio, ε_r=3.9	AIN, ε_r=9.8	Si3N4, ε_r=6-7	Sio2, ε_r=4.99	Sio2, ε_r=4.99	Sio2, ε_r=4.99
S_{11}	3.1dB-	0.9dB-	0.68dB-	.8dB-	-	-5.6dB	-2.54dB
S_{21}	-15dB	-17dB	-35.7dB	-30dB	-	-24dB	-33.18dB
T	8.2μs	49μs	8.2μs	-	-	30μs	29.6μs

of the beam using five membranes in the form of flexure Serpentine for spring constant were reported as reported k=1.213N/M. In addition, the suitable design surfaces; including, length 45μm, width 4.5μm and thickness 1.7μm, and the number of members 4were selected to minimize the objective function of the switch. After the optimal design of the switch from the RF MEMS switch, the electrostatic pull-in voltage was calculated as 2V. The response time of the MEMS switch was about 29.6μs and the capacitance ratio was equal to 70. The return loss and isolation were S_{11}=--2.54dB and S_{21}=-33.18dB for the optimized switch at the frequency of 40 GHz.

6 Conclusion

Table 7 presents the comparison of our work with some typical developed capacitive RF-MEMS switches.

As shown in the Table 7, the designed switch has an optimal spring constant better than the previous work, and also the lower stimulation voltage and isolation and return loss due to the compromise between the parameters. As compared to the previous works, the design is remarkable and appropriate. But, generally speaking, with the presentation of the planned design and in many indicators, they exhibit their values and their superiority to other design methods that are based on trial and error.

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Arrived: 18. 01. 2019
Accepted: 17. 04. 2019

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Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
ISSN 0352-9045

Publisher / Založnik:
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