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On Realization of a New High-Precision and Low-Power CMOS Analog Multiplier Circuit

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Abstract. This paper proposes a new current-mode four-quadrant analog multiplier in the CMOS technology based on dual translinear loops. Compared with the previous works, this circuit has a simpler structure resulting in a higher frequency response, low-power consumption and low body-effect error. The circuit is thoroughly analyzed in terms of the of body-effect error and its results are presented. In order to verify its performance, the circuit is used in two useful applications: as an amplitude modulator and frequency doubler. The circuit is designed and simulated using HSPICE and 49 parameters (BSIM3v3) inthe 0.18 μm technology. The simulation results demonstrate the linearity error of 0.76%, THD of 0.92 in 1MHz, -3dB bandwidth of 104MHz and maximum power consumption of 0.18mW. the Monte Carlo analysis is carried out to ensure robustness of the circuit performance against process variations.

Keywords: Analog multiplier; current mode; translinear loop; four-quadrant; low power.

Zasnova analognega množilnika z visoko natančnostjo in majhno porabo moči v tehnologiji CMOS

V članku predstavljamo nov tokovni štirikvadrantni analogni množilnik v tehnologiji CMOS na osnovi dvojnih povratnih vezav. V primerjavi z obstoječimi množilniki ima predlagani množilnik preprostejšo zgradbo, kar ima za posledico višji frekvenčni odziv, majhno porabo moči in manjšo strukturno napako. Delovanje vezja in njegovo zmogljivost smo preverili pri zasnovi amplitudnega modulatorja in frekvenčnega podvajevalnika. Vezje smo zasnovali in simulirali s programskim paketom HSPICE in parametri level 49 (BSIM3v3) v tehnologiji 0.18 μm. Rezultati simulacij potrjujejo napako linearnosti 0.76 %, 0.92 THD pri 1MHz, pasovno širino 104 MHz in največjo porabo moči 0.18 mW. Z analizo Monte Carlo smo preverili zmogljivost vezja glede na odstopanja v tehnološkem procesu.

1 INTRODUCTION

The intensive use of analog multipliers as an essential building block of the analog signal system in a multitude of applications, such as modulators, frequency doublers, artificial networks, fuzzy integrated systems, automatic gain controlling [1-4], is the key driving factor for their considerable study and conception. The multiplier provides a product of two continuous signals, such as x and y, yielding an output of z = Kxy, where K is a constant value with a suitable dimension. The linearity, speed, bandwidth and power dissipation are the main goals of the design. At present, the power consumption is a key parameter in designing a high-performance mixed-signal integrated circuit. Some of the multipliers [5-9] are not optimal for the low-voltage and low-power applications. Several techniques for reducing the power consumption in circuits of this type have recently been proposed, they include the floating gate technique [10-12], bulk-driven method [13, 14], subthreshold mode [15, 16], or class-AB mode [17, 18]. However, these analog multiplier circuits have been proposed either in the voltage or current modes.

One of the important classes of multipliers which uses current-mode technique is based on the translinear loop (TL) principle [19-21]. TL is a special device arrangement that allows a useful large signal relationship among its currents [19]. Usually, the devices employed in the TL loops can be BJT, MOS transistors or diodes. If diodes are used, usually an extra active circuit is required [21]. The advantage of this circuit is independence of the output current expression on technological parameters and the circuit operation is not affected by temperature variations, ideally.

Considering the operation region of the TL transistors, they can be classified in two classes: weak inversion [22-24] and strong inversion [25-29]. For the weak inversion, although it leads to circuits offering a low power dissipation, the bandwidth and dynamic range are limited. For the TL circuits in the strong inversion, the error resulting from the body effect is a serious problem for causing a mismatch in the threshold voltages which in turn, affects the linearity and precision of the circuits. However, in some studies this

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effect is properly discussed and a few techniques are proposed [30,31]. Also, some CMOS multiplying circuits are designed using MOS transistors operating in the linear region [31-33]. Several CMOS multiplying circuits are designed using a short-channel MOSFET, but they has not compensate for the error due to the carrier mobility reduction [34-38]. Therefore, the accuracy of these circuits is degraded.

In this paper, a new topology of the analog-multiplier circuit based on a translinear loop is presented. Its main advantages are a high-precision performance as well as low power dissipation. In order to verify the efficiency of the performance circuit, the error caused by the body effect is analyzed and then minimized in the simulation results. Moreover, to prove the process and threshold voltage-variation effect on the circuit performance, the Monte-Carlo simulation is adopted. The paper is organized in five sections: The proposed method for implementation of the multiplier circuit as well as the transistor level design are presented in section 2. In section 3, the HSPICE simulation results of the proposed circuit are presented to prove the efficiency of the design. The performance analysis of the circuit is described in section 4. Finally, conclusions are outlined in section 5.

2 CIRCUITDESCRIPTION

The principle of operation of the proposed multiplier is based on the square-difference algebraic characteristic:

$$(X+Y)^2-(X-Y)^2=4XY \tag{1}$$

Thus, subtraction, summing and squaring are the operations needed to be done for the multiplier circuit. To generate Equation (1) in an analog multiplier circuit, two squarer blocks are required toproducea two-squarer function and its outputs need to be subtracted. Fig. 1 shows the proposed four-quadrant CMOS analog multiplier circuit. It is based on two dual translinear loops. The first loop, consisting of (M_1-M_4), realizes the $(X-Y)^2$ function and the second loop, consistingof(M_3-M_6),therealizes the $(X+Y)^2$ function. The drain current of the MOS transistor operated in the saturation region is given by:

$$I_{DS}=K\left(V_{GS}-V_t\right)^2 \tag{2}$$

$$V_{GS}=V_t+\sqrt{\frac{I_{DS}}{K}} \tag{3}$$

Where $K=0.5\mu_0C_{OX}(W/L)$ is the transistor transconductance parameter, μ_0 is the electron mobility, C_{OX} is the gate oxide capacitance per unit area, $W/L$is the transistor aspect ratio, $V_{GS}$is the gate-to-source voltage and V_t is threshold voltage of the MOS transistor.Applying KVL in the first dual translinear loops yields:

$$V_{GS1}+V_{GS2}=V_{GS3}+V_{GS4} \tag{4}$$

Assuming that all CMOS transistors operate in the saturation region, using Equation (2) and Equation (3) and considering $I_{DS3}=I_{DS4}=I_B$, we have:

$$\sqrt{I_{DS1}}+\sqrt{I_{DS2}}=\sqrt{I_{DS3}}+\sqrt{I_{DS4}} \tag{5}$$

$$\sqrt{I_{DS1}}+\sqrt{I_{DS2}}=2\sqrt{I_B} \tag{6}$$

Writing KCL at nodes A and Bas:

$$I_{DS2}=I_{DS1}+I_{in1} \tag{7}$$

$$I_{o1}=I_{DS1}+I_a \tag{8}$$

Since $I_{DS2}=I_a$ and substituting Equation (7) in Equation (8), we have:

$$I_{DS1}=(I_{o1}-I_{in1})/2 \tag{9}$$

$$I_{DS2}=(I_{o1}+I_{in1})/2 \tag{10}$$

Substituting Equation (9) and Equation (10) in Equation (6) and squaring both sides:

$$4I_B=I_{o1}-(I_{in1}/2)+(I_{in1}/2)+2\sqrt{I_{o1}^2-I_{in1}^2} \tag{11}$$

Eliminating $I_{in1}/2$ and squaring both sides again yields:

$$16I_B^2-8I_BI_{o1}=-I_{in1}^2 \tag{12}$$

Then, the output current of I_{o1} can be written as:

$$I_{o1}=\frac{I_{in1}^2}{8I_B}+2I_B \tag{13}$$

In asimilar way, for I_{o2} we have:

$$\sqrt{I_{DS3}}+\sqrt{I_{DS4}}=\sqrt{I_{DS5}}+\sqrt{I_{DS6}} \tag{14}$$

and:

$$\begin{cases}I_{DS5}=I_{DS6}+I_{in2}\\ I_{o2}=I_{DS6}+I_b\end{cases},\quad \begin{cases}I_{DS6}=(I_{o2}-I_{in2})/2\\ I_{DS5}=(I_{o2}+I_{in2})/2\end{cases} \tag{15}$$

resulting:

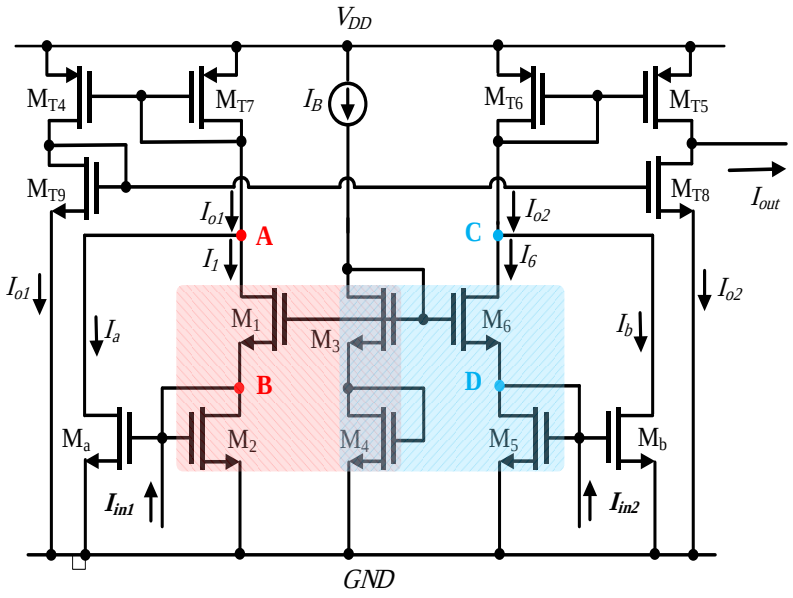

Figure1.Proposed current-mode analog multiplier circuit.

$$I_{o2} = \frac{I_{in2}^{\ 2}}{8I_B} + 2I_B \tag{16}$$

The total output current of I_{out} is given by:

$$I_{out} = I_{o2} - I_{o1} \tag{17}$$

Considering $I_{in1} = I_X - I_Y$ and $I_{in2} = I_X + I_Y$, and substituting Equation(13) and Equation (16) into Equation (17) results in:

$$I_{out} = \frac{I_X I_Y}{2I_B} \tag{18}$$

As clearly seem from Equation (18), the output of the proposed circuit yields a multiplication of I_X and I_Y divided by the constant current of $2I_B$ here I_B is a constant current of $10\mu A$ normalized to one.

3 Simulation Results

The analog multiplier circuit of Fig. 1 is simulated using HSPICE with the $0.18\,\mu m$ CMOS technology, the supply voltage is 1.8 V and the bias current of I_B is set to $10\mu A$. As mentioned, Equations (13) and (16) are the current squarer of the input signals, and thesimulation result of thefirst squarer circuit is shown in Fig. 2 where the upper waveform is the input current, the middle waveform is the output current and the bottom waveform shows the error measurement. The average error in this simulationremains as low as 0.29 %.

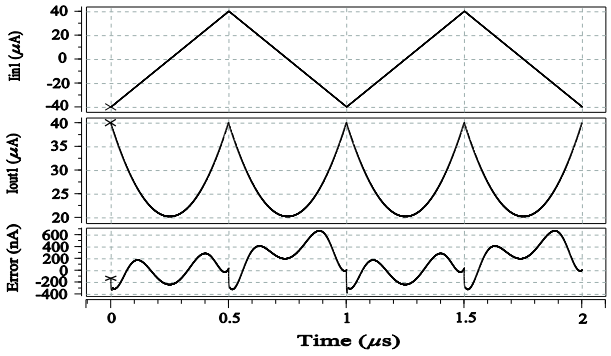

Figure 2. Simulation results of thecurrent squarer of the input signal (I_{in1}) in the loop ($M_1 - M_4$) and error measurement (frequency = 1 MHz).

Fig.3 shows the DC transfer characteristic of the proposed analog multiplierwhere I_X is set to a pulse with a variable amplitude from -20μA to 20μA to varying I_Y from -10μA to 10μA As a result, the output current varies from -10μA to 10μA.Within this range, the measured nonlinearity error is 0.76 %.

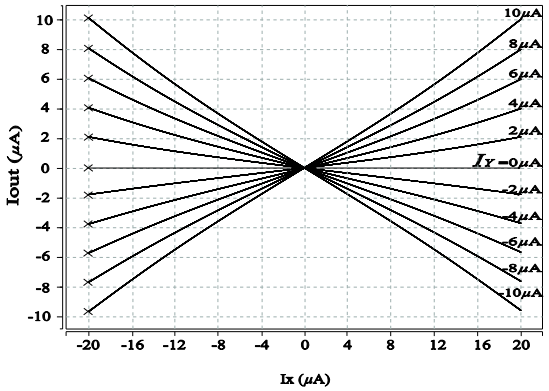

Figure 3. Simulation results of thecurrent squarer of the input signal (I_{in1}) in the loop ($M_1 - M_4$) and error measurement (frequency = 1 MHz).

Fig. 4 shows results of other simulations with error measurements in which I_X and $I_Y$are sinusoidal at 200 KHz with amplitudes of 10μA and 5μA, respectively, which yields a sinusoidal output with a high precision that marked with ared line. Within this range, the measured nonlinearity error is 0.76 %.

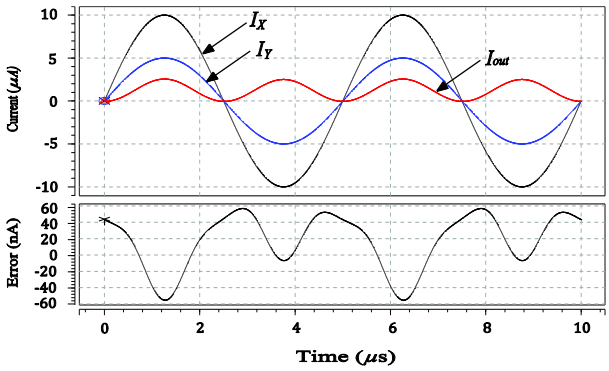

Figure 4. Other simulations of theanalog multiplier circuit in 0.2 MHz and error measurement.

Fig. 5 demonstrates the total harmonic distortion (THD) versus theinput signal at 100 kHz and 1 MHz simultaneously. The simulations are performed for both I_X and I_Y, in which one of them is constant andthe other one is sinusoidal. In the worst case, the input signal of $20\mu A_{P-P}$ at a frequency of 1 MHz results in THD of less than 0.92 %.

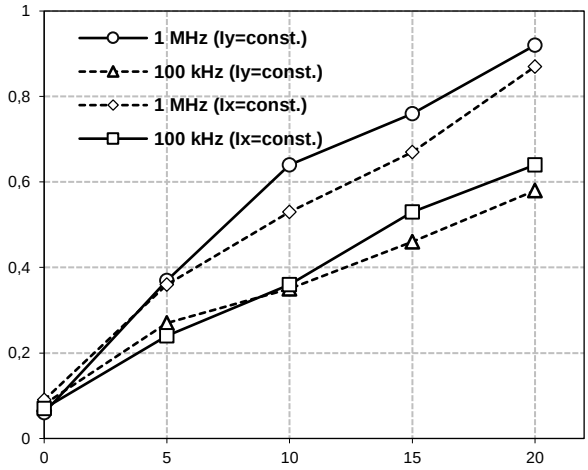

Figure 5. Relation between THD ,I_X and I_y.

The frequency response of the circuit in Fig. 6 shows thatthe -3dB bandwidth is 104 MHz when the input signal is applied to $I_X$and I_Y = 10 µA. It should be pointed out that the input signals are applied in where the circuit output is 0 dB for aprecise measuring ofthe-3 dB bandwidth of the circuit. Thetotal power consumption is 0.18 mW.

Fig. 7 demonstrates the multiplier being used forthe balance modulator. $I_X$andI_Y are 1 MHz and 100 kHz, with avariable amplitude froma -20μA to 20μA carrier and modulation signals, respectively, fed to theinputs of the proposed multiplier, while the bias currentis constant. Fig. 8 shows how the multiplier circuit can be employed as a frequency doubler. If both frequencies of the input currents are 1 MHz, the figure shows the corresponding output waveform with adouble frequency as well as the error quantity.

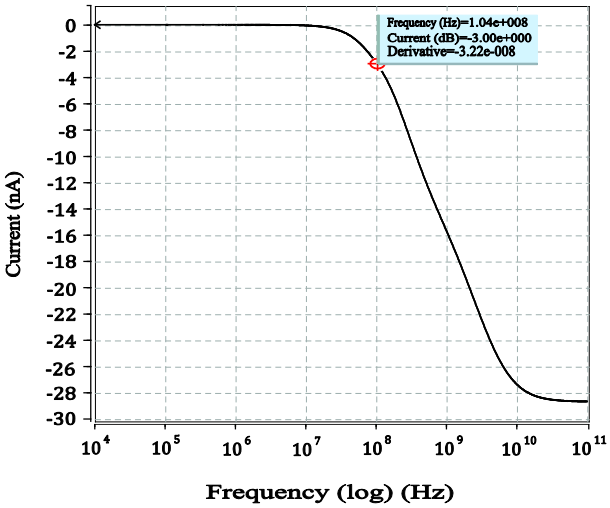

Figure 6. Frequency response of the proposed circuit.

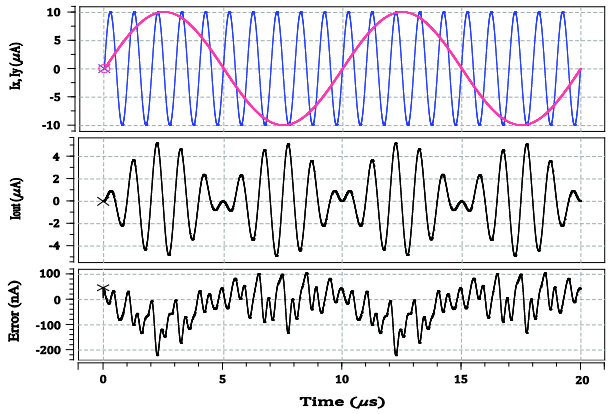

Figure 7. Proposed multiplier as an amplitude modulator. A1 MHz carrier sinusoid and 100 kHz modulating signal (upper waveform); AC modulated output (middle waveform); Error measurement (lower waveform).

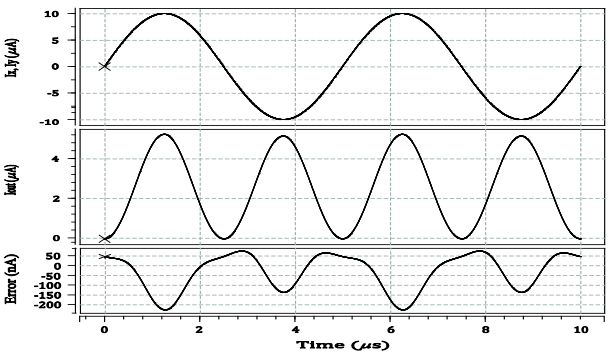

Figure 8. Proposed multiplier as a frequency doubler: a) input waveform (upper); b) output waveform (middle); c) error measurement (lower).

4 PERFORMANCE ANALYSIS

In this section, the characteristics of the analog multiplier in the terms of the body-effect error and threshold-voltage mismatch in a translinear loop are discussed. TheMonte Carlo analysis and temperature-variation simulations are carried out to verify the circuit performance of process variation conditions

4.1 Body Effect Error

In the MOS transistor, thebody effect refers to achange in the transistor threshold voltage resulting from a voltage difference between the transistor source and substrate, characterized by:

$$V_t = V_{t0} + \gamma\left[\sqrt{\left(2\phi_b + |V_{SB}|\right)} - \sqrt{2\phi_b}\right] \quad (19)$$

Where V_{t0} is the zero-bias threshold voltage, γ is the body-effect coefficient and ϕ_b is the bulk potential. To avoid this effect, the cascaded MOS transistors are placed in separate wells and V_{SB} will be zero. Thus, these transistors will have azero-bias threshold voltage.

Let us consider the first translinear loop, consisting of $(M_1 - M_4)$. In athin loop, theM_2 and M_4 transistors bulk are connected to the ground, hence $V_{SB} = 0$ and $V_t = V_{t0}$, but intheM_1 and M_3 transistors $V_{SB} \neq 0$. Considering this mismatch betweentheM_1 and M_3 transistors, we can write

$$V_{GSc} = V_{t1} + \Delta V_1 \quad (20)$$

$$V_{GS3} = V_{t3} + \Delta V_3 \quad (21)$$

Substituting Equation (20) and Equation (21) in Equation (4) yields:

$$V_{t1} + \Delta V_1 + V_{GS2} = V_{t3} + \Delta V_3 + V_{GS4} \quad (22)$$

Where$V_{t1} = V_t + \delta, V_{t3} = V_t - \delta$ and δ is the mismatch term between V_{t1}, V_{t3}. Rewriting Equation 6, $I_{DS1} = I_{DS2} = I_B$, $I_{DS3} = (I'_{out} - I_{in})/2$, $I_{DS4} = I_f - I_{in}$ and assuming$V_{t2} = V_{t4}(|V_{SB}| = 0)$, we obtain

$$\delta + 2\sqrt{\frac{I_B}{K}} = -\delta + \sqrt{\frac{I_3}{K}} + \sqrt{\frac{I_3 + I_{in}}{K}} \quad (23)$$

Substituting $I_3 = (I'_{out} - I_{in})/2$ in Equation (23), squaring both sides and ignoring the terms containing $\delta^2$are get

$$8\delta\sqrt{\frac{I_B}{K}} + \frac{4I_B}{K} = \frac{I'_{out}}{K} + \frac{\sqrt{I'^{\,2}_{out} - I^{\,2}_{in}}}{K} \quad (24)$$

Assuming $I_B = K\Delta V^2$and squaring both sides of Equation (24), current I'_{out} can be expressed as:

$$I'_{out} = \frac{I_{in}^{\,2}}{8K\Delta V\left(\Delta V + 2\delta\right)} + 2K\Delta V\left(\Delta V + 2\delta\right) \quad (25)$$

In this equation we can see that themismatch error Between the threshold voltages is dispensable, because $\Delta V \gg 2\delta$.

Subtracting Equation (18) from Equation (25), we obtain theoutput-current error quantity:

$$|I_{error}| = I_{out} - I'_{out} = \frac{I_{in}^{\,2}}{8K\Delta V^{\,2}} + 2K\Delta V^{\,2}$$

$$-\left[\frac{I_{in}^{\,2}}{8K\Delta V\left(\Delta V + 2\delta\right)} + 2K\Delta V\left(\Delta V + 2\delta\right)\right] \quad (26)$$

Ignoring theterms containing $\Delta V^n (n = 3,4,5)$, δ^2

$$|I_{error}| = \frac{\delta}{4K\Delta V^{\,2}\left(\Delta V + 2\delta\right)} I_{in}^{\,2} - 4K\delta\Delta V \quad (27)$$

TermΔV^3 in Equation (27) shows avery small error. The advantage of using the function$(X+Y)^2 - (X-Y)^2$ in the multiplier circuit is the possibilityto cancel the offset and body-effect errors by eliminating the second term in Equation (25). Consequently, the output current is given by:

$$I_{out} = \frac{I_X I_Y}{2I_B + 4\delta K\Delta V} \quad (28)$$

4.2 Mismatch and Temperature Effects

The Monte Carlo analysis of the proposed circuit with 100 iterations is carried out by applying amismatch in thetransistors aspect ratio and threshold voltage withthe Gaussian distribution. This is done to ensure the robustness of the circuit performance against the fabrication process (see Fig. 9). The output of the multiplier without any mismatch shown in Fig. 5 is considered as an ideal output without any error (0%).The Monte Carlo analysis is theycarried outdemonstratingthat 91% of thetotal samples occurs with an error of less than ±1% forthan threshold voltage and transistors aspect-ratio variations.

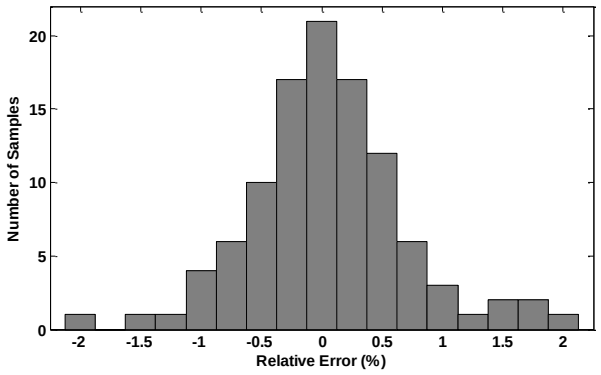

Figure 9. Monte Carlo analysis of the multiplier circuit for the mismatch in the transistors aspect ratio and threshold voltage.

Fig. 10 shows the circuiterror atvarious temperatures, while the maximum error occurring at 80 ^{o}C is 0.93 %. In this simulation, the obtained output at the temperature of 25 ^{o}C is considered as the reference value (relative error=0). The outputs in other temperatures are thancompared with that value and the relative error is computed. It should be pointed out that the input signals are the same as the signals applied in the Monte Carlo analysis. The equations should be written in italics and numbered:

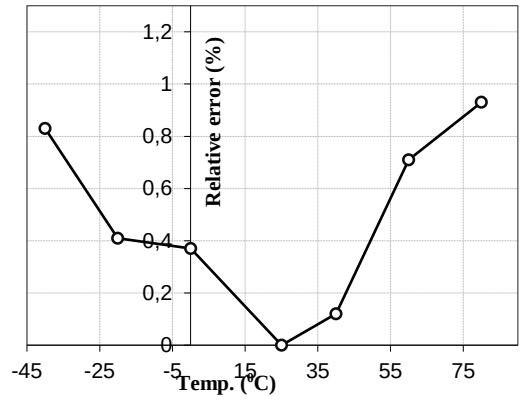

Figure 10. Relative error of the circuit versus different temperatures.

5 CONCLUSION

A four-quadrant CMOS multiplier based on dual translinear loops in a current mode is proposed. The performance of the multiplier is simulated using the HSPICE software. The simulation results indicate that the multiplier has remarkable benefits in terms of a high bandwidth (104 MHz), low-power consumption (0.18 mW), and low body-effect error. In order to verify the circuit performance, the designed circuit is used in two useful applications: the amplitude modulator and frequency doubler. Moreover to prove the process and threshold-voltage variation effect on thecircuit performance, theMonte-Carlo simulation was adopted. The characteristics of the circuit are summarized in Table 1 and compared with the former works to prove the efficiency circuit.

Table 1.Comparative parameters of the proposed multiplier with other recent works.

Reference	[5]	[8]	[19]	[37]	[38]	This work
Power consumption (mW)	0.7	0.47	0.52	0.34	0.15	0.18
Bias current (μA)	100	-	-	10	-	10
Power supply (V)	5	±1.5	2.8	3.3	±0.75	1.8
THD(%) (1MHz,20μA)	-	0.87	1.45	0.97	0.8	0.92
Nonlinearity (%)	-	1.3	1.12	1.1	1.1	0.76
−3db bandwidth (MHz)	12.3	24.3	137	41.8	300	104
Technology (μm)	2.4	0.35	0.18	0.35	0.18	0.18

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