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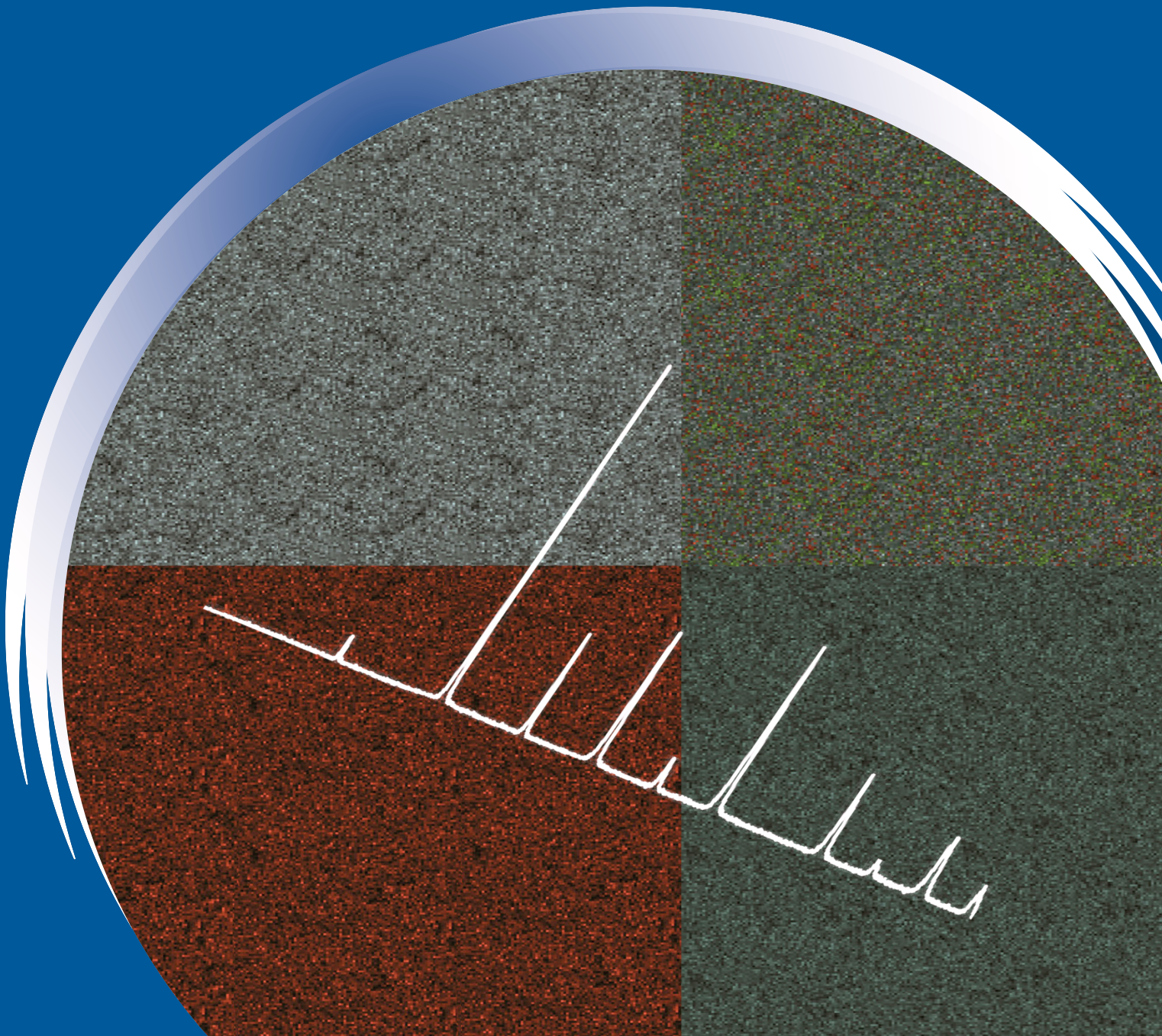

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Electrocaloric and pyroelectric properties of $0.6Ba_{0.85}Ca_{0.15}Zr_{0.10}Ti_{0.90}O_3$ –$0.4BaTi_{0.89}Sn_{0.11}O_3$ ceramics

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Abstract: Ferroelectric materials are gaining considerable attention for energy storage, electrocaloric and pyroelectric energy harvesting applications. In particular, $Ba_{0.85}Ca_{0.15}Zr_{0.10}Ti_{0.90}O_3$ (BCZT) and $BaTi_{0.89}Sn_{0.11}O_3$ (BTSn) ceramics are among the best-studied lead-free $BaTiO_3$-based ferroelectrics with high piezoelectric and electrocaloric properties. In this work, we prepared a 0.6BCZT–0.4BTSn solid solution. The structural, energy storage, electrocaloric, and pyroelectric properties are investigated. An energy density of 61.4 mJ cm^{-3} with a high energy efficiency of 82.4 % at 90 °C is achieved. The electrocaloric temperature change, which is determined indirectly via the Maxwell relation, is 0.5 K at 86 °C and 25 kV cm^{-1}. It is stable over a wide temperature range of around 65 °C and has a coefficient of performance of 15. Moreover, a pyroelectric energy density of 124.1 mJ cm^{-3} is achieved. The results of this study show that the 0.6BCZT–0.4BTSn ceramics is a multifunctional material with energy storage, electrocaloric and pyroelectric properties.

Keywords: Lead-free; ceramic; BCZT; energy storage; electrocaloric; pyroelectric; energy harvesting

Elektrokalorične in piroelektrične lastnosti $0.6Ba_{0.85}Ca_{0.15}Zr_{0.10}Ti_{0.90}O_3$ –$0.4BaTi_{0.89}Sn_{0.11}O_3$ keramike

Izvleček: Feroelektrični materiali pridobivajo veliko pozornost v raziskavah, ki se osredotočajo na elektrokalorične in piroelektrične pojave ter na shranjevanje energije. Zlasti keramiki $Ba_{0.85}Ca_{0.15}Zr_{0.10}Ti_{0.90}O_3$ (BCZT) in $BaTi_{0.89}Sn_{0.11}O_3$ (BTSn) sodita med najbolj raziskane keramične materiale brez svinca na osnovi $BaTiO_3$. V tem delu smo pripravili trdno raztopino 0.6BCZT–0.4BTSn. Raziskali smo strukturne, elektrokalorične in piroelektrične lastnosti keramike 0.6BCZT-0.4BTSn ter njeno zmožnost shranjevanja energije. Keramika izkazuje gostoto shranjevanja energije v višini 61.4 mJ cm^{-3} z najvišjim energijskim izkoristkom 82.4 % pri temperaturi 90 °C. Elektrokalorična temperaturna sprememba določena preko Maxwellove enačbe, znaša 0.5 K pri temperature 86 °C in električnem polju 25 kV cm^{-1} ter je stabilna v širokem temperaturnem območju 65 °C s koeficientom učinkovitosti 15. Keramika izkazuje tudi piroelektrično gostoto energije 124.1 mJ cm^{-3}. Rezultati kažejo, da je keramika 0.6BCZT-0.4BTSn večfunkcijski material, ki izkazuje elektrokalorične in piroelektrične lastnosti ter zmožnost shranjevanja energije.

Ključne besede: keramika brez svinca; BCZT; shranjevanje energije; elektrokalorik; piroelektrik; zbiranje energije

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1 Introduction

To alleviate growing environmental concerns, the green energy industry is developing rapidly [1]–[4]. In particular, high-efficiency electrocaloric (EC) cooling technologies have attracted much attention, especially in ferroelectric materials. This is due to their ability to be efficiently driven by electric fields that are readily available, making them promising for use in solid-state cooling systems to cool microelectronic devices [5]–[7]. This is due to their polarization and entropy change near the ferroelectric phase transition upon application/removal of an electric field, resulting in an adiabatic temperature change (ΔT), known as the EC effect [8]–[10]. In addition, dielectric capacitors such as ferroelectric materials have been widely used in energy-scavenging technologies based solely on their intrinsic polarization [11], [12].

The waste heat produced by many electronic devices presents an opportunity for energy harvesting technologies, which can convert it in various ways [13]. One approach to enhance device efficiency, involves harvesting and converting this wasted heat through pyroelectric energy harvesting [14], [15]. This method requires converting heat energy into clean electricity using materials exhibiting the pyroelectric effect [16]. This effect known as the converse of the EC effect, involves the transformation of waste or heat energy into electrical voltage when subjected to temperature variations [17]. Its magnitude can be assessed using the Olsen cycle, similar to the Ericson cycle [18], [19]. Accordingly, the density of pyroelectric energy harvesting (U_{pyro}) can be calculated from the recorded polarization–electric field (P–E) hysteresis loop of ferroelectric materials. Since ferroelectrics are a subgroup of pyroelectrics, $BaTiO_3$ (BT)-based materials are considered promising candidates for pyroelectric energy harvesting. These materials exhibit significant spontaneous polarization and can undergo polarization changes across a broad temperature range, fulfilling the requirements of the EC effect. For example, U_{pyro} value of 229 mJ cm^{-3} was found in $0.5BaZr_{0.2}Ti_{0.8}O_3$–$0.5Ba_{0.7}Ca_{0.3}TiO_3$ ceramics [20]. In addition, a comparable U_{pyro} value of 210 mJ cm^{-3} was obtained in $BaTi_{0.91}Sn_{0.09}O_3$ ceramics [21].

Ceramic dielectric capacitors play crucial roles as energy conversion and storage devices by absorbing and releasing large voltages or current pulses within a short lifetime between microseconds and milliseconds [22]. This property makes them promising candidates for energy-storage devices within pulsed-power and power-conditioning electronic applications [2], [23]. Pure BT ceramics capacitors exhibit a ferroelectric tetragonal phase with high dielectric permittivity close to the Curie temperature (T_c) and a relatively square-like P–E hysteresis loop, with both large remanent polarization (P_r) and coercive field (E_c). These properties lead to high energy loss (U_{loss}), low recovered energy density (U_{rec}) as well as low energy storage efficiency (η), limiting BT ceramics from practical application in energy storage devices [24]. Doping BT material with Ca^{2+} at the A-site and with Zr^{4+}/Sn^{4+} at the B-site could be beneficial to adjust the P–E hysteresis loop by reducing the P_r and increasing the difference ΔP between the maximal polarization (P_{max}) and P_r, thereby enhancing simultaneously its U_{rec} and η [22], [24]–[27].

In 2009, Liu et al. reported a high piezoelectric coefficient of d_{33} ~ 620 pC N^{-1} in $Ba_{0.85}Ca_{0.15}Zr_{0.10}Ti_{0.90}O_3$ (abbreviated as BCZT) ceramics related to the morphotropic phase boundary occurring at room temperature. Subsequently, $BaTi_{0.89}Sn_{0.11}O_3$ (abbreviated as BTSn) with a quasi-quadruple point (coexistence of cubic–tetragonal–orthorhombic–rhombohedral phases) was found to have high dielectric permittivity (~ 75 000) and improved piezoelectric coefficient of d_{33} ~ 697 pC N^{-1} at ~ 42 °C [28]. As a result, the chemical modification of BT (e.g., Ca, Zr, Sn, etc.) enhance further the dielectric and piezoelectric poperties [29]–[35]. With the chemical modification, the thermal stability of the properties can be tailored by approaching the rhombohedral–orthorhombic (R–O, T_{R-O}) and orthorhombic–tetragonal (O–T, T_{O-T}) phase boundaries with the corresponding phase transition temperatures to the T_c peak temperature together with shifting T_c to room temperature [31]. The sequence of phase boundaries enhance the thermal stability of the properties over a wide temperature range, which is essential to achieve practical applications [31].

We have previously reported the EC properties of BCZT and BTSn ceramics studied by the indirect Maxwell approach [36], [37]. BTSn ceramics showed high ΔT~0.71 K at 40 °C at 25 kV cm^{-1}, but in a relatively narrow temperature span (T_{span}) [37]. Meanwhile, BTSn ceramic showed a U_{rec} of 84.4 mJ cm^{-3} with high η of 91.0 %. In contrast, BCZT ceramics showed a ΔT~0.57 K at 100 °C at the same electric field in a relatively broader T_{span} of 70 K [36]. However, the U_{rec} was ~75 mJ cm^{-3} with a very low η of 37 %, limiting BCZT from practical applications. In order to prepare multifunctional material with both enhanced electrical properties and thermal stability, we prepared $(1-x)Ba_{0.85}Ca_{0.15}Zr_{0.10}Ti_{0.90}O_3$–$xBaTi_{0.89}Sn_{0.11}O_3$ solid solution system (x = 0.2, 0.4 and 0.6) as previously reported in our previous work [38]. In this work, we investigated structural, energy storage, EC effect and pyroelectric energy harvesting properties of 0.6BCZT-0.4BTSn ceramics (abbreviated as 0.4BTSn).

2 Materials and methods

The $0.6Ba_{0.85}Ca_{0.15}Zr_{0.10}Ti_{0.90}O_3$–$0.4BaTi_{0.89}Sn_{0.11}O_3$ (abbreviated as 0.4BTSn) ceramics was prepared by conventional solid-state method, by homogenizing BCZT and BTSn calcined powders. The preparation process of 0.4BTSn ceramics is described in detail in our previous work [38].

The crystalline structure of crushed 0.4BTSn ceramic pellet at room-temperature (RT) was investigated by X-ray powder diffractometer (XRD, BRUKER AXS D4 ENDEAVOR) equipped with Cu-Kα-radiation. Diffraction patterns were recorded in the 10–80° *2θ*-range with a step size of 0.02° using Cu-Kα-radiation. Phase identification was performed with the COD-2020 database using the standard diffraction peaks of $BaTiO_3$ with orthorhombic (PDF#81–2200) and tetragonal (PDF#05–0626) symmetries [39].

The microstructure of sintered ceramics was examined using a scanning electron microscope (SEM, Zeiss EVO 10 SEM, Carl Zeiss Microscopy, Germany) equipped with an energy dispersive X-ray spectrometer (EDXS, ZEISS SmartEDX Instrument, Carl Zeiss Microscopy, Germany). Prior to the microstructural analysis, the samples were ground and finely polished using a colloidal silica suspension. The bulk density of the sintered ceramics was determined by the Archimedes' method using deionized water as medium. In addition, the average grain size was determined from the digitized images of the polished surfaces processed with ImageJ software (version 1.52a, National Institutes of Health, USA) by measuring more than 300 grains using the average grain intercept (AGI) method.

For the electrical properties, the ceramic pellets were cut, thinned, and polished to a thickness of about 400 µm and then the Cr/Au electrodes were sputtered on sample' surfaces. The dielectric properties were measured using a precision LCR Meter instrument (Agilent, 4284A, USA) in the temperature range from –50 to 200 °C. The polarization versus electric field (*P*–*E*) hysteresis loops were recorded using Aixacct TF analyzer 2000 (Aixacct, Aachen, Germany) from 30 to 140 °C using a triangular excitation signal with a frequency of 10 Hz.

3 Results

The XRD patterns of the 0.4BTSn ceramic at room temperature is shown in Figure 1 (a). It shows peaks characteristic of the perovskite phase. The XRD fitting pattern extended by $2\theta \approx 45°$ using the Lorentz fitting method is shown in the inset (Figure 1 (b)). The enlarged peak presents a splitting of two peaks that could be the coexistence of orthorhombic $(022)_O$ and tetragonal $(200)_T$ peaks

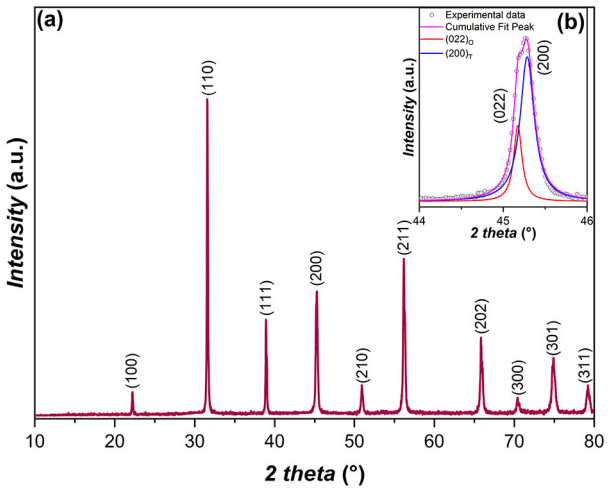

Figure 1: (a) Room-temperature XRD pattern of the 0.4BTSn ceramics, and (b) the enlarged view of the peak splitting at $2\theta \approx 45°$.

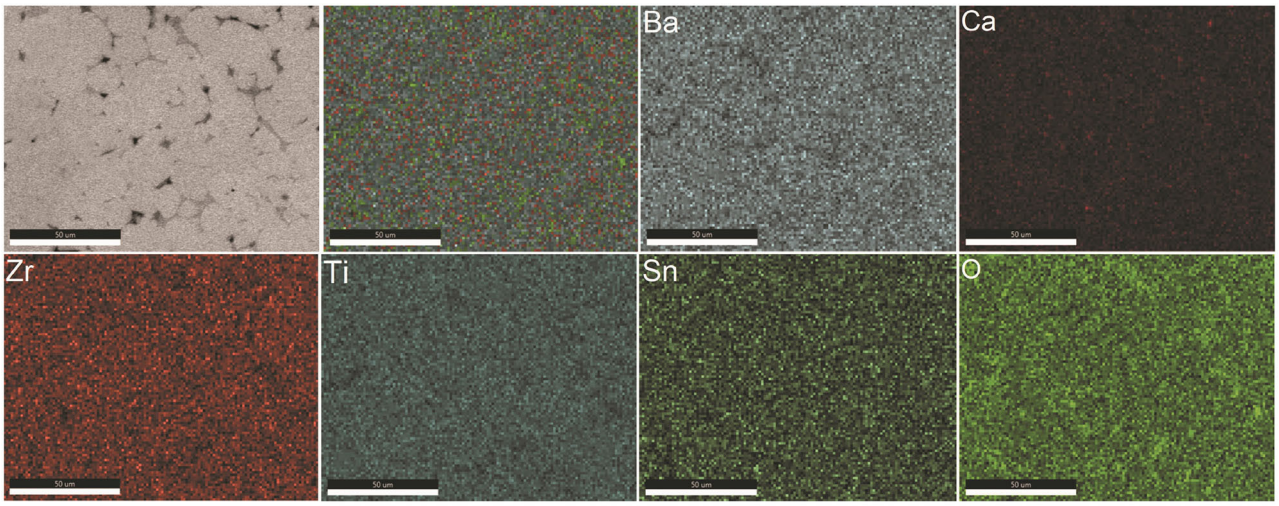

Figure 2: SEM image and EDXS maps show the distribution of elements Ba, Ca, Zr, Ti, Sn and O on the surface of the 0.4BTSn ceramic (Scale bar: 50 µm).

forming a $(022)_O/(200)_T$ doublet [40]. These results were confirmed by using Rietveld refinement, as reported in our previous work [38].

To gain insight into the microstructure and chemical composition of the 0.4BTSn ceramics, Figure 2 shows the SEM and the elemental mapping images on the polished surface of the sample. A compact and dense microstructure with an average grain size of (12.0 ± 4.8) μm were observed. The density of the ceramic was 5.5 g cm^{-3}, which corresponds to 93 % of the theoretical density. Furthermore, the EDXS mapping images show a homogeneous distribution of all contained elements (Ba, Ca, Zr, Ti, Sn and O).

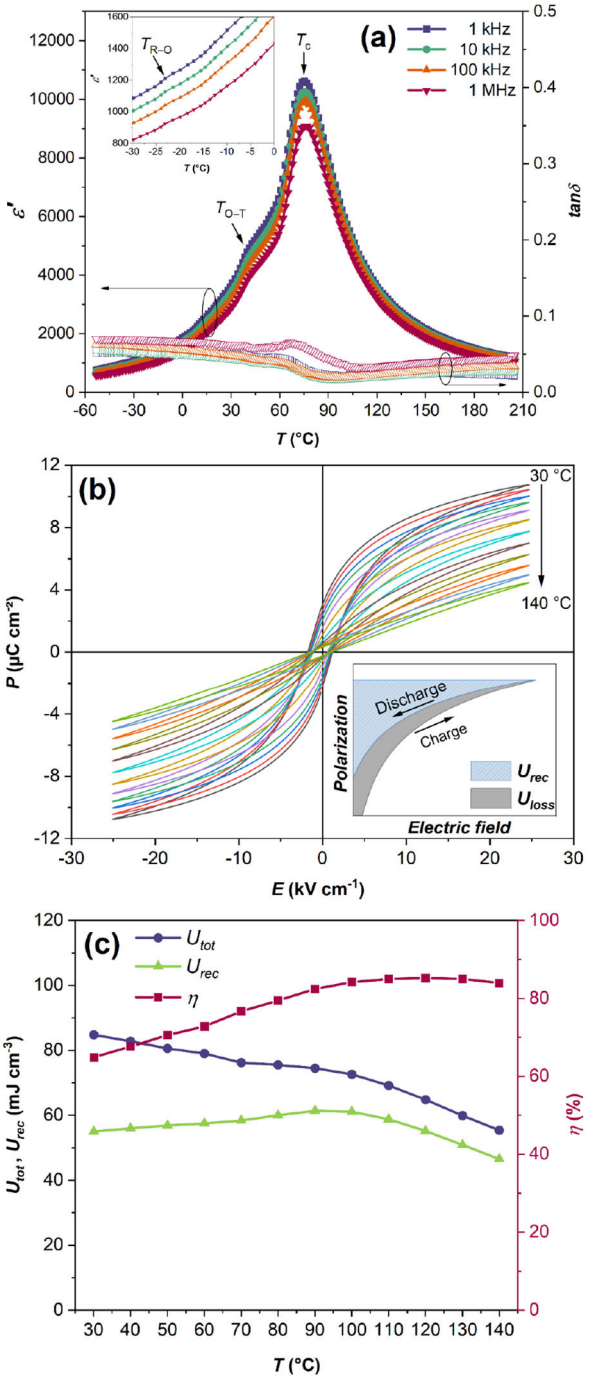

Figure 3: Temperature dependence of (a) *ε´* and *tanδ*, and (b) *P–E* hysteresis loops for 0.4BTSn ceramics. Inset: A schematic depiction of the relevant U_{rec} and U_{loss} determined via *P–E* hysteresis loops. (c) The corresponding energy storage properties as a function of temperature.

The temperature dependence of the dielectric permittivity (*ε´*) and dielectric loss (*tanδ*) of the 0.4BTSn sample are shown in Figure 3 (a). Sequential anomalies corresponding to R–O (T_{R-O}), O–T (T_{O-T}), and tetragonal-cubic (T_c) phase transitions at about –23, 37, and 75 °C, respectively, are observed. The maximum value of permittivity (ε'_{max}) and the peak-permittivity temperature (T_m) were found to be ~ 10630 at ~ 77 °C and 1 kHz, corresponding to a dielectric loss of *tanδ* ~ 0.04.

P–E hysteresis loops at different temperatures are shown in Figure 3 (b). As the temperature increases, the P_{max} decreases continuously due to the ferroelectric-paraelectric phase transition above temperatures around ~ 80 °C. To further investigate the energy storage properties, the recorded *P–E* hysteresis loops as a function of applied electric field and temperature were used. Inset in Figure 3 (b) shows schematically the areas presenting the U_{rec} and the U_{loss} in blue and gray colors, respectively. The total energy density (U_{tot}) can be calculated by integrating and gathering U_{rec} and U_{loss} areas using equations (1) and (2). Therefore, the η can be estimated using equation (3) [41]. The temperature dependence of the energy storage properties is plotted in Figure 3 (c). At room temperature, the U_{rec} value was found to be ~ 55 mJ cm^{-3} with η ~ 65 %, which is twice as high as that of pure BCZT (η ~ 37 %) at 25 kV cm^{-1} [36]. At 120 °C, high η value of 86 % was found in 0.4BTSn ceramic, exceeding that of pure BCZT (η ~ 72%) [36].

$$U_{tot} = \int_0^{P_{max}} EdP \quad (1)$$

$$U_{rec} = \int_{P_r}^{P_{max}} EdP \quad (2)$$

$$\eta\,(\%) = \frac{U_{rec}}{U_{tot}} \times 100 = \frac{U_{rec}}{U_{rec} + U_{loss}} \times 100 \quad (3)$$

For environmentally friendly solid-state cooling devices, the electrocaloric properties of 0.4BTSn ceramics were indirectly evaluated via the Maxwell relation using the measured electric polarization *P* (*T*, *E*). First, a fifth-order polynomial fit of the upper polarization branches was performed at each fixed applied electric field [5]. The thermal evolution of the polarization was

derived. The polarization (*P*) decreases continuously with increasing temperature as presented in Figure 4 (a). The isothermal entropy change (*ΔS*) and the *ΔT* were estimated using Maxwell relation with equations (4) and (5), where *E*, *ρ* and C_p denote the applied electric field, mass density and specific heat of the sample, respectively [5]. The value of C_p (0.48 J g^{-1} K^{-1}) was taken from Ref. [42].

$$\Delta S = \int_{E_1}^{E_2} \left(\frac{\partial P}{\partial T} \right)_E dE \tag{4}$$

$$\Delta T = -\int_{E_1}^{E_2} \frac{T}{\rho C_p} \left(\frac{\partial P}{\partial T} \right)_E dE \tag{5}$$

Figure 4 (b) shows the temperature dependence of *ΔT* at different applied electric fields. The T_{O-T} and T_c are visible and more pronounced with increasing the applied *E*. The maximum *ΔT* was found to be around the T_c. As the *E* increases, *ΔT* increases and its maxima

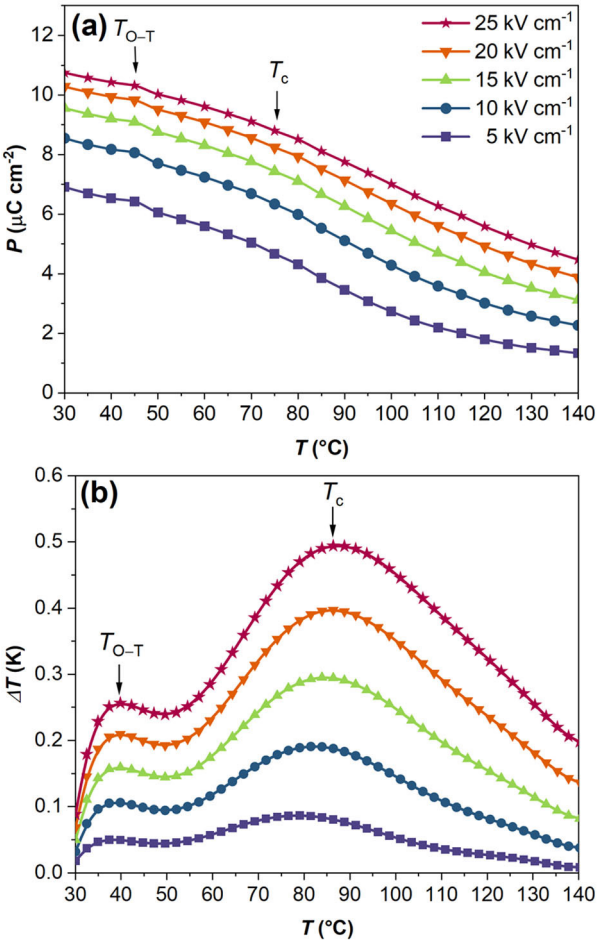

Figure 4: Temperature dependence of (a) *P* and (b) *ΔT* of the 0.4 BTSn ceramics measured at different applied electric fields from 5 to 25 kV cm^{-1}, showing the transition temperatures T_{O-T} and T_c.

shift slightly to higher temperatures. At 25 kV cm^{-1}, *ΔT* reaches a maximum of 0.5 K at 86 °C, then gradually decreases. A crucial parameter for evaluating the EC effect of a material is the EC responsivity, written as $\zeta = \Delta T/\Delta E$. This calculated coefficient was found to be $\zeta = 0.20$ K mm kV^{-1} at the peak temperature. Table 1 presents comparable results for some of the previously published EC outcomes for lead-free ferroelectric materials compared to 0.4BTSn ceramics.

For practical cooling applications, maintaining a significant EC effect over a wide temperature range (T_{span}) is of great importance. T_{span} is usually specified as the full width at half maximum (FWHM) of the EC peak (at the FE–PE phase transition), which can exceed 45–60 °C at a high EC effect benchmark [43]. The diffuse phase transition has been found to be directly related to the broadened EC peaks at low electric fields [44]. Improved T_{span} value of 65 °C is obtained, which could be explained by the successive phase transitions and to the diffuse phase transition.

Another important parameter for evaluating the suitability of EC materials for use in solid-state refrigeration systems, is the refrigerant capacity $RC = \Delta S.\ T_{span}$ [5]. This parameter *was* found to be 33.1 J kg^{-1}. In addition, the coefficient of performance (*COP* = input power/output cooling power = $|T.\Delta S|/|U_{rec}|$) is considered a crucial parameter for estimating the refrigeration cycle performance and evaluating the efficiency of the material [5]. The calculated *COP* value is 15 at 90 °C, which is higher than some other lead-free [45]–[47]. In summary, the 0.4BTSn ceramics could be an advantageous material for some specific EC cooling systems in a wide temperature range.

Ferroelectric materials with enhanced polarization change upon heating have a high potential for use in pyroelectric energy harvesting [18]. For this reason, the pyroelectric energy harvesting performances of 0.4BTSn ceramic were evaluated. The magnitude of the pyroelectric effect can be evaluated using the Olsen cycle. Figure 5 (a) depicts a diagram illustrating the functioning of the pyroelectric energy harvesting effect employing the Olsen cycle. It involves two isothermal (A→B, C→D) and two isoelectric (B→C, D→A) processes per cycle [18]. The pyroelectric energy density (U_{pyro}), which is achieved in certain temperature and electric field ranges, corresponds to the area A→B→C→D→A, which can be described by equation (6) [48]. The U_{pyro} divided by the total heat energy that is absorbed by this process gives the pyroelectric energy efficiency (η_{pyro}) (see equation 7). Analogous to the EC effect, we define the pyroelectric responsivity (ζ_{pyro}) by the equation (8), when the energy harvesting density can be rationalized by the temperature change of the corresponding Olsen cycle,

$$U_{pyro} = \oint EdP \quad (6)$$

$$\eta_{pyro} = \frac{U_{pyro}}{\rho C_p \left(T_H - T_L\right)} \quad (7)$$

$$\zeta_{pyro} = \frac{U_{pyro}}{\Delta E.\Delta T} \quad (8)$$

Figure 5 (b) shows the high-temperature dependence of U_{pyro} and η_{pyro} at T_L = 30 °C, E_L = 5 kV cm^{-1} and E_H = 25 kV cm^{-1} in 0.4BTSn ceramic. It is observed that U_{pyro} increases with T_H, and the maximum U_{pyro} value is 124.1 mJ cm^{-3} at T_H = 140 °C. Meanwhile, η_{pyro} increases andreaches a maximum value of 0.08 % at T_H = 120 °C. Accordingly, ζ_{pyro} is calculated to be 0.56 × 10^{-7} J cm^{-2} V^{-1} K^{-1}. The obtained pyroelectric energy harvesting parameters are improved compared to some reported lead-free $BaTiO_3$-based ceramics [48], [53], [54]. Accordingly, 0.4BTSn ceramic has the potentials to be used as a working material in pyroelectric energy harvesting applications.

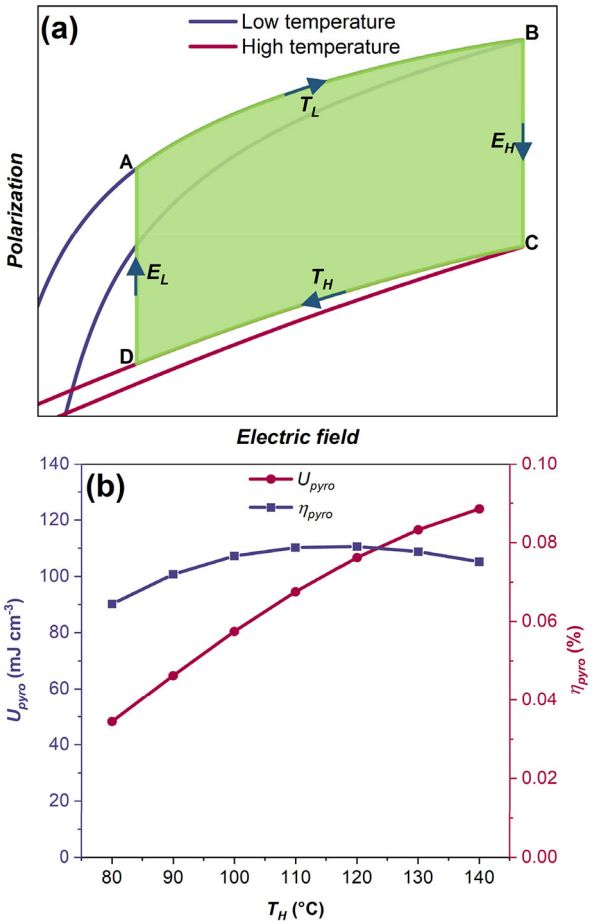

Figure 5: (a) A diagram illustrating the principle of pyroelectric energy harvesting using *P–E* hysteresis loops measured at two different temperatures based on the Olsen cycle. The green region represents the U_{pyro}. (b) The high-temperature dependence of U_{pyro} and η_{pyro} of 0.4BTSn ceramics between 5 and 25 kV cm^{-1}.

4 Conclusions

In summary, the multifunctional lead-free 0.4BTSn ceramic was prepared by the solid-state reaction method. The energy storage, electrocaloric and pyroelectric energy harvesting properties were systematically investigated. Increased energy storage performances (U_{rec} = 61.4 mJ cm^{-3} and η = 82.4 % at 90 °C), electrocaloric properties (ΔT = 0.50 K, ζ = 0.20 K mm kV^{-1}, RC = 33.1 J kg^{-1} and COP = 15 at T_c = 86 °C with T_{span} = 64.9 °C) as well as pyroelectric energy harvesting performances (U_{pyro} = 124.1 mJ cm^{-3}, η_{pyro} = 0.08 % and ζ_{pyro} = 0.56 × 10^{-7} J cm^{-2} V^{-1} K^{-1} at T_L = 30 °C and T_H = 140 °C) were obtained. These results indicate that the 0.4BTSn sample is a good, eco-friendly, and thermally-stable multifunctional ferroelectric material for energy storage, electrocaloric, and pyroelectric applications.

Table 1: Comparison of the electrocaloric properties of 0.4BTSn ceramics with other lead-free BT-based ceramics reported in the literature.

Ceramic	T_c (°C)	ΔT (K)	ΔE (kV cm^{-1})	ζ (K mm V^{-1})	Ref.
$Ba_{0.94}Ca_{0.06}Ti_{0.90}Sn_{0.10}O_3$	47	0.55	20	0.280	[49]
$Ba_{0.85}Ca_{0.15}Zr_{0.10}Ti_{0.90}O_3-0.4BaTi_{0.89}Sn_{0.11}O_3$	86	0.50	25	0.200	This work
$BaTi_{0.89}Sn_{0.11}O_3$	52	0.71	25	0.284	[37]
$Ba_{0.85}Ca_{0.15}Zr_{0.10}Ti_{0.90}O_3$	100	0.57	25	0.228	[36]
0.8$Ba(Ti_{0.89}Sn_{0.11})O_3$–0.2$(Ba_{0.7}Ca_{0.3})TiO_3$	65	0.63	25	0.025	[43]
0.3$BaHf_{0.2}Ti_{0.8}O_3$–0.7$Ba_{0.94}Sm_{0.04}TiO_3$	64	0.46	30	0.180	[47]
$Ba_{0.97}Ce_{0.03}Ti_{0.99}Mn_{0.01}O_3$	55	0.41	30	0.140	[50]
$Ba_{0.85}Ca_{0.15}Zr_{0.1}Ti_{0.88}Sn_{0.02}O_3$	80	0.84	32	0.262	[44]
$Ba_{0.7}Sr_{0.3}TiO_3$	40	0.67	40	0.160	[51]
$Ba_{0.82}Ca_{0.18}Sn_{0.065}Ti_{0.935}O_3$	30	0.59	50	0.118	[52]

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6 Conflict of interest

The authors declare no conflict of interest.

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Design of Capacitive Sensing Chopper Amplifier Used in Artificial Nose Detection System

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Abstract: In this paper, we present the theoretical background and design procedure of a fully differentiated precision charge amplifier that can be used to detect small capacitive changes in an artificial nose detection system (ANose). We will show that with appropriate topology and optimization of circuit parameters, we can reduce 1/f noise and the offset and thus improve the sensitivity while keeping the power consumption at an acceptable level. Since the rate of capacitive changes due to adsorption/desorption is slow, a well-known technique such as chopping and autozeroing is used in a new way and described in the paper. The advantages and disadvantages of the proposed techniques are described. A combination of these two techniques in a single topology and new capacitive sensor ports are used to improve the detection sensitivity. Ideally, a sensitivity of 3 zF/√Hz can be achieved, but it could be slightly worse due to various non-idealities not considered.

Keywords: Fully differential chopper amplifier 1; Capacitive sensors 2; Ripple reduction loop (RRL) 3; Artificial nose 4

Nabojni sekalni ojačevalnik za detekcijo kapacitivnih sprememb v umetnem nosu

Izvleček: V članku je predstavljeno načrtovanje ter teoretičen in simulacijski postopek pri izgradnji popolnoma diferencialnega, natančnega sekalnega nabojnega ojačevalnika, ki služi zaznavanju majhnih kapacitivnih sprememb v sistemu Umetni nos. Pokazali bomo, da lahko s pravilno topologijo in optimizacijo parametrov vezja zmanjšamo 1/f šum in ničelno napetost ter tako izboljšamo občutljivost, hkrati pa ohranimo porabo energije na sprejemljivi ravni. Ker je hitrost kapacitivnih sprememb zaradi adsorbcije in desorbcije relativno počasna, smo uporabili tehniko sekanja in zmanjševanje ničelne napetosti in 1/f šuma. Ti dve tehniki sta v članku uporabljeni na nov način in bosta podrobneje opisani. V nadaljevanju sledi opis prednosti in slabosti predlagane tehnike. Kombinacija obeh tehnik sekanja v eni topologiji in nove, diferencialne kapacitivne senzorske povezave se uporabljajo za izboljšanje občutljivosti zaznavanja. Teoretični izračun kaže, da je v idealnem primeru možno doseči občutljivost 3 zF/sqr(Hz). V realnosti pričakujemo nekoliko slabšo občutljivost, zaradi različnih neidealnosti, ki jih nismo upoštevali pri teoretičnem izračunu.

Ključne besede: Popolnoma diferencialen sekalni ojačevalnik 1; Diferencialni kapacitivni senzorji 2; RRL 3 ; Umetni nos 4.

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1 Introduction

The development and optimization of a detection system for artificial nose (ANose) with increased sensitivity for measuring small changes in differential capacitance represents a significant improvement in sensor technology. The collaboration between LMFE, JSI and FKKT in improving the ANose system emphasizes the importance of interdisciplinary collaboration in improving sensor capabilities [1] - [7].

The transition from an existing ANose system with thirty differential capacitive sensor pairs and thirty ASICS [2, 7] to a new integrated system with 256 capacitive sensor pairs integrated on a single ASIC shows promising progress in sensor array technology and ANose. The integration of the electronics for all channels on a single ASIC requires the development of an extremely low-noise input charge amplifier with minimal area and low power consumption. This innovation is essential for

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accurate measurements of small capacitive changes on modified capacitors due to adsorption processes.

The focus of the work is to analyze the influence of different noise sources that affect the overall noise during the measurements and to design a circuit that can improve the noise characteristics. This analysis is crucial for optimizing the noise performance of the new system. Through a detailed analysis of the chopping technique, the capacitive sensor setup and the ripple reduction loop (RRL), the paper provides valuable insights into the design considerations and techniques used to achieve high sensitivity and low noise in the ANose system. The inclusion of simulation results in the paper adds a practical dimension to the theoretical framework and demonstrates the effectiveness of the proposed design and techniques.

The article is organized as follows. Section 2 presents the basic concept of the chopping technique. A one channel of ANose with the proposed capacitive sensor and the connection of a specially arranged chopper amplifier to the differential capacitive sensor pair is discussed in Section 3. The working principle of the ripple reduction loop (RRL) is described in Section 4. Section 5 presents some simulation results, while the last section concludes the article.

2 Chopping technique

The use of the chopping technique in the amplifier design for the ANose detection system is well justified. Chopping is a well-known method for attenuating offset voltage, 1/f noise and other unwanted artifacts in CMOS amplifiers, especially when amplifying small, low-frequency signals. In the context of the ANose detection system, which involves measuring extremely small changes in the capacitance, it must be ensured that the noise contribution and offset voltage of the amplifier do not distort the small signals. By designing a chopper amplifier, the system should effectively suppress these noise sources and maintain the integrity of the measured signals, allowing accurate detection of capacitance changes caused by adsorption processes. The use of a chopper amplifier in this application is a thoughtful approach to overcoming the challenges associated with amplifying and capturing small signals in a high-precision sensor system. By taking advantage of chopping, the design can improve signal quality, increase sensitivity and minimize the effects of noise and offset voltage, optimizing the performance of the ANose sensing system to detect small capacitance changes.

For this reason, we have developed a chopper amplifier. The operating principle is shown in a simplified block diagram in Figure 1. a) [9]. The challenges associated with DC input offset voltage and 1/f noise in CMOS amplifiers are significant, especially in high-precision applications such as the ANose sensor system. To combat the effects of 1/f noise, it is critical to select a chopper frequency in the amplifier design that exceeds the 1/f noise corner frequency of the amplifier. In addition, with this approach we may also measure the noise spectrum caused by the adsorption/desorption process in a band up to several 100kHz.

In the chopper amplifier configuration, the input signal is first subjected to upward modulation, where the signal is modulated to a higher frequency. Both the 1/f noise and the offset voltage of the amplifier are then added to the high frequency modulated signal. The amplified signal, including the noise and offset, is then modulated again with the same frequency, resulting in demodulation of the signal back to a lower frequency, while the offset voltage and 1/f noise are modulated upwards. This demodulation technique effectively separates the desired signal from the unwanted noise and offset components by up-modulating the noise and offset so that they can be removed later in the process.

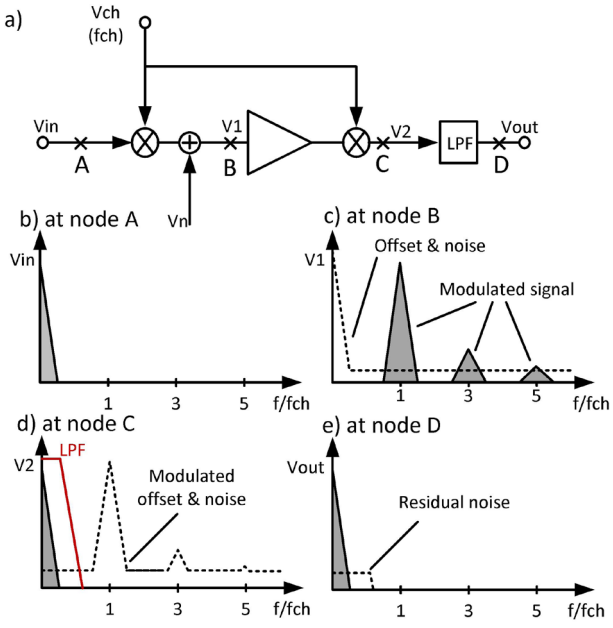


Figure 1: Simplified block diagram of chopper amplifier with spectrums in various nodes. a) Block diagram of chopper amplifier. b) Spectrum of the input signal Vin (node A), c) Spectrum of offset and noise together with the modulated input signal after amplification (node B), d) Spectrum after the second chopper (node C). The red shape represents the transfer function of a first order LPF filter, and e) the spectrum after the LPF (node D).

By integrating this modulation-demodulation approach into the design of the chopper amplifier, the system can effectively counteract the effects of 1/f noise and offset voltage of the circuit. Consequently, this strategy improves the overall quality and precision of the signals and facilitates the detection of small capacitance changes. In addition, the application of low-pass filtering in the system attenuates high-frequency components, as shown in Figure 1e). It is obvious that the chopper technique contributes to the reduction of 1/f noise and offset voltage when the chopper frequency exceeds the 1/f noise corner frequency of the amplifier. Furthermore, it is important to recognize that in practical scenarios, the level of thermal noise at the output of a chopper amplifier may slightly exceed that of a standard amplifier due to the folding of the thermal noise. In addition, charge injection effects may occur during operation of the amplifier, which must be taken into consideration [10]. To summarize, the integration of chopper amplifiers with modulation-demodulation techniques together with low-pass filtering is a powerful strategy to attenuate the noise and the offset voltage problems, ultimately improving signal quality and accuracy.

3 One channel of ANose system

Figure 2 shows the simplified circuit diagram of one channel of the measuring system amplifier, which contains several important components for accurate signal processing. The programmable input DC signal source generates two DC voltages, Vsp and Vsn, which serve as input signals to the system. These DC voltages are chopped by the input differential chopper Ch01, resulting in the square wave signals Vin1 and Vin2; chopping frequency is programmable. They are connected to a pair of capacitive differential sensors as shown in Figure 2. The charges coming from the sensors are further processed by a low-noise charge amplifier consisting of a Gm1_Gm2 cell, which converts the charges into voltages via a feedback loop consisting of a differential chopper (Ch02) and feedback capacitors Cfb.

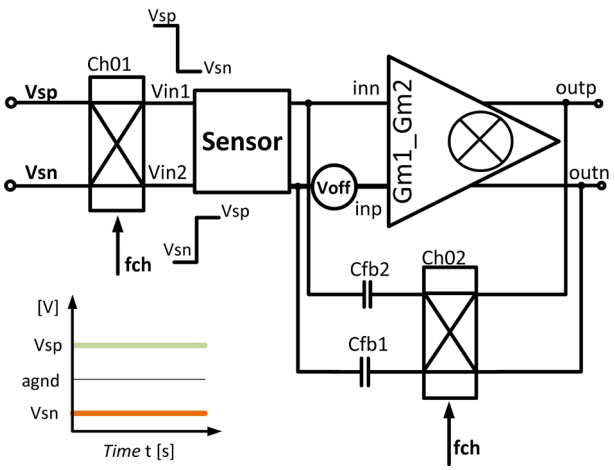


Figure 2: Charge amplifier for one channel of ANose detection system.

The arrangement of the components in this amplifier channel shows a systematic approach to signal processing and amplification. By using chopping techniques and incorporating feedback mechanisms, the amplifier design aims to increase sensitivity, reduce noise and optimize signal integrity for accurate detection of small capacitance changes in the ANose detection system. It is important to note here that the signal coming from the sensor due to capacitive changes can be several orders of magnitude smaller than offset or 1/f noise; fortunately, with correct signal processing it appears in different frequency band.

The integration of programmable input signals, differential chopping and a low-noise charge amplifier illustrates a comprehensive approach to signal processing in the measuring system. This design enables the precise measurements of extremely small capacitance variations and improves the overall performance and sensitivity of the ANose sensor system. The signal processing scheme shown in Figure 2 assumes that the chopping frequency exceeds the 1/f corner frequency of the amplifier. The signals Vin1 and Vin2 are square wave signals with a frequency fch and amplitudes of Vsp-Vsn, which represent the DC voltage difference between Vsp and Vsn. It is important to note that signals Vin1 and Vin2 are 180° out of phase; when Vin1 is connected to Vsp, Vin2 is connected to Vsn and vice versa (see Figure 3:a).

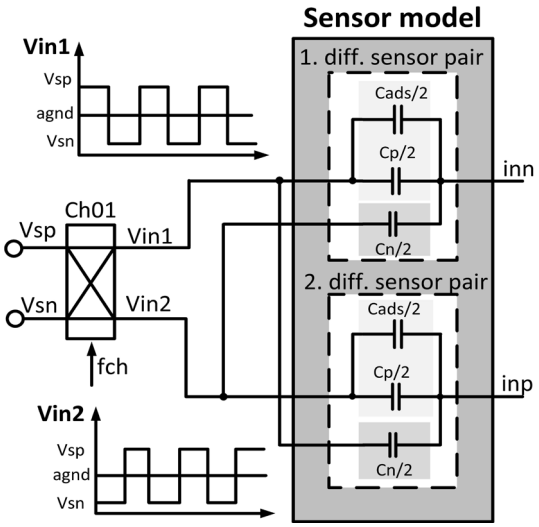
The details of the connection of the input voltages Vin1 and Vin2 to the capacitive differential sensor are shown in Figure 3.a. A sensor consists of two differential sensor pairs with a comb-like structure (see Fig. 3 b). Comb capacitors are covered with a thin layer of silicon dioxide. Each pair is then functionalized with different receptor molecules [1].

The measurement of sensor capacitance changes due to the adsorption of target molecules are significantly influenced by the electric field. In humid air, the breakdown voltage—where the air becomes conductive due to ionization—ranges from 5 to 10 megavolts per meter (MV/m). For 1um space between fingers of comb sensors capacitors and sensing voltage of 5V, we are already at the limit. However, it is possible to reduce the sensing voltage but then also the sensitivity is reduced. In addition, the gap between fingers cannot be smaller because of sensor functionalization technology. This is the main reason why 180 nm CMOS technology is good for our detection system.

Assuming that surface of Cp is functionalized, and surface of Cn is not functionalized, the adsorption of target molecules changes the capacitance Cp, while the capacitance Cn remains the same. The capacitance changes due to adsorption are represented by Cads1 and Cads2 on Figure 3.a. The signal connection structure ensures that the differential signal generated by the sensor pair is effectively detected and processed by the differential charge amplifier, so that the charges at the output of the charge amplifier are effectively converted into differential voltage. To detect these small differential capacitance changes, each part of the sensor is divided into two parts to extract differential charges across the inn and inp nodes.

By organizing the sensor structure in this way, two pairs are formed as shown in Figure 3. The first pair includes

(a)



(b)

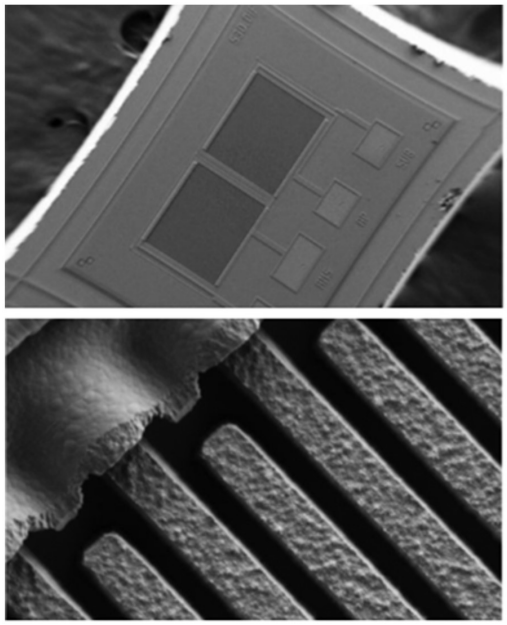


Figure 3: a) Differential capacitive pair connection; b) Comb capacitive sensor.

Cp1 + Cads1 and Cn1, while the second pair consists of Cp2 + Cads2 and Cn2. In addition, the signals Vin1 and Vin2 are connected to the differential sensor pairs, as shown in Figure 3. Vin1 is connected to a node consisting of capacitors Cads1 and Cp1, while Vin2 is connected to a node with Cn1. In the second differential sensor pair, the Vin2 signal is connected to Cads2 and Cp2, while Vin1 is connected to Cn2.

At this point we assume that Vsp -Vagnd = Vagnd - Vsn = Vs, so that the charges in time (n-1) and (n) at the first differential sensor pair at inn and assuming that the sensors are connected to the virtual ground of the charge amplifier are (1) and (2):

$$q(n-1) = (V_s(n-1) - \mathrm{Vagnd}) \cdot \left(C_{ads1} + C_{p1} - C_{n1}\right) \quad (1)$$

$$q(n) = (V_s(n) - \mathrm{Vagnd}) \cdot \left(C_{n1} - C_{ads1} - C_{p1}\right) \quad (2)$$

Charges in time (n-1) and (n) on the second differential sensor pair on inp are given by (3) and (4):

$$q(n-1) = (V_s(n-1) - \mathrm{Vagnd}) \cdot \left(C_{n2} - C_{ads2} - C_{p2}\right) \quad (3)$$

$$q(n) = \left(V_s(n) - \mathrm{Vagnd}\right) \cdot \left(C_{ads2} + C_{p2} - C_{n2}\right) \quad (4)$$

Now let's take a closer look at the signals in the time domain and parts of the charge amplifier. For one differential capacitive pair, and if Vsp = - Vsn = Vs, we can calculate the voltage step Vin1 on one capacitor pair according to (5):

$$\mathrm{Vin}_1 = \mathrm{V}_{sp} - \mathrm{V}_{sn} = 2\ \mathrm{V}_s = \Delta\mathrm{Vin} \quad (5)$$

The same is true for the second differential pair (6):

$$\mathrm{Vin}_2 = -\mathrm{V}_{sn} - \mathrm{V}_{sp} = -2\ \mathrm{V}_s = -\Delta\mathrm{Vin} \quad (6)$$

$$\left|\mathrm{Vin}_1\right| = \left|\mathrm{Vin}_2\right| = \Delta\mathrm{Vin} \quad (7)$$

The signals Vin1 and Vin2, generated after the first chopper in the circuit in Figure 3, have rectangular shapes with a step size of ΔVin, as suggested in (5), (6) and (7). These waveforms consist of transitions between two different voltage levels, resulting in a square wave or a rectangular waveform at the output. The step size ΔVin indicates that the amplitude is the difference between the high and low voltage levels Vsp and Vsn. Assuming an ideal amplifier (block Gm1_Gm2) with an offset voltage of zero and assuming that Cp = Cn and Cads=0 and also that the nodes inn and inp are at virtual ground potential, the charge conservation equation for the simplified single-ended circuit during the transition of the input signal from low to high at Vinp

(or from high to low at Vinn) can be expressed as equation (8):

$$\left[\Delta Vin\cdot\left(C_{p1}+C_{ads1}\right)-\Delta Vin\cdot C_{n1}\right]+ \\ +\left[\left(Voutn\left(n\right)-Voutn\left(n-1\right)\right)\cdot C_{fb1}\right]=0 \quad (8)$$

For Cads=0 the output voltages are equal, therefore:

$$Voutn\left(n\right)=Voutn\left(n-1\right)$$

At the transition from high to low, the circuit behaves similarly to the transition from low to high, but with reversed polarity, since the input voltage jump by –ΔVin, and thus the changes in the output voltages also have reversed signs. If the capacitances Cads1 and/or Cads2 are no longer zero, the output voltages are also no longer zero:

$$Voutp\left(n\right)=Voutp\left(n-1\right)+\frac{C_{ads1}}{C_{fb2}}\Delta Vin \quad (9)$$

$$Voutn\left(n\right)=Voutn\left(n-1\right)-\frac{C_{ads2}}{C_{fb1}}\Delta Vin \quad (10)$$

Looking differentially and if $C_{fb2}=C_{fb1}=C_{fb}$:

$$Vout_{diff}\left(n\right)=Vout_{diff}\left(n-1\right)+\Delta Vin\cdot\frac{C_{ads1}+C_{ads2}}{C_{fb}} \quad (11)$$

The differential output voltage is proportional to ΔVin and the ratio between (Casd1 +Cads2) and Cfb.

The first sub cell within the amplifier block gm1_gm2, called gm1, acts as a transconductance amplifier. This sub-cell converts the input voltage applied to node inn into an output current as defined in equation (12).

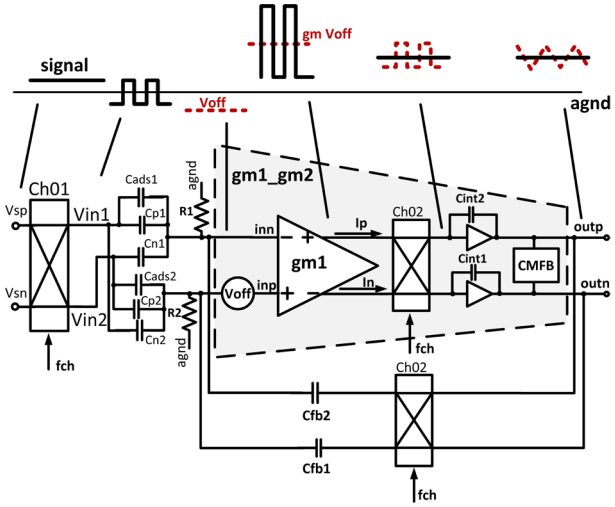


Figure 4: Charge amplifier with signals in the time domain. Black signals are caused by Cads, while signals in red are due to the offset voltage of the op-amp.

$$ip\cong\left(\frac{\frac{C_{ads1}}{C_{fb2}}\Delta Vin}{A}\right)\cdot g_{m1} \quad (12)$$

Table 1: Value of charge amplifier parameters.

Parameters of charge amplifier			
Cads	100fF	Cp1, Cp2	200fF
Ain	1V	Cn1, Cn2	200fF
vdd	5V	R1, R2	30kΩ
Voff	5m	Cint1, Cint2	250fF
agnd	2.5V	Cfb_1, Cfb_2	200fF
Vsp	3.5V	fch	1M
Vsn	1.5V		

It is assumed that the influence of the parasitic capacitance at the inn node on the circuit is negligible, assuming ideal behavior in the time domain. The expression containing gm1 as the trans-conductance of the first stage and A as the ideal open-loop gain of the entire amplifier gm1_gm2 refers to the operating characteristics of the amplifier block. A similar expression applies to the input inp. The chopper Ch02 reverses the connection of ip and in into two integrator stages; they convert currents to voltages and at the same time serve as low-pass filters. The voltage at the output of the integrator is calculated from equation (13):

$$Voutp\left(t\right)=Voutp\left(0\right)+\frac{ip\cdot t}{C_{int2}}= \\ =Voutp\left(0\right)+\frac{\left(\frac{C_{ads1}}{C_{fb2}}\Delta Vin/A\right)\cdot gm1\cdot t}{C_{int2}} \quad (13)$$

Since ip = -in, the voltages Voutp and Voutn at the end of Tchp/2 are Voutp = -Voutn. This condition indicates an antiphase relationship between the output voltages at the end of the first half of the chopping period. At the transition from (inn, inp) to (outp, outn), the cell gm1_gm2 acts as a voltage amplifier, with Voutp and Voutn representing integrated versions of the output currents (ip, in) derived from gm1.

The common mode feedback loop (CMFB) serves as a correction mechanism for the common mode output voltage. By using two integrators in the circuit design, the currents ip and in are effectively converted into two voltages. Up to this point, we have neglected the offset voltage of the amplifier. If we add the model of the offset voltage of gm1 to equations (12) and (13), we obtain equation (14). This equation gives a more detailed insight into the total output current (ip, in), taking into account the characteristics of the transconductance and the effects of the offset voltage of the gm1 amplifier.

$$ip = \left(\frac{\frac{C_{ads1}}{C_{fb2}} \Delta Vin(t)}{A} \right) \cdot g_{m1} + \frac{V_{off}}{2} \cdot g_{m1} \quad (14)$$

The current ip is now made up of both the direct current component (DC), which is caused by the offset, and the alternating current component (AC), which is caused by the input voltage. This combined current is then chopped with Ch02, a component that reverses the connection of the currents to two output stages. Under ideal conditions, the process is equivalent to multiplying each signal by ±1, so that the measured signal is down sampled, and the offset is up-sampled. See Figure 4 for time domain signals and Table 1 for values of simulation parameters. The voltages Voutp and Voutn at time t are calculated according to equation (15):

$$V_{outp}(t) = V_{outp}(0) + \frac{C_{ads1} g_{m1} \Delta \boldsymbol{Vin} t}{C_{fb2} C_{int2} A} + \frac{\boldsymbol{v_{off}} g_{m1} t}{C_{int2}} \quad (15)$$

Equation (18) represents the complete output voltage, (16) represent the DC part, while (17) represent the V_{AC} part.

$$V_{DC} = \frac{C_{ads1} g_{m1} \Delta \boldsymbol{Vin}}{C_{fb2} C_{int2} A} t \quad (16)$$

$$V_{AC} = \frac{\boldsymbol{v_{off}} g_{m1}}{C_{int2}} t \quad (17)$$

$$V_{outp}(t) = V_{outp}(0) + V_{DC} + V_{AC} \quad (18)$$

V_{DC} is contribution of Cads1 and V_{AC} is contribution of the offset voltage (voff) and the 1/f noise of the gm1 cell.

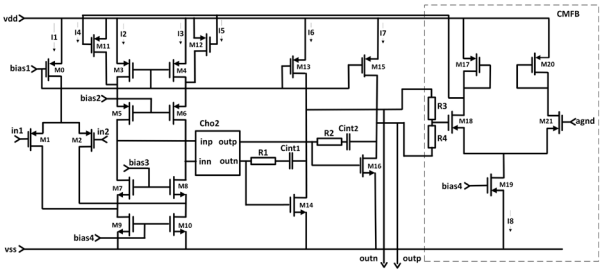


Figure 5: Simplified circuit diagram of gm1_gm2 cell.

Figure 5 shows simplified circuit diagram of gm1_gm2 cell. It is built as modified folded cascode amplifier that implements a gm1 part of the cell using PMOS folded cascode circuit. The output currents are chopped using chopper Cho2, which is constructed from for CMOS switches, followed by two integrator stages. The common mode feedback amplifer(CMFB) controls the common-mode output voltage levels through the gm1 stage. The value of transistors dimensions, supply current, bias voltage and passive component of gm1_gm2 cell are presented in Table 2.

The ripple caused by the offset voltage, which is transferred to frequency fch, can significantly affect the signal quality and accuracy.

Table 2: Dimensions of transistors, supply current, bias voltages and passive components of gm1_gm2 cell.

Parameters of gm1_gm2 cell			
Mo	$16 \frac{10u}{2u}$	R1, R2	5kΩ
M1, M2	$4 \frac{24u}{1u}$	R3, R4	1.5MΩ
M3, M4	$12 \frac{10u}{2u}$	bias1	4V
M5, M_6	$16 \frac{10u}{0.5u}$	bias2	3.668V
M7, M_8	$16 \frac{8u}{1u}$	bias3	1.187V
M9, M_{10}	$24 \frac{8u}{2u}$	bias4	0.9V
M11, M12	$4 \frac{10u}{2u}$	I1	80uA
M13, M15	$32 \frac{10u}{2u}$	I2, I3	60uA
M14, M16	$8 \frac{8u}{1u}$	I4, I5	20uA
M17, M20	$4 \frac{10u}{2u}$	I6, I7	160u
M18, M21	$4 \frac{4u}{1u}$	I8	40u
M19	$8 \frac{8u}{2u}$	agnd	2.5V
vdd	5V	vss	0V

For example, if we have an offset voltage of 10mV, the amplitude of the AC voltage at the chopping frequency for fc=1 MHz, transconductance of 0.1mS and Cint=10pF, the calculated output AC voltage, also known as ripple voltage, is 50mV. To attenuate or remove this ripple caused by the offset voltage (and 1/f noise), we could use LP filtering, however more efficient and better technique is so called ripple reduction loop (RRL), that will be described in the next section.

3.1 Ripple reduction loop

The ripple at the output due to the modulated offset and 1/f noise of the transconductance amplifier cell gm1 is undesirable as it can affect the accuracy and

performance of the system, especially in applications with low frequency signals such as ANose. There are several effective techniques to mitigate this ripple, such as filtering techniques and other suppression techniques described in the literature [9], [10]. It is crucial to address this issue as excessive ripple can eat up headroom and degrade the quality of the output signals. One approach to reduce the ripple is the ripple reduction loop (RRL) shown in Figure 6 and the value of parameters are listed in Table 3.

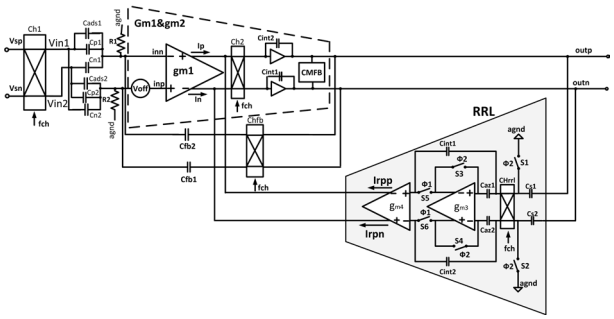


Figure 6: RRL that consists of sensing capacitors Cs1, Cs2, a demodulating chopper CHrrl, autozeroed S-C integrator and a compensation transconductor gm4.

Table 3: Parameters of RRL that are used in simulation.

Parameters of RRL			
Caz1, Caz2	33fF	$Cint1_{RRL}$, $Cint2_{RRL}$	33fF
Cs1, Cs2	33fF	fch	1MHz

RRL is specifically designed to detect the ripple at the output of the voltage amplifier. As soon as the ripple is detected, the RRL generates compensating currents to compensate the DC offset current generated by the transconductance amplifier gm1. Ideally, it is possible to reduce the ripple completely. In the ideal case, the output ripple of the signals Voutp and Voutn should no longer be present after using the RLL technique [8].

Ripple voltage at the output without RRL can be calculated from equation (19):

$$V_{ripple} = \frac{\left(V_{offset} \cdot g_{m1}\right)}{\left(2 \cdot f_{chop} \cdot C_{int}\right)} \tag{19}$$

The ripple caused by the offset voltage can be reduced by decreasing gm1 or increasing Cint. Since reducing gm1 can lead to increased noise, this approach is not effective. Adjusting parameters such as chopping frequency (fch) and integration capacitance (Cint) can affect the residual offset, chip area and power consumption. By using the RRL technique, the system can effectively suppress the output ripple and improve the overall performance and stability of the charge amplifier.

In this paper, an AC-coupled discrete-time ripple reduction loop (RLL) is presented. The block diagram and the components of the ripple reduction loop (RRL) are shown in Figure 6. This diagram illustrates how the RLL is structured, and which are the main components involved in the ripple reduction process.

The ripple reduction loop (RRL) consists of the following important components:

i. Sensing capacitors (Cs1,2). These capacitors Cs1,2 sense and convert the large ripple voltage at the amplifier's output into an AC current, which is proportional to the slope of the ripple.
ii. A demodulating chopper (CHrrl). The demodulating chopper processes the AC current generated by the sensing capacitors, helping to extract and isolate the ripple component for further signal processing
iii. An integrator. It is utilized to integrate the AC current signal, acting as a low-pass filter to smooth out the ripple and convert it into a voltage signal proportional to the ripple amplitude. It serves also as S/H stage.
iv. A compensation trans-conductor gm4. It receives the voltage signal from the integrator and generates compensating currents to compensate the effects of the ripple in the output signals.

The RRL generates a notch at frequency fch with a width determined by flexible design parameters such as Cs1,2 and gm4 [8]. A passive integrator consisting of a current buffer and an integration capacitor used in the RRL has the offset of the current buffer, which produces a second harmonic ripple that would require a large integration capacitor for filtering [10], [11]. In our system, we designed an integrator with automatic zeroing and switched capacitor (see Figure 6), as this is a common technique used in precision analog circuits to reduce offset errors. In this design approach, the integrator is reset during one phase of the operating cycle so that its offset voltage is stored on a self-zeroing capacitor (Caz1,2). The implementation of a self-zeroing switched capacitor (SC) integrator in the circuit enables periodic storage and clearing of the offset voltage. This process minimizes the offset error of the integrator and the S/H stage and improves the accuracy of the circuit by effectively reducing the unwanted voltage offsets of the RLL. However, it is essential to note that the output of the integrator must not be connected to gm4 during the integration phase of the offset cancellation. If such a connection is made, there is a risk that error-compensating currents will be fed into the voltage amplifier (block gm1&gm2). During this time, the voltage at the input of gm4 is kept constant by the voltage stored in the capacitors Cint1 and Cint2.

The SC integrator consists of sampling capacitors Cs1,2, a demodulation chopper CHrrl, integration capacitors Cint1,2, auto-zero capacitors Caz1,2 and a single-stage operational amplifier gm3. CHrrl is synchronised with fch, and the remaining switches (S1-S6) are controlled with the switching frequency faz, which is set to half of fch (see Figure 7). The signal faz contains an integration phase Φ1 and an auto-zero phase Φ2, and each phase comprises a complete cycle of fch. Thus, a ripple can be detected and stored by the full-cycle ripple reduction loop (RRL) operation during Φ1. A timing diagram is shown in Figure 7.

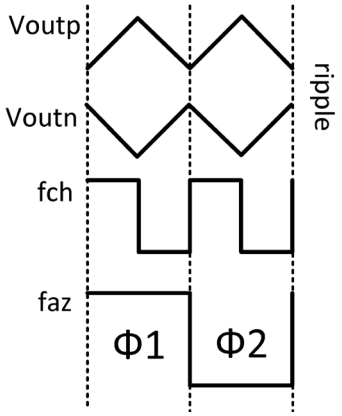


Figure 7: Timing diagram of output ripple, chopping frequency (fch) and auto zeroing frequency (faz), which is set to half of fch.

During Φ1, Cs1,2 plays a critical role in the operation of the circuit by converting the ripple voltage into an alternating current. This alternating current is further processed by demodulation of CHrrl (a demodulating chopper). The demodulated signal is then integrated at Cint1 and Cint2. The voltages at capacitors Cint1 and Cint2 are used to drive gm4, which converts the differential voltage into two currents to compensate for the offset current of gm1. During phase 2 (Φ2), the measuring capacitors Cs1,2 are short-circuited to the analog ground so that no ripple current can be integrated. At the same time, the input voltage at gm4 is kept at a constant level, as the voltages at Cint1 and Cint2 are kept constant during this phase.

This configuration ensures that no additional ripple current is introduced or integrated during Φ2 and the input voltage at gm4 remains stable. Gm3 is configured in the unity gain configuration so that its offset is sampled and stored on Caz1,2. During this time, Cint1 and Cint2 are disconnected from the output of gm3, hold the voltage set at the end of the last Φ1 and are connected to the input of gm4. In this way, the correct compensation current is fed into gm1 in both phases. Ideally, the compensation current fully compensates the offset current of gm1 so that no output ripple occurs in the steady state.

Before looking at the simulation results, let's calculate SnR and minimum capacitance that can be detected using proposed charge amplifier. Assume the BW is 1Hz, Cads = 100fF, Cp = Cn = 200fF, Vndth_in = 10nV/. RMS signal and RMS noise at the output of the charge amplifier can be calculated from equations (20) and (21):

$$V_{sout\_RMS} = \frac{V_{in}}{\sqrt{2}} \cdot \frac{C_{ads}}{C_{fb}} \tag{20}$$

$$V_{ndout\_RMS} = V_{ndth_{in}} \left(1 + \frac{C_{ads} + C_p + C_n}{C_{fb}}\right) \tag{21}$$

The calculated SnR for the proposed conditions is 140dB/√Hz. The minimum capacitance that can be detected, is thus Cads>=2.82· zF/√Hz.

4 Simulation results

The presented topology of a fully differential capacitive coupled chopper amplifier with a differential capacitive sensor pair at the input and RRL was simulated in Cadence using TSMC's 180nm CMOS technology PDK.

The simulation consists of the same blocks as shown in Figure 6. First, a capacitively coupled charge amplifier is simulated when the RRL is switched off. The ripple at the output of the charge amplifier is mainly caused by the offset voltage of the transconductance amplifier gm1. In the simulation, we set the offset voltage of gm1 to 5mV, which corresponds to the typical offset of CMOS amplifiers, Cads = 0fF, Vin = 1V, fch = 1MHz, gm1= 0.1mS and Cint =10pF. The calculated output voltage ripple from equation (19) is Vripple= 25mV and the measured voltage ripple from the simulation is 26mV, which is almost identical (see Figure 8 and Table 4).

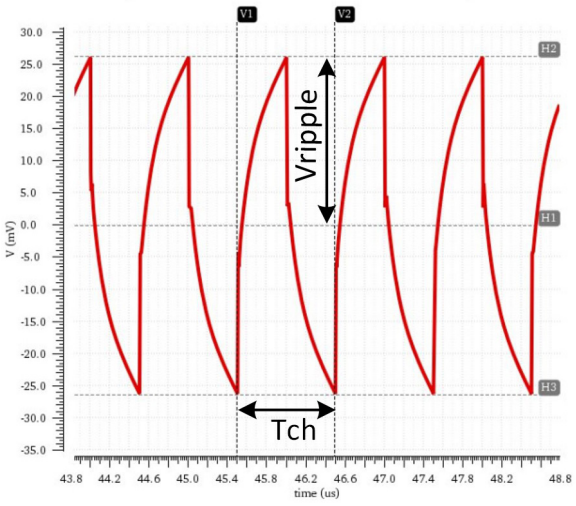


Figure 8: Differential signal at output of charge amplifier without RRL and with Cads is 0.

Figure 9 shows the result (output voltages) when RRL is switched on. It can be seen that RRL can suppress the ripple caused by the offset voltage of gm1 by a factor of approx. 100. If you enlarge the diagram in Figure 9a, you can see that some ripple is still present (see Figure 9b).

The measured ripple is 0.00038 V, as shown in Table 4 in the third row. Then we performed another simulation when Cads was no longer zero. The DC output voltages (see Figure 9 and Figure 10) are calculated using equations (9) and (10). The data used for the simulations are Vin = 1V, Cads1 = Cads2 = 100fF and Cfb1 = Cfb2 = 200fF and the signal ground is Vdd/2 = 2.5V. The DC output voltages are 3V and 2V, i.e. 0.5V, which are different. First, we simulated the system when RRL was switched off.

And then we did a simulation when RRL was switched on. The measured voltage ripple without RRL is 26mV and the measured voltage ripple with RRL is 0,3mV.

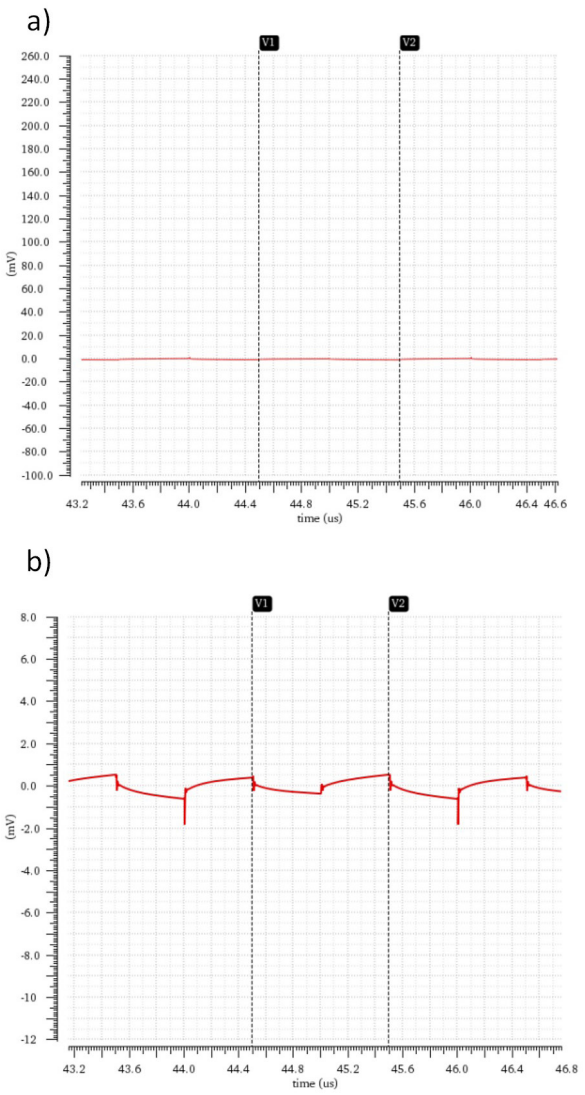


Figure 9: a) Simulation result at the output of the charge amplifier with RRL and with Cads is 0. b) The second graph is a zoom of the first graph in y direction.

The ripple reduction loop (RRL) reduces the ripple voltage by at least a factor of 100, which is the main reason why the RRL is indispensable in our system on a chip. Table 4 shows the different voltage ripples and differential output voltages when changing the values of Cads without RRL and with RRL. It can be seen from Table 4 that RRL effectively suppresses the ripple voltage caused by the offset voltage of a gm1 cell.

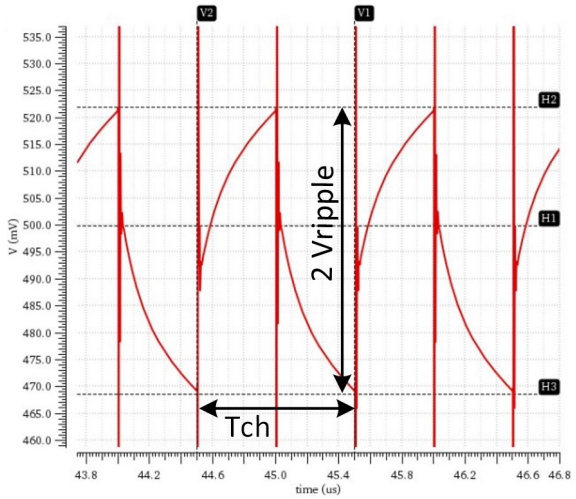


Figure 10: Differential signal at outputs of the charge amplifier without RRL and Cads is set to 100fF.

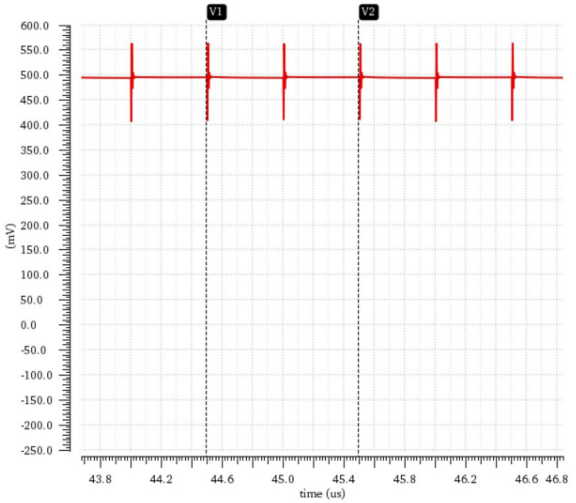


Figure 11: Simulation result at outputs of the charge amplifier with RRL and Cads is set to 100fF.

Table 4: Different values of Cads without and with RRL.

	Cads	RRL	Vripple	Vdiff
1.	0fF	No	0.02608V	0V
2.	100fF	No	0.02634V	0,52V
3.	0fF	Yes	0.00038V	0V
4.	100fF	Yes	0.0003V	0,49V

If we compare the above results with the results from article [8], we find that our system without including RRL has a 10x lower output ripple voltage (Vripple). That means that if we suppress the output ripple voltage by 100x with added RRL, we are left with output ripple voltage in the order of microvolts.

In last decade, a lot of work has been done in field of offset compensation. Article [8] presents a low-power precision instrumentation amplifier for use in wireless sensor nodes with ripple reduction loop, positive feedback loop and DC servo loop. Chip was fabricated in 65nm technology with fixed gain of 100 and BW in Hz, with low supply voltage (1V) and current (1.8uA). They achieve reduction of output ripple by 1000x. The article [12] proposes the use of a so-called fill-in technique to eliminate IMD pulses in chopper amplifiers that is caused by the interaction between the input signal and the chopper clock. The chip was made in 180nm BCD process with 5V supply voltage and 0.55mA with GBW of 4.2MHz with fin of 79kHz. Reported results for fin = 79kHz with fill-in technique is -125.9dB at 1kHz. Article [13] describes amplifier for electroretinography (ERG) and new method dynamic offset zeroing for reduction of large unwanted ripple. The chip was fabricated in 0.18um technology, with supply volage of (0.5 -1.8) V with 7uA supply current. The gain of the system is 60dB and BW of 300Hz. The reported residual ripple in rms is 6mV.

The comparison of results from the literature with our own circuit is difficult, since we try to measure extremely small capacitive changes, while in other work different quantities are measured. However, comparing the remaining ripple of our circuit with the work of [8] shows that, the remaining ripples are similar. Furthermore, the circuitry described in [8] and [13] have smaller bandwidth, compered to ours. The article [12] talks about suppression of CH-induced unwonted IMD tone at a certain frequency, depending on input signal frequency and con not be directly compered with our system.

Our system measures extremely small differential capacitive changes with sensitivity in a range of zF/√Hz with programmable bandwidth in a range of several 100kHz. We think that our simulation results shows that we constructed good system with suppressed ripple by factor of 100x, which means that we are left with less than 0.3mV ripple at the output. This motivates us for future research and system improvements.

5 Conclusions

In this paper, we present the first steps towards building a precision artificial nose detection system comprising 256 differential capacitive pairs and complete front-end electronics for all channels on a single ASIC. The presented topology of capacitive sensors and chopper amplifier with a proposed new topology for differential capacitive sensors is the main contribution. However, the topology requires further optimization.

Other performance parameters need to be addressed and carefully simulated. One of them is the noise characteristics, which directly affect the detection capability and tell us how sensitive our detection system can be and how close the real detection limit is to the theoretical calculation from Section 3. We will also perform other simulations and analysis of the existing topology, including frequency domain simulations, CMRR, PSRR, gain accuracy, etc. We intend to continue work on building an even more complex topology which includes AD conversion. Furthermore, we will compare the simulation results with experimental data in future studies.

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Radiation Analysis of Optimized Wearable Antenna Sensor at 2.4GHz on Human Body for Wireless Body Area Network Applications

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Abstract: The technology of wireless wearable antenna sensors is driving the impressive expansion of wireless body area networks health and wellness monitoring applications. This is because body sensors are regarded as extremely sophisticated data collecting and information systems. Wearable, networked sensors that can be utilized on, inside, or outside of the body are a part of the human anatomy. The most recent international standard for wireless body area networks is IEEE 802.15.6, which attempts to establish a standard for very dependable, short-range, low-power communication inside the human body. In light of this, a study was conducted to investigate on optimal wearable antenna sensors and developed a novel compact slotted planar wearable antenna sensor operating at 2.4 GHz. Additionally, its performance including path loss, channel modeling, power transmitted, power received, and other factors was examined in order to determine how well these sensors would work for IEEE 802.15.6 wireless body area networks applications. This work provides a thorough theoretical and practical investigation of the behavior of the suggested antenna sensor in relation to the human body and free space. The theoretical and experimental results correspond quite well, despite the intricacy of the human body's physiological behavior.

Keywords: Wireless Body Area Networks; Wearable antenna sensor; Channel modeling; IEEE 802.15.6; Human Body

Analiza sevanja optimiziranega senzorja nosljive antene na človeškem telesu pri frekvenci 2,4 GHz za uporabo v brezžičnih omrežjih za telo

Izvleček: Tehnologija brezžičnih antenskih senzorjev, ki se nosijo, je gonilna sila izjemnega razvoja brezžičnih omrežij za spremljanje zdravja in dobrega počutja. Senzorji za telo namreč veljajo za izjemno izpopolnjene sisteme za zbiranje podatkov in informacij. Nosljivi omrežni senzorji, ki se lahko uporabljajo na telesu, v njem ali zunaj njega, so del človeške anatomije. Najnovejši mednarodni standard za brezžična omrežja za območje telesa je IEEE 802.15.6, ki poskuša vzpostaviti standard za zelo zanesljivo komunikacijo kratkega dosega z majhno močjo znotraj človeškega telesa. Izvedena je bila študija, v kateri so bili raziskani optimalni senzorji za nosljive antene, in razvit nov kompakten senzor z režasto ploskovno nosljivo anteno, ki deluje pri frekvenci 2,4 GHz. Poleg tega je bila preučena njegova zmogljivost, vključno z izgubo poti, modeliranjem kanala, oddano in prejeto močjo ter drugimi dejavniki, da bi ugotovili, kako dobro bi ti senzorji delovali za aplikacije brezžičnih omrežij IEEE 802.15.6 za območje telesa. To delo zagotavlja temeljito teoretično in praktično raziskavo obnašanja predlaganega antenskega senzorja na človeško telo in prosti prostor. Teoretični in eksperimentalni rezultati se kljub zapletenosti fiziološkega obnašanja človeškega telesa precej dobro ujemajo.

Ključne besede: brezžična omrežja za območje telesa; nosljivi antenski senzor; modeliranje kanalov; IEEE 802.15.6; človeško telo

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1 Introduction

The proliferation of miniature sensors and the growing use of wireless networks have resulted in network applications that can be used on the human body to provide a wide range of services [1]. These days, the healthcare industry has seen a tremendous transformation because to the advancement of wireless wearable technologies [2]. A wireless body area network (WBAN), is essentially a wireless sensor network (WSN), put together with various nodes, actuators, and sensors, among other intelligent devices. Power consumption for WBAN data transmission is high; therefore selecting the appropriate antenna for a given application is crucial [3]. In this context, the WBAN uses have known a large field of application domains, such as the medical domain [4], the military domain [5], sports [6], multimedia [7], etc.

Antenna sensor designs are crucial for cutting down on power consumption, decreasing channel loss, and boosting throughput. Wearable antenna sensor deployment, however, is hampered by a number of electromagnetic factors that can impair WBAN performance and wireless channel stability, including multipath, human body shadowing, fading and interference effects from signal attenuation, and energy absorption by bodily tissues[8] [9]. The study [10] states unequivocally that the human body is made up of naturally occurring absorbent layers. The attenuation of propagation signals along the human body is caused by these tissue layers acting as a low-loss dielectric medium.

It becomes necessary to reduce multiple electromagnetic variables in order to guarantee reliable body surface-to-body surface communication between the coordinator and the sensor nodes within the human body propagation environment. These include the human body's tissues avoiding radio signal diffraction, reflection, and absorption. Furthermore, characterization and analysis of the behavior of the wireless communication channel between devices installed on the human body become essential due to the complexity of the environment surrounding the human body. Characterizing propagation properties, signal attenuation, interference, and other body-centric limitations is the aim of this endeavor. Furthermore, the design and optimization of resource allocation plans, antenna designs, power control mechanisms, and communication protocols in Body Area Networks depend heavily on precise channel modeling. Furthermore, this latter makes it possible for scientists and engineers to assess and enhance the functionality of wireless connections, guaranteeing dependable and effective communication between implanted or wearable technology and the outside network architecture.

A WBAN is regulated by IEEE Standard 802.15.6. This standard gives WBAN systems access to the physical and media access control levels. As a result, these layers are founded on precise simulations of wireless propagation channels and antenna layouts for various frequency ranges [9]. The IEEE 802.15.6 standard was created expressly to satisfy the requirements of various WBAN-dependent medical applications [1][2]. According to a study by Al Barazanchi et al. (2022) in [10], these applications include remote patient monitoring in healthcare institutions as well as the monitoring of elderly people in their homes. The primary objective of this standard is to enable short-range, energy-efficient wireless communication that can be used for applications on, inside, and around the human body.

Furthermore, there are three different categories for communications in WBAN networks: There are three types of communication: in-body, on-body, and off-body. [11] [8]. In order to account for this, different channel models have been categorized based on the kind of body communication link—in-body, on-body, and off-body [12] [13].

Three possible scenarios for deployment are suggested by the WBAN standard: The human body has three types of nodes: (I) an implant node injected beneath the skin, which can be put in the deep tissues or just beneath the skin; (II) a surface node on the skin's surface; and (III) an external node, also referred to as the Gateway Node. The latter node is off-body and situated a few centimeters away from the skin [8]. In addition, four channel models (CMs) have been established under the WBAN standard: CM1 refers to the implant to implant; CM2 to the body surface model; CM3 to the body surface model; and CM4 to the external model [8] are the body surface to body surface models.

An essential and crucial component of wireless body area networks is the RF antenna sensor, whose design greatly influences factors such as radiation pattern, energy efficiency, directivity, transmission range, and radiation pattern. Over the past ten years, wearable antenna sensors have become increasingly important for on-body applications because of their capacity to identify microstructure deformations, human motions, and to monitor and oversee human health [14].

Standard industrial antenna sensors may offer precise data, but if integrated into body wear for sensing purposes, their large and stiff design restricts the user's movements. Thus, the creation of new antenna sensors that are compact in size, light in weight, low in power consumption, and flexible is crucial for WBAN applications. [15]

When creating WBAN-focused antenna sensors, one of the main study areas is choosing or creating appropriate materials for wearable antenna sensors. While a wide variety of antenna sensors have been produced for WBAN in the past, new and improved designs are constantly being created in response to market requests [16].

Since microstrip patch antennas have so many benefits, including low production costs, light weight, durability and dependability, and compact size, they are typically used in sensing applications. Due to the interaction of electromagnetic waves with dielectric characteristics, these function as sensors. [17][18]

In light of the aforementioned topic, new wearable microstrip antenna sensors optimized for 2.4 GHz were investigated, put into use, and their performance (including path loss, channel modeling, power transmitted, power received, etc.) was examined in order to use them for IEEE 802.15.6 international standard wireless body area networks applications.

2 Literature review

Numerous methods have been put out in the literature for WBAN network path loss performance evaluation and channel modeling, utilizing a variety of analytical channel models as well as numerous experiments and simulations. The literature has presented a number of methods for channel modeling between on-body sensors. Electromagnetic signals go through the human body in WBAN. Because of this, the human body is thought of as a wave propagation medium. The authors of the study [19] discussed, for example, how crucial channel modeling is in body area networks for estimating path gain and link loss using an electromagnetic propagation wave approach.

Furthermore, a number of methods have been presented in the literature to demonstrate the significance of WBAN channel models between on-body sensors for both the deployment of these sensors and their use in the assessment of body area network performance in accordance with IEEE 802.15.6 specifications.

In order to evaluate the effectiveness of the proposed WBAN in terms of energy consumption, packet loss, and radio modulation type, for instance, the authors of the studies[20][21] proposed a simulation and channel modeling of a WBAN network made up of one coordinator and eleven sensor nodes. The channel was characterized using a lognormal shadowing path loss model. Consequently, the authors of some studies [22] and [23] have stated that, for interior situations, the lognormal model is more accurate than the Nakagami and Rayleigh channel models. Additionally, the CM3A and CM3B on-body path loss models suggested by the IEEE 802.15.6 standard have been used by the authors of other studies[24],[25],[26], and [27] for channel modeling between on-body sensors. The two route loss models have been used to the frequency ranges of 2.4–2.45GHz in these investigations by the authors. Tests of CM3's efficacy have been conducted in anechoic chambers and hospital rooms. Furthermore, in the research done in [26], authors examined the effects of power and modulation scheme variations on BAN performance in terms of packets received at the coordinator, packet loss rate, and delay at 2.45 GHz frequency using the CM3B path loss model. Additionally, the CM3B path loss model has been suggested for usage by the authors in [27]. The purpose of this work is to investigate and assess how inter-body area networks interference affects a body area networks energy consumption performance.

However, a number of studies based on human-body phantoms and voxel-human body models have been presented to define the on-body channel between wearable antennas at various frequency bands. For instance, the authors of experiments conducted in[28] [29][30] have demonstrated the applicability of the S21 parameter in channel modeling between wearable antennas and a capsule endoscope that is implanted inside the human body in the small intestine. The various biological tissues have been taken into consideration in these investigations. Additionally, the authors of the study conducted in[31] suggested a patch antenna design operating at 2.4 GHz as well as an analytical channel characterization between two wearable antenna sensors mounted on a straightforward 3D cylindrical phantom. Nevertheless, in this investigation, the human body phantom's muscular tissue was the sole thing taken into account.

More recently, in the same field, the authors presented an analytical and experimental method for simulating the on-body route loss and path gain channel between two wearable antenna sensors for Wireless Body Area Networks in studies[32], [9]. Because the authors created an on-body channel model based on an earlier voxel-based channel model proposed in Hall et al.[33] and Alves et al.[34], these studies[31],[32],[9] generally share certain commonalities. They also suggested comparable experimental and analytical contributions. Even though these studies[31],[32],[9] use novel approaches, the authors neglected to consider the SAR study, which looked at how various antenna sensors behaved in the presence of a human body, particularly the effect of power absorption on bodily safety. They

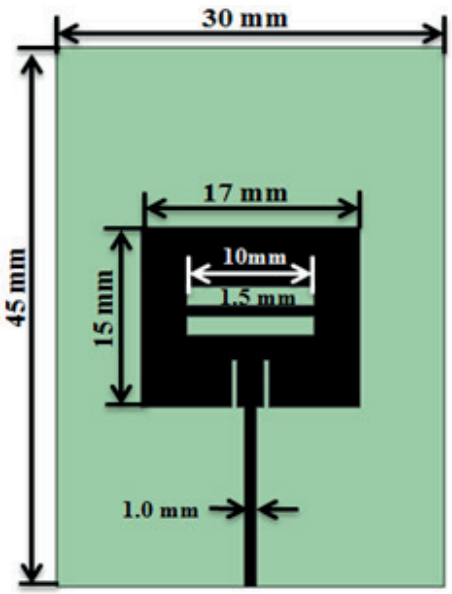
also neglected to use biological tissue such as skin, fat, and muscle for accurate and realistic channel modeling. As a result, the writers just take into account the muscle tissue. Furthermore, without considering the realistic biological properties of the conductivities and permittivities of each human body tissue, the authors of the studies by Hamdi et al.[32] and Hamdi et al.[9] altered the conductivity and permittivity of the human body muscle at random. Because of this, estimated return loss and path loss findings from simulations will be produced, which are not indicative of the real-world circumstances in the channel modeling of the human body environment.

By proposing a rigorous on-body path loss modeling theoretically and experimentally that takes into account the real dielectric biological tissue parameters of a human body and is based on our voxel-based channel model, we hope to add to the body of literature already in existence regarding on-body channel modeling between wearable sensors. Additionally, we aim to take into account the power absorption effects on the behavior of wearable antennas in both free space and the presence of a human body. For this reason, in addition to frequency and the distance between the Tx and Rx antennas, attenuation resulting from the human body should also be taken into account (IEEE 802.15.6 draft).

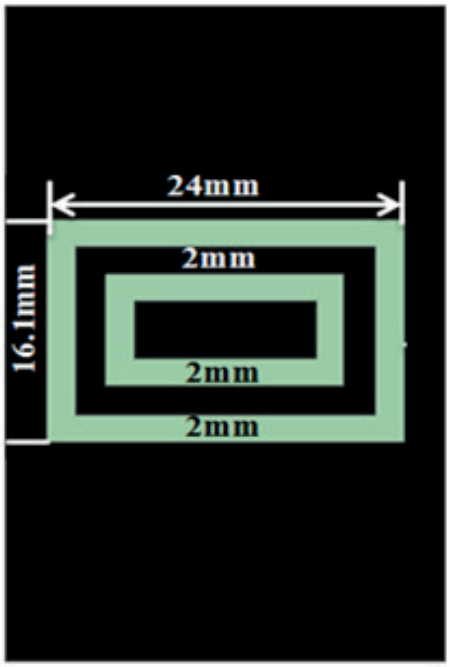
3 Antenna sensor design flow:

This work proposes the use of HFSS-19 Software to operate a rectangular microstrip patch antenna at 2.4 GHz. Using a range of design flows and simulations, we have examined the effects of the human body on antenna performances. The suggested antenna is thought to be a very effective antenna for use in human body applications. The compact slotted Perfect Electrical Conductor (PEC) material is printed on a FR-4 dielectric substrate to create this wearable antenna. Because of its flexibility, this substrate material can be inserted into the body or fabric. Developing and positioning the antenna on the human body in a way that minimizes the impact of power absorption by the tissues is another difficult task. The substrate with a low dielectric constant of 4.3 and low dielectric height of 1.6mm was selected in order to lessen the influence that radiation waves would have on the human body and to have an efficient antenna in terms of radiation patterns.

The slotted ground plane and inset feed line are composed of copper-annealed material, which is advantageous for on-bodies applications since it lessens the power that 2.4 GHz creeping waves absorb from human body tissues. We have changed the printed patch's width, length, and widths of the two inset gaps in order to maximize the suggested antenna's performance in terms of impedance adaptation between the patch and the feed line. Fig. 1 depicts the suggested wearable antenna construction and its dimensional parameters.



(a) Top view



(b) Bottom view

Figure 1: Proposed microstrip antenna sensor

The proposed antenna sensor is developed in the dimensions of 30 x 45 x 1.6 mm^3 with respect to length, width and the height of antenna. It was fabricated and tested to analyze its performance over simulated antenna. The performance analysis is illustrated in results and performance analysis section. The fabricated an-

tenna images and measuring views of antenna under test (AUT) is given as Fig. 2.

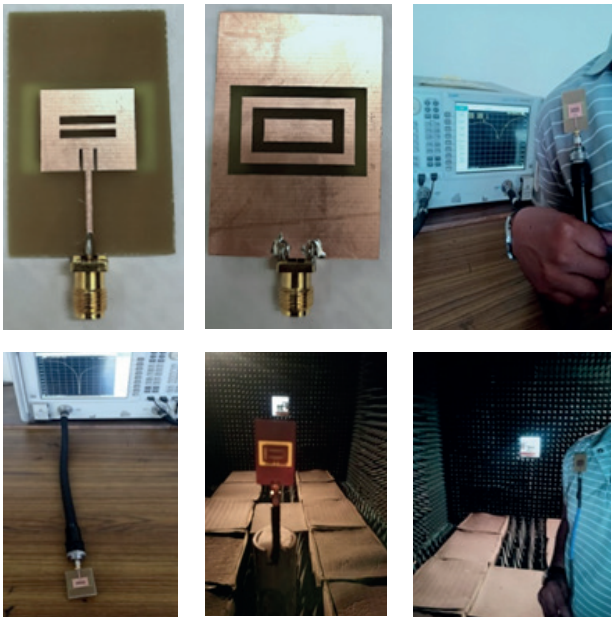


Figure 2: Fabricated and AUT views of proposed microstrip antenna sensor

4 Results and performance analysis

The radiation performance of the proposed antenna sensor is enhanced by incorporating slots on ground and patch as shown in Fig. 1. The radiation behavior of proposed antenna sensor with and without slots on ground and patch was explored below.

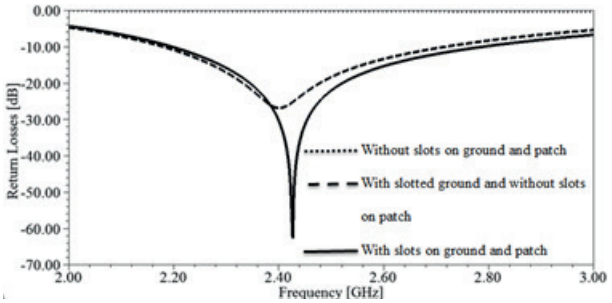


Figure 3: Return losses of proposed microstrip antenna sensor at different stages

In telecommunications measurements, the return loss term represents the loss of power, which have been returned or reflected from an antenna to a transmission line. It's a ratio between the incident power and the reflected power. For improved impedance matching, the return loss measurement should falls below -10 dB line [41], [42]. The proposed antenna sensor without slots on ground and patch is not given any operating band below -10dB and the planar sensor with slotted ground and patch achieved improved return losses than the sensor with slotted ground and without slots on patch at 2.4GHz. The return losses enhancement for different stages of design can observe in Fig.3.

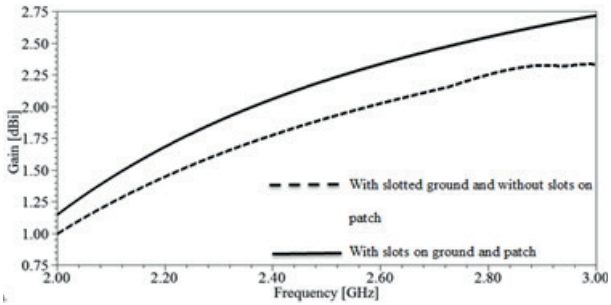


Figure 4: Gain of proposed microstrip antenna sensor at different stages

The gain was extracted for the designs, those showed the return losses less than -10dB and shown in Fig.4. Here also observed the sensor with slotted ground and patch achieved improved gain than the sensor with slotted ground and without slots on patch. The extracted results from different stages of sensor design are listed in Table 1.

Table-1: Results of proposed microstrip antenna sensor at different stages

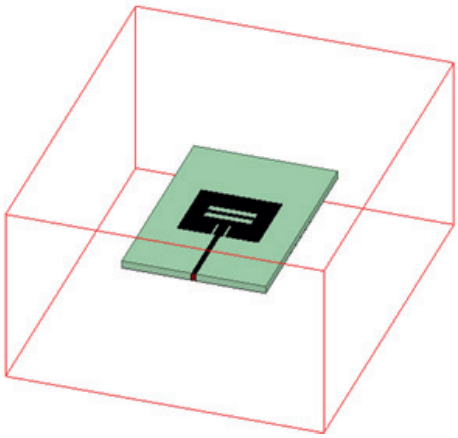
Antenna Sensor Design stage	Frequency (GHz)	Return losses (dB)	Operating band (GHz)	Gain (dBi)
Without slotted ground and patch	-	-	-	-
With slotted ground and Without slots on patch	2.4	-26.88	2.18-2.72	1.78
With slotted ground and patch	2.43	-62.76	2.20 -2.79	2.1

From the above results analysis, it is justified that the proposed antenna sensor with slots on ground and patch reflecting significant radiation than other stages of design. So it was implemented as shown in Fig.1, fabricated and tested as shown in Fig. 2.

4.1 Near field radiation analysis:

With aim to use the proposed antenna sensor for IEEE 802.15.6 international standard wireless body area networking applications, the radiation activities from pro-

posed antenna sensor are observed by mounting the antenna sensor in free space and on human body as shown in Fig. 5 i.e. the radiation behavior of the proposed antenna sensor on the free space and human body is theoretically and experimentally explored as below.



(a) Free space

(b) Human body

Figure 5: Mounting of antenna sensor in free space and on human body

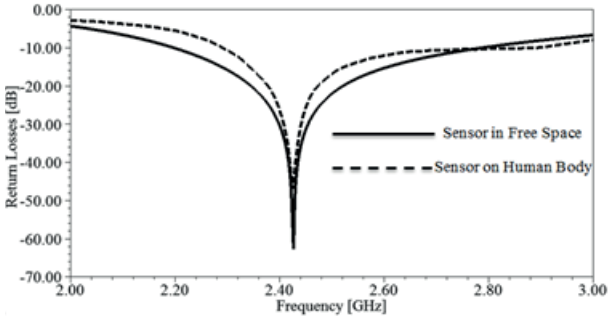


Figure 6: Return losses simulated antenna

Primarily, the performance analysis is done by measuring return losses (reflection characteristics) for simulated and fabricated wearable antenna sensors. The return losses extracted from simulation of the proposed antenna sensor by placing it in free space and on human body was plotted in Fig. 6. Similarly, the return losses measured from fabricated antenna sensor under test by placing it in free space and on human body was plotted in Fig. 7. It's clearly observed from Fig. 6 and Fig. 7 that the antenna exhibit improved impedance matching, as indicated by a return loss measurement that falls below -10 dB line at 2.4 GHz in free space and in human body environments.

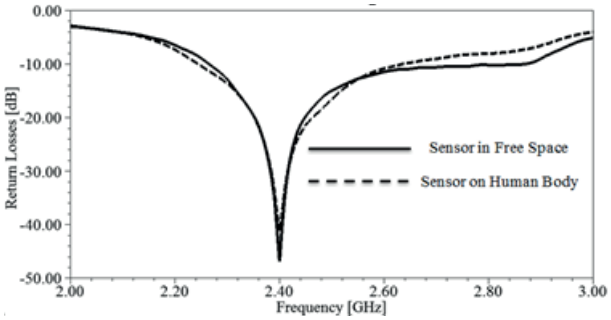


Figure 7: Return losses fabricated antenna

From extracted results of return losses, it was observed more return losses when the antenna placed on human body compared to the return losses when the antenna in free space, it may be due to the highest values of physiological parameters of the human body such as the conductivity of the muscle tissue and the power absorbed by each different tissue layers (Skin, fat, Muscle). The observed reflection characteristics (return losses) of the proposed antenna sensor from simulation and AUT are listed in Table 2.

Power is one of the important radiation characteristic in telecommunications measurements why because the transmission and reflection parameters are related to the power. The incident power on proposed antenna sensor, the accepted power and radiated power by the proposed antenna sensor are measured from simulation and AUT. The respected results are given as Fig. 8 and Fig. 9.

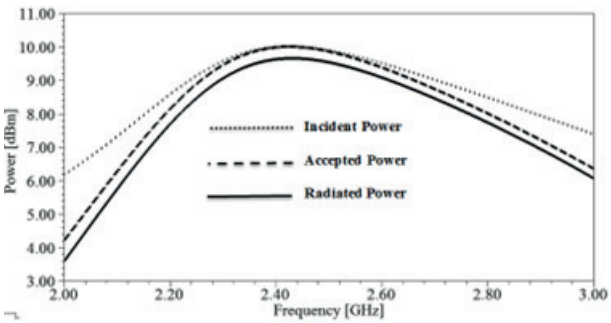


Figure 8: Incident, accepted and radiated powers from simulation of proposed antenna

Table-2: Reflection characteristics of simulated and fabricated antenna

Simulated/ Fabricated	Free Space/ On Body	Operating Frequency band	Peak Resonant Frequency	Return Losses at PRF
Simulated antenna	Free Space	2.20 -2.79	2.43	-62.76
	On Body	2.29-2.9	2.42	-46.88
Fabricated antenna	Free Space	2.26-2.87	2.40	-46.9
	On Body	2.24-2.64	2.40	-41.1

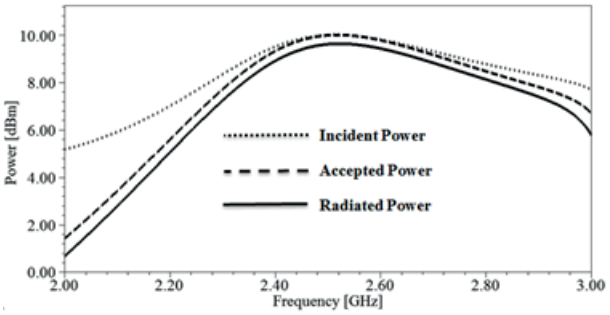


Figure 9: Incident, accepted and radiated powers from measurements of AUT

From the above power measurements, it is observed that, as return losses states, the proposed antenna transmitting more than 90% of incident power. It is the good evidence to the achieved significant return losses as shown in Fig. 6. The Power measurements taken from simulated and fabricated antenna are listed in Table 3.

Table-3: Power measurements of simulated and fabricated antenna

Simulated/ Fabricated	Frequency (GHz)	Incident Power (dBm)	Accepted Power (dBm)	Radiated Power (dBm)
Simulated antenna	2.4	9.98	9.98	9.62
Fabricated antenna	2.4	9.5	9.32	8.91

4.2 Far field radiation analysis:

The analysis of far field radiation is necessary and essential to study the impact of electromagnetic phenomena such as the influence of energy absorption on the power and gain of wearable antenna sensors in free space and especially in the presence of a human body. It is, therefore, necessary to understand the behavior of these devices in free space and in close proximity to the human body, as well as the influence of human body power absorption on the radiation performance of the wearable antenna.

In the Fundamental mode of excitation, the proposed antenna radiates with significant gain towards the direction perpendicular to the patch. Fig. 10 showing the three dimensional (3D) polar gain radiation pattern of proposed antenna at 2.4GHz when it placed on shoulder of on human body. Fig. 11 is the plot of measured and simulated gain over all frequencies in sweep when the antenna in free space and on human body. In the free space environment, the proposed antenna has a gain of 2.1 dBi at 2.4 GHz. In the human body environment, the proposed antenna has a gain of 1.62 dBi at 2.4 GHz. However, according to the obtained results when the antenna is placed on human body, it was noticed a slight decrease of the antenna gain. Therefore, during transition, from free space to human body environment, the peak gain is reduced from 2.1dBi to 1.62 dBi, for proposed antenna sensor.

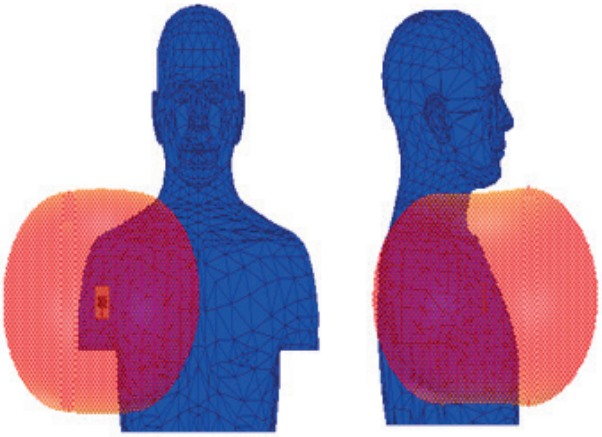


Figure 10: Proposed antenna 3D polar gain pattern of on human body at 2.4GHz

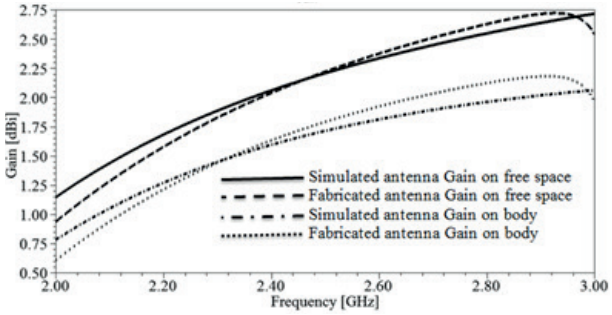
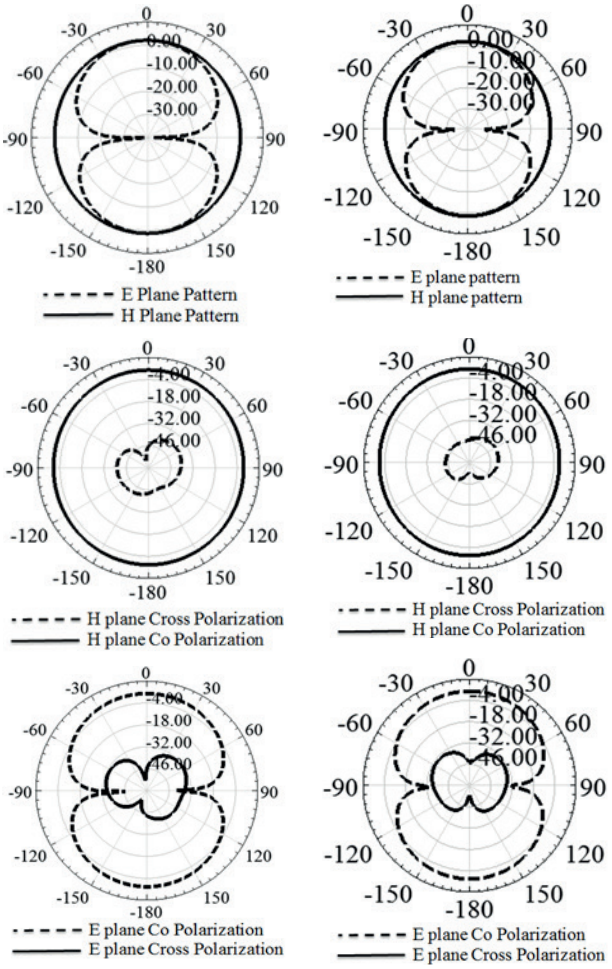


Figure 11: Gain over the sweep when the antenna in free space and on human body.



(a) Co and Cross polarization of proposed antenna in free space environment

(b) Co and Cross polarization of proposed antenna on human body environment

Figure 12: Co and Cross polarizations of proposed antenna at 2.4GHz.

The slight decrease and attenuation in radiation patterns is may be due to the impacts of biological parameters of the human body such as the high conductivity of the muscle, skin and fat tissues. The Co and Cross polarizations of proposed antenna in free space and on human body environments were developed to know matching between the transmitting and receiving antennas.

The co and cross polarization results are shown in Fig. 12 along with principle plane (E & H plane) patterns. From Figure 12, it is observed low cross polarization compared to co polarization and co polarized patterns have same level as principle plane patterns. So, as discussed [35][36][37], if observed low cross polarization compared to co polarization and co polarized patterns have same level as principle plane patterns, the characteristics of both transmitting antenna and receiving antenna are same. So, these observed far field gain radiation characteristics confirm that the proposed wearable designed antenna is suitable for free space and on-body medical applications.

It is summarized in table 4 the performance comparison of the proposed designed antenna with other antennas designed in several recent studies in the existing literature. In comparisons in terms of all performance metrics, it is noticed that the proposed antenna is more efficient than several other antennas presented in the literature.

Table-4: Proposed antenna performance comparisons with previous works

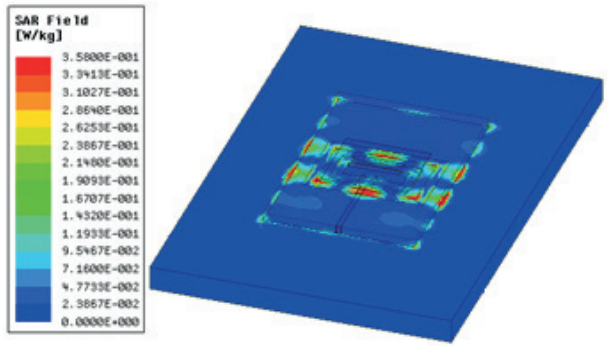
Reference Number	Frequency (GHz)	Return Losses (dB)	Gain
This paper	2.4	-62.76	2.1
[2]	2.4	-43.01	2.61
[31]	2.4	-23.91	-
[9]	2.4	-21	6.37
[38]	2.45	-23.94	-
[39]	2.4	-15	-
[40]	2.4	-22.13	-

4.3 Specific absorption rate (SAR)

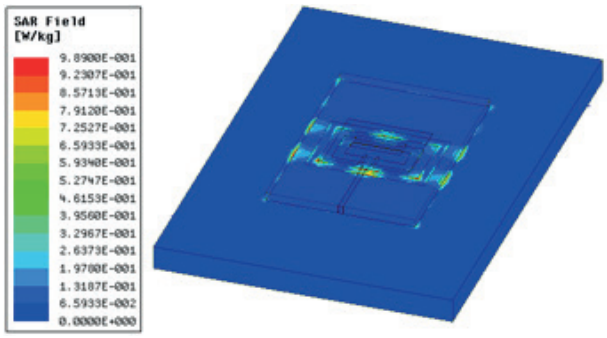
Here presented a Specific Absorption Rate (SAR) analysis of proposed wearable antenna at 2.4 GHz for on-Body medical applications. A Human body is a complex propagation medium, it is highly conductive. As a result, human body tissue leads to additional effect to propagation waves such as diffraction, reflection, shadowing and power absorption. Considering the losses due to the human tissue frequency absorption and the complexity of this propagation environment, one of the most critical challenges in WBAN is the design of efficient wearable antennas and the analyses of the Specific Absorption Rate to protect the human body from radio frequencies and to ensure human body safety. The absorbed power per unit mass of human body is analyzed by the SAR. Moreover, electromagnetic waves radiated by wearable antennas and penetrated in human body tissues can cause harmful and devastating effects of human body. The specific Absorption Rate quantifies electromagnetic energy radiation absorbed by tissues and represents the amount of energy or power deposition per unit mass of biological tissue. The standard unit for SAR is watt per kilogram (W/kg).

According to the study conducted in [2], the international community has standardized and regulated the SAR limitations. The maximum safety limit of SAR specified by the federal Communications Commission

is 1.6 W/kg for 1 g of tissue and 2 W/kg for each 10 g of tissue. In this work, it is calculated the SAR over 1g and 10g of human body tissue and shown in Fig. 13. As shown Fig. 13, it is observed 0.358 W/kg SAR over 1g and 0.989 W/kg over 10g of human body tissue. These SAR results make the proposed antennas suitable for Wireless Body Area Networks and for wearable applications.



(a) SAR for 1g of human body tissue

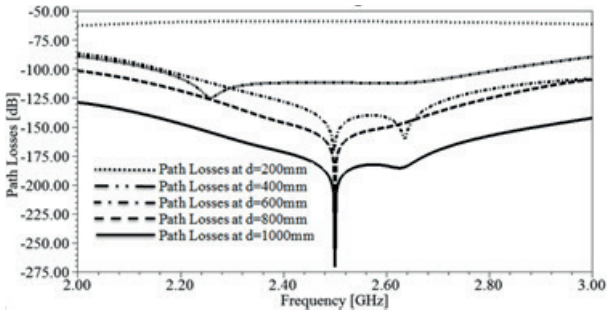


(b) SAR for 10g of human body tissue

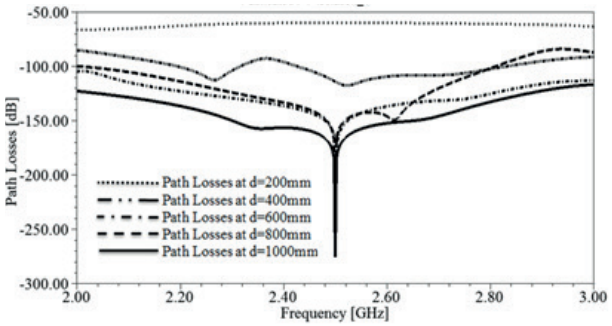
Figure 13: Proposed antenna SAR analysis

4.4 Path loss modeling:

As per the initial report on channel modeling for wearable and implantable Wireless Body Area Networks specified in the IEEE 802.15.6 standard, the S21 parameter serves as the channel parameter employed to measure the path loss between the wearable antennas [2]. Therefore, in this work, it was studied the S21 (path losses) channel parameter for path loss modeling in on-body antenna distances and free space antenna distances. Here, the S21 parameter signifies the path loss between the transmitting antenna and receiving antenna separated with the distance of 'd' mm within the topology of the Body Area Network. The study of S21 is the electromagnetic interaction between the transmitting and receiving antenna elements controlled by varying distance 'd' between them. Actually the S21 and 'd', both are inversely proportional to each other.

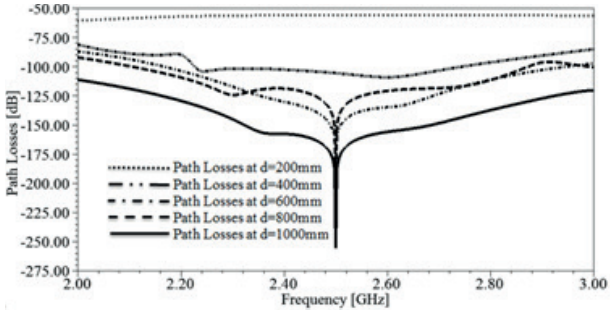


(a) Simulated Path loss characteristics at different values of d

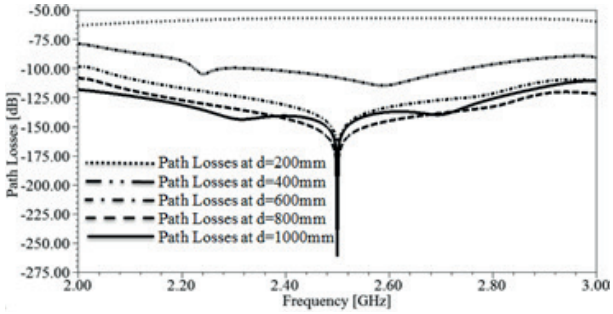


(b) Measured path loss characteristics at different values of d

Figure 14: Path loss characteristics from free space to free space over the sweep



(a) Simulated Path loss characteristics at different values of d



(b) Measured path loss characteristics at different values of d

Figure 15: Path loss characteristics from human body to human body over the sweep

In the proposed work, Fig. 14 (Path loss characteristics from free space to free space over the sweep) and Fig. 15 (Path loss characteristics from human body to human body over the sweep) presents the simulated and measured scattering S21 parameter between transmitting and receiving proposed antennas at various values of 'd' over the sweep. As per the survey, the researchers suggested less than of -15dB path losses. The studies from Fig. 14 and Fig. 15 justified the distinction path losses in proposed work. From this study of path losses over frequencies in sweep, it was computed path losses over different distances'd' at 2.4GHz and shown in Fig. 16.

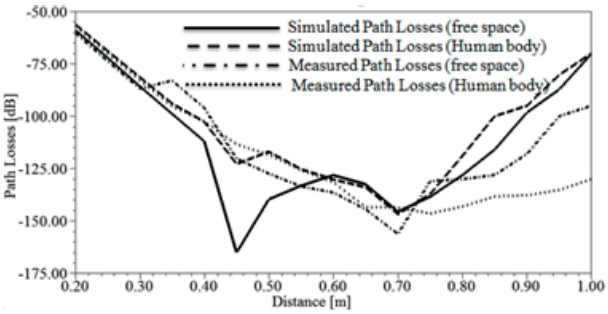


Figure 16: Path loss characteristics over distance between transmitting and receiving antenna at 2.4GHz

From Fig. 16, it was observed the shrinkage of path losses as distance increasing to certain value (700 mm) after that observed heightening the path losses with the increasing of distance with same amount from that certain distance value. From this study of path losses over the distance, it is summarized that the 700 mm distance is suggestible for better electromagnetic interaction between transmitting and receiving antenna on both free space and human body.

5 Conclusions

The proposed work presented path loss modeling between wearable antenna sensors in both free space and human body environments. The proposed model can be applied for channel modeling in the wireless body area networks field. Also, it is proposed a design flow and performance analysis of the wearable antenna in free space and on human body model. The performance of the proposed antenna in terms of return loss, and gain in both environments has been studied. Moreover, a specific absorption rate analysis has been performed to ensure human body safety. According to the obtained simulation results, we have examined the channel attenuation between the transmitting and receiving antenna placed on different positions using S21 parameter.

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Free Software Support for Compact Modelling with Verilog-A

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Abstract: Verilog-A is the analog subset of Verilog-AMS - a hardware description language for analog and mixed-signal systems. Verilog-A is commonly used for the distribution of compact models of semiconductor devices. for such models to be usable a Verilog-A compiler is required. The compiler converts the model equations into a form that can be used by the simulator. Such compilers have been supplied with commercial simulators for many years now. Free software alternatives are much more scarce and limited in the features they offer. The paper gives an overview of Verilog-A, Free software Verilog-A compilers, and Free software/Open source simulators that can simulate compact models defined in Verilog-A. Advantages and disadvantages of individual compilers and simulators are highlighted.

Keywords: analog circuits, compact models, Verilog-A, compiler, simulation

Odprtokodna programska oprema za uporabo kompaktnih modelov v jeziku Verilog-A

Izvleček: Verilog-AMS je opisni jezik za mešana analogno-digitalna vezja. Verilog-A je njegov podsklop, ki je namenjen opisu analognih vezij. Pogosto ga uporabljamo za distribucijo kompaktnih modelov polprevodniških elementov. Da bi take modele lahko uporabili v simulatorju vezij, potrebujemo prevajalnik za Verilog-A. Ta pretvori model v obliko, ki jo simulator lahko uporabi pri izračunu odziva vezja. Prevajalniki za Verilog-A so že dlje časa sestavni del tržnih programskih paketov za simulacijo vezij. Odprtokodnih alternativ je manj in podpirajo samo del specifikacije jezika. Članek poda pregled odprtokodnih prevajalnikov in simulatorjev s podporo za kompaktne medele opisane v jeziku Verilog-A s poudarkom na prednostih in slabostih posameznih prevajalnikov in simulatorjev.

Ključne besede: analogna vezja, kompaktni modeli, Verilog-A, prevajalnik, simulacija

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1 History of Verilog-A

Verilog-A is a hardware description language (HDL) for analog circuits. It is based on Verilog, which by itself is a HDL for digital circuits. The history of Verilog [1] dates back to 1980s when Gateway Design Automation introduced the language. In 1990 the language was acquired by Cadence Design Systems. The language was transferred to public domain where it was supported and extended by Open Verilog International (OVI). In 2000 Accellera Systems Initiative was founded from the merger between OVI and VHDL International and has been managing the language to date.

Verilog has been standardised by IEEE as standards 1364-1995 (Verilog-95) [2], 1364-2001 (Verilog-2001) [3], and 1364-2005 (Verilog-2005) [4]. Since then Verilog has evolved into SystemVerilog which offers new design (data lifetime specification, more advanced data types, new procedural blocks, and interfaces) and verification features (new data types, object-oriented programming model, generation of constrained random values, assertions, coverage, and synchronisation primitives). SystemVerilog has been standardised by IEEE as standards 1800-2005 (superset of Verilog-2005) [5] and 1800-2009 (SystemVerilog 2009) [6] with fur-

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ther updates in 2012 (1800-2012) [7], 2017 (1800-2017) [8], and 2023 (1800-2023) [9].

In parallel to the evolution of Verilog a new HDL for analog/mixed signal systems was being developed. Verilog-A, which is a HDL for purely analog systems, was released in 1996 by OVI [10]. Its syntax was based on the syntax of Verilog, but the language constructs were designed for describing analog systems in terms of ordinary differential equations (ODE). The language was primarily created to standardize the Spectre simulator's behavioral language in times when it was facing competition from VHDL that was getting analog capabilities via incorporating analog HDL languages like MAST [13]. Verilog-A was developed with a more advanced language in mind - one that would be capable of describing analog, as well as, mixed-mode systems. The language was released in 1998 and was deemed Verilog-AMS (version 1.3). In the year 2000 version 2.0 of Verilog-AMS was released. Since then Verilog-AMS has beed updated in 2009 (version 2.3.1), 2014 (version 2.4.0) [11], and 2023 (Verilog-AMS 2023) [12]. Currently work is underway to merge Verilog-AMS with SystemVerilog to produce SystemVerilog-AMS [14]. Verilog-A and Verilog-AMS did not become IEEE standards and have remained under the oversight of Accellera. Modern Verilog-A is the analog subset of Verilog-AMS.

Free software [15] alternatives for Verilog-A are important, among other things, because they make Verilog-A and the compact models defined in Verilog-A available to a wide audience without having to pay the high cost of commercial tools. Free software means that the users have the freedom to run, copy, distribute, study, change and improve the software. It is usually licensed under the GNU General Public License (GPL) or some other compatible license. Free software must not be confused with free software (lowercase). The latter means only that the price of the software is zero and does not give its users the same freedom as Free software. All Free software is Open source [16], but every Open source software is not Free software. Open source licenses can be more restrictive that GPL. Free software has great impact. As an example, consider the importance, usefulness, and implications of the GNU C Compiler [17] or Free software for Verilog-95 simulation (i.e. Verilator, [18]).

2 Using Verilog-A for compact modelling

Verilog-A is commonly used for the distribution of compact models (CM) of semiconductor devices. Compact models provide the equations linking terminal currents to terminal voltages of circuit components like MOSFETs, bipolar transistors, diodes, etc. The usual approach to formulating circuit equations is modified nodal analysis (MNA) [19] where as many as possible branch currents are explicitly expressed and substituted into Kichoff current law equations.

In every circuit one Kirchoff current law equation (KCL) can be constructed for each node, with the exception of the reference node. Each node is associated with a nodal voltage (potential) which becomes an unknown in the system of equations. An exception to this is the reference node whose nodal voltage is assumed to be zero. Branch currents that cannot be explicitly expressed are kept as unknowns in the system of equations. In circuit simulation such branch currents are treated as the associated quantities of so-called flow nodes. For each flow node an equation has to be added to the system. This equation is obtained from the constitutive relation of the element where the aforementioned branch resides and has a similar role as the KCL equation of an ordinary node. Flow nodes are typically used for modelling voltage sources and inductors.

Equations of a model are formulated as ordinary differential equations (ODE). Let us assume a circuit element has n nodes (ordinary and flow nodes) of which the first $m \leq n$ nodes are terminals. All terminals are assumed to be ordinary nodes. The associated quantities of the nodes are considered to be the independent variables and their values are listed in vector **x**. Let **y** denote the vector of terminal currents where a current is assumed to be positive if it flows into the corresponding terminal. Components of **y** that correspond flow nodes or internal nodes are assumed to be 0.

Let **g(x)** and **q(x)** denote two vector valued (nonlinear) functions of independent variables. These two functions represent the resistive and the reactive contributions to the equations associated with the aforementioned *n* nodes. For ordinary nodes the components of **g(x)** and **q(x)** correspond to resistive currents flowing from the nodes and charges accumulated at the nodes, respectively. For flow nodes they correspond to voltages and fluxes. The resistive currents are assumed to be positive if they flow outward from a node. After a Verilog-A compact model is compiled its equations are formulated as

$$\mathbf{y} = \mathbf{g}(\mathbf{x}) + \frac{\mathrm{d}}{\mathrm{d}t}\mathbf{q}(\mathbf{x}) \tag{1}$$

As an example, let us consider a semiconductor diode in Figure 1. The model has two terminals (A and C) and one internal node (Ai). It comprises a linear resistor (R_S) that models the series resistance of a diode and a core

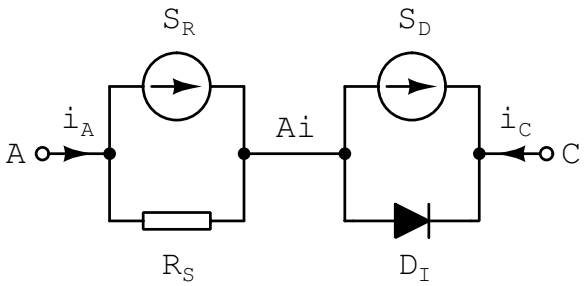

Figure 1: Model of a semiconductor diode. Noise sources S_D and S_R are treated separately by Verilog-A.

diode that models the nonlinear diode characteristic and its charge storage. The noise generated by the diode and its series resistance is modelled by noise sources with power spectral densities S_R and S_D. Vectors **y** and **x** in equation (1) can be written as $\mathbf{y} = \begin{bmatrix} i_A & i_C & 0 \end{bmatrix}^{\mathrm{t}}$ and $\mathbf{x} = \begin{bmatrix} v_A & v_C & v_{Ai} \end{bmatrix}^{\mathrm{T}}$. The two nonlinear vector-valued functions are

$$\mathbf{g}(\mathbf{x}) = \begin{bmatrix} R_S^{-1}\left(v_A - v_{Ai}\right) \\ -i_D\left(v_{Ai} - v_C\right) \\ R_S^{-1}\left(v_{Ai} - v_A\right) + i_D\left(v_{Ai} - v_C\right) \end{bmatrix} \tag{2}$$

$$\mathbf{q}(\mathbf{x}) = \begin{bmatrix} 0 & -q_D\left(v_{Ai} - v_C\right) & q_D\left(v_{Ai} - v_C\right) \end{bmatrix}^T \tag{3}$$

To simplify expressions let us neglect the diode's junction capacitance and assume it exhibits only diffusion capacitance. Then functions i_D and q_D can be written as

$$i_D(u) = I_S\left(\exp\left(\frac{u}{V_T}\right) - 1\right) \tag{4}$$

$$q_D(u) = \tau\frac{I_S}{V_T}\exp\left(\frac{u}{V_T}\right) \tag{5}$$

The power spectral densities of the two noise sources are $S_R = 4kT / R_S$ and $S_D = 2qi_D\left(v_{Ai} - v_C\right) + K_f i_D\left(v_{Ai} - v_C\right)^{A_f} / f$. I_S, τ, K_f, and A_f are diode parameters and V_T is the thermal voltage (kT/q). The Boltzmann constant, the absolute temperature, and the electron charge are denoted by k, T, and q, respectively. The core diode noise source (S_D) comprises a frequency-independent shot noise component and a flicker noise component whose power spectral density is inversely proportional to the frequency. The Verilog-A code defining the diode model is

```
 `include "constants.vams"
 `include "disciplines.vams"
module diode(A,C);
    inout A, C;
    electrical A, C, AI;
    parameter real Is = 1e-14 from [0:inf];
    parameter real Rs = 0.1 from (0:inf];
    parameter real Tau = 1e-6 from [0:inf];
    parameter real Kf = 1e-12 from [0:inf];
    parameter real Af = 1 from (0:inf];
    real VT, id, qd, g;
    analog begin
      VT = `P_K*$temperature/`P_Q;
      id = Is*(exp(V(AI, C)/VT)-1);
      g = Is/VT*exp(V(AI, C)/VT);
      qd = Tau*g;
      I(A, AI) <+ V(A, AI) / Rs;
      I(AI, C) <+ id + ddt(qd);
      I(A, AI) <+ white_noise(4*`P_K*$temperature/
      Rs, "rs");
      I(AI, C) <+ white_noise(2*`P_Q*id, "id");
      I(AI, C) <+ flicker_noise(Kf*pow(id, Af), 1, "flicker");
    end
endmodule
```

Once all models formulate their equations along the lines of (1) the system of equations describing a circuit can easily be assembled. For each circuit element the components of vector **y** corresponding to terminals are simply added to the KCL equations of nodes to which these terminals are connected. Rows of (1) that correspond to internal nodes and complement the circuit's KCL equations as extra equations.

Verilog-A is capable of describing all aspects of a device covered by a legacy SPICE3 model implemented in C. There are several advantages in using Verilog- A. The models are significantly shorter. This arises from two facts. Writing a model in C can require many lines of code for expressing concepts that are expressed with a single line in Verilog-A. Secondly, Verilog-A compilers automatically derive the expressions for the derivatives of functions **g** and **q** with respect to components of **x**. These expressions must be formulated manually in SPICE3 models and can easily double the amount of C code that needs to be written. Manual implementation of derivatives is error prone. Incorrectly implemented derivatives result in convergence problems during simulation which can arise only under certain circumstances and are thus not easily detectable.

Table 1: Length in lines of code (l) and the number of parameters (p) for various MOSFET compact device models.

Compact model	released	language	l	p	l/p
BSIM3 3.2.4	2001	C	14176	439	32
BSIM3 3.3.0	2005	C	13741	441	31
BSIM4 4.5.0	2005	C	23882	789	30
BSIM4 4.8.2	2020	C	27561	926	30
BSIM4 4.8 (Cogenda)	2019	Verilog-A	12591	897	14
BSIM6 6.0.0	2013	Verilog-A	3628	757	4.8
BSIM-BULK 107.1.0	2022	Verilog-A	4992	1073	4.7

Table 1 lists selected BSIM3, BSIM4 and BSIM-BULK (BSIM6) models [20]. The number of parameters of a model (p) is closely correlated with the size of the model expressed as lines of code (l). It is evident that SPICE3 models implemented in C are significantly more verbose than models implemented in Verilog-A. Models that are implemented in Verilog-A since their inception (BSIM6, BSIM-BULK) comprise roughly 6 times fewer lines of code per parameter than SPICE3 models implemented in C (BSIM3, BSIM4). Even models translated from a SPICE3 model (e.g. Cogenda BSIM4 4.8 [21]) comprise less than half the amount of code per parameter compared to SPICE3 models.

Modern device models, like BSIM-BULK, BSIM-SOI, HICUM, MEXTRAM, etc., are all released by their developers (mostly universities) in Verilog-A. Compact Model Coalition (CMC) [22] performs quality checks and verifies if the released models comply with standards.

3 Interfacing with a simulator

Simulators typically require from a model to compute the contributions to KCL equations (given by vector-valued functions **g** and **q**) for a given vector of independent variables (**x**). The system of first order differential equations is assembled as discussed in section 2 and can be expressed as

$$\mathbf{g}^*\left(\mathbf{x}^*\right)+\frac{\mathrm{d}}{\mathrm{d}t}\mathbf{q}^*\left(\mathbf{x}^*\right)=0 \tag{6}$$

where vector **x*** is obtained by meaningfully merging vectors of independent variables corresponding to individual circuit elements (**x**) because an independent circuit variable can appear in multiple circuit elements. Functions **g*** and **q*** are obtained by adding up contributions from circuit components (**g** and **q**) depending on the way their terminals are connected to the circuit's nodes. Each node corresponds to one KCL equation. Contributions of grounded terminals are ignored. The last *n* - *m* components of each element's **g** and **q** correspond to extra equations. These equations complement the set of KCL equations to form the circuit's system of equations.

Numerical algorithms employed by simulators depend on the derivatives of **g*** and **q*** with respect to the independent variables **x***. These derivatives are gathered in the Jacobian matrices **G*** and **C*** whose components are given by

$$G_{ij}^*=\frac{\partial g_i^*}{\partial x_j^*} \tag{7}$$

$$C_{ij}^*=\frac{\partial q_i^*}{\partial x_j^*} \tag{8}$$

Because **g*** and **q*** were constructed by adding contributions from vector valued functions **g** and **q** matrices **G*** and **C*** can be constructed by adding contributions from Jacobian matrices **G** and **C** computed for functions **g** and **q**, respectively. To summarize, an analog device model must compute the Jacobian matrices **G** and **C** alongside **g** and **q** for a given vector of independent variables **x**.

In time-domain analysis equation (6) must be numerically integrated to obtain a system of nonlinear algebraic equations. When backward Euler integration is used equation (6) becomes

$$\mathbf{g}^*\left(\mathbf{x}^*\left(t_{k+1}\right)\right)+\frac{\mathbf{q}^*\left(\mathbf{x}^*\left(t_{k+1}\right)\right)-\mathbf{q}^*\left(\mathbf{x}^*\left(t_k\right)\right)}{t_{k+1}-t_k}=\mathbf{0} \tag{9}$$

where t_{k+1} is the timepoint for which we are solving the circuit and t_k is the previous timepoint where the circuit's solution is already known. In older simulators (e.g. SPICE3, Gnucap, and QUCS) numerical integration is performed by the device model itself. Consequently models in transient analysis do not compute a separate **q**(**x**). Instead they replace **g**(**x**) and its Jacobian with

$$\mathbf{f}\left(\mathbf{x}\right)=\mathbf{g}\left(\mathbf{x}\right)+\frac{\mathbf{q}\left(\mathbf{x}\right)-\mathbf{q}\left(\mathbf{x}\left(t_k\right)\right)}{t_{k+1}-t_k} \text{ and} \tag{10}$$

$$\mathbf{F}\left(\mathbf{x}\right)=\mathbf{G}\left(\mathbf{x}\right)+\left(t_{k+1}-t_k\right)^{-1}\mathbf{C}\left(\mathbf{x}\right) \tag{11}$$

In this way the code that computes the DC solution can be used without any modification for computing the time-domain solution from

$$\mathbf{f}^*\left(\mathbf{x}\right)=0. \tag{12}$$

Here $\mathbf{f}^*(\mathbf{x})$ is assembled from contributions of individual elements (i.e. $\mathbf{f}(\mathbf{x})$) in the same way as previously $\mathbf{g}^*(\mathbf{x})$ and $\mathbf{q}^*(\mathbf{x})$ have been assembled from $\mathbf{g}(\mathbf{x})$ and $\mathbf{q}(\mathbf{x})$.

This approach violates the separation between the simulator and the models and unnecessarily increases the size of the device model. On the other hand, it also has some advantages besides code reuse between DC and time-domain analysis, like the capability to implement non quasi-static effects in transistor models without adding extra nodes to the circuit (for how this is done in case of a bipolar transistor, see [23]). Serious flaws can also arise from this approach, e.g. the charge conservation problem in early MOSFET models [24, 25]. Charge nonconservation is a serious bug that was facilitated by the capability of handling numerical integration within models themselves. The problem originated from the attempt to formulate model's dynamics with ordinary reciprocal capacitors between nodes instead of charges stored at nodes. Charge non-conservation is impossible to "implement by accident" if charge based modelling is enforced like in Verilog-A.

Modern simulators separate numerical integration from device model evaluation. Using the formulation given by (6) as the basis of a circuit simulator adding new types of analysis becomes a much simpler task. This has been demonstrated in the past by commercial and free simulators, like Spectre [26] and fREEDA [27].

4 Free software compilers for compact models in Verilog-A

This sections gives an overview of Free software Verilog-A compilers where the term Verilog-A compiler is meant in a very broad sense. Two of these compilers (ADMS and OpenVAF) only support a subset of Verilog-A for compact modelling. The third one (Modelgen-Verilog) aims to be a full Verilog-AMS compiler once completed. Since this paper's focus is on compact modelling all three compilers are viable candidates for compiling compact models once their limitations are taken into account.

4.1 ADMS

ADMS (Automatic Device Model Synthesizer) [28] is the oldest of Free software Verilog-A compilers. It was developed by Motorola. At the time of its development MOSFET models were becoming excessively large. Back then the state of the art model (BSIM4) had almost 1000 parameters. The only way to use an advanced MOSFET model was either to use its official Open source implementation for the SPICE3 simulator and accept all the quirks and shortcomings of SPICE3 or implement the model from scratch for the simulator of choice.

Most commercial simulators at the time offered an API (e.g. [26, 29]) via which an external model could be implemented in C. Implementing a model with several hundred parameters involves writing tens of thuosands of lines of C code. Derivatives of currents and charges must be manually implemented. This process is error prone and slow. Furthermore, due to different APIs a large part of the model has to be rewritten for each simulator.

Verilog-A solves these problems since the model has to be implemented only once and the implementation can then be used by all simulators supporting Verilog-A. ADMS was developed as a tool that compiles Verilog-A into a model utilizing the C API of a selected simulator. After defining a new ADMS backend tailored to a specific simulator one can compile arbitrary Verilog-A models (within the limitations of ADMS) for that simulator. The process of compilation with ADMS is fairly slow. For a modern CMC model it can take more than a minute (e.g. for PSPv103 [42]). The generated code must be compiled (usually with a C/C++ compiler) and linked either statically with the simulator (e.g. Xyce [36]) or into a dynamic library that can be loaded by the simulator on-demand (e.g. Spectre [26], Ngspice [33], Gnucap [34]).

ADMS itself is implemented in C utilizing the Glib library [31]. The compiler operates by parsing the Verilog-A code and representing it in the Extensible Markup Language (XML) [30]. The specifications for the code generator (backend) are defined in XSLT, a subset of XSL [32], which is a language for representing XML document transformations. Models generated by ADMS are approximately 20% slower that hand-coded models [28].

Over the years ADMS has been used as the only available Verilog-A solution for compact modelling in Open source simulators like Ngspice [33], Gnucap [34], Quc-

sator [35], and Xyce [36]. Of all the listed simulators Xyce is the most advanced one with the best ADMS support. Nevertheless its ADMS integration has many limitations [37]. CMC models can be handled by ADMS after applying some manual modifications to the model (e.g. [38]).

ADMS is no longer being developed by its author. Development has been taken over by the Qucs project [39]. Contributions to the Git repository since 2017 are scarce and have ceased in 2022.

4.2 OpenVAF

OpenVAF [40] is a fairly recent development. It evolved from VerilogAE [41] whose primary purpose was to ease the process of model parameter extraction by retrieving the model equations from Verilog-A code. OpenVAF translates Verilog-A into a dynamic library with the help of the LLVM library [47]. LLVM emits highly optimized machine code and is generally used for implementing compilers. The resulting dynamic library interfaces with the simulator via the Open Source Device Interface API (OSDI API) [46].

Internally OpenVAF translates Verilog-A code into an abstract syntax tree (AST). Then it performs several transformations in the steps that follow. The first step resolves undefined references to other parts of the code to produce high-level intermediate representation (HIR). HIR is further processed by constructing a control flow graph, thus defining the execution order of the statements. Symbolic derivatives of expressions with Verilog-A operators ddx and ddt are computed to be later used during the construction of the Jacobians and module's output variables. The result of HIR processing is the medium level intermediate representation (MIR). From MIR the LLVM intermediate representation (IR) is generated. IR is a high-level abstraction of the machine code. LLVM performs several low-level optimizations on IR before emitting machine code for the target platform.

The resulting code is very efficient and faster than the code generated by an ordinary C/C++ compiler from ADMS output. OpenVAF supports a significant part of the Verilog-A specification and can compile all of the CMC models without any manual modifications. There are some limitations, though. The compiler does not

Table 2: Simulation runtimes for various models (taken from [42]). Builtin devices defined in C/C++ are denoted by a dash in the compiler column.

Simulator	Free	Compiler/built-in	t [s]	Comment
HICUM/L2v2p4p0 characteristic				
Ngspice	yes	OpenVAF	9.16	
Ngspice	yes	-	14.64	slow implementation
Xyce	yes	ADMS	36.42	strict convergence checks
Xyce	yes	-	26.56	strict convergence checks
ADS	no	proprietary	8.63	
ADS	no	-	7.01	
Spectre	no	proprietary	52.61	
Spectre	no	-	25.33	
BSIMSOI 4.4.0 characteristic				
Ngspice	yes	OpenVAF	8.47	
Ngspice	yes	-	7.98	manually optimized model
BSIMBULK 106.2 characteristic				
Ngspice	yes	OpenVAF	2.08	
Ngspice	yes	ADMS	3.38	
BSIMBULK 106.2 transient				
Ngspice	yes	OpenVAF	9.47	
Ngspice	yes	ADMS	13.70	
PSP 103.8 inverter				
Ngspice	yes	OpenVAF	20.01	
Ngspice	yes	ADMS	25.07	
PSP 103.8 with ISCAS C7552				
Ngspice	yes	OpenVAF	1200	
Ngspice	yes	ADMS	1500	

support analog events, genvars, hidden states, Laplace filters, paramsets, and hierarchical modules. But since these features are rarely used in compact models the lack of them does not represent a significant shortcoming at this point in time.

OpenVAF has replaced ADMS in Ngspice. It is also used by a free but closed-source simulator Spice Opus [48]. Finally, it is the core part of a novel Free software simulator VACASK [43, 44] for which the devices supported by the simulator are almost exclusively defined in Verilog-A.

Table 2 outlines the performance of OpenVAF-generated models with respect to builtin models (manually coded in C/C++), models generated by ADMS, and models generated by commercial compilers. These results are sparse and not sufficient to reliably determine the compiler that produces the fastest models, but nevertheless, they are a good indicator what one can expect from ADMS and OpenVAF.

Several Verilog-A compilers were tested by using the compiled HICUM model to compute the transistor's characteristics. OpenVAF comes out close to the top, second only to the compiler in ADS [49]. Xyce with ADMS comes out as one of the slowest solutions. This can be largely attributed to more strict convergence checks in Xyce when compared to Ngspice. Ngspice performance on this test problem can be attributed to sub-optimally coded derivatives in the built-in HICUM model.

When compared to a mature and highly optimized manually written builtin model in Ngspice (BSIMSOI 4.4.0) the OpenVAF-compiled model exhibits only 6% slower performance. On the two BSIMBULK test problems (characteristic and transient) the ADMS-compiled model is 45% to 60% slower than the one compiled with OpenVAF. This difference is significantly greater than the difference between models compiled by ADMS and manually coded models (models generated by ADMS are on average 20% slower). On the PSP inverter test problem the ADMS-compiled model is 20% slower than the one compiled with OpenVAF. The large test problem (ISCAS C7552) once again confirms the speed difference between models generated by ADMS and OpenVAF. These two benchmark results, the result obtained with the BSIMSOI model, and the fact that ADMS models are on average 20% slower than hand-coded models indicate that OpenVAF-generated models are roughly as fast as manually coded compact models.

4.3 Modelgen-Verilog

Modelgen-Verilog (MGV) [45] is a Verilog-AMS compiler for the Gnucap [34] circuit simulator. It has been in development since 2023. The ultimate goal of the project is to implement full support for Verilog-AMS in Gnucap. Presently the compiler outputs C++ code that is tightly coupled with the Gnucap simulator. After compiling and linking the code a dynamic library is obtained that can be loaded by Gnucap. The dependence on Gnucap could be removed in the future as backends for other simulators get added.

At the present (June 2024) the compiler seems to be capable of processing some CMC models [50], albeit quite inefficiently since a compiled PSP103 model uses 30 internal nodes, while its Verilog-A source code defines only 17 internal nodes. Consequently, simulations with the generated devices are reportedly slow [50]. A comparison akin to that in Table 2 has not been published yet.

A significant improvement in speed is expected from paramset support. Paramsets substitute most of the model parameters with concrete numbers upon which the expressions are simplified (constant folding) thus significantly reducing the computational burden of model evaluation. Further speedup could be obtained if the analog part of the compiler would implement optimizations akin to those in OpenVAF.

Modelgen-Verilog is a project whose ambitions are much bigger than the topic of this paper. Currently the compiler supports paramsets, analog events, hierarchical models, Verilog-A disciplines, discontinuities, and frequency domain filters. These features are missing in the remaining two Verilog-A compilers. Due to its early stage of development not many optimizations have been applied yet and there is a lot of room for improvement.

5 Free software/Open source simulators supporting compact models in Verilog-A

Table 3 gives a concise overview of the Free software/Open source analog circuit simulators that support compact models defined in Verilog-A. Note that the term Free software cannot be applied to Ngspice because of its license. Despite this Ngspice is still Open source and parts of it are Free software.

Core size of a simulator is the size of the simulator's source code excluding code that defines the device models. Simulators usually offer some kind of parameter sweep which is significantly more efficient than repeatedly running the simulator with a modified input file. Although a sparse linear solver is almost a must for a circuit simulator, not all simulators use one (e.g. Qucsator).

Table 3: Comparison of Free software simulators. Asterisk denotes a feature under development as of September 2024.

	Xyce	Ngspice	VACASK	Gnucap	Qucsator
Language	C++	C	C++	C++	C++
Core size (lines of code)	185500	63800	36700	28600	50300
Verilog-A CM support	ADMS	OpenVAF	OpenVAF	MGV or ADMS	ADMS
Operating point (OP)	yes	yes	yes	yes	yes
Small-signal AC	yes	yes	yes	yes	yes
Transient	yes	yes	yes	yes	yes
Small-signal noise	yes	yes	yes	no	yes
Harmonic balance	yes	no	no*	no	yes
Analyses supported by sweep	all	OP	all	OP	all
Sweep depth	arbitrary	2	arbitrary	arbitrary	1
Analysis/device separation	yes	no	yes	no	no
Sparse solver	yes	yes	yes	yes	no
Parallel evaluation	yes	yes	no	no	no
Parallel solver	yes	no	no	no	no
SPICE devices	yes	yes	no*	yes	partly

The process of simulation can be divided into two steps that in general must be repeated multiple times in order to complete a circuit analysis: evaluation of the circuit's components and solving a system of linear equations. Both steps can take advantage of parallel processing which can speed up the simulation and facilitate the simulation of circuits that are too big to fit on a single computer. Not many simulators exploit parallelism (only Xyce and partly Ngspice).

Finally, for a simulator it is important to provides basic SPICE device models (e.g. Gummel-Poon BJT, MOSFET levels 1-3, and 6, JFET, and MESFET). Mature simulators provide these device models (Xyce, Ngspice, Gnucap) while newer ones do not (VACASK, Qucs).

In the remainder of this section a more detailed description will be given for each one of the mentioned simulators.

5.1 Xyce

Xyce [36] is the most advanced of all the simulators listed in Table 3. Like all modern simulators, Xyce's core separates the device models from analysis implementation which makes it possible to implement a new analysis without having to change the device models. The simulator is capable of accelerating computations via parallel computing. Numerical capabilities are provided by the Trilinos [51] suite of libraries that offer unified wrappers around various state of the art solvers (like KLU). Element evaluation, as well as, certain linear solvers can take advantage of parallel processing. The latter is efficient only for very large circuits. Xyce offers all the standard SPICE circuit analyses, as well as, harmonic balance analysis.

Support for compact models in Verilog-A is provided by ADMS. The development team announced in 2022 [52] that they intend to build their own Verilog-A compiler based on an in-house Python library for (symbolic) differentiation. Since then there has been little news regarding this subject. Currently ADMS in Xyce has many limitations [37], largely due to the nature of ADMS.

5.2 Ngspice

Ngspice [33] is the most commonly used Open source simulator. It is based on the original SPICE3f5 source code in C. The original source code has been significantly extended and many bugs and shortcomings were fixed. One of these shortcomings was the original linear solver library of SPICE3 [55], which by now is no longer competitive. It has been replaced with the much faster KLU library [56].

Unfortunately, as is customary with all SPICE-based simulators, the models are tightly coupled with the circuit analyses. This makes it hard to add new types of analysis without making extensive changes to the large library of device models. Ngspice partly supports parallel evaluation of elements, either on multiple local CPU cores via OpenMP [53], or (for some elements) on a GPU via CUDA [54]. The linear solver, however, is not parallel.

Support for Verilog-A compact models was implemented at first with ADMS. Recently, the OSDI API has been

implemented which in turn makes it possible to use OpenVAF-generated models.

5.3 Gnucap

Gnucap [34] has a long history dating back to 1982. Since then it has been in slow, but steady development. The set of circuit analyses is fairly limited (only operating point/DC sweep, AC, and transient analyses are supported). The separation between the device models and the analyses is not complete as the models still have separate matrix loading functions for the time domain and for the frequency domain. This is alleviated by the fact that Gnucap's models are mostly generated with Modelgen, Gnucap's own model generator, not to be confused with Modelgen-Verilog. Models generated by both model generators are accessed by the simulator through the same API. Another shortcoming of Gnucap is its linear solver which is outdated. On the bright side, the solver offers functionality not available in other Free software circuit simulators because it can do partial solves of matrices when only a part of the matrix changes.
Support for Verilog-A compact models is provided by ADMS. Recently, development of a novel Verilog-AMS capable compiler for Gnucap has started (Modelgen-Verilog [45]). The compiler already supports a large subset of Verilog-AMS.

5.4 Qucsator

Qucsator [35] is a fairly new simulator whose beginnings date back into early 2000s when it started as the Quite universal circuit simulator (Qucs) project's own simulator. The simulator offers operating point/DC, AC, S-parameter, transient, and harmonic balance analysis. The models are tightly coupled with the analyses so implementing a new kind of analysis generally means all device models need to be modified, too. A major shortcoming is the fact that the simulator does not use a sparse linear solver. Instead an ad-hoc dense matrix solver is used, which makes the simulator impractical for anything but the smallest of circuits. Support for Verilog-A compact models is provided by ADMS.

5.5 VACASK

VACASK [43, 44] is a recently published simulator. It separates the models from the analyses thus simplifying the implementation of analyses by avoiding changes in device models. VACASK uses a state of the art linear solver (KLU).

The simulator offers operating point/DC, AC, small-signal transfer function (DC and AC), transient, and noise analysis. Harmonic balance analysis is currently under development, as well as, support for SPICE builtin device models. VACASK supports the OSDI API so that Verilog-A compact models compiled with the OpenVAF compiler can be used. In fact, most of the simulator's device library is implemented in Verilog-A. An exception to this are independent sources, linear controlled sources, and inductive couplings. These elements cannot easily be implemented in the Verilog-A subset supported by OpenVAF if one wants them to provide the same kind of interface as SPICE3 models do.

VACASK is in early stages of development. Preliminary benchmarks indicate that in single CPU mode it runs faster than Xyce, Gnucap, and Ngspice [43].

6 Conclusion

Verilog-A is the analog subset of Verilog-AMS. Over the years Verilog-A has become the de-facto standard for distributing compact models of semiconductor devices. Models implemented in Verilog-A need not specify any derivatives which makes the models significantly shorter and the coding process less errorprone. Verilog-A focuses on the equations describing the behavior of a circuit element. This reduces the size of a compact model by a factor up to 6 compared to SPICE3 compatible C code. Verilog-A compilers can significantly speed up the execution of a model by applying optimizations before the final machine code is emitted. The resulting model can be as fast as the hand-coded version of the model.

Verilog-A compilers are supplied with most commercial simulators. The available alternatives in the realm of Free software are much more scarce. Simulator developers can choose between three alternatives. ADMS is an old solution that requires manual intervention in the model code. OpenVAF is a modern compiler that produces fast models. Both alternatives support only a subset of Verilog-A. OpenVAF is more suitable because it is capable of compiling all public CMC models without modifications. The third alternative (Modelgen-Verilog) is a Verilog-AMS compiler that already supports a large part of the standard despite being in the early stages of development. It is capable of compiling Verilog-A compact models, but the resulting code is somewhat inefficient. Unfortunately its interface currently supports only the Gnucap simulator.

Several Open source and Free software simulators support Verilog-A, ranging from the most advanced one (Xyce), through SPICE3-based Ngspice, and newer simulators like Qucsator, Gnucap, and VACASK. All of these simulators support compact models defined in Verilog-A via one of the three mentioned alternatives.

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