

# DESIGN CONSIDERATION FOR POWER MODULES OF ELECTRO-MOTOR DRIVES

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**Key words:** electro-motor drive, power modules, PWM current switch, optimized AC drive

**Abstract:** The major component of electro-motor drive is the power module producing a PWM signal to drive the motor from the Battery DC source. The power consumption or the efficiency of the electric drive is dominantly the function of the high side and low side semiconductor switch which performs the PWM current to the AC motorcoil. The design of such switch is therefore crucial for the drive performance.

In the paper the design considerations are discussed for the optimization of electrical mechanical and thermal performances of the three phase motor drive power module.

The measurement results on the optimized module are presented together with the price/performance analysis of the power module.

## Načrtovalski vidiki za močnostne krmilnike elektromotorjev

**Ključne besede:** trifazni krmilnik, tokovna stikala, PWM krmiljenje, optimizacija krmilnika

**Izvleček:** Glavni del krmilnika elektromotorja je močnostni modul, ki generira PWM pulzno-širinsko moduliran signal, ki napaja motor iz baterije. Poraba moči oziroma učinkovitost močnostnega krmilnika je v večini funkcija zgornjih in spodnjih polprevodniških stikal, ki priklapljajo PWM tok na navitje motorja. Pravilno načrtovanje takega stikala je zato bistvena za delovanje krmilnika. V članku so predstavljene možnosti optimizacije električnih, mehanskih in termičnih veličin in njihov učinek na delovanje trifaznih krmilnikov za elektromotorje. Predstavljeni so rezultati meritev z optimiziranim krmilnikom. Prav tako je predstavljena cenovna analiza za izboljšave glede na osnovni sistem.

### 1. Introduction

The PWM signal is used to provide power AC supply to the three phase coil of the AC motor /1/ as shown in fig.1.

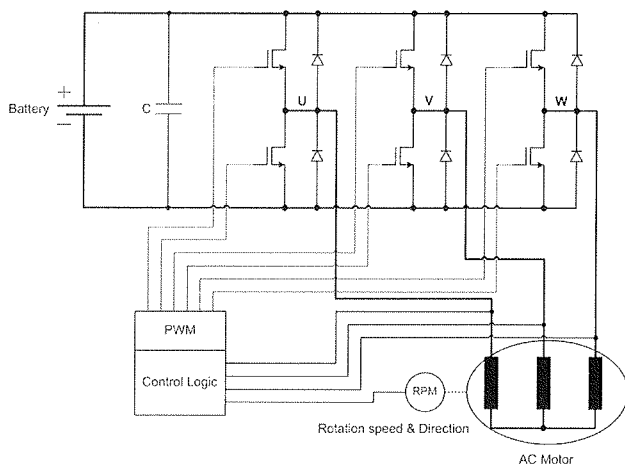


Fig. 1: AC motor system

### 2. System partitioning

For low power motors the optimal solution is to combine both the low power PWM control signals generation with the power switches in a single ASIC.

This could work as long as the motor power is low enough to be able to design the three low side and the three high side switches on the same ASIC. In this case we need to consider the ASIC power dissipation to be able to make a decision if this approach can be a cost effective solution. To analyze the cost-performance of a single ASIC the simplified models can be used considering the maximal allowed power dissipation of the ASIC, the cost of the mixed signal silicon area, the cost of a single device silicon area, the power dissipation of the bonding wires, the packaging cost and the assembly cost.

The power dissipation of the ASIC is a combination of the power dissipation due to the losses on the semiconductor switch when conducting and the power dissipation due to the so-called switching losses which are caused during the switch conductance transition, and the losses due to charging and discharging the battery buffer capacitor during switching.

The switching losses can be as high as one third of the total power dissipation so a conservative figure for the maximal power dissipation expressed with maximal allowed motor current is approximately

$$r_{on} I_{max}^2 = 2P_{dm} / 3 \quad 2.1$$

where the  $r_{on}$  is the resistance of the switch in ON state including resistance of connections (bonding and bus bars),

$I_{max}$  is the maximal motor current and  $P_{dm}$  is a maximal allowed power dissipation of the drive.

The silicon area is in linear proportion to the  $r_{on}$  but is different for mixed signal silicon (Am) and single device silicon (Ad).

A simple rule of thumb gives us the following approximate relations.

One square mm is required for a 50V drain-source break down voltage to achieve 100mOhms on resistance. On the other hand the same performance can be achieved with only 0,7 mm<sup>2</sup> using single device silicon Ad.

Taking into account that the cost of Am silicon area is about 1.5 times the cost of Ad silicon area, this simply means that the cost efficiency of the single silicon area is more than two times higher.

Unfortunately the simple linear model for the silicon area cost is not applicable for larger silicon area due to final defect density of the silicon processing which further reduces the benefits of larger integration. It has been estimated that using some simplification the break point between a single ASIC approach which combines the low power drivers and the power switches is close to the area of about 30 mm<sup>2</sup>.

In this case the required area for low power control electronic is about 9mm<sup>2</sup>, so the remaining 21mm<sup>2</sup> is used for six switches with  $\gamma_{on}$  of about 30mOhms.

### 3. Analysis of maximal power capability of single ASIC motor drive

Using equation 2.1. the maximal current can be calculated:

$$I_{max}^2 = 2P_{dm} / 3 \cdot 0.03 \quad 3.1$$

$P_{dm}$  can be calculated from the best possible thermal resistance from the packaged ASIC to the ambient.

Fig. 2 shows the thermal profile of the ASIC packaged in a power package with thermal resistance of 0.5 degree C/Watt mounted to the heat sink with 230mm x 200mm x 40mm.

The maximal possible power  $P_{dm}$  can be calculated from the temperature difference between maximal ambient temperature and maximal junction temperature, taking into the account the total thermal resistance of the set-up. In our case the maximal ambient temperature is 120 degrees C and the maximal junction on temperature 150 degrees C. The worst case thermal resistance is 1 degree C/Watt, which gives us the next power  $P_{dm}$  is 30W.

30W maximal power dissipation of the ASIC for three phase AC motor can provide the maximal motor phase current

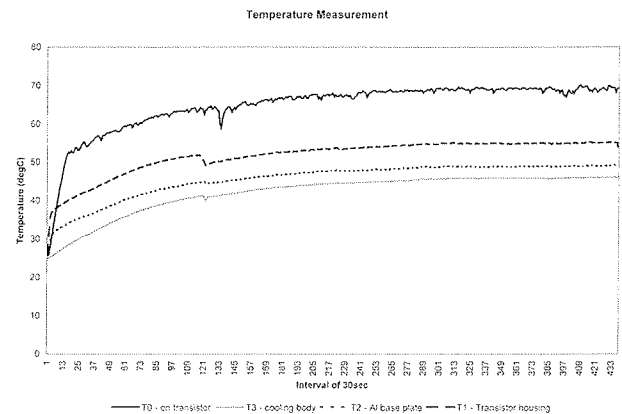


Fig. 2: Thermal profile of the dedicated ASIC model

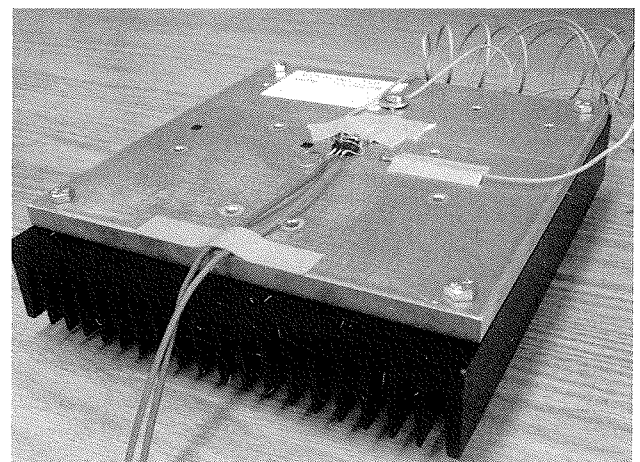


Fig. 3: Single ASIC model set-up

according to equation 2.1, where the total power dissipation is the sum of the power dissipation of six switches, i.e. two per phase. This leaves us with 30W/6 per switch, so only 5W can be entered into equation 2.1.

The result is:

$$I_{max} = \sqrt{2 \cdot P_{dm} / 3 \cdot 0,03} \cong 10A$$

This is therefore the limit for single ASIC power drive. Depending on the maximal battery voltage and transistor break-down voltage the typical maximal electro-motor power would range from 300W to max 1kW.

### 4. Design consideration for power motor using external power switches

From the above analysis it is clear that the most critical figure which needs to be improved is the maximal power dissipation. Here we have two measures which could be improved.

The first one is the reduction of  $r_{on}$  resistance which can be lowered based on large silicon area using low cost sin-

gle device silicon, and which can be further minimized by the use of parallel devices. However it is required that the device is connected using low resistance connections. An example of such low resistance is shown in figure 4, where the transistor drain is soldered to 3mm thick copper bus-bar and the source is bonded with thick multiple Al wires. This arrangement using 5 transistors with the area of 30 mm<sup>2</sup> provides  $r_{on}$  resistance of 500μOhms.

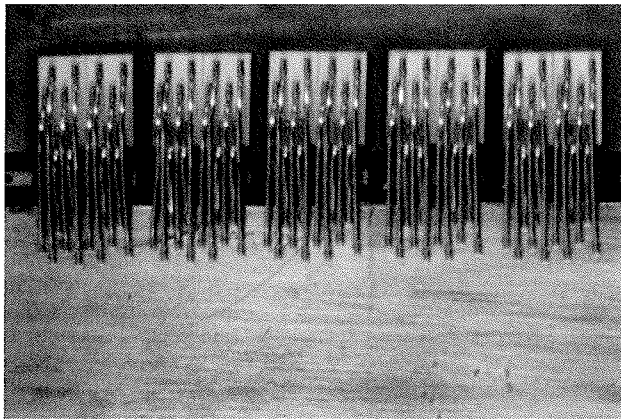


Fig. 4: Transistor connections

The second improvement is to reduce the thermal resistance of the transistor junction to the ambient. Direct soldering to the copper bus-bar reduces this thermal resistance to less than 0,05 degrees C/Watt, so the only remaining critical thermal path is the heat-sink to ambient air for passive. The photograph of the power drive three + 1 phase switch is shown in figure 5.

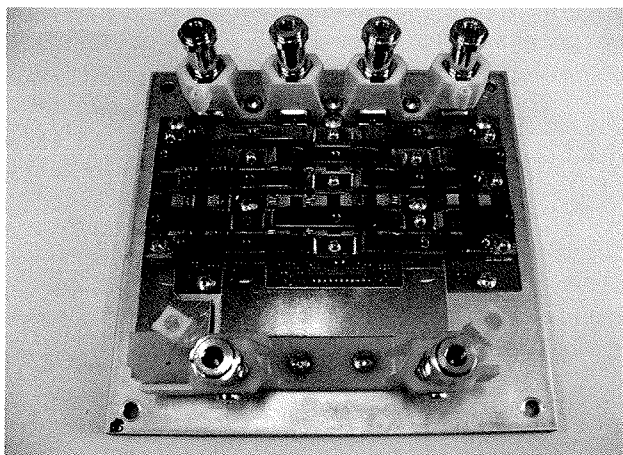


Fig. 5: The photograph of the power drive

For this arrangement a thermal resistance for transistor junction to the ambient has been reduced to 0,15 degree C/Watt. Taking into the account the  $r_{on}$  resistance improvement from 30mOhms to 400μOhms, i.e. 75 times and the thermal resistance improved which is approximately 7 times the total maximal current increase is  $\sqrt{75 \cdot 7} = 17$  times, which leads us to maximal current of about 220A.

The power drive which has been designed based on described principles is shown in figure 6.

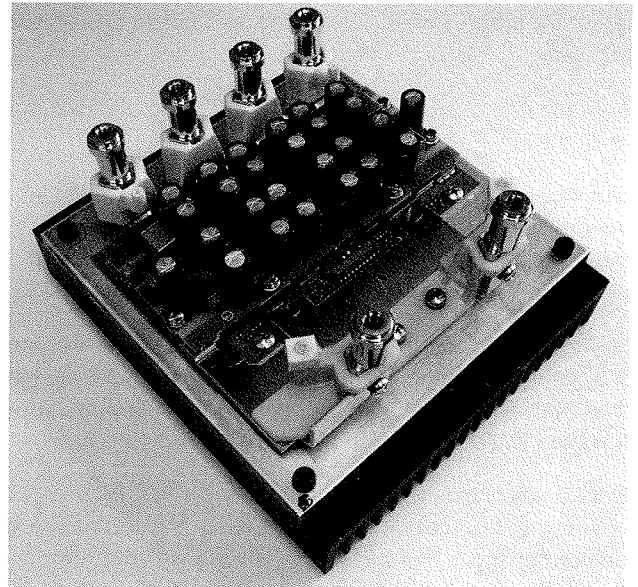


Fig. 6: Power drive

The measurement results using the peak required current for 60 minutes are shown in figure 7.

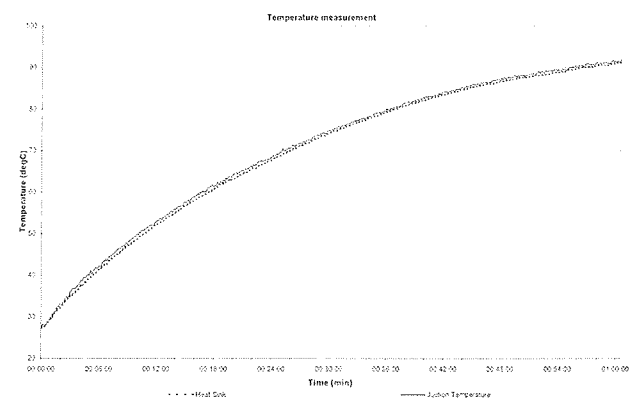


Fig. 7: Measurement results of power drive: The upper curve shows temperature behaviour of transistor junction; the lower curve shows temperature behaviour of the heat sink

## 5. Conclusions

The analysis of single ASIC power drive with integrated power switch has been presented. The results of this analysis have been implemented on the design of power drive with external power switches. The proposed design guide lines have improved the cost-effectiveness by the factor of around 1,6 times compared to leading manufacturers of such devices /2/. The designed power drive has been measured to show superior performance compared to the existing power drives in the market /3/.

## 6. Acknowledges

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