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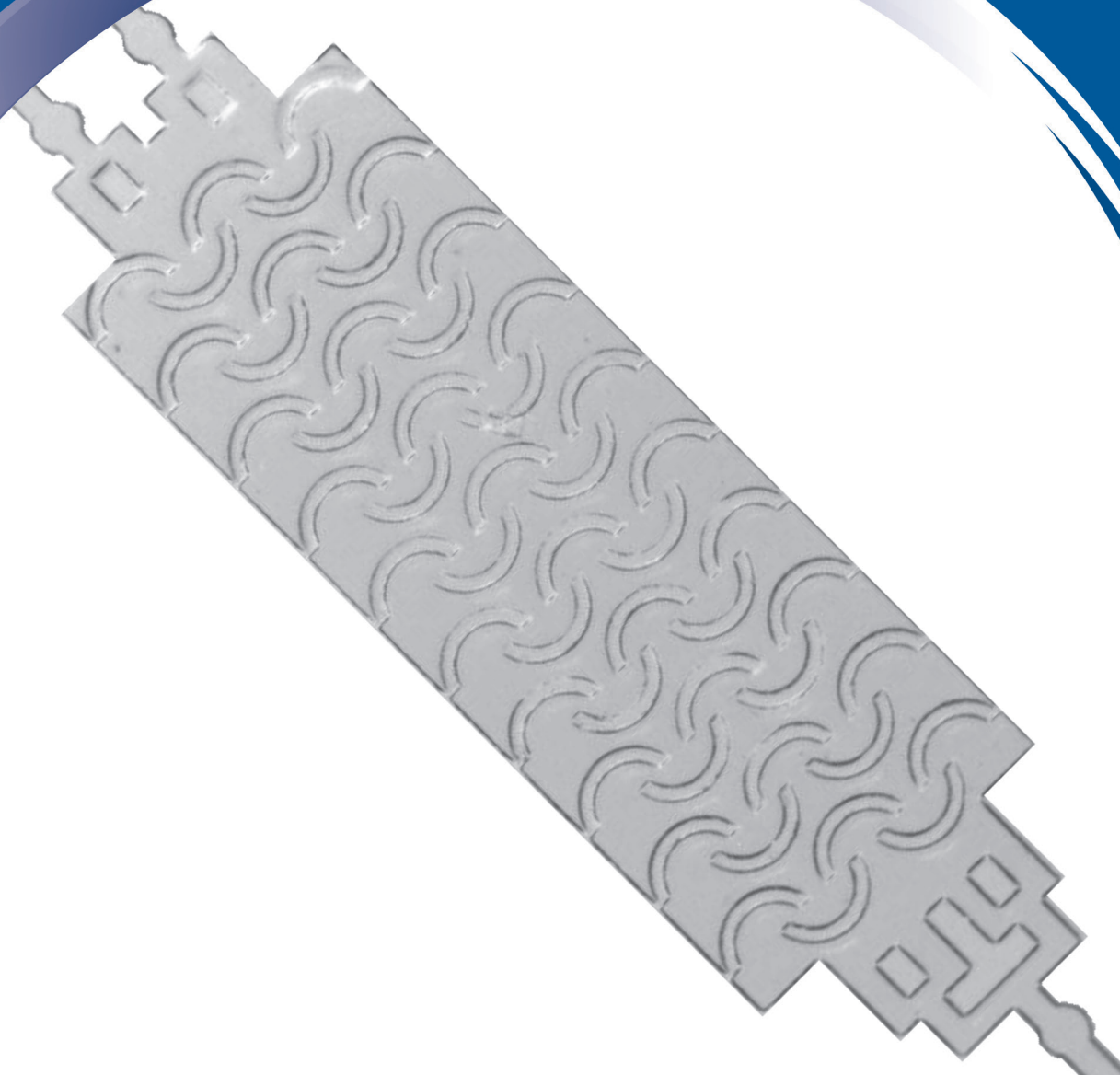

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Low-power OTA-C Based Tuneable Fractional Order Filters

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Abstract: In this study, a low-voltage low-power, simple operational transconductance amplifier (OTA) based fractional order low-pass and high-pass filters of order (n+α) are designed and simulated with CADENCE-PSPICE where 0<α<1 and n≥1. The employed transconductance amplifier operates at ±0.75 V. To simulate designed filters, 0.35 µm TSMC CMOS technology parameters are used. The simulation results verify theoretical statements. The power dissipations of simulated low-pass filters of orders 1.3, 1.5, 2.3 and 2.5 are 14.6 nW, 13 nW, 17 nW and 15.3 nW, respectively. For the same filter orders, the corresponding dissipation values of high-pass filters are respectively 45.2 nW, 42.7 nW, 47.5 nW and 45 nW. In addition to the low-power low-voltage operation, another significant advantage of the proposed circuit topologies is that the OTA based low-pass and high-pass topologies provide electronic tuning capability of the orders and frequency responses of the filters without any structural change on these topologies. Therefore, same circuit topology can be used for the different orders of the same filter by just changing the biasing currents of the used OTAs. Additionally, OTA-C based filters offer usage of the grounded capacitors as well as resistorless realization.

Keywords: Fractional filter; fractional circuit; low power

Nastavljiv filter frakcijskega reda nizkih moči na osnovi OTA-C

Izvleček: Članek predstavlja nizko in visoko pasovne filtre nizkih napetost in majhne moči na osnovi transkonduktančnega operacijskega ojačevalnika (OTC). Filtri reda (n+α) so načrtani in simulirani v CADNECE_PSPICE okolju, pri čemer je 0<α<1 in n≥1. Transkonduktančni ojačevalnik deluje pri napetosti ±0.75 V. Filtri so simulirani v 0.35 µm TSMC CMOS tehnologiji. Poraba moči simuliranih nizkopasovnih filtrov reda 1.3, 1.5, 2.3 in 2.5 so 14.6 nW, 13 nW, 17 nW in 15.3 nW. Visokopasovni filtri enakih redov porabijo 45.2 nW, 42.7 nW, 47.5 nW in 45 nW moči. Nizko napetostno delovanje pri nizki porabi moči omogoča možnost elektronske nastavitve reda filtra brez spreminjanja topologije. Ista topologija tako omogoča izvedbo filtra različnega reda le s spreminjanjem mirovnega toka OTA. Filti na osnovi OTA-C omogočajo ozemljitev kondenzatorjev in izvedb o brez uporabe uporov.

Ključne besede: frakcijski filter; frakcijsko vezje; nizka moč

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1 Introduction

Fractional calculus is a branch of mathematics that considers differential equations of arbitrary order in contrast to classical calculus. It eliminates the requirement that the order of differential equations has to be integer. Therefore, it generalizes conventional differential and integral equations and helps the modelling of the real world phenomena better [1, 2]. Fractional calculus has found applications in engineering, biology, control, viscoelasticity, electromagnetism, diffusion theory etc. [3]. By applying fractional calculus to electronics, sinusoidal oscillators, multi-vibrator circuits, phase locked loops, analogue fractional order controllers, differentiators-integrators and fractional order filters have emerged [3-23].

In the literature, several definitions of fractional derivatives have been proposed. One of them is the Riemann and Liouville fractional derivative, which is given as

$$\frac{d^{\alpha}}{dt^{\alpha}} f(t) \equiv D^{\alpha} f(t) = \frac{1}{\Gamma(1-\alpha)} \frac{d}{dt} \int_0^t \frac{f(\tau)d\tau}{(t-\tau)^{\alpha}} \qquad (1)$$

where Γ(.) is the Gamma function and fractional order α is 0<α≤1 [4]. Applying the Laplace transform to (1) with zero initial conditions yields

$$L\left\{{}_{0}^{C}D_{t}^{\alpha}(t)\right\}=s^{\alpha}F(s) \tag{2}$$

where s^{α} is called the fractional Laplacian operator [14].

Even though a non-integer order filter is usually required based on the specifications of applications, current practice rounds off the filter order to the nearest integer. Therefore, the filters used today are integer orders. However, this approach limits the freedom of design. Fortunately, introducing fractional calculus into filter design removes this limitation and presents some advantages. The main advantage is that it enables the stepping attenuation of the fractional filter that is –20×(*n*+α) dB/dec or –6×(*n*+α) dB/oct [2].

In all of the designs of fractional order filters, the fractional Laplacian operator s^{α} has been used, due to the fact that transfer functions can be designed easily. However, a standard two-terminal component, which meets the fractional Laplacian operator, has not as yet been produced. Therefore, different methods have been proposed for approximating the fractional Laplacian operator. By means of these methods, integer order transfer functions are achieved [16]. In previous studies on fractional filters, namely fractional domain first order filters and second order filters, researchers mostly prefer to emulate s^{α} via R-C networks [3, 13, 17]. Instead of following this procedure, in this study substitution of the integer order approximation function into s^{α} is preferred and then the final transfer function is used for implementation.

In this paper, by using the (1+α) order transfer function provided by [3], OTA-C based fractional step approximated Butterworth filter circuits of order (*n*+α) are designed and simulated. The aim of this study is not designing a new OTA active element or improving of OTA performance metrics. On the contrary, the target of this study is exploiting of OTAs presented features for designing fractional order filters.

2 Design steps of the fractional order filters

In this section, general design equations for the approximated fractional order low-pass and high-pass filters of orders of (1+α) and (*n*+α) are derived and given in order.

2.1 The Approximated fractional Butterworth low-pass filters of order (1+α)

The transfer function of the low-pass filter of order (1+α) was firstly introduced by [17] but it has an undesired peak in the pass-band. The modified version of the transfer function of the approximated fractional order Butterworth low-pass step filter was proposed by Freeborn et al. as [3]

$$H_{1+\alpha}^{FLP}=\frac{c_1}{s^{\alpha}(s+c_2)+c_3} \tag{3}$$

where c_1, c_2 and c_3 are coefficients which are determined by nonlinear curve fitting to achieve Butterworth characteristics in the frequency response. As mentioned above, there is no commercially available electronic device to make the characteristics of the fractional Laplacian operator s^{α} available. A solution of this problem is the using integer order circuits. Therefore, approximation methods like Carlson, Oustaloup, Matsuda, Continued Fraction Expansion (CFE) and the Charef method can be used. However, the resulting approximation functions are only valid in a limited frequency band. As the order of the approximation function increases, the accuracy as well as frequency band increase. Also, it demands more in terms of the hardware and power. Therefore, there is a trade-off between accuracy and cost in hardware. Among these methods, the CFE method was preferred in this study from the circuit complexity point of view [9, 24].

According to the CFE method, the second order approximation function of s^{α} is defined as [9]

$$s^{\alpha}\cong\frac{(\alpha^2+3\alpha+2)s^2+(8-2\alpha^2)s+(\alpha^2-3\alpha+2)}{(\alpha^2-3\alpha+2)s^2+(8-2\alpha^2)s+(\alpha^2+3\alpha+2)} \tag{4}$$

Substituting (4) into (3), the following integer order transfer function is derived as

$$H_{1+\alpha}^{FLPF}(s)\cong\frac{c_1}{m_0}\frac{(m_2s^2+m_1s+m_0)}{s^3+k_0s^2+k_1s+k_2} \tag{5}$$

The expressions for m_0, m_1, m_2 and k_0, k_1, k_2 are found as

$$\begin{aligned}
m_0&=\alpha^2+3\alpha+2\\
m_1&=8-2\alpha^2\\
m_2&=\alpha^2-3\alpha+2\\
k_0&=(m_1+m_0c_2+m_2c_3)/m_0\\
k_1&=(m_1(c_2+c_3)+m_2)/m_0\\
k_2&=(m_0c_3+m_2c_2)/m_0
\end{aligned} \tag{6}$$

The values of c_1, c_2 and c_3 are determined by curve fitting by minimizing the cumulative pass-band error between responses of $H_1^{BWLPF}(s)$ and $H_{1+\alpha}^{FLPF}(s)$, where $H_1^{BWLPF}(s)$ and $H_{1+\alpha}^{FLPF}(s)$ are the 1st order and the (1+α) order fractional Butterworth filter responses, respectively.

Before realizing the fractional order transfer functions, the stability of the fractional order transfer functions must be determined. To achieve that, the *s* to *w* domain transformation which requires that $w=s^{1/m}$ is selected. In this transformation, it is assumed that all of the fractional orders can be expressed as $\alpha_i=k_i/m$ (i=1,2,3,…) where *m* is the common factor. The stability condition of this method is that all of the pole angles $|\theta_{wi}|$ have to be greater than π/(2x*m*). Detailed information and examples about stability can be found in [25]. According to the *s* to *w* domain transformation, for α=0.3 and α=0.5, the following characteristic equations from (3) are obtained as

$$w^{13}+0.477w^3+0.8\ (\alpha=0.3) \tag{7a}$$

$$w^{15}+0.68w^5+0.859\ (\alpha=0.5) \tag{7b}$$

where $s=w^{1/10}$. For both of the characteristic equations, the stability condition is that the pole angles $|\theta_{wi}|$ (i=1,2,3,…) have to be greater than π/(2x10). The minimum pole angles for (7a) and (7b) are calculated as |15.1671°| and |14.1656°| respectively, which satisfy the stability condition being greater than 9°.

To realize the integer order transfer function of (5), a block diagram (BD) of the inverse follow the leader feedback (IFLF) with the input distribution form can be used. The function of (5) can also be achieved by cascading of the first order transfer function of an integrator and second order transfer function of the single amplifier biquad (SAB) or the multiple amplifier biquad (MAB). But this way does not provide electronic tuning capability, at the same time it increases design complexity and power consumption. Thus, the IFLF form design is preferred. The BD diagram of the fractional low-pass filter is shown in Fig.1 where G_i (i=0,1,2) corresponds to the scaled version of corresponding output quantity. The transfer function of this topology is expressed as

$$H(s)=\frac{\frac{G_2}{T_1}s^2+\frac{G_1}{T_1T_2}s+\frac{G_0}{T_1T_2T_3}}{s^3+\frac{1}{T_1}s^2+\frac{1}{T_1T_2}s+\frac{1}{T_1T_2T_3}} \tag{8}$$

where G_0, G_1, G_2 and T_1, T_2, T_3 are gains and time constants, respectively. By equating (5) with (8), it can be obtained that

$$\begin{aligned} &G_2=\frac{c_1m_2}{k_0m_0}, G_1=\frac{c_1m_1}{k_1m_0}, G_0=\frac{c_1}{k_2}\\ &T_1=\frac{1}{k_0}, T_2=\frac{k_0}{k_1}, T_3=\frac{k_1}{k_2} \end{aligned} \tag{9}$$

At the circuit realization, expressions in (9) will be utilized to determine the bias currents of OTAs in the filter.

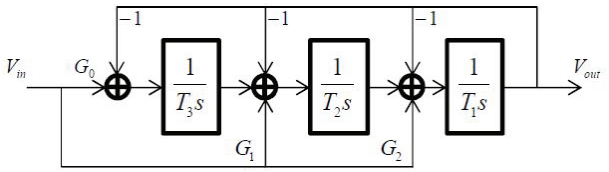


Figure 1: The BD diagram of the approximated Butterworth low-pass fractional order filter

2.2 The Approximated fractional Butterworth high-pass filters of order (1+α)

The transfer function of the fractional high-pass filters of order (1+α) can be obtained by replacing *s* with 1/*s* in (3). By performing this transformation and same steps in the Section 2.1, the following transfer function is derived as

$$H_{1+\alpha}^{FHPF}(s)\cong\frac{(c_1/c_3)}{k_0}\frac{(m_0s^3+m_1s^2+m_2s)}{s^3+\frac{k_1}{k_0}s^2+\frac{k_2}{k_0}s+\frac{k_3}{k_0}} \tag{10}$$

The expressions for m_0, m_1, m_2 are same as those in (6), but the expressions k_0, k_1, k_3 and k_4 are found as

$$\begin{aligned} k_0&=m_0+(m_2c_2/c_3)\\ k_1&=m_1+((m_1c_2+m_2)/c_3)\\ k_2&=m_2+((m_0c_2+m_1)/c_3)\\ k_3&=m_0/c_3 \end{aligned} \tag{11}$$

The BD diagram of the fractional high-pass filters of order (1+α) is portrayed in Fig.2. The transfer function of this topology is given by

$$H(s)=\frac{G_3s^3+\frac{G_2}{T_1}s^2+\frac{G_1}{T_1T_2}s}{s^3+\frac{1}{T_1}s^2+\frac{1}{T_1T_2}s+\frac{1}{T_1T_2T_3}} \tag{12}$$

By equating (10) with (12), it can be found that

$$G_3 = \frac{c_1 m_0}{c_3 k_0}, G_2 = \frac{c_1 m_1}{c_3 k_1}, G_1 = \frac{c_1 m_2}{c_3 k_2}$$
$$T_1 = \frac{k_0}{k_1}, T_2 = \frac{k_1}{k_2}, T_3 = \frac{k_2}{k_3} \quad (13)$$

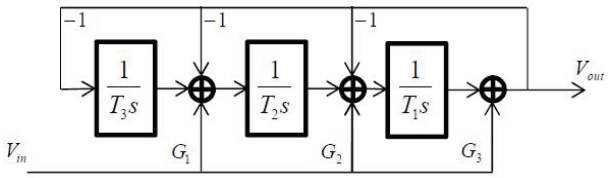


Figure 2: The BD diagram of the approximated Butterworth high-pass fractional order filter

2.3 Fractional low-pass filters of order (n+α)

The transfer functions of the fractional low-pass filters of order (*n*+α) could be reached by using polynomial division given by (14) [3]

$$H_{n+\alpha}^{FLPF}(s) = \frac{H_{1+\alpha}^{FLPF}(s)}{B_{n-1}^{LP}(s)} \quad (14)$$

where $H_{1+\alpha}^{FLPF}(s)$ is the fractional low-pass filter given by (5) and $B_{n-1}^{LP}(s)$ is the (*n*–1) order standard low-pass Butterworth polynomial.

From (14), the general form of fractional low-pass filters is derived as

$$H_{n+\alpha}^{FLPF}(s) \cong \frac{X_2 s^2 + X_1 s + X_0}{Y_{n+2} s^{n+2} + Y_{n+1} s^{n+1} + ... + Y_1 s + Y_0} \quad (15)$$

where the coefficients X_i (*i*=0,1,2) and Y_i (*i*=*n*+2, *n*+1,...0) can be found using k_j and m_j (*j*=0,1,2) in (5) and the coefficients of the Butterworth low-pass polynomial $B_{n-1}^{LP}(s)$.

The BD diagram of the fractional low-pass filters of order (*n*+α) is shown in Fig.3b. The transfer function of this topology is expressed as

$$H_{n+\alpha}^{FLPF}(s) = \frac{\frac{G_2}{T_1 T_2 ... T_n} s^2 + \frac{G_1}{T_1 T_2 ... T_{n+1}} s + \frac{G_0}{T_1 T_2 ... T_{n+2}}}{s^{n+2} + \frac{1}{T_1} s^{n+1} + \frac{1}{T_1 T_2} s^n + ... + \frac{1}{T_1 T_2 ... T_{n+2}}} \quad (16)$$

By equating (15) with (16), it can be obtained that

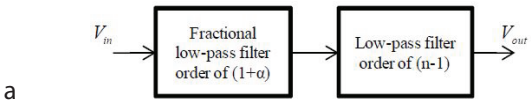
$$G_i = \frac{X_i}{Y_i}, i = 0,1,2$$
$$T_i = \frac{Y_j}{Y_{j-1}}, i = 1,2,...,n+2; j = n+2,...,1 \quad (17)$$

An alternative way of the realization of the fractional low-pass filters of (*n*+*α*) is the cascade connection of fractional order filter $H_{1+\alpha}^{FLPF}(s)$ and Butterworth filter of order (*n*–1) as portrayed in Fig.3a. The transfer function of the block is given as [23]

$$H_{n+\alpha}^{FLPF}(s) = H_{1+\alpha}^{FLPF}(s) \frac{1}{B_{n-1}^{LP}(s)} \quad (18)$$

where $B_{n-1}^{LP}(s)$ *is* the (*n*–1) order low-pass Butterworth polynomial.

a



b

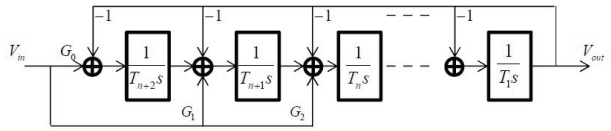


Figure 3: The realization of the approximated Butterworth low-pass fractional (*n*+α) order filters via: a cascade connection; b polynomial division

2.4 Fractional high-pass filters of order (n+α)

As following the similar procedure carried out in the section of the (*n*+α) order fractional low-pass filters, the developed BD diagram and design equations for their high-pass counterparts are depicted in Fig.4 and expressed as

$$H_{n+\alpha}^{FHPF}(s) = \frac{H_{1+\alpha}^{FHPF}(s)}{B_{n-1}^{HP}(s)} \quad (19)$$

where $H_{1+\alpha}^{FHPF}(s)$ is the fractional high-pass filter given by (10) and $B_{n-1}^{HP}(s)$ is the Butterworth high-pass polynomial derived by writing 1/*s* instead of *s* in $B_{n-1}^{LP}(s)$. Substituting (10) into (19), the general IFLF form of fractional high-pass filters is obtained as

$$H_{n+\alpha}^{FHPF}(s) \cong \frac{X_3 s^2 + X_2 s + X_1}{Y_{n+2} s^{n+2} + Y_{n+1} s^{n+1} + ... + Y_1 s + Y_0} \quad (20)$$

where the coefficients X_i (*i*=1,2,3) and Y_i (*i*=*n*+2, *n*+1,...0) can be derived using k_j (*j*=0,1,2,3) in (11) and m_j (*j*=0,1,2)

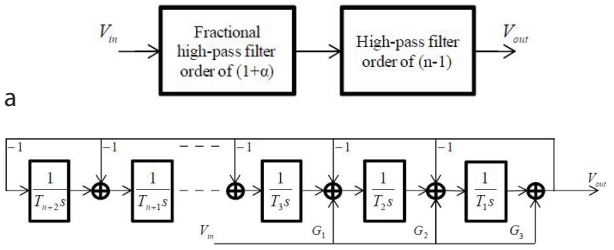
in (6) and the coefficients of the Butterworth high-pass polynomial $B^{HP}_{n-1}(s)$.

From Fig.4b, the transfer function of this topology is found as

$$H^{FHPF}_{n+\alpha}(s)=\frac{G_3 s^{n+2}+\frac{G_2}{T_1}s^{n+1}+\frac{G_1}{T_1T_2}s^{n}}{s^{n+2}+\frac{1}{T_1}s^{n+1}+\frac{1}{T_1T_2}s^{n}+.....+\frac{1}{T_1T_2...T_{n+2}}} \quad (21)$$

By equating (20) with (21), it can be obtained that

$$G_i=\frac{X_i}{Y_j}, i=1,2,3;\ j=n,n+1,n+2$$
$$T_i=\frac{Y_j}{Y_{j-1}}, i=1,2,...,n+2;\ j=n+2,...,1 \quad (22)$$



a

b

Figure 4: The realization of the approximated Butterworth high-pass fractional (*n*+α) order filters via: a cascade connection; b polynomial division

The transfer function of the Fig.4a is given by

$$H^{FHPF}_{n+\alpha}(s)=H^{FHPF}_{1+\alpha}(s)\frac{1}{B^{HP}{}_{n-1}(s)} \quad (23)$$

where $B^{HP}_{n-1}(s)$ is the (*n*–1) order high-pass Butterworth polynomial.

Band-pass filters can also be attained by cascading the high-pass and low-pass filters as demonstrated in Fig.5.

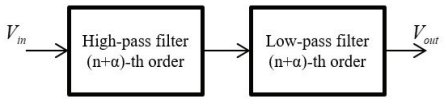


Figure 5: The realization of the approximated Butterworth band-pass fractional (*n*+α) order filters via cascade connection

3 OTA-C based realizations of the fractional filters

To achieve very low cut-off frequencies with OTA-C filters, very low transconductance values are required. In order to achieve low transconductance values, the OTA structure shown in Fig.6 is chosen [26]. It is chosen due the fact that this OTA building block has very simple internal construction to provide advantages of less power consumption and chip area. At the same time, it allows a wide range of transconductance controllability. Moreover, its linear input range is improved over the classical differential pair. In this scheme, the input voltages V_{ip} and V_{in} are applied to improved cross coupled MOS (Metal Oxide Semiconductor) cell composed of M_1-M_2 and M_3-M_4. The output current I_0 is related to input differential voltage (V_{ip}–V_{in}) as $I_0=g_m\times(V_{ip}-V_{in})$. The OTA is biased in manner of operating in subthreshold region for low voltage operation. The transconductance of the OTA is adjusted by the bias current source I_B. The supply voltages V_{DD} and V_{CC} are selected as +0.75 V and –0.75 V, respectively. The output current expression of the chosen OTA is given by

$$I_o=I_B\left(\tanh\left(\frac{V_{id}}{2nV_T}+\frac{\ln m}{2}\right)+\tanh\left(\frac{V_{id}}{2nV_T}-\frac{\ln m}{2}\right)\right) \quad (24)$$

where the V_{id} is the input voltage difference (V_{ip}–V_{in}), V_T is the thermal voltage, *m* is the ratio of aspect ratios of the M_1(M_2) and M_3(M_4) and *n* is the subthreshold slope factor.

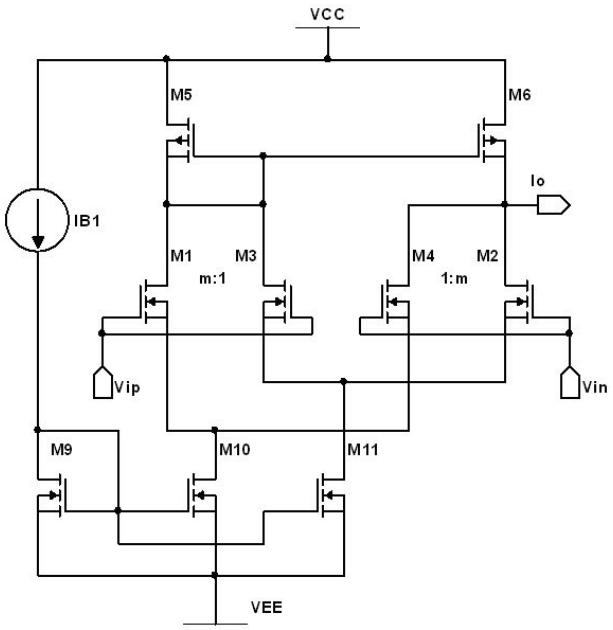


Figure 6: The used OTA structure

The realized filter topologies are depicted in Fig.7 and Fig.8, respectively. From these figures, the related time constants could be expressed as

$$T_k = \frac{C_k}{g_{mk}} \tag{25}$$

where k is 1, 2 and 3.

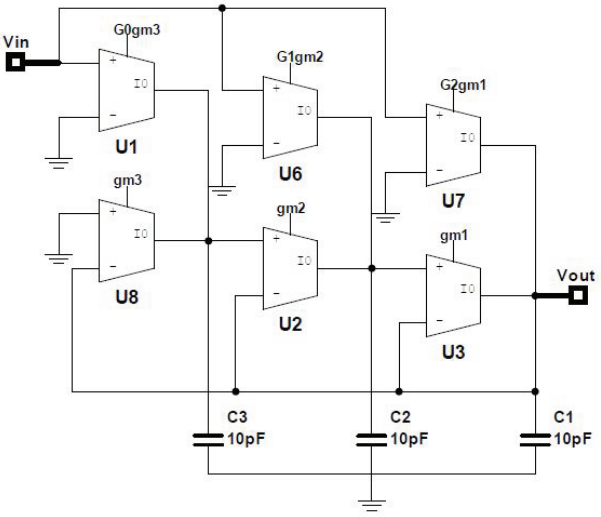


Figure 7: The circuit of OTA-C based fractional order Butterworth low-pass filter of order (1+α)

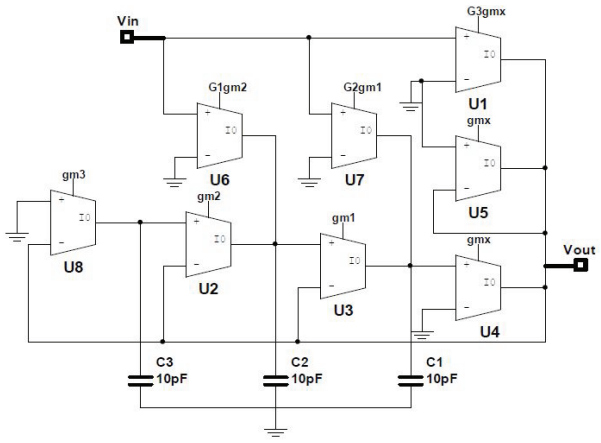


Figure 8: The circuit of OTA-C based fractional order Butterworth high-pass filter of order (1+α)

Adding extra (n–1) OTA-C integrators to Fig.7 and Fig.8, the (n+α) order low-pass and high-pass filters are realized according to the polynomial division method, respectively. If the cascade connection method is preferred, the circuit of the (n–1) order corresponding Butterworth filters should be connected to output ports of circuits in Fig.7 and Fig.8, respectively.

4 Simulation

In this section, while the circuit level simulations of the OTA-C based low-pass and high-pass filters of order (n+α) are performed via PSPICE with 0.35 μm TSMC CMOS technology parameters, their corresponding transfer functions are simulated numerically. Then both of the results are given in comparative way.

4.1 The Approximated fractional Butterworth low-pass filters

The parameters given by (9) are calculated and the scaled versions according to f = 100Hz are given in Table 1 for α = 0.3 and α = 0.5.

Table 1: The calculated parameters given by (9) for α = 0.3 and α = 0.5

	α = 0.3	α = 0.5
T_1	$4.6\ 10^{-4}$	$5.5\ 10^{-4}$
T_2	$14\ 10^{-4}$	$14\ 10^{-4}$
T_3	$61\ 10^{-4}$	$54\ 10^{-4}$
G_0	1.01	1.01
G_1	0.685	0.6
G_2	0.115	0.07

From Table 1, the required bias currents of OTAs for α = 0.5 and for α = 0.3 with the equal values of the integrator capacitors of 10 pF are calculated and given in Table 2.

Table 2: The calculated bias current of OTAs according to Table 1

	α = 0.3	α = 0.5
I_{b1}	1.8 nA	1.5 nA
I_{b2}	573 pA	597 pA
I_{b3}	135 pA	154 pA

The results of frequency simulations for α = 0.5 and α = 0.3 are demonstrated in Fig.9, the corresponding theoretical values are also given in same figure. It can be clearly seen from the Fig.9 that the stop-band attenuation changes according to the fractional order α which supports the theoretical statements, as it is expected. The derived stop-band attenuations for α = 0.5 and α = 0.3 are respectively –30.4 dB/dec and –25.61 dB/dec in the range of 628 to 6280 rad/sec, which are close to –20×(1.5) dB/dec = –30 dB/dec and –20×(1.3) dB/dec = –26 dB/dec. Therefore, unlike the integer order filters, stop-band attenuation of –20×(α+1) dB/dec can be achieved closely. Moreover, the stop-band attenuation increases by increasing the order α. However, it should

be taken into account that there is not a very precise slope of attenuation beyond 6280 rad/sec because the used approximation function is just the second order form. On the other hand, the filter presents quite flat response in the pass-band for the all values of α.

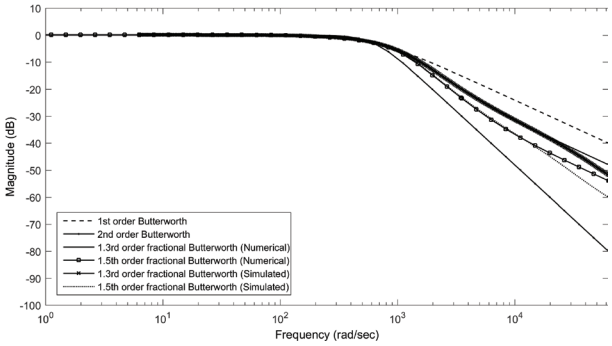


Figure 9: The numerical and simulated responses of fractional Butterworth low-pass filters of different orders

The power dissipations of low-pass filters of orders 1.3 and 1.5 are derived as 14.6 nW and 13 nW, respectively. Hence, the proposed filter topologies are suitable for low power applications.

In order to compare proposed filter circuits with the others in the literature, some performance parameters are given in Table 3. It can be deduced from Table 3 that proposed circuits outperform the work in [23] in terms of power efficiency as well as slope of stop-band attenuation. Additionally, proposed filters support electronic tuning in contrast to the work in [23]. On the other hand, even though the work in [22] has advantages over proposed circuits in terms of power consumption and supply voltage, it needs very low and accurate bias currents so it can be very difficult to achieve such a very low and accurate current levels. Different from works of [22-23], comparing proposed circuits with the others, proposed filters have advantages of the low power consumption and low supply voltage, integration capability, good slope of the stop-band attenuation and electronic tunability. But it should be considered that other circuits except the works of [22-23] are based on discrete form circuit components.

To observe output Total Harmonic Distortion (THD) level, a fixed frequency of 30 Hz and variable amplitude sinusoidal input signal is applied to the fractional low-pass filters. The realized output is presented in Fig.10.

Table 3: The comparison of some performance parameters of the fractional order filters of order 1.5

		[3]	[14]	[16]	[18]	[22]	[23]	This study
Filter Types		LP-HP	LP-HP BP -BR	LP-HP BP	LP	LP-HP	LP	LP-HP
Approx. Method - order		CFE -2nd	CFE -4th	CFE -2nd	FEA	CFE -2nd	CFE -2nd	CFE -2nd
Circuit configuration		FPAA based	RLC circuit	SAB circuit	CCII based	Sinh/Log domain building block based	DDCC based	OTA based
Mode		VM	VM	VM	VM	CM	VM	VM
Technology		-	-	-	-	0.18 µm	0.35 µm	0.35 µm
Voltage supply		-	-	-	-	500 mV	±500 mV	±750mV
Electronic tunability		Supported	Not supported	Not supported	Not supported	Supported	Not supported	Supported
Integration capacitor (min)		-	-	-	-	60 pF	751 pF	10 pF
Power cons. (Sim.)	LP	-	-	-	-	5.47 nW	185 µW	13 nW
	HP					3.56 nW	-	42.7 nW
Cut-off freq. (Theo.\Sim..)	LP	1 kHz \ -	1 kHz \ -	- \ -	- \160 Hz	10 Hz \11.8 Hz	1.7 kHz \-	100 Hz \101.6 Hz
	HP	10 kHz \ -	- \ -	- \ -	- \ -	- \3.87 Hz	- \ -	100 Hz \100.3 Hz
Stop-band attenuations Sim. (Theoretically -30 dB/ dec or -6 dB/oct)	LP	-30.75 dB/ dec	-	-29.74 dB/dec	-	-9.1 dB/oct	-31 dB/dec	- 30.4 dB/dec
	HP	-29.49 dB/ dec	-	-	-	-9.2 dB/oct	-	-29.7 dB/dec

It is clearly seen that, the THD level is acceptable up to 120 mV input amplitude.

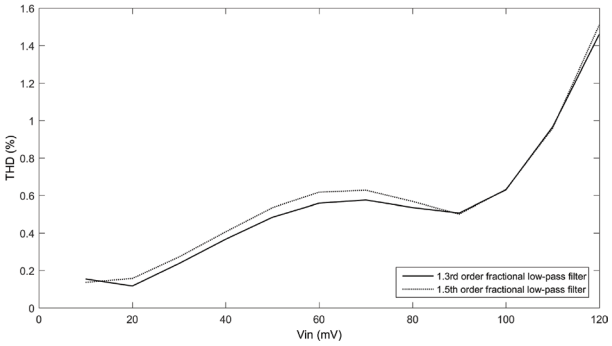


Figure 10: The output THD versus a fixed frequency-variable amplitude input voltage

To evaluate the time domain response of the low-pass filter, as an input, a 30 Hz sinusoidal signal with 50 mV amplitude is applied to filter of order α = 0.5. The obtained output signal is shown in Fig.11.

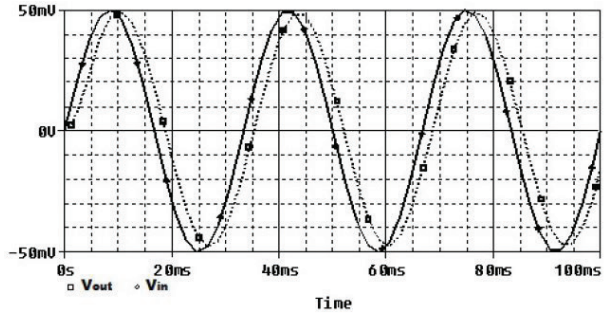


Figure 11: The time domain response of the 1.5th order fractional Butterworth low-pass filter

To gain more insights about higher order fractional filters and show applicability of the cascade realization, the simulated responses of the 2.3rd and 2.5th order fractional low-pass filters are depicted in Fig.12. The power dissipations of low-pass filters of orders 2.3 and 2.5 are derived as 17 nW and 15.3 nW, respectively. The simulated pass-band attenuations of these filters are respectively –45.3 dB/dec and –50.13 dB/dec while their theoretical values are –45 dB/dec and –50 dB/dec.

4.2 The Approximated fractional Butterworth high-pass filters

The parameters provided by (13) are calculated and given in Table 4 for α = 0.3 and α = 0.5, respectively.

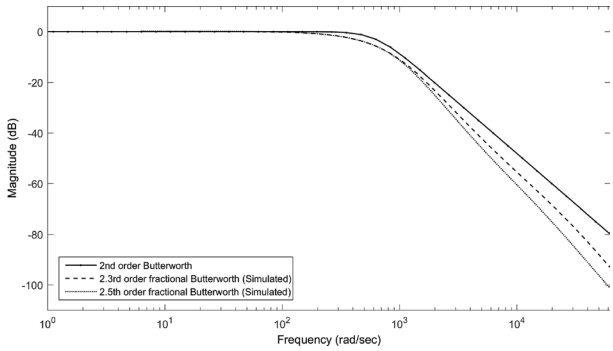


Figure 12: The simulated responses of the 2.3rd and 2.5th order fractional Butterworth low-pass filters

Table 4: The calculated parameters given by (13) for α = 0.3 and α = 0.5

	α = 0.3	α = 0.5
T_1	$4.13\ 10^{-4}$	$4.71\ 10^{-4}$
T_2	$18\ 10^{-4}$	$18\ 10^{-4}$
T_3	$55\ 10^{-4}$	$46\ 10^{-4}$
G_1	0.12	0.07
G_2	0.68	0.6
G_3	1	1

According to Table 4, the corresponding bias currents of OTAs for α = 0.5 with the same values of the capacitors of 10 pF are obtained and presented in Table 5.

The results of simulations for α = 0.3 and α = 0.5 are illustrated in Fig.13. It can be deduced from the Fig.13 that the stop-band attenuation changes according to fractional order α. The reached stop-band attenuations for α = 0.5 and α = 0.3 are respectively –29.7 dB/dec and –25.5 dB/dec, which are close to –20×(1.5) dB/dec = –30 dB/dec and –20×(1.3) dB/dec = – 26 dB/dec.

Table 5: The calculated bias current of OTAs according to Table 4

	α = 0.3	α = 0.5
I_{b1}	2 nA	1.75nA
I_{b2}	467 pA	448 pA
I_{b3}	149 pA	178 pA
I_{bx}	2 nA	2 nA

The power consumptions of high-pass filters of orders 1.3 and 1.5 are simulated as 45.2 nW and 42.7 nW, respectively. The main reason of higher power dissipations of the high-pass filters in contrast to their low-pass counterparts is the summation node constructed by the U4(g_{mx}) and U5($1/g_{mx}$) shown in Fig.8.

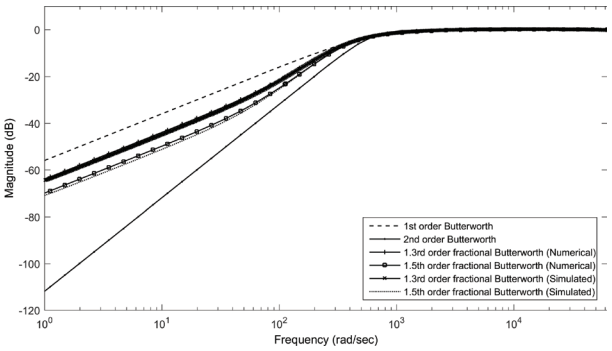


Figure 13: The numerical and simulated responses of fractional Butterworth high-pass filters of different orders

To evaluate output THD level versus input voltage, a fixed frequency of 1 kHz and variable input sinus is applied to the fractional high-pass filters. The obtained THD level doesn't exceed 2.9% up to 120 mV input voltage. Thus, the high-pass filters can be kept in acceptable THD range up to 120 mV input amplitude.

To attain higher order fractional high-pass filters, the cascade connection is preferred because of its simplicity. The simulated responses of the 2.3rd and 2.5th order fractional high-pass filters are presented in Fig.14. The power dissipations of high-pass filters of orders 2.3 and 2.5 are derived as 47.5 nW and 45 nW, respectively. The simulated pass-band attenuations of these filters are respectively –45.1 dB/dec and –49.3 dB/dec while their theoretical values are –46 dB/dec and –50 dB/dec.

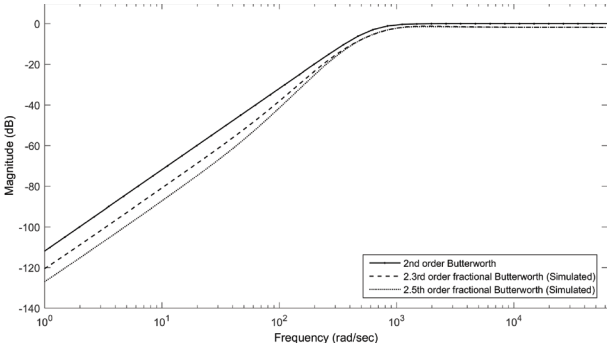


Figure 14: The simulated responses of the 2.3rd and 2.5th order fractional Butterworth high-pass filters

5. Conclusion

In this study, the OTA-C based approximated fractional order Butterworth filters are introduced, designed and simulated. The general design equations are derived and given in order for the readers. Even though the fractional filters are approximated by higher degree integer order transfer functions or R-C networks composed of the many branches, these are the simple ways of circuit implementations until fractional electronic components become commercially available. The simulation results confirm theoretical statements. However, it should be taken into account that there are small deviations from the ideal cases due to approximation functions, rounding errors and the non-ideal characteristics of active elements. Nevertheless, it can be said that unlike their integer order counterparts, fractional order filters provide fractional stepping attenuation in the stop-band. Furthermore, it can be deduced from simulations that the proposed filter topology is appropriate for low amplitude-low frequency signals like biomedical signals, such as EEG (electroencephalograph), EOG (electrooculogram). This is because the frequency bandwidth of the filters is not very wide owing to the approximation functions used. At the same time, since the proposed fractional filter topologies allow for attenuation of less than multiples of 20 dB/dec, more information could be kept in the stop-band in comparison with their integer order counterparts. In addition, the proposed filter circuits allow for electronic tuning of order and frequency response without any structural changes on related topologies and also provide the low-voltage low-power operation.

6 References

1. Ortigueira, M. D: 'An introduction to the fractional continuous time linear systems: the 21st century systems', IEEE Circuits and Systems Magazine, 2008, 8, (3), pp. 19-26
2. Elwakil, A. S.: 'Fractional-order circuits and systems: emerging interdisciplinary research area', IEEE Circuits and Systems Magazine, 2010, 10, (4), pp. 40-50
3. Freeborn, T. J., Maundy, B., Elwakil, A. S.: 'Field programmable analogue array implementation of fractional step filters', IET Circuits, Devices and Systems, 2010, 4, (6), pp. 514-524
4. Radwan, A. G., Elwakil, A. S., Soliman, A. M.: 'Fractional-order sinusoidal oscillators: design procedure and practical examples', IEEE Transactions on Circuits and Systems-1, 2008, 55, (7), pp. 2051-2063
5. Maundy, B., Elwakil, A., Gift, S.: 'On a multivibrator that employs a fractional capacitor', Analog Integrated Circuits and Signal Processing, 2010, 62, pp. 99-103
6. Tripathy, M. C., Mandal, D., Biswas, K., *et al.*: 'Design and performance study of phase locked-loop using fractional order loop filter', International Journal of Circuit Theory and Applications, 2014, 43, (6), pp. 776-792

7. Podlubny, I., Petras, I., Vinagre, B. M., *et al.*: 'Analogue realizations of fractional-order controllers', Nonlinear Dynamics, 2002, 29, (1), pp. 281-296
8. Bohannan, G. W.: 'Analog fractional order controller in temperature', Journal of Vibration and Control, 2008, 14, (9-10), pp. 1487-1498
9. Krishna, B. T.: 'Studies on fractional order differentiators and integrators: a survey', Signal Processing, 2011, 91, (3), pp. 386-426
10. Santamaria, G., Valuerde, J., Perez-Aloe, R., *et al.*: 'Microelectronic implementations of fractional order integrodifferential operators', Journal of Computational and Nonlinear Dynamics, 2008, 3, (2).
11. Varshney, P., Gupta, M., Visweswaran, G. S.: 'Implementation of switched capacitor fractional order-differentiator (PD^{δ}) circuit', International Journal of Electronics,2008, 95, (6), pp. 1105-1126
12. Acharya, A., Das, S., Pan, I., *et al.*: 'Extending the concept of analog Butterworth filter for fractional order systems', Signal Processing, 2014, 94, pp. 409-420
13. Radwan, A. G., Elwakil, A. S., Soliman, A. M.: 'On the generalization of second order filters to the fractional order domain', Journal of Circuits, Systems and Computers, 2009, 18, (2), pp. 361-386
14. Freeborn, T. J., Maundy, B., Elwakil, A.: 'Fractional resonance based RLβCα filters', Mathematical Problems in Engineering, 2013, (2013)
15. Soltan, A., Radwan, A. G., Soliman, A. M.: 'Butterworth passive filter in the fractional order', International Conference on Microelectronics, Hammamet, 2011, pp. 1-5
16. Maundy, B., Elwakil, A. S., Freeborn, T. J.: 'On the practical realization of higher-order filters with fractional stepping', Signal Processing, 2011, 91, (3), pp. 484-491
17. Radwan, A., Soliman, A., Elwakil, A.: 'First order filters generalized to the fractional domain', Journal of Circuits, Systems and Computers, 2008, 17, (1), pp. 55-66
18. Soltan, A., Radwan, A. G. &Soliman, A. M.: 'CCII based fractional filters of different orders', Journal of Advanced Research, 2014, 5, (2), pp. 157-164
19. Freeborn, T., Maundy, B., Elwakil, A. S.: 'Approximated fractional order Chebyshev lowpass filters', Mathematical Problems in Engineering, 2014, (2014)
20. Tripathy, M. C., Biswas, K., Sen, S.: 'A design example of a fractional order Kerwin-Huelsman-Newcomb biquad filter with two fractional capacitors of different order', Circuits, Systems, and Signal Processing, 2013, 32, (4), pp. 1523-1536
21. Tripathy, M. C., Mandal, D., Biswas, K., *et al.*: 'Experimental studies on realization of fractional inductors and fractional order bandpass filters', International Journal of Circuit Theory and Applications, 2014, 43, (9), pp. 1183-1196
22. Tsirimokou, G., Laoudias, C., Psychalinos, C.: '0.5-V fractional order companding filters', International Journal of Circuit Theory and Applications, 2014, 43, (9), pp. 1105-1126
23. Khateb, F., Kubanek, D., Tsirimokou, G., *et al.*: 'Fractional order filters based on low voltage DDCCs', Microelectronics Journal, 2016, 50, pp. 50-59
24. Das., P., Pan, I.: 'Basics of fractional order signals and systems', 'Fractional Order Signal Processing: Introductory Concepts and Applications' (Springer Press, 2012), pp. 13-30
25. Radwan, A. G., Soliman, A. M., Elwakil, A. S. et al.: 'On the stability of linear systems with fractional order elements', Chaos, Solitans and Fractals, 2009, 40, (5), 2317-2328
26. 'Transconductors in subthreshold CMOS', http://wordpress.nmsu.edu/pfurth/files/2015/06/cissd1995.pdf, accessed 22 November 2016

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A Novel Space Vector Modulation Based Control Strategy for Z-Source Inverter

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Abstract: In this study, a novel control strategy based on Distributed Space Vector Modulation is proposed to improve dynamic performance of a Z Source Inverter (ZSI) while utilizing only capacitor voltage feedback. Distributed space vector modulation allows ZSI output voltage to be controlled by Z source capacitor voltage with a simple equation. Therefore, only one voltage feedback is enough to control inverter output voltage. Furthermore, zero state is not utilized in the proposed control strategy, so an additional control loop for the modulation index is no longer necessary. Flexible modulation index allows work with flexible dc line voltage and limits the voltage stresses in the inverter switches so ZSI has low cost switches and high efficiency. Moreover, the proposed control method was investigated for both resistive and inductive loads due to ZSI load power factor-dependent characteristics. The effectiveness of the suggested control method is verified by Matlab/Simulink simulations, considering the sudden changes in both the dc source and load level.

Keywords: dc-ac power converters; inverters; power conditioning; impedance source inverters ; power system dynamics; linear feedback control systems.

Kontrolna strategija inverterja na osnovi modulacije prostorskega vektorja

Izvleček: Predstavljena je nova kontrolna strategija na osnovi distribuirane modulacije prostorskega vektorja za izboljšanje dinamičnih lastnosti inverterja z Z virom (ZSI) le z uporabo kapacitivne napetostne povratne zanke. Distribuirana modulacija prostorskega vektorja omogoča nadzor izhodbe napetosti ZSI z napetostjo vhodnega kondenzatorja z eno preprosto enačbo. Za nadzor napetosti je tako potrebna le ena povratna zanka. V strategiji ni uporabljeno ničelno stanje. Kontrolna zanka za modulacijo prav tako ni več potrebna. Fleksibilen modulacijski indeks omogoča delo s fleksibilno dc napetost in omejuje napetostni stres v stikalih inverter, kar omogoča uporabo cenenih stikal z visokim izkoristkom. Predlagana kontrola je bila uporabljena na rezistivnih in induktivnih bremenih. Učinkovitost metode je bila preverjena v Matlab/Simulink okolju.

Ključne besede: dc-ac močnostni pretvornik; inverter; dinamika moči; linearna povratna zanka

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1 Introduction

Power conditioning units (PCU) are widely used in different areas like industry, energy plants, transportation, etc. Z Source Inverter (ZSI) is an emerging and promising topology for these units, having significant benefits such as buck-boost capability, low cost, reduced volume, and higher efficiency when compared to Voltage Source and Current Source Inverters [1]. Due to its advantages, ZSI has been widely investigated from various aspects; i.e., modulation methods, closed loop control methods, design, and novel topologies [2, 3].

Although ZSI has some significant superiorities, it has the drawback of poor dynamic performance. ZSI output voltage amplitude depends on both modulation index (M) and dc line voltage, so it is strictly connected with a shoot through duty ratio (D). ZSI has a buck-boost characteristic; similar to other buck-boost converters, the transfer function between shoot through duty ratio and ZSI output has a right half plane zero [4]. RHP zero causes an instability in the system. During step changes in shoot through the duty cycle, an initial collapse dip occurs in the capacitor voltage, followed by a damped oscillation. This causes a disturbance in the output voltage of the inverter [5],[6]. Therefore, proper controller design is needed for high dynamic performance. There are many researches dealing with this problem, and their suggestions can be classified

under four groups: capacitor voltage control, direct DC line voltage control, indirect DC line voltage control, and unified control.

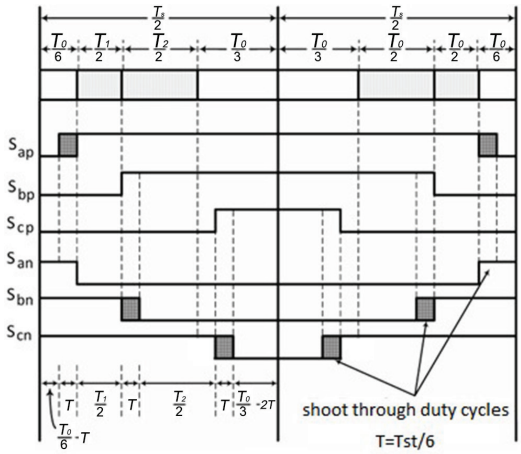
Using [7, 8] only capacitor voltage (Vc) has been suggested for controlling. In this method, Vc is kept constant; however, output voltage stability and voltage stress across switches have not been considered. In [9, 10] one model, predictive control has been proposed to keep Vc constant; however, it has four current sensors and a voltage sensor for feedbacks. Therefore, it is too complicated and too expensive. In direct dc line voltage control [6], an external sensing circuit has been given to measure dc line voltage (Vi) directly and stabilize it due to the pulsating nature of dc line voltage. However, the complex design of the external sensing circuit makes the control system expensive. In [6], [11-13], indirect dc line voltage control methods have been proposed to eliminate Vi measurement problems because of their pulsating nature. Nevertheless, they utilize zero state (Z) as a margin between D and M, because they use the constant modulation index as a result of constant Vi. Thus, they work with a low modulation index and a high dc line voltage. As a result, their voltage stress across bridge switches and switching losses are much higher than they could be. In [14] a unified control method is proposed, with an output voltage control loop getting feedback directly from ZSI output. Shoot through duty ratio and modulation index are controlled simultaneously. The main *drawback* of this method occurs in grid-tied applications, because output voltage feedback is fixed to network voltage.

Choosing the correct modulation technique is also an important factor for ZSI control design. There are different modulation techniques for ZSI in literature: Simple Boost Control, Maximum Boost Control, Maximum Constant Boost Control, Traditional Space Vector Modulation, and Modified Space Vector Modulation. A detailed comparison of these methods has been given in [15]. It is very important to choose the right modulation technique to achieve the lowest voltage stress on switches, highest efficiency, and the lowest THD.

In the majority of power conditioning units, the main goal of the control loops is to achieve a stable output at the desired level. When we consider ZSI in a PCU, the control loop should be focused on getting a stable output voltage. Nevertheless, most previous researches endeavored to be keep the capacitor voltage (Vc) or dc line voltage (Vi) constant. Moreover, in order to limit voltage stress across inverter bridge and switching losses, ZSI should operate with the lowest possible dc line voltage. None of the aforementioned methods have been taken into account, both in order to simultaneously obtain a stable output during transients and to limit switching losses. An indirect output voltage governed by controlling impedance network capacitor voltage is preferred to overcome the drawbacks listed above and to get a simple configuration [16].

ZSI behavior is affected by load power factor and has been investigated in some researches [17-18]. For this reason, the effectiveness of the controller used in ZSI for different power factor levels needs to be validated. In this paper, a PI control strategy has been given considering different power factor levels. Transfer function between shoot through duty ratio and inverter output voltage is needed to design a PI compensator. Thus, a dynamic model of ZSI is obtained by state space averaging and small signal analysis. There are some studies about dynamic modelling of ZSI in the literature, such as [8], [13], [19-21]. However, the modulation index is not considered as a control variable. Moreover, they do not consider input voltage as a perturbation source; in this case, the input voltage drop scenario would not be reflected in the model. The ZSI dynamic model, which is given in this research, considers all of these issues and is utilized to control output transfer function. The designed PI controller considering this dynamic model is tested with simulations.

a)



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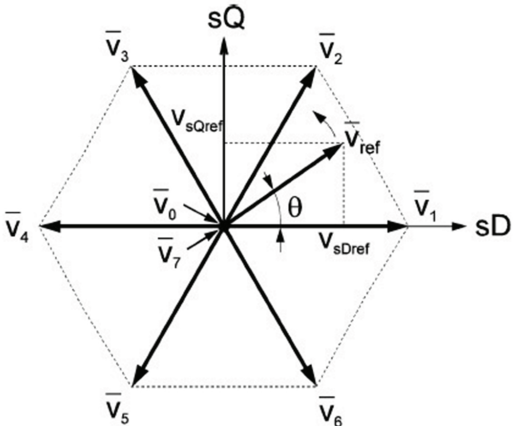


Figure 1: a) DSVM switching pattern; b) Voltage space vectors

2 Distributed Space Vector Modulation

The Distributed Space Vector Modulation (DSVM) switching pattern is given in Figure 1. Shoot through duty cycles are divided into six parts, which are settled not only into zero states but also between active states. This results in a well-balanced distribution of shoot through states and thus a better performance can be achieved.

DSVM gives the chance to get the highest DC bus utilization, and DSVM allows ZSI output voltage estimation with only z-source capacitor voltage feedback. The DSVM scheme can be seen in Figure 1. Related equations are given in (1)-(6).

$$V_k = \left(\frac{2}{3}\right) V_{in} \tag{1}$$

$$V_{ref\_max} = V_{out\_peak} = \left(\frac{\sqrt{3}}{2}\right) V_k \tag{2}$$

$$V_{outpeak} = \frac{V_{i_{peak}} M}{\sqrt{3}} \tag{3}$$

$$M = 1 - D \tag{4}$$

$$V_{i_{peak}} = \frac{V_c}{1 - D} \tag{5}$$

$$V_{out_{peak}} = \frac{V_c}{\sqrt{3}} \tag{6}$$

The terms used in these equations are described below.
k: voltage space vector number (1,2...6)
V_i: ZSI dc line voltage
V_{in}: ZSI dc input voltage
$V_{ref,max}$: ZSI ac output voltage peak value (reference)
V_{out}: ZSI ac output voltage
M: modulation index
D: shoot through duty ratio
V_c: ZSI impedance network capacitor voltage

As can be seen from (4), no zero state is used in the proposed control method. Thus, it is guaranteed to get the minimum possible dc line voltage and the minimum voltage stress to get the desired output voltage level. According to (6), the ZSI output voltage can be estimated by a very simple calculation using only the capacitor voltage feedback. This is a very precious relationship because it allows ZSI output voltage control without output voltage feedback. So, it is possible to control ZSI output voltage indirectly by capacitor voltage control. It is necessary to achieve control to output transfer function to design a suitable controller. So, this is needed to get a dynamic model of ZSI.

3 Modelling of ZSI

It is essential to get a dynamic model of ZSI to analyze both steady state and transient operation; it is also essential to get a transfer function between shoot through duty ratio and z source capacitor voltage to design a proper controller. However, ZSI has a nonlinear characteristic, as can be seen in Figure 2.

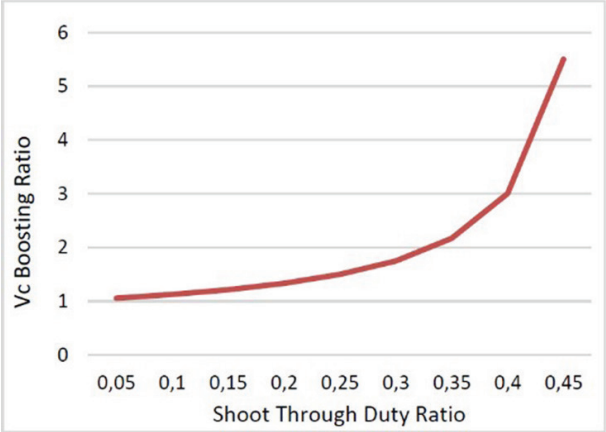


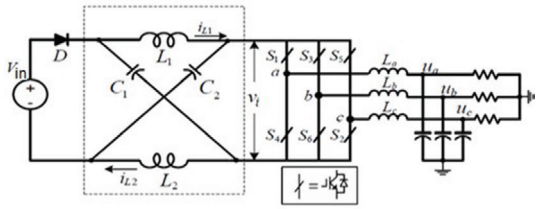
Figure 2: Nonlinear relationship between shoot through duty ratio and capacitor voltage boosting ratio

Because of the nonlinear characteristic of ZSI, the system shall be linearized around an equilibrium point due to utilizing a linear controller. Therefore, the state space averaging method is used to get the ZSI model, and small signal analysis is used to linearize the system around an equilibrium point. Although previous researches have ignored the modulation index as a control variable, in this research it is considered a control variable to determine the exact dynamic inverter model. Moreover, it is also essential to consider input voltage as a perturbation source to get a model for analyzing dynamic problems like inverter input voltage drop.

In order to simplify ZSI ac side as a dc load it has been considered ZSI has a balanced load. The circuit diagram can be seen in Figure 3.

Three states are considered while modelling ZSI: shoot through mode, zero voltage vector mode, and active voltage vector mode. These modes can be shown with the proper switch states in Table 1.

a)



b)

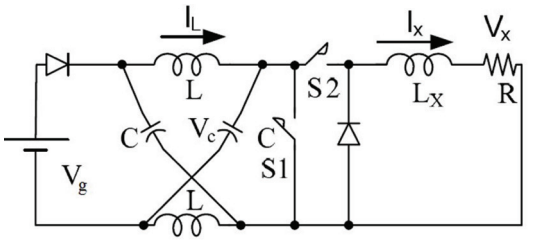


Figure 3: a) ZSI basic structure; b) DC equivalent ZSI circuit

Table 1: ZSI operatıng modes accordıng to swıtch modes

Item	S1 Position	S2 Position
ZERO STATE	OPEN	OPEN
SHOOT THROUGH	CLOSED	OPEN
ACTIVE STATE	OPEN	CLOSED

In this model the state variables are inductance current, capacitor voltage, and load current.

$$x(t)=\left[i_L(t)\ v_c(t)\ i_x(t)\right] \tag{7}$$

Considering three operating modes and using the state space averaging method, the state space average model can be written as in (8).

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_c(t) \\ i_{Lx}(t) \end{bmatrix}=\begin{bmatrix} 0 & \frac{2d-1}{L} & 0 \\ \frac{1-2d}{C} & 0 & -\frac{m}{C} \\ 0 & \frac{2m}{L_x} & -\frac{R_x}{L_x} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_c(t) \\ i_{Lx}(t) \end{bmatrix}+ \\ +\begin{bmatrix} \frac{V_{in}}{L}(1-d) \\ 0 \\ \frac{V_{in}}{L_x}m \end{bmatrix} \tag{8}$$

As can be seen in (8), i_L, v_c, and i_x are state variables, M and D are control variables, and v_c and v_x are the outputs to be controlled.

Steady state equations of state variables can be derived from the state space model, as in (9)-(11).

$$V_c=\frac{D'}{D'-D}V_{in} \tag{9}$$

$$I_L=\frac{D'}{D'-D}I_{Lx} \tag{10}$$

$$I_{Lx}=\frac{V_c}{R_x} \tag{11}$$

Small signal analysis was used to linearize the system around an equilibrium point. In this analysis, the general form for the variable is $x=X+\hat{x}(t)$, where *X* is the variable's component at the equilibrium point, *x* is the variable in the state space model (as in (7)), and is the perturbation signal. By using these formulas for all the variables, the state space model to be used for the dynamic model can be achieved as in (12).

$$\begin{bmatrix} s\hat{I}_L \\ s\hat{V}_c \\ s\hat{I}_x \end{bmatrix}=\begin{bmatrix} 0 & \frac{2D-1}{L} & 0 \\ \frac{1-2D}{C} & 0 & -\frac{M}{C} \\ 0 & \frac{2M}{L_x} & -\frac{R_x}{L_x} \end{bmatrix}\begin{bmatrix} \hat{I}_L \\ \hat{V}_c \\ \hat{I}_x \end{bmatrix}+ \\ +\begin{bmatrix} \frac{1-D}{L} & \frac{2V_c-V_{in}}{L} & 0 \\ 0 & -\frac{2I_L}{C} & -\frac{I_x}{C} \\ -\frac{M}{L_x} & 0 & \frac{2V_c-V_{in}}{L_x} \end{bmatrix} \tag{12}$$

State equations of ZSI small signal analysis are given in (13)-(15).

$$sL\hat{i}_L=(2D-1)\hat{v}_c+(1-D)\hat{v}_{in}+(2V_c-V_g)\hat{d} \tag{13}$$

$$sC\hat{v}_c=(1-2D)\hat{i}_L-M\hat{i}_x-2I_L\hat{d}-I_x\hat{m} \tag{14}$$

$$sL_x\hat{i}_x=2M\hat{v}_c-R_x\hat{i}_x-M\hat{v}_{in}+(2V_c-V_{in})\hat{m} \tag{15}$$

It is possible to control the output transfer function by using small signal equations and steady state equa-

$$G_{VcD}(s)=\frac{(-2I_LL_xL)s^2+(2L_xV_c-L_xV_{in}-4DL_xV_c+2DL_xV_{in}-2I_LLR_x)s}{(CL_xLs^3+CLR_xs^2+4L_xD^2-4L_xD+2LM^2+L_x)s+(4R_xD^2-4R_xD+R_x)}+ \\ +\frac{2R_xV_c-R_xV_{in}-4DR_xV_c+2DR_xV_c+2DR_xV_{in}}{CL_xLs^3+CLR_xs^2+(4L_xD^2-4L_xD+2LM^2+L_x)s+(4R_xD^2+4R_xD+R_x)} \tag{16}$$

tions. The output control transfer function (16) is provided as a third order transfer function.

The derived transfer function has a right half plane (RHP) zero that causes a non-minimum phase response.

As seen in Figure 4, a step change in shoot through duty ratio causes a high oscillation in capacitor voltage. Thus, ZSI output voltage would be oscillated, too. In order to prevent this unwanted oscillation a closed loop control is used.

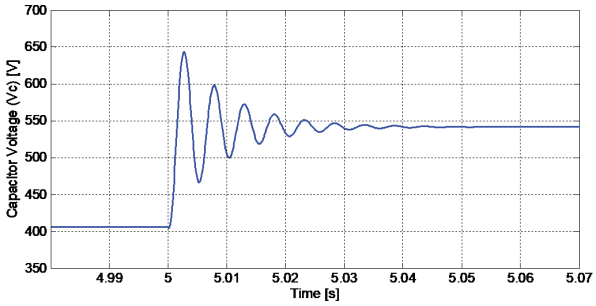


Figure 4: Vc oscillation during a step change in D

4 PI Control of ZSI

In the proposed method, shoot through duty cycle and modulation index are adjusted to track a reference sinusoidal output. As seen in Figure 5, just one control loop is utilized to control the variables M and D. PI controller is used to adjust shoot through duty ratio, and modulation index is calculated considering the shoot through duty ratio to eliminate an unnecessary control loop.

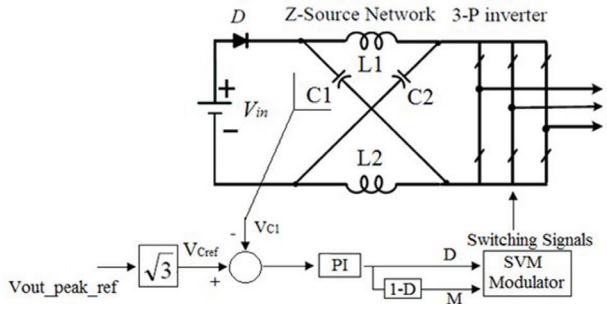


Figure 5: PI control schema

This is aimed to get high stability so only one control loop is utilized in the system. Inverter output voltage tracking is achieved with z source capacitor voltage reference and feedback. As seen in Figure 5, the M=1-D equation is used to adjust the modulation index considering dc line voltage. Therefore, an additional control loop is needed for the modulation index to be eliminated.

The circuit parameters used to investigate the performance of the proposed method are given in Table 2.

Table 2: ZSI Parameters

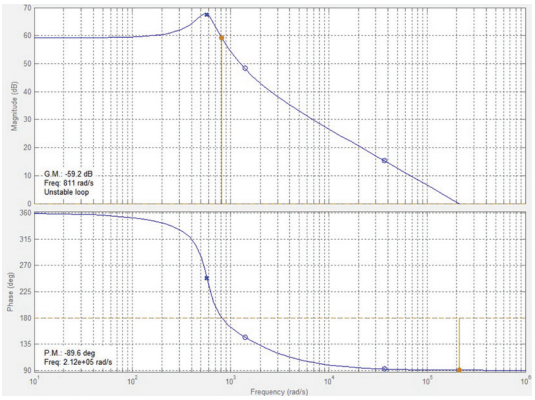
Circuit Parameter	Value
L1, L2	650 µH
C1, C2	500 µF
Input voltage	450 V
Switching Frequency	2 kHz
Load Resistance	12,5 Ω
Load Inductance	340 µH

Transfer function between shoot through duty ratio and Z source capacitor voltage is given in (17).

$$G_{VcD} = \frac{-2,346x10^{-5}s^2 - 0,7096s + 5625}{1,105x10^{-10}s^3 + 4,063x10^{-6}s^2 + 0,001106s + 6,125} \quad (17)$$

Compensated and uncompensated system bode diagrams can be seen in Figure 6.

(a)



(b)

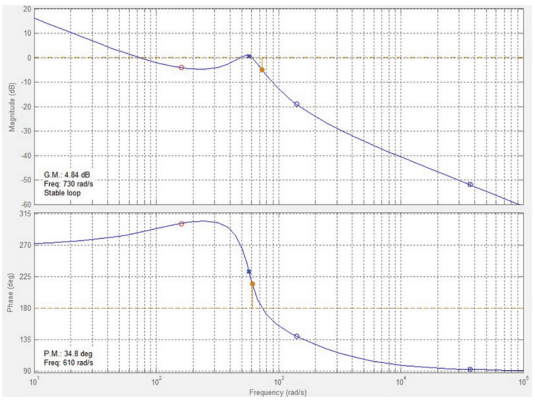


Figure 6: (a) Uncompensated and (b) compensated system bode diagram

5 Results

The proposed control method is tested with Matlab/Simulink simulations for two different power factor levels (PF = 1 and PF = 0,9) to investigate the performance of controller for different kinds of loads. The Simulink diagram of the control system can be seen in Figure 7.

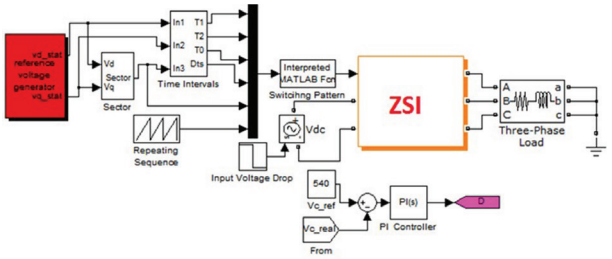


Figure 7: Simulink diagram of the control system

The proposed method is tested for two situations:

1. 11% input voltage drop (450 V to 400 V) at 0,5 seconds.
2. 75% load decrease at 0,4 seconds, and then a 75% load increase at 0,7 seconds.

The results are given in Figures 8-12. As seen in Figure 8, the proposed control method compensates overshoots and oscillations of the capacitor voltage, as given in Figure 4. Therefore, it contributes to the safety of the system.

Figure 9 (a) and (b) show that when the input voltage decreases, the shoot-through duty cycle D increases in order to obtain the desired ac output voltage, with a transient regulation. Figure 9 (c) and (d) show that when the load increases or decreases, the shoot-through duty cycle D respectively reduces or increases in order to obtain the desired ac output voltage. Moreover, as can be seen in Figure 10, dc line voltage is increased during input voltage step down so it is not kept constant, contrary to previous researches. Figure 11 shows the phase-A output voltage and current. Note that the current is scaled to ten times the actual value to be comparable with the voltage. Fig. 11(a) and (b) shows the output voltage and output current after the input voltage changes. Also, Figure 11(b) and (d) shows the ac voltage and current during the load variation.

The zoomed version of the inductor current and the dc line voltage are shown in Figure 12 to illustrate the impact of the shoot-through states. It can be observed from this figure that the inductor current is increasing during the shoot-through states, while dc line voltage is zero because of the short-circuit of the dc line.

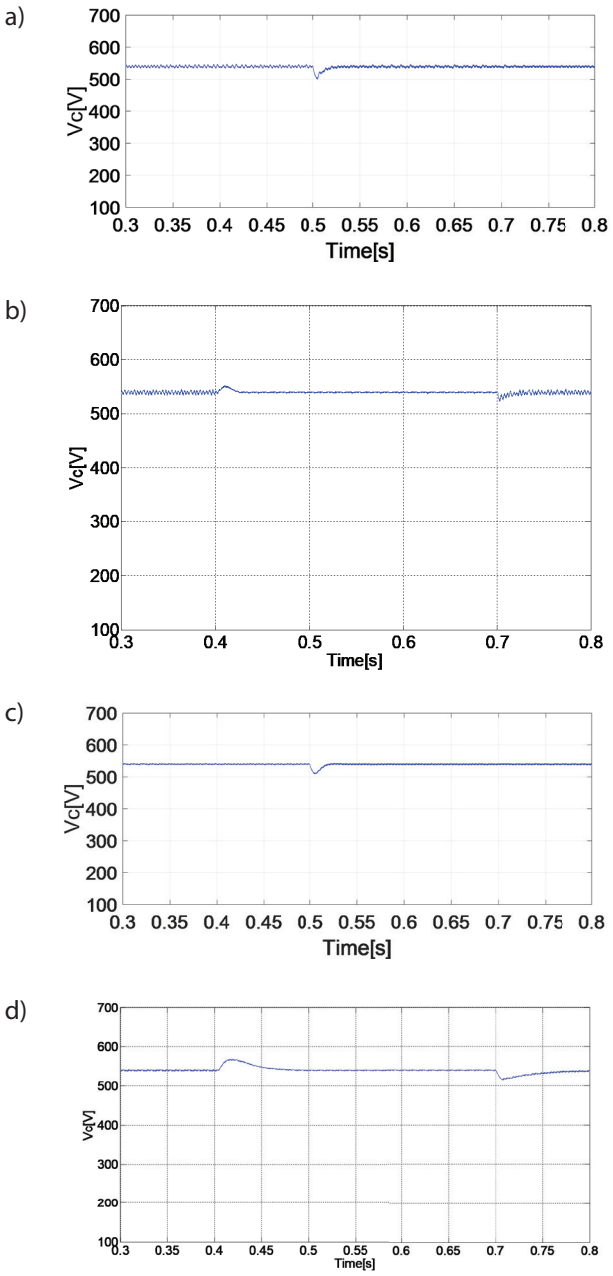


Figure 8: Capacitor voltage (Vc) response for a) 11% input voltage step down (PF=1); b) 75% load change (PF=1); c) 11% input voltage step down (PF=0,9); and d) 75% load change (PF=0,9)

As seen in the figures, the proposed PI control method has a good dynamic performance for both resistive and inductive loads. Control performance is nearly excellent for resistive load, and inverter output voltage becomes stable in half a period during a disturbance. Control performance is also very good for inductive load, and inverter output voltage becomes stable in the 2-3 period during a disturbance. Contrary to previous works, variable dc line voltage lets the ZSI work with a flexible

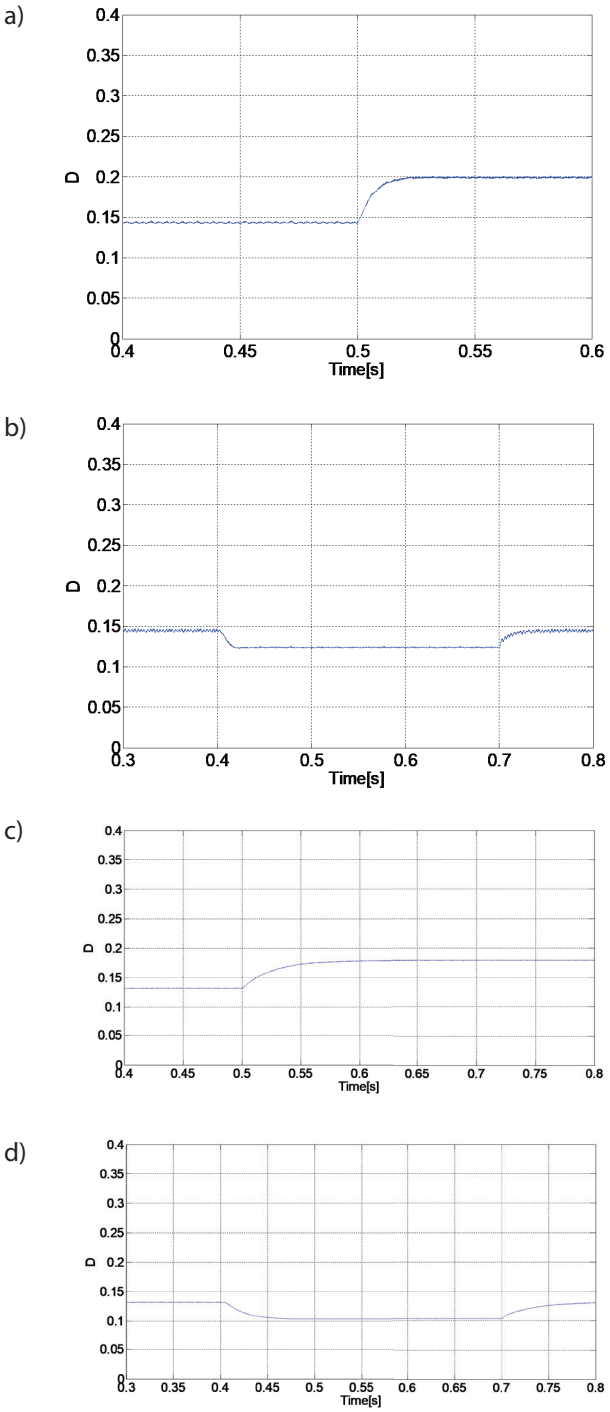


Figure 9: Shoot Through Duty Ratio (D) response for a) 11% input voltage step down (PF=1); b) 75% load change (PF=1); c) 11% input voltage step down (PF=0,9); and d) 75% load change (PF=0,9)

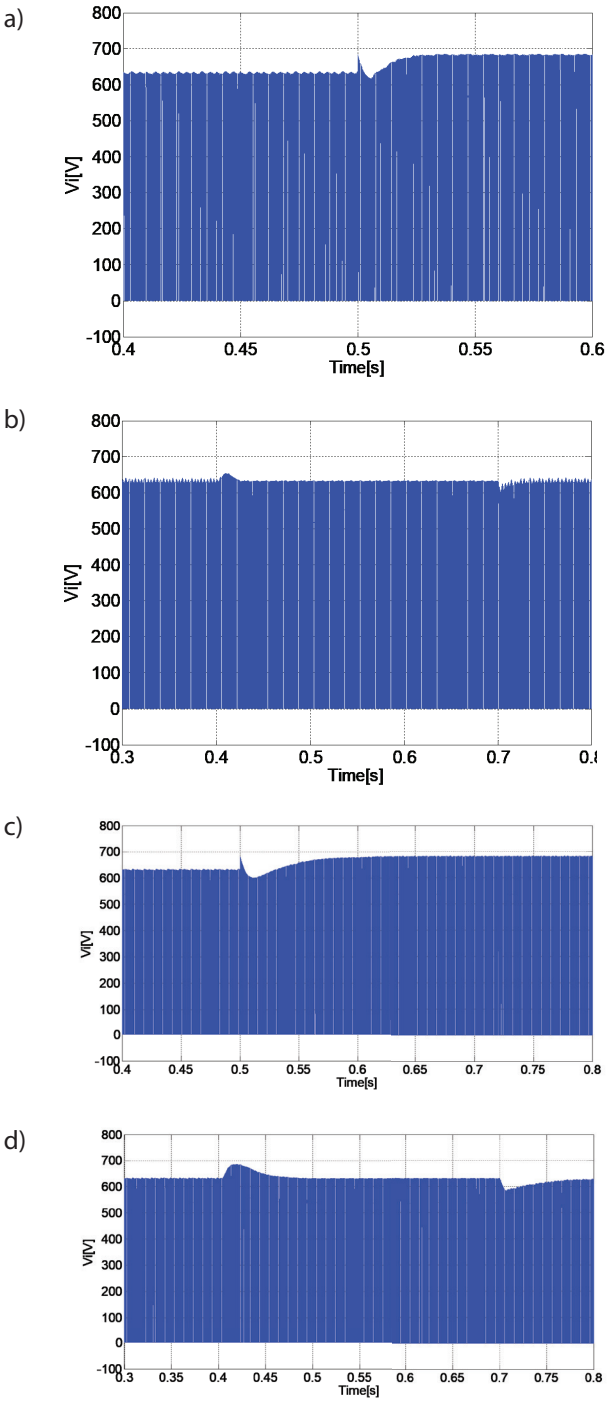


Figure 10: Dc line voltage (Vi) response for a) 11% input voltage step down (PF=1); b) 75% load change (PF=1); c) 11% input voltage step down (PF=0,9); and d) 75% load change (PF=0,9)

modulation index; therefore, ZSI becomes capable of working with lower voltage stress on switches. Flexible modulation index and SVM lets it work with minimum dc line voltage. Thus, voltage stress on switches is minimized.

6 Conclusion

In this research, a dynamic model of ZSI is given. It considers both modulation index (*M*) and shoot through

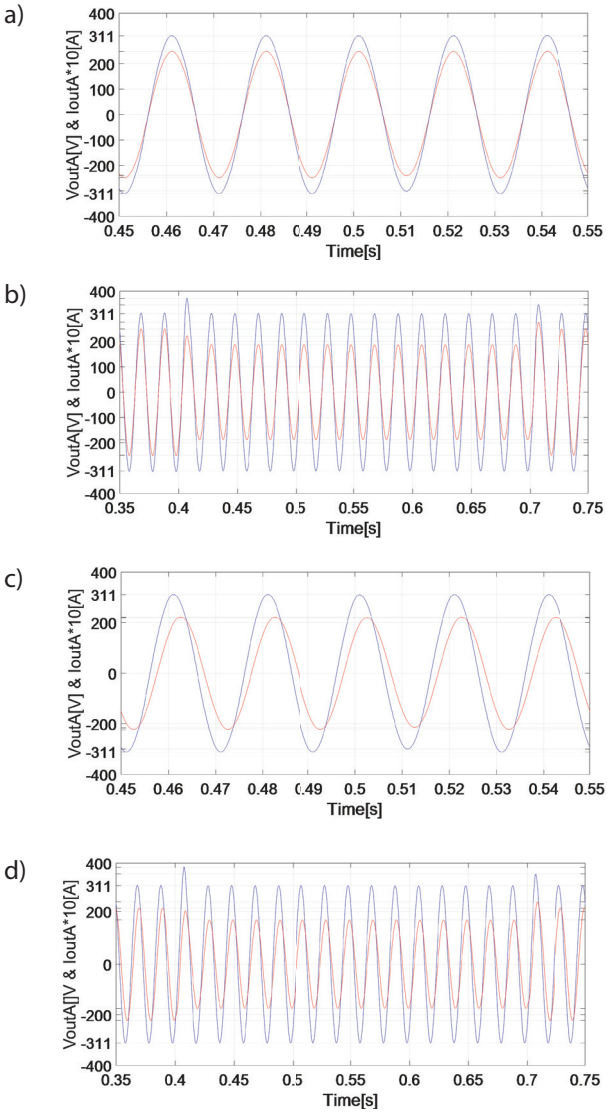


Figure 11: Phase-A output voltage (Vout) and Output current (Iout) response for a) 11% input voltage step down (PF=1); b) 75% load change (PF=1); c) 11% input voltage step down (PF=0,9); and d) 75% load change (PF=0,9)

duty ratio (*D*) as control variables; moreover, three operation states (active, zero, and shoot through) are considered for modelling to get a successful model. Considering this dynamic model, a control method based on distributed space vector modulation, which eliminates the drawbacks in the previous researches, is proposed for ZSI. In the proposed method, inverter output voltage is controlled via z source capacitor voltage feedback in order to achieve a high dynamic performance. Furthermore, the proposed method is investigated with a novel approach by considering different load power factor levels. Although the proposed method is effective for different loads, research results show that linear control methods are not enough for

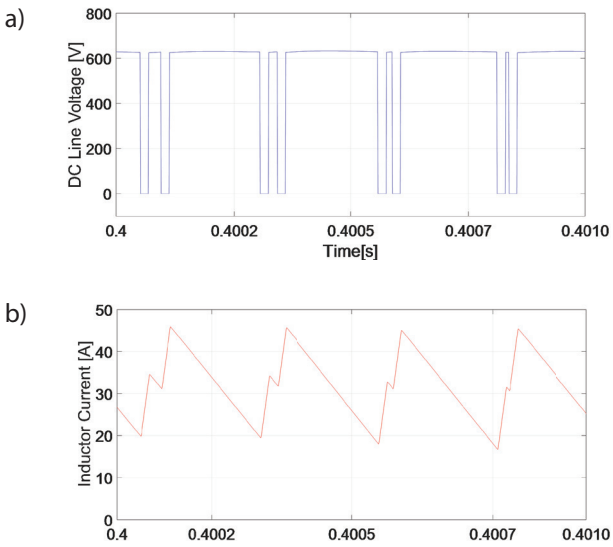


Figure 12: The zoomed version of a) the dc line voltage (V_i); b) the inductor current (I_i)

systems that have a load power factor range that is too wide. Moreover, very high input voltage oscillations make linear controllers useless because of the transfer function, which is obtained on an equilibrium point. Therefore, nonlinear control systems with a new approach shall be utilized for wide power factor ranges and wide input voltage oscillations variations.

7 Acknowledgement

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8 References

1. F. Z. Peng, "Z-Source Inverter", *IEEE Transactions On Industry Applications*, vol. 39, no. 2, pp. 504-510, 2003. [Online] Available: http://dx.doi.org/10.1109/TIA.2003.808920
2. Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. E. Town, "Impedance-Source Networks for Electric Power Conversion Part I: A Topological Review", *IEEE Transactions On Power Electronics*, vol. 30, no. 4, pp. 699-716, 2015. [Online] Available: http://dx.doi.org/10.1109/TPEL.2014.2313746
3. Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. E. Town, S. Yang, "Impedance-Source Networks for Electric Power Conversion Part II: Review of Control and Modulation Techniques", *IEEE Transactions On Power Electronics*, vol. 30, no. 4, pp.

1887-1906, 2015. [Online] Available: http://dx.doi.org/10.1109/TPEL.2014.2329859
4. M. M. Bajestan, M. A. Shamsimejad and D. A. Khaburi, "Derivation of AC small signal model and analysis of trans Z-source inverter", in *23rd Iranian Conference on Electrical Engineering*, Tehran, May 2015, pp. 1624-1629. [Online] Available: http://dx.doi.org/10.1109/IranianCEE.2015.7146479
5. A. Florescu, O. Stocklosa, M. Teodorescu, C. Radoi, D. A. Stoichescu, S. Rosu, "The advantages, limitations and disadvantages of Z-source inverter", in *IEEE International Semiconductor Conference (CAS)*, Sinaia, Oct. 2010, pp. 483-486. [Online] Available: http://dx.doi.org/10.1109/SMICND.2010.5650503
6. G. Sen, M. Elbuluk, "Voltage and current programmed modes in control of the Z-source converter", *IEEE Trans. Ind. Appl*., vol. 46, no. 2, pp. 680–686, 2010. [Online] Available: http://dx.doi.org/10.1109/TIA.2010.2040054
7. X. Ding, Z. Qian, S. Yang, B. Cui, F. Peng, "A PID control strategy for dc-link boost voltage in Z-source inverter", in *IEEE 22nd Annual Aplpied Power Electronics Conference*, Anaheim, USA, 2007, pp. 1145–1148. [Online] Available: http://dx.doi.org/10.1109/APEX.2007.357659
8. M. Shen,Q. Tang, F. Z. Peng, "Modeling and controller design of the Z-source inverter with inductive load", in *IEEE Power Electron. Spec. Conf.*, Orlando, 2007, pp. 1804–1809. [Online] Available: http://dx.doi.org/10.1109/PESC.2007.4342275
9. W. Mo, P. C. Loh, F. Blaabjerg, "Model predictive control for Z-source power converter", in *8th Int. Conf. on Power Electronics*, Jeju, 2011, pp. 3022–3028. [Online] Available: http://dx.doi.org/10.1109/ICPE.2011.5944809
10. M. Mosa, O. Ellabban, A. Kouzou, A. R. Haitham, J. Rodriguez, "Model Predictive Control Applied for Quasi-Z-Source Inverter", in *Applied Power Electronics Conference and Exposition*, Long Beach, 2013, pp. 165-169. [Online] Available: http://dx.doi.org/10.1109/APEC.2013.6520202.
11. C. J. Gajanayake, D. M. Vilathgamuwa, P. C. Loh, "Development of a Comprehensive Model and a Multiloop Controller for Z–Source Inverter DG Systems", *IEEE Trans. Ind. Appl*., vol. 54, no.4, pp. 2352-2359, 2007. [Online] Available: http://dx.doi.org/10.1109/TIE.2007.894772
12. O. Ellabban, J .V. Mierlo, P. Lataire, "A DSP-based dual-loop peak DC-link voltage control strategy of the Z-source inverter", *IEEE Transactions on Power Electronics*, vol. 27, no. 9, pp. 4088-4097, 2012. [Online] Available: http://dx.doi.org/10.1109/TPEL.2012.2189588
13. Y. Liu, B. Ge, H. Abu-Rub, F. Z. Peng, "Control System Design of Battery-Assisted Quasi-Z-Source Inverter for Grid-Tie Photovoltaic Power Generation", *IEEE Transactions On Sustainable Energy*, vol. 4, no. 4, pp. 994-1001, 2013. [Online] Available: http://dx.doi.org/10.1109/TSTE.2013.2263202
14. S. Yang, X. Ding, F. Zhang, F. Z. Peng, Z. Qian, "Unified control technique for Z-source inverter", in *IEEE Power Electron. Spec. Conf*., Rhodes, 2008, pp. 3236–3242. [Online] Available: http://dx.doi.org/10.1109/PESC.2008.4592452
15. Ö. Girgin, V. Erginer, M. H. Sarul, "Analysis and Comparison of Control Methods of Z-Source Inverters Used in Photovoltaic Systems", in *Proceedings of the World Congress on Electrical Engineering and Computer Systems and Science (EECSS 2015)*, Barcelona, July 2015, pp. 148/1-148/11. [Online] Available: http://avestia.com/EECSS2015_Proceedings/files/papers/EEE148.pdf
16. V. Erginer, M. H. Sarul, "A novel control method for Z-source inverters used in photovoltaic systems", in *the 7th IET International Conference on Power Electronics, Machines and Drives (PEMD)*, Manchester, April 2014, pp. 1-5. [Online] Available: http://dx.doi.org/10.1049/cp.2014.0250
17. M. Shen, F. Z. Peng, "Operation Modes and Characteristics of the Z-Source Inverter With Small Inductance or Low Power Factor", *IEEE Transactions On Industrial Electronics*, vol. 55, no. 1, pp. 89-96, 2008. [Online] Available: http://dx.doi.org/10.1109/TIE.2007.909063
18. V. Erginer, M. H. Sarul, "A novel reduced leakage current modulation technique for Z-source inverter used in photovoltaic systems", *IET Power Electronics*, vol. 7, no. 3, pp. 496-502, 2014. [Online] Available: http://dx.doi.org/10.1049/iet-pel.2013.0187
19. P. C. Loh, D. M. Vilathgamuwa, C. J. Gajanayake, Y. R. Lim, C. W. Teo, "Transient modeling and analysis of pulse-width modulated Zsource inverter", *IEEE Trans. Power Electron*., vol. 22, no. 2, pp. 498–507, 2007. [Online] Available: http://dx.doi.org/10.1109/TPEL.2006.889929
20. J. Liu, J. Hu, L. Xu, "Dynamic modelling and analysis of Z source converter-derivation of AC small signal model and design-oriented analysis", *IEEE Trans. Power Electron*., vol. 22, no. 5, pp. 1786–1796, 2007. [Online] Available: http://dx.doi.org/10.1109/TPEL.2007.904219
21. M. Forouzesh, Y. P. Siwakoti, F. Blaabjerg, S. Hasanpour, "Small-Signal Modeling and Comprehensive Analysis of Magnetically Coupled Impedance-Source Converters", *IEEE Transactions On Power Electronics*, vol. 31, no. 11, pp. 7621-7641, 2016. [Online] Available: http://dx.doi.org/10.1109/TPEL.2016.2553849

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Digital implementation of a demodulator for HF RFID reader device

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Abstract: This paper presents a demodulator for high frequency radio frequency identification (HF RFID) signals based on the Costas loop [1]. A description is presented of how correlation between two signals can be simplified in terms of the operations involved and implemented using a digital Costas loop [2, 3]. After carrier direct down conversion and bandpass filtering, the proposed demodulator is used to demodulate the subcarrier signal. A brief description is given of the signal characteristics of HF RFID signals at a carrier frequency of f_c = 13.56 MHz and the operation of the subcarrier demodulator. Packet error rate (PER) measurement results are presented for protocols ISO/IEC 14443 type A and type B at a bitrate fc/128 (approximately 106 kbit/s), FeliCa at fc/64 (approximately 212 kbit/s), and ISO/IEC 15693 at fc/512 (approximately 26.48 kbit/s). A comparison between the measured PER results and the theoretical BPSK PER limit is presented. Also shown is the comparison with a HF RFID reader integrated circuit ST25R3911 [4], where an almost 11 dB improvement in PER performance for ISO/IEC 14443 type B fc/128 was achieved.

Keywords: HF RFID reader; digital demodulator; correlation; Costas loop; packet error rate

Digitalna implementacija demodulatorja za HF RFID izpraševalnik

Izvleček: V tem članku predstavimo demodulator za visoko frekvenčno radiofrekvenčno identifikacijo (HF RFID) na osnovi Costas-ove zanke [1]. Opišemo poenostavitev korelacije med dvema signaloma na osnovi vpletenih operacij in implementacijo z uporabo Costas-ove zanke [2, 3]. Po direktnemu mešanju nosilca navzdol in pasovno prepustnem filtriranju uporabimo predstavljen demodulator za demodulacijo podnosilnega signala. Po kratkem pregledu karakteristik signalov na področju HF RFID pri nosilni frekvenci f_c = 13,56 MHz, opišemo delovanje demodulatorja in njegovo delovanje preizkusimo z meritvami pogostosti paketnih napak (angl. packet error rate ali PER). Predstavimo rezultate PER meritev za protokole ISO/IEC 14443 tip A in B pri podatkovni hitrosti fc/128 (približno 106 kbit/s), FeliCa pri hitrosti fc/64 (približno 212 kbit/s) in ISO/IEC 15693 pri hitrosti fc/512 (približno 26,48 kbit/s). Naredimo primerjavo med izmerjenimi vrednostmi in teoretičnimi mejami za kodiranje bitov, ki se uporablja v naštetih protokolih. Prav tako za protokol ISO/IEC 14443 tip B podatkovne hitrosti fc/128 naredimo primerjavo z integriranim vezjem HF RFID izpraševalnika ST25R3911 [4], kjer smo dosegli skoraj 11 dB izboljšavo v PER zmogljivostih.

Ključne besede: HF RFID izpraševalnik; digitalni demodulator; korelacija; Costas-ova zanka; pogostost paketnih napak

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1 Introduction

In HF RFID a reader and a contactless card or tag form a master/slave communication setup. The reader generates the magnetic field required to both power and communicate with the tag. The tag extracts power from its antenna to supply itself and uses antenna load modulation to answer reader commands. The tag modulates the carrier signal with a subcarrier signal, where the subcarrier frequency is defined as the carrier frequency divided by a whole number (e.g. 16, 32 or 64). The changes in the load of the tag antenna can be seen by the reader as either changes in carrier field amplitude or phase or both, depending on distance, orientation, and other parameters of the reader-tag antenna system (resonance frequencies, quality factors, etc.).

In the reader receiver the carrier is down converted using direct down conversion. After amplification and bandpass filtering to remove DC and higher order components of conversion, only the frequency band which holds the subcarrier signal remains. Bit information is encoded in the phase or the amplitude of the subcar-

rier signal, so a reliable means of extracting the information is required.

In the field of HF RFID, Y.-H. Kim, M.-W. Seo, Y.-C. Choi, and H.-J. Yoo [5] have proposed and implemented a receiver architecture where a comparator with selectable detection threshold is used to digitize the subcarrier signal after carrier direct down conversion and bandpass filtering. The burden of bit recognition thus falls with the decoding circuit following the comparator. This implementation is simple and effective, but suffers from rapidly degrading noise performance. In addition, any damage to the signal by external interferers or effects of the reader-tag antenna system can cause the comparators to output dubious pulses that are hard to interpret correctly by the decoder. Bit duration and subcarrier presence detection can also suffer as a result.

H. Min, Y. Liu, and C. Huang [6] have proposed digital correlation based receivers for RFID, but focused on the ultra-high frequency (UHF) RFID domain (from 860 MHz to 960 MHz). Their implementation consumed a large amount of hardware (12 parallel correlator banks) to tackle the problem of large frequency deviations present in UHF tag replies, due to the nature of tag operation at such frequencies**.**

In the HF RFID domain, C. Angerer [7] presented a receiver structure that used an integrator as a simple rectangular pulse correlator and algorithm for synchronization. While their results show good performance, their work is based on the EPC global HF standard.

The demodulators in the listed papers are based on classical implementations of correlators as a finite impulse response or FIR filter, where coefficients represent the signal being searched for.

This paper presents a demodulator based on the Costas loop that uses simplified correlation to extract phase and amplitude information from the subcarrier signal. The demodulator was implemented in the digital domain so testing could be done on a field-programmable gate array (FPGA) development board. The output of the demodulator is a bit stream that holds information about the subcarrier phase or amplitude. An additional output is a signal indicating the start of a data packet or presence of signal collisions due to multiple tags responding at the same time. The subcarrier demodulator performs simplified correlation to extract bit information from the phase or amplitude of the subcarrier. An advantage of the demodulator presented in this work over classical implementations using multiplier-accumulators is that reception of HF RFID signals can be made robust against variations in subcarrier frequency or phase (for example due to active tag transmission). Additional benefits come from the ability of the architecture of the demodulator to support different data rates with the same hardware and easy scalability in terms of desired performance. A brief comment on this is at the end of section 3.

First, a brief overview of the signal characteristics in the HF RFID field is presented in section 2. Next, the demodulator design and operation are described in section 3. The hardware implementation and measurement setup are presented in section 4. In section 5, the theoretical reception limits for HF RFID protocols are defined. The packet error rate measurement results for protocols defined in standards ISO/IEC 14443, ISO/IEC 15693 and JIS X – 6139 (FeliCa) at their base data rates are presented in section 6.

2 Signal characteristics

Standards ISO/IEC 14443, ISO/IEC 15693 and JIS X – 6139 (FeliCa) describe protocols used in HF RFID and NFC (Near Field Communications – a rapidly growing subdomain of HF RFID, popular in mobile devices). The protocols share similarities with each other, which can be used in the design of the demodulator.

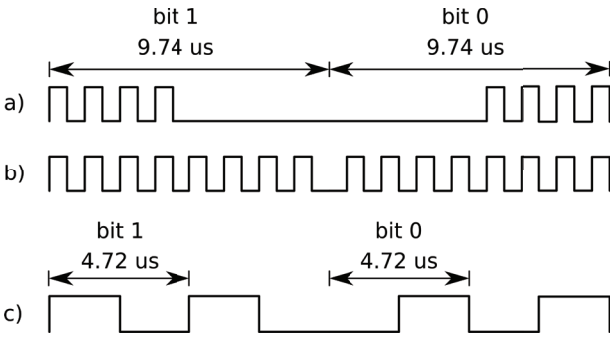

Figure 1: Bit coding of HF RFID protocols

Figure 1 shows the bit coding for a) ISO/IEC 14443 type A $f_c/128$ and b) ISO/IEC 14443 type B $f_c/128$, where the subcarrier frequency is 847.5 kHz. At the bottom of figure 1, c) shows FeliCa $f_c/64$, where the subcarrier frequency is 211.875 kHz. Not shown is the bit coding for ISO/IEC 15693 $f_c/512$, which uses Manchester coded subcarrier, like in a), but with 8 periods of 423.75 kHz subcarrier followed by 8 periods of no subcarrier for bit 1, for a total bit length of approximately 37.76 μs. One can notice that there are two types of coding schemes, Manchester and BPSK. The demodulator design is accordingly divided into two parts: reception of BPSK coded subcarrier and reception of Manchester coded subcarrier. Both use the same hardware, but with different settings.

3 Demodulator design and operation

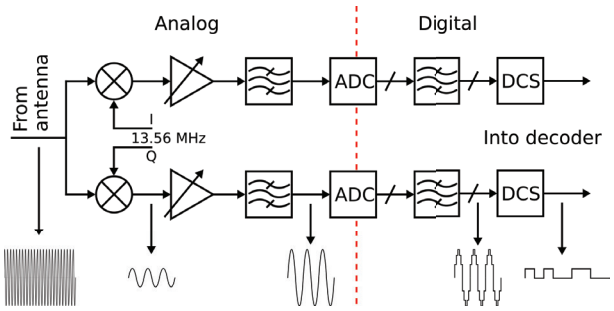

Figure 2: Block schematic of a HF RFID reader receiver

Figure 2 shows the reception path of a HF RFID reader. The carrier signal from the antenna is first directly down converted. The conversion result is then amplified and bandpass filtered to remove the DC component and to remove high frequency components. The end result are I and Q channels with a subcarrier signal, ready to be converted to digital signals by analog to digital converters (ADCs). The digital signals are further bandpass filtered to remove unwanted spectral images and to more accurately define the bandwidth (BW). At this stage in the reception chain, there is a digitized subcarrier signal with a bandwidth of twice the data rate, in case of BPSK, or four times the data rate, in case of Manchester code. The proposed demodulator (digital correlation system or DCS) is used at this stage to convert the subcarrier signal into a baseband signal, to provide filtering (as ideal correlation does), and to perform symbol and packet start recognition.

$$(f * u)(\tau) = \int_{-\infty}^{\infty} f^{*}(\tau)\, u(t+\tau)\, dt \qquad (1)$$

Equation 1 describes correlation between two signals, where *f* is a signal in which the pattern *u* is searched for. In the above equation, *f** is the complex conjugate of signal *f*. In our case, *f** is the digitized subcarrier signal that is compared to a known sample *u*. A local subcarrier clock can be used as signal *u*. In this way the subcarrier signal, or more accurately its frequency or phase, can be compared with the local subcarrier clock's frequency or phase. The operation of correlation can be divided into three main parts: multiplication, time or phase adjustment, and integration or averaging.

The subcarrier signal is mixed with two local subcarrier clocks in 90 degree phase relation between them, effectively performing direct quadrature conversion. The I channel subcarrier signal is thus split into I and Q subchannel baseband signals. The same operation is performed on the Q channel subcarrier signal. Because the clocks are single-bit signals and the digitized subcarrier is a multi-bit signal, the operation of multiplication can be reduced to an operation of inversion and addition (sign change in a number represented in two's complement representation). When the clock is '1' the subcarrier amplitude is unchanged and when the clock is '0' the sign of the subcarrier amplitude is inverted.

The phase of the I sub-channel clock is corrected to match the phase of the subcarrier signal. Naturally, the phase relationship between I and Q sub-channel clocks is kept constant. When phase lock between the subcarrier signal and I sub-channel clock is achieved, mixing is effectively reduced to full wave rectification of the subcarrier signal. The I sub-channel holds all the information about the phase of the subcarrier, while the combination of I and Q sub-channels determines in which way to correct the phase. To remove noise and higher order components of mixing, the signal is filtered with both a finite impulse response (FIR) and infinite impulse response (IIR) digital filters. Decimation can be employed before the IIR filter to reduce its size. The FIR filter removes the exact higher order frequencies of mixing, while the IIR filter removes noise and provides a frequency characteristic that closely follows the spectrum of the data in the base band. In this setup, classical correlation is replaced by mixing, phase correction and filtering (a Costas loop). The added benefit over classical correlation is being able to control the phase and frequency of the local subcarrier clock (signal *u*) and thus use the same structure to demodulate signals with varying subcarrier phase or frequency throughout the data packet.

Another advantage is the ability to be able to freely set the cutoff frequency of the IIR low pass filters to match the spectrum of the data packet without the need to change the structure of the demodulator. ISO/IEC 14443 type A and B high bitrates have identical bit coding (BPSK coded $f_c/16$ or 847.5 kHz subcarrier), but slightly different data packet structure. At $f_c/64$ kbit/s 4 subcarrier periods are used to represent a bit, 2 subcarrier periods are used at $f_c/32$ kbit/s and 1 subcarrier period at $f_c/16$ kbit/s. The spectrum of the input subcarrier signal changes with data rate, so the cutoff frequency of the IIR filters can be adjusted accordingly while using the same topology and hardware.

The disadvantage is the need for a pilot tone in the subcarrier signal, so the loop has time to achieve phase lock. However, all HF RFID BPSK protocols have long pilot tones (>20 subcarrier periods).

Figure 3 shows the basic structure of the proposed subcarrier demodulator. The symbol recognition algorithm (SRA) block tracks the demodulator output signal and performs symbol recognition and start of packet detection for BPSK coded protocols or collision detec-

tion for Manchester coded protocols. The numerically controlled phase (NCP) block controls the phase of the I and Q subcarrier clocks. Only the signs of the multi-bit signals from the filter outputs are used, as only one phase correction of fixed size is possible per subcarrier period. As such, the time in subcarrier periods the loop takes to achieve phase lock (or approximate phase lock), depends on the phase correction resolution. In the case of ISO/IEC 14443 type B f_c/128 kbit/s, a main clock frequency of f_c=13.56 MHz is used. The subcarrier frequency is f_c/16 or 847.5 kHz. This means that there are 16 samples for every subcarrier period. The size of the phase correction is one sample, or 1/16 of the subcarrier period, which means that the phase corrections are coarse, but sufficient for successful demodulation of the subcarrier signal. Ideally, it takes 4 phase corrections at most to align the I subcarrier clock phase to the input subcarrier phase. With excessive noise it can take longer. Phase corrections are disabled when a phase change is occurring on the subcarrier signal so a false phase correction does not occur.

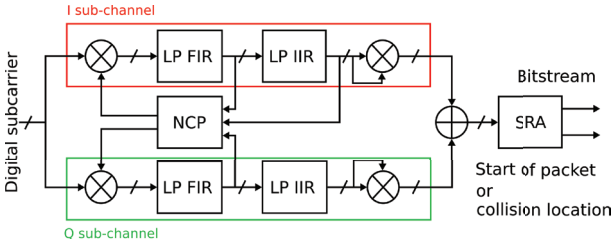

Figure 3: Block diagram of the proposed demodulator

The architecture can easily be scaled if size is a limitation, at the cost of performance. For example, the area of the IIR low pass filters can be reduced by reducing the filter order or increasing the ratio between the filter sampling frequency and cutoff frequency. The cost for this is worse noise attenuation and, as a result, worse noise performance.

4 Hardware implementation

The demodulator was implemented on a field-programmable gate array (FPGA) development board for debugging and testing purposes. Since only the digital part of the receiver could be implemented on a FPGA, the analog front end (AFE) and ADCs were implemented with separate ICs, as shown in figure 4. For the AFE, the reader IC ST25R3911 was used. The IC was configured into a test mode, where the AFE outputs were available on its output pins. ADCs were used to sample the AFE outputs and relay their data to the FPGA. This way, a direct comparison between the proposed demodulator and ST25R3911 was possible.

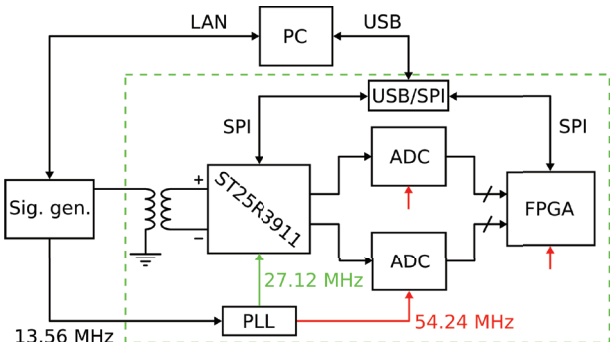

Figure 4: Measurement setup block diagram

5 Packet error rate theoretical limits

To have an absolute benchmark to compare with measurement results a theoretical limit of the bit error rate (BER) or packet error rate (PER) for HF RFID protocols is needed. We derive the theoretical limit from [8].

$$E_b = V_{Srms}^2 T_b \tag{2}$$

$$N_0 = \frac{V_{Nrms}^2}{BW} \tag{3}$$

$$BER_{BPSK} = \frac{1}{2} erfc\left(\sqrt{\frac{E_b}{N_0}}\right) \tag{4}$$

$$PER = 1 - (1 - BER)^l \tag{5}$$

Equation 2 describes the energy per bit E_b in relation to the signal *rms* voltage V_{Srms} and the bit duration T_b. Equation 3 describes the noise power spectral density N_0 in relation to the noise *rms* voltage V_{Nrms} and the bandwidth of the noise *BW*. Equation 4 shows the ideal performance of BPSK coded protocols, such as ISO/IEC 14443 type B. Equation 5 shows the relation between the bit error rate and packet error rate for a given packet length of *l* bits. Bit length *l* needs to hold the number of all bits that need to be received successfully in order for the packet to be received successfully, as standard HF RFID data packets do not include error correcting codes. Special symbols, start, stop, parity, and CRC bits all need to be included. The longer the data packet, the less likely it will be received correctly in its entirety in a noisy environment.

This limit only takes into account the errors that arise from bit errors in the presence of noise, but not the errors that occur when packet start or end are not detected due to noise. However, the limit is very useful since it represents an absolute marker unrelated to demodulator architecture, against which demodulator

performance can be compared. The smaller the difference between the measured and the theoretical limit, the better the performance of the demodulator is.

A similar formula can be written for Manchester coded protocols:

$$BER_{Manchester} = \frac{1}{2} erfc\left(\sqrt{\frac{E_b}{8N_0}}\right) \quad (6)$$

Equation 6 describes the ideal performance of Manchester coded protocols, such as ISO/IEC 14443 type A for a data rate of f_c/128 kbit/s. Compared to equation 4, we have a factor of 8 present in the denominator of the fraction inside the square root. This factor is the result of differences between Manchester code and BPSK. It stems from the need to correctly recognize both bit halves and a smaller distance between bit symbols in the constellation diagram for Manchester coded signals. Interestingly, ISO/IEC 14443 type A f_c/128 kbit/s has the same theoretical PER as type A f_c/16 kbit/s (type A data rates larger than f_c/128 kbit/s are BPSK coded), which demonstrates the superior robustness of BPSK compared to Manchester code with regards to noise.

Table 1 shows the E_b/N_0 (energy per bit to noise power spectral density ratio or SNR per bit) values in dB for 10 % PER for all protocols and data rates for data packets 10 bytes long (8 data and 2 CRC bytes).

Table 1: Theoretical 10 % PER limits for a 10 byte long data packet for various HF RFID protocols and data rates.

Protocol	Data rate [kbit/s]	10 % PER Eb/N0 [dB]
ISO/IEC 14443 type A*	fc/128	12.69
ISO/IEC 14443 type A	fc/64	6.67
ISO/IEC 14443 type A	fc/32	6.67
ISO/IEC 14443 type A	fc/16	6.67
ISO/IEC 14443 type B	fc/128	6.91
ISO/IEC 14443 type B	fc/64	6.91
ISO/IEC 14443 type B	fc/32	6.91
ISO/IEC 14443 type B	fc/16	6.91
ISO/IEC 15693*	fc/2048	12.68
ISO/IEC 15693*	fc/512	12.68
FeliCa	fc/64	6.78
FeliCa	fc/32	6.78

When comparing different protocols from table 1, one can observe the difference in E_b/N_0 the data structure and bit coding make. Protocols marked with an asterisk * have Manchester coded bits, whereas the rest are BPSK coded. The difference between Manchester code and BPSK result is 6.02 dB, as can be seen when comparing ISO/IEC 14443 type A f_c/128 kbit/s and f_c/64 kbit/s (same data structure, different bit coding).

6 Measurement results

The testing of the performance of the demodulator was done with PER measurements. For each SNR value a number of noisy packets were sent and the success rate of reception measured.

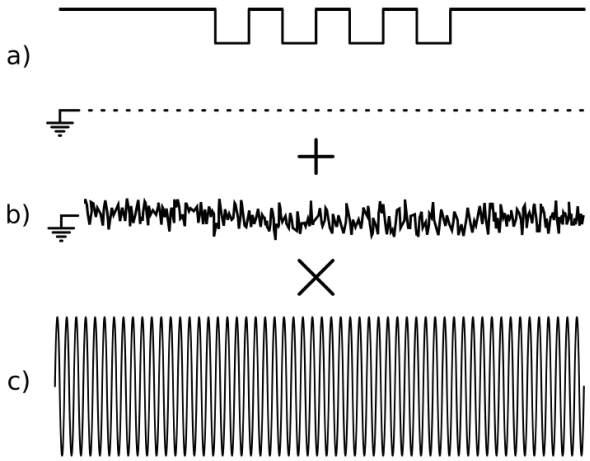

Figure 5: Sketch of the test pattern generation procedure.

Figure 5 shows the three steps in test pattern generation. First, a modulation signal with the correct packet structure was created, as shown in a). Then, band limited additive white Gaussian noise (AWGN) was added, as shown in b). The noise BW was 5 MHz while N_0 was determined by the desired SNR value (equation 3). The noise BW was selected so it encompassed the entire BW of the data spectrum and usable frequency range of the AFE. The noisy modulation signal was then scaled and used to modulate a 13.56 MHz carrier, as shown in c). The test pattern generation was done in a Python script and uploaded to the signal generator to be fed into the device under test.

An external clock source supplied a clock signal synchronous to the carrier field. The gain of the AFE was reduced to avoid adding more noise to the packets by any other noise sources (thermal and 1/f noise in the receiver, oscillator phase noise in the waveform generator). This was done to ensure the artificially generated noise was indeed the dominant noise source. The modulation signal was appropriately scaled, so that the signal levels at the ADC inputs were at nominal levels. Each packet had length of 8 data bytes, 2 cyclic redundancy

check (CRC) bytes, and packet structure as defined in ISO/IEC 14443 for type B at a data rate of f_c/128 kbit/s. Two sets of measurements were done, first on the FPGA development board with the proposed demodulator and later on the HF RFID reader IC ST25R3911.

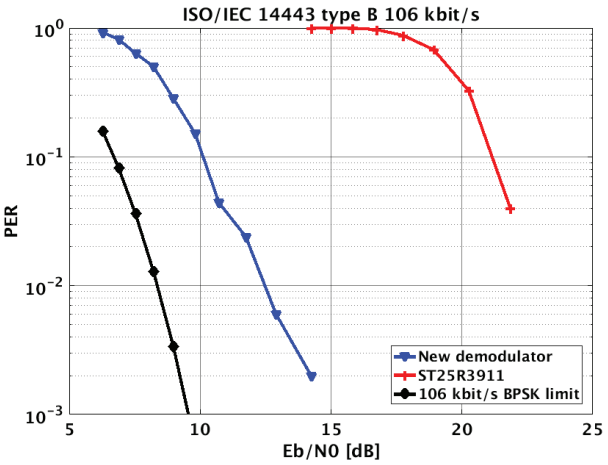

Figure 6: Packet error rate measurement results and the theoretical 106 kbit/s BPSK PER limit.

Figure 6 shows the PER versus the E_b/N_0 value in dB for both sets of measurements. For each data point 500 packets were sent. Figure 6 also shows a 3.1 dB difference between the theoretical limit and measured results at the 0.1 PER mark (10 % fail rate). Also shown is an almost 11 dB improvement compared to the HF RFID reader IC ST25R3911.

Similar results were obtained with other protocols at their base data rates as shown in table 2.

Table 2: PER measurement comparison for various protocols.

Protocol	Data rate [kbit/s]	10 % PER Eb/N0 [dB]	Diff. to limit [dB]
ISO/IEC 14443 type A	fc/128	15.7	3.0
ISO/IEC 14443 type B	fc/128	10.2	3.1
ISO/IEC 15693	fc/512	19.1	6.4
FeliCa	fc/64	9.2	2.4

7 Conclusion

This paper presented a HF RFID demodulator based on a Costas loop for reception of protocols defined in ISO/IEC 14443, ISO/IEC 15693 and JIS X 6139. Demodulator design and operation were described. PER measurement results for ISO/IEC 14443 type A and B f_c/128 kbit/s, FeliCa f_c/64 kbit/s, and ISO/IEC 15693 single subcarrier f_c/512 kbit/s along with theoretical limits were presented. PER measurement results for ISO/IEC 14443 type B f_c/128 kbit/s showed good performance in noisy environment compared to theoretical f_c/128 kbit/s BPSK PER limit, where a 3.1 dB difference was observed. The difference between the theoretical limit and measurement results can be explained by the fact that the theoretical limit does not include the probability of errors in packet start or end detection, but only the probability of bit errors. Improvements in demodulator design reduce this difference. The theoretical limit serves as an absolute marker against which demodulator performance can be compared. Additionally, an almost 11 dB improvement was observed compared to HF RFID reader ST25R3911 for protocol ISO/IEC 14443 type B f_c/128 kbit/s.

8 References

1. J. Costas, "Synchronous Communications," *Proceedings of the IEEE*, vol. 44, p. 1713-1718, 1956.
2. B. Shamla, K. G. Gayathri Devi, "Design and Implementation of Costas loop for BPSK Demodulator," *India Conference (INDICON), 2012 Annual IEEE*, Kochi, 2012.
3. P. Shachi, Rahul Mishra, Ravi Kumar Jatoth, "Coherent BPSK Demodulator using Costas Loop and Early-Late Gate Synchronizer," *2013 Fourth International Conference on Computing, Communications and Networking Technologies (ICCCNT)*, 2013.
4. STMicroelectronics, "ST25R3911 NFC/HF Reader IC." Available: http://www.st.com/en/nfc/st25r3911.html.
5. Y.-H. Kim, M.-W. Seo, Y.-C. Choi, H.-J. Yoo, "A 13.56 MHz Receiver SoC for Multi-Standard RFID Reader," *Electron Devices and Solid-State Circuits*, 2008.
6. H. Min, Y. Liu, C. Huang, "Digital Correlation Demodulator Design for RFID Reader Receiver," *Wireless Communications and Networking Conference*, 2007.
7. C. Angerer, "A Digital Receiver Architecture for RFID Readers," Symposium on Industrial Embedded Systems, 2008.
8. John G. Proakis, M. Salehi, *Digital Communications,* Fifth edition. McGraw-Hill, 2008.

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Design of Fault-Tolerant Reversible Floating Point Division

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Abstract: In semiconductor industries power dissipation and the size of the computational devices are playing a major role. Size of a single transistor may limit the scaling of semiconductor devices. In turn, an alternative technology is needed for computational devices; one such technology is Reversible Logic. In this paper, a new set of reversible gates named as KMD Gates are proposed, they are capable of producing many logical functions compared to the conventionally available reversible gates. The proposed gates satisfy the reversibility and universality properties of reversible logic. In addition, these gates are having parity preservation, so they are fault-tolerant. A n-bit fault-tolerant reversible floating point division unit (FTRFPD) is designed in IEEE 754 single precision standard using the proposed fault-tolerant KMD reversible gates. This FTRFPD has parallel adder, latch, multiplexer, shift register, rounding and normalization register. All the functional blocks are fault-tolerant in nature as they are, they are constructed from the Fault-Tolerant Gates. The FTRFPD is capable of dividing two numbers using the non-restoring algorithm. Quantum Cellular Automata (QCA) is incorporated for validating the functionality of the reversible logic gates and division unit. The QCA based simulation results confirm that the designed unit is having reduction in Quantum Cost by 9.85%, in Delay by 29.63% and in Number of Gates by 33.54 % over the existing designs.

Keywords: Reversible Logic; Quantum Cost; Delay.

Načrtovanje proti napakam odpornega reverznega deljenja s plavajočo

Izvleček: Poraba moči in velikost računskih elementov igrajo pomembno vlogo v polprevodniški industriji. Velikost posameznega tranzistorja lahko omejuje velikost poprevodniške naprave, zaradi česar je potrebna drugačna tehnologija za računske elemente, kot na primer reverzibilna logika. Članek predlaga nov set reverzibilnih vrat kot KMD vrat, ki omogočajo več logičnih operacij kot klasična vrata. Vrata zagotavljajo reverzibilnost in univerzalnost reverzibilne logike. Poleg tega predlagana vrata ohranjajo polariteto, kar pomeni, da so odporna proti napakam. Enota za deljenje s plavajočo vejico (FTRFPD) je načrtana v IEEE 785 standardu z enojno natančnostjo z uporabo predlaganih KMD vrat. FTEDPD ima paralelni množilnik, zapah, miltiplekser, pomikalni regiter ter zaokroževalni in narmalizacijski register. Vsi funkcijski blogi so odporni na napake saj vrebujejo proti napakam odporna vrata. FTEDPD lahko deli dve števili brez algoritma obnovitve. Za validacijo vrat in deljenja je uporabljen QCA (Quantum Cellular Automata). QCA simulacije potrjujejo zmanjšanje stoška kvanta za 9.85%, zakasnitve za 29.63% in števila vrat za 33.54% glede na obstoječe dizajne.

Ključne besede: reverzibilna logika; strošek kvanta; zakasnitev.

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1 Introduction

In modern VLSI technology, size and power dissipation are the major challenges to computational devices. The size reduction of a transistor scaling has its own physical limits. Also, smaller transistors dissipate more power, and it has other second-order effects, which affect the functionality of the circuits. Landauer has proved that the irreversible computing devices dissipates heat energy in the order of KTln2 Joules for the loss of a single bit of information (where K is Boltzmann's Constant = 1.3807 x 10^{-23} J, T is room temperature) [1]. However, Benett has shown that the reversible computation using reversible gates is the solution to this issue [2]. It has two approaches physical and logical reversibility. Logical reversibility is the ability of the device to retrieve its input and output from each other logically;

whereas Physical reversibility is provision to reverse the input and output in electronic or quantum circuits [3].

Parity checking is one of the common mechanism adapted to detect the error in the transmission and data logic. During the computation, if the parity of the input data is preserved, then there is no need for checking the intermediate stages. Thus, the parity-preserving functional units can be constructed with parity-preserving reversible gates [4].

The division is one of the most complicated functions of computer arithmetic. In this paper, we have proposed fault-tolerant reversible logic gates to construct division unit. n-bit fault-tolerant reversible floating point division (FTRFPD) circuit is constructed with these gates. The proposed design is vulnerable to errors, and it is better than the existing ones in terms of quantum costs, garbage outputs and constant inputs.

The entire paper is organized as follows: in Section II, the basic definitions and performance measuring parameters are discussed. Section III discusses the relevant work previously done by various researchers in the same field. Section IV & V deal with the proposed new fault-tolerant reversible gates and fault-tolerant reversible floating point division unit. Finally, in Section VI the results obtained for the proposed division unit are being discussed.

2 Basic definitions

In this section basic definition of QCA, QCA clocking and performance measures commonly used are discussed.

2.1 QCA Basics

The basic element of QCA is a cell, which represents a bit of information as in Fig.1a. Each cell has four metal islands known as quantum dots. In quantum dots, two electrons occupy the four dots in "diametrically opposite" positions to polarize the dot. Logic '0' or Logic'1' is represented by the polarization position of dots as shown in Fig.1b[5].

The polarization can be computed as,
$P= ((P_1+P_3)-(P_2+P_4))/(P_1+P_2+P_3+P_4)$,
where P_i= Charge in the i^{th} quantum dot.

2.2 QCA Clocking

QCA circuit's information flow is controlled by the Bennett Clocking scheme. It has four phases to process the

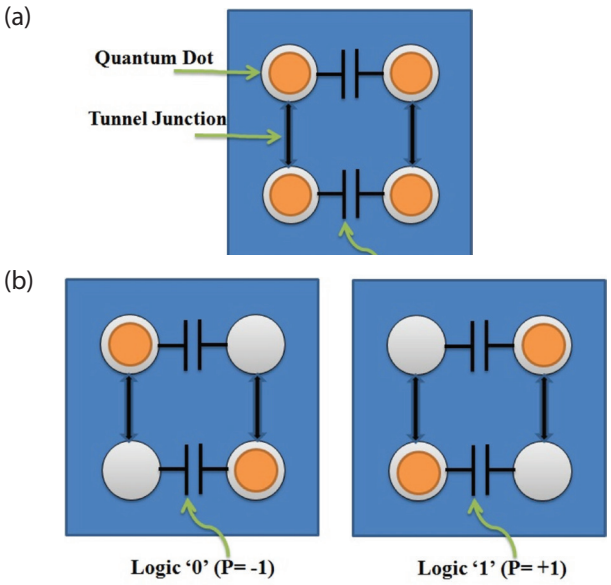


Figure 1: (a) QCA cell; (b) QCA cell polarized with logic '0' and logic '1'

information which is a switch, hold, release and relax as in Fig. 2. Each clock zone is 90-degree phase-shifted, which enables the computation to be carried out in a sequential manner [6].

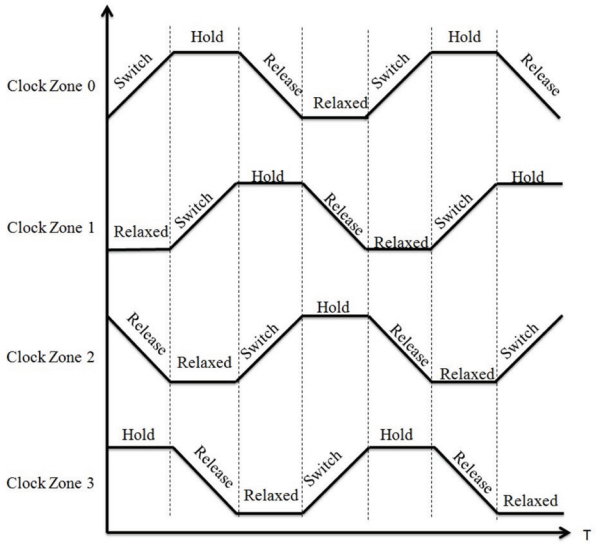


Figure 2: QCA Clocking with four phases

2.3 Performance measures

Four Performance measures encountered in this work are listed below:

- Quantum Cost: Quantum cost is calculated as the total number of 2*2 primitive gates required to derive the given reversible logic function [7]. Here the primitive gates refer to the conventional gates. They are Feynman, Toffoli, Fredkin and Peres gates.

- Garbage output: The unwanted output of the reversible circuit is known as garbage output [7].
- Constant inputs: The input set to a stable value throughout the computation of the reversible circuit is known as constant inputs [7].
- Number of gates: It is defined as the total number of reversible gates that are utilized to obtain the desired reversible logic [7].
- Delay: The delay of the reversible circuit is equal to the total number of gates in the circuit. [8]. In other words, the maximum number of gates between the input to the output of the function is the delay of the reversible circuit.
- Simple Reversible Gates: Fredkin, Feymann (CNOT), Toffoli and Peres are the most popularly used reversible gates. Toffoli is known as universal reversible 3 input gate, from this any reversible circuit can be derived [9]-[12].
- Other reversible gates: There are many other authors who proposed their own reversible gates such as DKG gate, MRG gate [13], NFT gate, TR gate and BVF gate [14]. Since, except NFT other gates are not fault-tolerant and the circuits derived from those gates are not fault-tolerant.

2.4 Fault-tolerant reversible logic

A Gate is said to be fault-tolerant reversible logic gate only when it satisfies the following three properties:

- Reversibility: In reversibility, input and output functions are uniquely derived from each other and vice versa for a reversible gate [15].
- Input ⇔Output
- Universality: When a reversible gate is able to realize NOT, NAND / AND & NOR / OR functions in the output, it satisfies universality property [15].
- Fault Tolerance: Nowadays, a reversible circuit is expected to be reliable under all environmental conditions. In other words, it should be vulnerable to the fault occurrence. A gate having the same parity as in equation (1) in its input and output is said to be a fault-tolerant gate [4].

$$I_1 \oplus I_2 \oplus I_3 \ldots\ldots \oplus I_n = O_1 \oplus O_2 \ldots\ldots \oplus O_n \quad \text{--------} \quad (1)$$

where, I_i = Inputs and O_i = Outputs of a gate

3 Related reversible logic works

A new reversible Half adder, Full Adder, Ripple carry Adders are being built using the proposed reversible logic gates. These gates satisfy the universality and reversibility conditions as a fundamental requirement for a reversible gate [16].

Fault-tolerant full adder (FTFA) is proposed using two Islam Gates (IG) which have 3 garbage outputs and 2 constant inputs. A carry skip BCD is designed with the proposed FTFA functional unit [17]. A fault-tolerant reversible adder (FTRA) is proposed in [18] and ripple carry adder (RCA), carry skip adder (CSA) and n-bit ALU are constructed using FTRA, which are fault-tolerant [18]. Low-cost parity-preserving reversible adders such as Carry look ahead adder (CLA), Carry skip adder (CSA) and BCD adder are constructed with less quantum cost and garbage output using LCG gates [19]. A fault-tolerant reversible decoder (n to 2n) is constructed using Double Fredkin and RDC gates [20].

A signed multiplier is designed with MNFT gate which is fault-tolerant. The operating speed of the multiplier is improved using Wallace tree structures [21]. A reversible single precision floating-point square root is proposed using a modified non-restoring algorithm with Reversible Controlled-Subtract-Multiplex [22].

As an initial step towards the sequential circuit design, the latches have been designed with reversible gates. RS Flip-flop is proposed in [23] with reversible gate BME and Peres. Also, D, RS and JK latches and flip-flops have been designed using MFG, FG and Toffoli reversible gates in [24].

Two approaches are proposed for n-bit fixed point division unit. Here, fault-tolerant reversible gates are utilized to make the entire division unit fault-tolerant. Both the approaches utilize nearly equal number of resources (quantum cost, garbage output etc.) [25]. A reversible floating point division is carried out with two different approaches which are conventional division and high-speed division. The results confirm that this approach is better than the previous [22] architectures in terms of quantum cost, garbage output [26]. A new fault-tolerant reversible RR gate is proposed to design a reversible division unit with fault-tolerance of n-bit. The module is constructed to meet the IEEE 754 format, which includes rounding register and normalization unit. Also, the division unit consumes less number of quantum cost, garbage output and number of gates than the previously available designs [8].

4 The proposed logic gates

A new reversible gate is introduced in two different methods: one is heroic act on the existing reversible gates and another is the creation of new gate to perform the desired operation. Fault tolerant 3*3 reversible gates are proposed to obtain the full adder function using Feynman and Fredkin gates [19]. These gates may not satisfy the universality property of a reversible gate.

Here, we propose 4 reversible gates, namely KMD gate 1, KMD Gate 2, KMD Gate 3 and KMD Gate 4 as shown in Fig. 3 (a-d). These gates satisfy the fundamental requirements (reversibility and universality) of a reversible gate [15]. In addition, they are fault-tolerant in nature, i.e. EXOR function of the inputs and the outputs are equal (parity preservation).

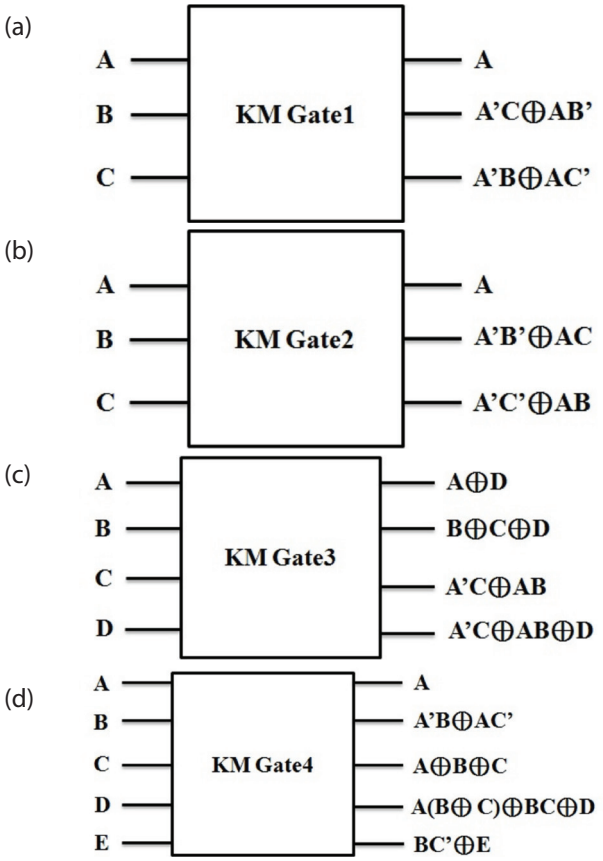


Figure 3: Block diagram (a) KMD gate 1 (b) KMD gate 2 (c) KMD gate 3 and (d) KMD gate 4

4.1 Fault-Tolerance, reversibility, and universality

The fault-tolerant (parity preservation) and reversibility characteristics of the proposed gates are satisfied for the proposed gates. The inputs and the outputs of KMD Gates are having the same priority. So, the EXOR of Inputs and Outputs gives always zero for a fault-tolerant gate.

Reversibility can be defined in two ways; one is, the computation overwriting the input vector with the output vector, and the other is, an unmodified copy of the input vector available elsewhere in the design [15].

For universality, a reversible gate must be able to produce NOT, AND & OR functions of 2-input format or it must be able to generate NOT, NAND / NOR functions of 2-input format [15]. The universality property of KMD Gates is represented in Table 1. From the above table, it is evident that all KMD Gates satisfy the universality property as stated in [15].

The proposed reversible gates can be constructed with fewer cells and occupy less area as shown in Table 2. Moreover, DKG and MRG are not fault-tolerant gates [13] [14]. But KMD Gates are fault-tolerant reversible gates. Thus, the construction of reversible circuits using these gates will have efficient fault-tolerant reversible circuits.

5 The Proposed methodology

In arithmetic operations, the basic operations are addition, subtraction, multiplication, and division. Of them, the division is the most challenging arithmetic

Table 1: Universality property of KMD gates

S. No.	Reversible Gate	Constant Input	Logic Function	Expression
	KMD Gate 1	A=1; C=0 / 1	Q=NOT (B)	Q = R′
		C=1	Q = NAND (A,B)	Q = A′ + AB′
		C=0	R = OR (A, B)	Q = A + A′B
	KMD Gate 2	B=C=0	R = NOT (A)	R = A′
		C=0	Q = NOR (A,B)	Q = A′B′ = (A+B)′
		C=1	R = AND (A,B)	R = AB
	KMD Gate 3	B=D=0; C=1	S = NOT (A)	S = A′
		B=1	R = OR (A, C)	R = A + A′C
		C=0	R = AND (A, B)	R = AB
	KMD Gate 4	B=C=1;D=0	Q = NOT(A)	Q = A′
		B=1	Q = NAND (A,C)	Q = A′ + AC′
		B=1; D=0 C=0	T = OR (A,C) Q = OR(A,C)	T = AC′ + C Q = AC′ + C

Table 2: Comparison of the proposed gates

Gates	Number of Cells used	Quantum Cost	Area (in µm2)
Fredkin gate [13]	187	5	0.19
DKG gate [13]	752	6	1.24
MRG GATE [13]	456	6	0.52
NFT gate[14]	128	-	0.142
KMD Gate 1	169	10	0.19
KMD Gate 2	121	10	0.13
KMD Gate 3	116	6	0.19
KMD Gate 4	244	12	0.42

operation in computer architecture design. A dedicated hardware module is incorporated into the division as part of the processor. It is a fundamental issue to identify the efficient division algorithm as per the IEEE 754 standard [27]. A complete division operation is a compound of sequential basic operations.

A proposed fault tolerant floating point division unit consists of the following elements: multiplexer, Parallel In Parallel Out (PIPO) left shift register, adder/subtractor unit, and rounding and normalization registers. All these functional units are designed as fault-tolerant.

There are two possible methods available for the division of integer numbers. They are restoring and non–restoring divisions. In both the methods, the base operations are addition/subtraction and shifting the variables [28].

For n bit D is a dividend (2n bits to store remainder and quotient after division), V is divisor, and Q is quotient register,

Restoring Division:
1. Shift the D (2n) to left one position.
2. Subtract V (n) from D(V-D) and place the result back in D.
3. If the Sign of D is 1, set MSB of Q_0 to 0 and add V back to D (Restore); otherwise, set Q_0 to 1.

Non-Restoring Division:
Step 1: (n times)
1. If the sign of D is 0, shift D left to the one-bit position and subtract V from D; otherwise, shift D and add V to D (V+D).
2. Now, if the sign of D is 0, set Q_0 to 1; otherwise, set Q_0 to 0.

Step 2:
1. If the sign of D is 1, add V to D (V+D).

In the restoring division, the left shift and subtract operation are equivalent to 2D-V. If D is negative, restore D and left shift, then subtract V which is equivalent to 2D+V. The latter case is used in the non-restoring division; which reduces the number of logical operations.

The following significant changes are made in the above algorithm and flow diagram which are shown in Fig.4:
- In the normal division, the dividend is shifted to the right side, here in the proposed method, it is left shifted.
- The shifting is advanced to the first place rather than after the subtraction.
- The remainder and quotient register are combined to form a single dividend register.

The complete flow diagram of restoring division is shown in Fig.4; in the case of non-restoring, and the path is slightly changed as combining 3a and 3b of Fig.4 without restoration. In addition, to meet the IEEE 754 standard of floating point representation, the rounding and normalization are carried out.

Algorithm:
Inputs: D (Dividend); V (Divisor) and Sel=0.
Outputs: R (Remainder) and Q (Quotient)

Steps:
1. Initial: Clk=High; SP=0; Sel=0; Count=0; D=0; V=0 (Registers are Initialized)
2. If (Clk)
   If (SP= =0)
   n-bit Inputs are parallel loaded in operand registers(D & V).
3. Else if (SP= =1 & Hold = = 0& Count <n)
   The operands are forwarded to n-bit parallel adder (as per non-restoring algorithm 2's complement addition).
   The output of the previous step is loaded into the D register and serial left shift one position in PIPO shift register.
4. If the partial result is positive (MSB=0) set Q_0=1; otherwise set Q_0=0;
5. Count = Count + 1;
6. If (Count>=n)
   If the result is negative; restore D and do rounding and normalization.
7. Dividend register MSB = Remainder; LSB = Quotient.
8. End.

5.1 Working Principle

The complete data path of fault-tolerant floating point division is shown in Fig.5. The significant units are multiplexers, registers (F2G), parallel adder, rounding and normalization units. The necessary control signals are

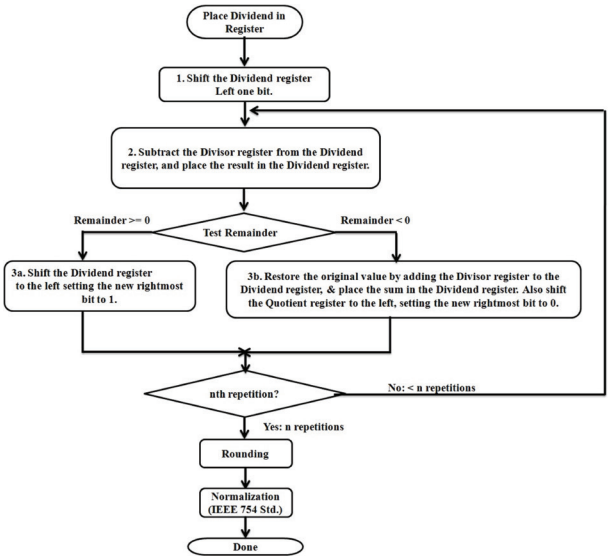


Figure4: Flow Diagram of floating point division

Clk, load, sel, SP, set q_0, shift and hold. These signals are released from the control unit at the appropriate time based on the Clk timing.

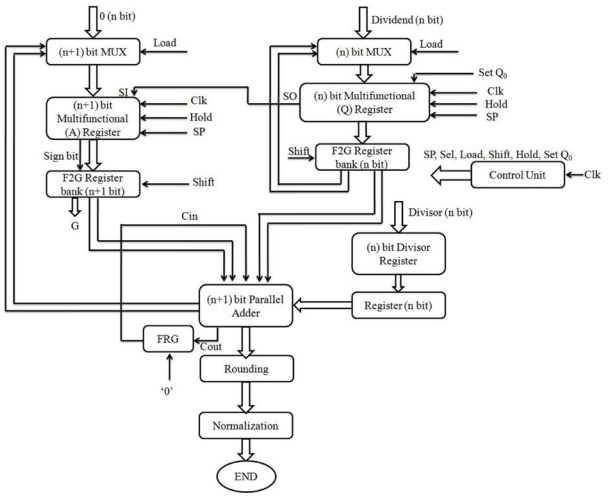


Figure 5: Fault-tolerant floating point division unit

When Clk is available and load & SP signals are high, the multifunctional registers are parallel loaded with '0' in 'A' register, and dividend in the Q register and divisor register are already loaded. In the next Clk, the dividend and divisor are loaded into (n+1) parallel adder. The adder performs the 2's complement addition, and the partial results are again stored back to higher order bits of the multifunctional register. In the meantime, left shifted (via F2G register) dividend is loaded back through the multiplexer and the MSB bit is serially shifted to the 'SO' of A register.

Here, non–restoring division is followed in order to reduce the number of computations [28]. So, it is not necessary to restore the dividend after an unsuccessful subtraction (ie. the partial result is negative). Instead, the partial result is 2's complemented via F2G register bank and an FRG register during the next cycle. The sign bit of the partial result decides the Q_0 value (ie. Q_0=0, if sign =1; 1, otherwise). The same procedure is repeated for 'n' Clk cycle. After n-cycle, if the result is negative, restoration takes place; otherwise, register Q contains the quotient and 'A' register contains the remainder of the successful division.

5.2 Key elements of reversible fault-tolerant division unit

The major functional units of reversible fault-tolerant division unit are multiplexers, operands registers, adder/subtractor, PIPO register, rounding and normalization registers. These functional units are being constructed using fault-tolerant gates; thereby the circuit becomes a fault-tolerant one.

Multiplexer:
KMD Gate 3 can be configured as a multiplexer with 'A' input as select line and others (B & C) are input data. The 3rd output provides the selected data. Fig.6 represents the 2 input multiplexer; when Sel=0; then C is selected; otherwise B is selected. The n-bit multiplexer can be derived by cascading the single bit structure. Here, the input D=0 provides 'sel' to be passed on to the next stage. The quantum cost of the n-bit Mux is 7n, and it has 2n garbage outputs.

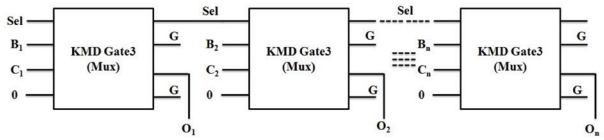


Figure 6: 2-input n-bit multiplexer

Reversible Parallel In Parallel Out (PIPO) Shift Register:
D latch can be derived from KMD Gate 3 as shown in Fig.7a. The 3rd output of the gate generates the necessary Q for the latch. A n-bit Parallel in Parallel Out (PIPO) is constructed by cascading the D-latches as shown in Fig.7a. The quantum cost of the n-bit PIPO is 7n, and it has 'n' garbage outputs.

A multifunctional register is designed using D-latch and multiplexers. It acts as a left shift register; PIPO register, SISO register, and normal storage register according to the control signal. Fig.7b shows the multifunctional register with control signals hold & SP and data signals SI (Serial Input) & PI (Parallel Input). The symbol of the register is shown in Fig. 7c. n-bit register has the quantum cost of 21n, number of gates 3n and 4n garbage outputs.

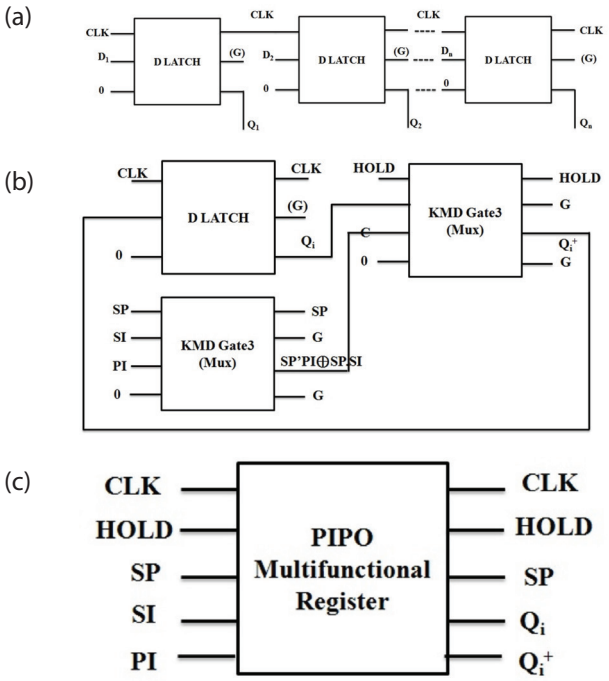


Figure 7: (a) n-bit PIPO Register (b) Construction of Multifunctional Register and (c) Symbol of Multifunctional Register

The output behavior of the multifunctional register is tabulated in Table 3 which is derived from equation (2). Here, the parallel load operation selects the external input, and the serial input transfers the previously computed data to the next register.

$$Q_i^+ = Hold'SP'I_i + Hold'SP.Q_{i-1} + Hold.Q_i \quad \ldots\ldots\ldots \quad (2)$$

The proposed D-latch using KMD Gate is having less of quantum cost, garbage output and gate count compared to the available latches as from Table 4. From the table, it is observed that the number of reversible gates used to construct D-latch in [8] is 7 which lead to high quantum cost and more garbage output, whereas the proposed design consists of one gate and least quantum cost of 9.

Table 3: Truth table for multifunctional register

Hold	SP	Qi+ (Next Output)
0	0	Ii (Input Loaded to Register in Parallel)
0	1	Qi-1 (Left Shift & LSB receiving input from Serial Input)
1	X	Qi (Maintaining Previous Value)

Fault Tolerant Reversible Adder:
The reversible fault-tolerant adder is being constructed using KMD Gate 4 with the quantum cost of 24 as shown in Fig.8. So, an n-bit adder consists of 21n quantum cost, 2n constant inputs, and 3n garbage outputs.

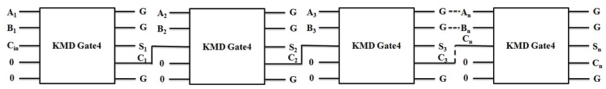


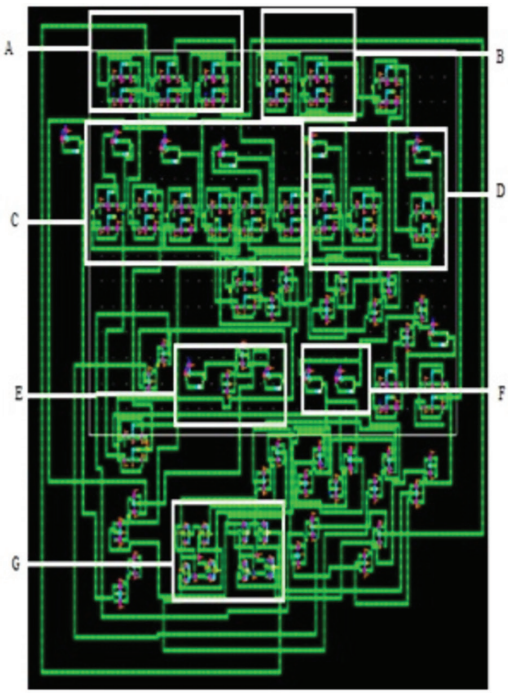
Figure 8: n-bit Fault-Tolerant Reversible Adder

Table 4: Performance analysis of D-latch

Parameters	[22]	[23]	[8]	Proposed design	Improvement % w.r.t		
					[22]	[23]	[8]
Quantum cost	14	10	47	9	35%	10%	80.8%
Garbage outputs	4	2	6	1	75%	50%	83.3%
Gate Count	3	3	7	1	66.6%	66.6%	85.7%
Number of Cells	-	-	-	116	-	-	-
Area	-	-	-	0.52μm²	-	-	-
Clock Zone	-	-	-	4	-	-	-

6 Results and Discussion

To perform the comparison between different reversible division logic circuits, few chosen parameters are,



A) (n+1)-bit Multiplexer
B) n-bit Multiplexer
C) (n+1)-bit Shift Register
D) n-bit Shift Register
E) Rounding Register
F) Normalization Register
G) Parallel Adder

Figure 9: 2-bit fault tolerant reversible divider circuit

quantum cost, garbage outputs, number of gates and constant inputs.

The QCA realization of the above functional units and entire division unit is done using QCADesigner 2.0.3 tool as shown in Fig.9. The structure consists of multiplexer, registers, adders, normalization and rounding off units. All those modules are integrated to form the fault-tolerant reversible floating point division unit.

Single bit multiplexers are combined to form the 2-bit and 3-bit multiplexers which receives dividend and zeros. At the same time, divisor register receives another divisor. The operands are then forwarded to the multifunctional register. This register is constructed using D-latch and multiplexer as in Fig.7. Then the operands are forwarded to the reversible adder. In the adder after every clk signal, the partial output is shifted one bit left. After n (number of bits) clk pulses, the adder output is forwarded to the rounding and normalization register to normalize the division as per the IEEE 754 single precision standard.

The cost and other parameters calculated for individual units of the n-bit division unit is shown in Table 5a. The major components are derived from KMD Gate 3, F2G, and KMD Gate 4. Since KMD Gate 3 is utilized to construct the multiplexer and multifunctional register, the uniformity of the divider is majorly improved.

Table 5b-e shows the comparison of quantum cost, number of gates, delay, and constant inputs of the division unit for 2 bits to 256 bits. From those tables, it is observed that the conventional and high-speed division array is exponentially increasing of Quantum Cost, Delay, and Constant Inputs with respect to a number of bits. But the proposed methodology is having linear relationship with the number of bits. So, proposed division unit can be utilized in any of the processor design. It is inferred that quantum cost, number of gates and delay are improved on a significant level compared to [25, 26]. For example, for the 256-bit division unit, the best available method has 3346 number of gates and delay [8]; while the proposed method has only 3076.

The pictorial representation of the consumption of quantum cost, number of gates, delay and constant inputs are shown in Fig. 10a-d. It is evident that the proposed method is having linear relation with number of bits, while the existing methods having quadratic relation with number of bits.

Table 5a: Performance measure calculations of individual modules of the division unit

S. No.	Module	Number of Bits	Gates Used	Number of Gates	Delay	Quantum Cost	Garbage Output	Constant Input
	Multiplexer	n	KMD Gate 3	n	n	6n	2n	n
		n+1		n+1	n+1	6n + 6	2n+2	n+1
	Multifunctional Register	n		3n	3n	18n	5n	3n
		n+1		3n+1	3n+1	18n+18	5n+5	3n+3
	Divisor Register	n	F2G	n	n	2n	2n	n
	Parallel Adder	n+1	KMD Gate 4	n+1	n+1	12n+12	3n+3	2n
	Register	n	F2G	n	n	3n	-	n
		n+1		n+1	n+1	3n+3	n+1	n+1
	Other Gates	1	Fredkin	1	1	5	2	1
	Total Cost			12n+4	12n+4	68n+44	20n+13	13n+6

Table 5b: Comparison of quantum cost for the existing and the proposed division unit.

Number Of Bits	Existing [25]		Existing [26]		Proposed
	Restoring	Non-Restoring	Conventional Division Array	High Speed Division Array	
2	210	203	33	82	180
4	360	353	74	165	316
8	660	653	204	415	588
16	1260	1253	656	1251	1132
32	2460	2453	2328	4267	2220
64	4860	4853	8744	15675	4396
128	9660	9653	33864	59995	8748
256	19360	19253	133256	234651	17452

Table 5c: Comparison of number of gates for the existing and the proposed division unit.

Number Of Bits	Existing [25]		Existing [26]		Existing [8]	Proposed
	Restoring	Non-Restoring	Conventional Division Array	High Speed Division Array		
2	59	57	13	34	44	28
4	95	93	33	69	70	52
8	167	165	79	175	122	100
16	311	309	251	531	226	196
32	599	597	883	1819	434	388
64	1172	1173	3299	6699	850	772
128	2327	2325	12739	25675	1682	1540
256	4631	4629	50051	100491	3346	3076

Table 5d: Comparison of delay for the existing and the proposed division unit.

Number Of Bits	Existing [25]		Existing [26]		Existing [8]	Proposed
	Restoring	Non-Restoring	Conventional Division Array	High Speed Division Array		
2	54	52	24	12	43	27
4	88	86	54	27	69	51
8	156	154	150	85	121	99
16	292	290	486	297	225	195
32	564	562	1734	-	433	387
64	1108	1106	6534	-	849	771
128	2196	2194	25350	-	1681	1539
256	4372	4370	99846	-	3345	3075

Table 5e: Comparison of constant inputs for the existing and the proposed division unit.

Number Of Bits	Existing [25]		Existing [26]		Proposed
	Restoring	Non-Restoring	Conventional Division Array	High Speed Division Array	
2	36	34	5	20	32
4	58	56	13	39	58
8	102	100	41	95	110
16	190	188	145	279	214
32	366	364	545	935	422
64	718	716	2113	3399	838
128	1408	1406	8321	12935	1670
256	2830	2828	33025	50439	3334

Table 6: Comparison of performance measures for n-bit division unit

Parameters	Existing [25]		Existing [26]		Proposed
	Restoring	Non-Restoring	Conventional Division Array	High Speed Division Array	
No. of Gates	18n+23	18n+21	3(n+2)2+2n/4	(n+2)(3n+11)/2	12n+4
Delay	17n+20	17n+18	3(n+2)2/2	-	12n+3
Garbage outputs	12n+18	12n+16	(n+2)2/2	(n+2)(3n+22)/4	20n+13
Quantum Cost	75n+60	75n+53	4(n+2)2+n/2	(n+2)(7n+27)/2	68n+44
Constant Input	11n+14	11n+12	(n+1)2+1/2	(n+2)(3n+14)/4	13n+6

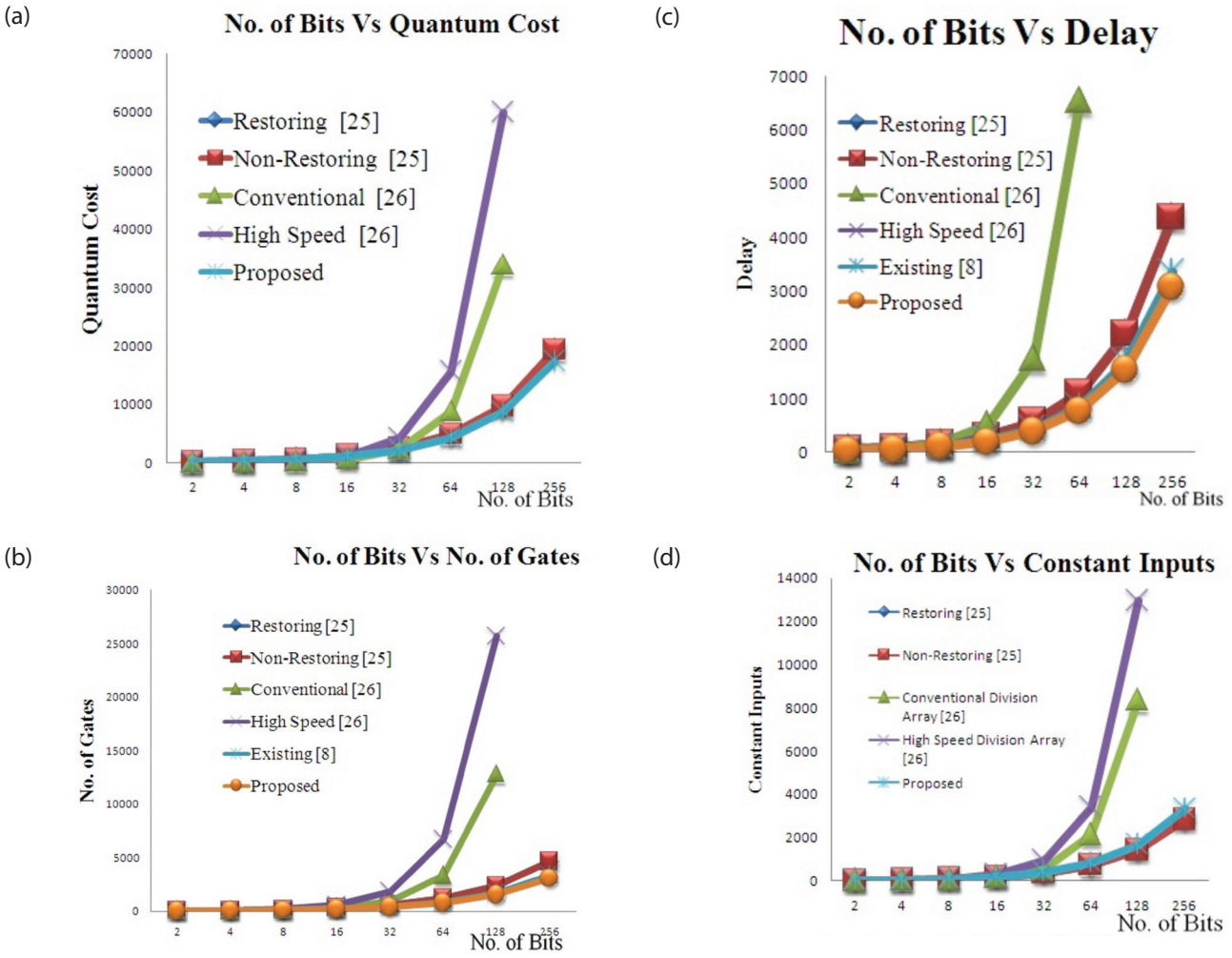


Figure 10: a. Number of bits vs Quantum cost; b. Number of bits vs Number of gates; c. Number of bits vs Delay; d. Number of bits vs Constant inputs

The estimated performance measurement of n-bit division unit is tabulated in Table 6. It is observed that the dependency factor 'n' – the number of bits is greatly reduced by the proposed method with respect to the existing [25, 26]. For example, conventional and high-speed division array have exponential relation with 'n', whereas the proposed method has a linear relationship. Moreover, the additional constant cost involved in 'n' is also reduced for the proposed method. From the last column of Table 6, it is observed that, the worst case additional cost is 44, but in the existing method, it is up to 60.

7 Conclusion

In this paper, we have proposed a new n-bit fault-tolerant reversible floating point division unit (FTRFPD) which functions according to the non-restoring algorithm. The proposed division unit is being constructed by the fault-tolerant reversible KMD Gates. The number of cycles and the number of computations required to complete the division is drastically reduced. Here, KMD Gate 3 is utilized to construct multiplexer and multifunctional register, for maintaining uniformity in the entire circuit design. The comparative results prove that the proposed method has greater improvement in the number of gates (12n+4), delay (12n+3) and quantum cost (68n+44) with respect to the existing methodology. Also, it has significant improvement in garbage output and constant input. The entire work is functionally verified using QCADesigner 2.0.3 tool. Furthermore, the efficient division unit can be incorporated into any ALU for floating point operation.

8 References

1. R. Landauer, "Irreversibility and heat generation in the computing process", *IBM J. Research and Development*, Vol. 5(3), July 1961, pp:183-191.

2. C.H.Bennett, "Logical reversibility of computation", *IBM J. Research and Development*, Vol. 17, November 1973, pp:525 – 532.
3. Chris Thachuk, "Logically and Physically Reversible Natural Computing": *Proc. 5th International Conference on Reversible Computation (RC'13)*, Vol. 7948,2013, pp. 247–262.
4. Behrooz Parhami, "Fault-Tolerant Reversible Circuits", *Proc. 40th Asilomar Conf. Signals, Systems, and Computers*, Pacific Grove, CA, October 2006, pp. 1726–1729.
5. K. Sridharan, Vikramkumar Pudi, "Design of Arithmetic Circuits in Quantum Dot Cellular Automata Nanotechnology", *Studies in Computational Intelligence*, Springer, Vol. 599, 2015.
6. Craig S Lent, Mo Liu and Yuhui Lu, "Bennett clocking of quantum-dot cellular automata and the limits to binary logic scaling", *Nanotechnology*, Vol. 17, 2006, pp.4240-4251.
7. Biswas, Md.Mahmudul Hasan, Chowdhury, Md.Hasan Babu, "Efficient approaches for designing reversible Binary Coded Decimal adders", *Microelectronics Journal*, Vol. 39, 2008, pp. 1693–1703.
8. Hafiz Md. HasanBabu, Md. Solaiman Mia, "Design of a compact reversible fault tolerant division circuit", *Microelectronics Journal*, Vol. 51, 2016, pp.:15–29.
9. T. Toffoli,"Reversible Computing", *Technical Report* MIT/LCS/TM-151, 1980, pp. 1-37.
10. E. Fredkin, T. Toffoli, "Conservative logic", *Int. J. Theor. Phys*., Vol. 21,1980, pp.219–253.
11. A. Peres, "Reversible logic and quantum computers", *Phys. Rev*., Vol. 32, 1985, pp. 3266–3276.
12. R. Feynman, "Quantum mechanical computers", *Found. Phys*., Vol. 16 (6), 1986, pp. 11-20.
13. Papiya Biswas, Namit Gupta, Nilesh Patidar, "Basic Reversible Logic Gates and It's QCA Implementation", *Int. Journal of Engineering Research and Applications*, Vol. 4 (6), June 2014, pp.12-16.
14. Ali NewazBahar, Sajjad Waheed, Nazir Hossain, "A new approach of presenting reversible logic gate in nano-scale", DOI 10.1186/s40064-015-0928-4, Springer, 2015.
15. Kalyan S. Perumalla, "Introduction to Reversible Computing", *CRC Press*, 2014.
16. Kamaraj, A., P.Marichamy, S.Karthika Devi, and M.Nagalakshmisubraja. "Design and Implementation of Adders using Novel Reversible Gates in Quantum Cellular Automata", *Indian Journal of Science and Technology*, Vol 9(8), 2017, pp. 1-7.
17. MD. Saiful Islam, Zerina Begum, "Reversible Logic Synthesis of Fault Tolerant Carry Skip BCD Adder", *Journal of Bangladesh Academy of Sciences*, Vol. 32 (2), 2008, pp.243-249.
18. Sen, Ganeriwal, Sikdar, "Reversible Logic-Based Fault-Tolerant Nanocircuits in QCA", *Hindawi*, dx.doi.org/10.1155/2013/850267, May 2013, 9 pages.
19. Valinataj, Mirshekar, Hamid Jazayeri, "Novel low-cost and fault-tolerant reversible logic adders", *Computers and Electrical Engineering,* Vol. 53, 2016, pp.56–72.
20. Md. Riazur Rahman, "Cost Efficient Fault Tolerant Decoder in Reversible Logic Synthesis", *International Journal of Computer Applications,* Vol. 108 (2), December 2014, pp. 7-12.
21. Xuemei, Fulong, Liangmin, Yonglong, Min Hu, "Design of fast fault tolerant reversible signed multiplier", *International Journal of the Physical Sciences,* Vol. 7(17), 23 April 2012, pp. 2506 - 2514.
22. A.V. Anantha Lakshmi, Gnanou Florence Sudha, "Design of a reversible floating-point square root using modified non-restoring algorithm", *Microprocessors and Microsystems*Vol. 50, 2017, pp. 39–53.
23. Belayet Ali, Mosharof Hossin, Eneyat Ullah, "Design of Reversible Sequential Circuit Using Reversible Logic Synthesis", *International Journal of VLSI design & Communication Systems (VLSICS)* Vol.2 (4), December 2011, pp. 37- 45.
24. Thapliyal H, Vinod A.P., "Design of reversible sequential elements with the feasibility of transistor implementation", *In Proceedings of the IEEE International Symposium on Circuits and Systems*, 2007, pp. 625–628.
25. Faraz Dastan, Majid Haghparast, "A novel nanometric fault tolerant reversible divider", *International Journal of the Physical Sciences* Vol. 6(24), 16 October 2011, pp. 5671-5681.
26. L.Jamal, H.M.H.Babu, "Efficient approaches to design a reversible floating point divider", *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems*, Vol. 13, 2013, pp.3004–3007.
27. IEEE standard for floating-point arithmetic, IEEE Std.754-2008, 2008, pp.1–58.
28. Carl Hamacher, Vranesic, Safwat Zaky, "Computer Organization", 5th Edition, Tata McGraw-Hill, 2011.

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A microfluidic micromixer fabricated using polydimethylsiloxane-based platform for biomedical applications

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Abstract: Personalised dosing microfluidic devices have great potential in transforming current biomedical treatment into more efficient and patient-tailored using lab-on-chip designs. One of the current challenges in manufacturing microfluidic devices is designing suitable mixers, at the microscale level, with intricate geometrical dimensions. The study aimed at designing micromixers using polydimethylsiloxane-based platform and investigated their performance and potential applications in biomedical devices. New microchip-like structure was fabricated and consisted of two inlets and one outlet. A mould was fabricated based on polydimethylsiloxane platform and the new design was examined in terms of mixing patterns. The flow-mixing process was tested for efficiency and robustness. The novel design showed consistent intricate dimensions suggesting fabrication method was robust and precise. The mixing ability of the micromixers showed semi-circular flow with efficient mixing at low liquids pressure (< 50 mbar) suggesting ability to mix fluids with various viscosities. Accordingly, the newly designed micromixers using polydimethylsiloxane-based platform with two inlets and one outlet have promise in biomedical fluid-mixing applications.

Keywords: Micromixer, PDMS; Mixing efficiency

Mikrofluidični mikro mešalnik z uporabo platforme na osnovi polidimetilsiloksana za biomedicinske aplikacije

Izvleček: Mikrofluidične naprave s poosebljenim doziranjem imajo velik potencial pri spremembi trenutnega biomedicinskega zdravljenja v bolj učinkovito zdravljenje s pacientu prilagojenim dizajnom lab-on-chip naprav. Trenutni izziv je načrtovanje ustreznih mešalnikov na mikro nivoju. Članek predstavlja načrtovanje mikro mešalnikov z uporabo platforme na osnovi polidimetilsiloksana in njihovo integracijo v biomedicinske naprave. Nova mikročip struktura ima dva vhoda in en izhod. Kalup je izdelan na osnovi polidimetilsiloksana. Nov dizajn je bil opazovan s strain različnih mešalnih vzorcev. Proces pretočnega mešanja je bil preizkušen na osnovi učinkovitosti in robustnosti. Mešalna sposobnost kaže semi-cirkularni pretok z učinkovitim mešanjem pri nizkih tlakih (< 50 mbar) in različnih viskoznostih tekočin.

Ključne besede: mikro mešalnik, PDMS; izkoristek mešanja

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1 Introduction

The proper mixing of reagents is an important process in biochemical experiments, which aims to incorporate various fluids as a way to detect concentrations of biological molecules. Microfluidic devices have attracted a huge attention due to a wide range of potential applications such as in diagnostics and pharmaceutical and biological applications [1-3]. The purpose of microfluidic mixing is to obtain a complete and fast mixing of numerous samples in microscale devices, by employing the diffusion effect at low Reynolds number in microfluidic systems [4]. Microfluidic technologies can be used to produce micromixers in order to make the whole process more efficient and reliable, minimizing cross-contamination and reducing the time and labour costs. Mixing in microchannels is a principle applied in many modern biomedical devices. Active and passive mixing approaches can be found in microfluidic chips [5]. Active micromixers require external energy sources (electro-kinetic [6], [7], ultrasonic [8], electrostatic or magnetic fields [9, 10] to generate perturbations in fluid flow. These devices provide a very good mixing characteristics and flow control. However, they are expensive for fabrication and cannot be easily integrated into complete microfluidic systems. Passive micromixers depend on diffusion process [11]. A smart geometric design is a key enabler of efficient mixing process in this type of micromixers. They can be manufactured in a simple way, using low-cost fabrication techniques and can be easily integrated with other functional components in Lab-on-chip [12] or Organ-on-chip [13] concepts, which are very popular nowadays. Taking into account above-mentioned advantages, this paper analyses fabrication process and testing of performances of a passive micromixer with innovative design. Various technologies can be used for manufacturing passive micromixers such as: printed circuit board (PCB) [14], low temperature co-fired ceramics (LTCC) [15], xurographic PVC foils-based technique [16], silicon-based or glass-based microfabrication [17], polydimethylsiloxane (PDMS) technology [18]. An integrated microfluidic chip for rapid mixing of multiple liquids which requires few manipulations of pipettes has been developed in [19]. That microfluidic chip was fabricated by PDMS casting, integrated a micromixer among four other components. The lost-wax casting technique was used in [20] for fabrication of 3D PDMS microfluidic devices, but with very simple design. The fabrication of PDMS microfilters, which were chemically bonded to polyimide (PI), polyethylene-naphthalate (PEN), and polyethylene-terephthalate (PET) substrates, was demonstrated in [21]. With regard to different geometrical shape of microchannels as a main constituent of passive micromixers, the following structures have been reported: lamination mixer [22], rotational-type mixer or spiral microchannels [23], groove micromixer [24], staggered herringbone mixer [25] and splitting and recombining the flow mechanism [26].

Manufacturing of high-performance microfluidic devices can be challenging, in particular when utilising complex structures of versatile and inconsistent shapes. This study investigates innovative and complex designs of micromixer and their fabrication using PDMS-based platforms. PDMS is chosen for the fabrication of the micromixer due to its biocompatibility, transparency and mechanical flexibility. Design is based on semi-circular shapes of barriers creating disturbances aiming to achieve better mixing performances. The experimental testing of the fabricated microfluidic chip has been also performed.

2 Design, simulation and fabrication of micromixer

2.1 Design of micromixer

The proposed innovative design of the microfluidic micromixer, including its dimensions is presented in Figure 1. The chip is composed of two inlets and one outlet. Internal structure of the chip consists of semi-circular barriers which could provide the chaotic advection with diffusion and enable efficient mixing of fluids from inlets. The calculation of the Reynolds number in the mixing area of 2000 µm width and 60 µm depth was between 0.2 - 3.0, therefore the chaotic advection with diffusion takes place. A design of microchannels was created in CleWin 4.0 software tool.

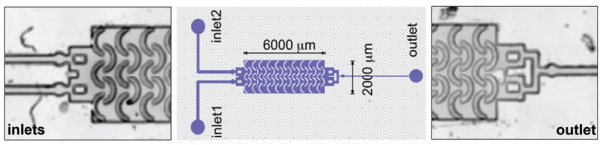

Figure 1: Design and dimensions of microfluidic chip showing the positions of the inlets, the mixing chamber and the outlet

2.2 Simulation results for the proposed micromixer

The proposed micromixer performances have been analysed through simulation results. Numerical simulation was carried out by software tool COMSOL multiphysics, using two modules Laminar Flow and Transport of Diluted Species. The Laminar Flow module has been used for determination of the speed field vector which then transferred into the Transport of Diluted Species module which calculates the concentration of fluid in the designed micromixer. In order to provide

evidence that proposed mixer operates properly we started simulation with the following parameters: the fluid pressure at inlets equal to 50 mbar, concentration of the red fluid (on one inlet) was 500 mol/m^3, and on another inlet (blue fluid) 0 mol/m^3. The obtained results of simulation are presented in Figure 2.

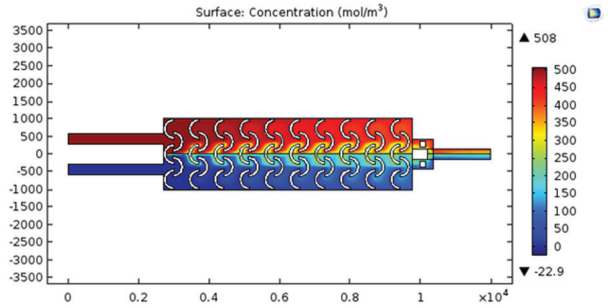

Figure 2: Simulation results of the micromixer design

From the presented simulation results it can be concluded that around internal semi-circular barriers good mixing of two fluids from inlets is performed.

2.3 Fabrication of micromixer

There are two main steps to manufacture a microfluidic chip in PDMS technology: (1) fabrication of a mould and (2) replica moulding. To fabricate a mould, photolithography was used to form a pattern of the designed channels as a moulding master on a glass substrate (75 mm × 50 mm size, 0.96 mm thickness, Corning, USA). A glass substrate was cleaned with isopropanol and heated at 120 °C for 15 minutes. A dry film photoresist (30 µm thickness, ORDYL) was covered and laminated on the glass substrate using a laminator. Using cutting-edge technologies and in-house built in systems, the first protective film was removed and then the resist was exposed for 10 seconds with an UV light (UV-KUB2) using the photomask. After exposing, the second protective film was removed. To etch the pattern, the resist was developed with agitated manually for 2 minutes in a bath containing commercial developers. Then it was rinsed with the commercial chemical, following with isopropanol. Finally, the mould was dried with compressed air. The process of mould fabrication is shown in Figure 3.

Once the mould was created, the microchannels were built using chemically integrated polymer-copolymer matrices, namely polydimethylsiloxane (PDMS), by replica moulding. Using soft lithography, PDMS was used to replicate the patterned glass substrate served as a master. A mixture of PDMS base and curing agent (Sylgard 184, Dow Corning, USA) was prepared in the ratio of 10:1 by weight, and was stirred vigorously until well mixed. The mixture was degassed using a vacuum

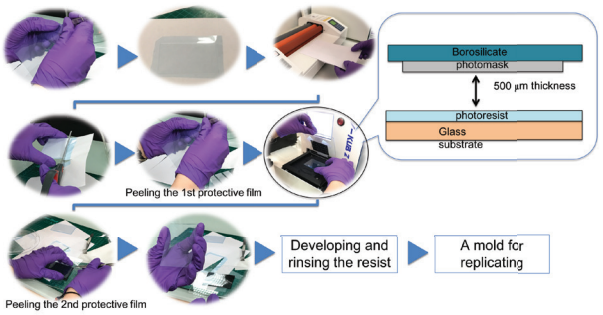

Figure 3: The process of mould fabrication using photolithography process

chamber in order to eliminate air bubbles for 30 minutes. Next, the mixture was cast onto the master. The master filled with PDMS was cured in an oven at 80 °C for 2 hours. Then the replica was cut along the edge of the mould using a scalpel blade and was peeled off from the master. To access holes for the fluidic inlets and outlet insertion point, the PDMS chip were punched using a biopsy punch (1 mm in diameter, Tedpilla). The surface of the punched PDMS chip was exposed to oxygen plasma for 2 minutes, and was placed as soon as possible against a clean glass slide to form a permanent bond. The process of PDMS replication is illustrated in Figure 4.

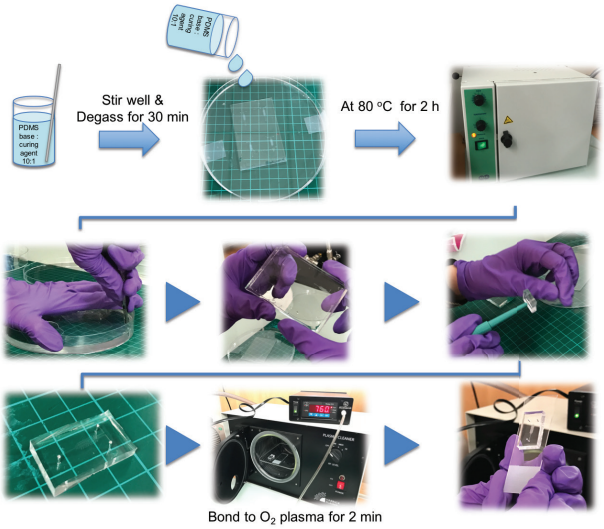

Figure 4: The process of PDMS replication using soft lithography

3 Experimental method

After microfluidic chips were fabricated, the pattern of microfluidic chip was examined under microscope. The size of microfluidic chip was comparable to one-euro coin as shown in Figure 5A. The measurements were

performed in a mixing channel with a cross-section of 2 × 6 mm^2. The first part of the channel was divided into two small inlets, and the shape of semi-circular was used as barriers in the mixing channel (the middle part) as shown in Figure 5B.

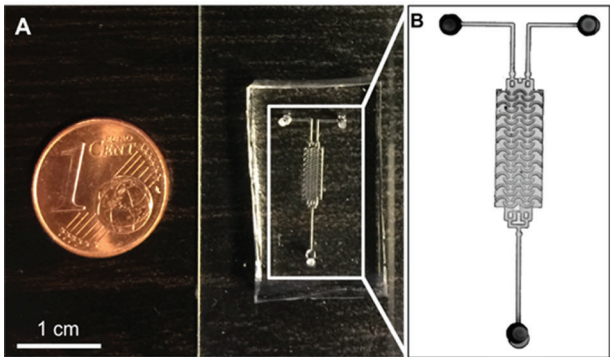

Figure 5: (A) Prototype of the fabricated microfluidic chip, (B) Microscope images showing the pattern inside microfluidic chip

The goal of microfluidic mixing is a thorough mixing of two or more samples in microfluidic devices. In order to achieve that goal, microchannel was designed with barriers to create the chaotic advection with diffusion (Reynolds < 10). Herein, the mixing pattern of the proposed microfluidic chip was studied with microfluidic flow controller (OB1) from Elveflow®. The experimental set-up of microfluidic system is shown in Figure 6.

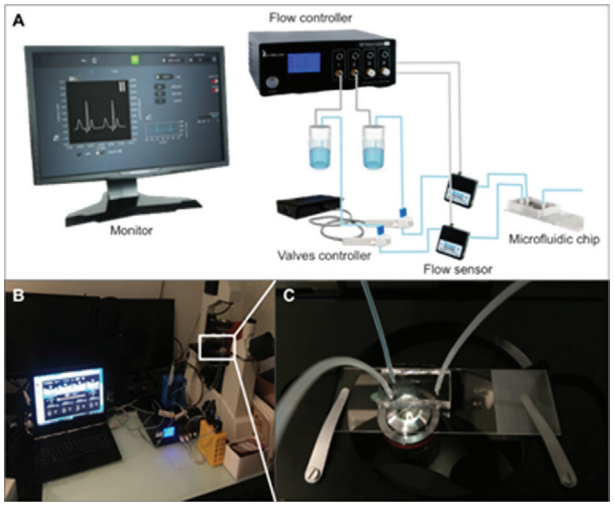

Figure 6: (A) Schematic illustration of experimental set-up for microfluidic mixing study. (B) Photo of experimental setup. (C) Zoom-in version of microfluidic chip under microscope

The flow controller was connected with vacuum pump, which is the pressure supply to the system. Pressure or flow was monitored by the Elveflow Smart Interface on computer. Microfluidic valves controllers were used to quickly start/stop flow. Flow/pressure sensor was also connected to the system for automatically adjusting the pressure in order to reach the set flow rate value. With this set-up, the pressured liquids from samples were smoothly and precisely flowed into microfluidic chip at desired rate. Flow in the chip was then observed under microscope.

4 Results and discussion

4.1 Testing of mixing performances at various pressures

In this study, liquid pressure was varied from 40-200 mbar. The pressure for each channel was set at desired value. Two channels were set at same pressure flows. One channel represented the drug, which was in blue solution and another channel contained just water, which represented normal saline solution using to dilute the drug. At the first stage, the accuracy of the system was verified. At predetermined pressure, we collected samples at each pressure for 6 minutes. The representative of samples collected in each set of experiment is shown in Figure 7A. The measured volumes and appropriate flow-rates are presented in Figure 7B.

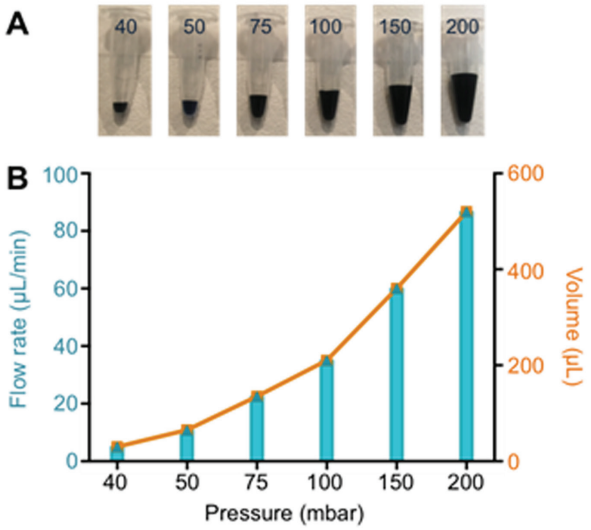

Figure 7: (A) Representative photos of samples collected at various pressure flows. (B) Volume and flow rate at studied pressure range

The flow-rate results were consistent with controlled pressured as expected. The obtain results indicate that the flow was precisely tuned and controlled as it was desired in this experiment. This precise flow control is important for flow transition into microchannel in order to simulate controlled drug injection into the microfluidic system.

4.2 Evaluation of mixing efficiency

To investigate the mixing performance, the standard deviation of the concentration of the colouring solution was calculated by a custom JavaScript in ImageJ. Briefly, the captured images were split into 8-bit images of red, green, and blue components. The red component was only used for measuring the intensities pixel-by-pixel via the detection zone. A standard curve relating intensities and concentrations was established. After converting the intensities to the concentrations, the homogeneity was represented by the standard deviation of the concentration over the detection area. The standard deviation can be normalized by the mean concentration to calculate the mixing index (MI): that was defined as in Eq. (1):

$$MI = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\frac{\left(C_i - \overline{C}\right)^2}{\overline{C}}} \quad (1)$$

Where Ci is the concentration of pixel i, N is the number of pixel over detection zone, and $\overline{C}$ is the ideally average concentration at well-mixing which is equal to 50% of the initial concentration. The standard deviation will be 0 for well-mixing. The mixing efficiency was defined as in Eq. (2):

$$\eta = 1 - \mathrm{MI} = 1 - \sqrt{\frac{1}{N}\sum_{i=1}^{N}\frac{\left(C_i - \overline{C}\right)^2}{\overline{C}}} \quad (2)$$

The efficiency is therefore between $0 < \eta < 1$. When $\eta = 0$ means the highest variation of concentration, *i.e.* no mixing. While $\eta = 1$ is well-mixing.

To relate the intensity with the corresponding concentration, the standard curve was evaluated. The preparation was used the concentration of 10 % (V/V) liquid food dye red in water solution. To cover the concentration, range from 0 – 100%, the standard curve was fit by a polynomial.

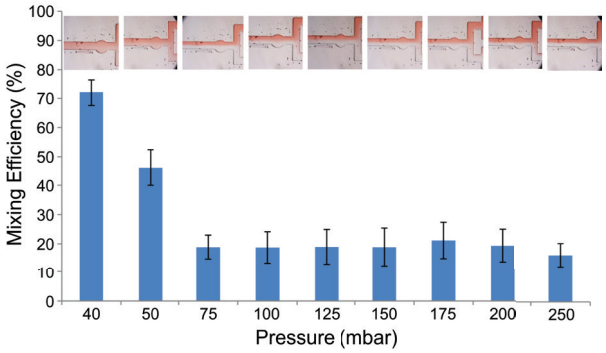

Figure 8: Mixing efficiency and enlarged images of outlet are representatives of the fluid flow within micromixer at different pressure flows

In addition, the mixing was investigated with different pressure set-ups. The liquid 1 (red colour) and liquid 2 (water), at room temperature, entered the inlets from separated channels. The flow in the proposed microfluidic chip was observed under microscope. The mixing efficiency was performed and mixing was quantified using above-mentioned equations. The results are illustrated in Figure 8. The mixing efficiency of is 72% at 40 mbar. It can be observed that at lower pressure (≤50 mbar), two solutions were mixed thoroughly inside microfluidic chip as shown in Figure 9. The proposed micromixer efficiency around 72 % for low pressure, is comparable with the already reported mixing efficiency. For example, in paper [27], authors reported the following maximum efficiency 69, 75, and 79 % for three types of configurations of meander types of microchannels. Additionally, in the paper [28], authors presented T-micromixer's with efficiency around ~20% at similar pressures.

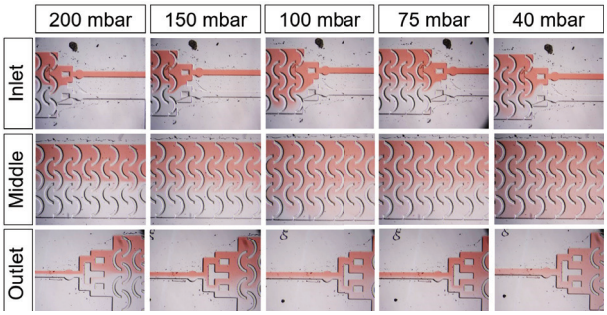

Figure 9: Microscopic images (4×) obtained by mixing experiment in micro-mixer device at various pressure flows

At high-pressure flow (>75 mbar), the mixing did not occur efficiently, because the high velocity flow rate along channel was generated, resulting in fluid could not travel across the channel by the chaotic advection at a very short period of time. Even though, the mixing was not efficient at high flow rates, the diffusion area was larger when flow rate was slower. However, design of a passive micromixer is dictated by its intended application. For example, for chemical reactors and for biosensing application, the flow rate and applied pressure of the tested liquid should be small. That means, the mixing effect in the microfluidic chip should be performed by diffusion. We proposed semicircular barriers in one row 3 and in the next row 2, shifted in the space. In this way, it is achieved that fluid going between these barriers and diffusion effect are pronounced and chaotic mixing realized. Having one and the next rows close to each other, the good mixing efficiency can be reached only for low flow and small

pressures, which is appropriate for intended (above-mentioned) applications of the proposed microfluidic chip.

5 Conclusion

Findings of this study showed that the new design of micromixers exhibits preferable features with promising efficacy in biomedical and fluid-mixing applications. The use of PDMS has enhanced the performance of the micromixers and enables improved flow-mixing properties, which has significant implications in biomedical sensors and molecular-based detection capabilities. The ability of the newly designed micromixers to mix fluids of solution at a significantly low pressure (<50 mbar) is indicative of its potential biomedical applications, and thus, future work will aim to enable further development and testing of the device in biological setting such as *in vivo* analyses.

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7 References

1. Yong Hwang S, Jae Seo I, Yong Lee S, Ahn Y. Microfluidic multiplex biochip based on a point-of-care electrochemical detection system for matrix metalloproteinases. Journal of Electroanalytical Chemistry 2015, doi: 10.1016/j.jelechem.2015.08.015.
2. Huang Y, Cai D, Chen P. Micro- and Nanotechnologies for Study of Cell Secretion. Analytical Chemistry 2011; 83: 4393-40.
3. Zhan Z, Yao P, Dong Z, Tung S, Hohnbaum J, Srinivasan B, Li JW. Insulin Detection Based on a PDMS Microfluidic System. Proceedings of the 2010 IEEE International Conference on Nano/Molecular Medicine and Engineering December 5-9, 2010, Hong Kong.
4. Sundra S, Fhong Soon C, Zainal N, Sek Tee K, Ahmad N, Hua Gan S. The Effects of Micromixing Two Solutions of Two Concentrations in a Two Tier PDMS Micromixer. IOP Conf. Series: Materials Science and Engineering 2017; 226: 012121 doi:10.1088/1757-899X/226/1/012121.
5. Lee CY, Chang CL, Wang YN, Fu LM. Microfluidic mixing: a review. Int J Mol Sci. 2011; 12: 3263-3287.
6. Oddy MH, Santiago JG, Mikkelsen JC. Electrokinetic instability micromixing. Anal. Chem. 2001; 73(24): 5822-5832.
7. Scott Lynn N, Henry CS, Dandy DS. Microfluidic mixing via transverse electrokinetic effects in a planar microchannel. Microfluid Nanofluid. 2008; 5: 493-505.
8. Yang Z, Matsumoto S, Goto H, Matsumoto M, Maeda R. Ultrasonic micromixer for microfluidic systems. Sensors Actuators A Phys. 2001; 93(3): 266-272.
9. Wen CY, Yeh CP, Tsai CH, Fu LM. Rapid magnetic microfluidic mixer utilizing AC electromagnetic field. Electrophoresis. 2009; 30(24): 4179-4186.
10. Liu F, Zhang J, Alici G, Yan S, Mutlu R, Li W, Yan T. An inverted micro-mixer based on a magnetically-actuated cilium made of Fe doped PDMS. Smart Mater. Struct. 2016; 25: 095049 (7pp).
11. Stroock AD, Dertinger SK, Ajdari A, Mezić I, Stone HA, Whitesides GM. Chaotic mixer for microchannels. Science. 2002; 295(5555): 647-651.
12. Schumacher S, Nestler J, Otto T, Wegener M, Ehrentreich-Förster E, Michel D, Wunderlich K, Palzer S, Sohn K, Weber A, et al. Highly integrated lab-on-chip system for point-of-care multiparameter analysis. Lab on a Chip 2012; 12(3): 464-473.
13. Balijepalli A, Sivaramakrishan V. Organs-on-chips: research and commercial perspectives. Drug Discovery Today 2017; 22(2): 397-403.
14. Cabello M, Aracil C, Perdigones F, Quero JM. Conditioning Lab on PCB to Control Temperature and Mix Fluids at the Microscale for Biomedical Applications. Spanish Conference on Electron Devices (CDE), 2017.
15. Malecha K, Golonka LJ, Baldyga J, Jasinska M, Sobieszuk P. Serpentine microfluidic mixer made in LTCC. Sensors Actuators B Chem. 2009; 143(1): 400-413.
16. Chirasatitsin S, Kojić S, Stojanović G. Optimization of microchannel fabrication using xurographic technique for microfluidic chips. Scientific conference ETIKUM'2017, Novi Sad, Serbia, December 06-08, 2017.
17. Silverio V, Cardoso S, Gaspar J, Freitas P, Moreira ALN. Design, fabrication and test of an integrated multi-microchannel heatsink for electronics cooling. Sensors and Actuators A: Physical. 2015; 235: 14-27.
18. He W, Xiao J, Zhang Z, Zhang W, Cao Y, He R, Chen Y. One-step electroplating 3D template with gradient height to enhance micromixing in micro-

fluidic chips. Microfluid Nanofluid, DOI 10.1007/s10404-015-1607-z.
19. Chen PC, Chen YC, Tsai CM. Microfluidic chip for rapid mixing and uniform distribution of multiple reagents using commercial pipettes. Microelectronic Engineering 2016; 150: 57-63.
20. Chung C, Chen YJ, Chen PC, Chen CY. Fabrication of PDMS Passive Micromixer by Lost-Wax Casting. International Journal of Precision Engineering and Manufacturing. 2015; 16(9): 2033-2039.
21. Lee M, Lopez-Martinez MJ, Baraket A, Zine N, Esteve J, Plaza JA, Ahmed N, Elaissari A, Jaffrezic-Renault N, Errachid A. Combination of PDMS microfilters and micromixers based on flexible thermoplastic films for size sorting and mixing of microparticles. J. Appl. Polym. Sci., 2015; 42088 (1 of 12), DOI: 10.1002/APP.42088.
22. Cha L, Kim J, Ryu SK, Park J, Jeong Y, Park S, Park S, Kim HC, Chun K. A highly efficient 3D micromixer using soft PDMS bonding. J Micromech Microeng. 2016; 16:1778-1782.
23. Sudarsan AP, Ugaz VM. Fluid mixing in planar spiral microchannels. Lab Chip. 2006; 6:74-82.
24. Stroock AD, Dertinger SK, Whitesides GM, Ajdari A. Patterning flows using grooved surfaces. Anal Chem. 2002; 74:5306-5312.
25. Stroock AD, Dertinger SKW, Ajdari A, Mezic I, Stone HA, Whitesides GM. Chaotic mixer for microchannels. Science 2002; 295:647-651.
26. Abadi HS, Packirisamy M, Wuthrich R. High performance cascaded PDMS micromixer based on split-and-recombination flows for lab-on-a-chip applications. RSC Advances 2013; 3:7296.
27. Kuo JN, Jiang LR. Design optimization of micromixer with square-wave microchannel on compact disk microfluidic platform. Microsyst Technol, 2014; 20:91-99.
28. Nimafar M, Viktorov V, Martinelli M. Experimental investigation of split and recombination micromixer in confront with basic T-and O-type micromixers. International Journal of Mechanics and Applications. 2012;2(5):61-9.

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Computer Simulation Model for Evaluation of Radiation and Post-Irradiation Effects in Voltage Regulator with Vertical PNP Power Transistor

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Abstract: The aim of the presented research was to develop a faithful SPICE simulation model of radiation and post-irradiation effects in a low-dropout voltage regulator with a vertical serial PNP transistor. The main parameters for the analysis of the circuit's radiation response were the voltage regulator's maximum output current and the minimum dropout voltage, as well as the serial transistor's excess base current. All the data, comprised of the old irradiation and new annealing results, were unified and normalised, in order to enable a broad insight in the radiation tolerance of the examined circuits. Initial radiation effects, as well as the late post-irradiation effects, were successfully simulated using the variations of the maximum forward emitter current gain and knee current of the serial PNP power transistor. Ten-year room temperature annealing led to a significant recovery of the serial transistor's excess base current, yet the maximum output current and minimum dropout voltage, in most cases, expressed further degradation. On the other hand, two short-term, high-temperature annealing periods led to the tremendous recovery of all of the irradiated voltage regulators, reducing the circuit degradation down to the level perceived after absorption of nearly 10% of the total ionising dose.

Keywords: vertical PNP transistor; excess base current; forward emitter current gain; computer simulation; voltage regulator, ionising radiation.

Računalniški simulacijski model za ocenjevanje sevalnih in post sevalnih vplivov na napetostni regulator z vertikalnim močnosnim tranzistorjem PNP

Izvleček: Cilj raziskave je bil razvoj zanesljivega SPICE simulacijskega modela sevalnih vplivov na low-drop napetostni regulator z vertikalnim serijskim tranzistorjem PNP. Glavni parametri analize odziva regulatorja na sevanje je bil največji izhodni tok in najnižja napetostna razlika med vhodom in izhodom (dropout napetost) ter bazni tok tranzistorja. Vsi podatku skupaj z rezultati starega sevanja in toplotne obdelave, so bili poenoteni in normalizirani za lažji vpogled v sevalno odpornost vezij. Začetni sevalni vplivi, kakor tudi post-sevalni vplivi, so bili uspešno simulirani s spreminjanjem ojačenja emitorskega toka in kolenskega toka tranzistorja PNP. Deset letna temperaturna obdelava pri sobni temperature je vodila k očitni ozdravitvi tranzistorskega baznega toka. Največji izhodni tok in najnižja dropout napetost je v večini primerov pokazala dodatno degradacijo. Po drugi strani pa sta dve kratkotrajni visokotemperaturni obdelavi pokazali občutno ozdravljenje obsevanih napetostnih regulatorjev, pri čemer je bila degradacija vezja ob 10% sevalni dozi zanemarljiva.

Ključne besede: vertikalni tranzistor PNP; bazni tok; ojačenje emitorskega toka; simulacije; napetostni regulator; ionsko sevanje.

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1 Introduction

Despite the increasing use of switching power supplies, linear voltage regulators still have a wide area of use in electronic devices, particularly in battery-powered systems [1]. This also applies to radiation-tolerant electronic devices, used in radiation environments such as satellites, nuclear and medical facilities as well as in the military environment. Bipolar transistors [2-5]

and analogue integrated circuits [6, 7] (including voltage regulators [8-11]) have been extensively examined in the radiation fields, particularly following the discovery of the enhanced low-dose-rate sensitivity (ELDRS) in bipolar transistors [12, 13].

Since the cost of dedicated radiation-tolerant integrated circuits is very high, in recent years extensive efforts have been made to identify commercial off-the-shelf (COTS) integrated circuits (and related technology processes) suitable for application in radiation environments [14]. Among the tested circuits is the low-drop-out voltage regulator *STMicroelectronics*® L4940V5, a circuit with a vertical PNP pass transistor [15], founded on the complementary BiCMOS process [16]. The circuit demonstrated unexpectedly high radiation tolerance [17-21], qualifying itself as a serious COTS candidate for use in moderate-dose radiation environments [17, 18]. Nevertheless, there were not enough data to create a faithful computer simulation model. Also, there were no detailed experiments that could quantify the circuit's post-irradiation response.

In order to provide a wider picture on the radiation and post-irradiation effects in the L4940V5 voltage regulator, various isothermal annealing procedures were implemented. After long-term room temperature annealing, two short-term isothermal annealing procedures were performed. Also, a computer simulation model was developed in order to model the response of the vertical serial PNP power transistor. These combined efforts should enable the acquisition of comprehensive knowledge on the L4940V5 voltage regulator's radiation response.

2 Theory

2.1 Radiation effects

Ionising radiation affects silicon bipolar junction transistors mainly through the mechanisms of charge-trapping, both in the oxide and on the semiconductor-oxide interface [14, 22]. The excess base current is the most important measure of the radiation-caused degradation of the bipolar junction transistor. It represents the difference between the base current measured after irradiation (I_B) and the base current prior to irradiation (I_{B0}) [14]:

$$\Delta I_B = I_B - I_{B0} \tag{1}$$

The base current has two components, the ideal one (I_{Bi}), affecting the transistor's current gain, and the recombination component (I_{Br}), being the current of only the internal recombination processes in the base area [8, 23]:

$$I_B = I_{Bi} + I_{Br} = I_S e^{\frac{V_{EB}}{nV_T}} + I_{Se} e^{\frac{V_{EB}}{n_e V_T}} \tag{2}$$

where: I_S – transport saturation current [24], I_{Se} – emitter-base leakage current, V_{EB} – emitter-base voltage, V_T – thermal voltage (being 26 mV at the room temperature of 20°C), n – ideality factor of the ideal base current, n_e – ideality factor of the recombination base current (or, in SPICE models, emitter-base leakage emission coefficient [24]).

Excess base current may be presented as the difference between the pre-irradiation and post-irradiation base currents. The detailed relation for the excess base current is [25]:

$$\Delta I_B = \frac{1}{2} q n_i P_E \left[s'' x_{dB} e^{\left(\frac{V_{eff}}{2V_T}\right)} - s' W_d e^{\left(\frac{V_{EB}}{2V_T}\right)} \right] \tag{3}$$

where: s' – pre-irradiation surface recombination velocity, s'' – post-irradiation surface recombination velocity, W_d – width of the depletion area in the base-emitter area prior to irradiation, q – elementary electron charge ($1.6 \cdot 10^{-19}$ C), n_i – intrinsic carrier concentration in silicon, x_{dB} – location of the depletion region at the surface of the base, P_E – emitter perimeter, V_{eff} – effective voltage (used in place of V_{EB}, in order to include the influence of the oxide-trapped charge on the total voltage on the emitter-base junction) [25]. The excess base current rises proportionally to the difference of the surface recombination velocities existing prior to and after the exposure to ionising radiation. For a heavily-doped emitter and low emitter-base voltage (up to 0.6 V) [26], the excess base current may be considered to be directly proportional to the increase of the concentration of interface traps [26, 27]. Nevertheless, the excess base current cannot be affected only by the interface traps. The influence of the oxide-trapped charge is particularly important in the cases when the emitter was not heavily doped. Build-up of the oxide-trapped charge will increase the surface potential of the P-type emitter area [25]. Therefore, the surface recombination velocity depends on both the interface traps and the oxide traps.

The ideality factor for the ideal base current is $n = 1$, but its value is not constant for the recombination current. Usually, the ideality factor of the recombination current is considered to be $n_e = 2$, the same as during the normal operation of the transistor with a high emitter injection level [22]. Nevertheless, in reality, the re-

combination current ideality factor has variable values between 1 and 2. Despite the long-known fact that the ideality factor is dependent on the applied base-emitter voltage [26], this fact is neglected in standard computer simulation models.

In NPN bipolar transistors, the P-type base, right beneath the isolation oxide, is the most sensitive area. The reason is the relatively low doping concentration of the P-base, in comparison with the N-type collector and emitter. Both oxide-trapped charge and interface traps would negatively affect the P-type base, causing a rise in the excess base current [23]. On the other hand, in PNP transistors, the N-type base is not so endangered, since the positive oxide-trapped charge will cause the electrons to accumulate in the base area, suppressing the negative effects of the interface traps during the initial phase of irradiation [25]. If the emitter area is not heavily implanted, it will be the area most affected by the influence of radiation, experiencing the negative influence of both interface traps (increasing the surface recombination in silicon) and oxide traps (causing the depletion of the emitter area beneath the oxide) [28]. Mutually, these effects cause the depletion region on the base-emitter junction to spread deep into the emitter area, affecting the rise in the excess base current [28]. The mentioned effects depend on many factors, such as doping concentrations, the geometry of the transistors, the quality of oxides and passivation layers, etc.

During the exposure to radiation of the silicon bipolar junction transistors, the initial phase will be dominated by the influence of the oxide-trapped charge [25]. At the same time, the concentration of the charge trapped at the interface between the silicon and silicon-dioxide will rise much more slowly, affecting the rise in the excess base current almost proportionally to the total absorbed dose [25]. Yet, after some time has elapsed in the ionising radiation field, the surface recombination velocity will reach its limit and the excess base current will enter the saturation phase.

2.2 Annealing

Stability of defects in semiconductors and oxides, caused by radiation, depends on time, electric field and temperature [22]. Thus, a concentration of defects in materials may significantly change after irradiation, with tendency to substantially reduce in high-temperature ambient [22]. Depending on the nature of radiation and trapped charge (both in oxide and a semiconductor-oxide interface), bipolar transistors may partially recover or even further degrade its characteristics. Analysis of post-irradiation, time-dependent effects should provide a more detailed insight into the radiation response of the circuits exposed. Thermal excitation usually leads to a significant defect annealing at temperatures of 100°C and greater, while the tunneling is a dominant effect at a room temperature [22]. Several procedures were usually used, based either on isothermal [14] or isochronal [22] annealing. Isothermal annealing procedures are performed at a constant temperature (either room or elevated) [14], and this approach often enables a qualitative evaluation of the radiation-induced defects. On the other hand, isochronal annealing is performed with constant, successive time intervals [22], usually much shorter than the ones used for isothermal examinations. Isothermal annealing is a more realistic test procedure, since it may simulate a real exploitation conditions, in periods from one day up to several years. On the other hand, isochronal annealing procedures may involve high temperatures, yet in much shorter time intervals (in order of minutes).

According to the published data [29], some integrated circuits showed annealing of the trapped holes from the oxide after the end of the elevated temperature (100°C) isothermal annealing, without a significant effect on the interface traps. Therefore, it would be possible for some devices to express radiation-induced degradation originating only from the influence of interface traps [29]!

3 Materials and methods

Analysis of irradiation and isothermal annealing effects was performed on integrated 5-volt, positive voltage regulators *STMicroelectronics*® L4940V5. Samples were irradiated in the ^{60}Co ionising radiation field in the Vinča Institute of Nuclear Sciences, Belgrade, Serbia, in the Metrology-Dosimetry Laboratory [17-19]. The devices absorbed total γ-radiation doses of 500 Gy(SiO_2), at a dose rate of 4 cGy(SiO_2)/s [20, 21]. For nearly ten years, the irradiated samples were kept in the office locker, at a room temperature always kept in the range 15–25°C.

After 85,000 hours, all the samples of voltage regulators were tested in the same conditions as immediately after the irradiation, with a room temperature of 20°C. Shortly afterwards, the L4940V5 voltage regulators were examined to see if it would be possible to recover most of the oxide-trapped charge after one-week's annealing at the temperature of 100°C, with a negligible effect on the interface traps. Consequently, another one-week annealing at 150°C should lead to the complete recovery of all the radiation-induced oxide-trapped charge and most of the interface traps.

The primary examined parameters were the voltage regulator's maximum output current, the serial transis-

tor's minimum dropout voltage and the total circuit's quiescent current. Measurement of the quiescent current enabled the calculation of the serial transistor's base current and, consequently, the serial transistor's forward emitter current gain [18, 20, 21]. Voltage and current vaweforms were recorded using the oscilloscope *Fluke*® 196C.

Several days after completion of the room-temperature annealing experiment, the circuits were annealed in the thermal chamber, at a temperature of 100°C, uninterruptedly for 168 hours. After the seven-day annealing, a new round of experiments was performed, with the same electrical parameters recorded. Finally, a day after the completion of the second round of electrical measurements, a final isothermal annealing sequence was performed, for another 168 hours with the same samples in the thermal chamber, yet this time at a temperature of 150°C. After the completion of the last annealing phase, the final data set on annealed voltage regulators was recorded. The presented sequence of isothermal annealing procedures, with the various temperatures and durations, should enable better insight into the influence of interface traps and the oxide-trapped charge on the radiation and post-irradiation response of a complex integrated circuit. Ten years should be a typical exploitation period for the electronic components in aerospace applications [22].

Since the manufacturer of the circuit L4940V5 did not provide the schematic circuit diagram of this voltage regulator, many efforts were made to gather the necessary data on the internal structure of this device. Using the published papers [30, 31] and patents [16, 32], the author created a basic computer simulation model in the program "LTspice IV" [33]. The created model was rigorously examined and improved until it enabled a pretty good recreation of a wide ensemble of experimental results. There was no intention to recreate all the details of the integrated circuit as made by its manufacturer, so it is not a straight replica of the particular circuit design. Yet, the presented simulation model was good enough to describe the circuit's response to the influence of γ-radiation.

In order to present the circuit's response for various bias and load conditions, previously published results were unified with the data from new experiments. The data on the mean values of the maximum output current [17, 18], minimum dropout voltage [20, 21] and on-line parameters [19, 34], procured immediately after the exposure of the L4940V5 devices, were extensively presented in previous years. However, new experiments on the isothermal annealing of the voltage regulator were done on the same samples, yet this time ten years later. So, in order to avoid the unnecessary repetition of the old data, mostly results normalised to the data on virgin devices are now presented. Yet, the creation of the computer simulation model, as well as in-depth analysis of the perceived radiation effects, was not possible without unification of all the experimental data obtained.

Descriptions of the experiments performed, the radiation sources, and the procedures implemented for procurement of the circuit's electrical parameters are in the detail provided in the references [17–21, 34, 35].

4 Results

Table 1 summarises the results on maximum output current and minimum dropout voltage (for load currents of 100 mA and 400 mA), obtained in the γ-radiation field with various biases and loads during irradiation. From the data on the quiescent current in the examined circuits, as well as from data on unloaded voltage regulators, the values of the serial transistor's base current and the internal control circuit's consumption were calculated (in a positive voltage regulator with the PNP pass transistor, total quiescent current represents the sum of these two currents [18, 21]). Consolidated results were presented, showing, firstly, data on unexposed circuits, then the data procured after absorption of total doses from 50 Gy up to 500 Gy, and, finally, the data procured during the isothermal annealing (long-term room-temperature, followed by short-term 100°C and 150°C annealing). Only the most important data necessary for the circuit response analysis are presented in the table, and all data were normalised to the values of virgin devices. Therefore, since the data on unloaded voltage regulators had basically the same trends in all three cases, only data obtained during the examination of the maximum output current are presented.

As previously reported on its radiation response [17-21], and being valid also following the implemented annealing of the tested circuits, the voltage regulator kept stable output voltage in all the examined operating points, regardless of the bias conditions during previous irradiation. The voltage reference circuit suffered negligible degradation, since the variations of the output voltage in unloaded devices could be measured in millivolts [21, 34]. The waveforms of the input voltage, output voltage and quiescent current, recorded on the laboratory setup, were presented in Fig. 1. Despite the high alternate current components, measured values of direct current enabled successful evaluation of the voltage regulator's radiation response.

Table 1: Relative values of serial transistor's dropout voltage (V_{EC12}; for tests with load current of 100 mA and 400 mA), maximum output current (I_{max}) and no-load quiescent current (I_{Q0}), as well as the accompanying data on the absolute values of the serial transistor's excess base current (ΔI_{B12}) in voltage regulator *STMicroelectronics*® L4940V5. Values were based on data recorded on virgin devices, during the exposure, and after irradiation, for the specified periods and types of isothermal annealing. Experimental results were extended with parameters of the serial transistor (maximum forward emitter current gain (β_{Fmax}) and knee current (I_{kF})), defined in the SPICE simulation models. Simulation models with serial PNP power transistors, having the parameters specified in the last two columns, were ones that reached high agreement with the data procured through all three types of experiment. Successive periods of isothermal annealing were marked as follows: annealing 1 (Θ_a = 20°C, t = 85,000 hours); annealing 2 (Θ_a = 100°C, t = 168 hours); annealing 3 (Θ_a = 150°C, t = 168 hours). Basic values of serial transistor's dropout voltage, base current and no-load quiescent current, experimentally procured on unexposed (D = 0 Gy) L4940V5 voltage regulators, for various bias and load conditions: a) 0 V, 0 A: V_{EC12} (100 mA) = 0.355 V [20], I_{B12} (100 mA) = 0.545 mA [20], V_{EC12} (400 mA) = 1.766 V [21], I_{B12} (400 mA) = 4.627 mA [21], I_{max} = 835.9 mA [18], I_{Q0} = 3.753 mA [18], I_{B12} (max) = 20.397 mA [18]; b) 8V, 1 mA: V_{EC12} (100 mA) = 0.394 V [20], I_{B12} (100 mA) = 0.703 mA [20], V_{EC12} (400 mA) = 1.736 V [21], I_{B12} (400 mA) = 3.824 mA [21], I_{max} = 855.1 mA [18], I_{Q0} = 3.772 mA [18], I_{B12} (max) = 19.028 mA [18]; c) 8 V, 100 mA: V_{EC12} (100 mA) = 0.392 V [20], I_{B12} (100 mA) = 0.734 mA [20], V_{EC12} (400 mA) = 1.763 V [21], I_{B12} (400 mA) = 4.417 mA [21], I_{max} = 852.5 mA [18], I_{Q0} = 3.806 mA [18], I_{B12} (max) = 25.304 mA [18]; d) 8 V, 500 mA: V_{EC12} (100 mA) = 0.378 V [20], I_{B12} (100 mA) = 0.731 mA [20], V_{EC12} (400 mA) = 1.793 V [21], I_{B12} (400 mA) = 5.638 mA [21], I_{max} = 820.5 mA [18], I_{Q0} = 3.806 mA [18], I_{B12} (max) = 25.304 mA [18].

STMicroelectronics® L4940V5		Type of experiment										Simulation	
Operation during irradiation and annealing		V_{EC12} (100 mA)			V_{EC12} (400 mA)			Imax				Parameters of serial PNP power transistor, Q_{12}	
Bias and load during irradiation	Dose, D [Gy]	V_{EC12} [p.u.]	I_{B12} [p.u.]	ΔI_{B12} [mA]	V_{EC12} [p.u.]	I_{B12} [p.u.]	ΔI_{B12} [mA]	I_{max} [p.u.]	I_{Q0} [p.u.]	I_{B12} [p.u.]	ΔI_{B12} [mA]	β_{Fmax}	I_{kF} [A]
0 V 0 A	0	1	1	0	1	1	0	1	1	1	0	270	0.225
	50	1.161	2.422	0.78	1.153	1.813	3.76	0.995	0.981	1.44	8.98	115	0.375
	100	1.144	4.128	1.71	1.208	3.395	11.08	0.956	0.959	1.760	15.49		
	500	1.631	75.43	40.57	1.298	7.478	29.98	0.966	0.874	1.997	20.34		
	Annealing 1	1.27	3.996	1.63	1.265	3.127	9.84	0.862	0.933	2.118	22.8		
	Annealing 2	1.087	3.486	1.36	1.067	2.669	7.72	0.916	0.965	1.567	11.56	67	0.49
	Annealing 3	1.234	2.312	0.64	1.08	1.659	1.82	0.898	0.967	1.28	5.71	125	0.38
8 V, 1 mA	0	1	1	0	1	1	0	1	1	1	0	340	0.225
	50	1.023	1.55	0.39	1.11	1.349	1.34	0.999	0.986	1.089	1.7	180	0.375
	100	0.990	2.119	0.79	1.139	1.938	3.59	0.993	0.976	1.435	8.27	115	0.425
	200	1.000	3.599	1.83	1.127	3.894	11.07	0.980	0.954	1.785	14.94	45	1.1
	300	1.003	5.747	3.34	1.242	6.859	22.41	0.974	0.938	1.870	16.55		
	500	1.251	27.89	18.91	1.347	8.567	28.94	0.958	0.917	1.904	17.2		
	Annealing 1	1.071	5.334	3.05	1.395	7.377	24.39	0.894	0.936	2.27	17.2		
	Annealing 2	1.071	3.115	1.49	1.187	2.712	6.55	0.937	0.962	1.904	11.71	60	0.7
	Annealing 3	1.198	1.508	0.36	1.181	1.42	1.61	0.946	0.973	1.616	2.57	150	0.39
8 V, 100 mA	0	1	1	0	1	1	0	1	1	1	0	340	0.225
	50	1.028	1.88	0.65	1.132	1.607	2.68	0.992	0.983	1.377	6.82	127	0.375
	100	0.987	3.011	1.48	1.161	2.719	7.59	0.968	0.967	1.723	13.08	55	0.75
	200	1.031	6.131	3.77	1.243	7.19	27.34	0.961	0.941	2.027	18.57		
	500	1.372	57.96	41.81	1.284	8.021	31.01	0.954	0.899	2.202	21.73		
	Annealing 1	1.372	11.38	7.62	1.336	7.63	29.28	0.891	0.922	2.065	19.26		
	Annealing 2	1.092	3.856	2.1	1.221	3.337	10.32	0.967	0.951	1.829	14.99	45	1
	Annealing 3	1.115	1.703	0.52	1.188	1.535	2.36	0.934	0.967	1.326	5.9	120	0.4
8 V, 500 mA	0	1	1	0	1	1	0	1	1	1	0	240	0.2
	50	0.971	1.929	0.68	1.085	1.591	3.33	1.007	0.98	1.164	4.15	100	0.375
	100	1.011	3.010	1.47	1.153	2.914	10.79	0.999	0.962	1.289	7.32		
	500	1.704	54.56	39.15	1.267	6.297	29.86	1.01	0.909	1.427	10.8		
	Annealing 1	1.235	13.42	9.08	1.35	5.692	26.45	0.932	0.943	1.432	10.42		
	Annealing 2	1.103	3.844	2.08	1.25	3.663	15.01	0.969	0.956	1.368	9.32		
	Annealing 3	0.997	1.696	0.51	1.161	1.453	2.55	0.942	0.967	1.148	3.76	105	0.375

Basic data on the vertical serial PNP power transistor, obtained using the SPICE simulations, are also included in Table 1. Since the previous research concluded that the control circuit did not have a significant influence on the voltage regulator's radiation response [20, 21], the focus of the computer simulation analysis was on the serial power transistor. The primary influence on the L4940V5 voltage regulator's radiation hardness was the interdigitated structure of its serial PNP transistor [17, 19]. Therefore, the serial power transistor's excess base current was the best measure of the circuit's radiation response.

After careful examination, the results from Table 1 may provide much information about the L4940V5 circuit's radiation and post-irradiation response. All the irradiated circuits expressed lower recovery (from deposition of the total dose of 500 Gy) during the ten-year room-temperature annealing than during the two seven-day high-temperature annealing sequences. Recovery of the circuits after two-week isothermal annealing was not complete, yet the main parameters pointed to circuit damage comparable to the state recorded after the absorption of the total ionising dose of 50 Gy.

Variations of the serial power transistor base current, presented in Table 1, may lead to the identification of two different circuit responses, for the irradiation and post-irradiation periods. The first category of results comprises the initial period of irradiation (up to 50 or 200 Gy, depending on the bias and load conditions), as well as the final periods of high-temperature isothermal annealing. The second category of results comprises the data procured after absorption of higher total doses, as well as the initial annealing periods (particularly the long-term, room-temperature annealing). The main means of identification of these categories is the saturation of the serial transistor's base current, in either of the three data ensembles. The threshold value of the base current, when overcurrent protection is activated, is approximately 35 mA. This value corresponds to the total voltage regulator's quiescent current of nearly 40 mA. When the serial transistor base current is always less than 35 mA, the radiation response of the PNP bipolar power transistor can be modelled with the standard Gummel–Poon model, with variations of only the maximum forward emitter current gain and the knee current. On the other hand, whenever the base current exceeded this threshold voltage, the SPICE model, successfully describing the circuit response for all three types of experiment, could not be made. In some cases, the power transistor base current was higher in control points with the collector current being 100 mA, than in the case when the collector current was 400 mA!

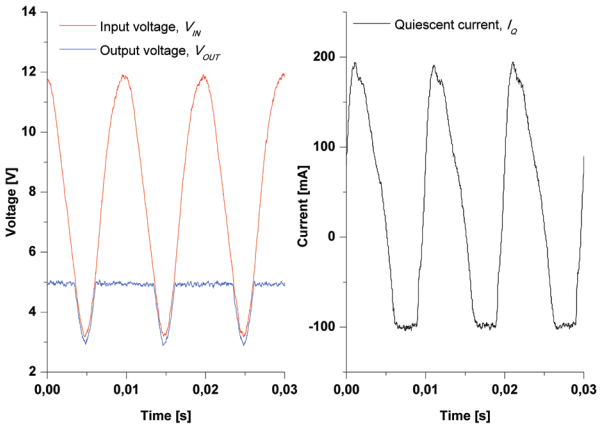

Figure 1: Waveforms of input and output voltage (left) and quiescent current (right), recorded on the unexposed L4940V5 voltage regulator during the examination of the maximum output current

The bias conditions had a great influence on the radiation response of the irradiated circuits. Data from Table 1 show opposite trends of the radiation response of the power transistor, on the one hand, and the rest of the circuit, on the other. While the serial transistor's base current increased, increasing also the voltage regulator's quiescent current, the quiescent current of the control circuit (I_{Q0}) declined [21]. Yet, the primary focus was on the examination of the characteristics of the vertical power transistor, since it had the most obvious effect on the voltage regulator radiation response. So, analysing the variations of the excess base current, shown in Table 1, the clear scale of the radiation sensitivity of exposed circuits may be defined. Gamma-radiation inflicted the greatest damage on biased and heavily loaded voltage regulators (V_{in} = 8 V, I = 500 mA). Lower degradation was seen in unbiased devices, followed by even lower degradation in biased and moderately loaded voltage regulators (V_{in} = 8 V, I = 100 mA). The least damage was expressed by biased and negligibly loaded devices (V_{in} = 8 V, I = 1 mA).

The waveforms of the quiescent current and output current recorded on the laboratory setup are presented in Fig. 1.

5 Discussion

5.1 Computer simulation

Fig. 2 presents a simplified computer simulation model of the L4940V5 voltage regulator, created in the program tool "LTspice IV" [33]. As can be seen from Fig. 2, the voltage reference and the error amplifier were represented only by general models. On the other hand,

the simulation model of the serial PNP power transistor, Q12, was very complex. The main reason is the negligible radiation degradation of the control circuit elements, in opposition to the serious degradation of the serial power transistor. Due to its strong influence on the results obtained, the model included many details on the power supply circuit and the accompanying cables.

Due to the low value of the main filter capacitor (nominally 330 μF), the examined voltage regulators operated in two periods: with the constant output voltage and with its decreased value, falling below the nominal value of 5 V (see Fig. 1). Therefore, the integrated circuit's quiescent current had very rapid variations in these two operation sequences. Also, since the local ground of the examined voltage regulator was separated from the power supply ground by a cable, 10 m long, it also increased the alternating current component of the voltage regulator's quiescent current. In the period of 10 ms, matching the inherent frequency of the single-phase diode bridge, there was, de facto, operation of the voltage regulator with the dominant alternating current superimposed on its direct current component. Relatively low values of the maximum output current (being 720– 850 mA), as well as high values of the minimum dropout voltage, are a direct consequence of the low capacity of the main filter capacitor. Nevertheless, the experimental configuration was not changed, in order to enable mutual comparison of all the obtained and presented data, dating back to 2006 [17]. Yet, even in these circumstances, measurement of the mean values of quiescent currents led to the correct calculation of the serial power transistor's base current and its forward emitter current gain. Despite the high alternate current components, the computer simulation proved that the measured values of direct current, presented in tables 1 and 2, enabled successful evaluation of the voltage regulator's radiation response.

The reaction of the anti-saturation circuit was also important, since it had a substantial influence on the quiescent current response. Whenever the dropout voltage on the pass PNP transistor fell below the threshold level, the anti-saturation circuit reacted in order to prevent the flow of excessive current from the serial transistor to the substrate and, consequently, to the ground contact. Therefore, the anti-saturation circuit was modelled in great detail.

Another important element was the overcurrent protection of the driver NPN transistor, Q13. In order to prevent the voltage regulator's quiescent current rising above its upper limit of 50 mA [15], the transistor Q15 activates and takes the excessive collector current of the driver transistor, indirectly limiting the base current of the serial transistor. The consequence of this protection is the reduction of the voltage regulator's maximum output current. This was exactly the circuit response that was recorded in numerous experiments, particularly after the absorption of the higher total doses of γ-radiation.

As the basic element for modelling the serial vertical PNP power transistor, the SPICE model of discrete transistor BC808-25 was used [36]. This is a discrete PNP transistor with the following nominal parameters: collector–emitter breakdown voltage BV_{CE0} = 25 V, nominal collector current I_C = 500 mA, cut-off frequency f_T = 100 MHz, with the maximum value of the forward emit-

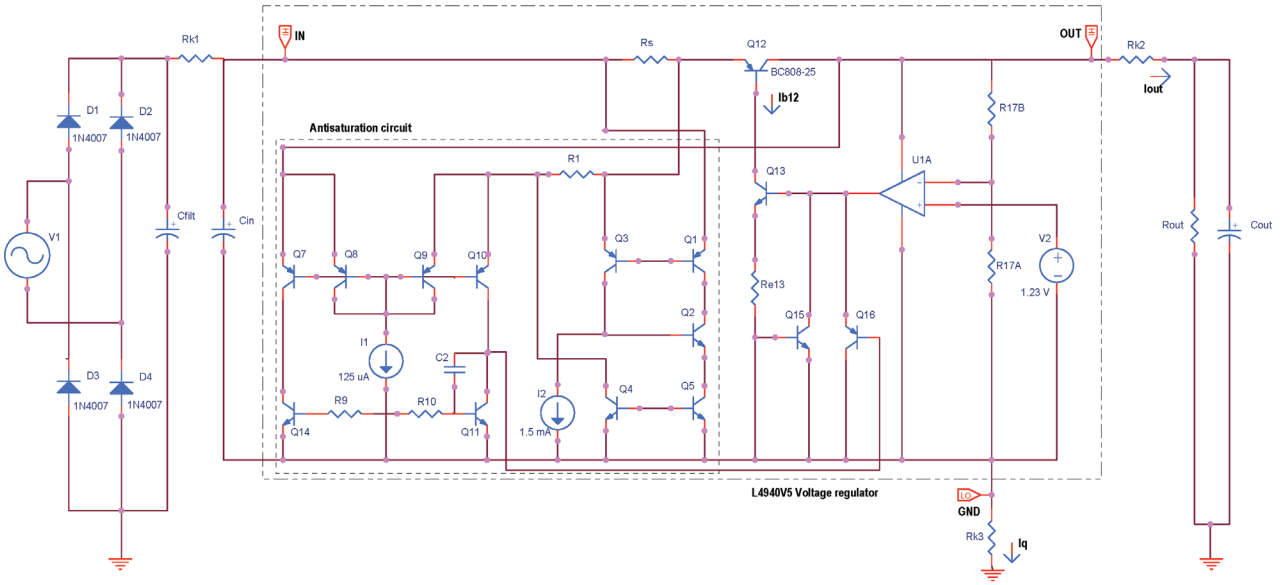

Figure 2: Schematic circuit diagram of L4940V5 voltage regulator

ter current gain being in the range β_F = 160–400 [37]. These data are close to the specified characteristics of the vertical PNP power transistor in device L4940V5 (f_T = 80 MHz, β_F = 50 for the load of 1 A, BV_{CE0} = 20 V) [15, 30].

Table 2 enables mutual comparison of simulation and experimental data on the serial transistor's base current. Simulation data on parameters variations of the vertical serial PNP power transistor are also included in Table 1. Transistor parameters were selected in order to enable the highest possible agreement with the results for all three types of experiments. In the initial period of irradiation, for total ionising doses from 0 Gy up to 200 Gy, the simulation model reproduced the experimental results very well. In the initial phase, a sharp decline of the forward emitter current gain was seen for all the tested operation conditions [17-21]. This decline was successfully modelled in the computer simulation using just the variations of the maximum forward emitter current gain (β_{Fmax}) and the forward knee current (I_{kF}). Variations of the current gain and the excess base current were most successfully modelled for the biased and negligibly loaded voltage regulators. For other devices, both unbiased or biased and loaded with higher currents, procuring a faithful simulation model was much more difficult. Without exception, when the devices reached saturation of the excess base current, precise modelling was impossible. Unbiased and heavily loaded circuits L4940V5 entered this phase after the absorption of low total doses (50 Gy), while the biased and negligibly loaded devices experienced saturation after longer exposure (200 Gy).

Table 2: Mutual comparison of absolute values of serial transistor's base current (I_{B12}) in voltage regulator *STMicroelectronics*® L4940V5, obtained both with SPICE simulation and experiment. Experiments were executed on variations of dropout voltage (V_{EC12}; for tests with load current of 100 mA and 400 mA) and maximum output current (I_{max}), for absorption of total ionising doses up to 500 Gy(SiO_2). The results were extended with parameters of the serial transistor (maximum forward emitter current gain (β_{Fmax}) and knee current (I_{kF})), defined in the SPICE simulation models. Only experimental results that reached high agreement with simulation models were presented. Successive periods of isothermal annealing were marked as follows: annealing 2 (Θ_a = 100°C, t = 168 hours); annealing 3 (Θ_a = 150°C, t = 168 hours).

STMicroelectronics® L4940V5		Simulation and experiment						Simulation	
Operation during irradiation and annealing		V_{CE12} (100 mA)		V_{CE12} (400 mA)		I_{max}		Parameters of serial PNP power transistor, Q_{12}	
Bias and load during irradiation	Dose, D [Gy]	Simulation	Experiment [20]	Simulation	Experiment [21]	Simulation	Experiment [18]	β_{Fmax}	I_{kF} [A]
		I_{B12} [mA]	I_{B12} [mA]	I_{B12} [mA]	I_{B12} [mA]	I_{B12} [mA]	I_{B12} [mA]		
0 V 0 A	0	0.72	0.55	4.67	4.63	20.77	20.4	270	0.225
	50	1.18	1.32	7.72	8.39	27.77	29.38	115	0.375
	Annealing 2	1.88	1.9	11.39	12.35	32.44	31.96	67	0.49
	Annealing 3	1.1	1.18	7.06	6.45	21.57	26.1	125	0.38
8 V, 1 mA	0	0.89	0.7	4.03	3.82	19.06	19.03	340	0.225
	50	1.08	1.09	5.17	5.16	21.53	20.73	180	0.375
	100	1.36	1.49	7.33	7.41	27.73	27.3	115	0.425
	200	2.5	2.53	12.39	14.89	34.39	33.97	45	1.1
	Annealing 2	1.98	2.19	10.85	10.37	31.11	30.74	60	0.7
	Annealing 3	0.94	1.06	5.8	5.43	20.67	21.6	150	0.39
8 V, 100 mA	0	0.89	0.73	4.03	4.42	19.06	18.07	340	0.225
	50	1.09	1.38	7	7.1	26.32	24.89	127	0.375
	100	2.14	2.21	11.51	12.01	33.87	31.15	55	0.75
	Annealing 2	2.52	2.83	12.72	14.74	35.21	33.06	45	1
	Annealing 3	1.13	1.25	7.14	6.78	24.22	23.97	120	0.4
8 V, 500 mA	0	0.79	0.73	5.7	5.64	23.23	25.3	240	0.2
	50	1.35	1.41	8.86	8.97	30.62	29.45	100	0.375
	Annealing 3	1.29	1.24	8.42	8.19	26.31	29.06	105	0.375

Partially unexpected were data on the long-term room-temperature annealing. Initial checks of several irradiated samples led to the assumption that, in the long-term perspective, irradiated L4940V5 voltage regulators would mostly recover [21]. Nevertheless, data obtained after 85,000 hours of room-temperature annealing did not support this hypothesis [34]. Despite the recovery of the serial transistor current gain and reduction of its excess base current, the maximum output current in most cases significantly declined. Yet, two successive one-week, high-temperature annealing sequences (100°C, followed by the 150°C exposure) led to the expressed circuit recovery. In all the examined cases, high-temperature annealing of devices irradiated until absorption of the total dose of 500 Gy led to nearly the same parameters as those recorded after absorption of 50–200 Gy. More important, these conditions could be again successfully modelled only with variations of the current gain and knee current of the serial transistor, just as in the initial period of irradiation.

5.2 Radiation effects

As can be expected from the theory [38], unbiased devices suffer the most obvious damage, while bipolar intergated circuits with a high positive bias voltage during irradiation show much less degradation from the influence of radiation. On the one hand, this could be expected, since the high positive bias voltage injects the electrons in oxide, causing the trapped holes to recombine and consequently reducing the total oxide-trapped charge concentration. Yet, unbiased irradiation cannot enhance the hydrogen ions transport and, therefore, will have less influence on the build-up of interface traps.

A sharp initial decline of the forward emitter current gain, presented in Table 1, points to the dominant influence of the oxide-trapped charge. The current gain declined rapidly, as presented in Table 1 and the maximum value of the forward emitter current gain decreased from 340 down to 55 (for biased and moderately loaded devices), following exposure to only 100 Gy. Also, at the same time the serial PNP power transistor's knee current significantly increased, rising from 0.225 A to 0.75 A. The emitter-base leakage emission coefficient, used in the simulation model of the transistor BC808-25 and, therefore, of the power vertical PNP transistor used in the present simulation, was a constant with a value n_e = 1.568 [36]. Other voltage regulator elementary circuits were not seriously affected by ionising radiation, so the remaining elements of the simulation model were not changed.

This initial rapid degradation of the serial transistor current gain clearly points to the main negative influence of the oxide-trapped charge. Yet, in the previous research it was calculated that the emitter area has a surface doping concentration equal to $3.3 \cdot 10^{17}$ cm^{-3} [21]. This is a relatively high value for a PNP power transistor, and it was therefore assumed that the emitter should not be so much affected by the influence of the oxide-trapped charge, particularly since the emitter crowding was not perceived [21]. Nevertheless, despite such a high impurities concentration for a power device, this value was not so high, particularly in comparison with a small-signal PNP transistor, having an emitter doping concentration up to 10^{20} cm^{-3} [28]. Also, the interdigitated structure of the pass element, with 40 elementary PNP power transistors [30], was another reason for its lower radiation tolerance. Therefore, the main reason for such an obvious rise in the excess base current was certainly primarily related with the emitter, rather than the base area.

After the initial phase of radiation exposure, the next phase showed saturation in the serial PNP transistor's excess base current, particularly after exposure of the samples to 500 Gy [18, 20, 21]. These results point to the reaction of the overcurrent protection of the NPN driver transistor Q13 (Fig. 2), preventing the rise of the voltage regulator's quiescent current above the foreseen maximum of 50 mA [15]. Saturation in the oxide-trapped charge build-up was always perceived for high total doses, being 500 Gy (with the exception of the biased and negligibly loaded samples). Yet, the problem is that it was not possible to create an adequate computer simulation model of the PNP power transistor for higher total doses! Whatever was implemented in the SPICE model of the serial transistor, it was not possible to get mutually faithful results for either the maximum output current (I_{out} = 720 – 850 mA) or the minimum dropout voltages (recorded for 100 mA and 400 mA) using the basic Gummel–Poon models. There were earlier attempts to simulate the increased recombination current in the base area, with the ideality factor of 2 [8]. Other tools, such as additional resistors, current sources, variations of the surface recombination currents or the other power transistor parameters did not help much. The most successful attempt was made with the implementation of a significantly increased base-emitter saturation leakage current (I_{se}). Yet, even in these cases, it was not possible to alter one simple fact: regardless of the output current (100 mA, 400 mA or 800 mA), for a dose of 500 Gy, the base currents were, in most cases, nearly the same, being 35–40 mA. Nevertheless, even with this saturation of the base current, the experiment indicated that the voltage regulator operated correctly, without significant degradation of its output voltage and with only a moderate decline of the maximum output current at some control points. The exponential dependence of the base current on

the emitter-base voltage, accompanied by the successful simulation of the voltage regulator response with high output currents, could not be realised. So, despite the variations of either the emitter-base leakage current (I_{se}) or the emitter-base leakage emission coefficient (n_e), a satisfactory simulation model suitable for the description of the high total-dose response could not be created.

5.3 Post-irradiation effects

Data on the ten-year room-temperature annealing, presented in Table 1, point to a significant recovery of the serial transistor's excess base current, hand in hand with further degradation of the maximum output current and, in some cases, minimum dropout voltage. More important, saturation of the excess base current remained present during the examination with higher currents, making it impossible to create faithful SPICE models of the first phase of annealing. Tremendous recovery of the excess base current may be observed particularly in unbiased devices, reducing the serial transistor's base current nearly twentyfold! Also, in this, the most obvious case, the maximum output current, i.e. the serial transistor collector current, significantly declined. Various previous studies emphasize that, at room temperature, oxide-trapped charge anneals with time, contributing to the recovery of current gain [25], while interface traps in the field oxide often do not anneal [39]. Thus, it may be assumed that, following the ten-year room temperature annealing of the L4940V5 voltage regulators, the oxide-trapped charge partially recovered, while the interface-trapped charge continued to build up. Therefore, the power transistor's current gain recovery was primarily affected by the positive influence of the recovery of the oxide-trapped

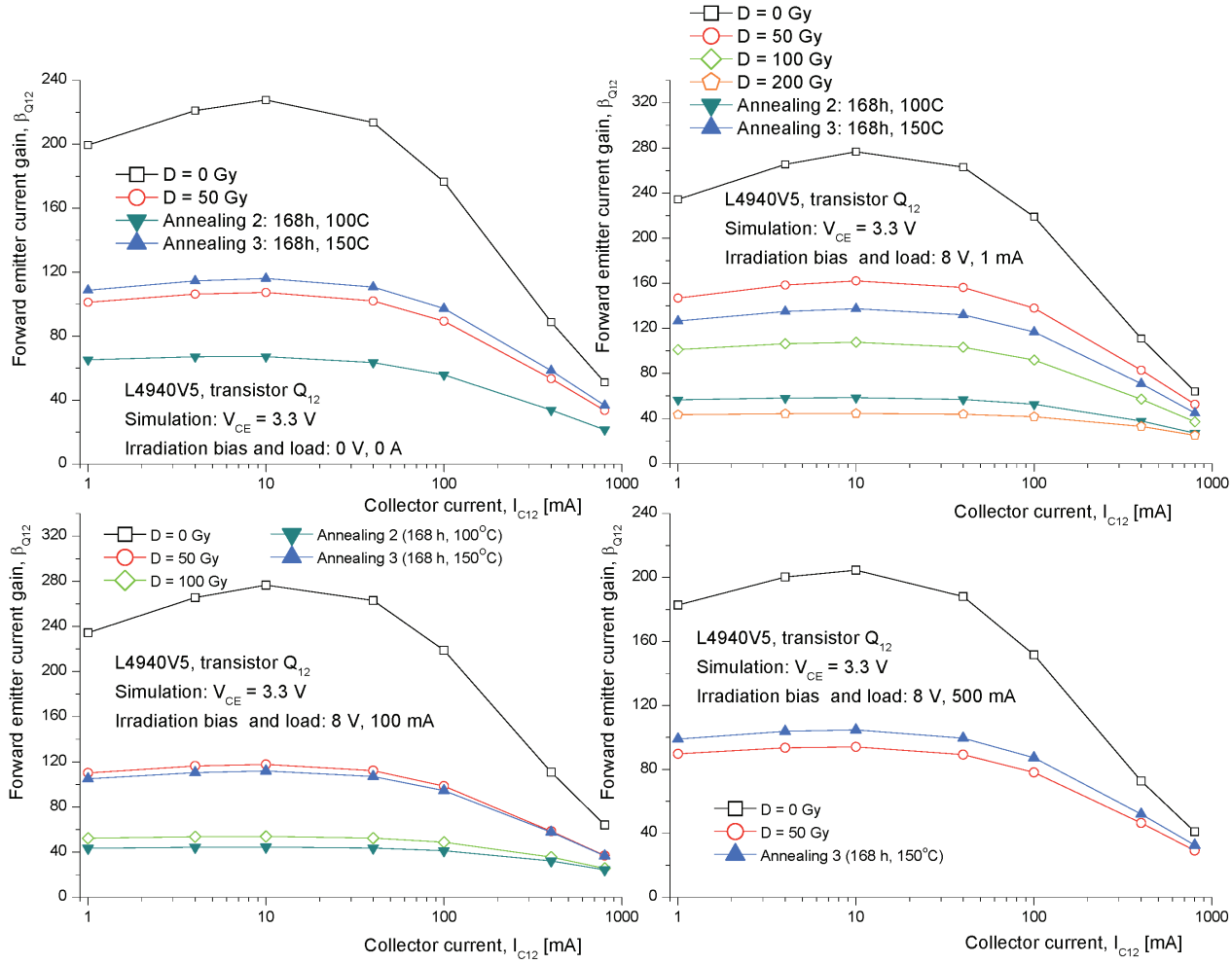

Fig. 3. Variations of the power PNP transistor current gain as a function of the collector current in: a) unbiased circuits (V_{in} = 0 V, V_{out} = 0 A); b) biased and negligibly loaded (V_{in} = 8 V, V_{out} = 1 mA); c) biased and moderately loaded (V_{in} = 8 V, V_{out} = 100 mA); d) biased and heavily loaded circuits during irradiation (V_{in} = 8 V, V_{out} = 500 mA). Diagrams were created for constant collector–emitter voltage, being V_{CE} = 3.3 V. Data were obtained from computer simulation models of the irradiated and annealed voltage regulators, which demonstrated high agreement with the experimental results presented in Table 1.

charge. The negative influence of further interface traps build-up, causing the serial transistor's collector current to decline, had a much less obvious effect on its forward emitter current gain.

The first high-temperature annealing sequence, including one-week at 100°C exposure, reduced the radiation damage to a level slightly above the one observed following the 100-Gy irradiation. The second sequence, involving 168-hour annealing at 150°C, further reduced the radiation damage down to the degradation caused by the total ionising dose of 50 Gy. With the exception of the samples that were heavily loaded during the irradiation, the voltage regulators' characteristics, following the high-temperature annealing sequences, could be successfully modelled, in the same way it was done in the initial phase of irradiation, using the variations of only the current gain and knee current. No sign of heavy saturation was observed in the forward emitter current gain after exposure to higher total doses of γ-radiation. Data on the short-term, high-temperature annealing pointed to a substantial recovery of the irradiated circuits, bringing them close to their pre-irradiation characteristics. Nevertheless, the data in Table 1 show that β_{Fmax} recovered only to 40–50 % of their pre-irradiation values. Yet, even this was enough for a nearly complete recovery of the voltage regulator's output parameters.

Fig. 3 presents diagrams of the serial transistor's forward emitter current gain variation as a function of its collector current, in the range from 1 mA to 800 mA. For the specified collector currents, values of the serial transistor base-emitter voltage were in the range from 620 mV to 830 mV. Diagrams were produced from computer simulation models for all four types of bias and load conditions, briefly described in Table 1. The vertical PNP power transistor operates with output current being at least 1 mA, since this current flows through the voltage divider resistors when the voltage regulator operates without load. All data were obtained with a constant collector– emitter voltage of V_{CE} = 3.3 V. Opposite to the results presented in Table 1, based on the measured mean values, the data presented in Fig. 3 were obtained using the instantaneous values of voltages and currents, at the operation point with constant output voltage (V_{out} = 5 V) and an appropriate input voltage of V_{in} = 8.3 V.

As can be seen from Table 1 and Fig. 3, the three isothermal annealing sequences led to similar characteristics of marginally irradiated and mostly recovered L4940V5 voltage regulators. The computer simulation models for these, principally different, periods, were basically the same. Yet, this could not be used as evidence that the distribution of the trapped charge was the same at the beginning and at the end of this decade-long experiment. Using only SPICE models, the influence of the interface traps and the oxide-trapped charge could not be separated. As already stated, the initial assumption of this research was that, as in the case of MOSFET-based logical circuits [29], most of the oxide-trapped charge would recover after 100°C annealing, while at the end of the 150°C annealing only the interface traps would remain. In discrete bipolar transistors, the interface states would recover first, after the annealing at 100°C–200°C, while the oxide-trapped charge would start to recover at higher temperatures, following the isothermal annealing at 150°C–300°C [14]. Taking into account the arguments presented in the previous chapters and paragraphs of this research, it seems that, indeed, the oxide-trapped charge in the tested circuits, at most, recovered after long-term room-temperature and short-term 100°C annealing. Nevertheless, there were no principal differences in the results obtained at the beginning of irradiation and at the end of the three annealing sequences, either in the model of the serial PNP power transistor or in the response of the entire L4940V5 voltage regulator. So, the results obtained may be used only for characterization of the total power transistor's and voltage regulator's radiation and post-irradiation response, rather than making it possible to qualitatively separate the effects of the interface traps and the oxide-trapped charge.

6 Conclusion

Data on the more than decade long examinations of the radiation tolerance of L4940V5 voltage regulators were unified and extended with the newly procured isothermal annealing results. These COTS, automotive circuits, demonstrated unexpectedly high radiation hardness during the previous experiments, potentially qualifying them as a cheap replacement for specially designed rad-hard power integrated circuits. The same samples, exposed to the γ-radiation more than ten years ago, were further analysed after long-term, room-temperature annealing, followed by two sequences of short-term, high-temperature annealing. The circuit response gave a unique opportunity to analyse exclusively the radiation hardness of the vertical serial PNP power transistor, since the small-signal, control circuit was marginally affected by ionising radiation.

A broad ensemble of the experimental data enabled the creation of a credible SPICE model, successfully describing the circuit response in the γ-radiation field. The initial phase of irradiation, up to 200 Gy, was efficiently recreated using the variations of the maximum forward emitter current gain and the knee current of the serial PNP power transistor. The data and computer simulation showed significant agreement for load cur-

rents of 100 mA, 400 mA and nearly 800 mA, for various input voltages. The subsequent exposure to γ-radiation could not be successfully modelled, due to the expressed saturation of the serial transistor's excess base current. The current limit protection of the driver NPN transistor further affected the circuit response.

Ten-year room-temperature annealing of integrated circuits, irradiated up to 500 Gy, caused the great recovery of the voltage regulator's quiescent current, yet followed by the further degradation of the maximum output current. The primary reason for the described response was the mutual recovery of the oxide-trapped charge and the build-up of interface traps above the emitter area of the serial PNP power transistor. On the other hand, two successive, one-week, high-temperature annealing periods caused the tremendous recovery of all the irradiated voltage regulators, reducing the circuit degradation down to the level specified after absorption of the total dose of 50 Gy.

The initial phase of irradiation caused the voltage regulator to degrade primarily through the influence of the oxide-trapped charge. The second phase of irradiation is a consequence of the activation of the overcurrent protection of the NPN driver transistor, followed by the saturation of the trapped charge density. Despite the relatively high doping concentration of the P-type emitter area in the vertical PNP power transistor, increased surface recombination in the area of the interdigitated emitter was the primary cause of the sharp increase in the serial transistor's excess base current.

Saturation of the serial transistor's excess base current after long-term, room-temperature annealing prevented the efficient modelling of this post-irradiation response. On the other hand, in most cases the response to the high-temperature annealing could be faithfully modelled in the same manner as during the initial phase of the voltage regulator irradiation.

7 Acknowledgement

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8 References

1. G. A. Rincon-Mora, Analog IC design with low-dropout regulators, McGrawHill Education (2014).
2. R.L. Pease, Total ionizing dose effects in bipolar devices and circuits, IEEE T Nucl Sci 50 (2003) 539-551.
3. D. M. Fleetwood, Total ionizing dose effects in MOS and low-dose-rate-sensitive linear-bipolar devices, IEEE T Nucl Sci 60 (2013) 1706-1730.
4. V. S. Pershenkov, V. B. Maslov, S. V. Cherepko, I. N. Shvetzov-Shilovsky, V. V. Belyakov, A. V. sogoyan, V. . Rusanovsky, V. N. Ulimov, V. V. Emelyanov, V. S. Nasibullin, The effect of emitter junction bias on the low dose-rate radiation response of bipolar devices, IEEE T Nucl Sci 44 (1997) 1840–1848.
5. J. Assaf, Bulk and surface damages in complementary bipolar junction transistors produced by high dose irradiation, Chin Phys B 27 (2018) 016103 1-8.
6. F. J. Franco, C. Palomar, J. G. Izquierdo, J. A. Agapito, SPICE simulations of single event transients in bipolar analog integrated circuits using public information and free opeen source tools, IEEE T Nucl Sci 62 (2015) 1625-1633.
7. M. R. Shaneyfelt, J. R. Schwank, D. M. Fleetwood, R. L. Pease, J. A. Felix, P. E. Dodd, M. C. Maher, Annealing behaviour of linear bipolar devices with enhanced low-dose-rate sensitivity, IEEE T Nucl Sci 51 (2004) 3172-3177.
8. J. Beaucour, T. Carribre, A. Gach, P. Poirot, Total dose effects on negative voltage regulator. IEEE T Nucl Sci 41 (1994) 2420-2426.
9. P. C. Adell, R. D. Schrimpf, W. T. Holman, J. L. Todd, S. Caveriviere, R. R. Cizmarik, K. F. Galloway, Total dose effects in a linear voltage regulator, IEEE T Nucl Sci 51 (2004) 3816-3821.
10. V. Ramachandran, B. Narasimham, D. M. Fleetwood, R. D. Schrimpf, W. T. Holman, A. F. Witulski, R. L. Pease, G. W. Dunham, J. E. Seiler, D. G. Platteter, Modeling total-dose effects for a low-dropout voltage regulator, IEEE T Nucl Sci 53 (2006) 3223-3231.
11. R. L. Pease, S. McClure, J. Gorelick, S. C. Witczak, Enhanced low-dose-rate sensitivity of a low-dropout voltage regulator, IEEE T Nucl Sci 45 (1998) 2571-2576.
12. E. W. Enlow, R. L. Pease, W. E. Combs, R. D. Schrimpf, R. N. Nowlin, Response of advanced bipolar processes to ionizing radiation, IEEE T Nucl Sci 38 (1991) 1342-1349.
13. R. L. Pease, ELDRS in bipolar linear circuits: a review, IEEE T Nucl Sci 56 (2009) 1894-1908.
14. A. Holmes-Siedle, L. Adams, Handbook of Radiation Effects, Oxford University Press (2004).
15. L4940 Series - very low dropout 1.5A regulators, STMicroelectronics (2003).
16. F. Bertotti, C. Cini, C. Contiero, P. Galbiati, Monolithically integrated semiconductor device containing bipolar junction transistors, CMOS and

DMOS transistors and low leakage diodes and a method for its fabrication, United States Patent 4887142, Dec. 12 (1989).
17. V. Vukić, P. Osmokrović, Total ionizing dose response of commercial process for synthesis of linear bipolar integrated circuits, J Optoel Adv Mater 8 (2006) 1538-1544.
18. V. Vukić, P. Osmokrović, Impact of forward emitter current gain and geometry of PNP power transistors on radiation tolerance of voltage regulators, Nucl Technol Radiat 25 (2010) 179-185.
19. V. Dj. Vukić, P. V. Osmokrović, On-line monitoring of base current and forward emitter current gain of voltage regulator's serial PNP transistor in radiation environment, Nucl Technol Radiat 27 (2012) 152-164.
20. V. Dj. Vukić, P. V. Osmokrović, Gamma-radiation response of isolated collector vertical PNP power transistor in moderately loaded voltage regulator L4940V5, J Optoel Adv Mater 15 (2013) 1075-1083.
21. V. Dj. Vukić, P. V. Osmokrović, Impact of the excess base current and the emitter injection efficiency on radiation tolerance of a vertical PNP power transistor in a voltage regulator, Inf MIDEM 43 (2013) 27-40.
22. G. C. Messenger, M. S. Ash, The Effects of Radiation on Electronic Systems, Van Nostrand Reinhold (1992).
23. D. M. Schmidt, D. M. Fleetwood, R. D. Schrimpf, R. L. Pease, R. J. Graves, G. H. Johnson, K. E. Galloway, W. E. Combs, Comparison of ionizing-radiation-induced gain degradation in lateral, substrate and vertical PNP BJTs, IEEE T Nucl Sci 42 (1995) 1541-1549.
24. Star-HSPICE Manual, Avant! Corporation (1998).
25. D. M. Schmidt, A. Wu, R. D. Schrimpf, D. M. Fleetwood, R. L. Pease, Modeling ionizing radiation induced gain degradation of the lateral PNP bipolar junction transistor, IEEE T Nucl Sci 43 (1996) 3032-3039.
26. H. J. Barnaby, B. Vermeire, M. J. Campola, Improved model for inncreased surface recombination current in irradiated bipolar junction transistors, IEEE T Nucl Sci 62 (2015) 1658-1664.
27. X. Li, J. Yang, H. J. Barnaby, K. F. Galloway, R. D. Schrimpf, D. M. Fleetwood, C. Liu, Dependence of ideality factor in lateral PNP transistors on surface carrier concentration, IEEE T Nucl Sci 64 (2017) 1549-1553.
28. A. Wu, R. D. Schrimpf, H. J. Barnaby, D. M. Fleetwood, R. L. Pease, S. L. Kosier, Radiation-Induced Gain Degradation in Lateral PNP BJTs with Lightly and Heavily Doped Emitters, IEEE T Nucl Sci 44 (1997) 1914-1921.
29. C. E. Barnes, D. M. Fleetwood, D. C. Shaw, P. S. Winokur, Post irradiation effects (PIE) in integrated circuits, IEEE T Nucl Sci 39 (1992) 328-341.
30. R. Gariboldi, M. Morelli, Very-low-drop voltage regulator with a fully complementary power process, IEEE J Solid-St Circ 22 (1987) 447–450.
31. A. Andreini, C. Contiero, P. Galbiaty, A new integrated silicon gate echnology combining bipolar linear, CMOS logic, and DMOS power parts, IEEE T Electr Dev 33 (1986) 2025-2030.
32. F. Bertotti, P. Ferrari, M. T. Gatti, Saturation limiting system for a vertical, isolated collector PNP transistor and monolithically integrated structure thereoff, United States Patent 4887141, Dec. 12 (1989).
33. LTSpice-Version 4.13q, Linear Technology Corporation (2012).
34. V. Dj. Vukić, Rapid and long-term gamma-radiation annealing in low-dropout voltage regulators, Nucl Technol Radiat 32 (2017) 155-165.
35. V. Dj. Vukić, P. V. Osmokrović, Failure of the negative voltage regulator in medium-photon-energy X radiation field, Microelectron Reliab 54 (2014) 79-89.
36. Standard.BJT, LT Wiki, Linear Technology Corporation (2012) http://ltwiki.org/?title=standard.bjt
37. BC808-25LT1G, General Purpose Transistors, On-Semiconductor (2016).
38. A. H. Johnston, B. G. Rax, Testing and qualifying linear integrated circuits for radiation degradation in space, IEEE T Nucl Sci 53 (2006) 1779-1786.
39. A. Johnston, R. Swimm, R. D. Harris, D. Thorbourn, Dose rate effects in linear bipolar transistors, IEEE T Nucl Sci 58 (2011) 2816-2823.

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