UDK621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 36(2006)4, Ljubljana

POROUS SILICON FOR SENSORS AND ON-CHIP INTEGRATION OF RF COMPONENTS

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INVITED PAPER
MIDEM 2006 CONFERENCE
13.09.2006 - 15.09.2006, Strunjan, Slovenia

Key words: sensors, porous silicon, micro-plate, RF components

Abstract: In this paper, porous silicon technology for use in bulk silicon micromachining and sensors will be described and examples of micro-hotplates, thermal sensors and microfluidic devices based on porous silicon technology will be presented. Another interesting emerging application of porous silicon technology that will be presented is its use as micro-plate on silicon for on-chip integration of RF-components (inductors, resonators). Examples of design, fabrication and characterization of integrated inductors on porous silicon micro-plates using standard CMOS technology will be presented. The properties that make porous silicon very appropriate for the above applications will be described.

Porozni silicij kot material za integracijo senzorjev in RF komponent na čipu

Kjučne besede: senzorji, porozni silicij, mikro-grelci, RF komponente

Izvleček: V prispevku opisujemo možnosti uporabe poroznega silicija pri mikroobdelavi silicija in izdelavi senzorjev. Opisali bomo primere izdelave mikro-grelcev, termičnih senzorjev in mikro-naprav za pretok tekočin. Kaže se še ena zanimiva uporaba tehnologije poroznega silicija pri izdelavi mikro-plošč na siliciju za integracijo RF komponent (rezonatorji, tuljave). Predstavimo primere načrtovanja, izdelave in karakterizacije integriranih tuljav na mikro-ploščah iz poroznega silicija v standardni CMOS tehnologiji. Pokažemo na lastnosti, ki omogočajo, da je porozni silicij izredno priemeren material za vse naštete uporabe.

1. Introduction

Porous silicon is a material with tunable properties, depending on the electrochemical conditions used in its fabrication and the resistivity and type of the silicon substrate used as starting material /1/. It may by macroporous, with large vertical pores of diameter from few hundreds of nanometers to several micrometers, or mesoporous/microporous with randomly distributed pores in the micron or nanometer range. High porosity mesoporous silicon is a nanostructured material with properties strongly related with its low dimensionality.

Intensive research in the early nineties has been devoted to nanostructured silicon for application in silicon optoelectronics, due to its bright visible luminescence at room temperature /2/. However, a lot of other interesting applications emerged later from this intensive research, including different sensor devices and different active and passive components on a silicon substrate /3-8/. In parallel, other types of porous silicon were investigated in detail, including macroporous silicon on different silicon substrates /9/ and combinations of macroporous and mesoporous (nanostructured) silicon /10/.

This paper will first describe the general properties of porous silicon that make it appropriate for use in silicon micromachining and sensors. It will then focus on the following applications:

a) Fabrication of micro-hotplates on silicon by porous silicon bulk micromachining in thermal sensors for gas flow, gas composition and acceleration measurements
b) RF isolation on bulk crystalline silicon for the integration of RF inductors and
c) Fabrication of buried microfluidic channels on silicon for sensors, microfluidic devices and lab-on-chip applications.

2. Results and discussion

2.1 Fabrication and properties of porous silicon

Porous silicon is formed by electrochemical dissolution of bulk crystalline silicon. For mesoporous silicon formation, aqueous or ethanoic HF solutions are mainly used. The structure and morphology of the obtained material depend on the type and resistivity of the silicon substrate and on the electrochemical parameters used. Porosity, pore size and pore distribution are essential parameters that characterize the material.

Chemical etching of slightly oxidized porous silicon in an HF-containing solution is highly selective to bulk or polycrystalline silicon. This property makes porous silicon very appropriate for use as sacrificial material in bulk silicon micromachining.

Highly porous silicon is a highly resistive material (ρ>1MΩcm) Oxidized porous silicon shows dielectric properties equivalent to those of thermal SiO_2. In comparison with thermal SiO_2, porous silicon is very rapidly oxidized due to its extremely high reactivity, so that much thicker layers of oxidized porous silicon compared to SiO_2 are grown on silicon within the same time. This property was tentatively used in the seventies for DC isolation on a silicon substrate /11/, mainly applied to bipolar devices. More recently, porous silicon is investigated for use in RF isolation on silicon /12/, for which it shows important advantages that will be described below.

2.2 Applications

2.2.1 Porous silicon for bulk silicon micromachining and suspended microstructures fabrication.

Due to the high growth rate of porous silicon on a silicon substrate, thick PS layers may be fabricated at relatively short times. This property of porous silicon, combined with its high chemical etch selectivity to bulk or polycrystalline silicon makes the material very appropriate for use as sacrificial layer in bulk silicon micromachining. On the other hand slightly oxidized porous silicon shows etch resistance to dry silicon etchants. This property is used to fabricate suspended porous silicon membranes by etching isotropically the silicon layer underneath. The produced structures are very useful in several applications.

Different interesting processes were developed at IMEL for fabricating suspended micromechanical structures (suspended membranes, cantilevels or resistors over a cavity on the silicon substrate), as follows:

a) A 3-step process for the fabrication of polycrystalline silicon suspended micromechanical structures /5, 13/ by: local formation of porous silicon on the bulk substrate, polycrystalline silicon deposition and patterning, and finally porous silicon dissolution to release the structures. An example of structures fabricated using this technology is given in fig.1.

b) A 4-step process for the fabrication of suspended porous silicon microstructures on Si was also developed /14/, involving: Local growth of porous silicon, photo resist deposition and patterning, isotropic etching of bulk silicon underneath porous silicon for membrane release, and finally resist stripping.

c) A process was developed for fabricating buried microfluidic channels and sealed cavities on silicon in a single two-step electrochemical process. Details are given in reference /15/.

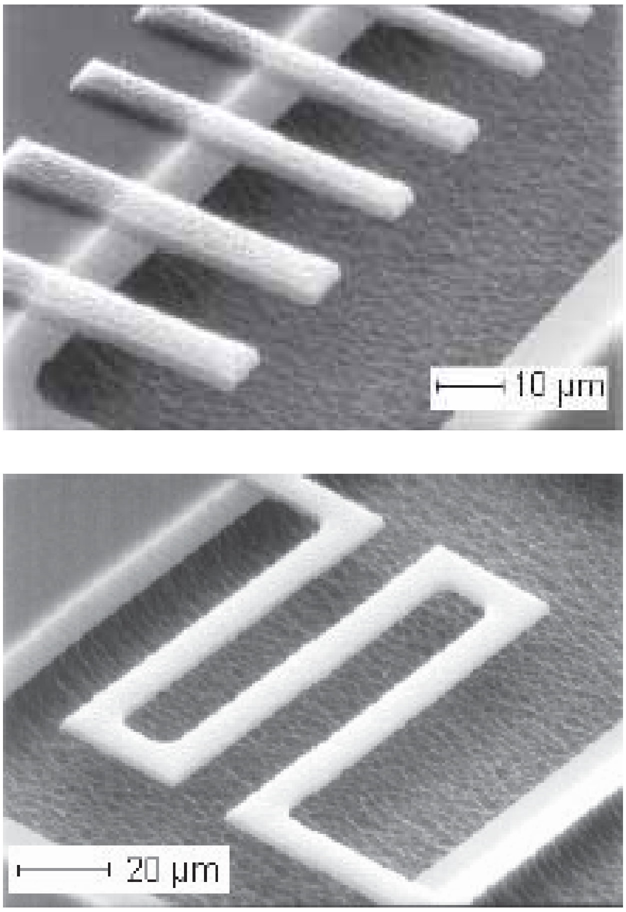


Fig. 1: Polycrystalline silicon micromechanical structures over cavity on a silicon substrate, fabricated with porous-silicon-sacrificial-layer technology

2.2.2 Porous silicon in micro-hotplate technology. Application in thermal sensors

Different types of micro-hotplates on bulk silicon may be fabricated using porous silicon technology, as illustrated in fig. 2. A thick compact porous silicon film, fabricated on a pre-defined area on the silicon substrate /16/ as illustrated in fig. 2 (a_1,a_2) is a simple and reliable micro-hotplate on bulk silicon allowing temperature increase on a heater on top of it up to 100-200^{o}C at relatively low power consumption, depending on the porosity of the material used. For example, with 65% mesoporous silicon, a thermal conductivity as low as 1.2 W/mK is obtained /17/). Thermal isolation on bulk silicon may by further improved by opening a cavity underneath the porous layer, as indicated in fig. 2 (b_1,b_2). This is possible by using a simple, two-step electrochemical process of porosification and electropolishing of Si /17/. When very low power consumption is needed (for example in the case of sensors working in an explosive environment) a process for the fabrication of porous silicon membranes suspended over an open cavity /14/ may be used, as indicated in fig. 2 (c_1,c_2). In this case, the fabrication process is slightly more complicated /14/. It involves porous silicon membrane formation and membrane release by dry etching of silicon through mask windows.

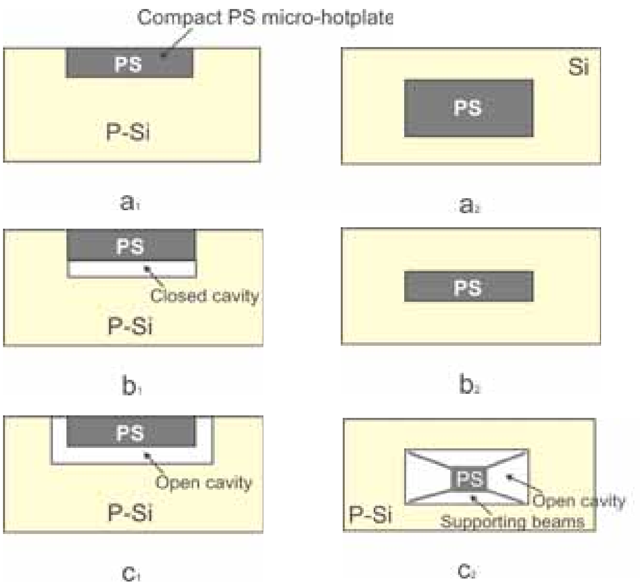


Fig. 2: Schematic representation of three different cases of porous silicon (PS) micro-hotplates on a silicon substrate. (a_1, b_1, c_1): cross sectional representation, (a_2, b_2, c_2): plan view.

2.2.3 Silicon thermal sensor using PS micro-hotplate technology

An example of thermal flow sensor using PS micro-hotplate is illustrated in fig. 3. A porous silicon (PS) micro-hotplate is used to integrate on top a heater and the hot contacts of two series of thermocouples (Th_1 and Th_2), their cold contacts being on bulk crystalline silicon (c-Si). This sensor shows high sensitivity and fast response and it finds different interesting applications. One such application is gas flow measurements. The sensor is placed in an appropriate housing and it is appropriate for measuring both laminar and turbular flows /18, 19/, due to its fast response. An example of housing is that of fig. 4, in which the sensor is placed in the center of a hemi-spherical tube, used as bypass to a larger tube (fig. 4a). This housing has been design for use in a flow meter for respiration monitoring developed at IMEL /20/. The external tube and the corresponding electronics are shown in fig. 4b. An example of sensor response in a large range of gas flow (from -200 to +200 slpm (standard liters per minute)) is shown in fig. 5. It is interesting to note that the response of the system is almost linear in the whole range of gas flow. This is an important advantage of this system compared to other micro-electromechanical (MEMs) systems commercially available.

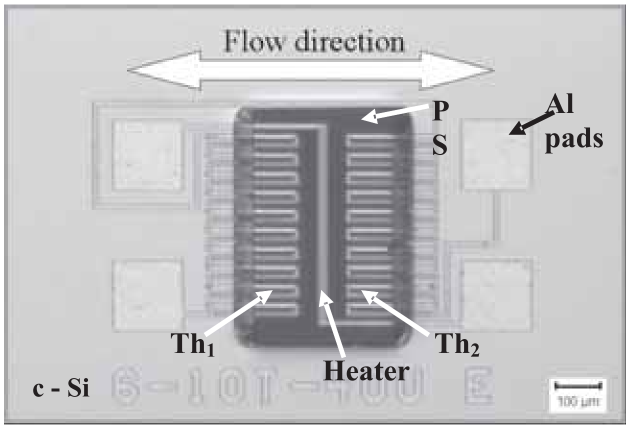


Fig. 3: Thermal sensor using porous silicon thermal isolation composed of a heater integrated on the porous silicon layer and two series of thermocouples (Th_1, Th_2) their hot contacts lying on porous silicon (PS) and their cold contacts on bulk crystalline silicon (c-Si)

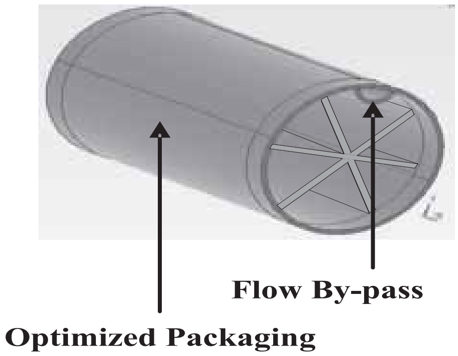
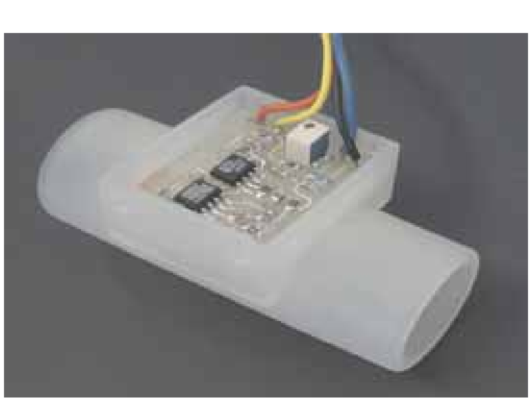


Fig. 4(a): Internal view of the housing of a gas flow sensor in a system for respiration monitoring. The sensor is based inside a bypass (hemi-spherical tube inside the larger tube), so as to assure laminar flow conditions.



Read-out Electronics

Fig. 4(b): External view of the housing with control electronics.

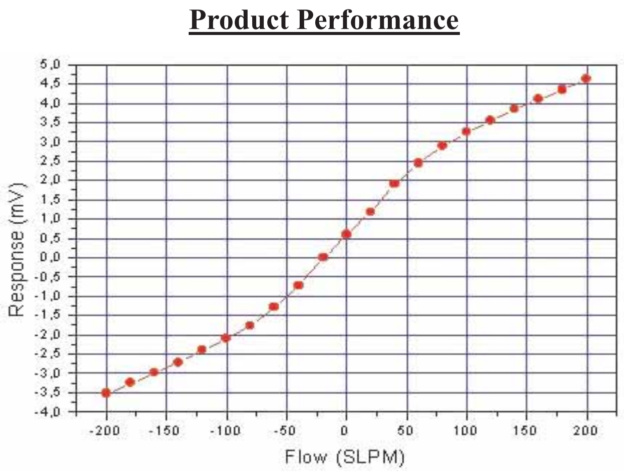


Fig. 5: Example of response of the system for respiration monitoring of fig. 4.

A more advanced device than that of fig. 3 uses a porous silicon membrane over cavity micro-hotplate, the rest of the technological steps being the same /17/. This introduces an improvement in local thermal isolation, thus allowing for higher temperatures on the heater, using the same power consumption. Comparative curves of temperature distribution around the heater for the two cases of compact porous silicon and porous silicon over air-gap micro-hotplates for an applied power of 35mW are shown in fig. 6. We see a substantial increase of maximum temperature on heater when we add an air-gap underneath the porous silicon layer.

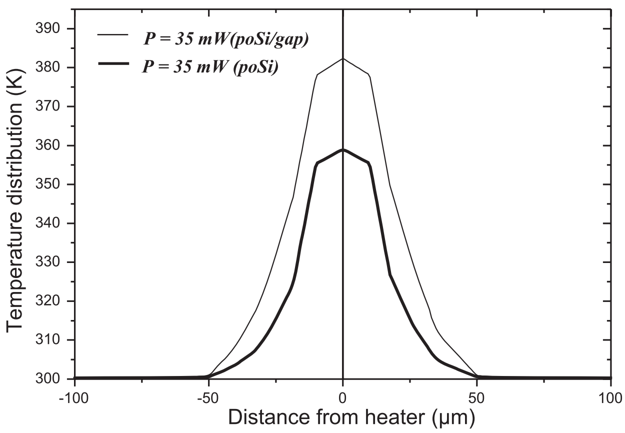


Fig. 6: Temperature distribution around a heater for two cases of micro-hotplates on silicon: a) a compact porous silicon micro-hotplate (black line) and b) a porous silicon over air gap micro-hotplate (grey line).

Thermal flow sensors using porous silicon suspended-membrane-over-cavity micro-hotplates at low power may operate at much higher temperatures, consumption. They are so appropriate for use as gas sensors in combination with catalytic materials, where an operation temperature above few hundreds of degrees C is in general needed for high sensitivity catalytic reactions. An example of conductometric gas sensor for the detection of methane, ethane etc. in an explosive environment /21/ is shown in fig. 7a. A platinum resistor is integrated on the porous silicon membrane, whose resistance charges with temperature. A temperature on the heater above 500°C may be achieved with an applied power of few tens of mW (fig. 7b) shows an image of a glowing Pt heater on a 60 µm^2 PS micro-hotplate as seen in an optical microscope, with a power of 50mW supplied to the heater. The heater started to emit detectable light when the supplied power exceeded 30mW.

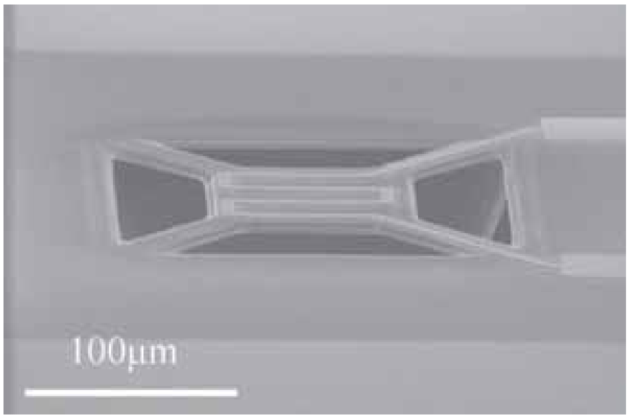


Fig. 7(a): Conductometric gas sensor with a platinum heater on a porous silicon micro-hotplate.

Fig. 7(b): Optical microscopy image of a glowing Pt heater on PS micro-hotplate, under 50mW power supply.

A microfluidic flow sensor based on a microchannel capped with a porous silicon membrane, on top of which the sensor active elements are integrated /12/, was also developed at IMEL (fig. 8), The sensor active elements are 3 resistors on the porous silicon capping layer as in fig. 8. The flow passes through the microchannel and thus the sensor is very appropriate for microflow measurements.

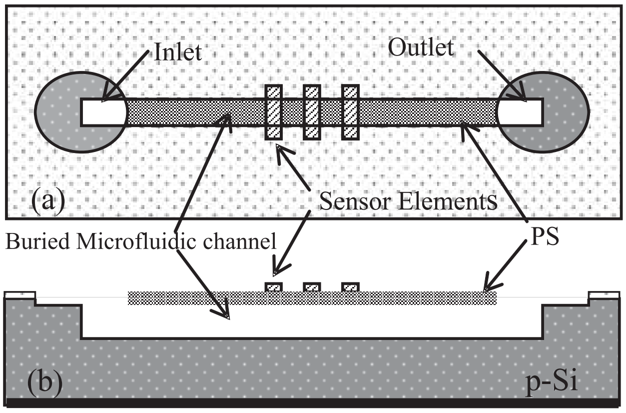


Fig. 8: Schematic representation of a plan view (a) and cross section (b) of a micro-flow sensor using a microfluidic channel capped with porous silicon, on top of which 3 sensor elements are integrated

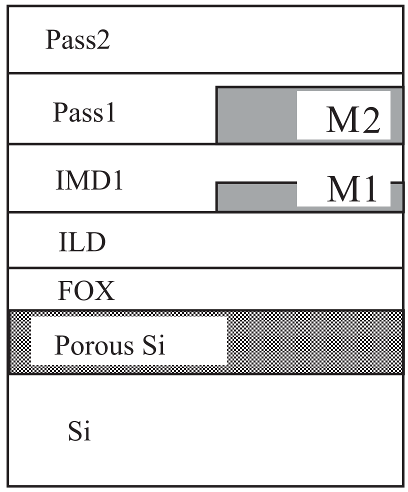


Fig. 9(a): Technology diagram for CMOS-compatible porous silicon integration.

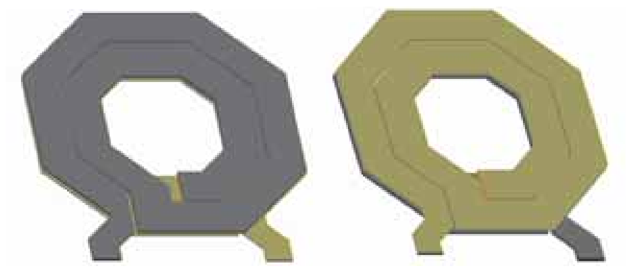


Fig. 9(b): 2-metal layer optimized inductor layout: light grey: metal 1, dark grey: metal 2.

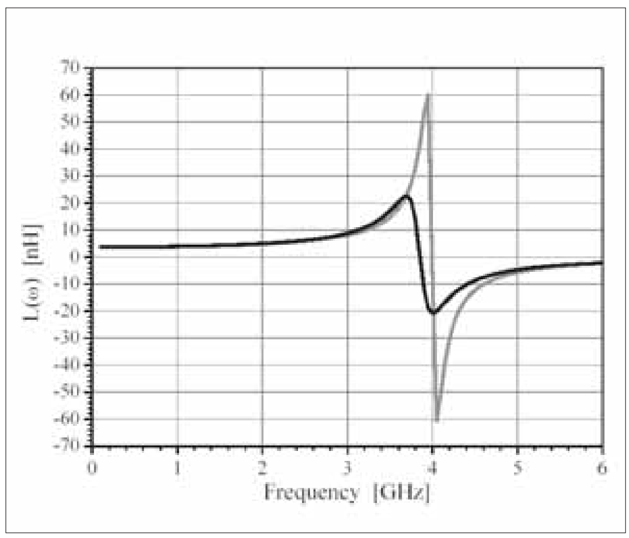


Fig. 10 (a): Simulation results of Inductance function for Cu metallization on bulk Si (black line) and on porous silicon RF micro-plate (grey line).

2.2.4 Integrated inductors on porous silicon dielectric layers

The properties that make porous silicon appropriate for local RF isolation on a silicon substrate are the following:

- Its relative dielectric constant and loss tangent are adjustable by changing the porosity and surface passivation of the material
- The porous silicon layers may be fabricated on selected areas on the silicon substrate
- Low stress material may be fabricated
- The thermal expansion coefficient of porous silicon is similar to that of bulk silicon

By employing a fairly thick porous silicon layer and a standard 2-metal CMOS process, optimized RF inductors on Si were designed and their properties were simulated /12/. An example of inductor's layout is shown in fig. 9b (light grey: metal 1, dark grey: metal 2), while in (a) the technology diagram for CMOS-compatible porous silicon integration is shown. The simulated inductance function (L(w)) and quality factor (Q) for Cu metallization are shown respectively in figs. 10 (a) and (b). Black lines correspond to the case of bulk silicon substrate, while grey lines to the case of porous silicon RF micro-plate. Q increases by a factor of 2 when using porous silicon instead of bulk silicon as substrate.

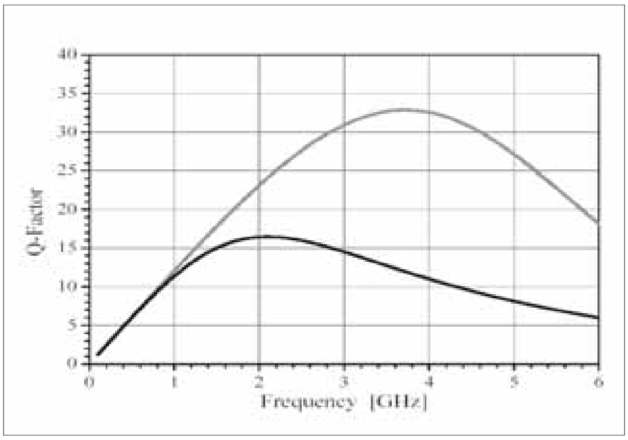


Fig. 10 (b): Simulation results of Q-factor when using Si (grey line) or porous Si (black line) substrate. The technology used in simulations was 0.13 μm-compatible, two-metal CMOS technology with Cu metallization.

2.2.5 Macroporous silicon technology

Mocroporous silicon layers may be fabricated on p-type silicon using an HF:DMF solution /23/. Ordering of the pores may be introduced by appropriate pre-patterning of the anodized area, in order to form pore initiation pits. An example of non-ordered porous silicon layer is shown

in fig. 11 ((a) plan view, (b) cross sectional SEM image). In fig. 12 we see an example of ordered macroporous silicon structures, fabricated by first creating ordered inverted pyramids on the silicon surface, followed by anodization for macroporous formation /10/.

A process for fabricating macroporous silicon membranes over a mesoporous layer or a cavity on a pre-defined area of the silicon substrate has been also developed at IMEL /24/. The process (fig. 13) consists in fabricating macroporous layers on a selected area on the silicon substrate (fig. 13 a), followed by porosification under electrochemical conditions for mesoporous silicon formation (fig. 13b).

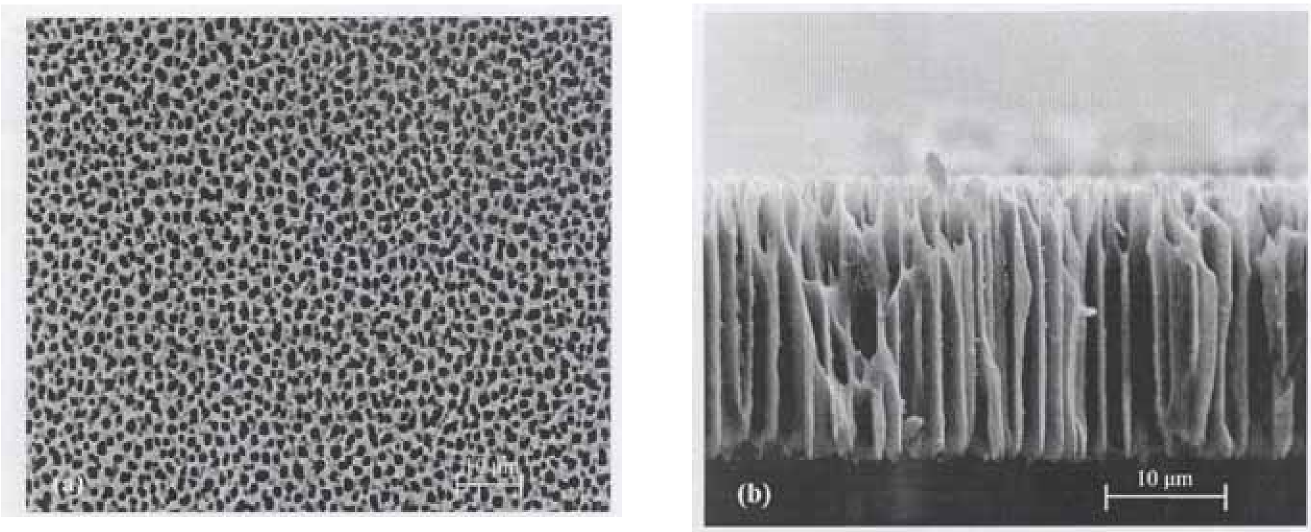


Fig. 11: (a) Plan view and (b) cross-sectional SEM images of macroporous silicon layers on bulk silicon

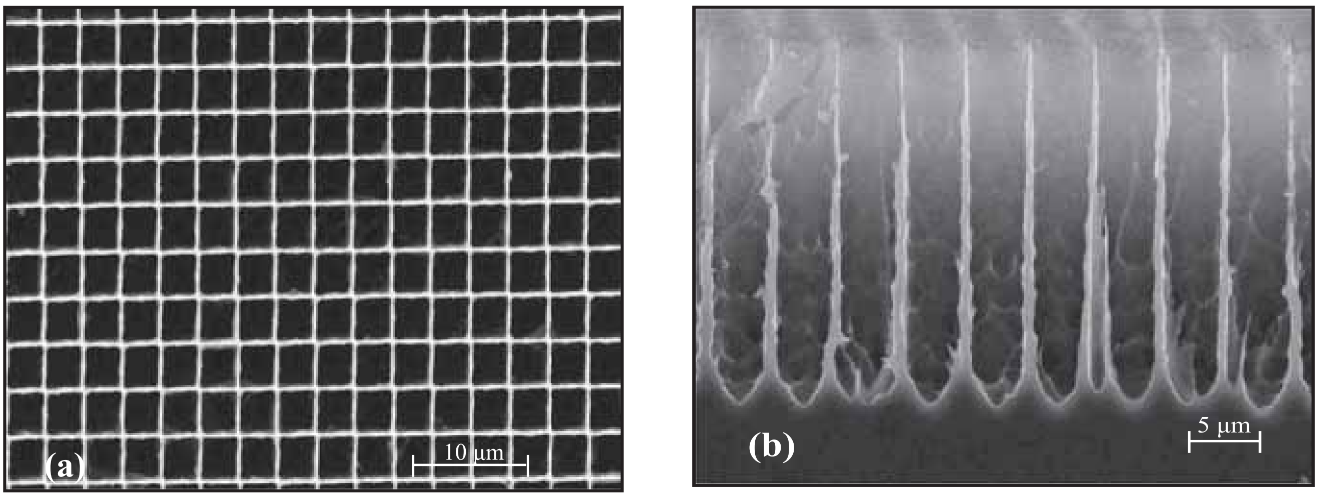


Fig. 12: Top view (a) and cross section (b) of a typical ordered macroporous Si layer

If the mesoporous layer is removed by chemical etching, a cavity is formed under the macroporous layer (fig. 13c).

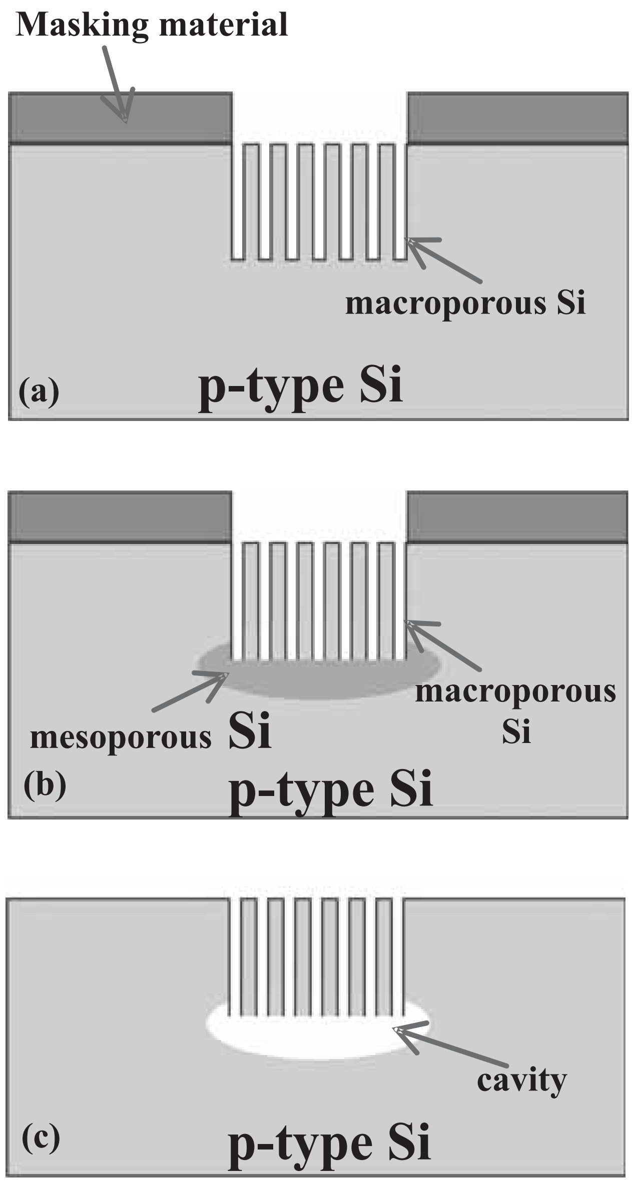


Fig. 13: Schematic representation of (a) a macroporous silicon layer on a pre-defined area on the Si-substrate (b) a macroporous silicon layer over a mesoporous layer, both fabrication a single two-step electrochemical process, (c) air cavity underneath the macroporous layer, fabricated by chemical dissolution of the mesoporous layer shown in (b).

3. Conclusion

Different technologies for bulk silicon micromachining using porous silicon technology were described. Their application in silicon sensors, microfluidic devices and RF isolation on a silicon substrate were also discussed.

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Prispelo (Arrived): 05. 09. 2006; Sprejeto (Accepted): 20. 10. 2006