Analysis of a power supply bypassing approaches

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Abstract. *In this paper analysis is presented how different values, arrangements and placement of bypass capacitors affects stability of the power supply voltage. Analysis is supported by measurements on a designed and manufactured printed circuit board and compared with results of simulations made in LT Spice. Simulations are developed, step by step from simplest one 100nF decoupling capacitor, to optimal bypass solution. Voltage fluctuations were reduced for 90 mV after adding second (equal) bypass capacitor in parallel to existing. Adding more than two capacitors in parallel did not show significant improvement. Using damp capacitor in addition to existing bypass capacitor reduced voltage noise for additional 80 mV down to 180 mV, being our final solution. Measurements on the PCB are well supported by simulations.*

1 INTRODUCTION

Every electronic circuit has power supply connections that supply constant DC voltage to all loads. One of the problems that has to be dealt with is that many high-speed electronic components are commonly used, which sink high-frequency currents. Power supply connections will always introduce impedance for this high-frequency currents that consequently cause power supply voltage noise. With constantly improving technology, the trend for high-performance integrated circuits is toward higher operating frequency and lower power supply voltages. For that reasons voltage noise must be kept at a minimum value, to ensure correct operation of the design [1], [2].

Voltage noise can be reduced by minimizing the impedance of the power supply circuitry, where the most common technique is to use bypass capacitors, which are maintaining low impedance paths for high-frequency currents. Impedance must be kept below the maximum impedance in whole range of the current transients. For lower frequencies up to 1 MHz, the bulk (electrolytic) capacitor is commonly sufficient [2]. However, at higher frequencies, ceramic bypass capacitors are used. In addition, they provide a localized source of DC power and are particularly useful in reducing peak current surges propagated across the board [1]. In ideal case, a capacitor has no losses and no series inductance, but in reality, every capacitor has its parasitic equivalent series resistance (ESR) and equivalent series inductance (ESL) [3]. These two parameters determine the frequency range, where the impedance is low enough, to serve its purpose. The impedance of capacitor drops with frequency up to the self-resonance frequency (1), where the minimal impedance is achieved [4].

$$f_0 = \frac{1}{2\pi\sqrt{ESL \cdot C}} \quad (1)$$

From that point on impedance increases with frequency due to ESL, which is influenced also by the connection traces and vias of the capacitor, as shown in the Figure 1.

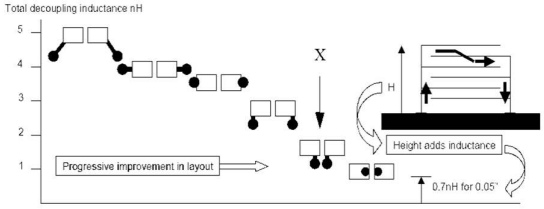

Figure 1: Inductance influenced by the connections.

To decrease the parasitic effects more capacitors can be put in parallel. If different capacitors are used, this causes unwanted parallel resonances, which lead to high impedance at this resonance frequencies. Between the self-resonant frequencies of two different capacitors, the impedance of the larger capacitor is essentially inductive, whereas the impedance of the smaller capacitor is capacitive. In this frequency range there exists a parallel resonant LC circuit. Around this resonant point, the impedance of the parallel combination is larger than the impedance of either isolated capacitor [3], [5].

For proper operation, capacitor values must be calculated for a specific load type. Furthermore, the dielectric material of the capacitor must be properly selected together with the case size. The bypass capacitors are often chosen according to past usage experiences and rules-of-thumb. In this paper, we will try to show, how all these properties influence in reality and compare that with simulations.

2 EXPERIMENT

2.1 Printed circuit board (PCB)

As shown in the Figure 2, we have designed a printed circuit board (PCB) with the MIC 4605-2YM chip, a power MOSFET gate driver with two outputs, each providing 1A of output current [6]. Its outputs are connected to resistor and a capacitor, connected in series to simulate the MOSFET gate impedance. When switching, the capacitors charge and discharge and the charging current is supplied from the power supply. With this configuration, the amplitude of current pulses can be controlled (resistor) and the frequency with input PWM signal. Resistor values determine the amplitudes of current pulses.

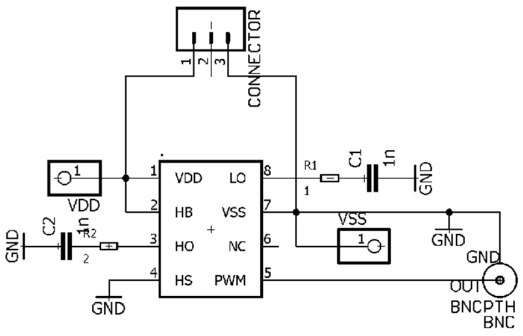

Figure 2: Detailed schematics of the chip

The PCB was designed using EAGLE PCB design software [7] in a way that it offers various positions for placement of decoupling capacitors and that the power supply traces are wide enough to allow different case sizes of capacitors to be soldered. Screw-terminal connector is positioned on the left side of the board for DC power supply. 2 mm wide power supply trace is routed from the connector to the chip MIC 4605-2YM on the right side of the board.

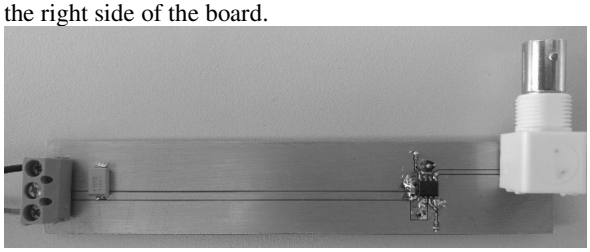

Figure 3: PCB design

For signal source connection to drive the chip, a BNC connector is provided. All ground is routed using ground plane. For measurements purposes, a pin header was put on VDD and GND pins of the chip. Bottom side of the PCB has a 2 mm wide trace directly under the chip (via at VDD pin), offering another option for positioning a decoupling capacitor. Figure 4 shows the detailed routing of the chip.

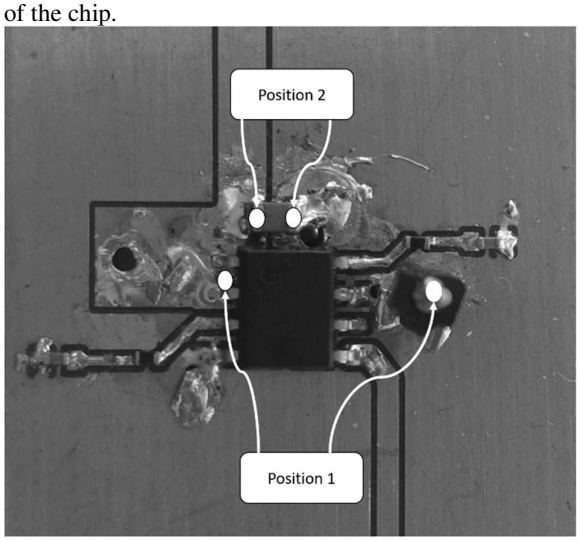

Figure 4: Chip routing details and probe positions

2.2 Measurement setup

The board was connected to a DC laboratory power supply, providing constant 12V DC voltage, controlled with multimeter, while a function generator was used to generate PWM signal. Voltage fluctuations of power supply were measured with an oscilloscope. Most of the measurements were made on pin-headers and also on some different spots on the PCB. Data from oscilloscope was later processed in Matlab.

2.3 Spice simulation model

Simulations were made with LT SPICE simulator from Linear Technology [8]. Since the LT spice library does not include a model for the MIC 4605-2YM, a model had to be added. A very useful source of information was the manufacturer's website, where they provide a model for another simulator: MPLAB Mindi [9]. This simulator was initially used for the transient simulation of the circuit. Value of each resistor was selected to get maximum amplitude of 1 A from both outputs. This simulation gave us enough information to make a model in LT Spice. To model the outputs of the chip, MOSFET transistors (included in LT Spice library, Si1555DL_P from Siliconix) were chosen that provide equal current pulses, as simulated in the MPLAB Mindi simulator. Correct MOSFET driving including invert and dead time was solved with two phase shifted square signal sources.

The chip model was included in a transient simulation with all necessary parasitic for the AC model of the power supply circuit, as shown in the Figure below.

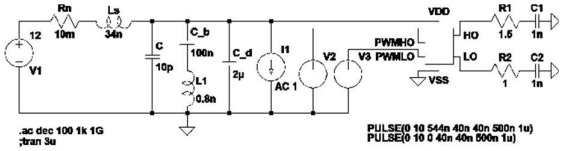

Figure 5: Basic simulation design

For accurate simulations, impedance of the traces was taken into consideration and included in simulation. We have used Saturn PCB design software [10] using basic trace parameters: trace width/height material and copper thickness, giving a value of capacitance and inductivity per centimeter. Trace parameters for our design are: 2 mm width, 1.6 mm height, material is FR-4 STD and copper thickness 35 µm. This results in inductance of 3.78 nH/cm and capacitance of 0.97 pF/cm. Multiplying this with trace length (9.5 cm) gives a good approximation for L_0 = 35.91 nH and C_0 = 9.21 pH and these results were used in the trace AC model.

3 RESULTS

3.1 Power supply bypassing design using simulations

Simulations of power supply impedance were made using different bypassing arrangements starting from simple to more advanced.

Simulation results using realistic 100 nF bypass capacitor with ESR set to 10 mΩ and ESL to 0.5 nF, are shown in the Figure 6. Due to ESL a series resonance appears at around 10.5 MHz, where impedance is limited

by ESR. Further on, the impedance starts to increase again as capacitor exhibits inductive behavior.

Putting more capacitors in parallel can improve impedance trough whole frequency range. Figure 6 presents simulation results, where two 100 nF capacitors are connected in parallel. Since both capacitors are the same, the resulting capacitance increases by two, while the inductance and resistance drops by a factor of two.
The increase of capacitance decreases the parallel resonance frequency. The impedance at frequencies above parallel resonance decreases significantly.

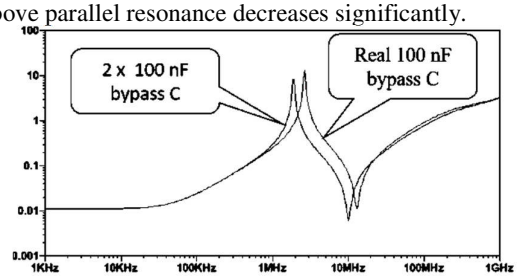

Figure 6: Impedance graphs of different bypass arrangements using a realistic capacitor model

Figure 7 presents bypassing arrangement using a 100 nF capacitor (same as in previous simulations) connected in parallel with a 1 nF capacitor with better parasitic values (ESR = 1 mΩ and ESL = 0.25 nF). Since another (better) capacitor was used, lower impedance is generally expected. But in the frequency range between self-resonances of capacitors additional parallel resonance of capacitors is introduced, where the impedance is actually larger than previous, where no additional capacitor was used.

It turns out, that using equal capacitors in parallel is the best option. The only problem that has to be solved is the first parallel resonance. Usually this is accomplished by introducing a damp capacitor with right capacitance and ESR to form a critical damped resonance circuit [11].

$$C_{damp} = 2.2\ uF, \quad ESR_{damp} = 0.235\ \Omega \tag{2}$$

With this solution, the power supply impedance is lower than 0.23 Ω in the whole frequency range of interest (0-50 MHz), as show in the Figure below.

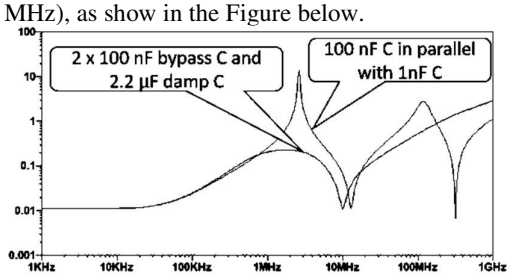

Figure 7: Impedance graph

3.2 Measurement of voltage ripple at different positions

This measurement shows importance of bypass capacitor placement. Figure 8 and 9 present two simulations and measurements results with equal bypass capacitors and different probe positions 1 and 2 (labeled in the Figure 3). Measurement closer to the capacitor (position 2) gives lower voltage fluctuations without spikes. Although both positions are very close to each other, the difference in voltage ripple is 100 mV. In simulation, the extra line length to the position 1 was modeled as additional impedance in series with the bypass capacitor. Impedance was estimated with Saturn PCB design program to be 1 nF. The good match between simulation and measurement validates the model parameters.

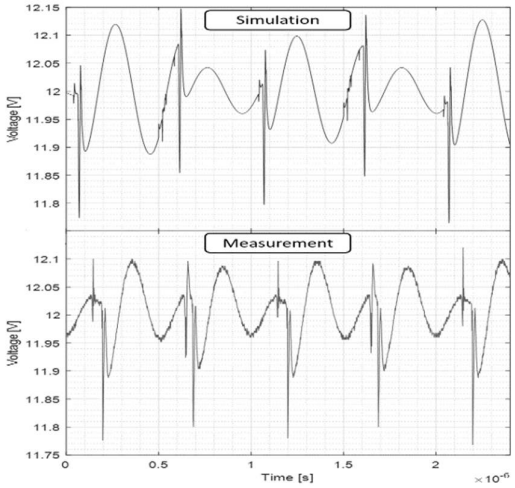

Figure 8: Simulation and measurement on PCB, position 1

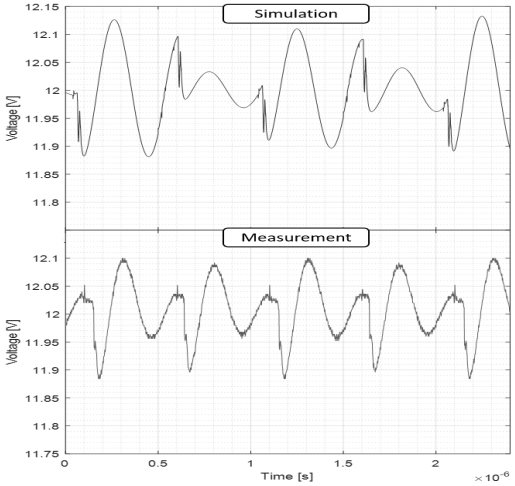

Figure 9: Simulation and measurement on PCB, position 2

3.3 Bypass effectiveness of parallel connected capacitors

We started with two equal 100 nF bypass capacitors and compared that with previous results. Figure 10 presents usage of one 100 nF bypass capacitor, $U_{pp} \approx 260$ mV. With two capacitors, voltage fluctuations were reduced to $U_{pp} \approx 170$ mV. Additional measurements on the PCB indicated that there is no significant decrease in voltage fluctuation after adding third bypass capacitor. This is mainly due to the fact, that more capacitors require more place and consequently more trace length. Thus, at one-point adding more capacitors in parallel is no more effective.

The best results are made with capacitors stacked on top of each other, this minimizes trace length and takes least amount of space on PCB.

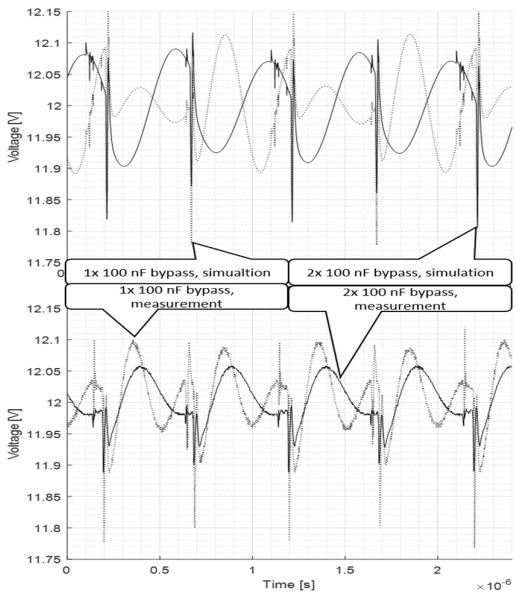

Figure 10: Comparison of parallel connected bypass capacitors

3.4 Optimizing bypassing with a damp capacitor

To reduce parallel resonance, damp capacitor is added in parallel to the existing bypass capacitor. According to the [11], capacitance and ESR values of damp capacitor were calculated.

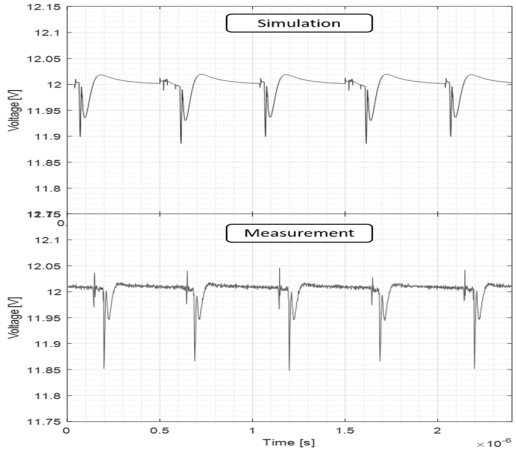

Figure 11: Simulation and measurement with bypass and damp capacitor, position 1

Required values were realized with ceramic capacitor, its parameters: 2.2 uF capacitance in series with 0.235 Ω resistor, to get ESR in desired range. Simulation AC analysis confirmed decrease of impedance at parallel resonance frequency, shown in Figure 7. After adding damp capacitor voltage fluctuations are limited to 180 mV, which is an 80 mV less, compared to usage of bypass capacitor alone. Simulations give somewhat lover values. This is expected, due to parasitic values, which cannot be approximated with high accuracy.

4 CONCLUSION

This paper presented different bypassing approaches. Analysis showed some simple and cost-efficient solutions and pointed out common mistakes one could do. Development of simulation lead to bypassing solution later tested on a real PCB. Usage of parallel bypass capacitors and damp capacitor showed significant improvement in voltage stability. Position of bypass capacitor is also very important. Every additional trace length causes noticeable increase of noise. Good match between simulation and measurement proved, that with accurate simulation we can predict bypass capacitors arrangement early in the development process of electronic circuit and avoid later malfunction. For further improvement of this research more testing could be done concentrating on capacitor type, manufacturer and materials.

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