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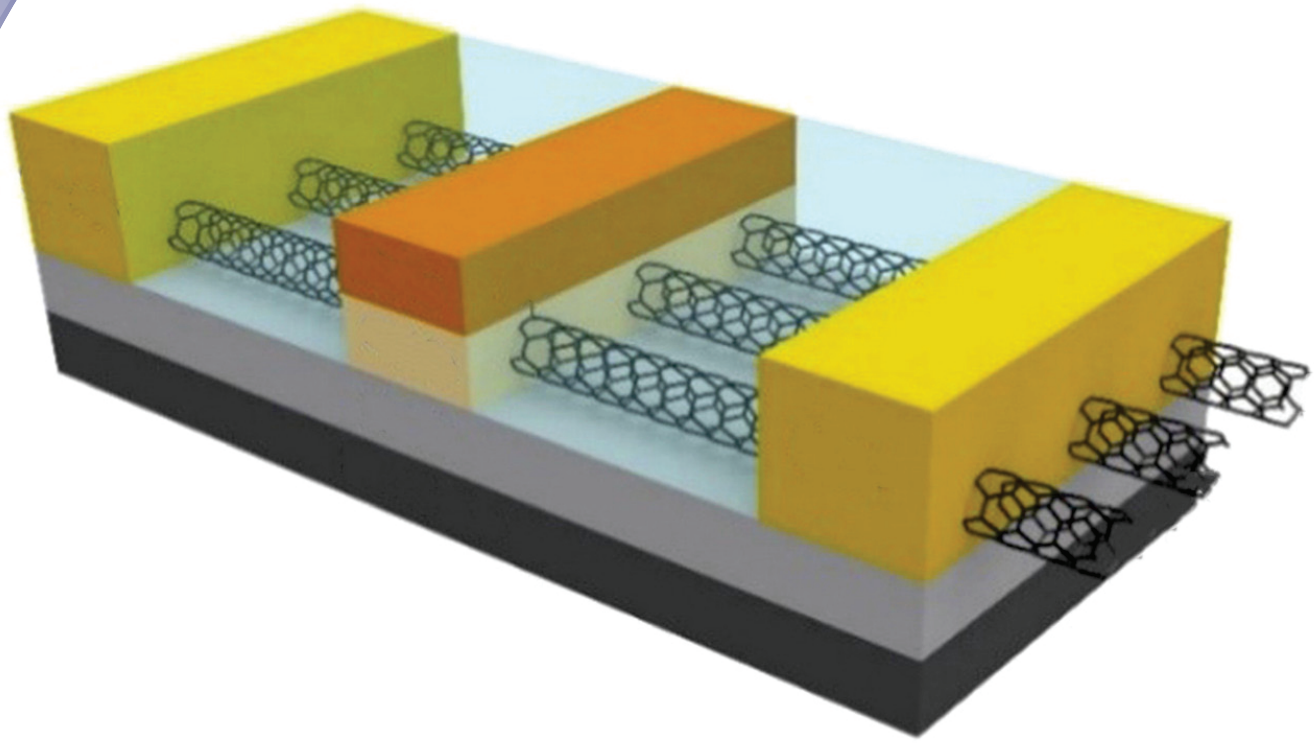

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# Voltage Differencing Transconductance Amplifier based Ultra-Low Power, Universal Filters and Oscillators using 32 nm Carbon Nanotube Field Effect Transistor Technology

*Islombek Mamatov, Yasin Özçelep, Firat Kaçar*

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**Abstract:** Carbon nanotube field-effect transistor (CNTFET) is a strong candidate to replace existing silicon-based transistors. The ballistic transport of electrons in the CNTFET channel leads to ultra-low-power and high-frequency devices. Although a lot of digital applications of CNTTFET were presented, less work was done in analog applications of CNTFETs. This paper presents analog applications of CNTFET and its implementation of voltage differencing transconductance amplifier (VDTA). The CNTFET VDTA based filters and oscillators were proposed. The VDTA circuits are resistorless and can be tuned electronically only by changing transconductance. The proposed CNTFET VDTA shows power consumption of 4000 times less than compared to silicon CMOS technology and a significant reduction in chip area. All simulations were performed using SPICE and MATLAB simulation tools.

**Keywords:** Carbon Nanotube (CNT); Carbon Nanotube Field Effect Transistors(CNTFET); Voltage differencing Transconductance Amplifiers (VDTA); MOSFETS

# Univerzalni filtri in oscilatorji na osnovi napetostnega transkonduktančnega ojačevalnika v tehnologiji 32 nm poljskega tranzistorja z ogljikovimi nanocevkami

**Izvleček:** Poljski transistor z ogljikovimi nanocevkami (CNTFET) je močen kandidat za zamenjavo obstoječih silicijevih tranzistorjev. Balističen prenos elektronov v CNTFET kanalu omogoča nizko porabo moči in visoke frekvence. Kljub številnim digitalnim aplikacijam CNTFETov, je na analognem področju zelo malo objav. Članek opisuje uporabo CNTFET v analognem vezju napetostno diferencialnega transkonduktančnega ojačevalnika (VDTA). Vezja so brez uporov in elektronsko nastavljiva s spreminjanjem transkonduktance. Predlagano vezje ima 4000 krat nižjo porabo moči kot ekvivalentna izvedba v silicijevi CMOS tehnologiji. Simulacije so izvedenev SPICE in MATLAB okolju.

**Ključne besede:** Ogljikove nanocevke (CNT); poljski transistor z ogljikovimi nanocevkami (CNTFET); napetostno diferencalni transkonduktančni ojačevalnik (VDTA); MOSFET

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## 1 Introduction

Silicon-based MOSFETs have already reached their limits in scaling. CNTFET, with its ultra-long mean free path (MFP), looks to overcome the limitations of conventional silicon-based MOSFETs due to its unique electronic and mechanical properties. These properties come from their strong atom-to-atom bonds, ballistic or near ballistic transport, and quasi 1D features

of the CNT channel. Besides, by changing the chirality of the CNT its material properties can be changed from semiconducting to metallic. Many attempts at building CNTFET models have been reported in the literature [1-9].

Two major geometries are available for CNTFET design, which are planar and gate-all-around. Sanchez et al. have compared all available architectures and their performances [1]. Dokania et al. have proposed gate-all-around (GAA) or also known as wrap gate, analytical SPICE model [2]. The gate capacitance and drain current in the channel should be accurately designed to predict the precise performance of CNTFETs. Ahmed et al. proposed a model of the gate capacitance in which CNTs are arranged arbitrarily, unlike other models in which CNTs are placed at a fixed distance [3]. The authors of [3] have reported a 3% error with numerical simulations. Ballistic or near ballistic transport models for the drain current are proposed in [4-9]. These models are SPICE compatible, which means that the model can be easily compiled and integrated with any other circuit. The model used in this paper is from the articles [8-9].

Nizamuddin et. al proposed CNTFET and CMOS-based three-stage, hybrid operational transconductance amplifiers (OTA) [7]. Marani et al. reported improvement in DC gain by 17%, 40% less power consumption, and a decrease in output resistance by 90% in comparison to CMOS OTA [7]. Low power mixed-mode active filter using 12 CNT and 2 capacitors was presented by Zanjani et al. [14]. Jooq et al. designed CNTFET based ring oscillators suitable for the internet of things (IoT) applications [17]. Low power CNTFET based RF oscillator is reported in [18]. Digital applications of CNTFET, such as adders and multipliers can be found in papers [19-21].

Most of the CNTFET studies are limited to simulations only since commercially CNTFETs are not available. Mindy et al. have proposed a method for the production of CNTFETS in commercial silicon manufacturing facilities and reported experimental measurements of CNTFETs fabricated in two different manufacturing facilities [22]. Besides, the authors have improved the speed of the fabrication process 1100 times, by decreasing the deposition of CNT on the wafer from 48 hours to 150 seconds. Rebecca et al. have reported the first experimental data for CNTFET CMOS analog circuitry [23]. They have successfully fabricated 2 stages CTNFET CMOS op-amp with the channel length of 3 µm, which achieves the gain > 700. Thus, the basics of CNTFET technology is CMOS too. Even so, when we write CMOS, we refer to silicon-based CMOS in this paper.

The first Voltage differencing transconductance amplifier (VDTA) was introduced by D. Biolek as an active element for analog signal processing[10]. However, any author did not perform the circuit implementation and application until the authors of proposed the realization of CMOS filters using VDTA [11]. The miniaturizations of electronic gadgets are becoming mainstream in today's technology. It will get harder and harder to integrate passive inductors into nano level circuits. VDTAs can be used to simulate inductors in signal processing circuits.

This work is organized as follows: Section 2 and 3 present the fundamentals of CNTFETSs and VDTAs respectively. The simulations' results and discussion of CNTFET VDTA including its comparison with CMOS VDTA are presented in section 4. In section 5,the application example of VDTA is presented. The universal filter realization is presented in section 5.1. The simulation results of CNTFET VDTA based oscillators are presented in section 5.2. Finally, in section 6 the conclusion of this paper is presented.

## *2 Carbon nanotube field-effect transistors fundamentals*

Carbon nanotubes can be classified as single-walled and multi-walled. CNTFETs presented in this paper are made from single-walled CNTS as shown in Fig. 1. The chirality of CNT is the key parameter that determines whether a material is metal or semiconducting. There are two parameters of chirality, n and m (in some books or papers also referred to as n1 and n2). The values of these chirality parameters vary according to the rolling up method of CNT. The CNT is metallic if the difference of n and m is a multiple of 3. Otherwise, if the difference of n and m is not a multiple of 3 then the CNT is semiconducting [12-13]. The CNTFET presented in this paper is designed with semiconducting CNT.

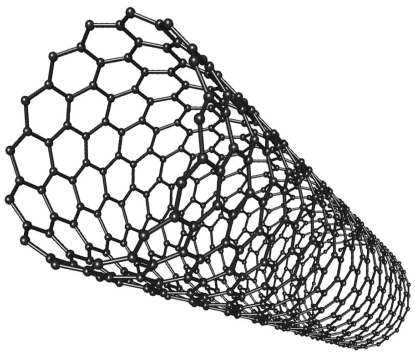


**Figure 1:** Rolled up Graphene sheet (Carbon Nanotube).

The bandgap is another key parameter which can be calculated from [12]:

$$E_G = \frac{2a_{cc}|t|}{2d} \approx \frac{0.8eV}{d} \quad (1)$$

Where, tight binging energy t is 3.0eV (also referred to as C-C bonding energy) and C-C bonding distance $a_{cc}$ of the nearest neighbor is 1.42A°. Whereas, equations for CNT diameter CNTFET threshold are given as [13]-[14]:

$$D_{CNT} = \frac{\sqrt{n^2 + m^2 + mn}}{\pi} a \quad (2)$$

$$V_T \approx \frac{aV_\pi}{\sqrt{3}eD_{CNT}} \quad (3)$$

Here, *a* (C-C unit vector length) is 0.246 nm. From equations, it is obvious that both bandgap and threshold voltages are dependent on the diameter of CNT. The width of CNTFET can be calculated from the parameters like the number of tubes, the distance between tubes, and the diameter of CNT.

$$W = (N-1)S + D_{CNT} \quad (4)$$

Numerical simulations of equations (1) and (3) were performed via MATLAB tool and the results are shown in Fig. 2 and Fig. 3. The exponential proportional dependency of CNT diameter for both bandgap and threshold voltage was observed. Both, threshold and band gap values increase as the CNT diameter value decreases.

The CNTFET model used in this research is shown in Fig. 4 [8-9;14]. The CNTs are placed under the gate separated by high-k (high dielectric constant) material. The CNT extension regions between S/D and gate are heavily doped. Default parameter values provided by authors of the model [8-9;24] are shown in Table 1.

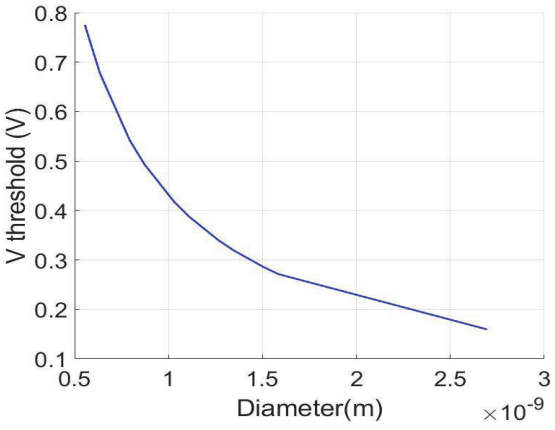



**Figure 2:** CNT Diameter vs V threshold.

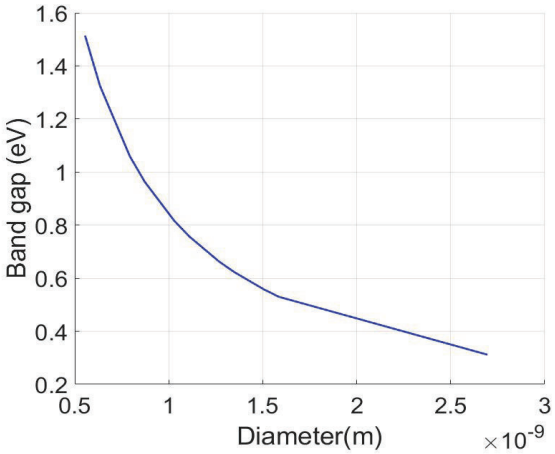
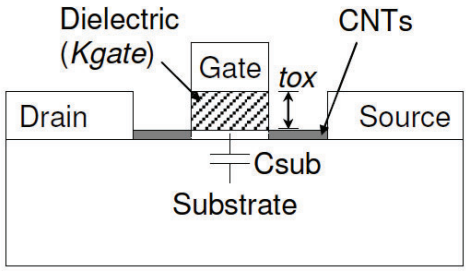



**Figure 3:** CNT Diameter vs bandgap.

(a)

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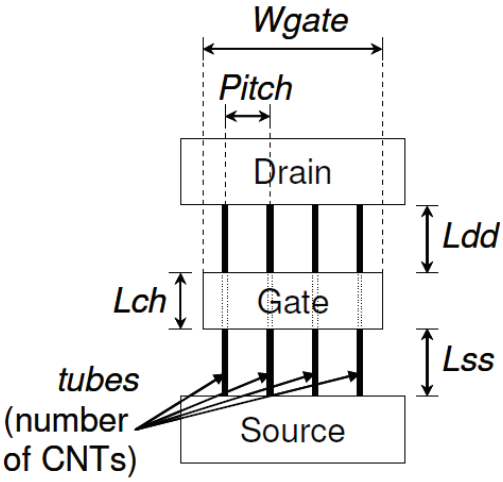


(c)

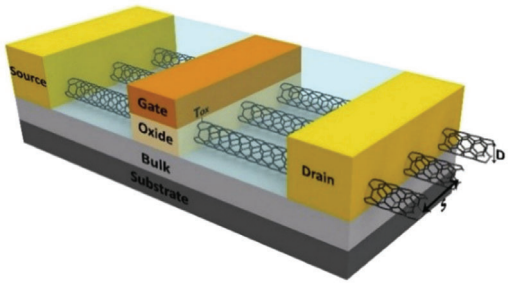


**Figure 4:** MSOFET-like CNTFET, a)1-D side view b) top view, c) 3-D view of typical TG CNTFET [8-9].

## 3 VDTA

The proposed VDTA's circuit symbol and its circuit architecture at CNTFET level are shown in Fig. 5 and Fig. 6 respectively. The VDTA is an active element with high impedance input terminals $V_P$, $V_N$, and high impedance output terminals Z, X+, and X-. The relationship between I/O terminals of an ideal VDTA can be expressed as follow [11]:

$$\begin{bmatrix} I_Z \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_{VP} \\ V_{VN} \\ V_{VZ} \end{bmatrix} \quad (5)$$

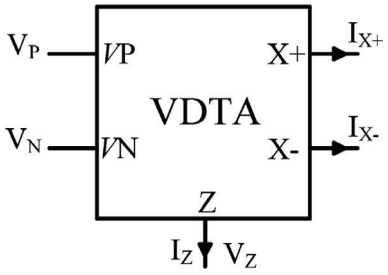


**Figure 5:** The Circuit Symbol of VDTA.

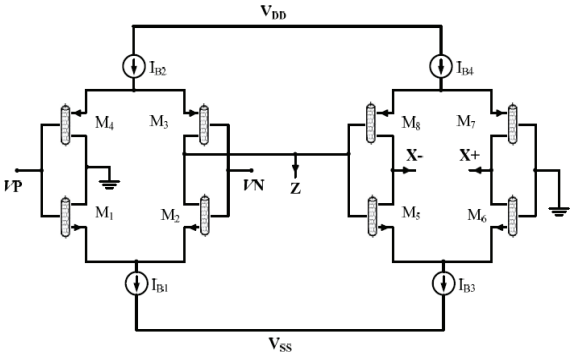


**Figure 6:** CNTFET implementation of VDTA.

Where $g_{m1}$ is the transconductance of the first stage and $g_{m2}$ is the transconductance of the second stage. The voltage difference at the input terminals P and N transforms into output currents at terminal Z by $g_{m1}$. Then the voltage at the terminal Z is converted to output currents by $g_{m2}$ at the output terminals x+ and x- [15]. VDTA can be tuned electronically by adjusting the values of $g_m$ of the first stage or second stage.

## 4 Simulations, results, and Discussions

All simulations were performed using HSPICE software. The parameters of CNT transistors used to get DC and AC characteristics of CNTFET VDTA are shown in Table 2. Supply voltages are fixed to $V_{DD} = -V_{SS} = 0.3V$ and biasing currents are –considered as $I_{B1} = I_{B2} = I_{B3} = 1\mu A$. DC varying between –0.3V and 0.3V was applied first to the P and N terminals to measure the output current and to the Z terminal. Then DC changing between –0.3V and 0.3V was applied Z terminal of VDTA to measure output currents at terminals +X and -X. The results of DC transfer characteristics for ideal current sources are shown in Fig. 7 and Fig. 8 in two steps. As expected, the output current increases as the CNT diameter increases. Because the $I_{on}$ of CNTFET increases as diameter increases due to an increase in carrier mobility and velocity [25]. For instance, in Fig. 7, the output current of CNTFET VDTA for 0.1V with CNT (7,0) is around 0,85μA, CNT (13,0) is around 0,89μA, CNT (19,0) and CNT (34,0) is 0,90 μA.

**Table 1:** Design parameters and definitions [24].

| Parameter | Definition | Value |
|---|---|---|
| Lch | Length of channel | 32nm |
| Lss, Ldd | The length of the doped CNT source/drain extension region. | 32nm |
| Pitch | The distance between the centers of two adjacent CNTs within the same device | 20nm |
| Dcnt | The diameter of Carbon Nanotubes | 1.5nm |
| Tox | The thickness of the high-k top gate dielectric material | 4nm |
| Parameter | Definition | Value |
| Kox | The dielectric constant of a high-k gate oxide material. | 16 |
| Tubes | The number of tubes in the device. | 3 |
| (n1, n2) | The chirality of tube | (19, 0) |

**Table 2:** Transistor dimension of Proposed CNFET VDTA FCS.

| Transistors | W(nm) | L(nm) | Chirality | $D_{CNT}$(nm) | Tubes |
|---|---|---|---|---|---|
| M1,M2,M5,M6 | 41.5 | 32 | 19,0 | 1.5 | 3 |
| M3,M4,M7,M8 | 221.5 | 32 | 19,0 | 1.5 | 12 |

The AC response of CNTFET VDTA for different CNT parameters is shown in Fig. 9 and Fig. 10. The same supply voltage and bias currents as in the previous section were used. Similar to DC simulations, two-step simulation and measurement was done to get the AC response of VDTA. In the first step, the input AC voltage of 1V was applied at one of the input terminals P or N, and the gain at the output terminal Z was measured. In the second step, both input terminals were grounded and the input AC voltage of 1V was applied to the Z

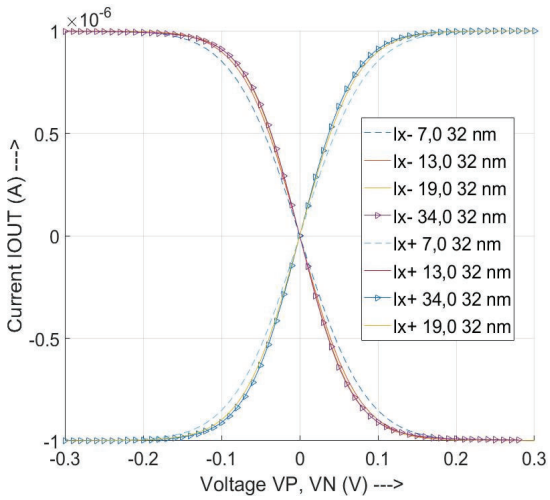


**Figure 7:** DC Characteristcs of CNTFET VDTA. Step 1 $V_{in} = V_P$ and $V_N$ vs $I_z$.

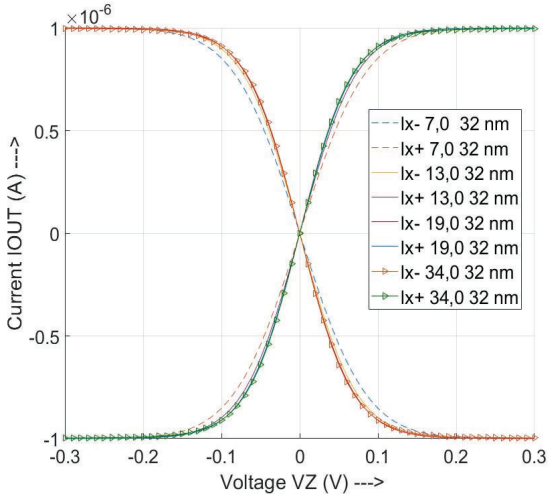


**Figure 8:** DC Characteristics of CNTFET VDTA. Step 2 $V_{in} = V_z$ vs $I_{x+}$ and $I_{x-}$.

terminal. The output gain was measured from the X+ terminal. Both steps of DC/AC simulations show the same results which prove that CNTFET VDTA is operating properly.

**Table 3:** Comparison of CNFET and CMOS technologies.

| VDTA Structure | Supply voltage | Biasing current | Power consumption | Transistor dimension N-type (channel WxL) | Transistor dimension P-type (channel WxL) |
|---|---|---|---|---|---|
| CMOS 18µm | ±0.3 | 1mA | 12mW | 1.296 µm² | 5.99904 µm² |
| CMOS 32nm | ±0.3 | 400 µA | 4.8mW | 0,00132 µm² | 0,00708 µm² |
| CNTFET 32nm | ±0.3 | 1µA | 1.2 µW | 0,00132 µm² | 0,00708 µm² |

Comparison of CMOS 0.18um, CMOS 32nm node technology VDTA, and CNFET 32 nm technology VDTA is shown in Table 3. All three architecture is designed to meet the same frequency response ($f_c \approx 3.5$ GHz). For the case of CMOS 32 nm VDTA, the DC characteristics degrade a little bit, the maximum output current does not reach the supplied ideal current source. Where CMOS 0.18 µm maximum current reaches and CNTFET VDTA maximum current reaches. Besides, even if the same dimensions (channel WxL) as for CNTFET VDTA are used for CMOS 32nm VDTA, the biasing current of 400µA is needed for CMOS 32nm technology to meet the same frequency response of CNTFET.

As we can see from graphs in DC simulations (Fig. 7-8) there is no much difference between CNT (7,0), (13,0), (19,0), and (34,0). However, the $V_{th}$ of (7,0) is much higher compared to (34,0).In AC simulations of VDTA (Fig. 9-10), we can observe a significant increase in gain with the change of CNT chirality from (7,0) to (19,0). Between (19,0) and (34,0) there is no much difference in gain but the diameter changes from 1.5 nm to 2.6 nm which will drastically increase the transistor dimension as well. Hence, we have selected CNT (19,0) for our further simulations. Another reason for selecting CNT (19,0) is to compare our simulation results with other references. Because all other works also used (19,0) CNT, including the authors of the original model from [24].

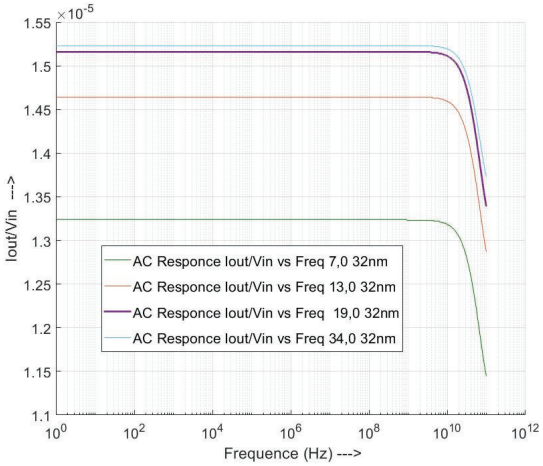


**Figure 9:** AC Characteristics of CNTFET VDTA. Step1 $V_{in} = V_P$ vs $I_z/V_P$.

## 5 Application example

VDTA has a wide range of applications in the analog signal processing field. One of them is a spectrum analyzer shown in Fig. 11. This spectrum analyzer uses low pass filters, bandpass filters, local oscillators, and mixers to get the final intermediate frequency (IF).

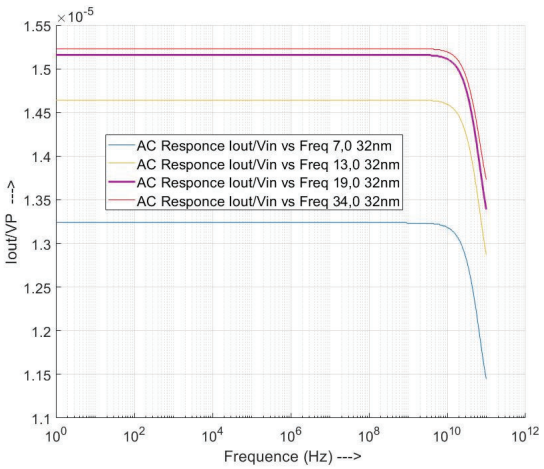


**Figure 10:** AC Characteristics of CNTFET VDTA. Step2 $V_{in} = V_z$ vs $I_{x+}/V_z$.

As an application example, this paper presents four filters and three local oscillators used in the spectrum analyzer.

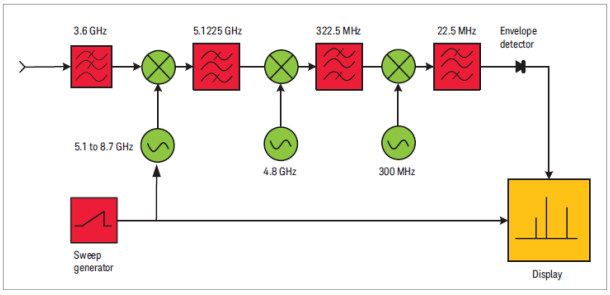


**Figure 11:** Spectrum analyzers [16].

### *5.1 Filters*

VDTA can be categorized as voltage mode and current mode. This paper presents voltage mode CNTFET VDTA. The realization of CNTFET voltage mode VDTA derived from ref [11] is shown in Fig. 6. Further, the universal filter topology of CNTFET VDTA is proposed as shown in Fig. 12. The presented CNTFET VDTA filter can operate as LP and BP filter.

The transfer function of the filter is as follow:
If $V_1 = V_{IN}$ then

$$BP \rightarrow \frac{V_{O1}}{V_{IN}} = \frac{sC_1 g_{m1}}{s^2 C_1 C_2 + sC_1 g_{m2} + g_{m1} g_{m2}} \tag{6}$$

$$LP \rightarrow \frac{V_{O2}}{V_{IN}} = \frac{g_{m1} g_{m2}}{s^2 C_1 C_2 + sC_1 g_{m2} + g_{m1} g_{m2}} \tag{7}$$

And the expressions for Quality factor and natural frequency are given below:

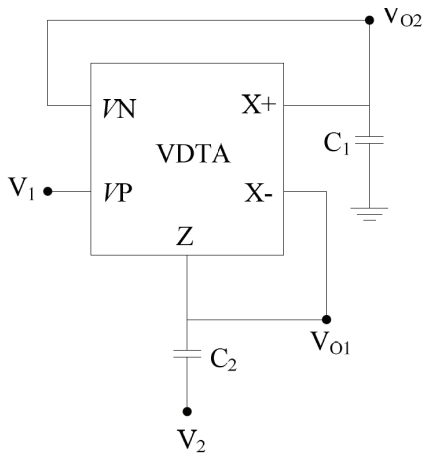


**Figure 12:** Application of proposed CNTFET VDTA filter.

$$w = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{8}$$

$$Q = \sqrt{\frac{C_2 g_{m1}}{C_1 g_{m2}}} \tag{9}$$

The filter blocks from Fig. 11 have been realized using proposed CNTFET VDTA from Fig.12 and the results are plotted in Fig. 13. The parameters of CNT transistors used for filter applications are shown in Table 2. The values of capacitors used for the filter application of CNTFET VDTA are shown in Table 4. The same supply voltage and bias currents as in the previous section were used. CNT (19,0) was selected for further applications of VDTA. There is no much difference between (7,0) and (19,0) CNT when the biasing current is set to 1µA. As biasing current increases, the center frequency of filters also increases due to an increase in transconductance.

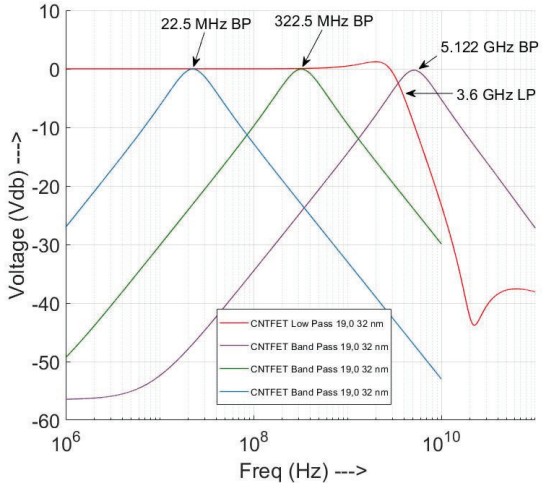


**Figure 13:** 3.6GHz LP, 5.122GHz BP, 22.5MHz BP and 322.5MHz BP filters.

**Table 4:** Capacitor values selected CNFET VDTA filters.

| Filters | C1 | C2 | Chirality n,m |
|---|---|---|---|
| 3.6 GHz LP | 80.5fF | 80.5fF | 19,0 |
| 5.122 GHz BP | 0.4334fF | 0.4334fF | 19,0 |
| 322.5 MHz BP<br>22.5 MHz BP | 74.5pF<br>10.72pF | 74.5pF<br>10.72pF | 19,0<br>19,0 |

### *5.2 Oscillator*

The oscillator is a DC to AC converter, which converts DC input signals to AC output signals such as sinusoidal waves. Local oscillators are used to change the frequency of the signal as in a spectrum analyzer from Fig. 11 and along with mixers, they improve the performance of receivers in electronic circuits. The circuit symbol of the CNTFET VDTA oscillator is shown in Fig. 14. The oscillator blocks from Fig. 11 have been realized using the proposed oscillator structure.

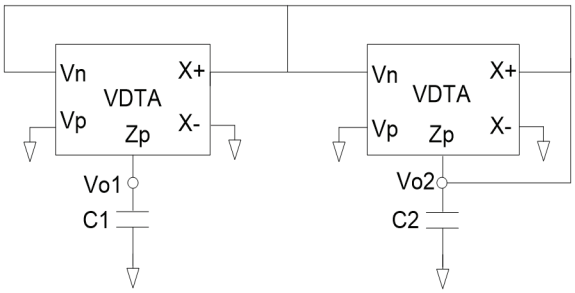


**Figure 14:** Application of proposed CNTFET VDTA quadrature oscillator.

The circuit analysis of the second-order characteristical equation can be represented as:

$$s^2C_1C_2 + sC_2(g_{m3} - g_{m4}) + g_{m1}g_{m2} = 0 \quad (10)$$

$$g_{m3} = g_{m4} \quad (11)$$

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad (12)$$

Where $g_{m3} = g_{m4}$ is the condition for oscillation and ωo is oscillation frequency. The parameters of CNT transistors used for oscillators applications are shown in Table 5. Supply voltages are fixed to $V_{DD} = -V_{SS} = 0.3V$ and biasing currents are considered as $I_{B1} = I_{B2} = I_{B3} =$ 1μA. The simulation results are plotted through Fig. 15-Fig. 17.

**Table 5:** Transistor dimension of proposed CNFET VDTA oscillator.

| Transistors | W(nm) | L(nm) | Chirality | $D_{CNT}$(nm) | Tubes |
|---|---|---|---|---|---|
| M1,M2,M5,M6 | 221.5 | 32 | 19,0 | 1.5 | 12 |
| M3,M4,M7,M8 | 1121.5 | 32 | 19,0 | 1.5 | 57 |

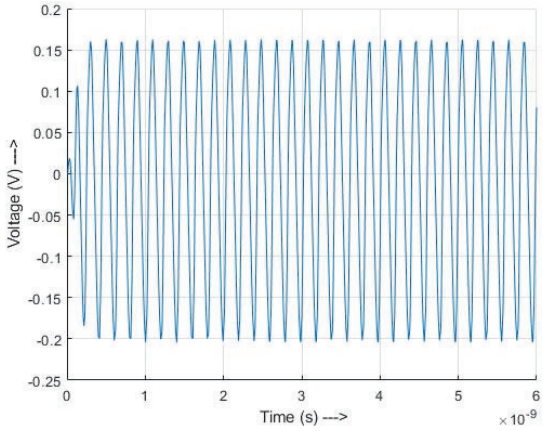


**Figure 15:** 5.1 GHz VDTA Based Oscillator C1=C2 =0.068fF.

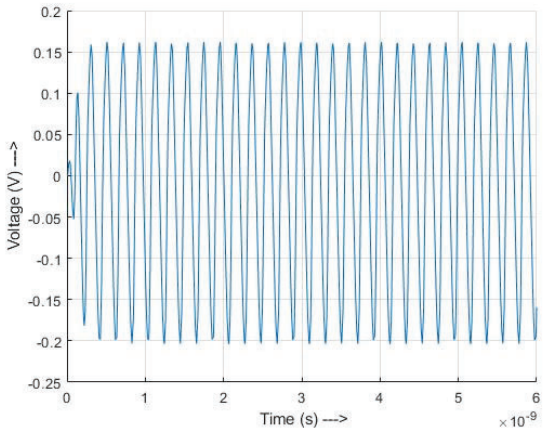


**Figure 16:** 4.8 GHz VDTA Based Oscillator C1=C2 =0.08fF.

## *6 Conclusion*

Ultra-low-power CNTFET based VDTA filters and oscillators were presented. As shown in Table 3. CNTFET 32 nm based VDTAs consume the power of 4000 times less than CMOS 32nm based VDTAs. Also, n-type CNTFETS occupy approximately 989 times less than space in the chip area (only considering effective channel WxL) compared to n-type MOSFET transistors while p-type CNTFETS occupy approximately 848 times less space(only considering effective channel WxL)

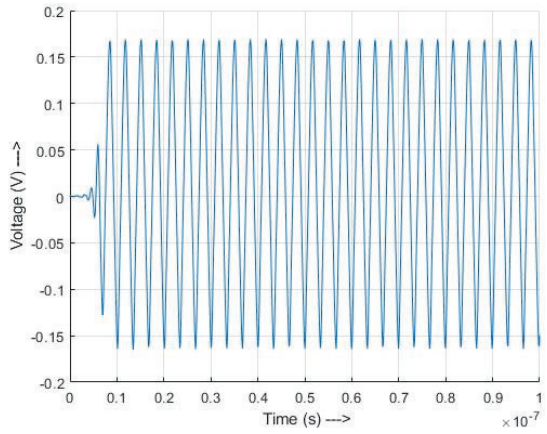


**Figure 17:** 300 MHz VDTA Based Oscillator C1=C2 =3.9fF.

compared to p-type 0.18µm technology node MOSFETS used in typical VDTAs. Higher biasing current or capacitors may be adjusted to change the center frequency of CNTFET filters. CNTFET VDTA based filters and first-ever CNTFET VDTA based oscillators for spectrum analyzer are presented as an application example.

## 7 Conflict of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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# Hardware Implementation of Chaotic Zigzag Map Based Bitwise Dynamical Pseudo Random Number Generator on Field-Programmable Gate Array

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**Abstract:** In this study, successful real-time hardware implementation of discrete-time chaotic zigzag map as a random number generator (RNG) on field-programmable gate array (FPGA) environment is presented. For the hardware modelling of the application, ready-to-use modules defined on 32-bit floating-point numbers and hardware description language (VHDL) are used. In the study, the non-linear dynamic behaviour of the chaotic generator synthesized on the Altera Cyclone IV GX FPGA chip is examined in terms of critical cryptographic competences such as system reliability and statistical randomness quality. The random numbers with poor statistical quality in the system are obtained by passing 32-bit chaotic trajectory outputs through a simple comparison circuit. In order to improve the statistical sufficiency of these numbers, the H function post-processing technique is used. In addition, statistical verification and hardware performance analysis of the generator through NIST 800-22 tests and FPGA chip statistics are presented in the study. The obtained successful results show that the zigzag map can be used in different chaos-based engineering applications, including embedded cryptographic applications. In addition, the low area-energy requirement of PRNG in terms of modelling technique facilitates its practical applicability on resource-restricted applications and architectures.

**Keywords:** FPGA; pseudo-random number generator; chaotic zigzag map; H function

# Strojna implementacija bitnega dinamičnega psevdo-random generatorja števil v FPGA na osnovi kaotične zigzag karte

**Izvleček:** Članek predstavlja strojno implementacijo časovno disktretne kaotične zigzag karte kot generator naključnih števil v FPGA okolju. Za strojno modeliranje aplikacije je uporabljen VHDL skriptni jezik. V smislu kvalitete naključnosti in zanesljivost je raziskano nelinearno dinamično obnašanje kaotičnega generatorja na Altera Cyclone IV GX FPGA čipu. Naključna števila s slabo statistično kvaliteto so dobljena s posredovanjem 32-bitne kaotične trajektorije v enostavno primerjalno vezje. Za izboljšpanje njihove kvalitete je uporabljena tehnika post procesiranja s H funkcijo. Dodatno je statistična verifikacija preverjena z NIST 800-22 testi in statistiko FPGA čipa. Rezultati nakazujejo možnost uporabe zigzag kart v različnih kaotičnih aplikacijah vključno s kriptografijo.

**Ključne besede:** FPGA; pseudo naključen generator števil; kaotična zigzag karta; H funkcija

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## 1 Introduction

In addition to cryptography, randomness is a common statistical concept for many areas such as game theory, simulation, statistic, quantum mechanics, programming and entertainment. This common concept, unlike other fields, corresponds to randomly distributed bit-level random numbers acquired from a specific entropy source in cryptography are not reproducible and predictable. In cryptography, random numbers can be obtained from two different design classes, namely

True Random Number Generators (TRNG) using physical noise sources and Pseudo Random Number Generators (PRNG) with deterministic structure. Although their output is unpredictable, TRNGs are susceptible to environmental changes and mostly offer hardware-dependent, slow and costly solutions [1-3].

Despite fulfilling an important cryptographic requirement such as unpredictability in terms of system security, statistical weakness is the most obvious deficiency of a physical TRNG. For PRNGs where random numbers with good statistical properties can be obtained at low cost, determinism and periodicity are the most important shortcomings of this design class. PRNGs are preferred due to their practical structure to obtain random numbers within cryptographic applications. However, due to the nature of determinism, the initial conditions and system parameters are decisive in the development of future states of PRNGs, unlike randomness. This case leading to predictability, limits the use of PRNGs for sensitive cryptographic applications. Furthermore, knowing the initial conditions (parameters) that contain all the entropy of the deterministic system, can completely remove the cryptographic confidentiality required for PRNGs [4-5].

Chaos theory is an important concept that has found application in many different disciplines such as biology, philosophy, meteorology, physics and sociology as well as different branches of engineering [4]. Chaos can be roughly defined as an irregular and unpredictable random behavior pattern observed in non-linear deterministic systems that are exponentially sensitive to initial conditions. The deterministic characteristic of chaotic systems is the most prominent feature distinguishing them from noise-based non-deterministic systems preferred for sensitive cryptographic applications. Due to their deterministic properties, the future states of chaotic systems can be predicted theoretically if the initial states are known exactly. However, in these systems characterized by a strong exponential dependence on the initial conditions, a very small error in the initial conditions due to the positive Lyapunov exponential can cause large deviations, also known as the butterfly effect, in the system trajectories evolving in time. Therefore, this divergent character can provide sufficient level of cryptographic secrecy by making the long-term estimation of dynamic system outputs in chaos state impossible [6-7].

Chaotic systems are divided into discrete and continuous time chaotic systems according to their mathematical modeling. In continuous chaotic systems, the evolution of the system is given by ordinary differential equations. It depends on the rate of change of the system's state variables. In discrete time, where the evolution of the system depends on the values of state variables, chaotic systems are expressed by simple non-linear equations [3, 8]. For both chaotic system models, exponential sensitivity to the initial conditions and the ability to produce long-term non-periodic oscillations are the basic characteristics of these systems coinciding with the pattern of random behavior. These basic characteristics of chaos, which are similar to the confusion and diffusion properties, also known as Shannon principles, are used for different purposes in cryptography such as video [9], audio [10], image [11] encryption schemes, stream cipher [12], s-box design [13], post-processing techniques [14] and secure additional input [2]. Random number generation is another important use of chaos theory in cryptography. Chaotic systems can often be used as entropy source in hardware-based PRNG and TRNG designs, especially because they eliminate the need for difficult and complex processes, such as obtaining and processing noise signals based on physical randomness.

In practice, the prediction of the future state information of the chaotic system is limited by the measurement sensitivity of the initial state information. Whereas, the lack of infinite measurement sensitivity from the circuit nodes depending on the presence of electrical noise makes it almost impossible to accurately determine the initial conditions of the chaotic system for hardware implementations. Therefore, hardware modeled chaotic systems alone can provide the reliability (security) and unpredictability needed cryptographically, unlike a simple deterministic PRNG [8].

In the literature, there are different chaos-based PRNG and TRNG paradigms implemented with FPGA chips offering important facilities such as flexibility, ease of modelling, low power consumption, parallel processing and speed. Some of these studies can be summarized as follows: Özkaynak [7] proposed an easily applicable RNG model on FPGA chips, which could be an alternative to discrete time chaotic systems using the fractional order Chua system. Tuna et al. [15] modelled the autonomous Lü-Chen chaotic system on Xilinx Virtex-6 FPGA chip using the Heun numerical method and presented a high-speed chaotic oscillator design that can be used for embedded cryptographic applications. In another study, Tuna [16] presented a real-time implementation of a PRNG using an artificial neural network (ANN) based 2D chaotic oscillator on Xilinx Virtex 6 FPGA chip in four different scenarios. Koyuncu and Özcerit [17] modeled the continuous-time Sundarapandian – Pehlivan chaotic system using the Range-Kutta (RK4) numerical analysis method as RNG on the same FPGA chip. De la Fraga et al. [18] presented the hardware modeling of a PRNG based on four different discrete time chaotic system scenarios in their study

used Xilinx FPGA Spartan 3E FPGA chip. Koyuncu et al. [19] proposed the use of a new chaos-RO based dual entropy core TRNG architecture using the Xilinx Virtex-6 FPGA chip. A new three-dimensional continuous-time autonomous chaotic oscillator (P3DS) has been used as the deterministic component of TRNG. In another study, Meranza-Castillón et al. [20] provided the hardware implementation of a chaotic enhanced Hénon map (EHM) based PRNG that can be used for image and video ecryption systems on the Altera DE2-115 FPGA chip. Garcia Bosque et al. [21] presented a logistic map based PRNG implementation on Xilinx Virtex 7 chip in which chaotic system parameters change dynamically to prevent the system to fall into short period orbits as well as increasing the statistical randomness quality. Kanzadi et al. [22] proposed a double entropy sourced PRNG architecture on the Xilinx Spartan 3 FPGA chip, combining the tent and logistic map outputs with the exclusive-OR (XOR) gate. In [23], another logistic map based study Tuncer proposed physical unclonable functions based on ring oscillator (RO-PUF) and logistic map to generate pseudorandom numbers. The generator was implemented in Altera Cyclone II FPGA chip with VHDL language. Çiçek et al. [24] proposed a TRNG architecture using a discrete time double entropy resource to overcome the intrinsic limited entropy problem of conventional single entropy core architectures by using hardware redundancy.

In this study, hardware implementation and performance evaluation of an FPGA-based PRNG using chaotic zigzag map as entropy source is given. The statistical and spectral properties of the chaotic time series obtained from the implemented system are analyzed cryptographically. The NIST 800-22 randomness test is used for statistical verification of random numbers obtained from chaotic time series. The presented study is important in terms of demonstrating the applicability of the modeled chaotic system for different chaos-based cryptographic purposes such as secure communication, video and image encryption and s-box design in addition to random number generation. Furthermore, chaotic PRNG can be easily used in resource-restricted architectures and cryptographic applications due to its low area-energy consumption.

The rest of the paper is organized as follows: In Chapter 2, theoretical details of the chaotic system are given. Details of the digital implementation of proposed PRNG on FPGA environment are presented in Chapter 3. In Chapters 4 the hardware performance and statistical success of chaos-based RNG have been analyzed cryptographically, respectively. The study is concluded by interpreting the results obtained in Chapter 5.

## 2 Chaotic zigzag map

The discrete-time one-dimensional chaotic zigzag map whose mathematical definition is given in Eq. 1, is proposed by Nejati and Beirami in [5]. In Eq. 1, $m$ is the state variable of the chaotic system and changes in the (- 3,3) closed interval. The zigzag map can display stable or chaotic behavior for different $m$ values in the defined interval. The bifurcation diagram given in Fig. 1 can be used to identify the chaotic behavior of the system for these changes. In Fig. 1, for $|m| < 1$ values its behavior is stable, while for intervals $m \in (2,1), (1,2), [3,2)$ and $(2,3]$ its behavior is chaotic. Especially for $m \in [3,2)$ and $(2,3]$ intervals, the $x_n$ output values of the system in chaos state occur with a large irregularity in the [-1,1] interval. For the same intervals, the $x_n$ output values of the chaotic system tend to infinity for large n values representing the iteration step. For $|m| = 2$, the map converges to 0 [5, 18].

$$x_{n+1} = \begin{cases} -m\left(x_n + \dfrac{2}{|m|}\right), & \text{for } x_n \in \left(-1, -\dfrac{1}{|m|}\right] \\ mx_n & \text{for } x_n \in \left(-\dfrac{1}{|m|}, \dfrac{1}{|m|}\right] \\ -m\left(x_n - \dfrac{2}{|m|}\right), & \text{for } x_n \in \left(\dfrac{1}{|m|}, 1\right] \end{cases} \quad (1)$$

In Eq. 1, the $x_n$ output values oscillating in the [-1,1] interval for the zigzag map are 32-bit floating-point (real number) format. Eq. 2 is used to obtain one-bit random numbers from these 32-bit numbers in each iteration. In Eq. 2, the $x_n$ output values normalized to the [0,1] interval, are compared with the threshold value and random bit sequences are attained.

$$b_{n+1} = \begin{cases} 1, & |x_n| > 0.5 \\ 0, & |x_n| < 0.5 \end{cases} \quad (2)$$

## 3 Implementation details of FPGA-based real-time chaotic zigzag map

The chaotic system in accordance with the 32-bit IEEE 754 floating-point number standard is designed to be operated on FPGA chips. The Quartus Prime Lite Edition 17.1 design software and the Altera Cyclone IV EP-C4GX150 FPGA chip are used together for synthesis and placement during the hardware implementation phase. In the chaotic system, Intel FPGA Intellectual Property (IP) cores library with ready-to-use circuit elements de-

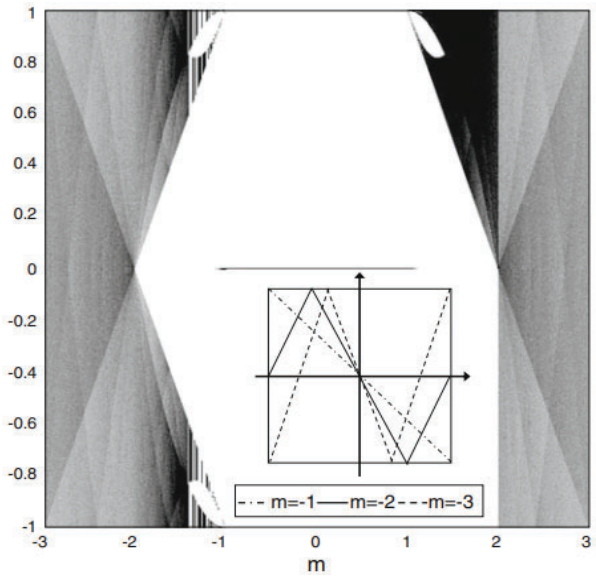


**Figure 1:** Bifurcation diagram for zigzag map

fined on floating-point numbers is used for multiplication, division, addition, subtraction and comparison operations. In addition to this, all other definitions and circuit elements needed in the system are designed by VHDL dataflow and behavioral coding technique.

The top-level block representation of the PRNG created by schematic and dataflow design techniques is shown in Fig. 2. The operating logic of the system given in Fig. 2 can be briefly described as follows: In Fig. 2, 32-bit $x_0$ and $x_n$ values represent the seed and output values of the chaotic system, respectively. When the chaotic system starts to work, the seed value $x_0$ is applied as input to the system and after a certain calculation time, the output value $x_1$ is obtained. This case is the initial position for the chaotic system and the output of the system is constant at value $x_1$, in this position. In order to obtain random numbers from the chaotic system, starting from $x_1$ value, the generated all $x_n$ values should be applied as input to the system, respectively. This case is called the feedback position for the chaotic system.

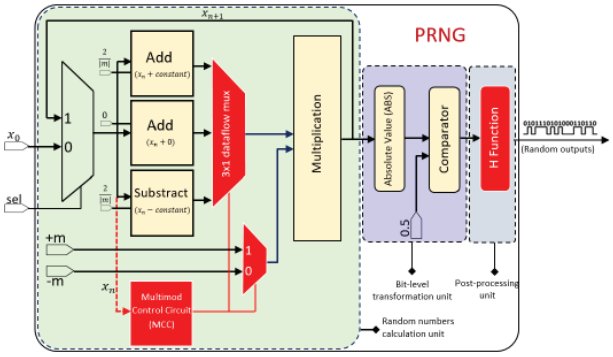


**Figure 2:** Top-level schematic diagram of zigzag map based PRNG

The chaotic system generates random numbers dynamically, when in the feedback position, different

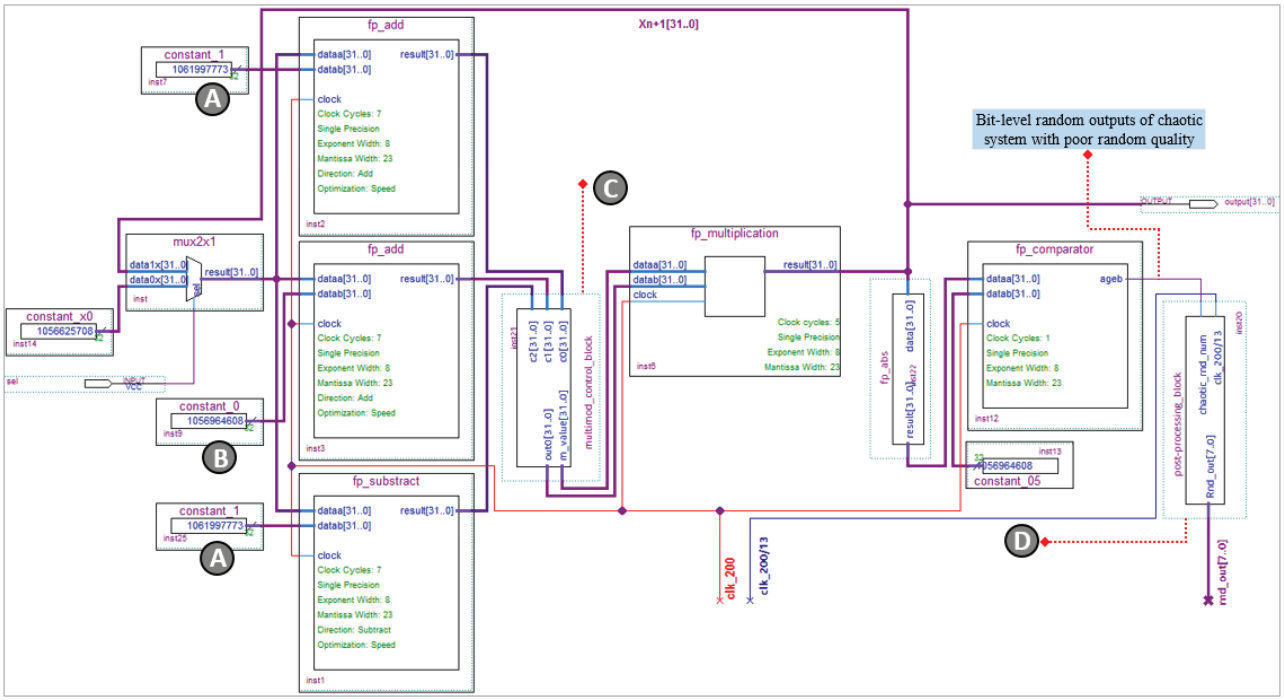


**Figure 3:** Hardware modeling of zigzag map in Quartus environment. In figure (A) is the common 2/|m| constant for Equation 1. (B) is the 0 (zero) constant used to ensure synchronization in the modeling phase. (C) and (D) are dataflow designed multi-mode control and post-processing circuit elements, respectively

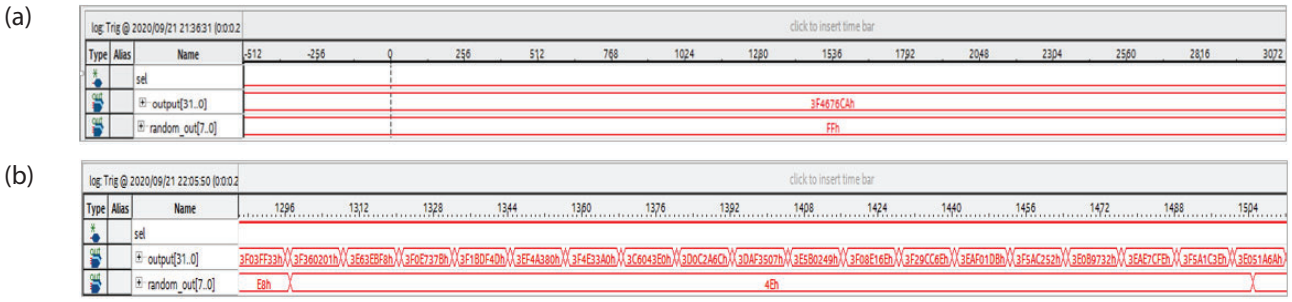


**Figure 4:** Real time simulation results of the zigzag map for (a) initial and (b) feedback positions

from the initial position. A triggering signal (sel) obtained from the physical ambiance is used as the selection pin of the mux at the input of the chaotic system to enable the transition between these positions. In order to obtain bit-level random oscillations (numbers) at the output of the PRNG, the 32-bit chaotic $x_n$ random numbers are passed through the digitization and post-processing blocks, respectively. Quartus modeling of PRNG whose schematic structure is given in Fig. 2 as in Fig. 3. Real-time simulation of 32-bit hexadecimal random outputs representing the chaotic trajectory for the modeled zigzag map is as in Fig. 4.

For the mathematical operations, two addition (fp_add), one subtraction (fp_substract), one multiplication (fp_multiplication), and one absolute value (fp_abs), ready-to-use IP core modules which are able to do calculations with floating-point numbers are used in Fig. 3. In addition to these ready-to-use circuit modules, two dataflow designed block circuit elements (multimod_control_block & post_processing_block) are used in Fig. 3 (C) and (D).

In the initial position, the input values of the chaotic system $x_0$ and m are 0.4898 and 2.5, respectively. The parameter  is the common factor of the three different equalities in Eq. 1. For this reason, instead of calculating the common (2/|$m$|) expression for the first and third equalities in Eq. 1 in each iteration, the mathematical equivalent of this expression is defined as constant (constant_1) as in Figure 3 (A). Therefore, the hardware equivalent of the equalities in Eq. 1 is (-$m$($x_n$ + constant)), ($m$($x_n$ + 0)) and ($m$($x_n$ - constant)) respectively in Fig. 3. In the system, it is important that the calculation time is the same for all three equalities in terms of synchronization. For this purpose, for the second equality consisting of only multiplication, the addition with 0 (zero) constant is made as in Fig. 3 (B). Thus, the calculation times of the parallel connected ($x_n$ + constant), ($x_n$ + 0) and ($x_n$ - constant) expressions were equalized in 7 clock pulses. The calculated results at each 7 clock pulses are simultaneously applied to $c_1$, $c_2$ and $c_3$ inputs of the multimode control circuit in Fig. 3 (C), respectively.

The outputs of the control circuit whose hardware modelling details are given in Fig. 5 are connected to the inputs of the multiplication circuit. The mathematical definition of the zigzag map consists of three different equations. Which equality will be used in the system is decided by looking at interval of the $x_n$ values. The main task of the multimode control circuit in Fig. 5 is to determine which equality result should be used by checking the $x_n$ interval and whether the common factor is positive or negative. For this, the dataflow designed circuit element (output_controller) in Figure 5 (A) is used. The task of this component is to determine the interval of $x_n$ by checking the c1 input to which the ($x_n$ + 0) addition result is connected. The multimode control circuit in Fig. 5 has two 32-bit vectorial outputs, out0 and m_value. The *out*0 output is switched to one of the input values $c_1$, $c_2$ and $c_3$ in accordance with the $x_n$ interval. When *out*0 output is switched to $c_1$ input, *m_value* output takes +$m$, in other cases ($c_0$, $c_2$) -$m$ values.

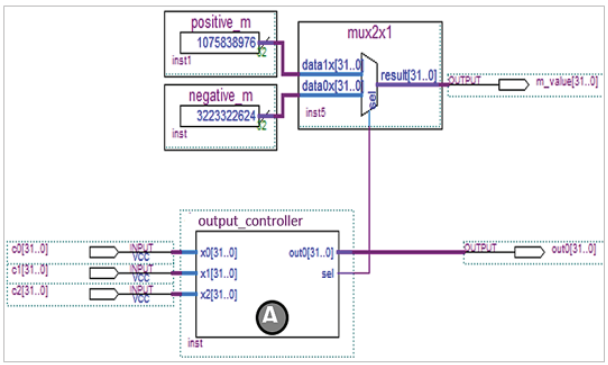


**Figure 5:** Hardware modelling of the multimode control block

The calculation time required for multiplication in the system takes 5 clock pulses. With the addition, the calculation time required to obtain a 32-bit $x_n$ random number in any iteration from the chaotic system is 12 clock pulses in total. The 32-bit random numbers whose absolute value is taken after the multiplication are applied as an input to the comparison circuit (fp_comparator) in Fig.3. The calculation time of the comparison circuit is 1 clock pulse and performs bit-level transformations according to Eq. 2. However, the sta-

tistical randomness quality of the random numbers obtained for the threshold value, selected as 0.5 in Eq. 2, is cryptographically insufficient. Random numbers obtained from the chaotic system are applied to the input of the post processing block in Fig. 3 (D) to remove this shortcoming. The hardware modeling details of this block circuit, in which H function [25] post-processing technique is used, are as in Fig. 6.

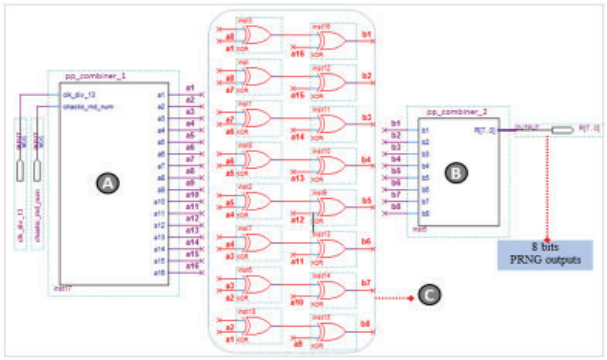


**Figure 6:** Hardware modelling of post-processing block

The post-processing technique in Fig. 6. consists of two combiner circuits (pp_combiner1 & pp_combiner_2), used to obtain the desired bit-level logic vectorial inputs and outputs, in (A) and (B) and the H function in (C). The H function post-processing technique based on Quasigroup transformation needs 16-bit vectorial input obtained from chaotic system trajectory to produce 8-bit vectorial random output in each iteration. The task of the first combiner circuit (pp_combiner_1) in Fig. 6 (A) is to combine one-bit random numbers generated in every 13 clock pulses and to obtain 16-bit logic vector inputs needed for the post-processing technique. Then, the random numbers passed through the XOR based H function block in Fig. 6 (C) are finally applied as an input to the other combiner circuit (pp_combiner_2) in Fig. 6 (B). The 8-bit combined outputs of this circuit are also the hexadecimal outputs of PRNG.

The frequency of the clock signal applied to the input of the chaotic system is 200 MHz. The time to generate a 1-bit random sign / number for PRNG is 13 clock pulses depending on the calculation time of the chaotic system. In other words, for a 200 MHz clock sign with a period of 5 ns, the chaotic system produces a one-bit random number every 65 (13x5) ns. Hence, the output bit rate of PRNG is 200/13 = 15.4 Mbit/s without post-processing technique. However, the post-processing technique reduces the output bit rate of the chaos-based generator by 1/2. For this reason, the final output bit rate of chaotic PRNG drops to 15.4/2 = 7.7 Mbit/s after the post-processing technique is applied.

The time to obtain 16 bit-length random number sequences for the post-processing technique in the system is 208 (13x16) clock pulses. The 8-bit random numbers generated by PRNG every 208 clock pulses, and the 32-bit outputs of the zigzag map are recorded in two different memory architectures for testing purposes, as in Fig. 7 (A) and (B). Column widths of these memory architectures consisting of 65.536 rows are 8 and 32 bits, respectively. In both memory architectures, 16-bit counters are used for addressing. The memory architecture in Fig. 7 (A) is used for statistical analysis, while the memory architecture in (B) is used to verify the existence of chaos in the system for time series derived from the zigzag map. The frequencies of the clock signal applied to the input of the counter and memory architectures are 960 KHz (200/208) and 16.7 (200/12) MHz, respectively.

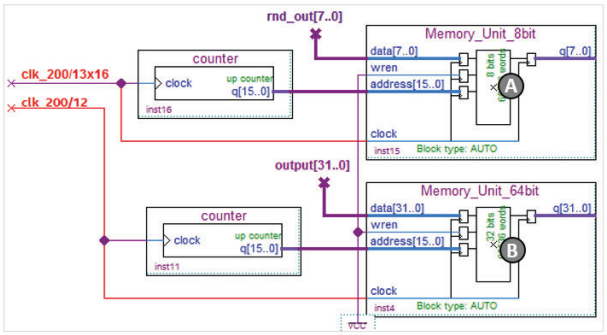


**Figure 7:** Memory architectures used for testing in the system

## 4 Experimental validation

Experimental analysis of the study is carried out in three stages. In the first stage, the existence of chaos in the system for zigzag map and exponential sensitivity of PRNG to initial conditions are analysed. In the second stage, statistical analysis of bit-level numbers obtained from chaotic time series is performed. In the last stage, the hardware design criteria of the proposed PRNG are examined and its performance based on these criteria is compared with other studies in the literature.

### 4.1 Lyapunov exponent analysis

The most distinctive feature distinguishing chaotic systems from other nonlinear systems is the exponential sensitivity to initial conditions, also known as the Butterfly Effect. The Lyapunov exponent is one of the frequently used method for analysing chaos in nonlinear systems and demonstrating the sensitive dependence of the system on initial conditions. The λ can be defined as the quantitative measurement of the amount of divergence and convergence in the phase space of two trajectories starting at very close points to each other. The existence of chaos in a nonlinear deterministic sys-

tem can be determined by looking at the sign of the λ value calculated as in the Eq. 3 of at least one trajectory. For at least one Lyapunov exponent greater than zero, the behaviour of the analysed system is defined as chaotic [18, 26]. The Lyapunov spectrum of the time series of the zigzag map obtained from the memory component in Fig. 7 (B) and the distributions of these series for the range [-1, 1] are as in Fig. 8 and 9 respectively.

$$\lambda = \lim_{n\to\infty} \frac{1}{n} \sum_{i=0}^{n-1} ln \mid f'(x_i \mid \tag{3}$$

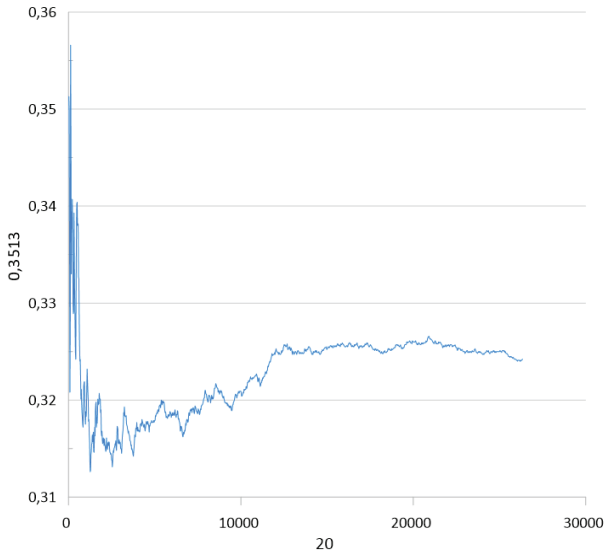


**Figure 8:** Lyapunov spectrum of the zigzag map

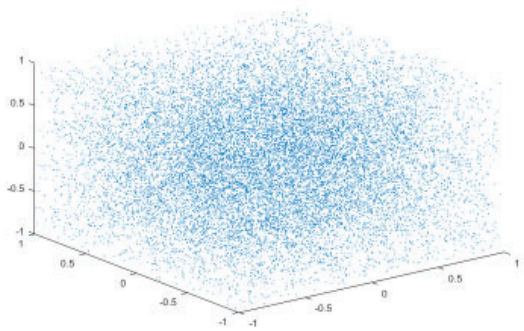

**Figure 9:** Distribution of time series obtained from chaotic system

The positive Lyapunov exponent in Fig. 8 confirms that the zigzag map for $x_0$ and $m$ input values is in chaos and the system display a random-like behaviour. This case also shows that the chaotic system exhibits non-periodic behaviour and that orbital outputs are unpredictable in long-term. This also shows that the orbital outputs of the chaotic system exhibiting non-periodic behaviour are unpredictable in the long-term and in this case, cryptographically reliable random numbers can be obtained from PRNG.

### *4.2 Statistical randomness analysis*

In the presented study, NIST SP 800-22 statistical randomness test suite [27] is used to verify the statistical sufficiency of PRNG. The test technique consists of 15 separate subtest criteria and calculates the α and p-value parameters for each test criterion. The p-value parameter, which is the probability random numbers are generated from an ideal RNG, varies in the range [0-1]. If p-value equals 1 for a test criterion, the sequence of numbers for the relevant test criterion is considered to be perfectly random. Otherwise, there is no randomness for the relevant test criterion. The α parameter, corresponding to the typical significance level, is in the [0.001– 0.01]. range. For $\alpha = 0.01$, TRNG is considered to correctly produce 99 out of every 100 random number sequences. For the numbers testing, the p-value parameter for each test criterion must be greater than the α parameter [3, 28]. The sample length of each random number sequence tested is equivalent to the memory capacity in Fig. 7 (A). In other words, a random number sequence obtained from the PRNG for testing purposes at once time, consists of 524.288 (65.536x8) bits. The measured NIST 800-22 test results for PRNG are given in Table 1.

**Table 1:** NIST 800-22 test results

| Test Name | p-value | Result |
|---|---|---|
| Frequency test | 0.703 | Success |
| Frequency test within a block | 0.728 | Success |
| Run test | 0.594 | Success |
| Test for the longest run of ones in a block | 0.512 | Success |
| Binary matrix rank | 0.679 | Success |
| Discrete Fourier transform | 0.912 | Success |
| Non-Overlapping template matching | 0.500 | Success |
| The overlapping template matching test | 0.490 | Success |
| Maurer's universal statistical test | 0.338 | Success |
| Linear complexity test | 0.697<br>0.415 | Success |
| Serial test | 0.793 | Success |
| Approximate entropy test | 0.654 | Success |
| Cumulative sums | 0.871 | Success |

In order for the outputs of any PRNG or TRNG to be used directly in cryptography, the randomness quality of the generator must be verified by statistical testing tools. In Table 1, the p-value > α condition has been fulfilled in all of the test criteria for the post-processed random

numbers. In this case, where the test criteria are considered successful, it can be said that the proposed zigzag map-based generator fulfils cryptographic requirements in terms of statistical randomness. The obtained results are important in terms of showing that the zigzag map can be used for different cryptographic purposes, especially random number generation methods.

### *4.3 Hardware performance analysis*

The area-energy requirement of any cryptographic RNG is important in terms of evaluating the applicability of the generator on today's cryptographic applications and devices, where area-energy consumption is a major problem [3, 14]. Despite having statistically impressive results, solutions with high structural complexity applied for security requirement can often make an RNG dysfunctional. Therefore, hardware cost analysis of any RNG is important in respect to evaluating the practical usefulness of the generator. For this reason, it is important for an RNG to fulfil the security-related statistical requirements with minimum hardware cost in terms of the efficiency of the cryptographic applications they are used.

Although based on simple mathematical definitions, the fact that chaotic orbital outputs consist of three different equalities increases the complexity of the zigzag map in terms of hardware implementation. However, besides the ready IP modules, the dataflow designed circuit elements in Fig. 3 (C) and (D) reduce this complexity as much as possible in terms of hardware. Especially since the ($m \,.\, x_n$) factor is common in all three equalities, only one multiplication circuit is used with the help of the control circuit in Fig. 3 (C) instead of three different multiplication circuits. In addition, in Eq.1, $2/|m|$ expression is common for the first and third equalities. For any initial value of the system parameter $m$, the value of this expression will not change during the running time of the PRNG. Therefore, instead of using extra division and absolute value circuits to calculate the value of this expression in the implementation phase, the mathematical equivalent of this expression is defined as constant circuit element as in Fig. 3 (A). This also simplifies the implementation of the chaotic generator as well as reducing the area-energy demand. The area-energy consumption parameters of the proposed zigzag map-based generator after the place-routing process is performed on FPGA chip are shown in Table 2.

**Table 3:** Comparison of the main characteristics of different chaos-based RNG proposals in the literature

| Ref. | Chaotic System | Hardware Characteristic | Test Tool | Frequency (MHz) | Post-Processing | Throughput (Mbps) |
|---|---|---|---|---|---|---|
| [8] | Logistic, Bernoulli and Tent Map | CMOS (0.25 µm) | NIST 800-22 | - | - | - |
| [20] | Enhanced Henon Map | FPGA | NIST 800-22 | 50 | | 3.9 |
| [21] | Logistic map | FPGA | NIST 800-22 | - | - | 1.0 |
| [24] | Bernoulli Map | FPGA | NIST 800-22 | 50 | - | 1.5 |
| [29] | Chua circuit | CMOS (0.18 µm) | FIPS 140-1 | - | 6-bit LFSR | 2.02 |
| [30] | Coupled chaotic oscillator | CMOS (0.35 µm) | FIPS 140-1 NIST 800-22 | 1.24 | Von Neumann | 2.0 |
| [31] | 3D chaotic system | FPGA | FIPS 140-1 NIST 800-22 | 373 | XOR | 4.59 |
| [32] | Tent Map | CMOS (0.18 µm) | NIST 800-22 | 250 (KHz) | 8-bit LFSR | 0.25 |
| [33] | Sprott 94 G chaotic system | FPGA | NIST 800-22 | 339 | - | - |
| [34] | Logistic and Henon map | FPGA | - | 190 | - | 1.0 |
| [35] | Piecewise-Affine Markov maps | FPGA | FIPS 140-1 | 24 | XOR | 60 (Kpbs) |
| [36] | Lorenz and Lü chaotic systems | FPGA | NIST 800-22 | 78 | - | - |
| [37] | Memristive Canonical Chua oscillator and logistic map | FPGA | NIST 800-22 | 59 | XOR | 0,1.25 |
| [38] | Time-delay chaotic system | FPGA | NIST 800-2 FIPS 140-2 | 120 | - | 4.0 |
| [39] | Sinusoidal iterator | FPGA | NIST 800-22 | 200 | - | 4.77 |
| This study | Zigzag map | FPGA | NIST 800-22 | 200 | H function | 7.7 |

**Table 2:** The FPGA chip statistics of the Zigzag map RNG

| Parameters (Altera Cyclone IV GX EP4CGX150DF31C8) | Total FPGA Unit | % Used for Zigzag Map PRNG |
|---|---|---|
| Total Logic Elements | 149.760 | 2.160 (1 % ) |
| Total combinational functions | 149.760 | 2.093 (<1 % ) |
| Total dedicated registers | 149.760 | 1.100 (1 % ) |
| Total memory bits | 6.635.520 | 93 (< 1 % ) |
| Embedded Multipliers 9-bit | 720 | 7 (1 %) |
| Total pins | 508 | 10 (2 % ) |
| Total PLLs | 8 | 1 (13 %) |
| Power Dissipation (mW) | | |
| Dynamic | - | 10.84 |
| Static | - | 105.17 |
| IO | - | 11.01 |
| Total | - | 127.02 |

The results given in Table 2 show that besides its good statistical properties, PRNG can be used easily in resource-restricted embedded cryptographic applications. PRNG architecture, based on general principles in terms of modelling technique, is a device independent generator model with low area-energy consumption, so it can be easily applied on resource restricted architectures. In addition, the generator's being based on digital design techniques and easy re-configurability feature are other important advantages in terms of hardware implementation.

The output bit rate performance of the proposed zigzag map based PRNG has been compared with other hardware based chaotic RNGs in the literature. Comparison results are as in Table 3. When the results in Table 3 are examined, it can be seen that PRNG offers a higher output bit rate compared to other studies, although the output bitrate decreases by 1/2 due to the post processing technique.

## 5 Conclusion

In this study, the hardware implementation of a new PRNG using the chaotic Zigzag map as entropy source on FPGA environment is presented. The bit-level random outputs of PRNG are obtained from the trajectory produced by the chaotic zigzag map for the initial value of $x_0$. The outputs representing the 32-bit chaotic orbit in the system are transformed into bit-level random numbers / signs with the help of a simple comparison circuit and subjected to post-processing technique. While the Zigzag map is in chaos state, PRNG's post-processed outputs successfully pass the NIST 800-22 tests. Statistical randomness results confirm that the chaotic system modelled can be used for different cryptographic purposes as well as random number generation methods. In addition, the low hardware resource requirement makes PRNG easily applicable in resource-constrained hardware architectures and applications. In another aspect, the study is important in terms of showing the usability of the zigzag map in different chaos-based engineering applications and being a source for these studies.

## 6 Conflict of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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# Design of a Low Power and High-Efficiency Charge Pump Circuit for RFID Transponder EEPROM

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**Abstract:** The charge pump (CP) circuit is an essential part of a radio frequency identification electrically-erasable-programmable-read-only memory (RFID-EEPROM). A CP circuit generates a boosted output voltage that is greater than the power supply voltage. However, the performance of the diode configured CP circuits is strongly affected by the extra power dissipation and the parasitic capacitance. The parasitic capacitors of the CP circuit are also responsible for increased power consumption. In this research, an improved CP circuit is designed for achieving higher output voltage gain by reducing the parasitic capacitances. Moreover, the proposed course consumes less power, which makes it more suitable for low power applications like RFID transponder. The proposed CP circuit is using the internal boosted voltage for backward control where active controls are applied to the charge transfer switch (CTS) to eradicate the reverse charge sharing trends. Simulated results showed that by using 1 pF pumping capacitor to drive the capacitive output load, the proposed circuit generates 9.56 V under 1.2 V power supply. In comparison with other research, works, this CP circuit consumes less power (only 15.26 µW), which is lower than previous research works. Moreover, the proposed CTS CP circuit can operate with the efficiency of 79.3%, which is found higher compared to other research works. Thus, the proposed design will be an essential module for low power applications like RFID transponder EEPROM.

**Keywords:** charge pump; charge transfer switch; non-volatile memory; transponder; RFID

# Zasnova vezja črpalke naboja z majhno močjo in visoko učinkovitostjo za RFID transponder EEPROM

**Izvleček:** Vezje črpalke naboja (CP) je bistveni del radijsko frekvenčne identifikacije električno izbrisljivega programabilnega pomnilnika samo za branje (RFID-EEPROM). CP vezje generira višjo izhodno napetost od napajalne. Kljub temu na delovanje CP vezij močno vpliva dodatna disipacija moči in parazitska kapacitivnost. Parazitski kondenzatorji vezja CP so prav tako odgovorni za povečano porabo energije. V tej raziskavi je predstavljeno izboljšano vezje CP, ki je zasnovano za doseganje višjega ojačenja izhodne napetosti z zmanjšanjem parazitskih kapacitivnosti. Poleg tega se predlagano vezje porabi manj moči, zaradi česar je bolj primerno za aplikacije z nizko porabo, kot je RFID transponder. Predlagano vezje CP uporablja notranjo ojačano napetost za povraten nadzor, kjer je uporabljena aktivna kontrola stikala za prenos naboja (CTS) za izkoreninjenje trendov delitve povratnega naboja.
Simulirani rezultati so pokazali, da predlagano vezje z uporabo črpalnega kondenzatorja 1 pF generira napetost 9,56 V pri vhodni napajalni napetosti 1,2 V. V primerjavi z drugimi raziskavami to CP vezje porabi le 15,26 µW moči. Poleg tega ima predlagano vezje CTS CP učinkovitost 79,3%. Predlagana zasnova bo tako bistveni modul za aplikacije z nizko porabo energije, kot je npr. RFID transponder EEPROM.

**Ključne besede:** črpalka naboja; stikalo za prenos naboja; trajni spomin; transponder; RFID

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## 1 Introduction

A typical RFID transponder is known as data carrying devices in RFID systems. RFID transponder can be embedded in objects like electronic devices, luggage, pets, or human being for identification. The RFID transponder is a chip or small circuit board coupled to an antenna [1]. A typical RFID chip contains mainly three blocks, such as analogue, logic, and memory blocks. To store information in the readerless RFID transponder, a small amount of NVM should be embedded [2] Transponder memory can contain read-only memory (ROM), Random Access Memory (RAM), non-volatile memory as EEPROM, flash memory, etc. and data buffers subjected to the device functionality [3]-[4].

Different types of memories exist in the market. Among them embedded NVM such as EEPROM is mostly used as tag memory in RFID, SoC, and FPGA systems. However, the prerequisites, additional masks, and fabrication steps made EEPROM and Flash memory highly expensive compared to a standard CMOS logic process. Many researchers wanted to develop EEPROM in a traditional CMOS logic process as it has the advantages of low cost and low power [5]-[8].

However, the maintenance and endurance features are inadequate due to the NMOS tunnelling junction or the single-ended memory cell architecture with a too-thin oxide [5]-[6]. It has a large area/bit and consumes much power as each bit cell contains its high voltage switch [7]-[8]. To generate the high voltages, an internal high-voltage generator circuit such as voltage doublers or CP circuit is required [9].

Currently, low-voltage and small size DC-DC converters are widely required for mixed-mode circuit schemes. To transform an input voltage from low to high with either a positive or reverse polarity, the CP circuit can be the vital element to encounter the demands [10]. In the CP circuit, capacitors are needed to store the energy of any devices instead of magnetic constituents. The capacitors required by the CP circuit can be small enough to be fabricated in IC. For low-power designs, CP circuits are needed to generate dc voltages higher than the power supply (VDD) or lower than the ground voltage (GND) of the memory chip. With the features of high-energy efficiency, small space, low power dissipation, and low current drivability, the CP circuit is chosen by the researcher as the compulsory module in EEPROM. Commonly, it is applied to the EEPROM in RFID transponder, DC-DC converters, and power supervision chips to write or to erase the floating-gate devices [11-13].

Dickson established the most widespread CP circuit in 1976, where the CP circuit used the diode-connected NMOS arrangement as a charge transfer device instead of switches [14] (Dickson, 1976). However, power efficiency and voltage gain in each stage are very low in the diode-connected CP circuit due to the body effect. Several types of research have been made to enhance the performance of the CP circuit [15-16]. Yan et al. have considered a CP with additional devices, which suffered from more power consumption for a lower current load [15]. Liu et al. proposed a CP with charge transfer switches (CTS) and parasitic capacitors to solve the problem of body effect. Besides, the CP circuit used the next pumping voltages to switch each CTSs [16]. However, the enlarged parasitic capacitance at every pumping stage decreases the pumping efficiency or the voltage gain. In 2009, Wang et al. also designed a CP circuit with the backward. They forwarded the CTS controlling method to recover the efficiency, to eradicate the body effect, and to escalate the voltage gain [17]. Nevertheless, the pumping efficiency or voltage gain is still lower with the PMOS switch in the output stage.

In this research, an improved CP circuit using CTS with reduced parasitic capacitance is described. The designed CP circuit is capable of reducing power consumption and increased voltage efficiency, which is compatible with the RFID transponder EEPROM. Silterra 0.13 µm CMOS process is utilized to design and verify the enhanced CP circuit. The comparative study proves that the proposed design decreased the parasitic capacitance, increased the pumping efficiency, and cut down the power consumption compared Liu et al. and Wang et al.'s CP circuit.

## 2 Materials and methods

In this research, CTS is the most widely used CP design method, which has been used by many researchers in their study. In this scheme, the dynamic charge transfer scheme in each step is the key to enhancing the boosted charge from the lower supply voltage. Most of the previous researchers included both the NMOS and PMOS transistors to implement the diode configuration in CMOS, where PMOS transistors created a large substrate current in each step of the charge transfer process, which eventually increased the power dissipation of the overall design. Therefore, in this research, a novel CTS-based CP circuit is proposed, where all the PMOS transistors are excluded, and NMOS transistors are utilized in all stages. This reduces the substrate current or in another term, the power dissipation of the overall circuit. The schematic diagram of the proposed CTS CP circuit is shown in Figure 1. In this research, Silterra 0.13 µm CMOS process is used to design the

schematic of the proposed CP circuit. From Figure 1, it is shown that one diode-configured MOSFET MD1 is utilized in this design to initiate the voltage from the supply voltage VDD to start the charge transfer process from one stage to another, whereas, another MOSFET MD2 is connected with the output stage of the circuit. On the other hand, transistors (MS1–MS9) are required to control the CTS and to transmit the boosted charges from the first stage to last using the backward charge transfer scheme. As all the CTS switches from MS1–MS9 does not entirely turn "OFF" during this transfer process, additional controlling transistors MN1 to MN9 and MP1 to MP9 are added in this design.

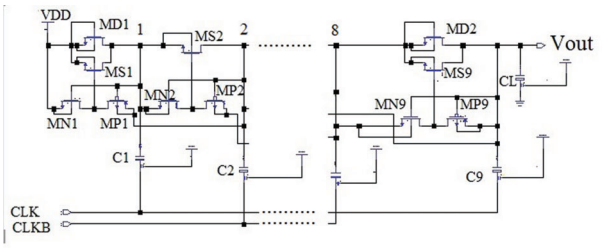


**Figure 1:** Schematic diagram of the proposed CTS based CP circuit.

In this research, when the clock signal CLK is in a high state, and the anti-phase clock signal CLKB is in a low condition, the gate of transistor MS2 is turned ON at the time of the charge pump process, which holds the amplitude of VDD as the pass transistor MN2 is switched OFF and MP2 is switched ON. Therefore, transistor MS2 has the value of VDD to node 2. On the other hand, when CLK is in a low state, and CLKB is in a high condition, the pass transistor MN2 is turned ON, and MP2 is turned OFF. Therefore, the gate voltage of MS2 becomes zero, which turns OFF the MS2 transistor entirely and the entire CP circuit feedbacks the charges from stage one to the next. In this design process, the total performance of the circuit closely depends on the sizing of the transistors. In this topology, zero $V_{th}$ MOSFETs help to overcome the threshold voltage drop at each stage, which helps to boost the pumping process of this scheme. Usually, the amplitude of the $V_{clk}$ is same as $V_{DD,}$ in this scheme. Thus, the voltage variation and the voltage fluctuation of each pumping node can be expressed as,

$$\Delta V \approx V_{CLK} = V_{DD} \tag{1}$$

$$\Delta V = V_{CLK} \frac{C_{pump}}{C_{pump} + C_{par}} - \frac{I_o}{f.(C_{pump} + C_{par})} \tag{2}$$

where $V_{CLK}$ is the voltage amplitude of the clock signals, $C_{pump}$ is the pumping capacitance, $C_{par}$ is the parasitic capacitance of each pumping node, $I_o$ is output current, and *f* is the clock frequency. If $I_o$ is small enough, and $C_{pump}$ is large enough, $I_o$ can be ignored from equation (2). Hence, the output voltage of the N-stage CP circuit can be expressed as

$$V_{out} = N.(V_{DD} - V_D) \tag{3}$$

where $V_D$ is the cut-in voltage of the pn-junction diode and N is the number of the stages taking part in pumping. The ripple voltage is defined as:

$$V_{ripple} = \frac{I_{out}}{fC_{out}} \tag{4}$$

where, $C_{out}$ is the load capacitance, which is ignored to calculate the ripple voltage of the proposed CP circuit. The number of stages determines the power efficiency because of $V_{out}$ and VDD, which are determined by the specific CMOS process [18].

Die layout of the proposed CP circuit with I/O padded structure is shown in Figure 2, where the CP circuit without I/O pad occupies only a small area of 224.2 µm × 73.2 µm. During the design process, all transistors and capacitors are placed in a manner that reduces the mismatch and parasitic capacitance. Figure 2 shows the chip layout of the proposed CP circuit with I/O pads.

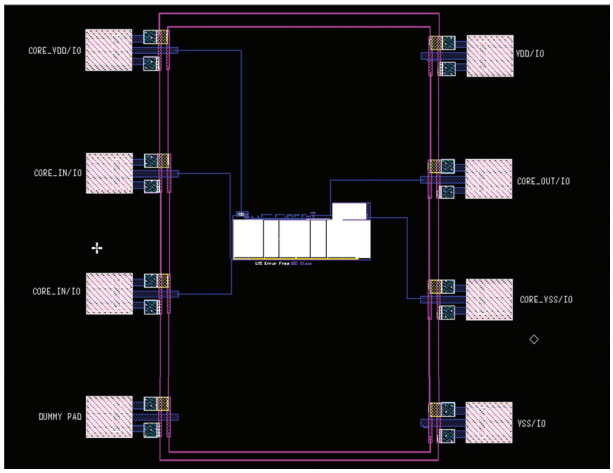


**Figure 2:** Die layout of the proposed CP circuit with I/O pads.

## 3 Results and discussions

The operating temperature was set to 27° C for the CTS CP circuit and the ELDOSPICE simulator (Mentor Graphics) was used within Silterra 0.13 µm CMOS process. VDD for simulating the outputs is set to 1.2 V. The simulated behaviour of the CTS CP circuit is illustrated in Figure 3. Figure 3 shows the simulated output voltage waveform of the proposed eight-stage CP circuit with

2pF pumping capacitors. Ideally, the output voltage of the designed eight-stage CP circuit with power supply voltage VDD= 1.2 V should be as high as 9.6 V (1.2 x 8 = 9.6 V). However, the output voltage of the proposed CP circuit is decreased due to some parasitic capacitances at every pumping node and the loading of the output current. Therefore, the simulated output voltage of the proposed CP circuit is achieved $V_{out}$= 9.56 V.

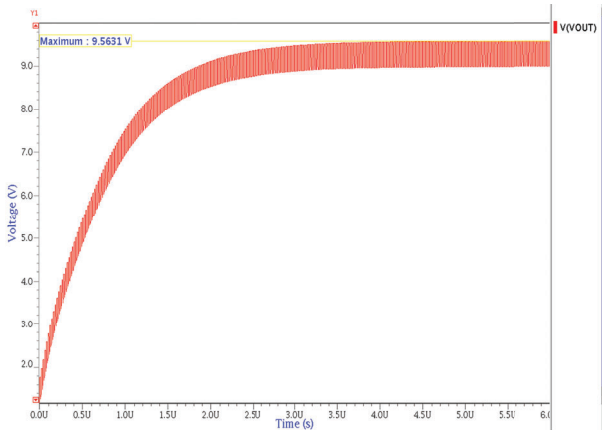


**Figure 3:** The simulated waveform of the proposed CTS CP circuit.

In this proposed design, both the clock signals (CLK and CLKB) amplitude is set to 1.2 V as same as the supply voltage. The circuit is simulated using 10.2 MHz clock frequency to observe the pumping performance of the proposed CP circuit. If the clock frequency is increased, the charge is transferred over a fixed time interval from one step to another in a faster way, which also increases the output voltage. At 50 MHz clock frequency, the proposed CP circuit exhibited the best performance. In this proposed design, increasing the clock frequency raises the output voltage gain, but incomplete charge transferring occurs if the circuit operates above 50 MHz clock frequency.

On the other hand, the proposed CP circuit is simulated for all 45 corners. In this research, 3 Vcc (1.1 V, 1.2 V, and 1.3 V), three temperatures (-40$^0$C, 27$^0$C and 125$^0$C), and five corners are examined, as shown in Figure 4. This corner analysis and process variation tests ensure the proposed CTS based CP circuit function correctly within manufacturing tolerances, which is compulsory in CMOS design. The corner test results revealed that the proposed CP circuit could function properly at different corners of VDD and temperature.

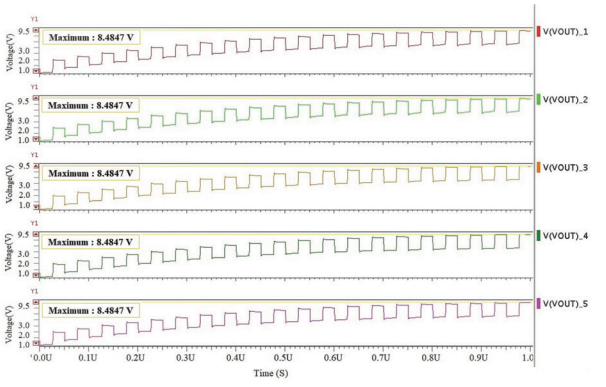


**Figure 4:** Post layout corner analysis of the proposed CP circuit.

The proposed design of the CP circuit achieved output voltage $V_{out}$ = 9.56 V, which is higher than recently published research works, as shown in Figure 5. The simulated results discovered that [16] and [19] CP circuits achieved poor $V_{out}$ due to threshold voltage loss and high parasitic capacitances in every node of the pumping stages. Conversely, to compare the simulated results with recently published research works, this proposed design is tested with different supply voltages, which is shown in Figure 5. From this comparison, it is evident that this novel CP circuit performed better than other research works for all the supply voltage values from 1.2 V to 2.4 V.

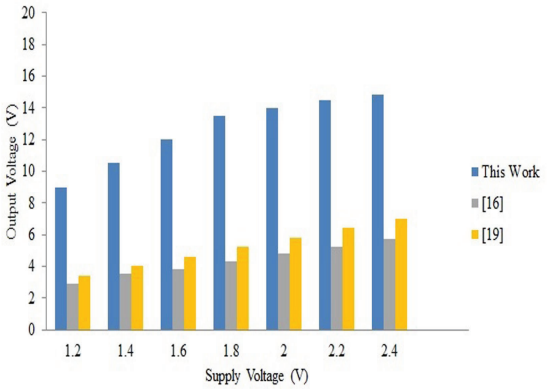


**Figure 5:** Comparison of output voltages against supply voltages among [16],[19] and this work under 1.2 ≤<VDD≤2.4.

On the other hand, the comparison results of the load current against different VDD among the proposed CP circuit, [16] and [19] are shown in Figure 6. From Figure 6, it is observed that the proposed CP circuit can operate successfully with a higher load current under different supply voltage ranges from 1.2 V to 2.4 V. The higher the load current a CP can drive the better its performance, so from Figure 6, it can be said that the proposed CP circuit's performance is better compared to [16] and [19] with higher load current.

Moreover, in this proposed design, a small number of pumping capacitors are utilized the parasitic capacitors ($C_{par}$) are removed as shown in [16], which helps to trim down the parasitic capacitance effect and leads to reduced load current against different supply volt-

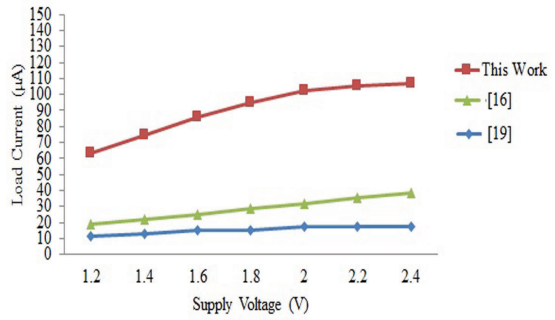


**Figure 6:** Comparison of load current against supply voltages among [16],[19] and this work under 1.2 ≤<VDD≤2.4.

age ranges 1.2≤<VDD≤2.4. The proposed CP circuit attained a higher output voltage $V_{out}$ at a low power supply voltage as this proposed topology can reduce the parasitic capacitance effect. Moreover, by using the backward control process with the dynamic CTS scheme, the triple well MOSFETs are turned on/off successfully. This proposed design CP circuit achieved lower power dissipation compared to recently published research works within a supply voltage ranges from 1.2 V to 2.4 V. At VDD = 1.2 V the power consumption of CP circuit from [19] was 51.57 μW. At the same voltage level, the CP circuit from [16] consumed 171.25 μW.

On the other hand, the proposed CP circuit dissipates only 15.26 μW, which is much lower than the recently published research works. The power efficiency at VDD= 1.2 V is calculated using equation (5) for [16], [19] and the proposed CP circuit with a different number of stages, which is shown in Figure 7. From Figure 7 it is found that for a different number of steps the proposed CP circuit can produce higher pumping efficiency up to 79.3% at 10.2 MHz using 2 pF pumping capacitances, which are much higher compared to [16] and [19].

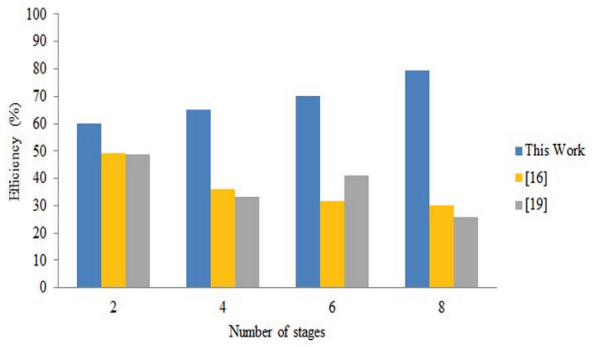


**Figure 7:** Graphical representation of the power efficiency of various CP circuits for different numbers of stages.

The size of each pumping capacitor of the CP circuit must be equal to get better comparison results. Consequently, every pumping capacitors of the proposed CP circuit, [16] and [19] circuits was set to 2 pF, 1 pF, and 0.1 pF, respectively. For HVG compatible CP circuit, power efficiency can be expressed as,

$$\eta_{power} = \frac{V_{out}.I_{out}}{(VDD - V_t).I_{in}} = \frac{V_{out}}{(N+1)(VDD - V_t)} \quad (5)$$

The number of stages only determines the power efficiency of $V_{out}$ and VDD is fixed by the application [18]. Compared to the initial Dickson CP circuit, when the diodes have zero Vt, the power efficiency is improved by VDD/ (VDD - $V_t$) using equation (5). Of course, the result is higher when VDD is low. The power efficiency at VDD= 1.2 V is measured for [16] and [19]. The proposed CP circuit with a different number of stages is, as shown in Figure 6. Table 1 summarizes the comparison studies among the proposed CP circuits along with the recently published research works.

Compared to all recently published research works, the proposed CP circuit has achieved the highest output voltage of 9.56 V under a supply voltage of 1.2 V, as shown in Table 1. In this design, the W/Ls of MD1 and MD2 were increased and the W/Ls of MS1-MS9 decreased, which helped to produce a higher output voltage, which is better than all the previous research outputs. However, [20] is made slightly higher output than this research work, which is achieved due to the higher supply voltage compared to this research work. Moreover, the proposed design achieved the highest pumping efficiency of 79.3%, which is better than [19, 21-22]. The result is achievable, as it has a smaller number of parasitic capacitances to turn out higher efficiency under low supply voltages. The pass transistors (MNs and MPs) were used in this design to prevent voltage loss and reverse the charge-sharing mechanism, which also improves the process of charge transfer and boosts the output voltage. In this research, the frequency was set to 10.2 MHz for the two anti-phase clock signals of the proposed CP circuit, which met the required specifications of the HVG.

Moreover, the designed CP circuit can perform up to 50 MHz, which makes the proposed design superior to [16, 20, 21-22]. In terms of accessibility. From the comparison table, it is also found that the proposed design has the lowest power dissipation of only 15.26 μW with eight stages of pumping capacitors, which is better than [16, 19, 21]. The proposed CP circuit used the triple well NMOS switch to control the CTSs dynamically instead of diode-configured switches in all stages. Hence, no substrate current is formed throughout the dynamic control process. Using PMOS transistors results in a substrate current at each step during

**Table 1:** Performance comparison of different cp circuits.

| References | [16] | [17] | [19] | [20] | [21] | [22] | [23] | This Work |
|---|---|---|---|---|---|---|---|---|
| Technology (µm) | 0.35 | 0.13 | 0.18 | 0.18 | 0.35 | 0.35 | 0.13 | 0.13 |
| Supply Voltage (V) | 3.3 | 1.5 | 1.8 | 2 | 3.3 | 3.3 | 1.2 | 1.2 |
| Clock Frequency (MHz) | 3 | 20 | 20 | 0.78 | 5 | 1.6~5.5 | 8 | 10.2 |
| Number of Stages | 4 | 5 | 4 | 8 | 6 | 4-8 | 3 | 8 |
| Output Voltage (V) | 3.18 | 6.32 | 5.95 | 9.8 | 14 | 4.8 ~ 8.5 | 3.08, -3 | 9.56 |
| Power Consumption (µW) | 304.76 | - | 205.56 | - | 150.48 | - | - | 15.26 |
| Layout area(µm$^2$) | - | - | 40x60 | 154x105 | - | - | 0.5mm$^2$ | 224.29 x 86 |
| Efficiency (%) | - | - | 25 | - | 31 | 75 | 60 | 79.3 |

the charge transfer process. As a result, the proposed CP circuit dissipated lower power with better reliability compared to recently published research works.

## 4 Conclusions

An enhanced CP circuit is illustrated in this research by using the four-stage CTS scheme to move the charges directly with improved pumping efficiency. Design and prefabrication simulation of the CP circuit was done with only 15.26 µW power dissipation, which was lower compared to recently published research works. 9.56 V of boosted internal supply voltage was obtained and 79.3 % pumping efficiency was achieved by decreasing the parasitic capacitance effects. Again, these were the highest value among compared research works. From these analyses, it is evident that the designed CP circuit can perform in low voltage devices with lower parasitic capacitances, which results in lower power consumption compared to previous designs.

## 5 Acknowledgements

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## 6 Conflict of interest

There is no conflict of interest among the authors.

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# A Concurrent Dual-Band Inverter-Based Low Noise Amplifier (LNA) for WLAN Applications

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**Abstract:** In this paper, a two-stage concurrent dual-band low noise amplifier (DB-LNA) operating at 2.4/5.2-GHz is presented for Wireless Local Area Network (WLAN) applications. The current-reused structure using resistive shunt-shunt feedback is employed to reduce power dissipation and achieve a wide frequency band from low frequency to-5.5-GHz in the inverter-based LNA. The second inverter-based stage is employed to increase the gain and obtain a flat gain over the frequency band. An LC network is also inserted at the proposed circuit output to shape the dual-band frequency response. The proposed concurrent DB-LNA is designed for RF-TSMC 0.18-µm CMOS technology, which consumes 10.8 mW from a power supply of 1.5 V. The simulation results show that the proposed DB-LNA achieves a direct power gain ($S_{21}$) of 13.7/14.1 dB, a noise figure (NF) of 4.2/4.6 dB, and an input return loss ($S_{11}$) of −12.9/−14.6 dBm at the 2.4/5.2-GHz bands.

**Keywords:** low noise amplifier (LNA); concurrent; dual-band; inverter-based

# Sočasni dvopasovni ojačevalnik z nizkim šumom (LNA) za aplikacije WLAN

**Izvleček:** V prispevku je predstavljen dvostopenjski sočasni dvopasovni ojačevalnik z nizkim šumom (DB-LNA), ki deluje na frekvenci 2,4 / 5,2 GHz za aplikacije brezžičnega lokalnega omrežja (WLAN). Trenutno uporabljena struktura, ki uporablja uporovno povratno povezavo, se uporablja za zmanjšanje porabe moči in doseganje širokega frekvenčnega pasu od nizkih frekvenc do 5,5 GHz v pretvorniškem LNA. Druga stopnja, ki temelji na pretvorniku, se uporablja za povečanje ojačenja in doseganje enotnega ojačanja v celotnem frekvenčnem pasu. LC omrežje je vstavljeno tudi v izhodno vezje za oblikovanje dvopasovnega frekvenčnega odziva. Predlagani sočasni DB-LNA je zasnovan za RF-TSMC 0,18 µm CMOS tehnologiji, s porabo 10,8 mW pri napajalni napetosti 1,5 V. Rezultati simulacije kažejo, da predlagani DB-LNA doseže neposredno ojačenje ($S_{21}$) 13,7 /14,1 dB, vrednost šuma (NF) 4,2 / 4,6 dB in vhodno povratno izgubo ($S_{11}$) -12,9 / -14,6 dBm v pasovih 2,4 / 5,2 GHz.

**Ključne besede:** ojačevalnik z nizkim šumom (LNA); sočasnost; dvopasovnost; pretvornik

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## 1 Introduction

Over the past few years, various and new wireless communication standards have been developed to extend transceiver functionalities. The development of the IEEE 802.11a/b (2.4/5.2-GHz) standard has been widely used in Wireless Local Area Network (WLAN) applications due to support for high data rate communication (up to 54 Mb/s) and the wide range of its applications [1-3]. Therefore, the new trend in RF front-end receiver features a low noise amplifier (LNA) capable of receiving multiband frequencies with a proper performance at each frequency band, as shown in Figure 1 [4].

The low noise amplifier (LNA) with dual bandwidth plays a critical role in the overall performance of the dual-band receiver. The design of the dual-band LNA (DB-LNA) includes some challenges such as high gain, low noise performance, low power dissipation, and proper input matching for both bands. Several approaches have been presented to implement the DB-LNAs with

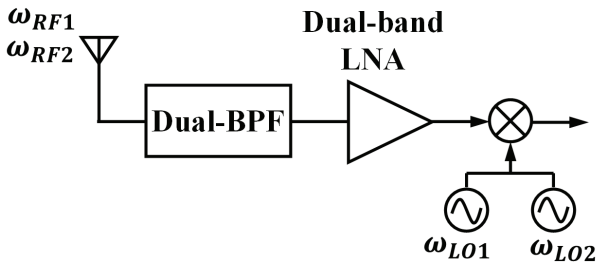


**Figure 1:** A concurrent dual-band receiver.

high performance operating at two different frequencies. The two single-band parallel LNAs configuration is one of the initial designs presented for DB-LNAs [5-8]. The measurement results show good performance at each frequency band at the expense of a larger chip area and higher power dissipation. The conventional methods use the switched inductors or switched capacitors in the input/output networks [9-14]. The structures consume low power, but generally degrade the gain and noise figure (NF) because of the insertion loss of their switches. Furthermore, LNA in such an approach can only operate with one band at a time. Another approach is to use a wideband LNA. Although this is a simple method for receiving multiple frequency bands simultaneously, the receiver sensitivity can be degraded due to the presence of unwanted signals in the wide frequency band. The most effective technique to achieve DB-LNA is to insert the notch filters in a wideband LNA [15-20]. Compared to the switchable LNAs, in this approach, the LNA supports simultaneous dual-band operations and consumes lower power. Hong et al. [17] used the cascode topology with gain boosting technique to achieve high gain and proper input matching. In addition, it employs the passive elements as bandpass/bandstop filters in the output network circuit to shape the frequency response, and to obtain a concurrent DB-LNA operating at 2.4/5.2GHz. Although this method results in a good performance in terms of linearity and power dissipation, it suffers from the unbalanced amplitude of the gain at the operating frequencies and weak roll-off in gain at the high band. Yu and Neihart [21] proposed a transformer-based multimode LNA using a reconfigurable multi-tap transformer as the gate inductor. The proposed LNA can dynamically achieve a single-band, or concurrent dual-band frequency response. However, it cannot provide high attenuation in the stopband and proper roll-off in gain at both bands in concurrent dual-band mode. In this paper, a two-stage concurrent DB-LNA in 0.18-µm CMOS technology is designed that operates at 2.4/5.2-GHz. The desired frequency bands are realized by using the LC network at the LNA output. The stagger tuning technique is also used to enhance the gain and provide a flat gain over the frequency band. Therefore, a concurrent DB-LNA with high balanced gain, proper roll-off in gain, and good input matching is obtained. The paper is organized as follows: Section 2 presents the design parameters of the proposed circuit, including the voltage gain, input impedance matching, noise figure, and band selection. In Section 3, the simulation results are presented and discussed. Finally, the conclusion is given in Section 4.

## 2 Design of proposed circuit

The schematic of the proposed DB-LNA is shown in Figure 2. It consists of two inverter-based stages using resistive shunt-shunt feedback along with an LC network connected at the circuit output.

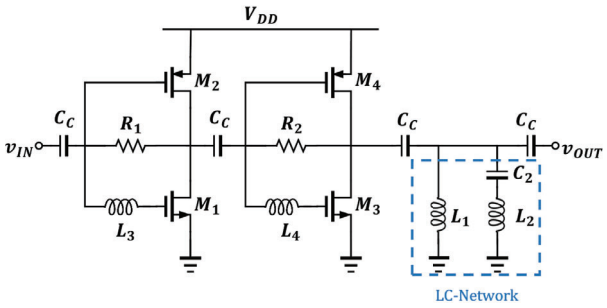


**Figure 2:** Schematic of the proposed DB-LNA.

In each stage, the current-reused technique is utilized to achieve low power dissipation and improve gain performance. Since the DC currents of transistors $M_2$ and $M_4$ are reused by $M_1$ and $M_3$, respectively, there is no requirement for additional driving currents for $M_1$ and $M_3$. The resistive feedbacks are utilized to achieve simultaneous proper input matching and flat gain. They also provide a self-biased structure for the proposed DB-LNA. The series peaking inductors of $L_3$ and $L_4$ are inserted in the gate of $M_1$ and $M_3$ to extend the bandwidth and provide proper input matching. The LC network of $L_1$, $L_2$, and $C_2$ is implemented at the LNA output to realize the dual-band frequency response within the LNA frequency response. The proposed circuit can provide high gain and good input matching at the two passbands with high attenuation in the stopband. The capacitance of CC is employed to provide the DC bias isolation of the circuit.

### 2.1 Bandwidth and gain analysis

A wideband amplifier operating over low frequency to 5.2-GHz is first designed to obtain the main structure of the proposed DB-LNA. Then, the frequency response of the DB-LNA is shaped by inserting an LC network. So far, several topologies are reported to achieve the wideband LNA, such as common-gate [22, 23] and

shunt resistive feedback [3, 24]. The common-gate (CG) configuration provides a wideband input impedance matching, high linearity, and good reverse isolation compared to the common-source (CS) configuration. Nevertheless, the CG configuration suffers from high NF, that is typically more than 3dB. Additionally, the feedback structure consumes more power. Using a modified inverter-based structure with shunt resistive feedback is an appropriate idea to improve the gain performance without additional power dissipation. Figure 3 shows a single modified inverter-based stage, which exhibits a relatively high flat gain over low frequency to 5.2-GHz.

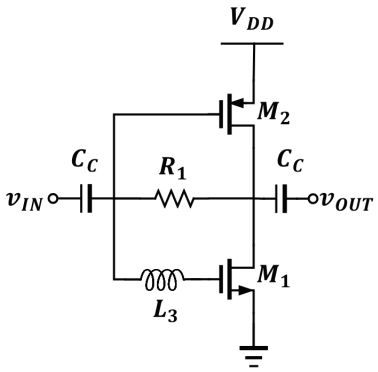


**Figure 3:** Schematic of the modified inverter-based LNA.

Higher gain is achieved by a second inverter-based LNA, which is connected in series with the first stage. However, the impedance mismatch between stages can result in ripples in the passbands, but using the stagger tuning technique results in flat gain over low frequency to 5.2-GHz. Figure 4 shows the proposed two-stage wideband LNA.

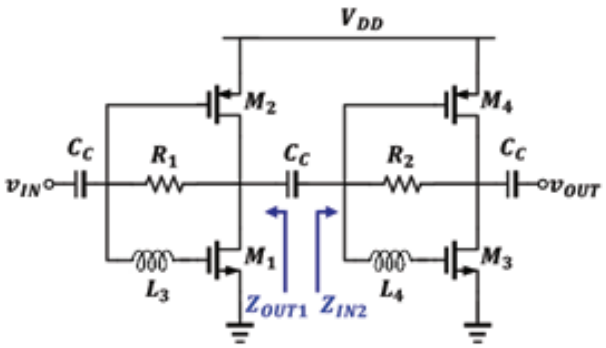


**Figure 4:** Schematic of the proposed wideband LNA.

The small-signal equivalent circuit of the proposed wideband LNA is shown in Figure 5. As can be seen, the feedback resistors of $R_1$ and $R_2$ are placed in parallel with the gate to drain capacitances ($C_{gd}$) to provide the wideband input matching. At the frequencies of interest, the impedances of the gate to drain capacitances are almost always much higher than the feedback resistor impedances that they are in parallel with. Therefore, $C_{gd}$ is neglected in the small-signal equivalent circuit of the proposed wideband LNA. In Figure 5, $Z_{L1}= r_{o1}||r_{o2}$ and $Z_{L2}= r_{o3}||r_{o4}$, where $r_{oi}$ is the drain output resistance of $M_i$. It is assumed that $R_2>>Z_{L2}$ for alleviating the loading effect of the second stage. By neglecting the gate-to-drain capacitance ($C_{gd}$), the input impedance of the second stage ($Z_{IN2}$) in case of $\omega<<\omega_T$ is obtained as follows:

$$Z_{IN2}(s)=\frac{L_4C_{gs3}s^2+1}{\left(C_{gs3}+C_{gs4}\right)s} \tag{1}$$

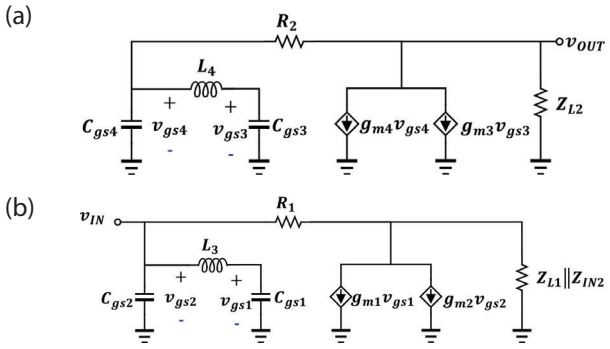


**Figure 5:** The small-signal equivalent circuit of the LNA (a) second stage and (b) first stage of the wideband LNA.

The overall voltage gain of the proposed wideband LNA is given by:

$$A_{v,T}=A_{v1}\times A_{v2} \tag{2}$$

where, $A_{v1}$ and $A_{v2}$ are the voltage gain of the first and the second stages, respectively. Based on the small-signal analysis, $A_{v1}$ can be expressed as below:

$$A_{v1}(s)=-\frac{L_3C_{gs1}g_{m2}s^2+g_{mT1}}{L_3C_{gs1}s^2+1}\left(R_1Z_{L1}Z_{IN2}\right) \tag{3}$$

where gm represents the transconductance of the MOS transistor, and $g_{mT1}=g_{m1}+g_{m2}$ is the overall transconductance of the first stage. Similarly, *A*v2 is obtained as follows:

$$A_{V2}(s)=-\frac{L_4C_{gs3}g_{m4}s^2+g_{mT2}}{L_4C_{gs3}s^2+1}\left(R_2Z_{L2}\right) \tag{4}$$

where $g_{mT2}=g_{m3}+g_{m4}$ is the overall transconductance of the second stage. By assuming a small value for $R_1$ and high value for $R_2$ and regarding (2), $A_{v,T}$ is given as follows:

$$A_{v,T}(s) \cong g_{mT1}g_{mT2}R_1Z_{L2}\frac{\left(L_3C_{gs1}\frac{g_{m2}}{g_{mT1}}s^2+1\right)}{\left(L_3C_{gs1}s^2+1\right)}\times \frac{\left(L_4C_{gs3}\frac{g_{m4}}{g_{mT2}}s^2+1\right)}{\left(L_4C_{gs3}s^2+R_1\left(C_{gs3}+C_{gs4}\right)s+1\right)} \quad (5)$$

By assuming $R_1/L_4$>5.2 GHz, $A_{v,T}$ can be simplified as:

$$A_{V,T}(s) \cong g_{mT1}g_{mT2}R_1Z_{L2}\frac{\left(1+\frac{s^2}{\omega_{z1}^2}\right)\left(1+\frac{s^2}{\omega_{z2}^2}\right)}{\left(1+\frac{s^2}{\omega_{p1}^2}\right)\left(1+\frac{s^2}{\omega_{p2}^2}\right)} \quad (6)$$

From (5) it can be seen that $A_{v,T}$ has four resonant frequencies $\omega_{p1,2}$ and $\omega_{z1,2}$, that expressed by:

$$\omega_{p1} = \frac{1}{\sqrt{L_3C_{gs1}}} \quad (7)$$

$$\omega_{p2} = \frac{1}{\sqrt{L_4C_{gs3}}} \quad (8)$$

$$\omega_{z1} = \frac{1}{\sqrt{L_3C_{gs1}\frac{g_{m2}}{g_{mT1}}}} \quad (9)$$

$$\omega_{z2} = \frac{1}{\sqrt{L_4C_{gs3}\frac{g_{m4}}{g_{mT2}}}} \quad (10)$$

From equation (6), it can be seen that the overall voltage gain is proportional to $g_{mT1}$ and $R_1$ ($Z_{L2}$ can be affected by load resistance). Since the input matching, power dissipation, and bandwidth limit the values of $g_{mT1}$ and $R_1$, the gain of the proposed wideband LNA can be adjusted by $g_{mT2}$. Moreover, the high band of the DB-LNA can be shaped by tuning $\omega_{p1}$ around 5.2-GHz. Figure 6 shows the overall frequency response of the proposed wideband LNA along with the frequency responses of the first and second stage. As can be seen, the proper roll-off in the upper-frequency response is achieved by setting $\omega_{z1}$ close to $\omega_{p1}$.

## 2.2 Input impedance

Impedance matching over a wide band is one of the most challenging tasks in wideband LNA design. The input matching condition of the inverter-based LNA can be improved by applying the shunt-shunt resistive feedback and inserting an inductor in series with the gate of the NMOS transistor. According to equation (1) and assuming $R_1/L_4$>5.2-GHz, the input impedance of the proposed wideband LNA in case of $\omega << \omega_T$ is expressed by:

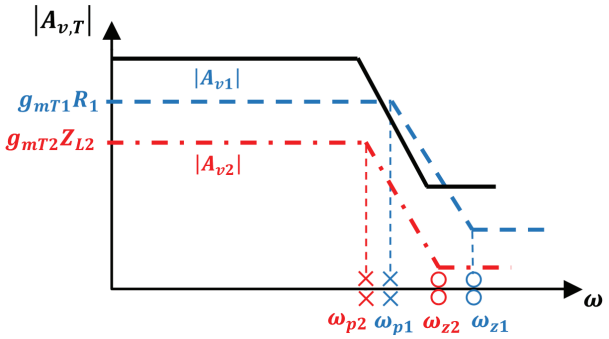


**Figure 6:** The frequency response ($|A_{v,T}|$) of the proposed wideband LNA.

$$Z_{IN}(s) = \frac{\left(1+R_1\left(C_{gs3}+C_{gs4}\right)s\right)\left(1+L_3C_{gs1}s^2\right)}{g_{mT1}\left(1+L_4C_{gs3}s^2\right)} \quad (11)$$

As mentioned earlier, by assuming $\omega_{p1}$ around 5.2-GHz, $Z_{IN}(s)$ can be simplified as follows:

$$Z_{IN}(\omega) \approx \frac{1+j\omega R_1\left(C_{gs3}+C_{gs4}\right)}{g_{mT1}\left(1-L_4C_{gs3}\omega^2\right)} \quad (12)$$

As can be seen, the input impedance is proportional to $g_{mT1}$, $R_1$, and $L_4$, thereby the trade-off between the gain and input matching can be reduced by only employing $g_{mT1}$ for satisfying the input matching condition.

## 2.3 Noise figure

The noise performance of the wideband LNA is evaluated by assuming the thermal noise of the transistors and the resistors as the dominant noise sources, and the flicker noise is neglected. The loss of inductors is

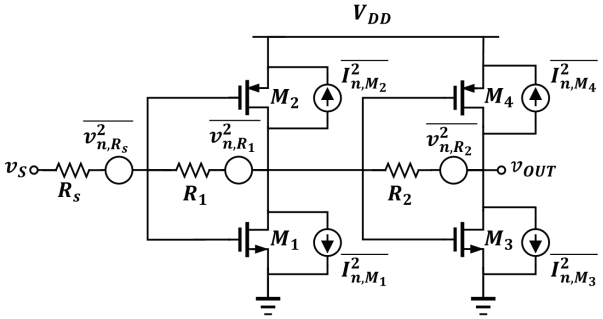


**Figure 7**: The simplified circuit of the wideband LNA for noise analysis.

neglected, and it is also assumed $L_3$ and $L_4$ resonate with the total capacitance at the input node of the first and the second stage, respectively. According to the mentioned conditions, the simplified circuit for noise calculation is derived, as shown in Figure 7.

The noise figure (NF) of the wideband LNA is given by:

$$NF = \frac{1}{A_{vs}^2}\frac{\overline{v_{n,out}^2}}{4KTR_s} \tag{13}$$

where $A_{vs}$ is the voltage gain from $v_S$ to $v_{OUT}$, and regarding $R_{IN} \approx R_1/2$, it can be expressed by:

$$A_{V1s}(s) = \frac{R_1}{R_1 + 2R_s}\left(g_{mT1}R_{o1}g_{mT2}R_{o2}\right) \tag{14}$$

where $R_{o1}$ and $R_{o2}$ represent the output resistance seen at the output nodes of the first and the second stage, respectively and they are given as:

$$R_{o1} \cong Z_{L1}\frac{R_s + R_1}{g_{mT1}R_s} \tag{15}$$

$$R_{o2} \cong Z_{L2}\frac{g_{mT1}R_2R_s + R_1}{g_{mT1}R_s + g_{mT2}\left(R_1 + R_2\right)} \tag{16}$$

According to Figure 7, the total output noise is expressed as:

$$\overline{v_{n,out}^2} = 4KTR_2 + 4KT\frac{\gamma}{\alpha}g_{mT2}R_{o2}^2 + \\ + \left(4KTR_1 + 4KT\frac{\gamma}{\alpha}g_{mT1}R_{o1}^2\right)\left(g_{mT2}R_{o2}\right)^2 + \\ + 4KTR_sA_{vs}^2 \tag{17}$$

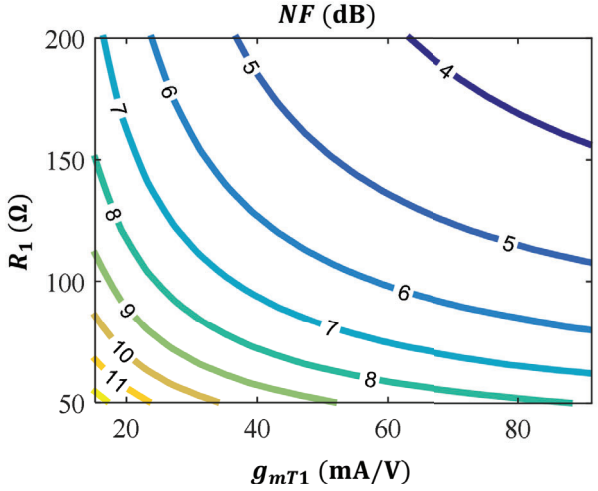


**Figure 8:** The contours of NF for $I_{D3}$=2 mA, $R_2$=5 kΩ, and $V_{eff1}$=$V_{eff3}$=0.2 V.

where α represents the ratio of $g_m$ to the zero-bias drain conductance gd0, and γ is the MOS transistor thermal noise coefficient. Figure 8 shows the contours of NF($g_{mT1}$, $R_1$) in the case of $I_{D3}$=2 mA, $R_2$=5 kΩ and $V_{eff1}$=$V_{eff3}$=0.2 V. As shown in Figure 8, there is a trade-off between $R_1$ and $g_{mT1}$ at a specific NF, and the proper NF can be achieved by choosing higher values for $R_1$ and $g_{mT1}$. Additionally, $R_1$ and $g_{mT1}$ are limited by input matching, and thereby, a lower NF can be achieved regarding proper input matching and power dissipation.

### *2.4 LC network*

As mentioned earlier, the circuit design starts with the design of a wideband LNA that exhibits a high flat gain over the low frequency to $f_2$=5.2-GHz. It should be noted $f_2$ is defined by $f_{p1}$. It is assumed that the receiver receives two frequency bands concurrently without using switches. Therefore, concurrent DB-LNA is a development based on a multiband theory to achieve dual-band characteristics. For this purpose, an LC network is inserted in the LNA output to achieve the requirements with minimum effect on the gain, NF, and input matching. The proposed LC network determines the low band of the concurrent DB-LNA and enhances the spurious frequency rejection at the low frequency. Figure 9 shows the proposed LC network. As can be seen the low band of $f_1$=2.4-GHz and the notch frequency of $f_3$=3.5-GHz are realized by $L_1$, $L_2$, and $C_2$ as follows:

$$f_1 = \frac{1}{2\pi\sqrt{\left(L_1 + L_2\right)C_2}} \tag{18}$$

$$f_3 = \frac{1}{2\pi\sqrt{L_2C_2}} \tag{19}$$

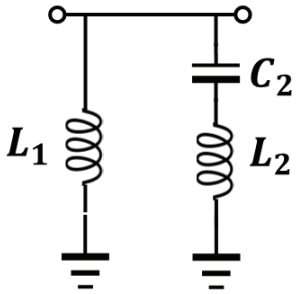


**Figure 9:** The proposed LC network used at the DB-LNA output.

Additionally, the frequency calibration method can be realized by using a varactor to tune the frequency shift due to the process variation. Figure 10 shows the frequency response of the proposed DB-LNA determined by the LC network.

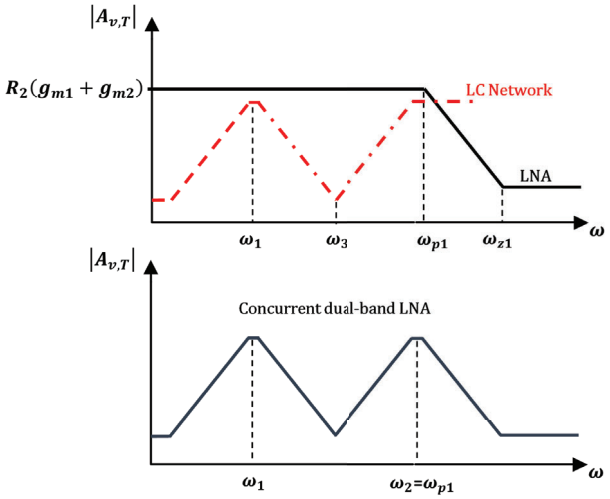


**Figure 10:** The frequency response ($|Av,_T|$) of the concurrent DB-LNA.

As shown, the proposed concurrent DB-LNA exhibits the operating frequencies of $f_1$=2.4-GHz and $f_2$=5.2-GHz.

## 3 Simulation results

The proposed concurrent DB-LNA is designed and simulated using Cadence Spectre-RF with 0.18 µm CMOS technology. The post-layout simulation results are reported in the paper, which take into account layout parasitic capacitances. The power supply of 1.5 V is used, and the minimum channel length is considered for all transistors. The first stage is designed to achieve moderate gain, low NF, and proper input matching over the lower frequencies to 5.2-GHz. Transistors $M_1$ and $M_2$ have the same width of 165 µm, while $M_1$ is biased at gate-source voltage ($v_{gs1}$) of 0.64 V, thereby $g_{m1}$= 60 mA/V and $g_{m2}$=25 mA/V. A higher $g_{mT1}$ value reduces the NF, but increases the power dissipation and degrades the input matching. According to (7) and (9), the $\omega_{z1}$ is located at about 1.85$\omega_{p1}$, thereby providing a proper roll-off at the upper-frequency band. The second stage enhances the gain and obtains a flat gain over a wide frequency band. For this purpose, the transistors $M_3$ and $M_4$ are designed to have $g_{m3}$=90 mA/V and $g_{m4}$=10 mA/V, while $M_3$ is biased at $v_{gs3}$=0.54 V with the total width of 310 µm, and $M_4$ has the width of 50 µm. The transistor dimensions chosen above and, according to (11) and (13), lead to $L_3$=4.2 nH, $L_4$= 2 nH, $R_1$=135 Ω, and $R_2$=1.5 kΩ. Figure 11 shows the simulated power gains of the two separate stages and the proposed wideband LNA operating over the low frequencies to 5.2-GHz.

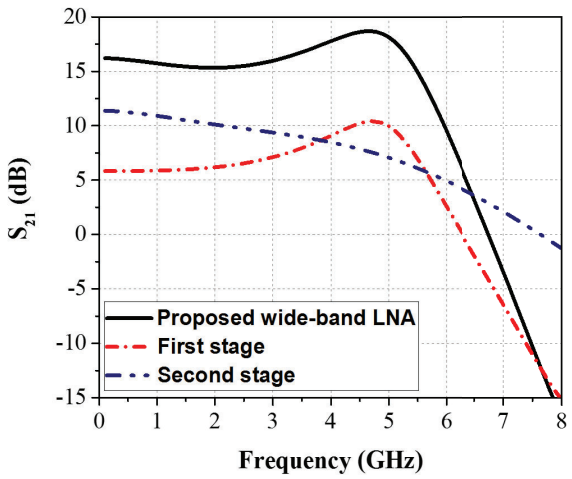


**Figure 11:** The simulated $S_{21}$ of the proposed LNA.

As shown in Figure 6, if the resonant frequencies of $A_{v1}$ and $A_{v2}$ are properly optimized, such as placing $\omega_{p2}$ at approximately 4-GHz and $\omega_{p1}$ at 5-GHz while keeping reasonable input-matching, a wideband flat power gain is expected. The dual-band gain response is achieved when the LC network is inserted at the output of the wideband LNA. Resonating at 3.8-GHz, $L_2$ and $C_2$ result in a very low output impedance. $C_2$ is chosen to be about 1.4 pF, while $L_2$ is adjusted about 1.5 nH. From (21), it can be seen that the low band operation of $f_1$=2.4-GHz is achieved with $L_1$=1.6 nH. Table 1 lists the optimized component values of the concurrent DB-LNA and the bias current of transistors.

**Table 1:** Parameters and their values.

| Component | Symbol | Value | Current (mA) |
|---|---|---|---|
| Transistor (Finger×W(µm)× L(µm)) | $M_1$ | (34×4.8×0.18) | 5 |
| | $M_2$ | (50×3.2×0.18) | 5 |
| | $M_3$ | (46×6.8×0.18) | 2.2 |
| | $M_4$ | (25×1.8×0.18) | 2.2 |
| Inductance (nH) | $L_1$ | 1.6 | |
| | $L_2$ | 1.5 | |
| | $L_3$ | 4.2 | |
| | $L_4$ | 2 | |
| Capacitance (pF) | $C_2$ | 1.4 | |
| | $C_C$ | 5 | |
| Resistance(Ω) | $R_1$ | 135 | |
| | $R_2$ | 1500 | |
| Bias (V) | $V_{DD}$ | 1.5 | |

Figure 12 shows the layout of the proposed DB-LNA, occupying 0.55 mm×0.48 mm chip area, excluding the pads.

The post-layout simulated power gain ($S_{21}$) and input return loss ($S_{11}$) of the concurrent DB-LNA are shown in Figure 13 and Figure 14, respectively. As shown in Figure 13, the balanced amplitude of the gain at the oper-

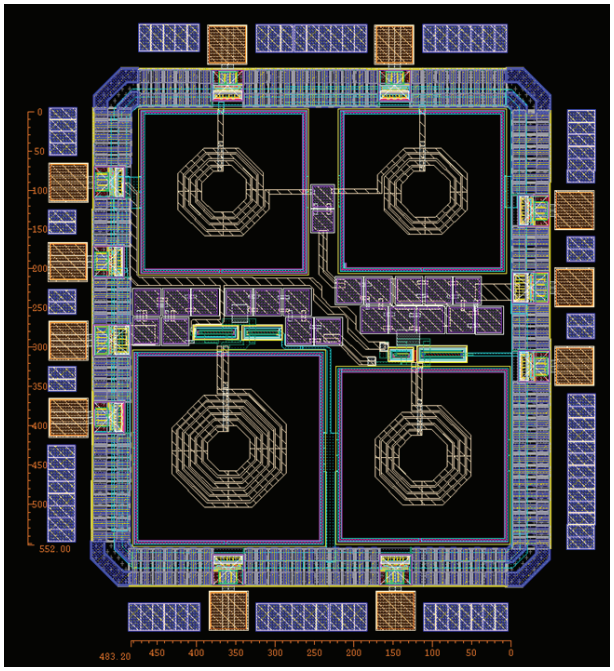

**Figure 12:** The layout of the proposed concurrent DB-LNA.

ating frequencies of 2.4-GHz and 5.2-GHz is achieved by choosing $L_1$=1.6 nH and $L_2$=1.5 nH. Figure 14 shows the value of $g_{mT1}$ that determines the input matching range. As shown in Figure 14, the simultaneous dual-band input matching smaller than -10 dB is achieved by choosing the $g_{mT1}$ smaller than 85 mA/V. However, the smaller values of $g_{mT1}$ can potentially achieve a higher noise figure up to 2 dB and yield a substantially lower gain.

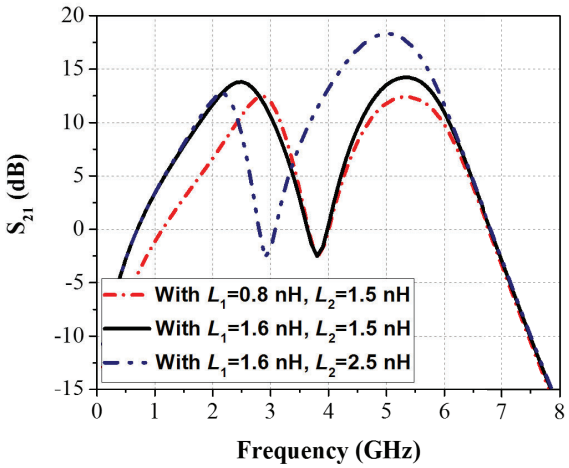


**Figure 13:** The simulated $S_{21}$ of the concurrent DB-LNA.

Noise analysis for the concurrent DB-LNA is carried out for $R_1$=135 Ω, as shown in Figure 15, in which the NF is 4.2 and 4.6 dB at the operating frequencies of 2.4-GHz and 5.2-GHz, respectively. The effect of $R_1$ on the noise performance of the proposed DB-LNA is also evaluated

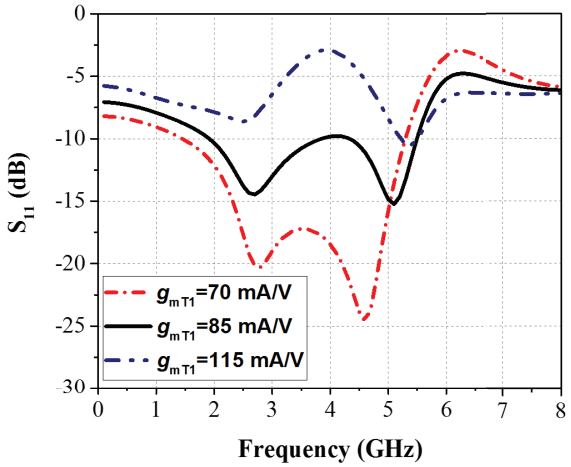


**Figure 14:** The simulated $S_{11}$ of the concurrent DB-LNA

in Figure 15 by varying the value of $R_1$. As shown in Figure 15, higher $R_1$ results in lower NF for both frequency bands. However, higher values of $R_1$ cause substantial peaking at the low band of the proposed DB-LNA.

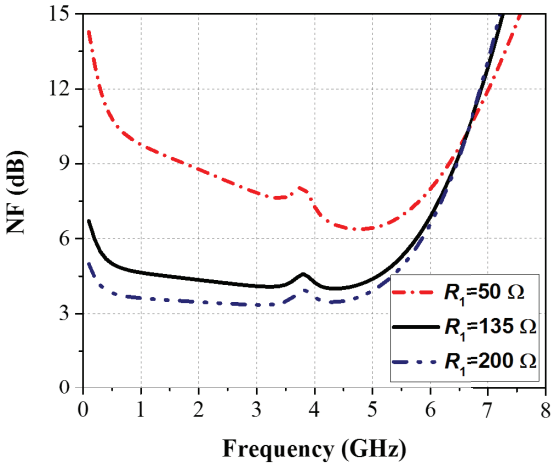


**Figure 15:** The simulated NF of the concurrent DB-LNA.

Figure 16 shows the third-order intermodulation intercept point (IIP3) simulations of the concurrent DB-LNA. The IIP3 is carried out by applying a two-tone test with 4-MHz frequency spacing. As shown in Figure 16, the post-simulated IIP3s are -6 dBm and -11 dBm at 2.4-GHz and 5.2-GHz, respectively.

Figure 17 shows the stability factors based on the S-parameters to consider the stability of the proposed DB-LNA. The necessary and sufficient conditions for unconditional stability are expressed as follows:

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2|S_{12}||S_{21}|} > 1 \quad (20)$$

$$\Delta = |S_{11}S_{22}-S_{12}S_{21}| < 1 \quad (21)$$

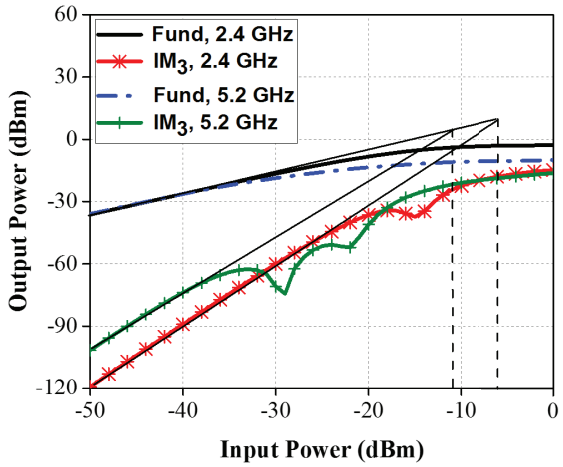


**Figure 16:** The simulated IIP3s with 4-MHz frequency spacing.

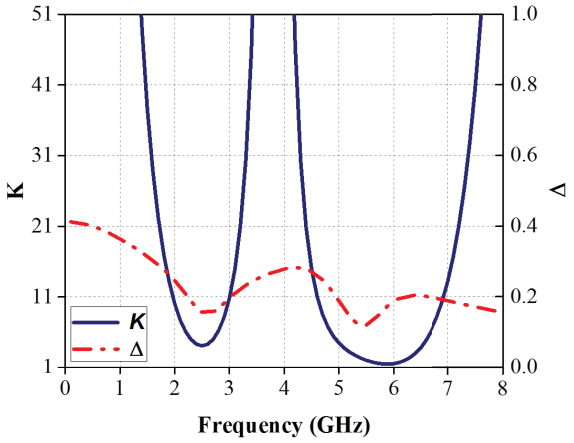


**Figure 17:** The simulated stability factors

As shown in Figure 17, the concurrent DB-LNA satisfies the conditions for unconditional stability at both frequency bands.

Monte Carlo analysis is carried out on the proposed DB-LNA to evaluate the effects of components mismatches on performance parameters such as $S_{21}$, NF, and $S_{11}$. In Monte Carlo simulation with 1000 iterations, a 2% mismatch with Gaussian distribution for all circuit components is considered. As shown in Figures 18 and 19, the mean $S_{21}$ of 13.97/14.11 dB (nominally 13.73/14.11 dB) with a standard deviation of 0.21/0.45 are obtained at the operating frequencies of 2.4/5.2-GHz. The results show a mean NF of 4.18/4.72 dB (nominally 4.25/4.67 dB) with a standard deviation of 0.06/0.13 at the operating frequencies of 2.4/5.2-GHz. In addition, mean $S_{11}$ of -12/-13.35 dB (nominally -12.95/-14.64 dB) with a standard deviation of 0.28/0.88 is obtained at the operating frequencies of 2.4/5.2-GHz.

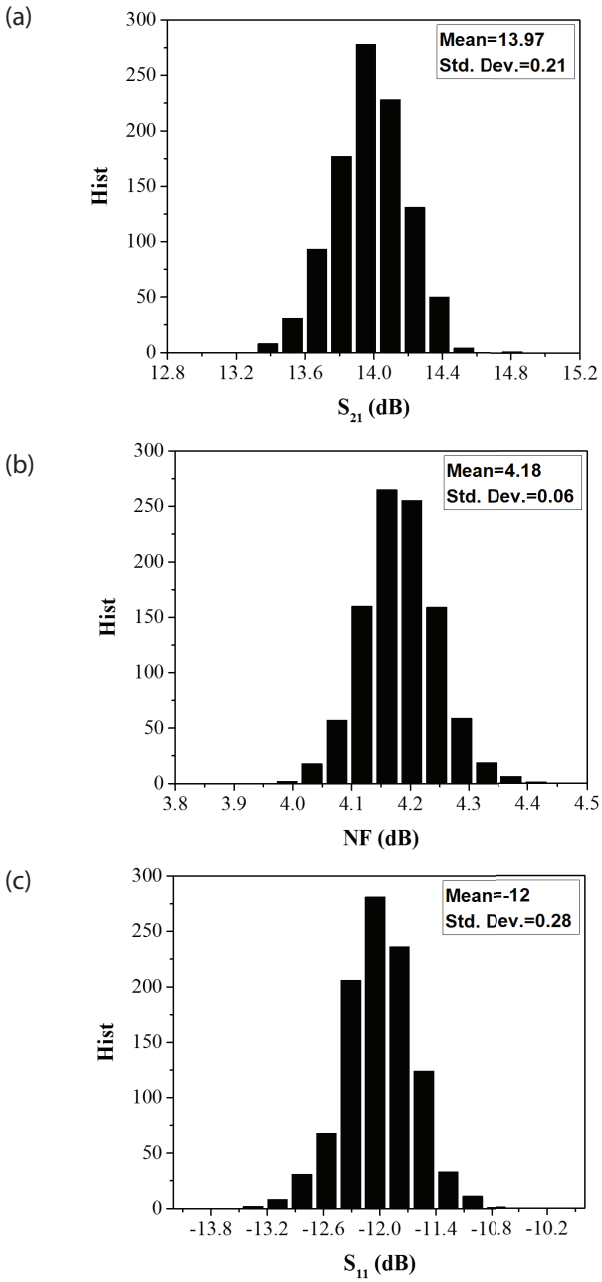


**Figure 18:** Monte Carlo simulation results at 2.4-GHz for (a) $S_{21}$ (b) NF and (c) $S_{11}$.

As seen in Figures 18 and 19, the Monte Carlo simulation results confirm the low sensitivity of the proposed DB-LNA to process variations at both frequency bands. The process corner cases and temperature variation are simulated at the operating frequencies, and the results are listed in Table 2. The proposed DB-LNA is also simulated over the power supply variation, and the results are listed in Table 3.

Table 4 has compares the performance of the proposed DB-LNA with similar reported works. A figure of merit (FoM) in both bands, which allows comparison between the concurrent DB-LNAs, is defined as follows:

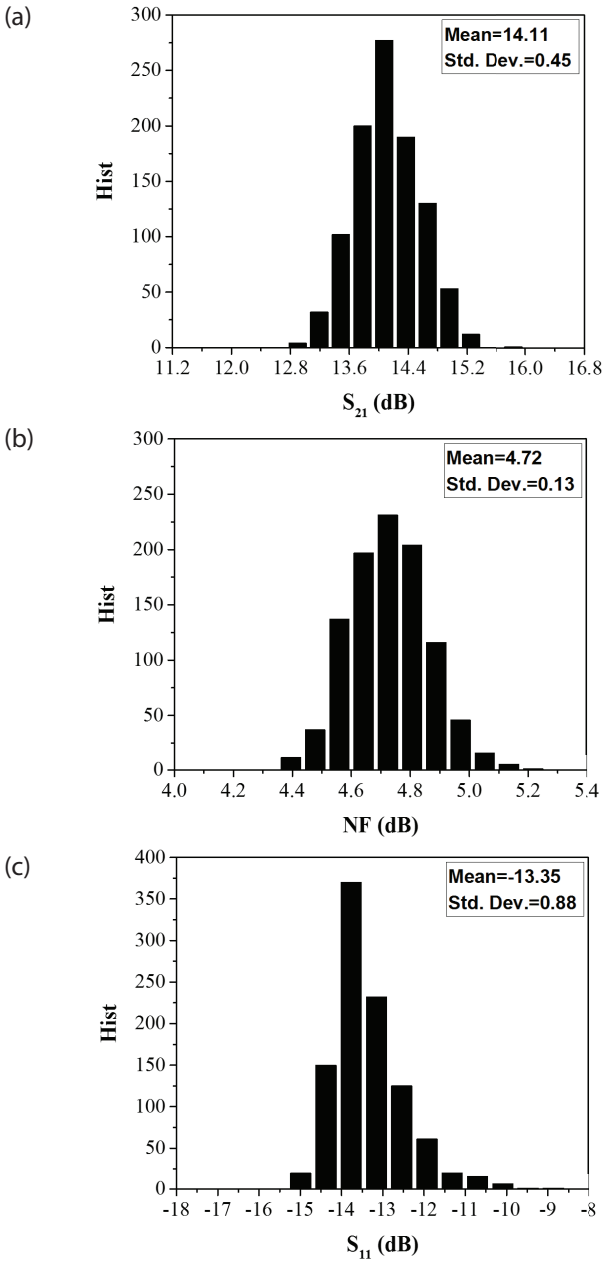


**Figure 19:** Monte Carlo simulation results at 5.2-GHz for (a) $S_{21}$ (b) NF and (c) $S_{11}$.

$$FoM = 10log\left(\frac{10^{\frac{S21(dB)}{20}} \times \sqrt{f_1 \times f_2}}{10^{\frac{NF(dB)}{10}} \times 10^{\frac{S11(dB)}{20}} \times P(W) \times Size(mm^2)}\right) \quad (22)$$

where $f_1$ and $f_2$ represent the centre frequencies of the low band and the high band of the concurrent DB-LNA, respectively. According to Table 4, the DB-LNA in (Roobert & Rani [25]) presents a high power gain and low NF at both bands. However, its operating frequencies are lower than those of the proposed DB-LNA. Moreover, (Neihart et al.,[26]) achieves a low power DB-LNA. However, it suffers from the unbalanced amplitude of the gain at the operating frequencies. As seen in Table 4, the proposed circuit exhibits high and balanced amplitude of the gain and excellent input matching, moderate linearity, and power dissipation.

## 4 Conclusion

This paper proposed and analytically investigated an inverter-based concurrent dual-band LNA (DB-LNA) operating at 2.4/5.2-GHz. By inserting an LC network at the wideband LNA output, the dual-band operation is achieved. Analytical expressions for the gain, input matching, and noise figure are presented. In addition, the trade-off between the noise figure, and the input matching is detailed. The post-layout simulated circuit exhibits 13.7 dB/14.1 dB power gain and 4.2 dB/4.6 dB noise figure at 2.4 and 5.2 GHz, respectively. Moreover, it draws a current of 7.2-mA from 1.5 V supply. Compared to other DB-LNAs, the proposed LNA presents a high balanced gain, proper roll-off, and good input matching. The proposed concurrent DB-LNA could thus be a good choice for multiband receivers.

**Table 2:** The performance of the proposed DB-LNA for different process corners and temperature

| Parameter | $S_{21}$ (dB) | NF (dB) | $S_{11}$ (dB) | $P_C$ (mW) | IIP3 (dBm) |
|---|---|---|---|---|---|
| FF@-40 °C | 19.3/22.9 | 2.9/3.4 | -8.9/-17.1 | 16.6 | -7/-8.5 |
| TT@27 °C | 13.7/14.1 | 4.2/4.6 | -12.9/-14.6 | 10.8 | -6/-11 |
| SS@85 °C | 7.9/6.4 | 5.9/6 | -21.7/-12 | 7.4 | -6.5/-8 |

**Table 3:** The performance of the proposed DB-LNA for power supply variation

| VDD (V) ±10% | $S_{21}$ (dB) | NF (dB) | $S_{11}$ (dB) | $P_C$ (mW) | IIP3 (dBm) |
|---|---|---|---|---|---|
| 1.35 | 9.3/8.4 | 4.8/4.7 | -17.8/-13.6 | 5.6 | -10/-12.4 |
| 1.8 | 13.7/14.1 | 4.2/4.6 | -12.9/-14.6 | 10.8 | -6/-11 |
| 1.65 | 16.6/17.9 | 3.9/4.7 | -11.2/-13.4 | 18.1 | -2/-8.5 |

## 5 Conflict of interest

The authors have no affiliation with any organization with a direct or indirect financial interest in the subject matter discussed in the manuscript.

**Table 4:** The performance summary of the proposed concurrent DB-LNA and comparison with state-of-the-art concurrent DB-LNAs

| Ref. | Tech. (nm) | $f_0$ (GHz) | $S_{21}$ (dB) | NF (dB) | $S_{11}$ (dB) | IIP3 (dBm) | $V_{DD}$ (V) | Power (mW) | Size* ($mm^2$) | FoM |
|---|---|---|---|---|---|---|---|---|---|---|
| [20] | 130 | 2.4 | 19.3 | 3.2 | -16.8 | -20.1 | 1.2 | 2.4 | - | - |
| | | 5.2 | 17.5 | 3.3 | -19.4 | -18.1 | | | | - |
| [21] | 130 | 2.05 | 14.9 | 4 | -8.6 | -2 | 1.2 | 12 | 0.44 | 5.8 |
| | | 5.65 | 14.9 | 4.8 | -32.4 | -4.2 | | | | 16.9 |
| [25] | 180 | 0.9 | 15 | 1.9 | -10 | -6 | 1.2 | 12 | 0.58 | 3.8 |
| | | 2.4 | 16 | 2 | -15 | -2 | | | | 6.7 |
| [26] | 180 | 2.4 | 14.2 | 4.4 | -14 | 3.4 | 1.8 | 7.2 | 0.61 | 8.7 |
| | | 5.2 | 14.6 | 3.7 | -13.5 | -2.7 | | | | 9.4 |
| [27] | 180 | 2.4 | 10.8 | 3.25 | -15 | 4.5 | 1.8 | 11.7 | 0.85 | 5 |
| | | 5 | 8 | 4.1 | -11 | 3 | | | | 0.9 |
| [28] | 90 | 0.9 | 22 | 2 | -21 | -5.5 | 0.5 | 5.2 | 0.091 | 24.3 |
| | | 2.3 | 24 | 2.7 | -15 | -6.65 | | | | 21.6 |
| [29] | SISL Avago ATF36163 | 2.45 | 28.4 | 0.7 | -13 | -6.6 | 1 | 36 | - | - |
| | | 5.25 | 28.8 | 1.1 | -20 | -5.1 | | | | - |
| [30] | 130 | 2.45 | 9.4 | 2.8 | -12.6 | -4.3 | 1.2 | 2.79 | 0.36 | 14 |
| | | 6 | 18.9 | 3.8 | -21 | -5.6 | | | | 21.9 |
| [31] | 180 | 1.217 | 13 | 1.58 | -10.6 | - | 1.8 | 11.6 | 0.14 | 9.5 |
| | | 1.568 | 11.5 | 3.1 | -10.7 | - | | | | 7.3 |
| [32] | 180 | 2.4 | 20 | 6.6 | -7 | - | 1.8 | 15 | 0.225 | 7.1 |
| | | 5.25 | 8 | 6.6 | -12 | - | | | | 3.6 |
| [33] | 150 PHEMT | 2.4 | 20 | 2.2 | -19 | -8.5 | 3 | 37.8 | 1.15 | 6.3 |
| | | 5 | 15 | 2 | -13 | -4 | | | | 1 |
| This work | 180 | 2.4 | 13.7 | 4.2 | -12.9 | -6 | 1.5 | 10.8 | 0.265 | 10 |
| | | 5.2 | 14.1 | 4.6 | -14.6 | -11 | | | | 10.6 |

*Excluding Pads

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# Multiband Stepped Antenna for Wireless Communication Applications

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**Abstract:** In this paper, a novel design of a coplanar waveguide fed (CPW) triple-band antenna is introduced. An ultra-wideband (UWB) characteristic is achieved by the initial design through the cut of a stepped shape from the lower part of the initial radiating patch and through the use of a truncated ground plan. To avoid the effects of the electromagnetic interferences with some co-existing wireless communication systems, a transition from the UWB to multiband function is assured by etching a simple circular ring inside the radiating patch. The antenna is printed on the low-cost FR4-substrate having a compact size of 0.162λ0×0.123λ0×0.008λ0 at 1.57 GHz. The design and the analysis of the antenna were done using the commercially software CST Microwave Studio™ while the fabricated prototype was tested and measured by using a R&S®ZNB Vector Network Analyzer. The measurements show that the fabricated prototype resonates between 1.57-2.33 GHz (38.97%), 5.84-6.41 GHz (9.31%), and 7.93-10.88 GHz (31.37%). Besides, the proposed antenna has consistent measured radiation pattern characteristics and it also reveals an acceptable realized gain and a high efficiency over the working ranges. Hence, the designed antenna can be a good candidate for many wireless communication systems.

**Keywords:** Multiband antenna; slot antenna; triple-band antenna; coplanar waveguide fed; wireless communication systems

# Večpasovna stopničasta antena za brezžične komunikacijske aplikacije

**Izvleček:** V prispevku je predstavljena nova zasnova troplastne antene s koplanarnim valovodom (CPW). Karakteristiko ultraširokega pasu (UWB) dosežemo z rezom stopničaste oblike osnovne zasnove spodnjega dela začetne sevalne krpice in z uporabo zmanjšane talne ravnine. Da bi se izognili učinkom elektromagnetnih motenj nekaterih soobstoječih brezžičnih komunikacijskih sistemov, je zagotovljen prehod z UWB na večpasovno funkcijo z jedkanjem preprostega obroča znotraj sevalne krpice. Antena je natisnjena na poceni substrat FR4 z velikostjo 0,162λ0 × 0,123λ0 × 0,008λ0 pri 1,57 GHz. Načrtovanje in analiza antene sta bila narejena s komercialno programsko opremo CST Microwave Studio™, medtem ko je bil izdelani prototip testiran in izmerjen z uporabo R&S®ZNB Vector Network analizatorjem. Meritve kažejo, da izdelani prototip resonira med 1,57–2,33 GHz (38,97%), 5,84–6,41 GHz (9,31%) in 7,93–10,88 GHz (31,37%). Poleg tega ima predlagana antena dosledno izmerjene karakteristike vzorcev sevanja in razkriva sprejemljivo ojačenje in visoko učinkovitost v delovnih območjih. Zasnovana antena je lahko dober kandidat za številne brezžične komunikacijske sisteme.

**Ključne besede:** večpasovna antena; režna antena; tropasovna antena; napajan koplanarni valovod; brezžični komunikacijski sistemi

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## 1 Introduction

Nowadays, the wireless communication field is one of the important technologies due to many services that offers for our daily life [1]. The Ultra-Wideband (UWB) technologies have acquired an impressive and vast appreciation in the wireless world owing to their advantages. Due to the prompt and vigorous development in the wireless domain, the UWB systems can easily interfered with other co-existing narrowband systems. To avoid potential interferences, the development of multiband antennas has received widespread concentration in recent years for designing efficient compact multi-functional devices [2-4]. Thus, there are strong demands to design multipurpose antennas which should ensure a multiband operation with suitable characteristics, such as: compact structure, low manufacturing cost, low-profile, easy integrating circuit boards and good radiation performances over the working bands [5-6]. Until now, with the use of a variety of techniques, various types of multiband antennas have been presented in the literature for many wireless communication systems application such as those proposed in [5-14]. Among of usual employed techniques to produce multiband function in broadband antennas included the technologies: fractals [7-9], multilayer [10-11], meta-materials [12], stubs loaded [13], slot-etched [14], loading the matching network [15], and radiators coupling [16]. Complex Sierpenski Gasket slots have been introduced in [7] for the production of multiband function. In [8], a multiband antenna has been proposed for IMT2000, GSM1800/1900 and LTE applications; its drawbacks are its large size which is about of 58×40×1.6 mm$^3$, and its very complicated wheel-like fractal structure. In [9], a multiband antenna for mobile terminals application has been proposed; it has large dimensions and uses a complicated binary tree fractal bionic structure to produce only a dual-band function. Whilst, a complex multilayer design constructed by periodic structures has been reported in [10] for dual-band application; its big size is another main drawback. A very selective antenna has been proposed in [11] for LTE-R and 5G lower frequency operations. In addition to the enormous size that presents of about 180×60×3.2mm$^3$ it has a complicated structure and very sharp working bands. By the incorporation of split ring resonator meta-material loads, a voluminous less efficient antenna which has sharp and close working bands has been proposed in [12]. The same problem of a weak separation between the different bands has been obtained by the designed antenna in [13]. In [14], two thin U-shaped inverted slits etched on a pentagon patch have been presented for WiMAX and WLAN applications where the presented design has good performances but it is large in size. In [15 ], a triple-band ground radiation antenna excited through a Balun has been designed where the voluminous size of the designed structure is about 70×26×0.8mm$^3$. As well in [16], a multiband antenna has been proposed for many wireless communication systems, but this structure has a large physical size and sharp working bands. Thereby, the antennas mentioned above have complex structures and/or large sizes. Thus, there is a strong need to design simple antennas with reduced size for multi-systems application. A simple compact CPW-fed triple-band antenna for wireless communication systems application is presented in this paper. The triple-band operation is achieved by etching a simple split-shaped circular ring on the radiating element. The designed antenna was firstly calculated and optimized using the commercially software simulator CST Microwave Studio™. To justify the calculated results, a prototype for the proposed design was realized and measured by R&S®ZNB Vector Network Analyzer and it also was tested and measured in an anechoic chamber. The main antenna parameters such as current density distributions, voltage standing wave ratio, antenna gain and efficiency are explored.

## 2 Antenna geometry and results

The front view and the dimensions of the proposed multiband antenna are presented in the Figure 1. Its main structure includes a stepped rectangular radiator and a constricted ground plane. To mitigate the effects of the electromagnetic interferences between the UWB systems and some narrow bands co-existing wireless communication systems (Bluetooth, LTE2600, WiMAX, WLAN, and X-band downlink satellite system),

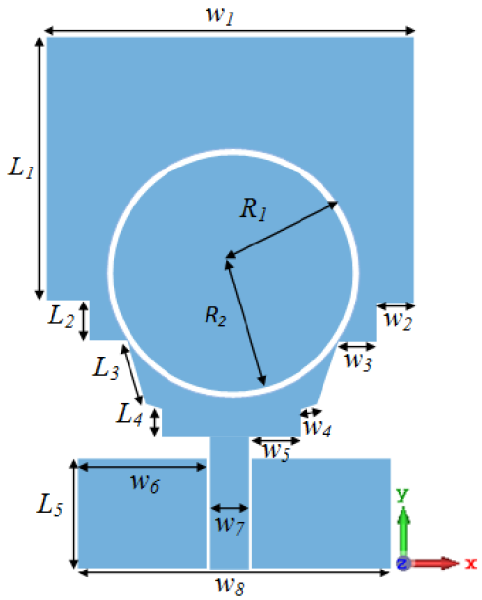
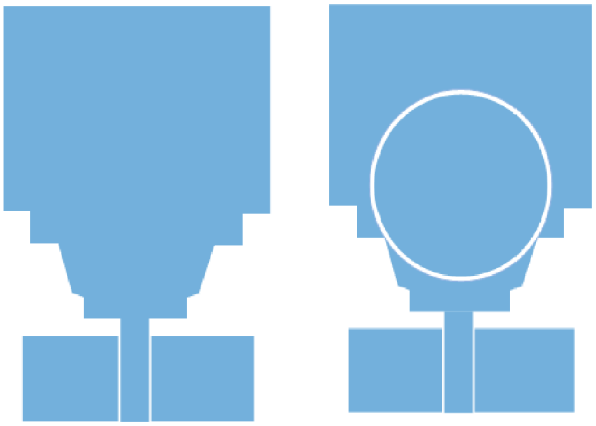



**Figure 1:** Configuration of the proposed multiband antenna.

a multiband function is introduced by etching a split-shaped circular ring on the radiating patch. The antenna is designed on a shipper substrate FR4-Epoxy having a relative dielectric constant of 4.4 and an overall size of 0.162λ0×0.123λ0×0.008λ0 at 1.57 GHz. Figure 2 depicts the designed antenna with and without the split-shaped circular ring.



(a) (b)

**Figure 2:** Antenna before and after etching the split-shaped circular ring, (a) First antenna, (b) Final antenna.

In order to understand the role of the etched split-shaped circular ring, the antenna is simulated before and after its introduction and the obtained results are illustrated in Figure 3.

It can be clearly shown that the split-shaped circular ring permits the transition from UWB to multiband function. The proposed radiating patch has a stepped shape that is created by cutting the metal from its lower part characterized by a high current distribution. The purpose of this cut is to affect the mutual and the capacitive coupling between the radiating patch and the truncated ground plane. In results, a good adaptation and a larger impedance bandwidth are achieved. Likewise, a lighter weight can be obtained; that is essentially wanted from the miniaturization viewpoint. Besides, more level of flexibility in the design and possibly minimized conductor losses are achieved. Based on the other published works like [17], the lower resonant frequency $f_r$ (in GHz) of conventional printed monopole antennas can be evaluated by the equation (1).

$$f_r = \frac{7.2}{L + W / 2\pi + s} \quad (1)$$

Here, *L* and *W* are the length and the width of the monopole; s is the gap separating the ground plane and the lower part of the radiator. The dimensions *L*, *W*, and *s* are taken in cm.

All the physical dimensions of the designed CPW-fed multiband stepped antenna were adjusted and optimized individually, by the use of the commercially software CST Microwave Studio™, to attain good performances especially in terms of working bandwidths, radiation patterns, and gain. The detailed dimensions of the proposed multiband antenna are listed in Table 1.

**Table 1:** Optimized dimensions of the proposed multiband antenna.

| Parameters | Dimensions (mm) |
|---|---|
| $w_1$ | 23.5 |
| $w_2$ | 2.19 |
| $w_3$ | 1.98 |
| $w_4$ | 0.77 |
| $w_5$ | 3.83 |
| $w_6$ | 8.84 |
| $w_7$ | 2.8 |
| $w_8$ | 21 |
| $L_1$ | 17 |
| $L_2$ | 1.98 |
| $L_3$ | 4.29 |
| $L_4$ | 1.77 |
| $L_5$ | 1.5 |
| $R_1$ | 9 |
| $R_2$ | 8.5 |

Figure 3 indicates that by etching the split-shaped circular ring on the stepped radiating element, a transition from the UWB to multiband operation is produced.

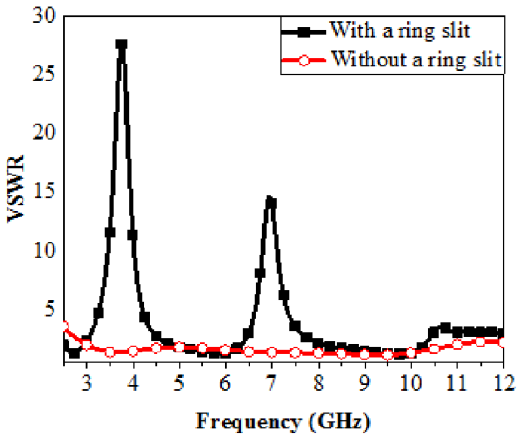



**Figure 3:** Role of the etched split-shaped circular ring on the VSWR characteristic of the proposed antenna.

The real and the imaginary parts of the impedance are depicted in Figure 4. Except around the notched bands,

the real impedance is about the input impedance of the excitation port value (50 Ω) over the operating bands. Beside, the imaginary part is almost vacillating around zero line throughout the operating bands. The Figure 5 reveals a collection of powers at the input and the output of the antenna. A good concordance can be shown between the accepted power and the radiated one which confirms a well adaptation of the antenna. Since the efficiency parameter is evaluated from the ratio of the radiated power to the accepted one, thus high level values of efficiency can be predicted at the working bands. Besides, very low power outgoing the port (i.e. power reflected back out of the input port) around the working bands is revealed, and is nearly equal to the accepted one around the rejected bands.

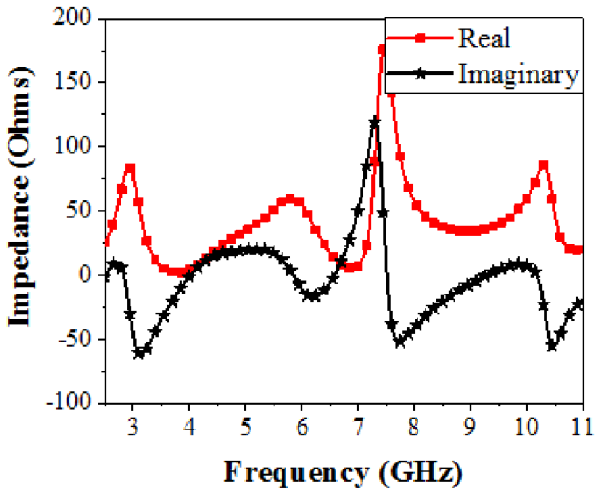



**Figure 4:** Real and imaginary impedance.

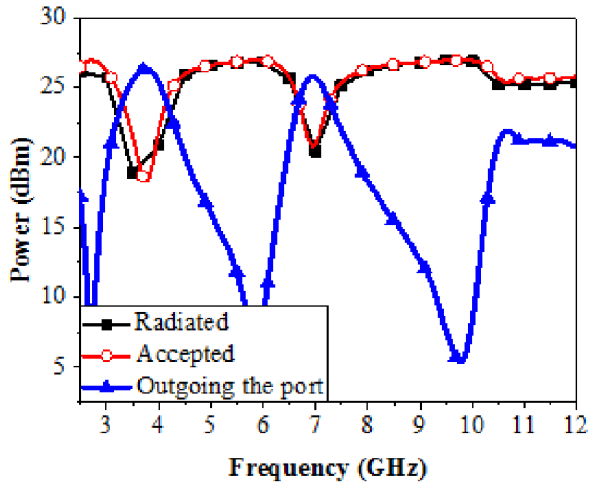



**Figure 5:** Powers at input and output of the designed antenna.

The presentation of the current distribution on the antenna's surface helps to show the structure responsible for the generation of the triple-band operation.

The current distribution on the surface of the designed antenna at the resonant frequencies of the two rejected bands is shown in Figure 6. It can be shown that at the two rejected resonant frequencies the current distribution is mightily concentrated on the split-shaped circular ring. A feeble current flowed along the rest parts of the radiating element is observed upholds the full contribution of the etched split-shaped circular ring on the rejection of the two bands and for the production of the triple-band operation. Figure 7 shows a photo of the fabricated prototypes (UWB and multi-band antennas) that are graved, by using a laser printer (LPKF S103), on the FR4-substrate with a whole size of 0.162λ0×0.123λ0×0.008λ0 at 1.57 GHz.

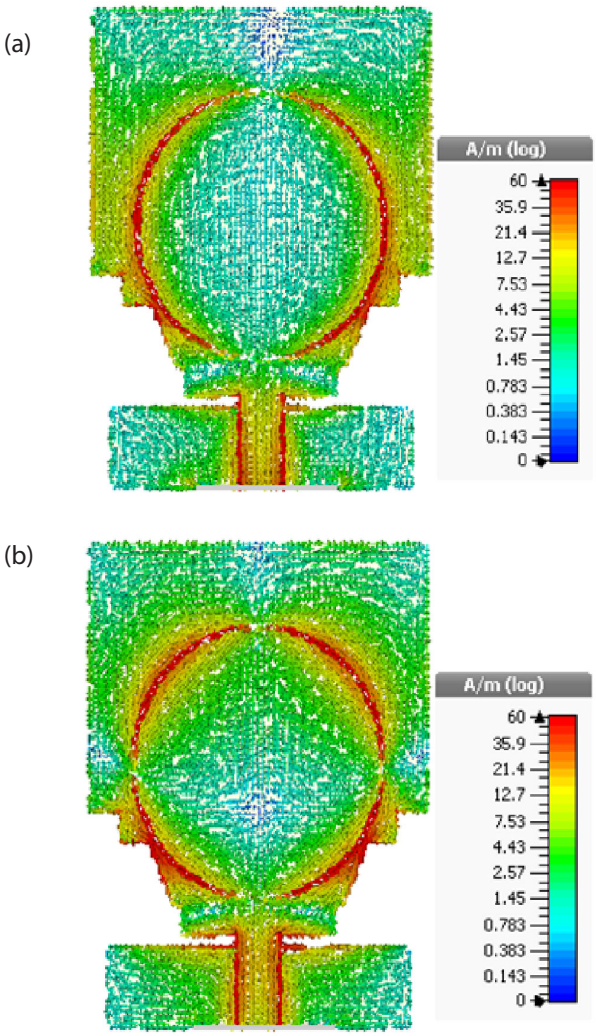



**Figure 6:** Surface current distribution on the surface of the antenna at two frequencies (a) 3.5 GHz, (b) 7 GHz.

To check the antennas operating frequencies, the voltage standing wave of the fabricated antennas was measured using an R&S®ZNB Vector Network Analyzer. Good agreements between the simulation and experimental results are achieved and the multiband char-

(a)

(b)

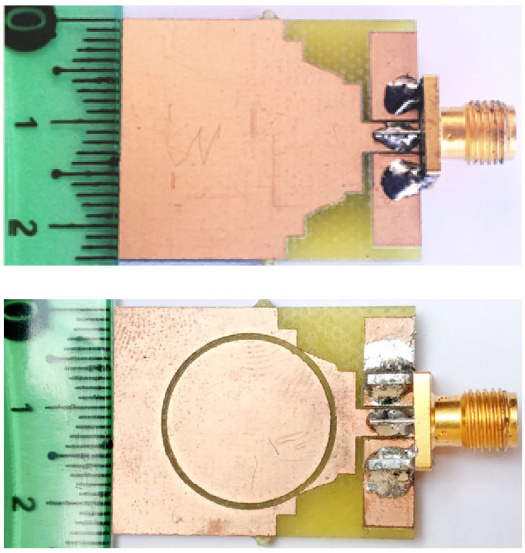


**Figure 7:** Fabricated prototypes (a) UWB antenna, (b) triple-band antenna.

acteristic of the antenna is demonstrated after etching the split-shaped circular ring. The small mismatch between the simulated results and the measured ones may be attributed to the intolerance in the fabrication and measurement processes, losses in port connection, and to inadmissible effects of the soldering that can affect the current distributions by creating parasitic inductance and capacitance links, and may be also due to the external disturbances which were not taken into account in the simulations. From the experimental results (Figure 8), the VSWR of the antenna covers the bands 1.57-2.33 GHz (38.97%), 5.84-6.41 GHz (9.31%), and 7.93-10.88 GHz (31.37%) covering the bands allocated to GSM1800, GSM1900, UMTS, GPS, GLONASS, DCS, PCS, TD-SCDMA, WCDMA, CDMA2000, DSRC, ITU8, and X band radar.

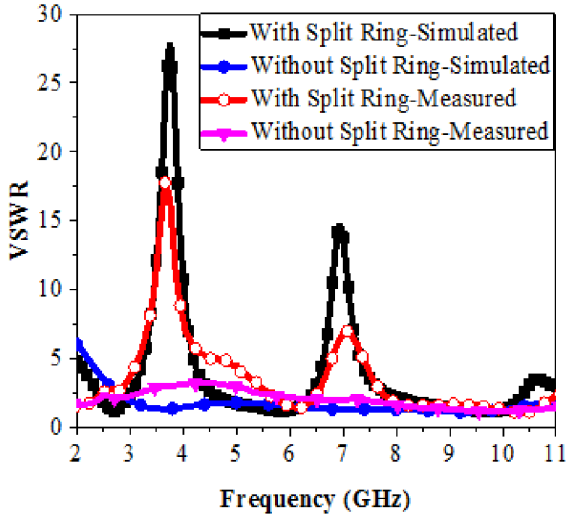



**Figure 8:** Measured and simulated VSWR of the proposed antenna with and without split-shaped circular ring.

It is evidently perceived that the introduction of the simple split-shaped circular ring on the patch of the designed antenna is responsible for the transition from the UWB to the multiband purpose and for the generation of the triple-band operation.

The radiation patterns were measured in an isolated anechoic chamber by using two antennas which are a double ridged horn antenna- model AH-118 (1-18) GHz and the fabricated antenna. Figure 9 and 10 show, respectively, the normalized co-polarization and cross polarization radiation patterns in both orthogonal planes at three different frequencies from the operating ranges: 1.99 GHz, 6.2 GHz, and 10.33 GHz.

(a)

(b)

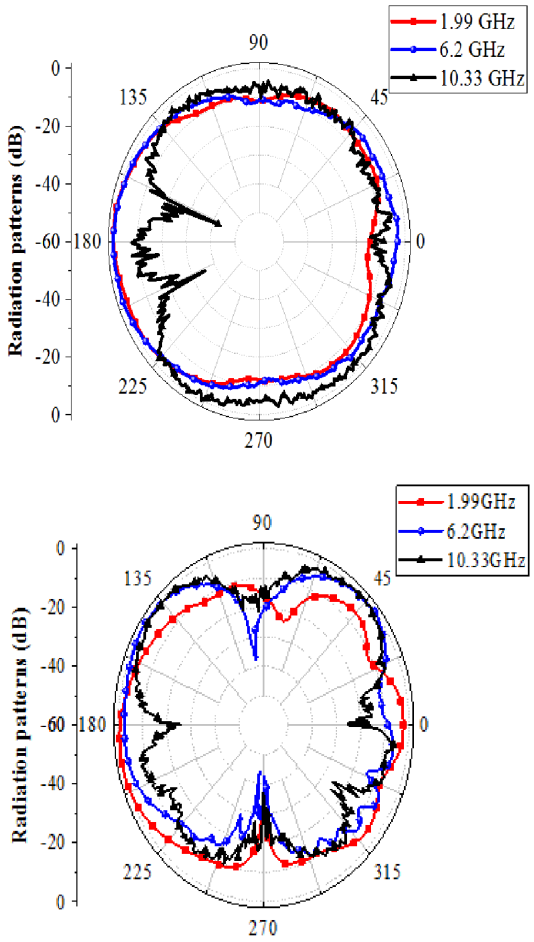



**Figure 9:** Measured normalized co-polarization radiation patterns at three frequencies, (a) *xz*-plane, (b) *yz*-plane.

We can see that the co-polarization radiation patterns are practically omnidirectional in xz-plane (H-plane) and bidirectional shape in yz-plane (E-plane). It is noted that the measured radiation patterns exhibit expected stable patterns along the working bands. Besides, with augmenting the frequency, the number and the impact of side-lobes and nulls strengthen and

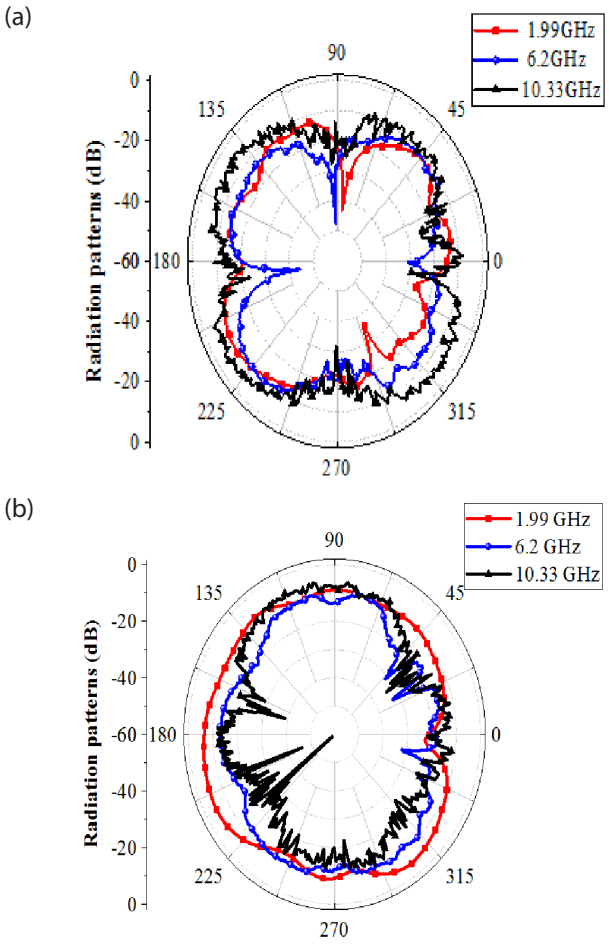



**Figure 10:** Measured normalized cross-polarization radiation patterns at three frequencies, (a) *xz*-plane, (b) *yz*-plane.

the measured antenna tends to provide bidirectional patterns in the xz-plane. Besides, analogous to the obtained results in [18-19], the cross-polarized patterns conserve their omnidirectional features over the three working bands. Figure 11 depicts the simulated realized gain and efficiency. Except at the notched bands, a reasonable and an acceptable increasing realized gain is obtained over the operating ranges; the simulated realized gain is better than the one calculated in [20].

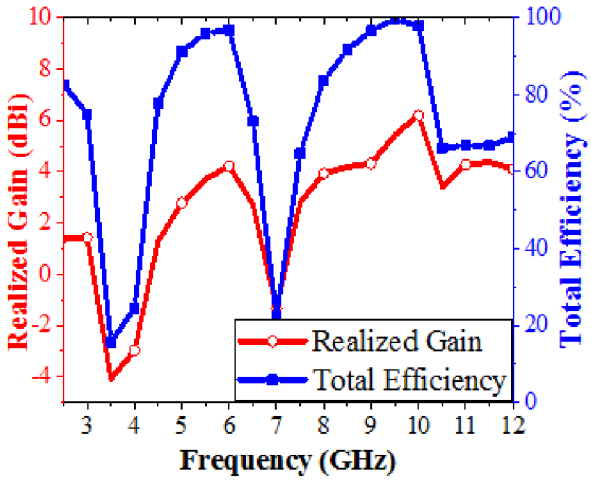



**Figure 11:** Realized gain and efficiency achieved by the proposed antenna.

Within the two notched ranges, the lowest values of the realized gain are located at around the two resonating frequencies of the split-shaped circular ring for –4.09dBi and –1.35dBi which at once validates the utility of the inserted split-shaped circular ring to produce the multiband function. As well, except at the two rejected bands, the simulated antenna efficiency is steady which is almost over than 80% along the working ranges; with two lowest values located of the two resonance frequencies of the etched split-shaped circu-

**Table 2:** Proposed antenna's comparative analysis with other recent reported antennas.

| References | Substrates | Sizes (mm3) | Bandwidths |
|---|---|---|---|
| [22] | Rogers 4003 | 40 × 50× 0.812 | 2.39–2.59 GHz (8.03%), 3.1–3.57 GHz (14.09%), 5.45–6.5 GHz (17.57%) |
| [23] | Rogers 6010LM | 50 × 50 ×2.54 | 0.7–0.96 GHz (31.32%), 1.18–3 GHz (87.08%) |
| [24] | FR4 | 61× 41× 1.6 | 1.379–1.564 GHz (12.57%), 2.947–3.075 GHz (4.25%) |
| [25] | FR4 | 125×108×1.6 | 1.53–1.97 GHz (25.14%), 2.22–2.56 GHz (14.23%), 3.31–4 GHz (18.88%) |
| [26] | FR4 | 60×60×1.56 | 2.31–2.89 GHz (22.3%), 4.15–4.27 GHz (2.85%), 4.64–4.74 GHz (2.13%) |
| [27] | FR4 | 40 × 40 × 1.6 | 2.88–3.92 GHz (30.59%), 5.26–6.28 GHz (17.68%) |
| [28] | FR4 | 50 × 50 × 1.6 | 2.56–3.63 GHz (34.57%), 9.35–12.25 GHz (26.85%) |
| [29] | FR4 | 60 ×60 ×1 | 2.51–3.72 GHz (38.84%), 4.83–6.37 GHz (27.5%) |
| [30] | FR4 | 60 ×60 ×1.59 | 1.96–2.33 GHz (17.25%), 3.74–10.4 GHz (94.20%) |
| [31] | FR4 | 50 ×35 ×1.6 | 2.35–3.22 GHz (34.52%), 4.78–5.79 GHz (18.39%) |
| Fabricated | FR4 | 23.5×31×1.5 | 1.57–2.33 GHz (38.97%), 5.84–6.41 GHz (9.31%), 7.93–10.88 GHz (31.37%). |

lar ring of about 15.71% and 22.22%. It is revealed that the obtained efficiency surpass the one attained by some recently published papers like in [21]. Additionally, in order to show the importance of the proposed antenna, a comparative review has been established in Table 2. It is clear that the designed antenna has a small size compared to some recently published structures.

## 3 Conclusion

A simple compact printed CPW-fed triple-band antenna has been successfully designed, fabricated, and experimentally assessed for the integration with multiple wireless communication systems. The multiband function has been introduced by etching of a split-shaped circular ring on the radiating patch and exploring its effect on the initial designed UWB antenna. The advantage of the introduced concept is the simplicity of the transition from the UWB to multiband function. The measured working impedance bandwidths extends from 1.57-2.33 GHz (38.97%), 5.84-6.41 GHz (9.31%), and 7.93-10.88 GHz (31.37%), covering the spectrum reserved to GSM1800, GSM1900, UMTS, GPS, GLONASS, DCS, PCS, TD-SCDMA, WCDMA, CDMA2000, DSRC, ITU8, and X band radar. The proposed antenna reveals consistent measured radiation patterns with acceptable realized gain and high efficiency over the operating bands. The simple geometry and the compact structure of the designed antenna meets the requirement of many wireless communication systems.

## 4 Acknowledgments

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## 5 Conflict of interest

The authors declare no conflict of interest.

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# Performance Analysis of Dispersion Compensation Schemes with Delay Line Filter

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**Abstract:** Optical communication is an effective system to achieve the high-speed data transmission for long distance. The main factor that affects the optical communication is dispersion. Dispersion leads to reduction of the system performance and Q-factor. Dispersion can be compensated using various techniques. Major techniques are compensation using Dispersion Compensating Fiber (DCF), Fiber grating technique, and Delay Line Filter (DLF). Analysis has been performed on the Bit Error Rate (BER) and Quality Factor (Q-Factor) of various schemes based on Eye Opening Penalty (EOP) with BER analyzer for dispersion compensation. It has been concluded that Impulse Invariant Response (IIR) based DLF at average results in 50% of better compensation when compared Fiber Bragg Grating and DCF based compensation techniques. The power of the received signal when transmitted at 0 dBm for 120 kms is –12.325 dBm which is the optimum power in which the signal can be received without distortion.

**Keywords:** Delay line Filter, BER, Q factor, Dispersion Compensation

# Analiza učinkovitosti disperzijskih kompenzacijskih načrtov z linijskim kasnilnim sitom

**Izvleček:** Optične komunikacije so učinkovit sistem za hiter prenos podatkov na dolge razdalje. Glavni dejavnik, ki vpliva na optične komunikacije je razpršitev (disperzija). Razpršitev vodi v zmanjšanje sistemskih zmogljivosti in faktorja Q. Razpršitev je mogoče kompenzirati z različnimi tehnikami. Glavne kompenzacijske tehnike so kompenzacija z uporabo vlaken za kompenzacijo disperzije, tehnike vlakenske periodične strukture in linijskim kasnilnim sitom. Opravljena je bila analiza pogostosti bitne napake in faktorja kvalitete (faktor Q) različnih načrtov kompenzacije disperzije, ki temelji na odprtosti očesnega diagrama z analizatorjem pogostosti bitnih napak. Ugotovljeno je bilo, da linijsko kasnilno sito z neskončnim impulznim odzivom v povprečju doseže 50% boljšo kompenzacijo v primerjavi s kompenzacijskima tehnikama vlakenske Braggove periodične strukture in vlakna za kompenzacijo disperzije. Pri oddajni moči 0 dBm je moč sprejetega signala po 120 kilometrih –12.325 dBm , kar je optimalna moč pri kateri je mogoče signal sprejeti brez popačenja.

**Ključne besede:** linijsko kasnilno sito, BER, factor Q, kompenzacija razpršitve

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## 1 Introduction

Optical communication is the methodology that allows light through an optical fiber for transmitting information from one place to another. The three basic components for optical transmission systems are fiber medium, light source and light detector. The communication channel must allow the optical signal to reach the receiver without any distortion by the channel. Information passes through the optical fiber experiences dispersion and attenuation which is the main factor that affects the communication. Mostly the lightwave system uses optical fibers as the communication channel. The reason is that silica fiber can transmit light with very few losses. Even then, optical power reduces to only 1% after 100 km. Hence, fiber losses are always an important design issue. This can be reduced by the

use of a repeater or amplifier. Fiber dispersion is also an important issue which should be taken care during the fiber designing. The transmitted signal will be degraded if optical pulses spread significantly outside their allocated bit slot. It becomes difficult to recover the original signal with high accuracy [1]. The optical signal in the fiber experiences various non-linear effects like Raman scattering and Kerr Effect. They both limit the received signal in fibers. Also, the signal experiences various dispersion like chromatic dispersion and polarization mode dispersion, which makes fibers not practical for long distance communication [2]. Recently, research in dispersion compensation of fibers have gained momentum with increase in demand for high bandwidth communication systems. With increase in need for high capacity and high speed communication systems for future, dispersion compensation techniques for long distance fiber communication is now necessary [3]. Fiber-Optic dispersion compensation on optical transmission systems is studied using various techniques. In order to improve the overall system efficiency and to reduce the dispersion which leads to transmission degradation, several dispersion compensation techniques were proposed [4]. The techniques which act as the solution for dispersion compensation is broadly classified as: Dispersion Compensation Fibers (DCFs), High-Order Mode (HOM) Fiber, Fiber Bragg Gratings (FBG), and delay line filter. Li.,L. et.al discussed about the use of ring resonators acting as passband microwave photonic filter in order to perform dispersion compensation [5]. Poornachari, P. et.al discussed about using Side Couple Integrated Space Sequence of Resonator (SCISSOR) acting as delay line based All Pass Filter for dispersion compensation [6]. Also, Dispersion is compensated at the receiver end using Digital Signal Processing techniques. K. Zhong et.al discusses the application of signal processing at receiver end for dispersion compensation in short Optical communications [7]. Kakkar, A et.al discusses the application of digital signal processing at both receiver end and at transmitter side for dispersion compensation [8]. Dispersion is also compensated in electronics means by pre-processing the signal and compensating it for dispersion at the transmitter end by substituting the signal using 2n bit look up table [9]. Also M. A. Ilgaz, et al., discussed a flexible approach to combating chromatic dispersion in a centralized 5G network which will be focused in the future work of this paper [10].

In this paper, we have designed a novel DLF IIR filter and the performance of IIR based DLF for dispersion compensation is compared with Dispersion Compensation Fiber and Fiber Bragg grating. The above mentioned techniques under goes various disadvantages like manufacturing cost, complex design, reduced flexibility, mainly length of the fiber. The distance of 120 kms can be covered using DLF IIR filter. Also it increases the speed of execution. The computational complexity is greatly reduced by this method and improves the performance of the interlever. The main advantage of this method is that it can be used to design the band pass filter without specifying the transition regions.

## 2 Dispersion compensation techniques

In an optical medium Dispersion Compensating Fiber (DCF) provides a large negative value of chromatic dispersion at the operating wavelength. Depending on the placement location of dispersion compensation fiber it is classified as pre, post and mix compensation. Dispersion compensation fiber is used to achieve the perfect compensation. The condition for perfect dispersion compensation is [11]:

$$D_{SMF} = L_{DCF} D_{DCF} \tag{1}$$

Where $L_{SMF}$ the length of the Single Mode Fiber (SMF) in the link, $L_{DCF}$-the length of the DCF is used to obtain dispersion compensation, while $D_{SMF}$ and DDCF gives the dispersion values for the single mode fiber and dispersion compensation fiber respectively. The pulse spread due to chromatic dispersion is given [11] in the equation (2).

$$\Delta t = LD(\lambda)\Delta\lambda \tag{2}$$

Where, t is Pulse Spread (ps); L defines Fiber Length (km); $D(\lambda)$ denotes Chromatic Dispersion factor (ps/nm-km); λ represents Operating Wavelength (nm); $\Delta\lambda$ is Spectral Width of the transmitter output (nm)

### 2.1 Pre-compensation Technique

In pre compensation technique the single mode fiber is placed after the dispersion compensation fiber. The dispersion compensation fiber experiences the positive dispersion and while single mode fiber which already has negative dispersion when they connect together the dispersion gets compensated. So that the data in the receiver experience no distortion [12-15].

### 2.2 Post-compensation Technique

In post compensation technique the single mode fiber is placed before the dispersion compensation fiber. The single mode fiber produces the negative dispersion whereas dispersion compensation fiber which already has positive dispersion when connected together gets compensated and reaches the receiver without any distortion. The post compensation technique consists of a

receiver with pin diode and BER analyzer, and transmitter with laser source. The transmission channel has single mode fiber followed by DCF. In the post compensation technique the dispersion is compensated at the receiver end [16-17].

### *2.3 Mix compensation Technique*

Mix compensation is a technique in which dispersion is compensated in both transmitter and receiver side where the dispersion compensation fiber is placed before and after the single mode fiber which results in increases performance compared with other compensation technique [20-22]. Figure 1 shows the block diagram of Mix Compensation technique as pre and post compensation can be achieved by modifying mix compensation. By considering the various types of nonlinear effects based on optical transmission, the Erbium Doped Fiber Amplifier (EDFA) system is utilized. According to the placement of DCF and SMF, dispersion compensation using compensation fiber is analyzed.

### *2.4 Fiber Bragg Grating*

A FBG is one of the methods of distributed Bragg reflector to reflect back the particular wavelength of light and transmit remaining. This is achieved by creating periodic variation in the refractive index of the fiber core [23].

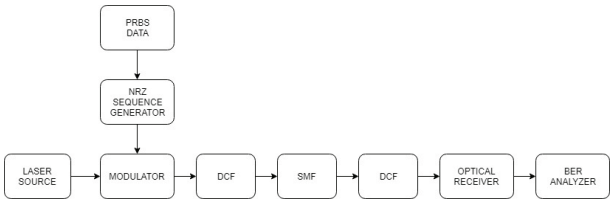



**Figure 1:** Block Diagram of Mix Compensation Technique

At each periodic refraction there is change in a small amount of reflected light. At a particular wavelength all the reflected light signals combine uniformly to one large reflection. This is referred to as the Bragg condition, and the wavelength at which the reflection occurs is known as the Bragg wavelength. The non-phase matched wavelengths are transparent fiber Bragg grating
The grating equation is [24],

$$\Lambda\left(sinsin\theta_{in} - sin\theta_{di}\right) = n\lambda \tag{3}$$

Where $\Theta_{in}$ and $\Theta_{di}$ are incident and diffracted angles.

The imprinted grating [24] can be represented as

$$n\left(z\right) = n_c + \delta n\left[1 + cos\frac{2\pi z}{\Lambda}\right] \tag{4}$$

where, $n_c$ is refractive index of core, $\delta_n$ is photo induced change in index

The reflection wavelength is given as $\lambda_{Bragg} = 2\Lambda n_{eff}$ and the peak reflectivity for the grating length of L and the coupling coefficient x is given by,

$$R_{max} = tanh^2\left(xL\right) \tag{5}$$

The full bandwidth in which the reflectivity [24] can have is

$$\Delta\lambda = \frac{\lambda_{Bragg}^2}{\pi n_{eff} L}\left[\left(xL\right)^2 + \pi^2\right]^{\frac{1}{2}} \tag{6}$$

### *2.5 Delay Line Filter*

Chromatic dispersion can be compensated using the optical filter in fiber communication. Optical communication is a way of transmitting the information by modulating the light signal with the information signal. The mathematical operation on a sampled, discrete-time signal to reduce or enhance certain conditions of that signal is performed in the digital filter. Two types of digital filters are recursive filter and non-recursive filters [25]. Delay line recursive filter is analyzed here. These filters are realized in the optical domain which comprises unit delay, weight element and adders. The input field is splitted into M+1 different elements in turn will be delayed separately by multiples of unit delays. Filter order can be determined by the highest delay. The multiple copies of the input field are recombined in the final stage.

The input field,

$$E_i = E_o\left(t\right)e^{j\omega t} \tag{7}$$

The output field composite of

$$E_o = b_o E_i + b_1 e^{j\omega T_1} E_i + b_2 e^{j\omega T_2} \tag{8}$$

Thus, the filter transfer function will be

$$H\left(e^{j\omega}\right) = \sum_{i=0}^{N} b_i e^{j\omega T_o} \tag{9}$$

Setting $Z = e^{j\omega T_0}$, transform of the filter will be

$$H\left(Z\right) = \sum_{i=0}^{N} b_i Z^{-i} \tag{10}$$

The DLF with the source of 1550nm is proposed in Figure 2 [26].

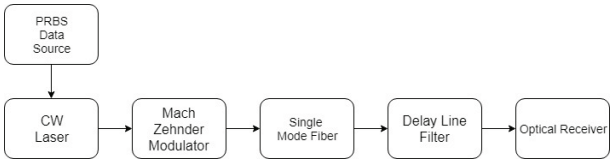



**Figure 2:** Optical link for system simulation

## 3 Implementation of DCF

Various Dispersion Compensation Modules (DCM) are implemented using Optisystem. Optisystem is a rapidly evolving software design tool that enables the user to design, test, and simulate the optical communication systems comprised of all optical components and also helps us to visualize the analysis for the optical link. Implementing realistic modeling of fiber-optic communication systems is more complex in which optisystem can offer a system level simulator for the design for the transmitter, channel, amplifier, and receiver models of the optical system. Initially compensation with dispersion compensation fiber is performed. Fiber-Optic dispersion compensation on optical transmission systems is studied using various techniques. In order to improve the overall system efficiency and to reduce the dispersion which leads to transmission degradation, several dispersion compensation techniques were proposed. Depending upon the placement of the dispersion compensation fiber the dispersion can be compensated pre, post and mix compensation method. The mix compensation portion is blocked in the layout. Transmitter system consists of the laser source, Non-Return-to-Zero (NRZ) waveform and Mach Zehnder modulator. NRZ waveform is generated from the binary values of Pseudo Random Binary Sequence (PRBS) at length of 128 bits, is provided to the Mach Zehnder modulator at a data rate of 10 Gbps. The communication system can be divided into three parts they are transmitter, receiver and channel.

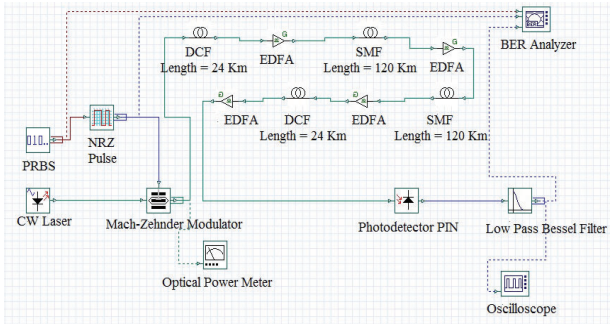



**Figure 3:** Simulation Layout of mix-Compensation Technique

The channel is the main area for the occurrence of the dispersion hence the compensation is mainly performed in the communication channel. As like the pre compensation technique the post compensation performs the same operation where the placement of the dispersion compensation fiber is after the SMF.

Figure 3 shows the simulation layout of the mix compensation technique. The mix compensation technique can be used for long distance communication. Since the dispersion is compensated in both the transmitter and the receiver side. This technique shows better performance compared to the pre and post compensation technique. Simulation layout shown in Figure 4 which clearly gives the arrangement of FBG.

The simulation of the DLF using IIR filter is given in Figure 5. Transmitter system consist of the laser source, NRZ waveform is generated from the binary values of PRBS at length of 128 bits, is provided to the Mach Zehnder modulator at a data rate of 10 Gbps.

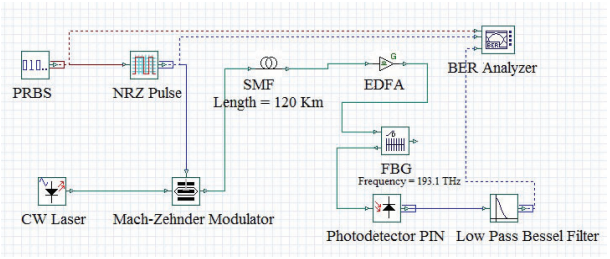



**Figure 4:** Simulation Layout of Fiber Bragg Grating

In which the BER and Q-factor can be analyzed using a BER analyzer. In this technique the dispersion is compensated using the delay line filter. The post compensation technique used in the DLF dispersion compensation, where the placement of delay line filters is followed by the single mode fiber.

The simulation of the DLF using IIR filter is given in Figure 5 from which the BER and Q-factor can be analyzed using the BER analyzer. In this technique the dispersion is compensated using the DLF. The post compensation technique used in the DLF dispersion compensation, where the placement of DLF is followed by the single mode fiber.

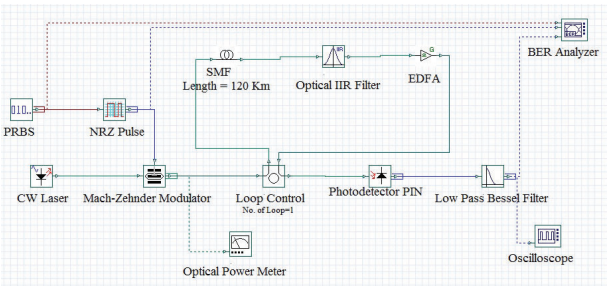


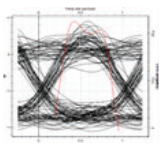
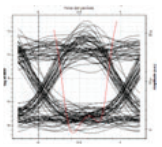
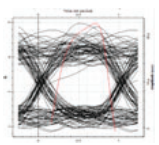
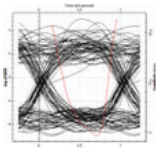
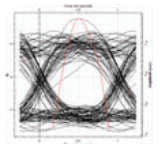
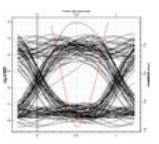

**Figure 5:** Simulation Layout of Delay line IIR Filter

## 4 Simulation results

The simulations of each technique are shown in this session. 0 dBm power is used for the transmission link. The results are analyzed at the receiver part which consist of a photo detector, electrical filter and BER analyzer where the eye pattern is analyzed. The inputs given to the BER analyzer are from PBRS at the length of 128 bits, NRZ and the output from low pass Bessel filter. Table 1 gives the BER pattern comparison of pre-compensation, post-compensation and mix-compensation. The Q-Factor and minimum BER for the compensation techniques are analyzed using BER analyzer. The Eye pattern for the simulation of pre, post and mix compensation techniques are given in Table 1.

Table 2 shows the performance comparison of Q-factor and Minimum BER. BER patterns are also analyzed using eye opening penalty which is shown in Table 1.

**Table 1:** Comparison of BER pattern for Pre, Post, Mix compensation techniques

| Parameter | Q-factor | Minimum BER |
|---|---|---|
| Pre Compensation |  |  |
| Post Compensation |  |  |
| Mix Compensation |  |  |

It is found that mix compensation gives better performance compared to the pre compensation and post compensation technique [26]. Also, the method of pre-compensation would not be suitable for systems that have variable distortion like polarization mode dispersion. Post compensation would be better equipped to handle variable sources of dispersion. But, having compensation at transmitter end and receiver end would result in better performance as seen above, but increase in performance also increases the cost of deployment of the system. Delay line based post compensation gives better performance than mixed form of compensation without the expense of increasing the cost of the system. From the comparison Table 2 the Q-factor and Min BER are also analyzed for various dispersion compensation techniques. It is clear form the result that the delay line IIR filter gives better performance.

**Table 2:** Comparison of Q-Factor and Minimum BER values

| Factors Analyzed | Q- Factor | Min BER |
|---|---|---|
| Pre Compensation | 4.89907 | 4.71181 x 10^-7 |
| Post Compensation | 4.96922 | 3.26974 x 10^-7 |
| Mix Compensation | 5.7533 | 4.23322 x 10^-9 |
| FBG | 6.16313 | 3.56 x 10^-10 |
| Delay Line IIR Filter | 11.08 | 6.8 x 10^-29 |

**Table 3:** Comparison of received power with various dispersion compensation techniques.

| Compensation Techniques | Received Power in dBm |
|---|---|
| DCF – Pre Compensation | –13.120 |
| DCF – Post Compensation | –12.109 |
| DCF – Mix Compensation | –10.125 |
| FBG | – 17.235 |
| Delay Line IIR Filter | –12.253 |

Table 3. shows the received power when a NRZ signal is transmitted in a fiber of length 120 kms. Power penalty for Delay line IIR filter is similar to other compensation techniques. However, delay line IIR filter results in a much better BER and Q-Factor when compared with other compensation techniques. Though DCF based mixed compensation technique produces better results when related with power, mix compensation requires use of two identical compensation components at the transmitter and receiver end which increases the complexity of the system. From the values of BER and Q-Factor, it can be seen that delay line IIR filter based dispersion compensation produces better results with

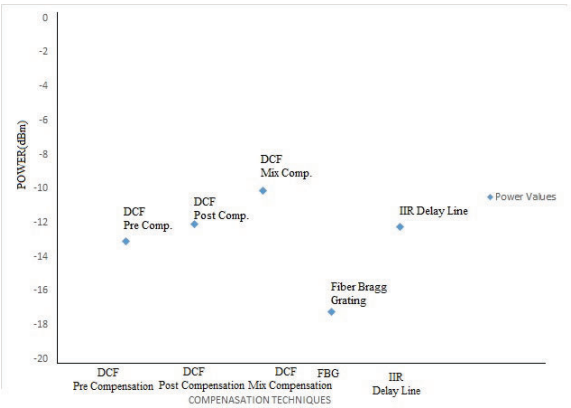



**Figure 6:** Received Power using various dispersion compensation techniques.

post compensation, when mixed compensation is used it can produce better results. But, that has been avoided as mix compensation technique can increase the complexity of the system. Figure 6 shows the received power when different compensation techniques are used.

**Table 4:** Comparison of BER pattern for DLF using FBG and DLF IIR Filter.

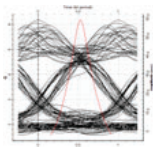
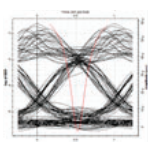
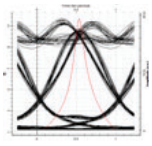
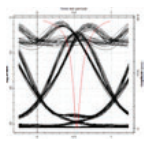
| Dispersion Compensation | Q-factor | Minimum BER |
|---|---|---|
| Fiber BraggGrating |  |  |
| Delay Line IIR Filter |  |  |

**Table 5:** Distance of Transmission vs Eye Height in DLF IIR Filter

| Distance | Eye-Height |
|---|---|
| 20 km | 0.003785 |
| 40 km | 0.001431 |
| 80 km | 0.000205 |
| 120 km | $2.9576 \times 10^{-5}$ |
| 160 km | $3.735 \times 10^{-6}$ |

The eye pattern for the fiber Bragg grating and delay line IIR filter is explained in the Table 3. Table 5. Compares the distance of transmission with eye height in DLF IIR Filter. Performance of DLF IIR filter has been demonstrated in Figure 7.

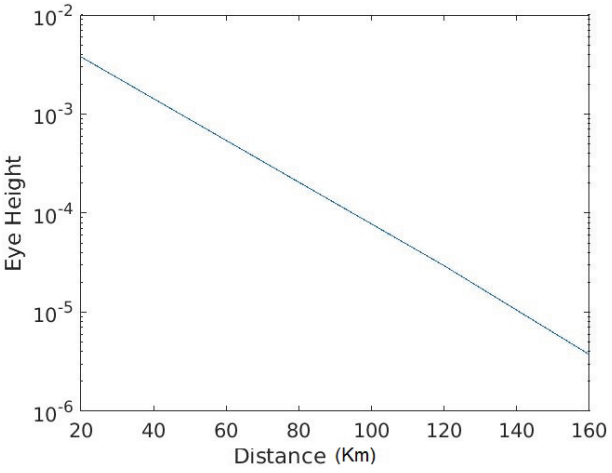



**Figure 7:** Distance of Transmission vs Eye-Height in DLF IIR Filter

## 5 Conclusions

A communication channel with laser source, NRZ waveform which is generated from the binary values of PRBS at length of 128 bits, is provided to the Mach Zehnder modulator with the single-mode fiber at the data rate of 10 Gbps for 120 km fiber is investigated. Initially, communication using single-mode fiber without any compensation schemes are analyzed, which shows when a signal travels for the longer distance it leads to the pulse spreading that results in dispersion. Dispersion compensation simulation is performed using various schemes and the performance has been compared. The most commonly used dispersion compensation techniques are pre, post and mix compensation. The performance comparison of these techniques is given in Table 2. Since there is more possibility of occurrence of dispersion in the receiver end, post compensation technique offers Q-factor of 4.96922 that gives better result compared with the pre-compensation technique. Mix compensation offers Q-factor of 5.7533 which is 13.5% greater than post compensation due to the compensation of the dispersion on both transmitter and receiver side of the optical link. The BER of the pre compensation is $4.71181 \times 10^{-7}$ which results of greater dispersion compensation, on comparing with the other compensation techniques.

Whereas the mix compensation scheme offers less bit error rate of $4.23322 \times 10^{-9}$ compared with the other two dispersion compensation schemes for the same optical link. Fiber Bragg grating also shows the effective result in the dispersion compensation compared with dispersion compensation using dispersion compensating fiber are next investigated. Ideal dispersion compensator FBG is used to provide effective Q-factor of 6.16313 which is 6.65% greater performance than Mix compensation and also offers a bit error rate of about $3.56 \times 10^{-10}$. This is because of low insertion loss. Finally, the delay line filters in dispersion compensation are also discussed. The IIR filter delay line is used to achieve better performance than other compensation techniques. The effective result can be achieved by the possible utilization of the feedback loops. On comparing the performance of the delay line filter with the other techniques, it is found that the Q-factor for delay line IIR filter of 11.08 which is 47.18% greater than Fiber Bragg grating and provides a minimum BER of 6.8 x 10^-29. Also, the IIR filter gives 50.7% higher Q-factor than Mix compensation schemes. So that the performance of delay line filters is efficient than other dispersion compensation schemes. In this work, a novel DLF IIR filter is designed, and performance of the filter is compared with other compensation techniques. The cost of implementing IIR filters to compensate dispersion is minimal compared with pre, post and mix com-

pensation techniques used in optical systems because the components used to design the dispersion compensation fibers are expensive.

## 6 Conflict of Interest

The authors declare no conflict of interest.

The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results

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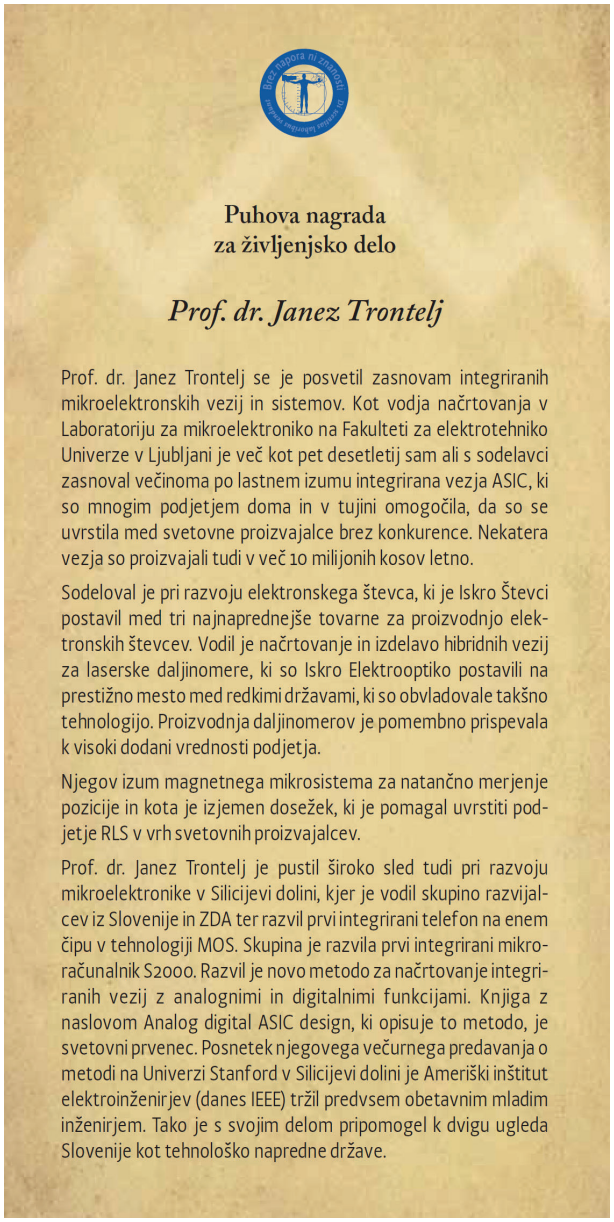
# Najvišje nagrade v slovenski znanosti v letu 2020

Odbor za nagrade, ki mu predseduje prof. dr. Janez Plavec, je konec novembra v Predsedniški palači v Ljubljani podelil najvišja priznanja za dosežke na znanstveno raziskovalnem področju. Slavnostni govornik na prireditvi je bil predsednik republike Borut Pahor.

Zoisovo nagrado za življenjsko delo sta prejela prof. dr. Stanislav Radovan Pejovnik in prof. dr. Tamara Lah Turnšek. **Puchovo nagrado za življenjsko delo** je prejel prof. dr. Janez Trontelj, dolgoletni član društva MIDEM.



Puhova nagrada
za življenjsko delo

*Prof. dr. Janez Trontelj*

Prof. dr. Janez Trontelj se je posvetil zasnovam integriranih mikroelektronskih vezij in sistemov. Kot vodja načrtovanja v Laboratoriju za mikroelektroniko na Fakulteti za elektrotehniko Univerze v Ljubljani je več kot pet desetletij sam ali s sodelavci zasnoval večinoma po lastnem izumu integrirana vezja ASIC, ki so mnogim podjetjem doma in v tujini omogočila, da so se uvrstila med svetovne proizvajalce brez konkurence. Nekatera vezja so proizvajali tudi v več 10 milijonih kosov letno.

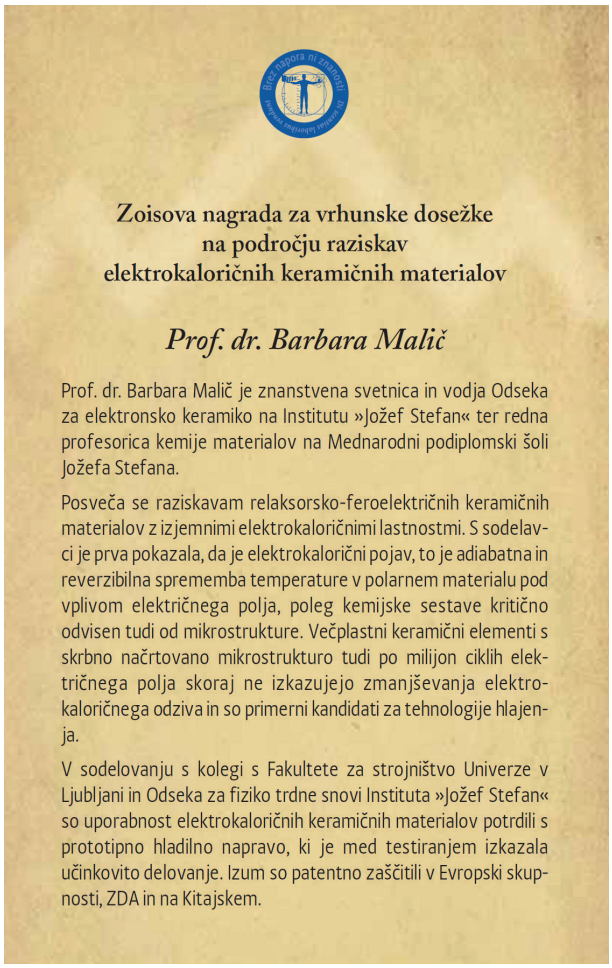
Sodeloval je pri razvoju elektronskega števca, ki je Iskro Števci postavil med tri najnaprednejše tovarne za proizvodnjo elektronskih števcev. Vodil je načrtovanje in izdelavo hibridnih vezij za laserske daljinomere, ki so Iskro Elektrooptiko postavili na prestižno mesto med redkimi državami, ki so obvladovale takšno tehnologijo. Proizvodnja daljinomerov je pomembno prispevala k visoki dodani vrednosti podjetja.

Njegov izum magnetnega mikrosistema za natančno merjenje pozicije in kota je izjemen dosežek, ki je pomagal uvrstiti podjetje RLS v vrh svetovnih proizvajalcev.

Prof. dr. Janez Trontelj je pustil široko sled tudi pri razvoju mikroelektronike v Silicijevi dolini, kjer je vodil skupino razvijalcev iz Slovenije in ZDA ter razvil prvi integrirani telefon na enem čipu v tehnologiji MOS. Skupina je razvila prvi integrirani mikroračunalnik S2000. Razvil je novo metodo za načrtovanje integriranih vezij z analognimi in digitalnimi funkcijami. Knjiga z naslovom Analog digital ASIC design, ki opisuje to metodo, je svetovni prvenec. Posnetek njegovega večurnega predavanja o metodi na Univerzi Stanford v Silicijevi dolini je Ameriški inštitut elektroinženirjev (danes IEEE) tržil predvsem obetavnim mladim inženirjem. Tako je s svojim delom pripomogel k dvigu ugleda Slovenije kot tehnološko napredne države.

*Vir: MIZŠ, Zbornik_Zois_2020.pdf.*

Med letošnjimi dobitniki štirih Zoisovih nagrad za vrhunske dosežke na posameznih področjih je tudi predsednica društva MIDEM **prof. dr. Barbara Malič**, ki je prejela ***Zoisovo nagrado za vrhunske znanstvene dosežke na področju raziskav elektrokaloričnih keramičnih materialov***.



Zoisova nagrada za vrhunske dosežke
na področju raziskav
elektrokaloričnih keramičnih materialov

*Prof. dr. Barbara Malič*

Prof. dr. Barbara Malič je znanstvena svetnica in vodja Odseka za elektronsko keramiko na Institutu »Jožef Stefan« ter redna profesorica kemije materialov na Mednarodni podiplomski šoli Jožefa Stefana.

Posveča se raziskavam relaksorsko-feroelektričnih keramičnih materialov z izjemnimi elektrokaloričnimi lastnostmi. S sodelavci je prva pokazala, da je elektrokalorični pojav, to je adiabatna in reverzibilna sprememba temperature v polarnem materialu pod vplivom električnega polja, poleg kemijske sestave kritično odvisen tudi od mikrostrukture. Večplastni keramični elementi s skrbno načrtovano mikrostrukturo tudi po milijon ciklih električnega polja skoraj ne izkazujejo zmanjševanja elektrokaloričnega odziva in so primerni kandidati za tehnologije hlajenja.

V sodelovanju s kolegi s Fakultete za strojništvo Univerze v Ljubljani in Odseka za fiziko trdne snovi Instituta »Jožef Stefan« so uporabnost elektrokaloričnih keramičnih materialov potrdili s prototipno hladilno napravo, ki je med testiranjem izkazala učinkovito delovanje. Izum so patentno zaščitili v Evropski skupnosti, ZDA in na Kitajskem.

*Vir: MIZŠ, Zbornik_Zois_2020.pdf.*

Podelitev Zoisovih in Puhovih nagrad in priznanj si lahko ogledate na povezavi:
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Iskrene čestitke vsem prejemnikom nagrad in priznanj, še posebej pa dolgoletnima članoma našega društva **prof. dr. Janezu Trontlju** in **prof. dr. Barbari Malič.**

Prof. dr. Marko Topič
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