

# *Analysis from the Perspective of Gate Material under the Effect of Negative Bias Temperature Instability*

*Nissar Mohammad Karim\*, Norhayati Soin, Fatema Banitorfian, Sadia Manzoor*

*Department of Electrical Engineering, University of Malaya, Kuala Lumpur 50603*

**Abstract:** In this article, we presented the effect of drain current on polysilicon and aluminium based p-MOSFET gates to analyze the Negative Bias Temperature Instability (NBTI) effect, as NBTI is one of the major reliability issues in submicron technology which reduces system lifetime and causes circuit failure. From the perspective of remodeling NBTI, there has been enormous amount of research works in the past. This work analyzed, NBTI from the perspective of the use of transistor gate material and compared two different gate metals under different widths of nanoscale. From the synthesized results, it was shown that NBTI effect is less in aluminium based p-MOSFETs than that of polysilicon as more amount of drain current is drawn by aluminium gate p-MOSFETs.

**Keywords:** Reliability, Negative Bias Temperature Instability, Drain Current, p-MOSFET

## *Analiza s stališča materiala vrat pri vplivu temperaturne nestabilnosti pri zaporni polarizaciji*

**Izveček:** V članku je predstavljen vpliv ponornega toka na vrata p-MOSFET tranzistorja na osnovi polisilicija in aluminija z namenom analize temperaturne nestabilnosti pri zaporni polarizaciji (NBTI). NBTI je ena izmed glavnih problemov zanesljivosti pri podmikronski tehnologiji saj zmanjšuje življenjsko dobo sistema in povzroča napake v vezju. V preteklosti je bilo na področju ponovnega modeliranja NBTI veliko raziskav. V tem delu je raziskan NBTI v perspektivi uporabe dveh različnih kovin vrat z različnimi širinami. Rezultati prikazujejo, zaradi večjega ponornega toka, manjši vpliv NBTIja p-MOSFET-ih na osnovi aluminija kot pri polisilicijevih.

**Ključne besede:** zanesljivost, temperaturna nestabilnost v zaporni polarizaciji, ponorni tok, p-MOSFET

\*Corresponding Author's e-mail: kingnissarkarim@gmail.com

### *1. Introduction*

In the field of electronics, prediction of circuit lifetime and system failure analysis has gained significance in the recent times of sub-micron technology. This raises significance concern in the applications of RF electronics, microchips and digital electronics [1-3]. Undoubtedly, these concerns are dependent on transistor reliability aspects. Negative Bias Temperature Instability (NBTI) is one of these reliability aspects; which are responsible for degrading the lifetime of transistors. As a result, the electronic devices stop functioning after a certain period of time. These phenomena have motivated researchers to work on the analysis of NBTI.

Previously, on the degradation of NBTI, various models [4-7] have been proposed by the researchers. Though, these could not find an ultimate solution for NBTI. One of the first models to define NBTI was Reaction-Diffusion model [4], which could not define NBTI in recovery stage. Alam et al. reformed this model and gave solution for many inadequacies of RD model [5]. Though, as per He et al., Alam et al. could not describe NBTI in recovery stage [6]. Many other models on NBTI also contradict with other models. As an example, the theory of Ielmeni et al. [7] contradicts with RD model in terms of frequency dependence. Still, there are works on NBTI degradation and modeling which do not give comparison with the previous models. Hence, it is difficult to get a clear picture on how to solve the NBTI issue from the perspective of degradation models. The incorpora-

tion of  $\text{HfO}_2$  was employed by Wilk et al. [8], which could not obtain a solution for NBTI degradation. Another work by Hatta et al. focused on geometric variation of p-MOSFETS where polysilicon was employed as the gate material [9]. But, none of these research works focused on the effect of NBTI when some other material is used in the gate rather than polysilicon.

From these studies, our research objective focused on the variation on the channel width of pMOSFETs by taking two different gate materials. As NBTI lowers the pMOSFET transistor parameters and drain current is one of these [10], our research will focus on the impact of drain current on two different gate materials which are polysilicon and aluminium respectively. On this analysis we will find out, in which material drain current degradation is less when the width is in different scales.

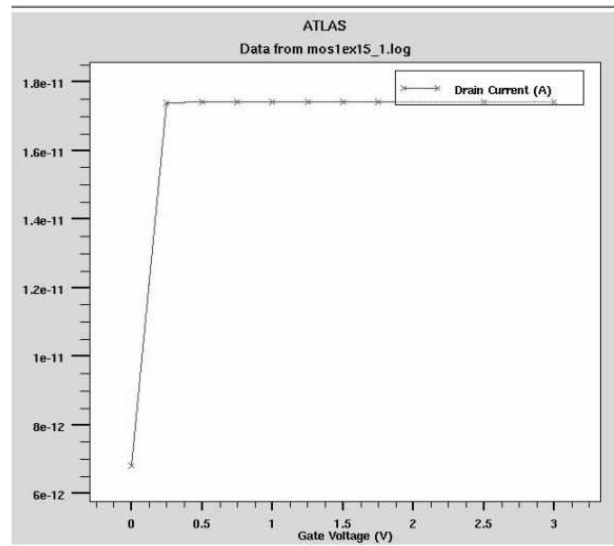
## 2. Simulation conditions and methods

To observe the NBTI characteristics, we simulated the p-MOSFET by taking a constant length (45nm) and by varying the width at 50nm and 70 nm respectively. This simulation was taken place in two stages with two different materials mentioned earlier. As polysilicon and aluminium are widely used in p-MOSFET design, we employed these two materials in our work. During the simulation process, the Effective Oxide Thickness (EOT) was kept constant and the temperature was kept to  $120^\circ$ . Silvaco simulator was used to study the NBTI effect on different gate materials.

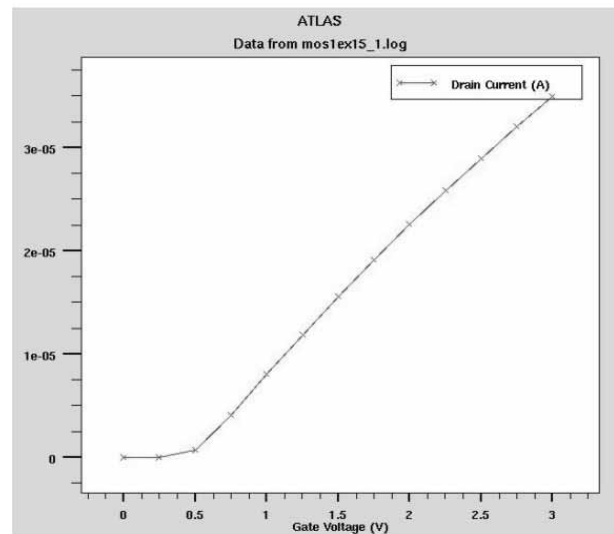
## 3. Results and analysis

From the simulation we obtained a gate voltage (v) vs. drain current (A) graph. For different negative voltages we plotted a drain current graph where the width was taken 50nm initially. At first, the simulation was performed with a gate material of polysilicon, where at 0.5 voltages we found  $1.75 \times 10^{-11}$ A current as shown in Figure 1. When the voltage was increased more, the current slightly went up and got saturated.

Having obtained the result for polysilicon with 50nm gate width, we simulated another pMOSFET with a gate material of aluminium where the channel width was same as before. At 0.5V stress, the drain current moved slightly above zero level. But, later the drain current started increasing linearly with respect to stress voltage as shown in Figure 2. In our experiment, at 3V, we found a drain current of  $3 \times 10^{-5}$ A.



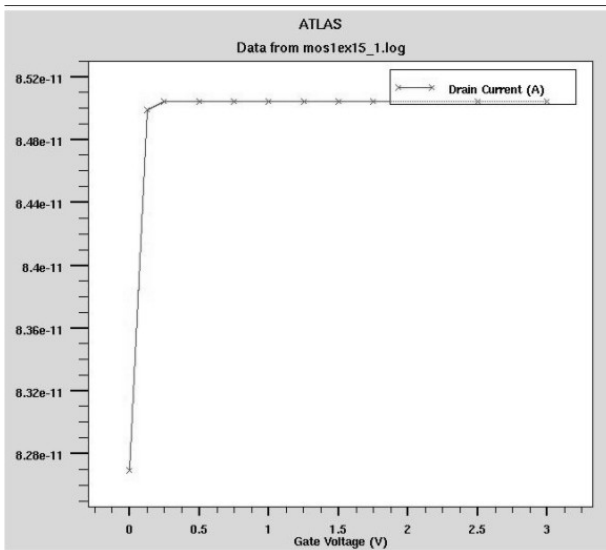
**Figure 1:** Simulation results where the gate material is polysilicon with 50nm width



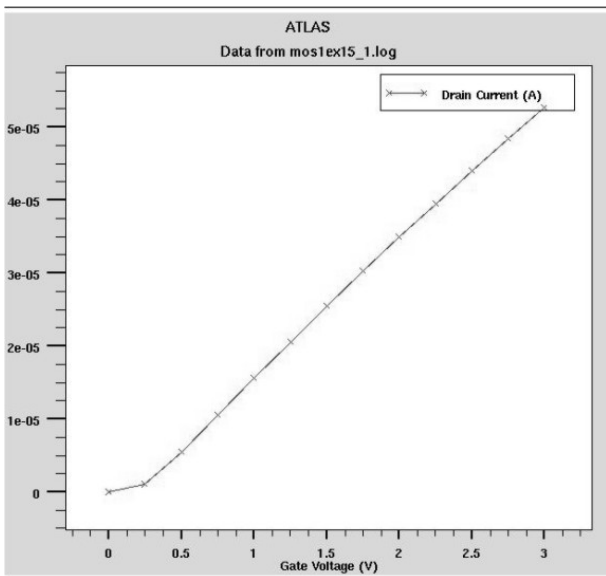
**Figure 2:** Simulation results where the gate material is aluminium with 50nm width

The simulation with poly with 70nm gate width showed a similar pattern of drain current graph as per Figure 3. Though, it exhibited a high level of drain current which is  $8.5 \times 10^{-11}$ A, which is much higher than the previous experiment with polysilicon.

Lastly, we performed the simulation for aluminium gate pMOSFET where the gate width was fixed to 70nm. The drain current pattern obtained from aluminium gate pMOSFET with 70nm channel width, was similar to the drain current pattern obtained from aluminium gate pMOSFET with 50nm channel width. In our experiment, it showed a maximum drain current of  $5.5 \times 10^{-5}$ A.



**Figure 3:** Simulation results where the gate material is polysilicon with 70nm width



**Figure 4:** Simulation results where the gate material is aluminium with 70nm width

From the above results, it is clear that at high temperature aluminium gate p-MOSFETS draw more drain current compared to polysilicon where the gate voltage is negative. On the other hand, in poly based p-MOSFETS the amount of drain current is less at an elevated temperature and negative stress. This is a persistent characteristic for different widths of transistors. Under NBTI effect, aluminium is a better choice than poly because it is more attuned with high temperature where polysilicon is more resistive at an elevated temperature. Hence, exploiting aluminium instead of polysilicon will result less NBTI effect.

#### 4. Conclusion

The reliability effect of polysilicon and aluminium gate p-MOSFET has been evaluated from the viewpoint of NBTI. We found a decreasing level of drain current in polysilicon gate p-MOSFETS due to NBTI effect where the widths of the pMOSFETS were varied. Hence, we conclude that, under NBTI effect aluminium is a better gate material than polysilicon.

#### Acknowledgements

This work was supported by the Bright Sparks Unit (BSU), University of Malaya (UM) and UM/MOHE HIRGA D000019-16001.

#### References

1. N.M. Karim, M.A.M. Ali, M.B.I. Reaz, Ask compatible CMOS receiver for 13.56 MHz RFID Reader, Informacije Midem, 40 (1), 2010, pp. 20-24.
2. H. Abdul-Majid, Y. Yusoff, R. Musa, T.K. Yew, M.-S. Sulaiman, A Low-cost Single-chip Readout Circuit for pH Sensing, Informacije Midem, 39 (2), 2009, pp. 100 -104.
3. M.A. Amiri, S. Mirzakuchaki, M. Mahdavi, Logic-based QCA Implementation of a 4x4 S-BOX, Informacije Midem, 40 (3), 2010, pp. 197-203.
4. K.O. Jeppson, C. M. Svensson, Negative Bias Stress of MOS Devices at High Electric Fields and Degradation of MOS Devices, J. Appl. Phys. 48 (1977), 2004-2014.
5. M.A. Alam, S. Mahapatra, A Comprehensive Model of PMOS NBTI Degradation, J. Microelectron. Reliab., 45 (2005). 71-74.
6. Y. He, Effect of variable body bias technique on pMOSFETNBTI recovery, Electronic Letters, 45 (2009), 956-957.
7. D. Ielmini, M. Manigrasso, F. Gattell M.G. Valentini, A New NBTI Model Based on Hole Trapping and Structural Relaxation in MOS Dielectrics, IEEE Transactions on Electron Devices, 56 (2009), 1943-1952.
8. GD Wilk, RM Wallace and JM Anthony, High- gate dielectrics: Current status and materials properties Considerations, J. Appl. Phys, 89 (2001), 5243-5275.
9. S.F.W.M. Hatta, N. Soin, D.A. Hadi and J.F. Zhang, Microelectronics Reliability, 50 (2010), 1283-1289.
10. R. Entner, Modeling and Simulation of Negative Bias Temperature Instability. PhD Dissertation, Technical University of Vienna, Austria (2007).

Arrived: 10. 11. 2011  
Accepted: 30. 06. 2012