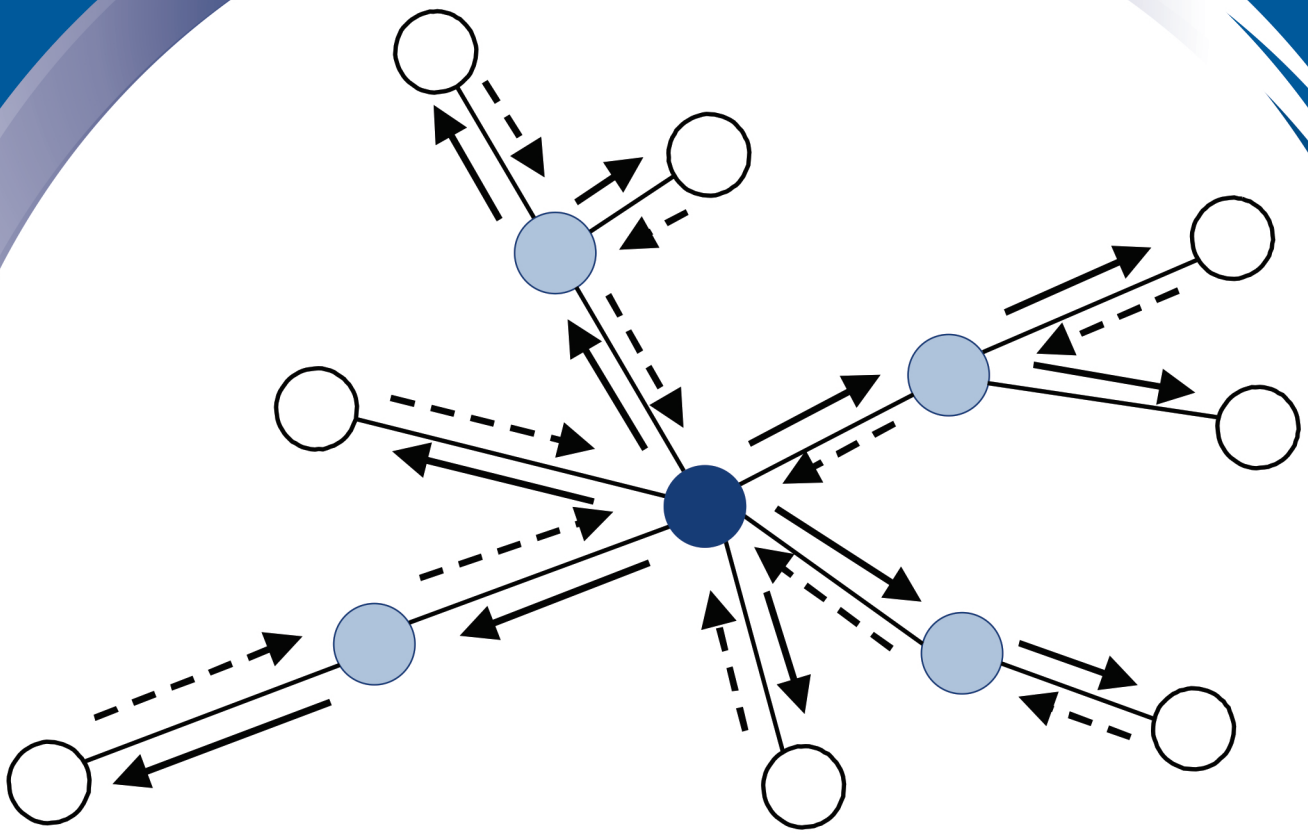
ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 48, No. 2(2018), June 2018

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 48, številka 2(2018), Junij 2018



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *2-2018*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 48, NO. 2(166), LJUBLJANA, JUNE 2018 | LETNIK 48, NO. 2(166), LJUBLJANA, JUNIJ 2018

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Headquarters | Naslov uredništva
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Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 48, No. 2(2018)

Content | Vsebina

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 48, No. 2(2018), 73 – 84

CMOS RGB Colour Sensor with a Dark Current Compensation Circuit

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Abstract: This article presents the design and development of a Red, Green, Blue (RGB) Colour Sensor with a dark current compensation circuit. The presented design employs a new approach to eliminate the conventional low pass filter, where it is normally required to integrate the pulsating signal. This is accomplished by employing switched capacitor circuit techniques. A covered photodiode is used to derive a proportional to dark current common mode voltage or compensated common mode voltage, Vdvcm. The measured performance of the sensor when it was used as an optical feedback solution for a light emitting diode (LED) backlighting system was very promising. The colour point accuracy, $\Delta u'v'$ = 0.002, while colour point drift over temperature was less than 0.008 at 50 °C. The maximum reduction of 36 mV output voltage error was observed when the Vdvcm was applied to the single to differential circuit. The overall power consumption of the fabricated sensor was 7.8 mW. The whole sensor design was implemented in 0.35 µm CMOS technology. The Vdvcm concept can be applied to other similar circuitry such as temperature-sensitive circuits.

Keywords: Integrated Circuit; RGB Sensor; Current Integration; dark current cancellation

CMOS RGB barvni sensor s kompenzacijskim vezjem temnega toka

Izvleček: Članek predstavlja obliko in razvoj RGB senzorja s kompenzacijskim vezjem temnega toka. Predstavljen dizajn, za eliminacijo pulzirajočega signala ne uporablja klasični nizkopasovni filter temveč tehniko preklopnega kapacitivnega vezja. Za določitev razmerja sofazne napetosti temnega toka ali kompenzirane sofazne napetosti je uporabljena fotofioda. Merjene lastnosti senzorja v uporabi povratne informacije LED sistema so zelo vzpodbudne. Natančnost barvne točke pri temperaturnem driftu pod 0.008 pri 50 °C je $\Delta u'v'$ = 0.002. Največje zmanjšanje izhodne napetosti je 36 mV. Senzor je izveden v 0.35 µm CMOS tehnologiji.

Ključne besede: integrirana vezja; RGB senzor; izničenje temnega

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1 Introduction

There are numerous applications of colour sensors in consumer application industries. Such applications are reflective colour sensing [1] and an optical feedback for RGB light source [2-4]. The latter application requires the system to maintain a given colour of the LEDs over temperature and time. Selecting the colour can be accomplished by specifying the colour coordinates in the CIE colour space. This is achieved via colour coordinate feedback (CCFB) technique.

An example of optical feedback solution [2] required a low pass filter (LPF), a gain stage, an analogue digital converter (ADC) and external RGB sensor. The solution is therefore unacceptable for small or portable devices which require a small footprint [3-5]. The LPF was used to average out pulse width modulation (PWM) voltage can have an effect on the response time of the total solution. Several digital colour sensors which employ light to frequency technique [6, 7] require an advanced processor such as DSP or PC to measure or calculate the frequency [8, 9].

Dark current can be caused mainly by the random movement of carriers (solely on carrier concentration) and the thermal generation combination. Dark current can affect the dynamic range [10, 11] of CMOS image sensors. It is also a subject of study in colour sensors [6] and photodetectors [12].

Reduction of dark current can increase the dynamic range of colour sensors [7]. Two approaches to reduce the dark current, namely through photodetector (photogate) physical modification [13] and secondly through electronic correction, are normally employed in a low dark current colour sensor. The latter approach was a circuit-based approach and it required a dummy photodetector. The real photo current is a result of the subtraction of active current from the photodetector and dark current from the shielded dummy photodetector [7, 14]. The photogate technique [13] required different biasing voltages; therefore, it is quite difficult to be implemented in small colour sensor design. The problem with the shielded dummy approach is that the biased voltage of the shielded photodetector differs from the one applied to the main photodetector. Recent work [15] had improved the work based on the subtraction technique [14]. An integration capacitor is usually used to store voltage, so the leakage due to switching and others has to be reduced in order not to affect the voltage stored in the integration capacitor. Another approach which was based on 'stored' voltage for biasing the current mirror or current source had been developed. This work was based on current steering of dark current to the ground instead of to the output [16]. This work however was prone to device mismatch.

Recent works [17,-19] which are based on the integrating current concept has managed to integrate ADC, RGB sensors and the function of the low pass filter (LPF) and gain stage. The works had eliminated the conventional LPF by employing an integration capacitor (C_{int}). The gain stage was also eliminated by using selectable capacitors and photodiode sizes, but the gain function remains the same. Nevertheless, the works [17], [19] did not employ a dark current cancellation circuit and the measured dark current is within 1 LSB [19]). The dark current limits the signal to noise ratio for sensors operating at high temperature or under low light conditions where the integration time is long.

The objective of this work was to solve the dark current issue in the recent CMOS colour or RGB sensor [17, 19] and improve dark current cancellation work [18]. The solution was not obvious, as either the differential transimpedance amplifier (TIA) or zero biasing technique cannot be employed in the design. The dark current cannot be cancelled at the digital level due to different sampling or integration time issues. An example of the application such as backlighting will also be presented.

This paper is organized as follows. Section 2 discusses the design aspect. It covers backlighting application, concepts, control signals, RGB Photodiode, Integrator (Switches and Capacitor array), dark current cancellation, a single to differential circuit and sample/hold (S/H) buffer amplifier and process, voltage and temperature (PVT) corners analysis. Sensor development and measurement results are discussed in section 3. This paper is concluded in the conclusion section.

2 Design

2.1 Backlighting application

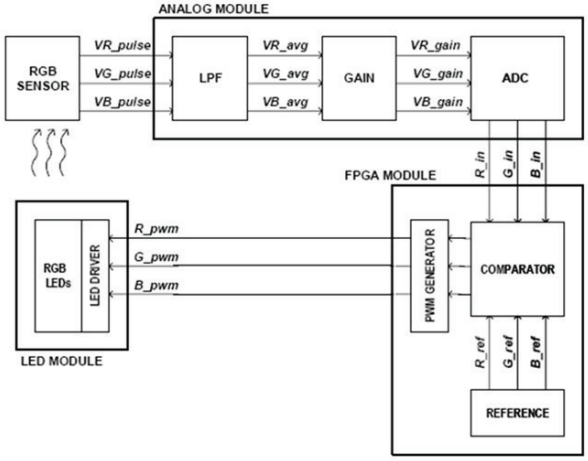

Figure 1: A typical Block diagram LED backlighting solution using optical feedback [2, 20]

The block diagram of the optical feedback system employed in RGB LEDs backlighting is shown in Figure 1. The general flow is as follows: The RGB sensor which is a colour sensor measures the intensity of each colour produced by the LED module. The low-pass filter (LPF) (in this solution only one low pass filter is used) averages the sensor voltage output over time before transferring it to an adjustable gain stage (the objective is to obtain the maximum analogue to digital converter (ADC) code when the LED is at full brightness). The ADC digitizes the averaged sensor voltage and the feedback controller (inside the FPGA) adjusts the PWM output according to the deviation of the measured sensor data from the reference values. The PWM signals are used to drive the external LED drivers, which control the on-time duration of the red, green and blue LEDs. The on-time duration is continually adjusted in real time to match the light output from the LED array to the RGB ratio needed to maintain the specified colour [2]. This measured condition-digitize-adjust is a free running process. A more detailed explanation can be found in Lim *et al.* [2]

2.2 Colour sensor concept overview

The proposed design as shown in Figure 2 is an improved version based on previous works [17 – 19]. It

receives signals from the photodiode array, a programmable setting can be applied to the signals, and it then converts the resulting differential voltage signal into digital words. The programmable settings are integration period, capacitor size and photodiode active area size. The design can sense pulsating light without the need of a filter. This is because the design works on the principle of integrating photodiode current.

Five major blocks are shown in Figure 2: test multiplexer (TEST_MUX), REFERENCE, ADC, TIMING GENERATOR and integrator and sample & hold (INTEG S&H). The TIMING GENERATOR is used to derive the required control signals (see Figure 3). INTGR and PRECHARGE SIGNALS are the inputs to the TIMING GENERATOR. The INTEG S&H block is the point of interest and will be explained in detail in this paper. Photomux shown in Figure 2 is a simplified idea; its function is to select the photodiode active area and channel or colour. Each switch for CHSEL [2:0] consists of three switches for colour selection (RGB). The integration of photo current is accomplished by using an array of capacitors, called integration capacitor, C_{int}, so together with switches (transistor symbol), it forms an integrator.

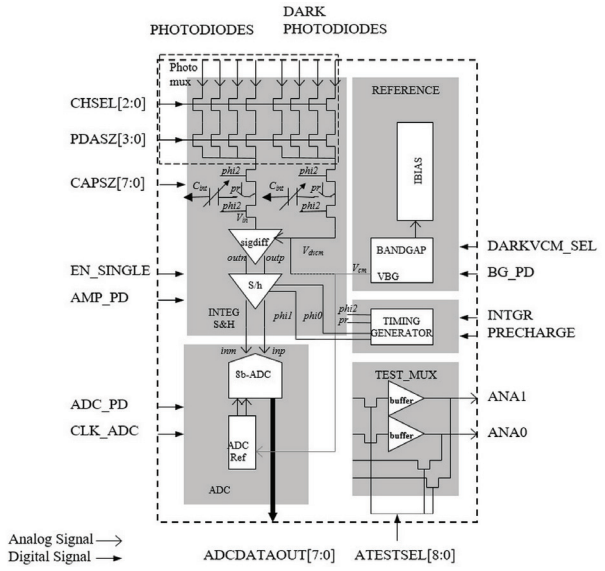

Figure 2: Block Diagram of a novel RGB colour sensor

Table 1 describes the description of the I/O of the proposed design.

Table 1: Pin List

Name	Type	Description
VDDA	P	Analog supply. Nominal 2.6V.
VSSA	P	Analog ground.
PDASZ[3:0]	DI	Photodiode size
CAPSZ[7:0]	DI	Capacitor select.
CHSEL[2:0]	DI	Channel select.
INTGR	DI	Integrating control signal
PRECHARGE	DI	Precharge control signal
EN_SINGLE	DI	Select 7 bit mode (active high)
CLK_ADC	DI	ADC clock
ADC_PD	DI	ADC power down pin (active high)
AMP_PD	DI	Amplifier power down (active high)
BG_PD	DI	Bandgap power down (active high)
DARKVCM_SEL	DI	Select normal V_{cm} (active high)
ATESTSEL[8:0]	DI	Analog test control signal (TSTMUX)
Photodiode pins	ANA	Photodiode connection
ANA1	ANA	TEST PIN1
ANA0	ANA	TEST PIN2.
ADCDATAOUT[7:0]	D0	ADC data out

The simplified integrator output, V_{in} is:

$$V_{in} = V_{prech\arg e} - \frac{I_{photodiode} \times T_{\text{int}egration}}{C_{\text{int}}} \quad (1)$$

where $V_{precharge}$ is the voltage across integration capacitor, C_{int}. The voltage is provided by the REFERENCE block. $I_{photodiode}$ is the photocurrent and $T_{integration}$ is the integration time.

From equation (1), when the light incident on the photodiode is PWM light, the integration phase (see Figure 3) is synchronized to a multiple of the PWM periods, then the voltage V_{in} is inversely proportional to the PWM duty cycle. A single to differential amplifier (sigdiff) is then used to produce the differential voltages for the differential input ADC; these values are later sampled by the S/H amplifier. In the single to differential circuit (*sigdiff)*, a compensated common mode voltage is used for dark current cancellation. The sampled values are held for analogue to digital conversion. At the same time, the C_{int} is charged back to the $V_{precharge}$ value. Details about integrator and sample hold (INTEG S&H) are discussed in Sections 2.5, 2.6, 2.7 and 2.8. A pipeline ADC with 8-bit resolution is used for analogue to digital conversion. The ADC can receive ± 1.2 V, i.e. differential input voltages with the nominal voltage (common mode voltage) of 1.2 V. The relationship of voltages and the ADC output is described in equation (2):

$$\text{ADC Output (DEC)} = \left(\frac{(inp\text{-}inm) + V_{ref}}{2V_{ref}} \right) \times 256 \qquad (2)$$

where *inp* is the positive input of the ADC, *inm* is the negative input of the ADC and V_{ref} is the reference voltage. For output of 0 DEC, the differential voltage is -1.2 V (e.g. inp = 0. 6 V, inm = 1.8 V) while for output 256 DEC (2^8), the differential voltage is 1.2 V.

Both equations (1) and (2) show that the concept is capable of integrating several functions (gain stage and LPF) into a single silicon. The REFERENCE block is used to generate bias voltages (e.g. VBG or V_{cm}) and bias currents for internal usage such as voltage to precharge the C_{int}. The design also includes extensive routing for testability. Each block's input can be overridden and each block's output can be measured. This allows an efficient means of debugging the signal chain within the design should the need arise.

2.3. Control signal

Figure 3 shows the simplified proposed control signal for the INTEG S&H block. 'pr' is the precharge control signal and 'phi2' is the signal to control the integrator switch (see Figure 5). 'phi0' and 'phi1' are signals to control the S/H buffer amplifier (see Figure 9). These signals are depicted in Figure 2.

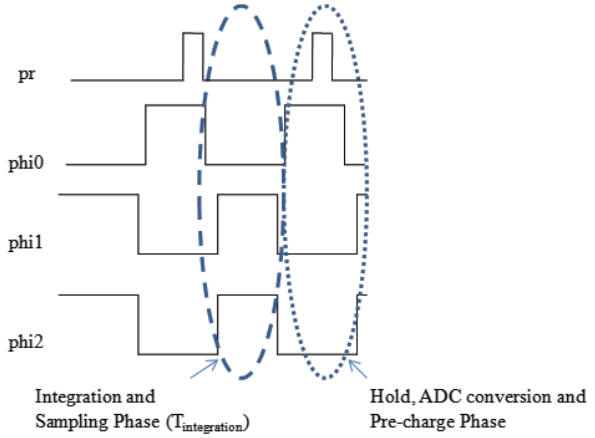

Figure 3: Control signals

2.4 RGB Photodiode

Figure 4 shows the RGB photodiodes. The RGB photodiodes are N-Well type photodiodes with colour photo array (CFA) filters [21], [22]. The RGB filters are arranged in a common centroid pattern. Photodiode sizes can be selected from ¼, ½, ¾, or full size. Light is converted to photocurrent by these photodiodes. An interface circuit called PhotoMux is designed to select photodiode sizes and channels (RGB). The total size of the RGB photodiodes is 400 µm × 400 µm.

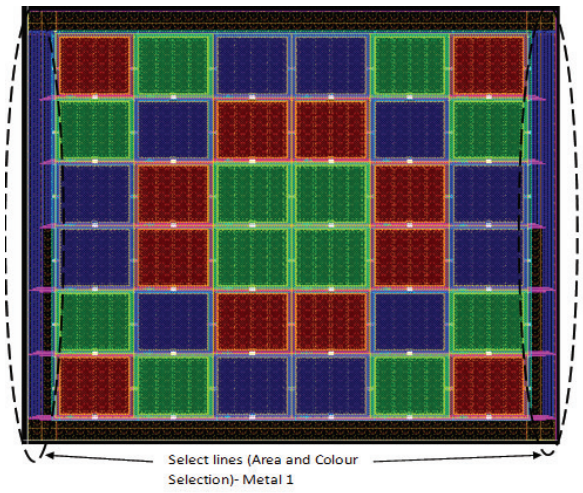

Figure 4: RGB Photodiodes

2.5 Integrator (Switches and capacitor array)

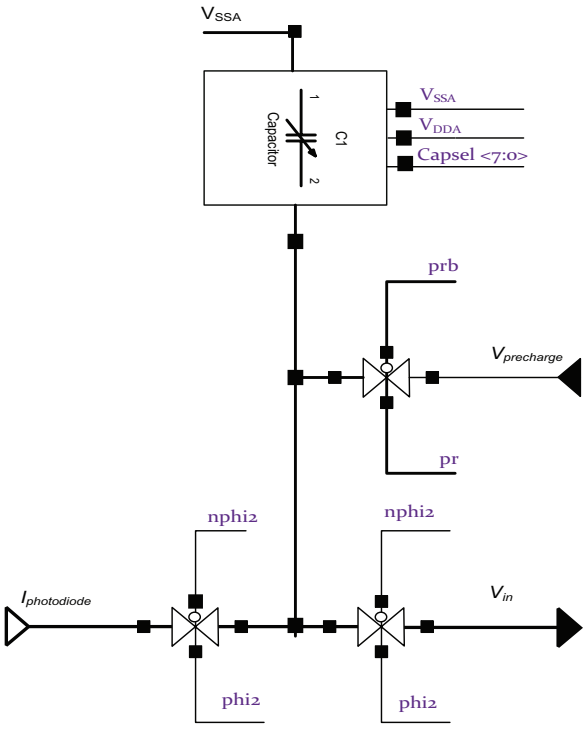

Figure 5: Switches and Capacitor Array (C_{int})

The integrator circuit in Figure 5 employs a capacitor array of 4x8 pF and switches. The value of the capacitance can be selected through the Capsel register. The capacitor block is pre-charged to ~1.8 V ($V_{precharge}$) when the 'pr' signal is high. Before the 'phi2' signal is high, the 'pr' signal is first low. The 'phi2' signal is high when integration is selected. During the integration period,

the pre-charged capacitor voltage starts to decrease as described by equation (1). The capacitor array together with photodiode sizes can be used to adjust the required V_{in}. This is similar to the gain stage function as in a prior work [2].

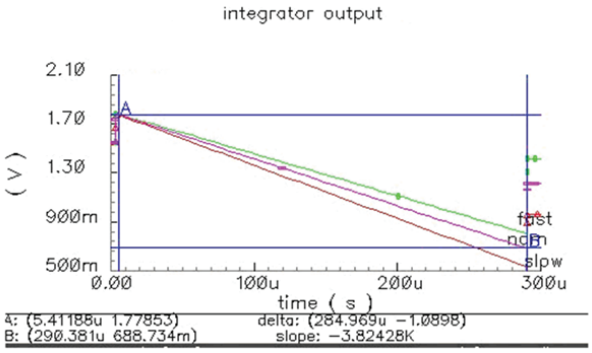

Figure 6: Integrator Output (V_{in}) Simulation at slow, fast and nominal corners

Figure 6 shows the integrator output simulation results; the simulated slope is 3824 V/s. The slope can be calculated based on equation (3):

$$I = C\frac{dV}{dT} \tag{3}$$

where *I* is the photodiode current, *C* represents the integration capacitor value and *dV/dT* is the slope. When all capacitors are selected (32 pF), the photodiode current (*I*) is 125 nA and using equation (3), the slope or *dV/dT* = 3906.25 V/s. The calculated slope is not very different compared to the simulated slope as shown in Figure 6. It is also shown that the capacitor corners (slow = minimum capacitance, fast = maximum capacitance) affect the slope more than transistor corners.

2.6 Dark current cancellation circuit concept

Figure 7 shows the dark current cancellation concept. Two operational amplifiers are used to create a single to differential circuit. The operational amplifier is based on the differential folded cascode amplifier, the concept of which is similar to a reported work [23]. Assuming no current into the negative terminal of the operational amplifier and V_{cm} is selected (DARKVCM_SEL = HI), current flowing into resistor, *R* is:

$$\frac{V_{cm} - V_{outp}}{R} = \frac{V_{outn} - V_{cm}}{R} \tag{4}$$

where V_{cm} is common mode voltage, V_{outp} is voltage of positive output, V_{outn} is voltage of negative output and R is resistor.

Re-arranging equation (4), $V_{outp} = 2V_{cm} - V_{outn}$, the differential output voltage, $V_{diff} = V_{outp} - V_{outn}$, since $V_{outn} = V_{in}$, V_{diff} is:

$$V_{diff} = 2V_{cm} - 2V_{outn} = 2V_{cm} - 2V_{\text{int}\,gr} \tag{5}$$

From equation (5), when V_{cm} is V_{dvcm}, theoretically the differential output voltage would be without a dark current element. This is firstly achieved by precharge an integration capacitor in the dark current circuit with V_{cm}. The stored voltage at the integration capacitor is discharged due to solely dark current. This voltage is now can be called V_{dvcm}. When DARKVCM_SEL is 0 V, the V_{dvcm} is applied to the operational amplifier and the dark current element from the uncovered photodiode can be eliminated. It is also easy to conclude that for the worst offset scenario of the single to differential amplifiers is:

$$V_{diff-offset} = 2V_{cm} + 4V_{offset} - 2V_{\text{int}\,gr} \tag{6}$$

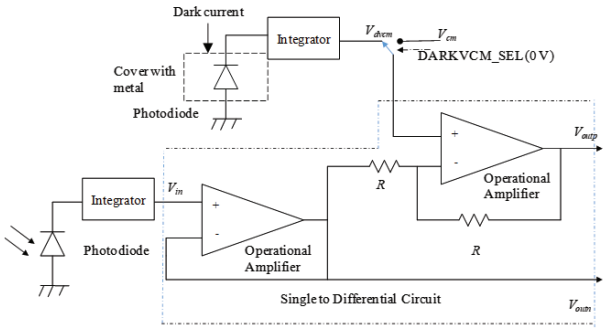

Figure 7: Dark Current Cancellation approach

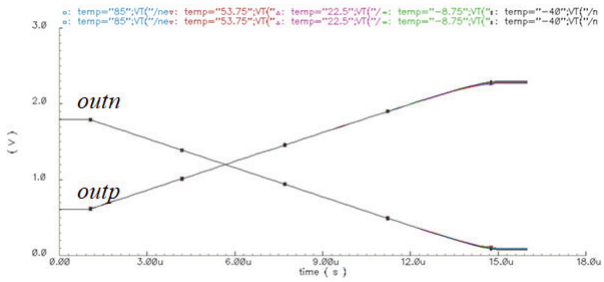

Figure 8: Non-Inverting Output (*outn*) and Inverting Output (*outp*)

The output of the non-inverting amplifier (*outn* = *inm* or input of ADC) will be cut-off at 100 mV as shown in Figure 8, which is due to the amplifier limitation. From equation (2), this corresponds to a maximum digital sensor output of 245 DEC when *outp* (equal to *inp*) is maintained at 1.2 V (a pseudo differential signal to ADC).

2.7 S/H Buffer amplifiers

An S/H buffer amplifier as shown in Figure 9 consists of an operational amplifier (Figure 10), two capacitors and switches. Bottom plate sampling is employed in the design in order to reduce the substrate noise [24].

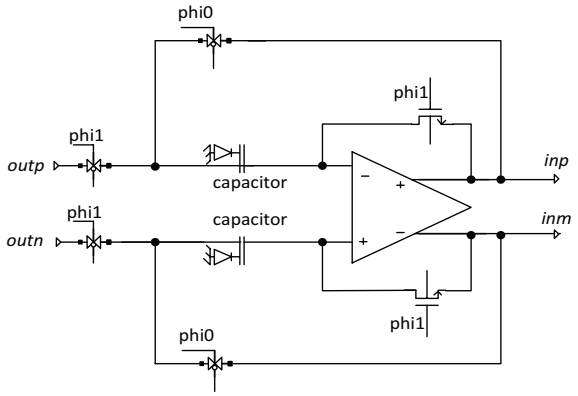

Figure 9: S/H buffer amplifier

The S/H buffer amplifier is used prior to the ADC block due to the ADC that is used in the colour sensor design is a free running ADC. Two capacitors with a value of 100 fF are used as the S/H capacitors. This value is optimized for low kT/C noise.

During the sampling ('phi0' is low) of the differential voltages, the output of the operational amplifier (as shown Figure 10) is shorted to its input and the DC voltage is set at V_{cm} by a common mode feedback circuit [25] in the operational amplifier. During the holding phase (phi1 is low) the output is shorted to the left/bottom plate of the S/H capacitor. By employing the common mode feedback circuit (CMFB), the output of this S/H buffer amplifier is always re-centred at V_{cm}. The CMFB employs the capacitive sensing technique. Two capacitors are used to average out the differential output voltage, the averaged output is connected to the CMFB amplifier input, the CMFB amplifier compares it with V_{cm} (connected to V_{ref}), and adjusts the biasing current until the averaged output is equal to V_{cm}. *ibias* is supplied by the bandgap circuit. V_{sample} is connected to phi1 while V_{hold} is connected to 'phi0'.

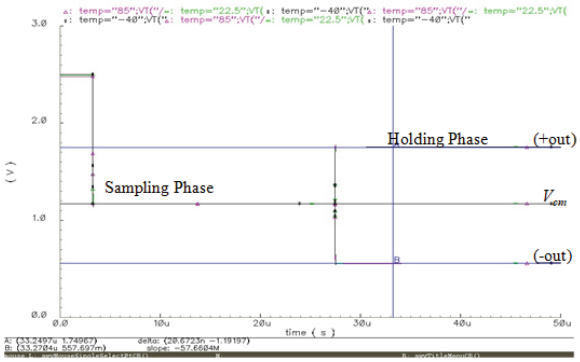

Figure 11: S/H buffer amplifier output at fast corner and vs. temperature

Figure 11 shows S/H buffer amplifier outputs during sampling and holding periods. During the sampling, both outputs are tied to V_{cm} and only during the hold-

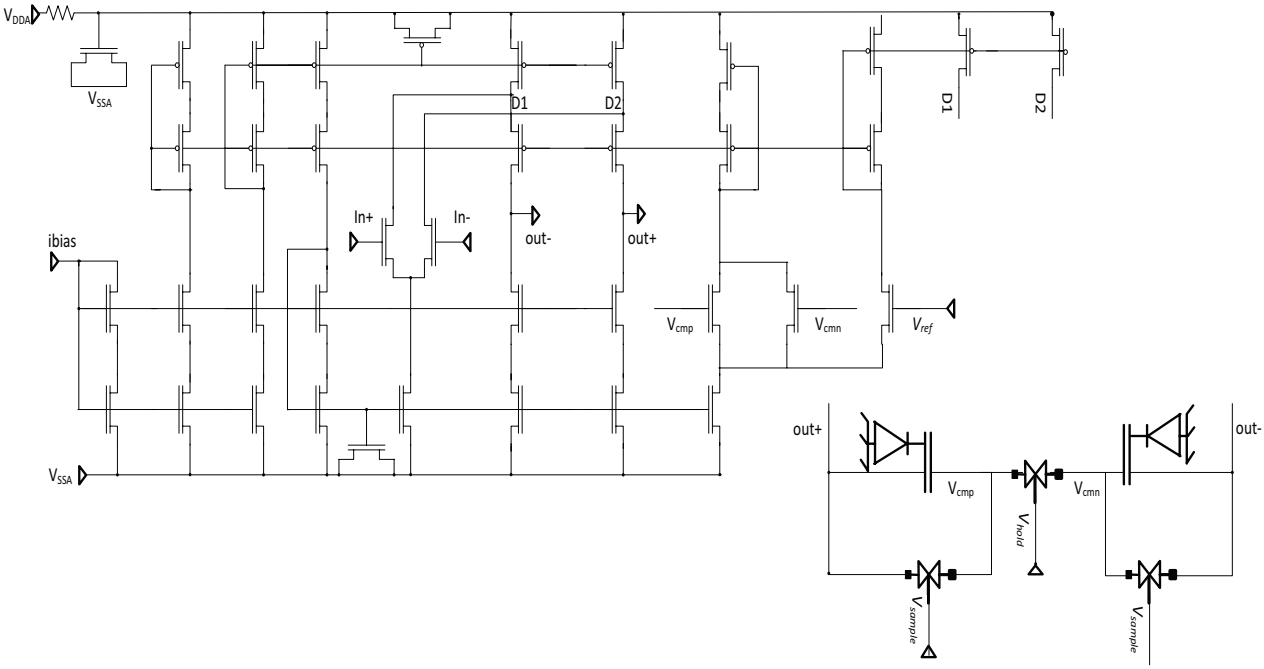

Figure 10: Differential input Operational Amplifier with the CMFB

Table 2: PVT Simulation of Sub-Blocks of INTEG S&H block

Parameter	PVT Min	PVT Nom	PVT Max	Units	Comments
Integrator output voltage	3415	3824	4349	dV/dt	Process variation
Single to differential output voltage			+2mV		From nominal differential signal
S&Hold buffer output voltage			3mV		Worst with Vdd variation

Note:
Temp= -40, 27, 85°C. FET= Fast, Slow, Nom. Resistor/Capacitor =MIN, NOM, MAX. VDD= 2.5, 2.6, 3.6 V. PVT Min = Slow, MAX, 2.5 V, 85°C corners. PVT Nom = Nom, NOM, 2.6 V, 27°C. PVT Max = Fast, MIN, 3.6 V, -40°C.

ing phase are the outputs connected to the sampled signals. Figure 11 also depicts the differential signal at an output of 1.19 V which is achieved whilst the common mode voltage is 1.19 V (V_{cm}). The S/H buffer amplifier seems immune to temperature variation (-40 °C, 22.5 °C, 85°C).

2.8 Process, voltage and temperature (PVT) corners analysis

Table 2 shows the summary of the PVT for the INTEG S& H block.

Table 3 shows the zero code calculation of pre-layout based on the output voltages of Single to differential amplifier and voltage references. The offset voltage of the amplifier is three times of PVT results as shown in Table 2.

Table 3: Zero Code Calculation based on Single to Differential Output

Parameters	Nom	Min	Max
VREFM (V)	0.602	0.57	0.619
Voffset (V)	0.006	0.006	0.006
VREFP (V)	1.750	1.727	1.773
Vcm (V)	1.167	1.151	1.178
Voutp (V)	0.602	0.593	0.601
Voutn (V)	1.744	1.721	1.767
Vref (VREFP- VREFM)	1.148	1.157	1.154
Vdiff-offset (V)	-1.142	-1.128	-1.166
Zero code (LSB)	~0	4	-2

Note: Equation 6 is used to calculate the $V_{diff\text{-}offset.}$ Equation 2 is used to calculate the zero code.

Table 4 shows the summary of the PVT zero code (photodiode current is zero) of post layout (extracted) complete design. At the PVT Nom, the design offset is at least 2 LSB. These offsets can be eliminated at the digital level.

Table 4: Zero Code Post layout Simulation of Complete Design

Parameter	PVT Min	PVT Nom	PVT Max
Integrator Output (V)	1.804	1.770	1.830
Output of single to differential amplifier (V)	1.175	1.179	1.147
Output of S/H buffer (V)	1.171	1.176	1.142
Non-overlapping-Clock, ph0-ph1 (ns)	7.85	4.15	2.94
Clock Delay, ph2-ph1 (ns)	2.83	0.9	1.06
Output ADC code	00000011	00000010	00001000

Note:
Temp= -40, 27, 85°C. FET= Fast, Slow, Nom. Resistor/Capacitor =MIN, NOM, MAX. VDD= 2.5, 2.6, 3.6 V. PVT Min = Slow, MAX, 2.5 V and 85°C corners. PVT Nom = Nom, NOM, 2.6 V, 27°C. PVT Max = Fast, MIN, 3.6 V and -40°C.

3 Sensor development and measurement results

3.1 CMOS Sensor implementation

Figure 12a shows the floor plan of the RGB colour sensor with a dark current cancellation block diagram. A Non-Overlap Block (TIMING GENERATOR) is used to generate 'phi0' and 'phi1' or 'phi2'. Biasing Circuitries (REFERENCE block) are used to provide necessary references such as *ibias*, bandgap voltage (VBG), current sources or sinks to the operational amplifiers and the ADC. VBG is a voltage reference based on bandgap voltage circuitry. The common mode voltage, V_{cm}, is based on this voltage reference. The total size of the basic core layout is 800 µm x 400 µm (without the RGB

photodiodes). Figure 12b shows the final layout of a RGB colour sensor with the dark current cancellation layout. TEST_MUX is not shown in the Figure 12a and Figure 12b. Decoupling capacitors, as shown in Figure 12b, are used to reduce noise from $V_{DD.}$ Figure 12c shows a picture of the fabricated sensor; all blocks or circuits (as in Figure 2) except the RGB photodiode are covered with a metal layer to protect them from light.

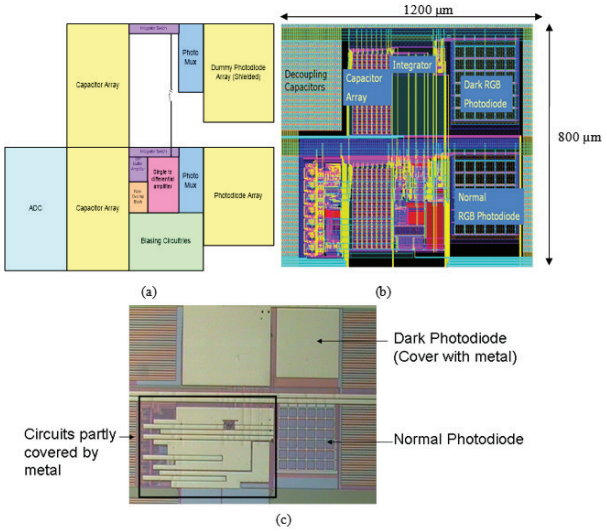

Figure 12: (a) Floor Plan of the novel CMOS RGB, (b) Layout of the implemented design, (c) Microphotograph of the novel CMOS RGB colour sensor with dark current cancellation

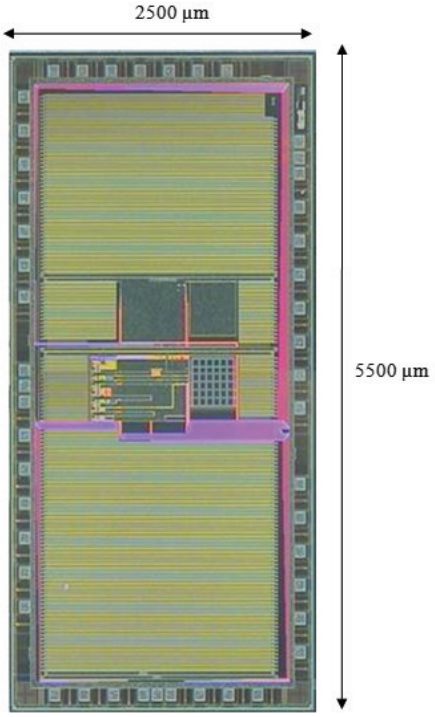

Figure 13: Microphotograph of the prototype CMOS RGB colour sensor with dark current cancellation and I/O pads

Figure 13 shows the complete prototype of the sensor with I/O bondpads. The prototype is I/O pad limited since the size is limited by the size of the I/O pad structure.

3.2 Test boards

Figure 14a shows the test system architecture for the sensor, while Figure 14a and 14b are the DUT board and Test Board respectively. The sensor was packaged in clear 48 pin TSOP and soldered onto the DUT board. Six voltage level shifter ICs (MAX 3001E) were used to connect the sensor and the PC/FPGA. These ICs were soldered onto the Test Board.

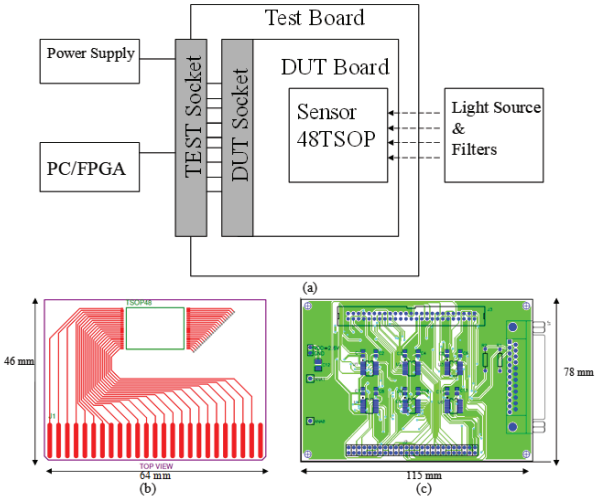

Figure 14: (a) Test System Architecture, (b) PCB drawing of the DUT board, (c) PCB drawing of the Test board

3.3 Measured colour sensor results

Table 5 shows the light intensity vs photodiode current.

Table 5: Light intensity vs photocurrent

Light intensity (lux)	Current (nA)
0	0.4
265	14
528	29
762	40
1049	55
1324	63
1583	78
1822	90

Note: Test condition: Red channel, VDD=2.6V, Integration time=150 µs, Photodiode size=400 µmx400 µm, room temp, C_{int} =32 pF

Table 6 shows the designed C_{int} value versus measured value. The value of smaller capacitors (4 pF and 8 pF), as shown in Table 6, were difficult to be realized, which could be due to a parasitic component associated with selection switches.

Table 6: Value of C_{int}

Designed value (pF)	Measured value (pF)
4	5.76
8	10.6
12	13.5
16	16.9
20	20.8
24	25.5
28	28.9
32	32.7

Table 7 shows the DC value of the voltage references (from biasing circuitries), VBG, VREFP, VREFM and total current consumption, ICC of the sensor across V_{DD} (power supply). The measured current consumption is very close to the simulated current consumption.

Table 7: Analog/bias parameters

	Simulation	Measurement		
	VDD(V)	VDD(V)		
	2.6	2.5	2.6	3.3
VBG(V)	1.167	1.171	1.183	1.171
VREFP(V)	1.750	1.757	1.76	1.75
VREFM(V)	0.602	0.624	0.63	0.617
ICC(mA)	2.856	~2	~3	~4

Based on Table 7, at nominal, the V_{cm} (which is VBG) is 1.183 V and V_{inm} (VREFP) is 1.76 V, and VREFP and VREFM are generated for ADC references. From Figure 7, V_{inp} (depicted as V_{outp} in the figure) is 0.624 V. Thus, using equation (6) and equation (2), the sensor offset is zero. This is agreed as shown in Table 3.

Figure 15 shows the ADC response or settling time (adacdataout<4>) which is 46 ns. The clock is at 4 MHz. The response indicates that the maximum ADC output frequency is approximately 21 MHz.

The results in Table 8 – Table 10 show that the sensor results agree with equations (1)-(3); hence, this has proven that the concept discussed in section 2.2 is fully functioning as designed. Out-V_{dvcm} is the sensor digital output when the V_{dvcm} is applied to the single to differential circuit. Out-V_{vcm} is the sensor digital output when the V_{vcm} is applied to the single to differential circuit. Table 8 also shows that the measured sensor offset is

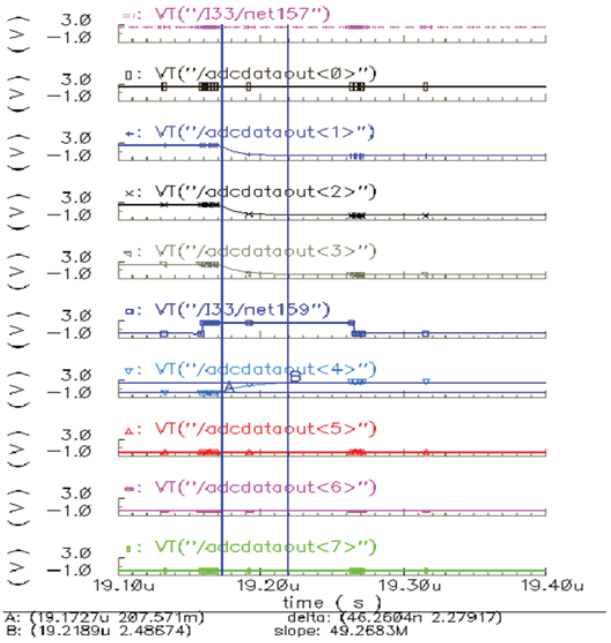

Figure 15: ADC response

similar to the post-layout simulation sensor offset, i.e. when V_{dvcm} is applied to the single to differential circuit.

Table 8: Digital CMOS sensor output vs integration time

	Integration time (unit)				
	0	4	8	12	15
Out-Vdvcm	1	12	23	32	40
Out-Vcm	2	13	23	34	41

Note:
Integration time of 0 = 150 µs.
Test condition: Red channel, VDD=2.6V, Photodiode size =100µmx400µm, C_{int}=32 pF, room temp, 150 lux.
V_{cm} = VBG, V_{dvcm} is V_{cm} generated from the dark photodiode.

Table 9: Digital CMOS sensor output vs photodiode size

	Photodiode Size(µmxµm)			
	100x400	200x400	300x400	400x400
Out-Vdvcm	39	73	105	133
Out-Vcm	39	75	106	134

Note:
Test condition: Red channel, VDD=2.6V, Integration time=15, C_{int} =32 pF, room temp, 150 lux
V_{cm} = VBG, V_{dvcm} is V_{cm} generated from the dark photodiode.

Table 9 indicates that the total integration capacitance increases when a larger photodiode is selected; however, the output is still linearly associated with the size of the photodiode.

Based on equation (2), and from Table 10, the biggest reduction of output voltage error is 36 mV when the compensated voltage common mode, V_{dvcm}, was applied to the single to differential circuit and the C_{int} is 4 pF. This observation of dark current reduction can be verified when ¼ of the dark current value (Table 5) with equation (3), equation (6) and equation (2), the calculated the dark current ADC code is 4 LSB (~36 mV). Overall, it is shown that when V_{dvcm} was applied to the single to differential circuit, an improvement of at least 1-bit resolution is achieved.

Table 10: Digital CMOS sensor output vs $C_{integration}$

	Cintegration (pF)							
	4	8	12	16	20	24	28	32
Out-Vdvcm	118	72	51	40	33	28	24	21
Out-Vcm	122	75	53	42	33	28	25	22

Note:
Test condition: Red channel, VDD=2.6V, Integration time=8, Photodiode size=100µmx400µm, room temp, 150 lux
V_{cm} = VBG, V_{dvcm} is V_{cm} generated from the dark photodiode.

As described in Table 6, the integration capacitance at the lower end is much higher than the targeted value. This will affect the value of output when 4 pF or 8 pF is selected. Nevertheless, the output follows the trend of $1/C_{int}$.

3.4 Colour point of backlighting application results

A digital controller similar to that in Lim *et al.* [2] was implemented and used to configure the basic CMOS RGB sensor as an optical feedback for a PWM-based LED backlighting solution. Several units were tested at 25°C with a power supply of 2.6 V. The colour set point was at CIE x = 0.287, y = 0.296 (9000 K). It was found that the average colour accuracy, $\Delta u'v'$, is 0.002 and the standard deviation was 0.0012.

For colour point stability measurement, RGB LEDs with colour coordinates of Red (x,y) = (0.691, 0.309), Green (x,y) = (0.161, 0.704) and Blue (x,y) = (0.131, 0.073) were used. The R:G:B luminance ratio was 2.6 : 3.9 : 1.0 respectively.

Figure 16a, 16b and 16c show colour drift with temperature (the CMOS RGB colour sensor temperatures are at -20°C, 25°C and 85°C respectively). The LED temperature was varied from 25°C to 70°C. From Figure 16a, 16b and 16c, it is shown that $\Delta u'v'$< 0.008 when the LED temperature is less than 50°C.

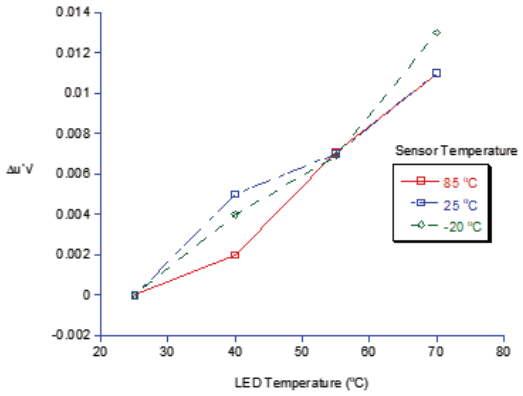

Figure 16 (a): Colour point drift with temperature at 25% duty cycle PWM

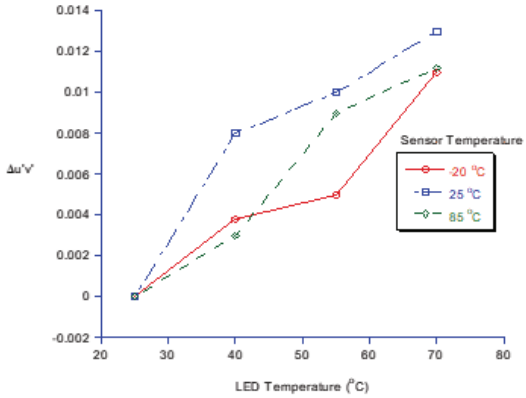

Figure 16 (b): Colour point drift with temperature at 50% duty cycle PWM

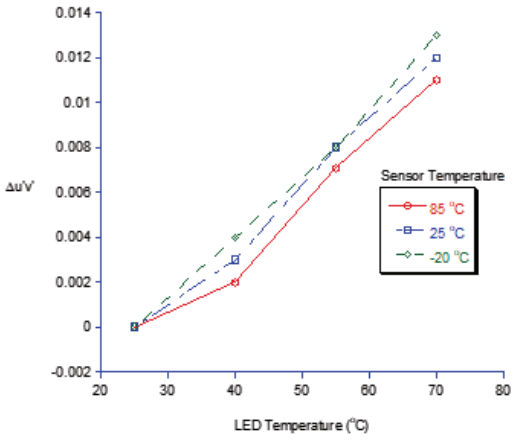

Figure 16 (c): Colour point drift with temperature at 100% duty cycle PWM

Table 11: Comparison of published colour sensors with dark current cancellation circuit

	[13]	[7]	[14]	[15]	[16]	This work
Technique	Photogate bias	Subtraction at digital level	Subtraction	Subtraction	Current source/ steer	Subtraction (modified Vcm)
Dark Current or Dark Signal	0.93 nA/cm^2 or 15 mV/s at 14 V/lux.s	Complete remove	Complete remove	Small	Complete remove. Max range is 12 nA	Complete remove
Dynamic Range (dB)	85	117	N/A	53	N/A	90
Sensor Application	Image	Color sensor	Image	Image	Image	Color Sensor

In Table 11, the performance of the presented design is compared with that of other colour or image sensors in CMOS technology. The presented design is able to completely remove dark current as described in equation (5). The work of Nahtigal and Strle [7] had achieved a very high dynamic range; however, it required a DSP to produce the required RGB colour luminosity; therefore, the work was quite complex and power consuming for portable application. The measured dynamic range (DR) of the design was 90 dB which is comparable to human eye capability. Overall, the performance of the design as a colour sensor was good and comparable to others.

Table 12: Published Colour sensor for backlighting application comparison

	[9]	[26]	This work
Topology	Analog	I-F	Current Integrating and ADC
Technology	LCD and off the shelf components	CMOS	CMOS 0.35 µm
$\Delta u'v'$	0.008	0.006	0.008
RGB	RGB Color Filter	Metal filter	RGB Color Filter

Table 12 shows the comparison of published colour sensors for backlighting application. The presented design has achieved comparable $\Delta u'v'$ results compared with several works [9], [26]. The work in Lee *et al*. [9] did use several off-the-shelf components, which will incur some cost and increase the size. Meanwhile, the work in Gourevitch *et al*. [26] required a DSP to produce the required RGB colour luminosity. The presented design is a complete integrated on-chip solution with real RGB colour signal.

4 Conclusion

In summary, the CMOS colour sensor with integration capacitor had eliminated the need for a low pass filter for detecting PWM light. The gain stage component was also eliminated by using selectable integrating capacitors and photodiode sizes, but the gain function remains the same. Together these techniques had also made the integration of RGB sensor possible. An ADC was integrated together with the circuits into a single silicon in order to produce digital outputs. The measurement results of the fabricated CMOS colour sensor with a dark current cancellation circuit had also proved that the novel dark current cancellation circuit functions as required. The cancellation of dark current was necessary for low value of C_{int} and longer integration time. The implemented CMOS colour sensor in 0.35 µm CMOS technology performed well from –20°C to 85°C as an optical feedback solution where $\Delta u'v' < 0.008$ was achieved at 50°C.

The implication of the research is the technique of using a compensated common mode voltage in the single to differential amplifier. This technique can be applied to other similar circuitries such as temperature-sensitive circuits, and in this case, the common mode voltage is temperature compensated rather than dark current compensated.

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Arrived: 24. 01. 2018
Accepted: 18. 04. 2018

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 48, No. 2(2018), 85 – 95

Multi-hop communication in Bluetooth Low Energy ad-hoc wireless sensor network

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Abstract: This paper presents a multi-hop mechanism for Bluetooth Low Energy (BLE) 4.0 ad-hoc wireless sensor network (WSN). The BLE 4.0 protocol supports only the piconet topology and does not support data transfer over multiple nodes. To overcome this limitation a mechanism to relay sensor data over multiple BLE 4.0 nodes using Master/Slave switching was developed. The mechanism dynamically creates communication paths within the BLE ad-hoc sensor network where all BLE nodes are identical. The sensor data query is initiated from a designated node and forwarded through the dynamically build network. The sensor data are collected over the same path, back to the designated node. The mechanism does not perform route discovery therefore no routing tables are needed. Using this mechanism, the range of the sensor data acquisition can be extended from BLE range to whole BLE sensor network.

Keywords: Bluetooth Low Energy (BLE); wireless sensor network; multi-hop mechanism

Multi-hop komunikacija v Bluetooth Low Energy ad-hoc brezžičnem senzorskem omrežju

Izvleček: Članek predstavlja multi-hop mehanizem za Bluetooth Low Energy (BLE) 4.0 ad-hoc brezžično senzorsko omrežje. BLE 4.0 protokol omogoča kreiranje samo piconet topologije in ne podpira prenosa podatkov preko več vozlišč. Da bi obšli to omejitev smo razvili mehanizem za posredovanje senzorskih podatkov preko več BLE 4.0 vozlišč s preklapljanjem med Master in Slave načinom delovanja. Mehanizem v BLE ad-hoc brezžičnem senzorskem omrežju, kjer so vsa vozlišča enaka, dinamično ustvarja komunikacijske poti. Poizvedba o senzorskih podatkih se sproži iz točno določenega vozlišča in se posreduje prek dinamično sestavljenega omrežja. Podatki posameznih senzorjev se posredujejo nazaj po isti poti do vozlišča, ki je poizvedbo sprožil. Glavna prednost tega mehanizma je vzpostavitev senzorskega omrežja brez usmerjevalnih tabel. Z uporabo tega mehanizma se pokritost z BLE lahko razširi na celotno senzorsko omrežje.

Ključne besede: Bluetooth Low Energy (BLE); brezžično senzorsko omrežje; multi-hop mehanizem

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1 Introduction

Bluetooth Low Energy (BLE) is a communication technology developed for low power consumption and low cost applications. It was introduced in 2006 as "Wibree" and in 2010 merged into the main Bluetooth standard with the adoption of the Bluetooth Core Specification Version 4.0 [1].

Due to the low energy consumption and ease of use the BLE technology is used in various devices, ranging from health care, fitness, home automation, toys, transportation and industry. Because of its low power consumption design, it is especially suitable for coin cell battery communication devices like wireless sensors. Several wireless sensors can form a Wireless Sensor Network (WSN) [2] that can acquire environmental data and send it through the network to the main device or gateway. From here data can be sent over existing network infrastructure to the remote client thus making a WSN and associated sensors a part of Internet of Things (IoT) [3].

In contrast to other wireless technologies, that are also used for wireless sensor networks like Zigbee and

ANT+, the BLE 4.0 only supports Peer-To-Peer (P2P) and star topology with no multi-hop capabilities. Although the BLE 4.0 protocol is already offering a wide spread of possible usage the data relaying over multiple nodes within the network would highly increase the number of potential uses.

While BLE lacks the multi-hop capabilities, there have been some attempts to implement multi-hop functionality using the Bluetooth application layer. Some implementations of multi-hop data transfer with BLE 4.0 are presented by Mikhaylov and Tervonen [4] as well as by Maharjan, Witkowski and Zandian [5]. In [4] a mechanism that relays data to a node with known address over intermediate nodes was suggested. The proposed mechanism was implemented on only four nodes carrying out two to three hops. The emphasized problem in the article is the high route time discovery, which takes about 25 seconds on average and is due to the service discovery time and data exchange for route establishment. In [5] the multi-hop mechanism is based on a tree network with unique node identity number addressing. The presented implementation of this approach limits the number of nodes that can be connected to each central device to at most three. The selected range of node addresses enables the forming of tree topology network up to level 5.

In this paper a mechanism that enables multi-hop data transfer to a central node over multiple BLE 4.0 nodes is presented. A wireless sensor network is constructed using tree topology. All wireless sensor nodes are identical and can transfer acquired data and/or relay data from the connected nodes. An evaluation wireless sensor network with 7 nodes was built to validate our multi-hop mechanism. Each node is composed of Bluegiga BLE113 [6] communication module mounted on breakout board [7], temperature sensors [8] with additional peripheral hardware, and power supply. BLE node was implemented on our developed demonstration evaluation board.

The rest of the paper is organized as follows: in the following section an overview of BLE 4.0 technology is presented. The third section is focused on the related work in BLE 4.0 multi-hop data transfer. In the fourth section our multi-hop data transfer mechanism is described. In the fifth section the implementation of the mechanism is described and the results are given. The paper concludes with section six.

2 BLE 4.0 technology

Bluetooth Low Energy (BLE) 4.0 is a wireless communication technology that allows data to be transmitted over the air between two BLE devices. It uses the 2.400 GHz - 2.4835 GHz Industrial, Scientific and Medical (ISM) band. BLE uses frequency hopping spread spectrum modulation technique called Direct-Sequence Spread Spectrum (DSSS) for interference minimization and security maximization [9]. In contrast to the classic Bluetooth that uses 79 1MHz channels the BLE frequency hopping spans over 40 2MHz channels. 37 channels are used for data transfer, whereas the remaining three channels are reserved for advertising [1].

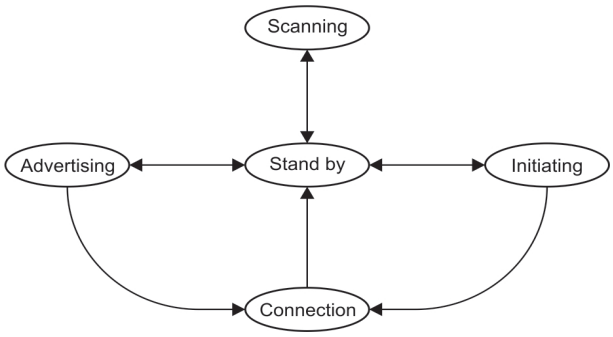

Figure 1: BLE 4.0 link layer state diagram

The connection and data transfer is achieved through the link layer state machine as shown in Figure 1. In Advertising state, the device has an advertiser role and transmits the advertisement packet on three advertising channels. The advertisement packet can contain from 2 to 31 bytes of advertisement data. Advertisement data can be intercepted by the devices that are in Scanning state. Depending on the gathered advertisement data the scanner can demand additional data, initiate the connection with the advertiser, or ignore the advertiser. After the connection is established both devices are in Connection state. Typically, the device that was initially scanning assumes the role of a master device whereas the advertising device becomes a slave device. While connected the devices cannot change their role.

When two devices are connected they form a master/slave pair as shown in Figure 2a. According to Bluetooth 4.0 standard a device cannot simultaneously assume master and slave role. Furthermore, while a master device can connect to several slave devices a slave device can connect only to one master device. This limits the possible network configurations to a P2P pair and to a simple star topology known as piconet topology, as depicted in Figure 2b.

Once the connection is established the devices can transfer data over 37 data communication channels. The data can be sent in unencrypted or encrypted packets that can have 0 to 31 bytes of Protocol Data Unit (PDU) payload [1]. Depending on the devices link layer state the PDU payload can contain the advertis-

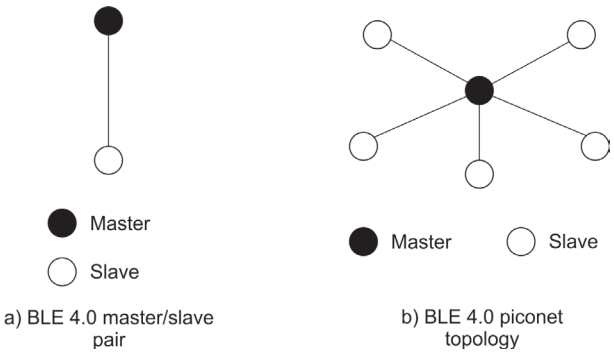

Figure 2: BLE Master/Slave connection options

ing or scanning device addresses and advertise or scanning response data. The encryption is achieved with security manager protocol (SMP) key distribution between master and slave during the pairing process.

The BLE 4.0 stack is composed of several protocol layers which can be divided into two logical entities: Controller and Host, as shown in Figure 3.

The Controller is composed of physical layer (PHY) and link layer (LL). Hardware implementation of Physical Layer is composed of a balun and an antenna which forms a radio frequency (RF) transceiver while the layers from Link Layer and above reside in a SoC.

The RF transceiver as a part of PHY is responsible for data transfer between devices.

The link layer from the Controller manages the transmission and reception of data packets with respect to the flow control and connection parameters established with other nodes. If device is in scanning, advertising or connection mode the link layer manages the data receiving and transmitting. It also provides first line of security by allowing the data exchange only from selected nodes. The connectivity between Controller and Host stack is managed by host controller interface (HCI).

Following the HCI layer are the Host layers. The logical link control and adaptation protocol (L2CAP) manages the data multiplexing for the attribute protocol (ATT) and security manager protocol (SMP). The SMP offers different security modes, data encryption and authentication services. The ATT manages the discovery of server-client attributes and enables the attributes reading and writing functionalities. The discovery and characteristics exchange of the BLE 4.0 protocol services are defined by the generic attribute profile (GATT) framework built on top of the ATT layer. The uppermost layers of BLE 4.0 stack are the generic access profile (GAP) and the applications layers. The GAP manages the communication between lower layers and applications and is responsible for establishing different modes of operation such as scanning and advertising [10].

BLE 4.0 protocol stack provides the device with all the support to operate in master or slave mode individually. Unfortunately, no support is provided for the device to operate in master and slave mode simultaneously thus BLE 4.0 protocol does not support multi-hop data transfer.

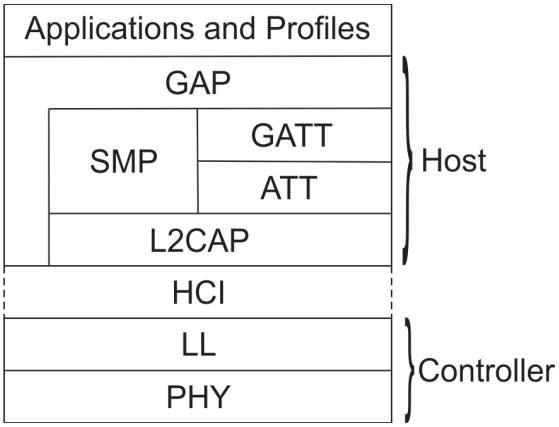

Figure 3: BLE 4.0 protocol stack

3 Current ble 4.0 multi-hop solutions

Although the BLE 4.0 emerged in 2010 there are currently just a few multi-hop implementations. In the first multi-hop implementation [4] the data transfer is achieved by implementing a new multi-hop GATT layer service. A service is divided into two parts: route discovery and data transfer. A transmitting node has a known end-node address so at first a route over intermediate nodes has to be established. At each route generation a gateway node to the target node, the target node, and number of required hops are stored in each node. After route discovery is completed the data is sent through the known route to the target node. The prime challenge at service implementation, as authors emphasized, was advertiser/scanner operational state switching and memory availability. The working multi-hop service was implemented in four nodes and results were presented. In another implementation of multi-hop data transfer [5] a tree network topology is used.

This implementation distinguishes three different node types: root node as main or central device, intermediary node that act as a peripheral or central device depending on connection initiation, and leaf nodes as the peripheral devices in the tree structure. Intermediary node is constructed from two devices: a central and

peripheral device, which are interconnected with I²C bus [11]. In their implementation the central device can be connected to at most 3 peripheral devices and with 2 byte addressing the tree network can be extended up to level 5. The tree network topology was successfully implemented and the results were presented. For future work authors emphasize on reducing the negative effects of node failures thus hopefully increasing the robustness of the network.

4 Multi-hop data acquisition mechanism

Data from distant nodes cannot be transferred using a direct connection, for instance if we have three nodes A, B, and C, as shown in Figure 4, where node C is not visible from node A, node A cannot directly acquire data from node C. In order for node A to acquire data from C, node B must first acquire data from C and then relay them to node A. To do this, node B must first become a master node, detect node C using scanning, make a connection, and retrieve data from node C. To relay data it must switch back to slave mode and advertise that the gathered data are available. The switch from slave to master operation in node B is initiated by node A inquiry.

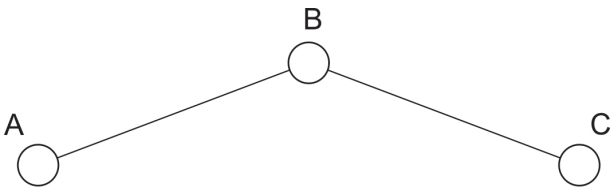

Figure 4: Distant BLE nodes

The basis of our multi-hop communication mechanism is the ability of each node to temporary assume the master role and to acquire the data from not already processed nodes, and relay acquired data to its master node along with its sensor data. Since this procedure is recursively repeated on each node a communication tree is dynamically generated on each data inquiry and can change with each query depending on the nodes availability and their latency.

The multi-hop communication mechanism can be viewed as a two phase protocol:

1. In first phase the communication tree is build. This is started when root node begins to collect available idle nodes. A node in master mode connects to the available idle nodes and sends COLLECT command to claim exclusive access to child node. Child node records connected master node as its parent node in order to prevent connections from other master nodes. This procedure is recursively repeated on each child node: it switches to master mode and start collecting available nodes. First phase is finished when there are no available nodes.
2. In second phase, every non-root node has a parent node which was determined during the first phase. Sensor data are reported back from leaf nodes towards the root node. The report is made in similar fashion as collecting: the node with acquired data from all its children switches back to slave mode and advertises that it has required data. When the parent detects that its child has available data, it connects to the child and initiates data transfer by sending READ command. When the data transfer from all children nodes is finished, the children reinitialize as idle nodes.

In the presented mechanism each master node connects twice to each of its children: first to collect available idle nodes, and then to request acquired data from child node. Since actions of the slave nodes occur when they are connected to a parent node, they are triggered by commands issued by parent node using established data connection. The multi-hop communication mechanism can be viewed as building the communication tree by sending commands towards leaf nodes and gathering sensor data in the opposite direction. The global root node initiates the data acquisition and triggers the generation of the communication network as depicted in Figure 5. Global root node operates as a master node only, thus its functionality can be interpreted as a subset of the sensor node functionality.

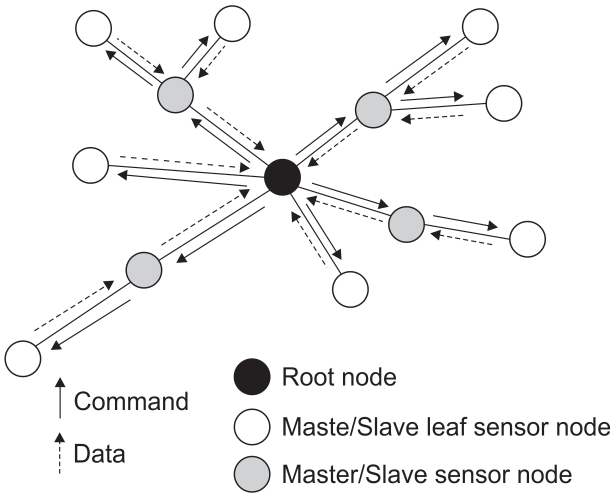

Figure 5: Command and data path in tree topology network

Let us present example with only three nodes to illustrate the concept of our multi-hop mechanism. Node A and node C cannot be directly connected due to long distance or some obstacle, while node B is reachable

by both nodes. Let us assume that the data inquiry is started from node A. The behaviour of the multi-hop mechanism is depicted in Figure 6 and Figure 7 where master nodes are denoted by black shading and slave nodes are white.

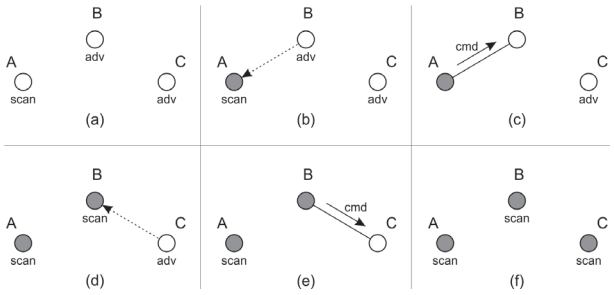

Figure 6: Communication tree formation

Figure 6 describes the communication tree formation of multi-hop communication mechanism:

- Initially all nodes are idle and are advertising their presence (Figure 6a).
- Node A is selected as a root node (inquiry node), node A became a master node and is scanning for neighbour nodes. It detects node B as an idle node (Figure 6b).
- Since node B is idle, node A connects to node B and issues a command to node B to start its own data inquiry (Figure 6c).
- Both node A and node B are scanning, however node C is reachable only by node B. Node B detects node C as an idle node (Figure 6d).
- While node A is still scanning nodes (for the data inquiry results) the node B connects to node C and issues a command to node C to start its own data inquiry (Figure 6e).
- All three nodes are scanning; node A and node B are scanning for data results, while node C is scanning for an idle node (Figure 6f).

The first phase terminates when there is no available idle node. The scanning of the node, which is searching for an idle node, is terminated by a predetermined timeout. The timeout must be long enough to guarantee the detection of an idle node in the vicinity (we used a value of 1 second).

Figure 7 describes the data acquisition of multi-hop communication mechanism:

- After the timeout in node C (Figure 7a), node C reads its sensor data and switches from scanning mode to advertising mode indicating that it has data available.
- Node B is scanning for its child nodes with sensor data and detects that node C have data ready (Figure 7b). Note that while node A is also scanning for nodes with data ready the node C is not its child and would be ignored even if it was detected.
- Node B connects to node C and node C sends its sensor data to node B. Node B adds its sensor readings to the received data from node C (Figure 7c).
- Node B finishes its scanning since it has processed all its children. Then it switches to advertising mode indicating that it has sensor data available. Node A which is scanning for its child nodes with sensor data ready, detects that node B has data ready (Figure 7d).
- Node A connects to node B and node B sends its sensor data to node A. Node A adds its sensor readings to the received data from node B (Figure 7e).
- Since Node A is the root node it report all gathered sensor data and switch from master mode to advertising mode (Figure 7f).

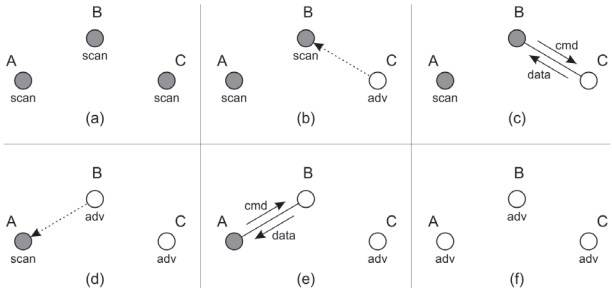

Figure 7: Data acquisition

From the single node point of view the multi-hop data acquisition mechanism is composed of:

- Master mode operation, which is further divided to operations:
  - Collecting all available neighbouring slave nodes and claiming exclusive access to the collected slave nodes. This is achieved by sending COLLECT command to all free slave nodes. Since the master node doesn't know how many available slave nodes are in its vicinity this operation has to be stopped using timeout.
  - Requesting sensor data from child node when the child node has acquired all available sensor data from its descendant nodes. This is achieved by sending READ command.
- Slave mode operation, which consists of following operation:
  - Idle operation: the node advertises that it is available and has no parent node. The node waits for the connection from any master node. After the node is connected to a master node, it accepts only COLLECT command. On

the receipt of this command it records parent node address and advertises parent node address along with its current state

- Serving data operation: the node has all available data from its descendant nodes. It advertises its parent node address and its current state. After the node is connected from the parent node it transfers the acquired data to the parent node. When the sensor data is transferred the node erases parent node address and restarts with the idle operation.

The simplified procedure of the multi-hop mechanism is:

```
while true {
 advertise idle
 while not (cmd = COLLECT) {} // wait for COLLECT command
 record connecting node
 master_mode
 advertise parent and data_ready
 while not (cmd = READ) {}   // wait for READ command
 send acquired data
 erase parent node address
}
```

The master mode operation of the multi-hop mechanism is:

```
start scanning  // switch to master mode
while not timeout {
 if node_available {
  add node to set
  connect
  send COLLECT cmd
 }
}
foreach node in set {
 if node data_ready {
  Connect node
  Send READ cmd
 }
}
```

The multi-hop mechanism was implemented using finite state machine. The states identify the current mode of operation of the node. Initially we used four states: *IDLE*, *COLLECT*, *READ*, and *READY*. States *IDLE* and *READY* states correspond to slave node operation and states *COLLECT* and *READ* correspond to master node operation. However, the resulting connection trees using these states were quite deep. This was because each slave node that entered the COLLECT state on request of a master node immediately started collecting free nodes in its vicinity and thus also competed with its master node. This is undesirable because it results in very deep connection trees with longer data acquisition time. To impose breadth-first generation of the connection tree generation an additional slave state *PREPARE* between the *IDLE* state and *COLLECT* state was introduced. This way the collected slave nodes start collecting remaining nodes after the master node finished the collect operation. Consequently, corresponding master state *TRIGGER* has to be added to control the additional slave state transition.

There are similar problems on the data acquisition part of the mechanism hence the *FREE* state was introduced between *READY* state and *IDLE* state to delay the releasing of slave nodes, and *RELEASE* state between *READ* state and *READY* state in order to control the state transition. The final finite state machine of the multi-hop node is depicted in Figure 8.

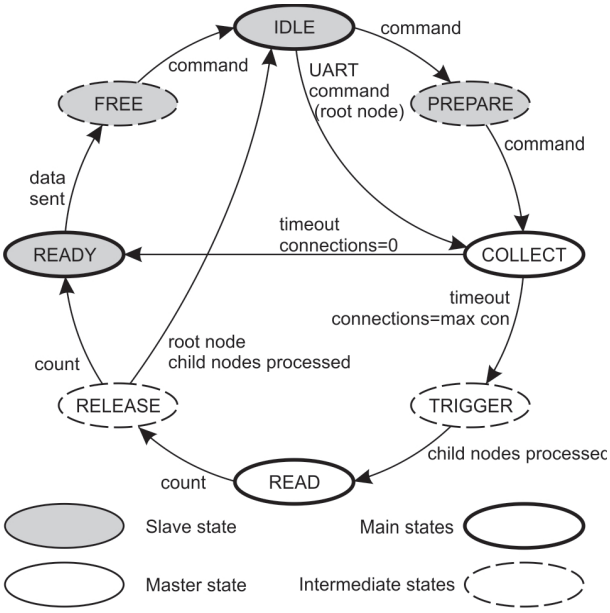

Figure 8: Master and Slave state mechanism

Initially all BLE nodes operate in slave mode and advertise their presence using unique 128bit multi-hop service UUID. Besides the multi-hop service identification master nodes require also additional data: whether the slave node is available and if the node has acquired data from its descendant nodes. While this information could be gathered by establishing the data connection such solution would cause larger delays since a slave node can connect to a single master node and while connected it is inaccessible to other master nodes. Best solution is to advertise current state of the node. Furthermore, to eliminate the unnecessary connections to the nodes, which are already collected by some node the slave node advertises the ID of its parent node. This way the master node can filter out the slave nodes which do not respond to it. Since there are no suitable predetermined advertisement packets in the GATT layer of BLE 4.0 protocol stack a custom advertising packet is used. The final advertising data are shown in Table 1.

Table 1: Advertising packet

ADV packet	Custom		128bit UUID
	Device state	Masters MAC address	
Data Length	1	6	16
Packet length	9		18

The advertising data is composed out of 27 bytes. Each advertising packet occupies one byte for packet type ID, one byte for packet length, and packet data. Device state occupies 1 byte and is a copy of the current state of the device. The master node ID is the MAC address of the master node. The master node ID of the node is initialized to NULL in the *IDLE* state. After first connection from a master node its MAC address is copied into the advertising packet and only connections from this master node is allowed until the node is released. Then the node enters the *IDLE* state and the master node ID is restored to NULL. Consequently, the master node ID of the root node is always NULL.

Generic multi-hop state machine implementation is:

```
1  while true {
2    switch (state) {
3     case IDLE:       // slave mode
4      if (cmd=PREPARE) {
5       parent = master_node
6       state  = PREPARE
7       advertise(parent,state)
8      }
9     case PREPARE:    // slave mode
10     if (cmd = COLLECT && master_mode = parent) {
11      state  = COLLECT
12      start_scan()  // switch to master mode
13     }
14    case COLLECT:    // master mode
15     if timeout state = TRIGGER
16     else if available_idle(node) {
17      connect(node)
18      send_cmd(PREPARE)
19      add_to_children_set(node)
20     }
21    case TRIGGER:    // master mode
22     if children_set_processed() state = READ
23     else if available_prepare(node, my_address) {
24      connect(node)
25      send_cmd(COLLECT)
26     }
27    case READ:       // master mode
28     if children_set_processed() state = RELEASE
29     else if available_ready(node, my_address) {
30      connect(node)
31      data_request_cmd(READ)
32     }
33    case RELEASE:    // master mode
34     if children_set_processed() {
35      state = READ
36      advertise(parent,state)
37     }
38     else if available_free(node) {
39      connect(node)
40      send_cmd(RELEASE)
41     }
42    case READY:      // slave mode
43     if (cmd = READ && master_mode = parent) {
44      send_sensor_data()
45      state = FREE
46      advertise(parent,state)
47     }
48    case FREE:       // slave mode
49     if (cmd = RELEASE && master_mode = parent) {
50      clear parent
51      state = IDLE
52      advertise(parent,state)
53     }
54   }
55 }
```

The states of the multi-hop mechanism are:

- *IDLE* state: the node is in slave mode but it has no parent node therefore it is available. It operates as a slave and advertises its state. On connection from a parent node using the PREPARE command the state changes to *PREPARE* state.
- *PREPARE* state: the node is in a slave mode but it is reserved by the parent node. It advertises its state and its parent node. It accepts the connections only from its parent node and the only viable action is to change to *COLLECT* state by COLLECT command.
- *COLLECT* state: the node is in master mode. In the master mode the advertisement is stopped. It scans the neighbouring nodes, collects available nodes, records them and sends them TRIGGER command for an exclusive access. After reasonable timeout, the collecting process is stopped. The node then switches to *TRIGGER* state if there are some collected nodes, otherwise the node switches to *READY* state.
- *TRIGGER* state: the node is in the master mode. The collected nodes are triggered to a *COLLECT* master state in order to acquire data from distant nodes. The node scans the neighbouring nodes and when a slave node, advertising that it was collected by this node, is found, *TRIGGER* command is given to this slave node. After all collected slave nodes are processed, the node switches to *READ* state.
- *READ* state: the node is in the master mode. It scans the neighbouring nodes and when a slave node, advertising that it has data ready for this node, the read process is triggered using *READ* command. After all collected slave nodes are processed, the node switches to *RELEASE* state.
- *RELEASE* state: the node is in the master mode. It scans the neighbouring nodes and when a slave node, advertising that it could be freed is detect-

ed, *RELEASE* command is given to free the collected slave node. After all collected slave nodes are processed, the node switches to *READY* state.
- *READY* state: the node is in the slave mode. When the data connection from the parent node is established the acquired data along with the local node sensor data are sent to the parent node. After the data transfer is completed the node switches to FREE state.
- *FREE* state: the node is in slave mode. It advertises that it could be freed. On the receipt of *RELEASE* command from the parent node it re-initializes all data structures and switches to *IDLE* state.

Initially all BLE nodes operate in slave mode. To initiate the data acquisition on a selected BLE node a command is issued on its UART peripheral interface to assume the role of the root node. At this point the root node starts collecting neighbouring nodes, acquires their data, and reports the acquired data over the UART peripheral interface.

5 Implementation and results

For testing and evaluation of the multi-hop communication mechanism a custom measurement board was developed. Peripheral hardware consists of power supply, USB and UART interface, LM75B temperature sensor [8], and a Bluegiga BLE113 breakout board [7].

Table 2: BLE113 specifications

Device	Bluegiga BLE113
Supply voltage	2V – 3.6V
Peripheral interface	UART, SPI, I2C,PWM,GPIO, ADC
TX consumption	18.2mA
RX consumption	14.3mA
Sleep mode consumption	0.4uA
TX power	0dBm to – 23dBm
RX sensitivity	-93dBm
SoC	CC2541 chip: - 8051 CPU, - 32MHz clock, - 128kB or 256kB Flash - 8kB SRAM
Smart stack	GAP, GATT, L2CAP and SM Bluetooth smart profiles
Max connections in master mode	8
Throughput	100kbps +

The main specifications of BLE113 module are presented in Table 2. The module is based on a CC2541 SoC from Texas Instruments with integrated 8051 CPU, Bluetooth radio and software stack [12]. Module offers a wide range of peripheral interface on 17 configurable I/O ports, two configurable I/O ports with 20 mA driving capability and two ports that can be used as digital I/O or I^2C communication channel. BLE113 module configurable ports offer a broad assortment of peripheral functionality:
- UART and SPI communication,
- three timers that each can offer timer, counter or PWM functionality,
- up to 12bits of resolution ADC converter

BLE113 is capable of managing 8 slave devices in master mode with over 100kbps throughput. Module is mounted on the BLE113 breakout board which is installed on a peripheral hardware board with temperature sensor. The communication between BLE113 module and temperature sensor is implemented with I^2C interface.

Software was written in BGScript language [13], which is event-driven BASIC-like application scripting language. Each event handling subroutine can consist out of numerous instructions and each instruction can be executed in 1-2ms [13]. Since the BLE113 module incorporates 8051 MCU with several GPIO ports as well as some general purpose communication protocols (e.g. I^2C, SPIO) we were able to develop a fully standalone BLE device without the external CPU and/or additional memory. BGScript incorporates additional APIs for managing Bluetooth connections and various hardware interfaces. In this regard I^2C data transfers for temperature sensor readings, UART for debugging purposes, and GPIO for external triggering were used.

Although the BGScript provides most common programming structures and relatively rich APIs it has several limitations. The main limitations are the limited amount of available RAM used for variables, the limited amount of available non-volatile memory for program storage and most notably the limited amount of program stack. The program stack is limited to at most 100 bytes which does not allow deep function nesting nor moderate size function parameters.

For the evaluation process seven BLE devices were used from which one was used as root device and six were used as child nodes. The collected data from each child node was a temperature stored as a short integer occupying two bytes.

Total amount of program code was around 60KB which is approximately 23% of available non-volatile memory [6]. The program code was the same on all nodes in the network. To initiate the data collection through

the network one node was connected to the computer. This node became a root node once it received the command to start the data collection over the USB/UART communication port. Detailed mechanism implementation in BGScript language for our measurement board is presented in technical report [14].

In the first experiment set we tested completely connected wireless sensor network where each pair of nodes are connectable. The nodes were placed in the same room at a random distance of a few meters from each other. Using such placement, we conducted two sets of tests. In the first test set the maximum number of connected slave nodes were limited to two. This way we forced the master nodes to connect to at most two child nodes which resulted in a binary tree network topology. In the second test set we released the maximum connection limitation. Since all nodes were relatively close, they formed a star topology. Both test sets consist of 2000 temperature data acquisitions and were collected automatically using python scripts on a PC computer. There was a pause of few seconds between each data acquisition to mitigate errors that might arise from environment disturbances.

In the first test set, when the number of child nodes was limited to two, the formed networks were binary tree networks with maximal depth of 3 and various fan-out shapes. In the test the isomorphic binary trees were collected together. Representations of the most frequent isomorphic network trees in the first test set are shown in Figure 9 whereas the frequency of the isomorphic network formation is presented in Table 3. The most common binary tree network was a balanced tree shown in Figure 9d. The data collecting time in balanced tree network varied from 13 to 16 seconds.

Table 3: Frequency of binary tree network formation

Binary tree network	9a	9b	9c	9d
Occurrences	33	44	413	1205

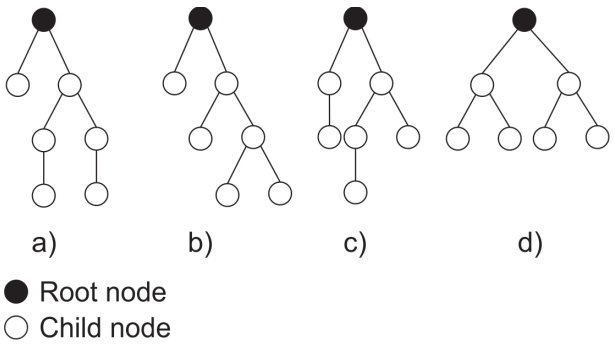

Figure 9: Binary tree networks

In the second test set performed without connection limitation, nodes formed a star topology structure where all child are nodes connected directly to root node. With this mode of operation, no multi-hop data transfer was conducted. The data collecting time varied from 20 to 38 seconds.

During 2000 data acquisition requests a total of 35 different tree network topologies were created.

In both test sets there were some cases where not all nodes were connected. This can be attributed to the environment disturbances when some nodes become inaccessible. Since we implemented only basic error handling in the multi-hop mechanism such errors might span over few consecutive tests.

Finally, we tested the mechanism in real-life environment. In the real-life environment the sensor nodes do not form a complete graph and if there is a limitation on the number of child nodes some nodes may become inaccessible. Therefore in the real-life environment the limitation on the number of the child node must be omitted. In our test the sensor nodes were placed throughout the building where they formed a sensor network shown in Figure 10.

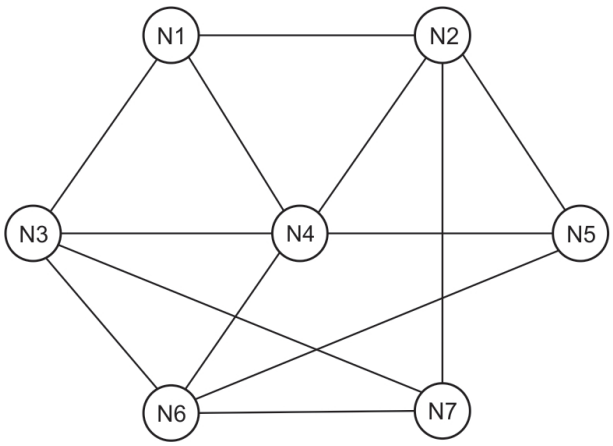

Figure 10: Sensor network connection graph

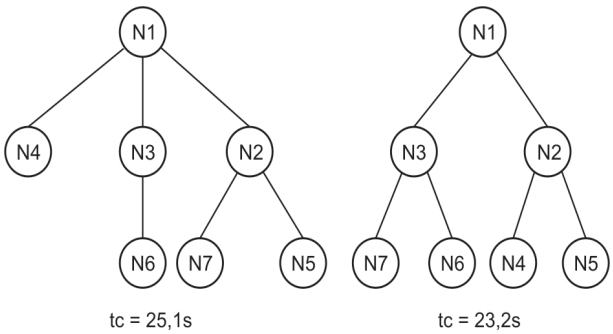

Figure 11: Tree networks with N1 as the root node

We conducted two sets of tests. In the first test set the N1 sensor node was chosen as a root node. In the Figure 11 two typical tree networks are depicted. The maximal depth of connection trees was 3. The data collecting time for these connection trees were 25,1 and 23,2 seconds respectively.

In the second test set N7 was chosen as the root node. In the Figure 12 two examples of tree networks are shown. The data collecting time for these connection trees were 27,2 and 25,5 seconds respectively.

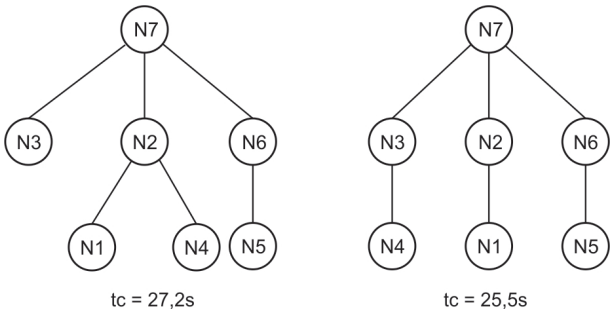

Figure 12: Tree network with N7 as the root node

6 Conclusions

As Bluetooth Low Energy technology continues to gain its use in wireless sensor network the demand for viable data transfer mechanisms over wireless sensor network also increases.

In this paper a multi-hop communication mechanism for data acquisition in Bluetooth Low Energy 4.0 ad-hoc wireless sensor network is presented. The goal was to extend the range of BLE wireless sensor network by relaying data over a series of identical sensor nodes in the wireless network.

Initially, the mechanism was coded using numerous nested functions and medium-size function parameters that increased program stack consumption. That led to program stack overflow and subsequently to unpredictable behaviour of BLE113 module such as device reboot or variable corruption. The code was later flattened to eliminate program stack overflows.

We demonstrated that our multi-hop data acquisition mechanism can be used for a sensor data collection in tree topology networks. Although the sensor data collection can take a noticeable amount of time the mechanism can be nonetheless used for relatively slow processes such as temperature measurements.

In future we will improve the reliability of the mechanism and include a time-to-live mechanism that will improve robustness and allow the use of mechanism in more dynamic environments.

7 Acknowledgments

The authors acknowledge the financial support from the Slovenian Research Agency (research core funding No. P2-0098).

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Arrived: 19. 12. 2017
Accepted: 03. 05. 2018

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 48, No. 2(2018), 97 – 113

Lossy and Lossless Inductance Simulators and Universal Filters Employing a New Versatile Active Block

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Abstract: In this paper six new implementations for realizing lossy and lossless active inductors are presented. The new topologies are obtained using a newly formulated active block namely, the extra X current conveyor transconductance amplifier (EXCCTA). The designed grounded inductor simulators (GIS) require only three grounded passive elements for implementation which is desirable for integrated circuit fabrication. Moreover, the inductance simulators are electronically tunable and free from matching requirements. Additionally, two structures of universal filters are also proposed. The voltage mode (VM) filter is multi input single output (MISO) structure and uses canonical number of passive components. The current mode (CM) filter is a single input multi output (SIMO) structure with grounded passive elements. The filter structures can realize all five standard filter responses without any matching conditions and have features of low/ high output impedance, low active and passive sensitivities, tunability, independent control of pole frequency and quality factor. The effect of non-idealities on the inductor and filter topologies are also analyzed. The simulations are performed in 0.18µm parameters from TSMC in Spice to validate the theoretical predictions. Experimental results using AD844 and LM13700 integrated circuits (ICs) for the proposed inductor and filter are also provided to further ascertain the feasibility of the proposed solutions.

Keywords: active inductor; current mode; current conveyor; filter; tunability

Izgubni in brezizgubni induktivni simulator ter univerzalen filter z z novim prilagodljivim aktivnim blokom

Izvleček: Članek predstavlja šest primerov realizacije izgubnih in brez izgubnih aktivnih dušilk. Nove topologije uporabljajo nov aktivni blok; ekstra X tokovni transkonduktančni ojačevalnik (EXCCTA). Načrtani ozemljeni induktivni simulatorji (GIS) zahtevajo le tri ozemljene pasivne elemente in so elektronsko nastavljivi ter neodvisni od zahtev ujemanja. Dodatno sta predlagani dve strukturi univerzalnega filtra. Več vhodni in eno izhodni filter v napetostnem načinu uporablja standardno število pasivnih elementov. Tokovni filter je eno vhodni in več izhodni z ozemljenimi elementi. Filtri lahko realizirajo vseh pet standardnih odzivov brez prilagajanj. Imajo nizko/visoko izhodno impedanco, nizko aktivno in pasivno občutljivost, nastavljivost, neodvisno kontrolo frekvence in faktorja kvalitete. Simulacije so izvedene v 0.18 µm tehnologiji iz TSMC in SPICE za validacijo teoretičnih predvidevanj. Eksperimentalni rezultati so pridobljeni s uporabo AD844 in LM13700 integriranih vezij.

Ključne besede: aktivna dušilka; tokovni način; tokovni ojačevalnik; filter; nastavljivost

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1 Introduction

The physical spiral inductors suffer from low realizable inductance value of the order of 1nH [1, 2], low quality factor, higher chip area requirement, excessive losses and susceptibility to process variations [1]. These drawbacks make them unsuitable for integrated circuit implementation. Since inductors are inevitable components given their broad spectrum of applications in active filters, parasitic cancellation, oscillators, radio frequency (RF) systems etc. [2]. The active simulation of inductors where active devices are employed instead of spiral inductors to emulated the behavior of passive inductors has become popular [1-3]. Analog filters are an integral part of almost every electronic system and so their synthesis and development remains an ever evolving field. Among various filter structures universal filters (UFs) are the most versatile as all the standard filter functions can be derived from them[6-9]. They serve as standalone solution to many filtering needs. The UFs find applications in phase locked loop FM stereo demodulator, telephone decoder, speech processing etc.[7-8]. The current mode active elements are the best choice for inductor and filter synthesis, owning to their large dynamic range, great linearity, wide bandwidth, higher slew rate and excellent low voltage performance compared to their voltage mode counterparts [6-7]. Numerous current mode active blocks have been employed for inductance simulation and filter design like second generation current conveyor (CCII) [4], differential voltage current conveyor (DVCCII) [2], dual X current conveyor (DXCCII) [22], current conveyor transconductance amplifier (CCTA) [28], differential current conveyor (DCCII) [11], differential difference current conveyor (DDCC) [1], fully differential current conveyor (FDCCII) [34], voltage differencing current conveyor (VDCC) [25], current feedback operational amplifier (CFOA) [13], modified current feedback operational amplifier (MCFOA) [18], inverting current feedback operational amplifier (CFOA-) [5], current differencing transconductance amplifier (CDTA) [37] etc.

The GIS can be categorized based on many criteria like number of active devices used, passive component count, lossy/lossless type inductance realization, use of grounded passive elements, feature of inbuilt tunability, capability of active element realization using the off the shelf integrated circuits (ICs) like AD844 etc. The GIS presented in [4, 12-13] require more than one active element for inductance simulation. The GIS implementations presented in [4, 12-13, 15, 21, 23] require more than three passive elements. Although in current fabrication technology it is feasible to implement floating capacitor but use of grounded capacitor has inherent advantages in terms noise cancelation, chip area and parasitic reduction. The GIS implementations in [5, 10, 12, 14-17, 19, 21-24] makes use of one or more floating capacitors. Tunability is one of the major design requirements in today's mixed mode systems. The GIS circuits in [1, 4-5, 11-24] did not have inbuilt tuning capability. A thorough comparison of the exemplary inductance topologies available in the literature with the proposed lossy/lossless GIS topologies is given in Table 1. The literature survey reveals that the draw backs of the majority of the presented inductor simulators are (i) no provision for on chip tunability (ii) use of more than one active element (iii) use of floating capacitor (iv) excessive use of passive elements (v) passive components matching requirnment.

In this research a new active block the extra X current conveyor transconductance amplifier (EXCCTA) is utilized in designing six topologies of lossy/lossless inductance simulators. All the designed GIS employ only a single active element and two/three grounded passive elements for implementation. No matching is required for implementation and inductance can be easily tuned via bias current of the transconductor. Further more, two minimum component VM and CM mode universal filters are proposed. The filters structures are characterized by following attributes (i) use of minimum number of active blocks and passive components (ii) inbuilt tunability (iii) use of grounded passive elements (iv) provision for independent control of pole frequency and quality factor (v) avalibility of output at low impedance in case of VM filter and high impedance in CM filter. The simulation are performed using 0.18µm parameters from TSMC in Spice to validate the theoretical findings. Additionally, an experimental study of pure inductor and VM SIMO filter is conducted using AD844 and LM13700 ICs. The measured results are compared with the ideal ones.

2 Extra X current conveyor transconductance amplifier (EXCCTA)

The proposed Extra X current conveyor transconductance amplifier (EXCCTA) is functionally a connection of extra x current conveyor (EXCCII) [26] and operational transconductance amplifier (OTA) [30]. The new block carries features of CCII and tunable OTA in a single integrated circuit structure. The Voltage current characteristics of the developed EXCCTA are given in matrix Equation1 and the block diagram is presented in Fig. 1. The block is found to be suitable for implementing minimum component filters and inductor simulators as it provides two independent current input X terminals and an inherent tunable structure.

Table 1: Comparison of exemplary active inductors with the proposed ones

Reference	No. of Active Devices Used	No. of Passive Elements	Capacitor Floating	Matching Condition	Inbuilt Tunability
[1] Fig. 5	MDO-DDCC (1)	3	No	Yes	No
[4]	CCII (3)	4	No	No	No
[5]	CFOA – (1)	3	Yes	No	No
[10]	VDBA (1)	2	Yes	No	Yes
[11]	DCCII (1)	3	No	Yes	No
[12]	OTRA (2)	5	Yes	Yes	No
[13]	CFOA (2)	4	No	Yes	No
[14]	DCCII (1)	3	Yes	No	No
[15]	OTRA (1)	4	Yes	No	No
[16]	MICCII (1)	3	Yes	Yes	No
[17]	GVCCIII (1)	3	Yes	Yes	No
[18]	MCFOA (1)	3	No	No	No
[19]	CFOA (1)	3	Yes	No	No
[20]	CCII (1)+Current Follower (1)	3	No	No	No
[21]	PFTN (1)	5	Yes	Yes	No
[22]	DXCCII (1)	3	Yes	Yes	No
[23]	OTRA (1)+Voltage Buffer (1)	4	Yes	Yes	No
[24]	CFOA (1)	3	Yes	No	No
Fig. 3 Proposed GIS-(1-2, 4-6)	EXCCTA (1)	3	No	No	Yes
Fig. 3 Proposed GIS-3	EXCCTA (1)	2	No	No	Yes

$$\begin{bmatrix} I_Y \\ V_{XP} \\ V_{XN} \\ I_{ZP+} \\ I_{ZP-} \\ I_{ZN+} \\ I_{ZN-} \\ I_{0+} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & g_m & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{XP} \\ I_{XN} \\ V_{ZP+} \\ V_{ZP-} \\ V_{ZN+} \\ V_{ZN-} \\ V_O \end{bmatrix} \quad (1)$$

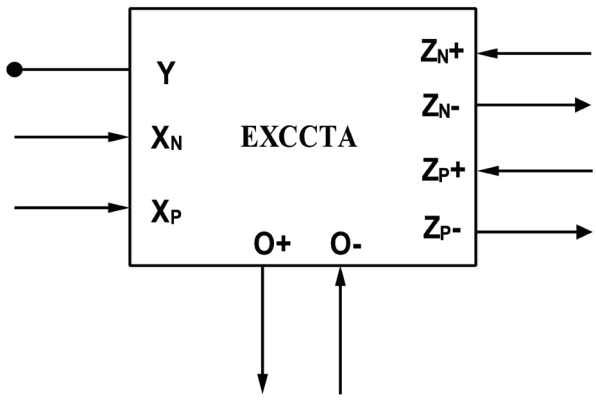


Figure 1: Block diagram of EXCCTA

The CMOS implementation of EXCCTA is presented in Fig. 2. It is a 9 terminal active element. The first stage consists of EXCCII transistors (M1-M28). The voltage applied at Y node appears at XP and XN nodes. The current input at X_p node is transferred to nodes Z_{p+} and Z_{p-}. In the same way the input current from X_N node is transferred to Z_{N+} and Z_{N-}. The current following in Z_N and Z_p terminals are independent of each other. The class AB output stage is selected for the implementation as it is suitable for low voltage operation [6]. The second stage is composed of OTA. The transconductance is realized using transistors (M29-M40).The output current of the trans-conductor depends on the voltage Z_{p+}. Assuming saturation region operation for all transistors and equal W/L ratio for transistors M29 and M30 the output current I_o of the OTA is given by Equation 2.

$$I_O = g_{mi}\left(V_{ZP+}\right) = \left(\sqrt{2I_{Bias}K_i}\right)\left(V_{ZP+}\right) \quad (2)$$

Where, the transconductance parameter $K_i = \mu C_{0x} W/2L$, (i=29, 30) W is the effective channel width, L is the effective length of the channel, C_{ox} is the gate oxide capacitance per unit area and μ is the carrier mobility. It is evident from (2) that the transconductance can be tuned by the bias current thus imparting tunability to the structure.

The most critical parameters of the EXCCTA can be computed by following the analysis procedure given in

[6]. The voltage transfer ratio between Y and X_p node can be derived as given in Equation 3.

$$\alpha_P = \frac{V_{XP}}{V_Y} = \frac{\frac{r_{09}r_{014}}{r_{09}+r_{014}}\left(g_{m9}+g_{m14}\right)\frac{r_{0p}}{2}g_{m4}}{\frac{r_{09}r_{014}}{r_{09}+r_{014}}\left(g_{m9}+g_{m14}\right)\frac{r_{0p}}{2}g_{m3}+1} \cong \frac{g_{m4}}{g_{m3}} \quad (3)$$

Where $r_{0p} = r_{03}//r_{07}$, r_0 is the output resistance of the MOS transistor and g_m is the transconductance of the MOS transistor. In the similar way the voltage transfer between Y and X_N can be obtained as given below. The current transfer ratios β_p and β_N depend on the load connected at X and Z terminals. This is a slight draw back but if the value of the load connected is less than MOS transistor resistance than an accurate transfer is achieved. The current transfer ratios are derived as given in Equation 5-6.

$$\alpha_N = \frac{V_{XP}}{V_Y} \cong \frac{g_{m1}}{g_{m2}} \quad (4)$$

$$\beta_P = \frac{I_{ZP}}{I_{XP}} = \frac{\frac{\frac{r_{010}r_{015}}{r_{010}+r_{015}}(g_{m10}+g_{m15})}{\frac{r_{010}r_{015}}{r_{010}+r_{015}}(g_{m10}+g_{m15})+R_{ZLOAD}}}{\frac{\frac{r_{09}r_{014}}{r_{09}+r_{014}}(g_{m9}+g_{m14})}{\frac{r_{09}r_{014}}{r_{09}+r_{014}}\left(g_{m9}+g_{m14}\right)+R_{XLOAD}}} \cong \frac{g_{m10}+g_{m15}}{g_{m9}+g_{m14}} \quad (5)$$

$$\beta_N = \frac{I_{ZN}}{I_{XN}} \cong \frac{g_{m20}+g_{m24}}{g_{m19}+g_{m28}} \quad (6)$$

The X terminal resistance of X_N and X_p terminal is calculated as given in Equations 7-8.

$$R_{XP} = \frac{1}{\frac{r_{09}r_{014}}{r_{09}+r_{014}}+\left(g_{m9}+g_{m14}\right)\frac{r_{0p}}{2}g_{m4}} \cong \quad (7)$$

$$\cong \frac{2}{r_{0p}g_{m4}\left(g_{m9}+g_{m14}\right)}$$

$$R_{XN} \cong \frac{2}{r_{0n}g_{m1}\left(g_{m19}+g_{m28}\right)} \quad (8)$$

Where $r_{0p} = r_{03}//r_{07}$ and Where $r_{0n} = r_{02}//r_{06}$

The Z and O nodes impedances are found to be high given by parallel output resistance of MOS transistors.

$$R_{ZP} = \frac{r_{010}r_{015}}{r_{010}+r_{015}} \quad (9)$$

$$R_{ZN} = \frac{r_{020}r_{024}}{r_{020}+r_{024}} \quad (10)$$

$$R_{Z0+} = \frac{r_{033}r_{039}}{r_{033}+r_{039}} \quad (11)$$

The extra transistor count should not be considered a disadvantage since the unused Z terminal can be removed reducing the transistor count.

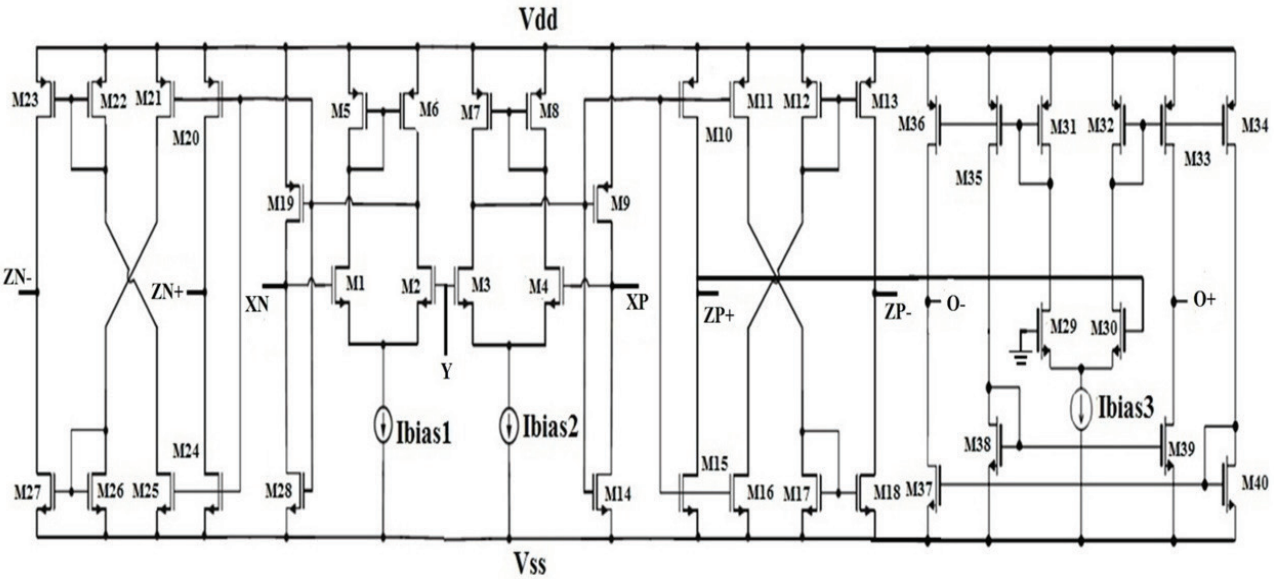


Figure 2: CMOS Implementation of EXCCTA

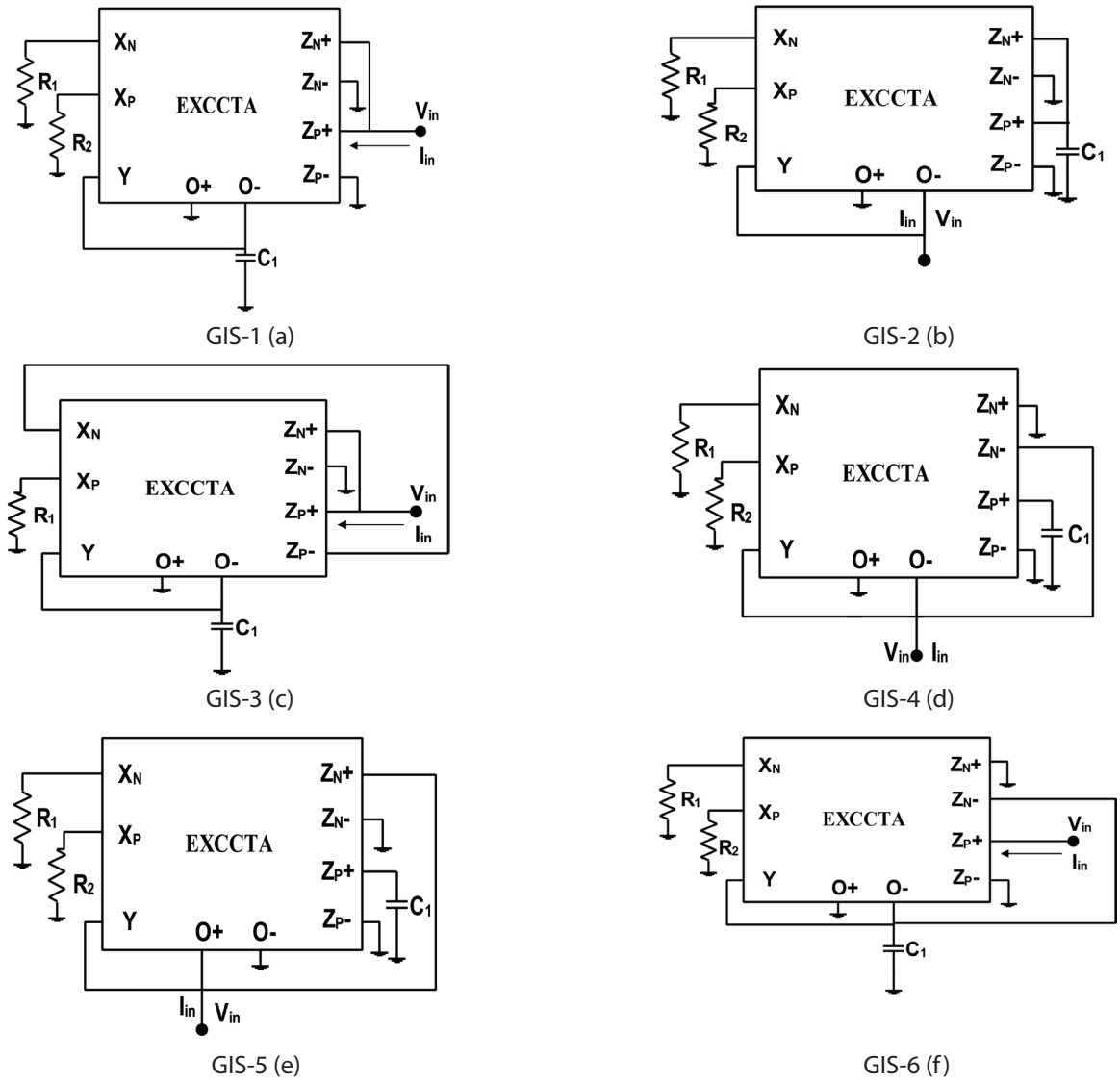


Figure 3: The proposed lossless and Lossy inductor simulators

Table 2: The impedance relations of the proposed active inductors

Simulator	Impedance Realized	Inductance (L_{eq})	Equivalent Resistance (R_{eq})	Type	Tunability	Matching Requirement
GIS-1	L_{eq}	$\frac{SC_1R_1R_2}{g_m(R_1+R_2)}$	-	Pure	Yes	No
GIS-2	L_{eq}	$\frac{SC_1R_1R_2}{g_m(R_1+R_2)}$	-	Pure	Yes	No
GIS-3	L_{eq}	$\frac{SC_1R_1}{2g_m}$	-	Pure	Yes	No
GIS-4	$\frac{1}{L_{eq}}+\frac{1}{R_{eq}}$	$\frac{SC_1R_2}{g_m}$	R_1	L in parallel with R	Yes	No
GIS-5	$-\frac{1}{L_{eq}}-\frac{1}{R_{eq}}$	$-\frac{SC_1R_2}{g_m}$	$-R_1$	-L in parallel with -R	Yes	No
GIS-6	$L_{eq}+R_{eq}$	$\frac{SC_1R_2}{g_m}$	$\frac{R_2}{R_1g_m}$	L in series with R	Yes	No

3 The proposed inductor simulators and universal filters

The proposed inductor simulators using a single EXCCTA and grounded passive elements are shown in Fig. 3(a-f). A simple analysis of the circuits reveals that the GIS-1 to GIS-3 realize pure inductance. The GIS-4 and GIS-5 implements lossy parallel RL inductors. It is noteworthy that the value of the parallel resistor in GIS-4/5 can be set using resistor R_1 independent of the inductance value that is set by R_2 and g_m which is an advantage. Finally, the GIS-6 realizes lossy series RL inductor. The series resistance in GIS-6 can be altered by changing R_1 without affecting the inductance.

All the presented inductor simulators use only grounded passive elements which is advantageous for integrated circuit implementation. The use of grounded capacitor saves chip area and also minimizes noise effects. Furthermore, all the simulators are free from components matching constraints and tunable via bias current of the OTA. The impedance relations of the inductors are given in Table 2.

Next, the proposed VM universal filter is presented in Fig. 4. The filter structure is obtained by modifying the proposed series inductor GIS-6. The SIMO filter uses canonical number of passive components and can realize low pass (LP), high pass (HP), band pass (BP), notch pass (NP) and all pass (AP) responses. Among the two capacitors one is always grounded which is an advantage. The features of the filter includes use of single active block, low output impedance, tunability and provision for independent control of quality factor and pole frequency. The transfer function, expression of -3dB cutoff frequency, quality factor and bandwidth of the filter are given in Equations 12-14. The output can be tapped from Y terminal or low impedance X_N terminal. The combination of filter input modes and applied input voltages for realizing all the five filter responses is summarized in Table 3.

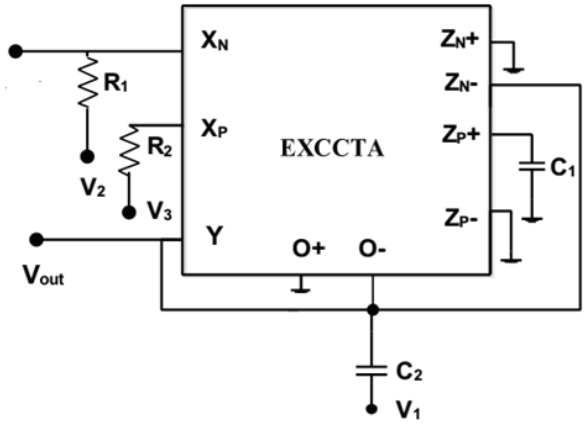


Figure 4: The proposed VM mode MISO filter

$$V_{out} = \frac{\frac{S^2C_1C_2R_2}{g_m}V_1 + \frac{SC_2R_2}{g_mR_1}V_2 + V_3}{\frac{S^2C_1C_2R_2}{g_m} + S\frac{C_2R_2}{g_mR_1} + 1} \quad (12)$$

$$\omega_o = \sqrt{\frac{g_m}{C_1C_2R_2}} \quad (13)$$

$$Q = R_1\sqrt{\frac{C_1g_m}{C_2R_2}} \quad (14)$$

Table 3: The activation sequence of the filter

Response	Inputs		
	V_1	V_2	V_3
LP	0	0	1
HP	1	0	0
BP	0	1	0
NP	1	0	1
AP	1	-1	1

The MISO CM filter is shown in Fig. 5. The filter employs three grounded passive elements and can realize all LP, BP and HP responses simultaneously. The AP response can be obtained by summing the HP, BP and LP responses. All the responses are available at high impedance nodes except the HP response which is available through the capacitor . The HP current can be sensed using a simple current follower. The features of the filter includes use of single active element, grounded passive elements and tunability. The transfer functions for five filter responses are given in Equations 15(a)-15(e).

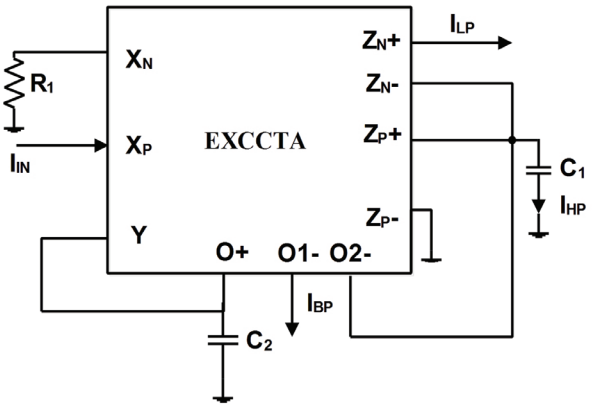


Figure 5: The proposed CM SIMO filter

$$\frac{I_{LP}}{I_{in}} = \frac{-1}{\frac{S^2C_1C_2R_1}{g_m} + SC_2R_1 + 1} \quad (15a)$$

$$\frac{I_{HP}}{I_{in}} = \frac{-\frac{S^2C_1C_2R_1}{g_m}}{\frac{S^2C_1C_2R_1}{g_m} + SC_2R_1 + 1} \quad (15b)$$

$$\frac{I_{BP}}{I_{in}} = \frac{SC_2R_1}{\frac{S^2C_1C_2R_1}{g_m} + SC_2R_1 + 1} \quad (15c)$$

$$\frac{I_{NP}}{I_{in}} = \frac{-1-\frac{S^2C_1C_2R_1}{g_m}}{\frac{S^2C_1C_2R_1}{g_m} + SC_2R_1 + 1} \quad (15d)$$

$$\frac{I_{AP}}{I_{in}} = \frac{-1-\frac{S^2C_1C_2R_1}{g_m} + SC_2R_1}{\frac{S^2C_1C_2R_1}{g_m} + SC_2R_1 + 1} \quad (15e)$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{g_m}{C_1C_2R_1}} \quad (16)$$

$$Q = \sqrt{\frac{C_1}{g_mC_2R_1}} \quad (17)$$

4 Non-Ideal analysis

In this section the Non-idealities of the EXCCTA are considered and their influence on the proposed inductors and filter circuits is analyzed. A simplified non-ideal model of EXCCTA is presented in Fig. 6 for analysis. The most important aspects contributing to the deviations in frequency performance are the non-ideal frequency dependent current and voltage transfer gains, $\alpha_i(s)$ and $\beta_i(s)$ respectively, where $\alpha_i(s) = \alpha_{0i}/(1 + s/\omega_{\alpha i})$ and $\beta_i(s) = \beta_{0i}/(1 + s/\omega_{\beta i})$. Ideally, $\alpha_{0i} = \beta_{0i} = 1$ and $\omega_{\alpha i} = \omega_{\beta i} = \infty$. Another important performance parameter is the associated parasitics at the X nodes which can be quantified as $Z_{XP} = Z_{XN} = R_{X(N,P)} + sL_{X(N,P)}$. The parasitic resistance and capacitance associated with the Y and Z nodes are R_{ZP}, R_{ZN} and R_Y. While the associated capacitances are C_{ZP}, C_{ZN} and C_Y. There ideal values being equal to zero.The γ represents the transconductance transfer inaccuracy of the OTA, while R_o and C_o are parasitics at the OTA output. If the effect of the non-ideal gains is considered the V-I relations of the EXCCTA will be modified to $I_Y = 0$, $V_{XP} = \beta_p(s)V_Y$, $V_{XN} = \beta_N(s)V_Y$, $I_{ZP+} = \alpha_p(s)I_{XP}$, $I_{ZP-} = \alpha_p'(s)I_{XP}$, $I_{ZN+} = \alpha_N(s)I_{XN}$, $I_{ZN-} = \alpha_N'(s)I_{XN}$, $I_{0+} = \gamma g_m V_{ZP+}$, $I_{0-} = \gamma' g_m V_{ZP+}$.

The modified expressions of inductance L_{eq} of the active inductor simulators taking into account the non-ideal current and voltage transfer gains of the EXCCTA is given in Table 4.

Table 4: Modified inductance L_{eq} of the active inductor simulators for non-ideal case

GIS-1	$L_{eq} = \frac{SC_1R_1R_2}{\gamma' g_m(\alpha_P\beta_PR_1 + \alpha_N\beta_NR_2)}$
GIS-2	$L_{eq} = \frac{SC_1R_1R_2}{\gamma' g_m(\alpha_P\beta_PR_1 + \alpha_N\beta_NR_2)}$
GIS-3	$L_{eq} = \frac{SC_1R_1}{\gamma' g_m(\alpha_P\beta_P + \alpha_N\beta_N)}$
GIS-4	$L_{eq} = \frac{\gamma' g_m\alpha_P\beta_P}{SC_1R_2} + \frac{\alpha_N'\beta_N}{R_1}$
GIS-5	$L_{eq} = \frac{-\gamma g_m\alpha_P\beta_P}{SC_1R_2} - \frac{\alpha_N\beta_N}{R_1}$
GIS-6	$L_{eq} = \frac{SC_1R_2}{\alpha_P\beta_P\gamma' g_m} + \frac{\alpha_N\beta_NR_2}{\gamma' g_mR_1}$

The expressions of transfer function, pole frequency and quality factor including the non-ideal gains for the VM and CM filters are presented in Equations 18-23, respectively.

$$V_{out} = \frac{\frac{S^2C_1C_2R_2}{\gamma g_m}V_1 + \frac{\alpha_N SC_2R_2}{\gamma g_mR_1}V_2 + \alpha_P\gamma V_3}{\frac{S^2C_1C_2R_2}{\gamma g_m} + S\frac{\alpha_N\beta_NC_2R_2}{\gamma g_mR_1} + \alpha_P\beta_P} \quad (18)$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{g_m\alpha_P\beta_P}{C_1C_2R_2}} \quad (19)$$

$$Q = R_1\alpha_N\beta_N\sqrt{\frac{\alpha_P\beta_P\gamma g_mC_1}{C_2R_2}} \quad (20)$$

$$\frac{I_{LP}}{I_{in}} = \frac{-\alpha_N\beta_N}{\frac{S^2C_1C_2R_1}{\gamma g_m} + SC_2R_1 + \alpha_N'\beta_N} \quad (21a)$$

$$\frac{I_{HP}}{I_{in}} = \frac{-\frac{S^2C_1C_2R_1}{\gamma g_m}}{\frac{S^2C_1C_2R_1}{\gamma g_m} + SC_2R_1 + \alpha_N'\beta_N} \quad (21b)$$

$$\frac{I_{BP}}{I_{in}} = \frac{\frac{\gamma'}{\gamma S C_2 R_1}}{\frac{S^2 C_1 C_2 R_1}{\gamma g_m} + S C_2 R_1 + \alpha_N' \beta_N} \quad (21c)$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{\gamma g_m \alpha_N' \beta_N}{C_1 C_2 R_1}} \quad (22)$$

$$Q = \sqrt{\frac{\alpha_N' \beta_N C_1}{g_m \gamma C_2 R_1}} \quad (23)$$

The sensitivity analysis of both the VM and CM universal filters is also carried out. The Equations 24-26 give the active and passive sensitivities of the VM filter and Equations 27-28 present the sensitivities of the CM filter.

$$S_{\alpha_P}^{\omega} = S_{\beta_P}^{\omega} = S_{\gamma}^{\omega} = S_{g_m}^{\omega} = -S_{C_1}^{\omega} = -S_{C_2}^{\omega} = -S_{R_2}^{\omega} = \frac{1}{2} \quad (24)$$

$$S_{R_1}^{Q} = S_{\beta_N}^{Q} = S_{\alpha_N}^{Q} = 1 \quad (25)$$

$$S_{\alpha_P}^{Q} = S_{\beta_P}^{Q} = S_{C_1}^{Q} = S_{\gamma}^{Q} = S_{g_m}^{Q} = -S_{C_2}^{Q} = -S_{R_2}^{Q} = \frac{1}{2} \quad (26)$$

$$S_{\alpha_N'}^{\omega} = S_{\beta_N}^{\omega} = S_{\gamma}^{\omega} = S_{g_m}^{\omega} = -S_{C_1}^{\omega} = -S_{C_2}^{\omega} = -S_{R_1}^{\omega} = \frac{1}{2} \quad (27)$$

$$S_{\alpha_N'}^{Q} = S_{\beta_N}^{Q} = S_{C_1}^{Q} = -S_{\gamma}^{Q} = -S_{g_m}^{Q} = -S_{C_2}^{Q} = -S_{R_1}^{Q} = \frac{1}{2} \quad (28)$$

It can be seen that the active and passive sensitivities are not greater than one which is desirable.

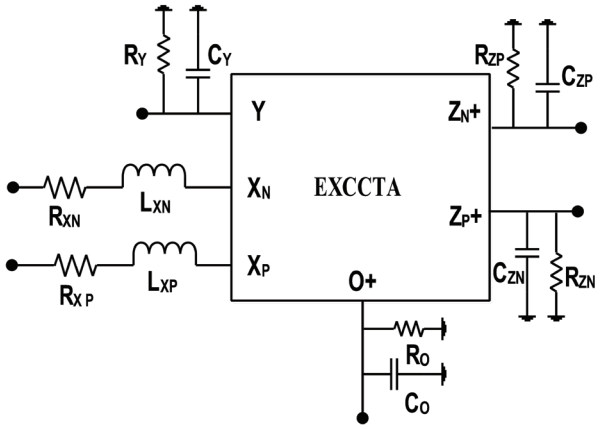


Figure 6: Non-ideal model of EXCCTA

5 Simulation results

In order to establish the workability of the proposed extra X current conveyor transconductance amplifier (EXCCTA). It was designed in 0.18µm parameters from TSMC. The circuit was simulated in spice to measure the important design metrics. The aspect ratios of the transistors are given in Table 5. The supply voltages are kept at V_{DD} = -V_{SS} = *0.9V*. The bias current was fixed at I_{bias} = 100µA. The bias current of OTA was set at 60µA which resulted in a transconductance of g_m = 0.334mS. The performance parameters of the EXCCTA are summarised in Table 6.

Table 5: Aspect ratios of the transistors

Transistor	Width (W µm)	Length(L µm)
M1- M4	3.06	0.72
M5- M7	9	0.72
M9- M23	14.4	0.72
M24- M28	0.72	0.72
M29-M32	3.6	1.8
M33-M40	7.2	1.8

The operation of the inductor simulators is evaluated next. The GIS-1 inductor simulator is tested, the passive component values are selected as R_1 = R_2 = 4kΩ, C_1 =

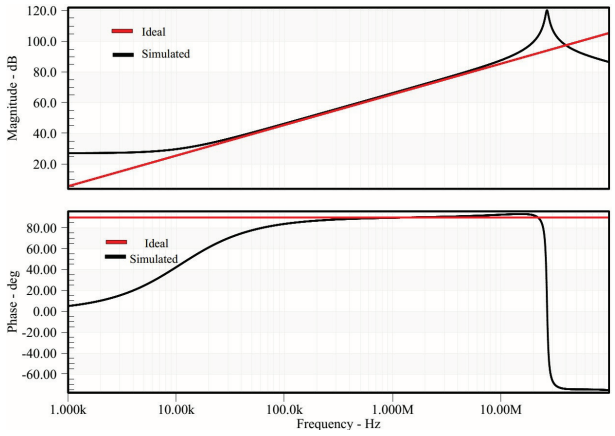


Figure 7: Magnitude and phase response of GIS-1

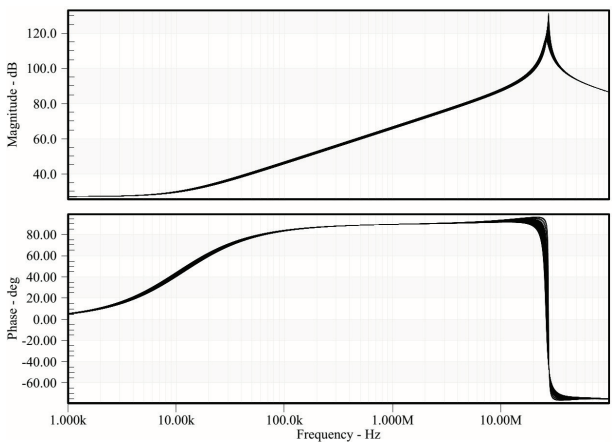


Figure 8: Monte Carlo result of GIS-1for 10% deviation in capacitance value

Table 6: Performance metrics of EXCCTA in Fig. 6

Voltage Gain	1.005
Current Gain (I_{ZP+} / I_{XP}), (I_{ZN+} / I_{XN}),	0.9998
Current Gain(I_{ZP-} / I_{XP}), (I_{ZN-} / I_{XN}),	0.964
Voltage Transfer Bandwidth	756.83MHz
Current Transfer Bandwidth (Z_{P+}, Z_{N+})	774.46 MHz
Current Transfer Bandwidth (Z_{P-}, Z_{N})	711.21 MHz
DC Voltage Range	±650mV
DC Current Range (Z_P,Z_N)	±140µA
DC Current Range (Z_{P-}, Z_{N-})	±60µA
X Node Impedance (RX)	39.940Ω
X Node Inductance (LX)	2.285µH
(Z_P,Z_N) Node Impedance	186.547kΩ
(Z_{P-}, Z_{N-}) Node Impedance	176.554kΩ

50pF and I_{bias} = 60µA resulting in the inductance of L_{eg} = 0.3mH. The magnitude response of the ideal and simulated inductor is given in Fig. 7. To study the effect of process variability on the performance of the inductor simulator Monte Carlo analysis is performed for 10% variation in the capacitance value with Gaussian distribution for 100 runs. It can be inferred from Fig. 8 that there is only slight deviation in the inductance value. To further ascertain the inductor's performance transient analysis is performed to verify the phase difference between current and voltage waveforms. The phase difference was found to be 87.2° as given in Fig. 9 which further verifies the behaviour of the synthetic inductor.

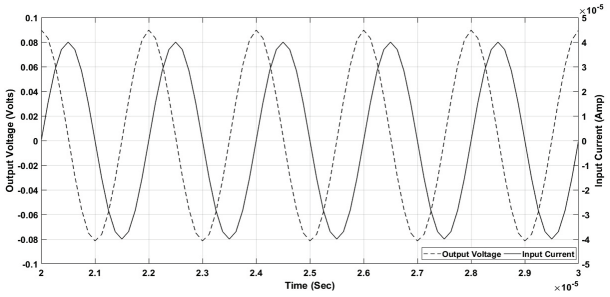


Figure 9: Transient analysis of GIS-1

The parallel inductor is now designed. The value of the passive elements are selected as $R_1 = R_1 = 4k\Omega$, $C_1 = 50pF$ and $I_{bias} = 60\mu A$ resulting in the inductance of $L_{eq} = 0.3mH$ in parallel with $R_{eq} = 4k\Omega$. It is to be noted that by appropriately selecting the value of R_1 the value of parallel resistor can be set without affecting the inductance. The magnitude response of GIS-3 is given in Fig. 10.

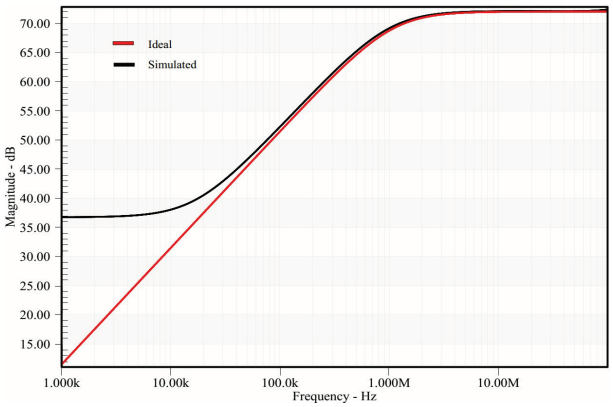


Figure 10: Magnitude response of GIS-3

6 Applications of the proposed inductance simulators

To examine the applicability and feasibility of the proposed inductor simulators in practical applications they are utilized in numerous applications. The pure inductor simulator GIS-1 is utilized in the design of third order Butterworth ladder filter [5] as shown in Fig. 11. The transfer function of the filter is given in Equation 29. The passive elements of the filter are selected as $C_1 = C_2 = 0.1$ nF, R_s = 1kΩ, R_L = 1kΩ and L_1 = 60 uH. The resistors R_s and R_L are the source and load resistances, respectively. The inductor in the passive implementation is replaced by the active GIS-1 Fig 3(a). The components of GIS-1 are selected as $R_1 = R_2 = 4k\Omega$ and C_1 = 10 pF to get L_{eq} = 60uH for the active inductor. The Ideal and simulated filter response are given in Fig.12. It can be deduced that the ideal and simulated curves bear close resemblance.

A current mode multifunction filter [27] is also designed using the GIS-1. The parallel passive RLC filter is shown in Fig. 13. The filter is designed for -3dB cutoff frequency of 2.054 MHz by selecting components values as C_f = 10pF, R_f = 10kΩ and L_{eq} = 0.6 mH. The pas-

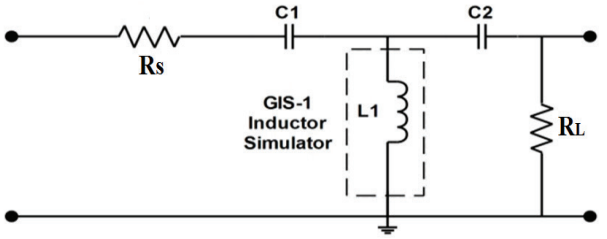


Figure 11: The third order Butterworth filter

$$\frac{V_{out}}{V_{in}} = \frac{\frac{S^3 R_L}{R_S+R_L}}{S^3+S^2\frac{Leq(C_1+C_2)+C_1C_2R_SR_L}{LeqC_1C_2(R_S+R_L)}+S\frac{C_1R_S+C_2R_L}{LeqC_1C_2(R_S+R_L)}+\frac{1}{LeqC_1C_2(R_S+R_L)}} \quad (29)$$

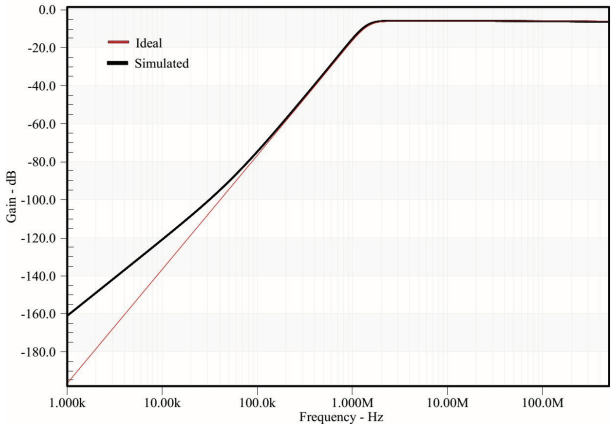


Figure 12: The response of third order Butterworth filter

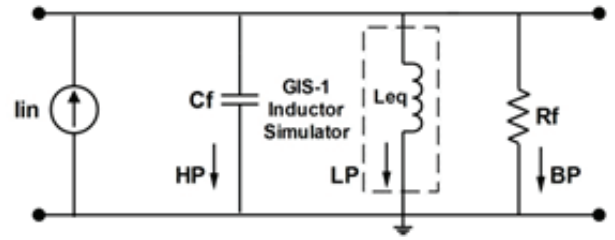


Figure 13: Current mode multi function filter

sive inductor in the filter is replaced by active inductor GIS-1. The components of GIS-1 Fig. 3(a) are selected as $R_1 = R_2 = 4k\Omega$ and $C_1 = 100$ pF to get $L_{eq} = 0.6$ mH. The ideal and simulated frequency response of the filter is given in Fig. 14.

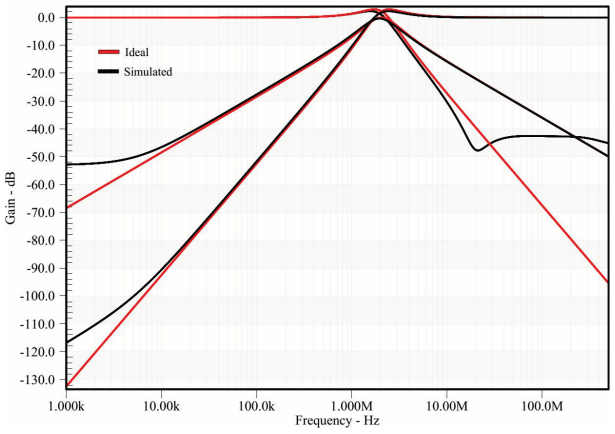


Figure 14: Frequency response of current mode multi function filter

$$f_o = \frac{1}{2\pi\sqrt{L_{eq}C_f}} \tag{30}$$

The two passive elements based inductor simulator GIS-3 is utilized in the design of voltage mode second order high pass filter as presented in Fig. 15. The transfer function and expression for frequency of the filter are given in Equations 31-32. The passive element values for the passive filter are selected as $C_f = 80$ pF, $R_f = 2k\Omega$ and $L_{eq} = 0.6$ mH which corresponds to -3dB cutoff frequency of 726.439kHz. To realize the required inductance the passive elements of the GIS-3 Fig. 3(c) are chosen to be $R_1 = 4k\Omega$ and $C_1 = 100$ pF to get L=0.6mH for GIS-3. The ideal and simulated response of the filter are given in Fig. 16.

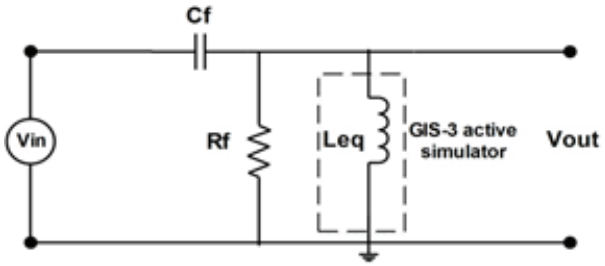


Figure 15: Voltage mode HP filter

$$\frac{V_{out}}{V_{in}} = \frac{S^2}{S^2 + S\dfrac{1}{C_f R_f} + \dfrac{1}{L_{eq}C_f}} \tag{31}$$

$$f_o = \frac{1}{2\pi\sqrt{L_{eq}C_f}} \tag{32}$$

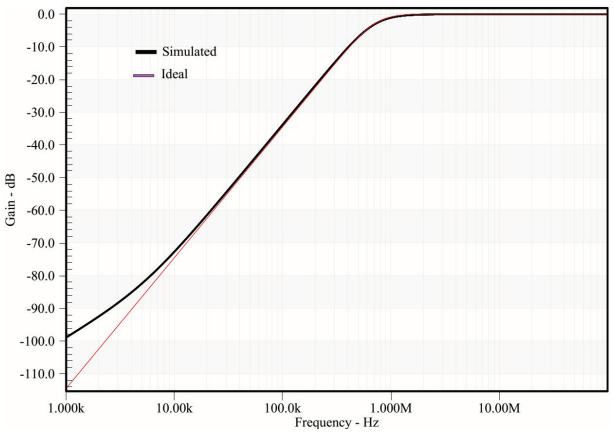


Figure 16: Frequency response of Voltage mode filter

Now the lossy parallel RL inductor GIS-4 is used in the design of second order current mode HP filter. The passive prototype of the filter is presented in Fig. 17 and the transfer function and pole frequency is given in Equations 33-34. The filter is designed for -3dB cutoff frequency of 918.88 kHz by choosing $C_f = 50$ pF, $R_{eq} = 4k\Omega$ and $L_{eq} = 0.6$ mH. The parallel $R_{eq}\|L_{eq}$ in the passive prototype are replaced by parallel RL active inductor simulator GIS-4 Fig.3 (d). The GIS-4 is designed with $R_1 = R_2 = 4k\Omega$ and $C_1 = 100$ pF. The ideal and simulated values are given in Fig. 18. To test the signal processing

capability of the filter transient analysis is performed. A sinusoidal current signal with 80μA p-p is applied to both filters with ideal passive elements and filter with simulated RL. The results are shown in Fig. 19. It is clear that the ideal and simulated curves follow each other closely verifying the correct functioning of the GIS-4 simulator.

$$\frac{I_{out}}{I_{in}} = \frac{S^2}{S^2 + S\frac{1}{C_f R_f} + \frac{1}{L_{eq} C_f}} \tag{33}$$

$$f_o = \frac{1}{2\pi\sqrt{L_{eq} C_f}} \tag{34}$$

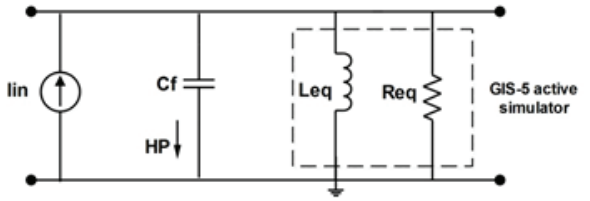


Figure 17: Current mode high pass filter

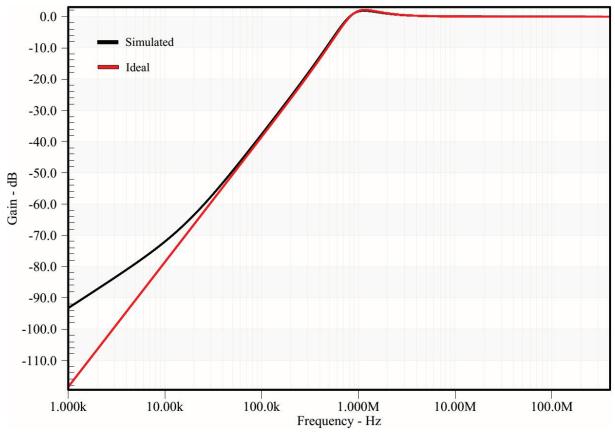


Figure 18: Frequency response of Current mode high pass filter

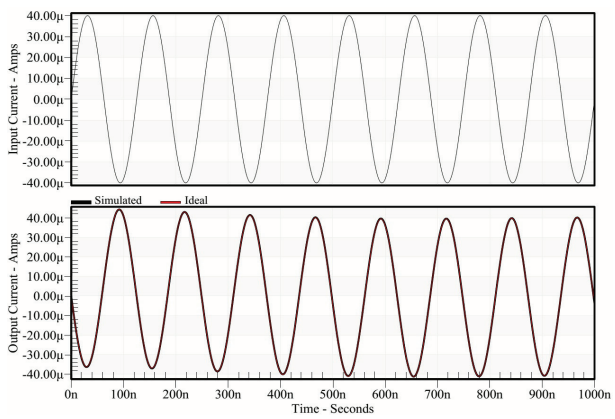


Figure 19: Transient analysis of Current mode high pass filter

7 Verification of the Proposed Universal Filters

The proposed MISO VM filter is tested. The filter is designed for -3dB cutoff frequency of 2.054MHz by selecting C_1 = 20 pF, C_2 = 20 pF, R_1 = 5kΩ and R_2 = 5kΩ. The resulting quality factor of the filter is found to be 1.29. The response of the filter is presented in Fig. 20. The response of the AP filter is given in Fig. 21. The simulated pole frequency of the is found to be 1.998MHz which translates in to 3.21% error this is due to parasitic elements discussed above. To investigate the signal processing capabilities of the filter transient analysis is also performed for the BP configuration. It can be inferred from the Fig. 22 that the filter performs well. The total harmonic distortion(THD) of the filter for band pass configuration is also calculated which is found to be perfectly within acceptable limit for wide input voltage range as shown in Fig. 23. The THD remains within 1% till 200mV input voltage.

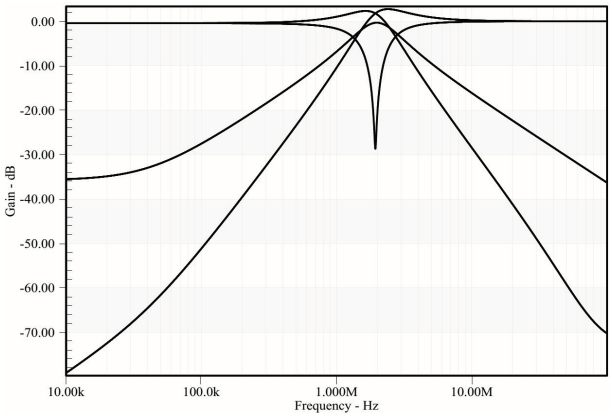


Figure 20: Simulated characteristics of the MISO VM filter

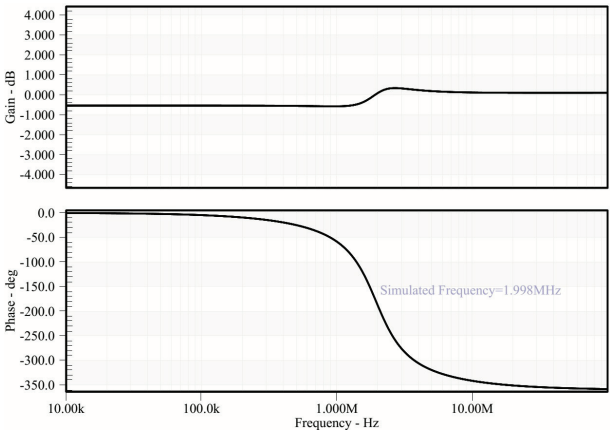


Figure 21: Simulated characteristics of the MISO VM AP filter

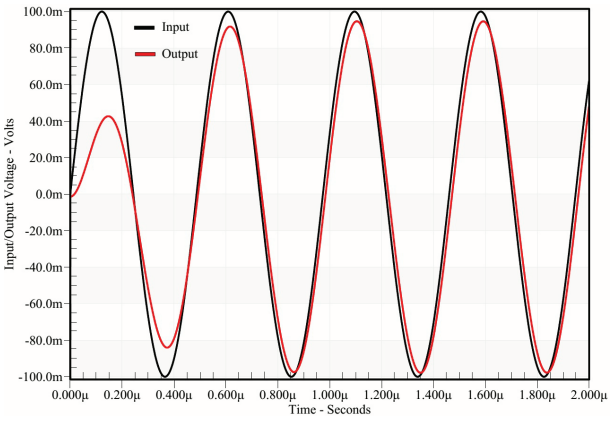


Figure 22: Transient analysis of the band pass filter

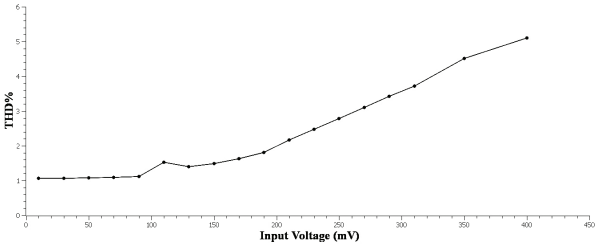


Figure 23: Total harmonic distortion of the band pass filter configuration

The effect of process variations on the proposed filter is studied by performing Monte Carlo analysis of the HP response of the filter. The analysis is carried out for 10% deviation in the two capacitor values adopting the Gaussian distribution. The result for 50 runs given in Fig. 24 shows that the filter functions well with minute deviations that can be accommodated by adjusting the bias current of the OTA for precise frequency control.

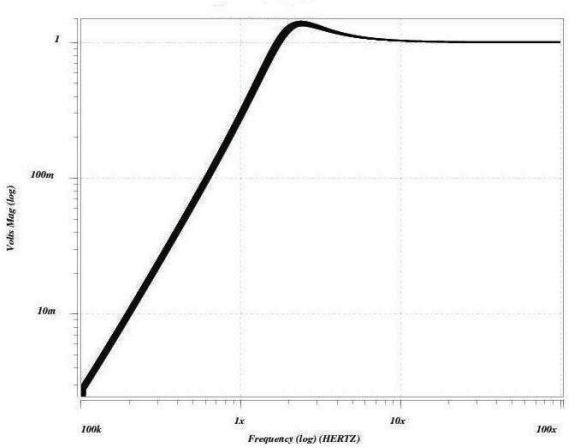


Figure 24: Monte Carlo analysis of the HP filter for 10% deviation in capacitance values

Table 7: Comparison of MISO filters available in the literature with the proposed filter

S. No.	Type of Filter	Active Block Used(No.)	No. of R+C	No. of grounded C+R	Matching Condition	Electronic Tunability	Inverting Input Needed	Low output Impedance
[29]	MISO (VM)	CCII+ (3)	2+2	0+0	No	No	No (Except for AP)	No
[30]	MISO (VM)	DVCC (3)	4+2	2+3	No (Except for AP)	No	No	No
[31]	MISO (VM)	CCTA (1)	2+2	0+0	No	Yes	No	No
[32]	MIMO (VM)	DVCC (1)	2+2	0+0	Yes	No	No	No
[33]	MISO (VM)	DOCCCII (2)	0+2	0+0	No	Yes	No (Except for AP)	No
[34]	MISO (VM)	VD-DIBA	1+2	0+0	No	Yes	No	No
[35]	MISO (VM)	CDBA (2)	4+2	0+0	Yes	No	No	Yes
[36]	MISO (VM)	DDCC (2)	2+2	2+1	No	No	No	No
[37]	MIMO (VM)	FDCCII (1)	3+2	1+1	No	No	No (Except for AP)	No
[38]	MISO (VM)	DDCC (3)	2+2	2+2	No	No	No	Yes
Proposed	MISO (VM)	EXCCTA (1)	2+2	1+0	No	Yes	No (Except for AP)	Yes

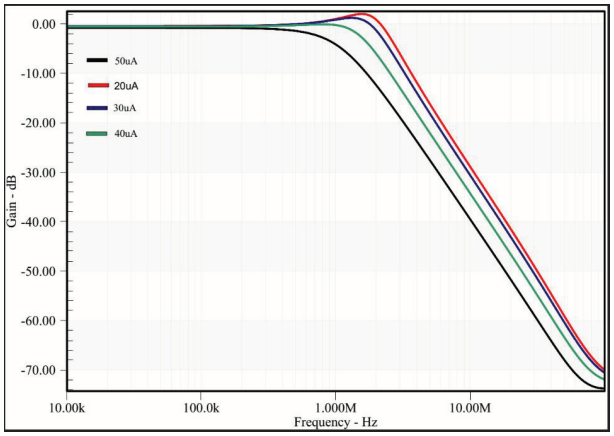


Figure 25: Simulated characteristics of the MISO VM LP filter for different bias currents

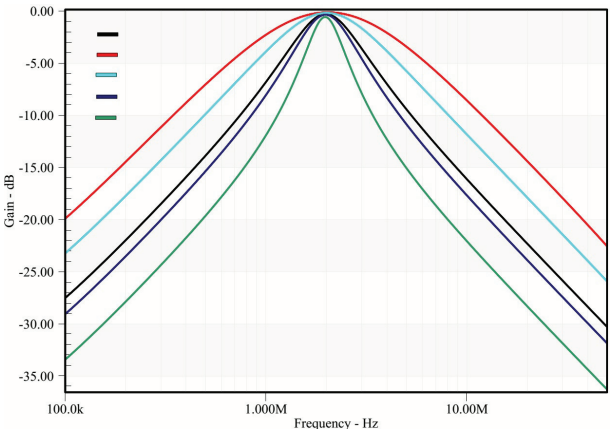


Figure 26: Simulated characteristics of the MISO VM BP filter for different quality factors

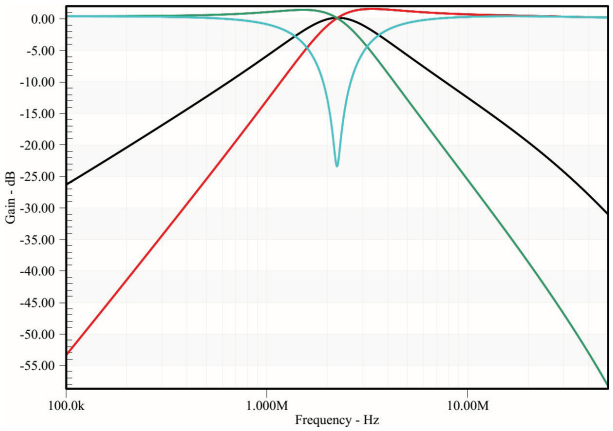


Figure 27: Simulated characteristics of the SIMO CM filter

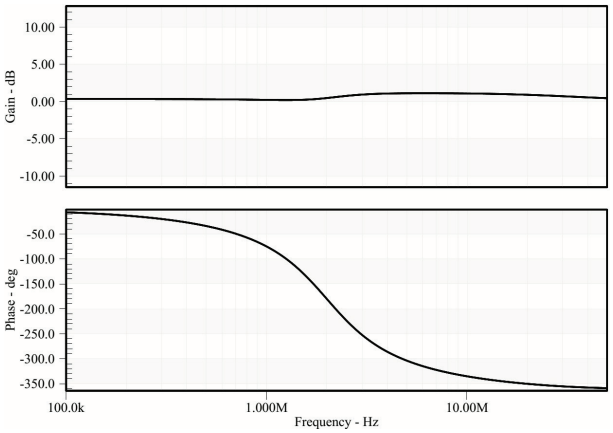


Figure 28: Simulated characteristics of the SIMO CM AP filter

Tunability is an importance feature of filters [28], this attribute enables a filter to be useful at different frequencies without requiring any alteration in the passive components values. The pole frequency of the proposed filter can be adjusted by varying the bias current of the OTA. The LP response of the filter is plotted for different bias currents as shown in Fig. 25. It can be seen from the figure that the bias current slightly effects the quality factor of the filter as can be deduced from Equations (13-14) . To realize a unity quality factor the resistance R_1 should be adjusted accord-

Table 8: Comparison of CM SIMO filters available in the literature with the proposed filter

S. No.	Type of Filter	Active Block Used(No.)	No. of R+C	No. of grounded C+R	Matching Condition	Electronic Tunability	High output Impedance
[39] Fig. 3	SIMO (CM)	CBTA (1)	2+2	2+2	No	Yes	No
[40]	SIMO (CM)	CDTA (1)	2+2	2+0	No	Yes	No
[41]	SIMO (CM)	DV-DXCCI (1)	2+2	2+2	No	No	Yes
[42]	SIMO (CM)	UCC (3)	2+2	2+2	No	No	Yes
[43]	SIMO (CM)	CCCII (3)	0+2	2+0	No	Yes	Yes
Proposed	SIMO (CM)	EXCCTA (1)	1+2	1+2	No	Yes	Yes

ingly. The quality factor of the proposed filter can also be tuned independent of the pole frequency by varying the resistance R_1 as can be seen in Figure 26 which gives the plot of Q for different values of resistance R_1.

A comparison is provided in Table 7 to compare the proposed VM MISO filter with the other state of the art filter structures.

Lastly, the CM SIMO filter is validate by designing it for -3dB cutoff frequency of 2.204MHz by selecting C_1 = 20 pF, C_2 = 20 pF, R_1 = 3.61 kΩ and OTA bias current of 50µA. The frequency response of the filter is given in Fig. 27 and the AP response is shown in Fig. 28 The filter is compared with other exemplary SIMO filter topologies to highlight its advantages as shown in Table 8.

8 Experimental Results

The EXCCTA can be easily implemented using commercially available integrated circuits AD844 and LM13700. The possible implementation of GIS-1 using only two AD844 and one LM13700 IC is shown in Fig. 29. The ICs are supplied with a bias voltage of ±10V, the I_{bias} of the OTA is fixed at 372µA. The passive components values are chosen to be R_1 = R_2 =1kΩ and C_1 = 10 nF resulting in the inductance of L=672µH. To test the circuit a triangular waveform with 2V p-p at 17kHz is applied through R_2 and R_3 to convert it in to corresponding input triangular current. A square wave form is obtained across the inductor. The oscilloscope output is shown in Fig. 30 which validates the correct functioning of the active inductor.

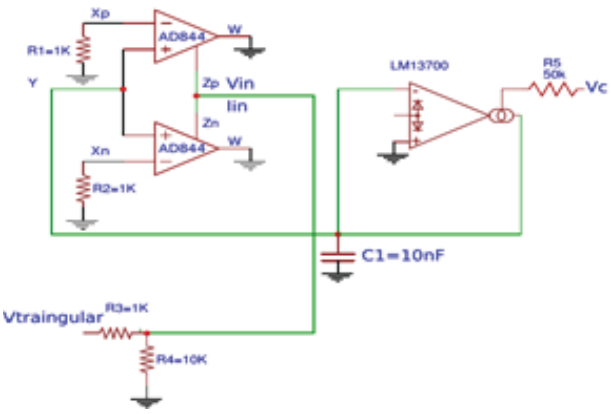
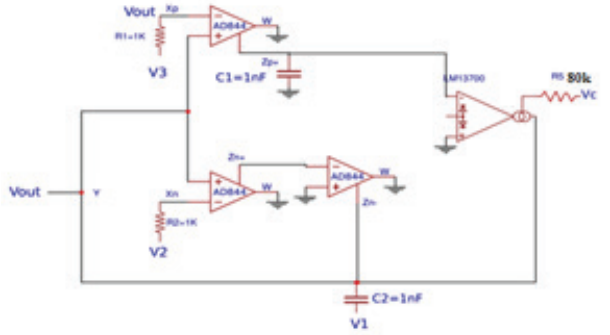


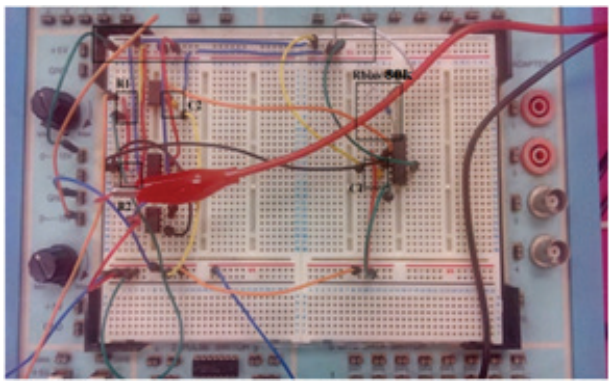
Figure 29: Implementation of the GIS-1 from the commercially available ICs

To further validate the VM filter it is implemented on breadboard using AD844 and LM13700 ICs. The filter implementation is given in Fig. 31 (a-b). The filter is designed for -3dB frequency of 343.199kHz by selecting

Figure 30: The experimental result of the inductor simulator



(a)



(b)

Figure 31: Experimental setup of the VM filter from the commercially available ICs (a) Block Diagram (b) Bread board implementation

passive components values equal to R_1 = R_2 =1kΩ, C_1 = C_2 =1nF and I_{bias} = 232.5µA. The ideal and experimentally calculated response of the filter is presented in Fig. 32. The measured frequency of the filter is found to be 321kHz leading to an error of 6.46%, this discrepancy arises due to non-idealities present in the EXCCTA and also due to the parasitics introduced by connecting leads and breadboard, nonetheless it verifies the practical feasibility of the proposed VM filter.

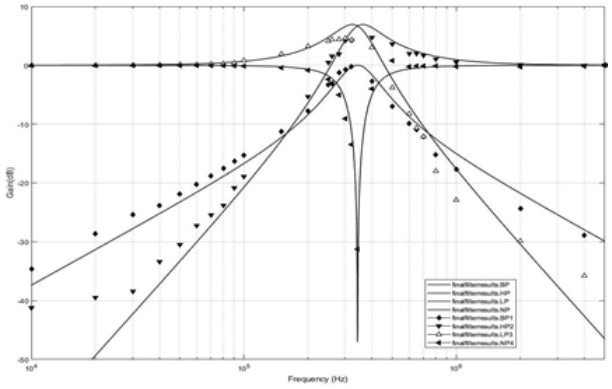
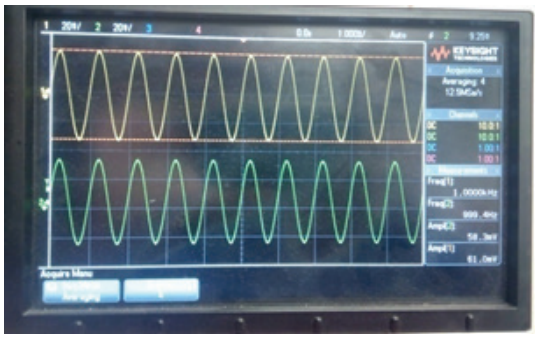
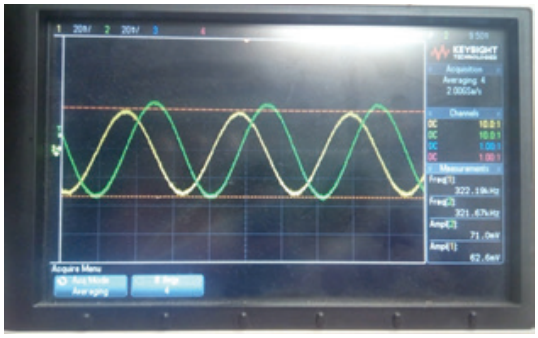


Figure 32: The ideal and experimental results of the VM MISO filter

(a)



(b)



(c)

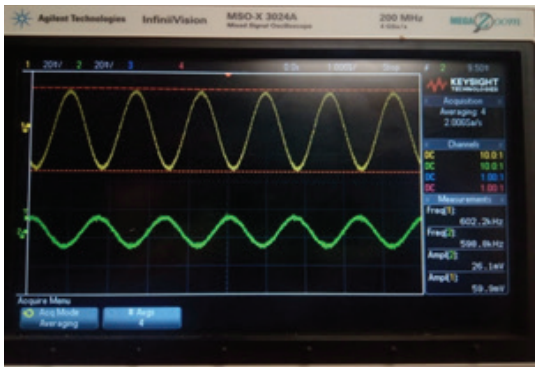


Figure 33: Time domain analysis of LP response (a) 1kHz (b)321 kHz (c) 600 kHz

The experimental time domain analysis of the filter is also performed by exciting it with a sinusoidal input signal of 60mV p-p at frequencies of 1kHz, 321kHz and 600kHz. The filter output obtained on the oscilloscope for LP configuration is presented in Fig. 33 (a-c).

9 Conclusion

In this research, a new active element namely EXCCTA is proposed. The EXCCTA is used to design six topologies of lossy and lossless active inductors. Additionally, to further elaborate its versatility two universal VM and CM filter structures employing a single EXCCTA are also proposed. The inductor simulators make use of single EXCCTA, grounded passive elements, requires no passive components matching and are perfectly tunable. The voltage mode filter is obtained by slightly modifying the proposed series inductor. The VM filter makes use of canonical number of passive elements and has low output impedance. The CM filter is SIMO type and utilize only three grounded passive elements for implementation. Both the proposed filter structures enjoy low sensitivities, inbuilt tunability and orthogonal control of quality factor and pole frequency. The non-ideal analysis of the inductor simulators and filter structures is also performed. The simulations are performed in 0.18µm parameters from TSMC to verify the theoretical analysis. Experimental results for pure inductor and SIMO VM filter are also included to substantiate the theoretical findings.

10 Acknowledgement

The authors gratefully acknowledge the support provided by UKM internal grant (GUP-2015-021) for this study.

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Arrived: 18. 12. 2017
Accepted: 04. 05. 2018

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 48, No. 2(2018), 115 – 120

The Design of Broadband LNA with Active Biasing based on Negative Technique

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Abstract: In this paper, we present a broadband LNA based on an improved negative feedback design. With the adjustment of the negative feedback inside the chip, the LNA achieves a planarized gain and an optimized operating bandwidth from 0.2 GHz to 4 GHz. To guarantee the good performance stability under severe environments, an active biasing is used inside the chip. As a result, effective compensations for the fluctuation of the supply voltage and the temperature variation are achieved. The LNA chip uses GaAs pHEMT at 0.25-μm technology node and SIP package technique. This broadband LNA shows good performances, including gain of about 15 dB, gain flatness of less than 1dB, and noise figure of less than 1.5 dB. The packaged size of this broadband LNA is 3 mmX3 mmX1 mm.

Keywords: feedback network; broadband LNA; active biasing; SIP package

Načrtovanje širokopasovnega LNA z aktivnim napajanjem na osnovi negativne tehnike

Izvleček: Članek predstavlja širokopasovni LNA na osnovi izboljšane negativne povratne zanke. Nastavljiva negativna zanka v čipu omogoča LNA doseganje ojačenja in optimalne pasovne širine med 0.2 in 4 GHz. Za doseganje dobrih lastnosti v neugodnem okolju je uporabljeno aktivno napajanje v čipu. Doseženo je efektivna kompenzacija fluktuacij napajalne napetosti in temperature. LNA čip uporablja GaAs pHEMT v 0.25 μm tehnologiji in SIP ohišje. LNA izkazuje dobre lastnosti vključno z ojačenjem 15 dB, stabilnostjo ojačenja pod 1 dB in šumom pod 1.5 dB. Velikost ohišja je 3 mmX3 mmX1 mm.

Ključne besede: povratno omrežje; širokopasovni LNA; aktivno napajanje; SIP ohišje

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1 Introduction

With the rapid evolution of wide-bandwidth technology, more attentions are drawn by the design of wideband receivers which are able to cover a wide range of frequency standards [1].

The main difficulty in designing a wideband LNA is to achieve high gain, low noise figure and excellent linearity simultaneously. There were various architectures reported in the literature to achieve wideband LNAs, including distributed LNAs, balanced LNAs, common gate LNAs and feedback LNAs. The first three share features of small input and output reflection coefficient while they have disadvantages such as low gain and high power dissipation [2, 3]. The feedback is featured for tradeoff among several performance specifications, which is popular in wideband LNA designs. There are many researches which have designed wideband LNAs utilizing feedback technology. However, only LNA die is considered in their works, and no parasitics of bonding wire and package are taken into account. Biasing circuit also has influence on the performance of LNA. The current mirror with temperature compensation is the most popular biasing, but it does not take the fluctuation of power supply into consideration [4].

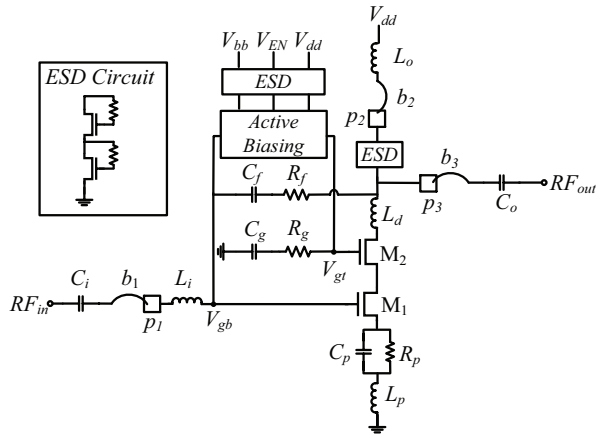
In this paper, we report a broadband LNA with an active biasing based on an improved negative feedback. In order to extend the bandwidth, a feedback unit is used between the drain and gate, and a RC cell is added at the source. The influence of external parasitics is introduced by applying equivalent circuit elements of bonding wire and ESD circuits. The stable performances under different severe conditions are achieved via an active biasing inside LNA die, which can compen-

sate the fluctuation of environmental temperature and the supply voltage variation.

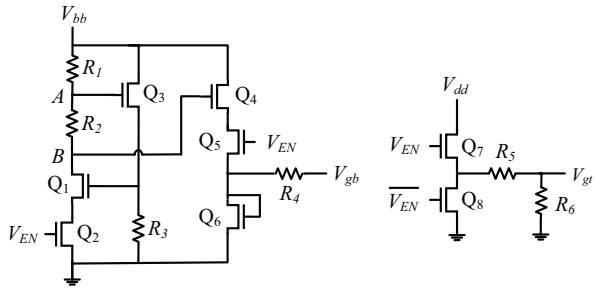
The LNA described in this paper exhibits a broad bandwidth of more than 20 octaves, from 0.2 GHz to 4 GHz, covering several communication standards like GSM, GPS, TD-SCDMA, WCDMA, and Bluetooth.

2 Design principle and approach

As the circuit diagram showed in Fig. 1(a), the wideband LNA in this paper is composed of Cascode amplifier, feedback circuit, active biasing circuit, ESD circuit, source degeneration inductance, input and output matching networks. We choose the Cascode topology for priority to eliminate miller effect and to increase reverse isolation [5]. A load capacitor Cg is added at the gate of M2 to improve power gain. And a resistor Rg is added in series in order to minimize the deterioration of stability due to the introduction of Cg. The equivalent element of bonding wires (b1, b2, b3), pads(p1, p2, p3) and the ESD circuits are also considered in our simulation.



(a)



(b)

Figure 1: (a) The electric circuit diagram of LNA Amplifier (b) A novel active biasing circuit

The active biasing circuit of the presented LNA is shown in Fig. 1(b). Q2 and Q5 work as switching transistor. When VEN is set at low voltage, the switching transistor is in off-mode, and only an infinitesimal current exists in biasing circuit. While in on-mode when VEN is set at high voltage, DC bias is supplied for the operation of LNA. Q6 works as diode for voltage stabilization.

E-mode transistor Q1 and Q3, resistor R1, R2 and R3 form the temperature compensation circuit. When the ambient temperature decreases, the drain current of Q1 increases. As a result, the potential at point A decreases. Thereby, the gate-to-source voltage and the source current of Q3 decrease. And the voltages on R3 which is also the gate-to-source voltage of Q1 would decrease. This results in the restriction of the drain current growth of Q1, which benefits the performance stability of the LNA. Similar temperature compensation phenomenon can be achieved when ambient temperature increases.

The temperature compensation circuit also works as a supply voltage regulation circuit. When Vbb decreases, potential would decrease at point A and B. Therefore the gate-to-source voltage of Q3 would decrease, which as we mentioned above, results in a decreasing of gate-to-source voltage of Q1.Then the drain current of Q1 would increase, which restricts the decrease of potentials at point A and B.

In conclusion, the active biasing circuit can compensate the temperature and voltage fluctuations effectively. Therefore, a stable output voltage can be achieved and stable performance at different severe conditions is guaranteed.

According to the feedback circuit of LNA, traditional negative feedback circuit is composed of a single resistor between drain and gate, which couples part of signal from output to input, and enhances the bandwidth along with the sacrifice of gain [6, 7].

In our design, we exhibit an improved negative feedback to further extend the bandwidth and improve the high-frequency performance of the LNA. As shown in Fig. 2(a), a capacitor Cf is introduced for the isolation of DC signal. And an inductor Ld is added at drain for the compensation of the capacitive portion of output impedance at high frequency, which extends the operating frequency range.

For simplification, we analyze the contribution of Zd and Zp, respectively. The simplified equivalent circuits are shown in Fig. 2(b) and 2(c).

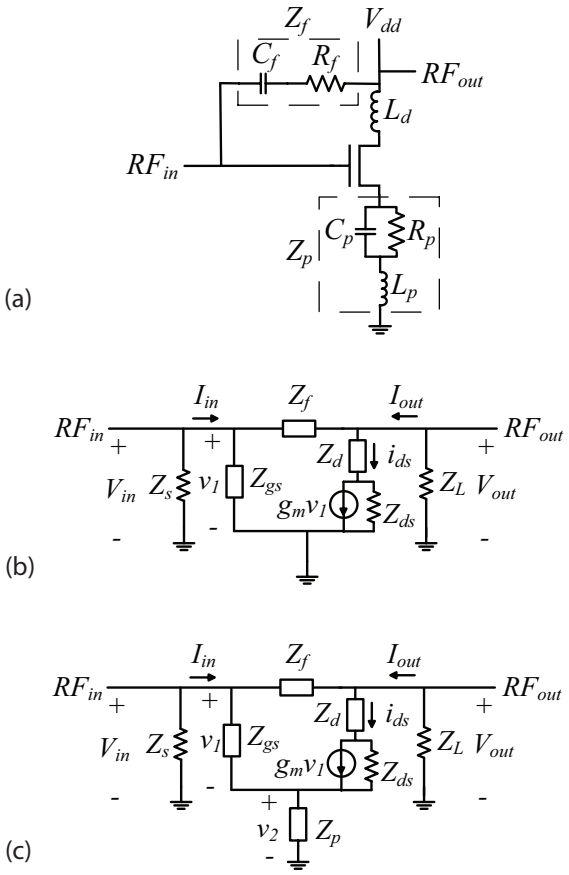


Figure 2: (a) Improved negative feedback amplifier (b) The equivalent circuit of LNA with L_d (c) The equivalent circuit of LNA with L_d and *RC* cell

From **Fig**. 2(b), we know

$$V_{in} = V_{out} \frac{Z_f}{Z_{gs} // Z_s + Z_f} \tag{1}$$

$$V_{out} = (I_{out} - i_{ds})[Z_s // Z_{gs} + Z_f] \tag{2}$$

$$R_{out} = \frac{V_{out}}{I_{out}} = \frac{(Z_{ds} + Z_d)(Z_{gs} // Z_s + Z_f)}{g_m Z_f Z_{ds} + Z_{ds} + Z_d} \tag{3}$$

Where

$$Z_{ds} = \frac{1}{sC_{ds}} // R_{ds} \tag{4}$$

The inductor Ld (Zd in equation (3)) is introduced to effectively eliminate the capacitive parts of load resistance, and as a result to achieve a broad bandwidth, as shown in curve B in Fig. 3.

As shown in Fig. 2(c), Zp at source consists of an inductor Lp and a RC parallel cell. The degeneration inductor Lp is introduced to reduce the difference between optimum impedances of NFmin and Gainmax, and to improve the LNA performance on NF and Gain simultaneously. As for the RC cell, the capacitor Cp behaves as open at low frequency and gain attenuation exists due to the resistor Rp. While at high frequency, the impedance of Cp is close to short and no signal flows through Rp. Therefore the gain flatness of LNA is improved.

The EM simulation of the presented LNA with novel negative feedback circuit is carried out using ADS. The gain performance comparison with traditional negative-feedback LNA as a function of frequency is shown in Fig. 3. Compared with curve A, operating from 0.2 GHz to 2.1 GHz, the bandwidth of curve B is extended pronouncedly, covering 0.2 GHz to 3.6 GHz, due to the introduction of Ld. From the comparison between curve B and C, the latter attains more ideal gain flatness covering 0.2 GHz to 4 GHz due to the gain attenuation at low frequency by the introduction of paralleled RC cell at source.

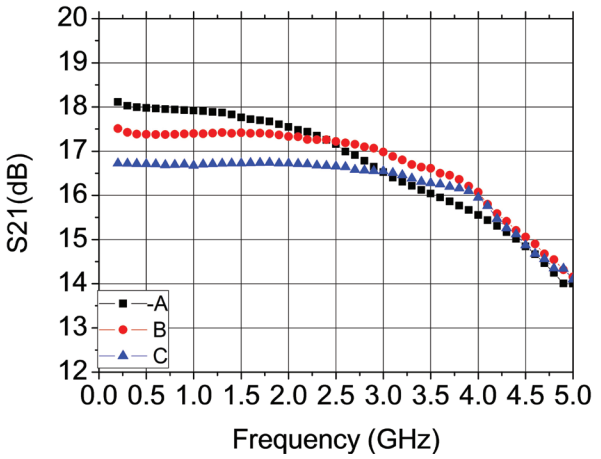


Figure 3: The Gain characteristic of LNA with various feedbacks, in which A: traditional feedback, B: feedback with additional L_d, C: presented novel feedback

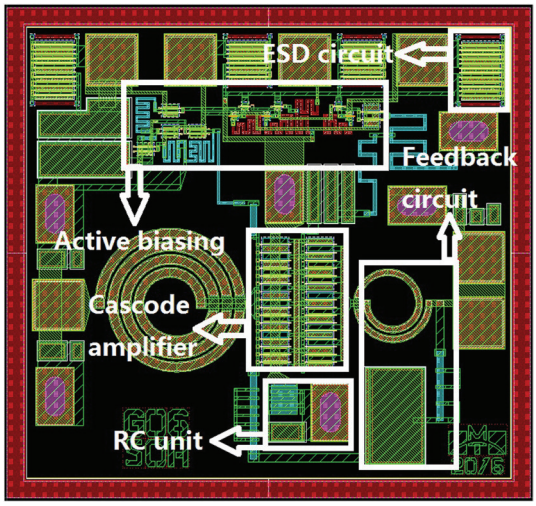
3 Implementation and measurements

The proposed LNA is constructed by an LNA die and several lumped elements including the output impedance matching inductor and capacitor, a decoupling capacitor and a DC blocking capacitor. SIP technique is used for integration. Based on the tradeoff between gain and output power linearity, we use a pair of 16 × 40 μm GaAs pHEMT with Cascode configuration on the LNA die.

The broadband LNA die is fabricated by 0.25-μm GaAs pHEMT process with the size of 0.8 mm × 0.75 mm, including all RF and DC pads, as shown in Fig. 4(a). In the design of LNA layout, ESD circuits are introduced at each DC supply pads for electrostatic protection.

The substrate of the SIP package consists of 4 metal layers. On the bottom metal layer there locates the LGA (Land Grid Array) pads, which have smaller parasites compared to traditional pins [8]. The second and third metal layers are patterned for biasing DC signal. The top layer is for RF signal. The total size of substrate is 3 mm × 3 mm.

(a)



(b)

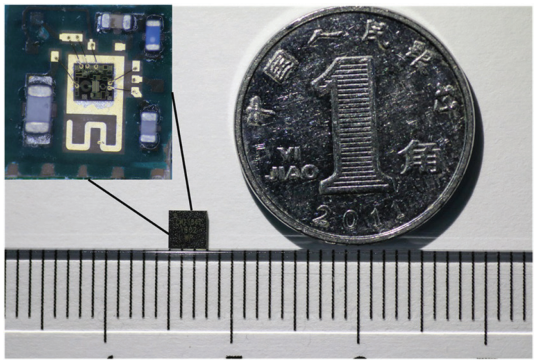
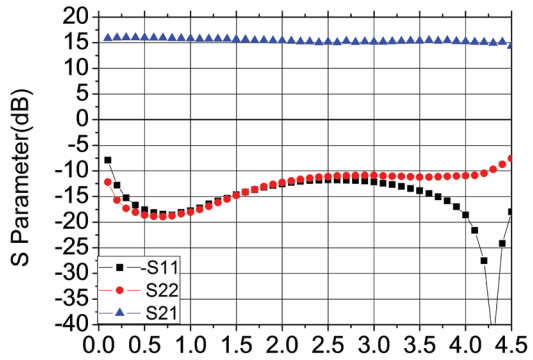


Figure 4: (a) Layout of LNA die (b) Packaged LNA

In order to minimize the size of the LNA chip, we use an inductor as the input matching element on the LNA die and put the input block capacitance, the output matching network which consists of a low-pass LC cell, an inductor Lo, and a capacitor Co on the package substrate.

When packaging is finished, we measure the LNA in detail under the bias condition Vdd=3.3 V and Vbb=3.3 V at room temperature. Fig. 5(a) shows the measured S-parameters. From 0.2 GHz to 4 GHz, LNA shows no-less-than 15 dB small signal gain, and less than -10 dB reflection loss at both input and output. The gain flatness within operating frequency band is about 1.2 dB. Fig. 5(b) shows the measured NF, P-1dB and IIP3. The NF of the LNA is less than 1.6 dB, while P-1dB is 17 dBm. The OIP3 is 19 dBm, from which we deduct the gain with 15 dB, therefore the IIP3 is 4 dBm.

(a)



(b)

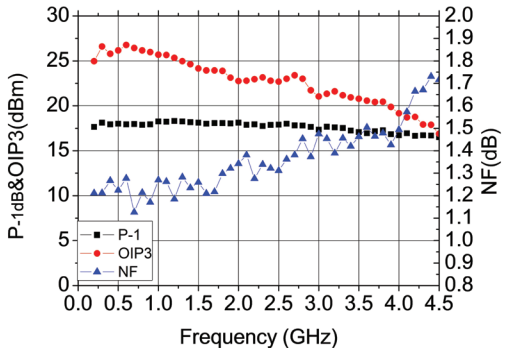


Figure 5: (a) The S-parameter of LNA. (b) The NF, P_{-1dB} and OIP3 of LNA.

To explore the advantages of the biasing circuit inside the LNA die, we measure the S-parameters and the NF at different temperature conditions (-40°C, 25°C, 85°C), as shown in Fig. 6(a) and 6(b). With the variation of temperature from -40°C to 85°C, the fluctuation of gain and NF are both within ±0.4 dB, which validates the temperature compensation of the active bias.

The comparison of published measurement results of wideband LNAs and this work is shown in Table 1. The bandwidth of this work is up to 20 octaves while maintaining a superior gain flatness, a low NF and a good linearity.

4 Conclusion

This paper presents a broadband LNA based on the improved negative feedback design. GaAs pHEMT at 0.25-

Table 1: Performance comparison of wideband LNA

Ref	Device Tech	Freq (GHz)	G (dB)	NF(dB)	ΔG (dB)	VDC (V)	P-1dB (dBm)	IIP3 (dBm)	Pdiss (mW)
[9]	0.5 μm GaAs pHEMT	2.5~5	17	2.4~3	1.6	1.5	-2	2.3	33
[10]	0.18 μm CMOS	0.9~1.1	10.7	1.3	None	2.5	18.4	3	50
[11]	0.18 μm CMOS	2.5~6.8	11.5	4.2	4	1.8	None	None	8.1
This Work	0.25 μm GaAs pHEMT	0.2~4	15	1.6	1.2	3.3	17	4	33

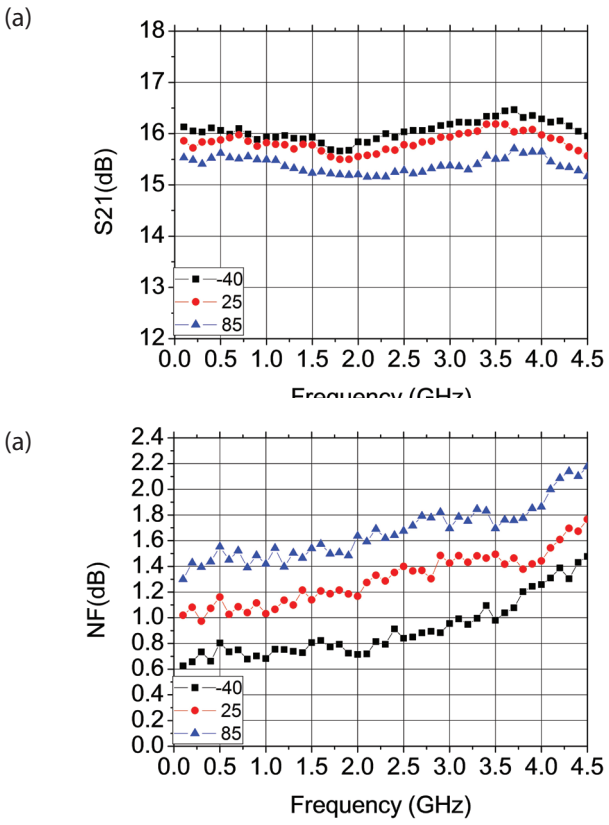


Figure 6: (a) The S-parameter of LNA. (b) The NF, P_{-1dB} and OIP3 of LNA.

μm technology node and SIP package technique are applied. The LNA consists of a pair of 16 × 40 μm GaAs pHEMTs with Cascode configuration and a novel negative feedback circuit between drain and gate which remarkably extends the operation bandwidth. An active biasing technique is applied to effectively compensate the fluctuation of the supply voltage and the temperature variation. The designed LNA has achieved a broad bandwidth of up to 20 octaves from 0.2 GHz to 4 GHz while maintaining a gain flatness of less than 1.2 dB. A low NF of less than 1.6 dB and a good linearity are also obtained. The presented LNA can be applied in severe conditions to cover several communication standards like GSM, GPS, TD-SCDMA, WCDMA, and Bluetooth.

5 Acknowledgment

This work was supported by the National Natural Science Foundation of China under Grant 61604128.

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Arrived: 24. 02. 2018
Accepted: 22. 05. 2018

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 48, No. 2(2018), 121 – 128

Real-Time Random Number Generation with Ring Oscillator Based Double Physically Unclonable Function

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Abstract: Integrated Circuit (IC) is a semiconductor wafer that is fabricated for millions of components. Although it is accepted that the same chemical properties are observed in the same type of ICs produced within the processes of wafer production, masking, etching, doping, atomic diffusion, ion implantation, metallization and packaging steps, these properties differ at microscopic levels. For example, the propagation delay is different in two logic elements in the same integrated circuit, and the silicon distribution in each LE is not equal. These differences have created the concept of Physically Unclonable Function (PUF). PUF is a function that creates values specific to the physical environment in which it operates. This article presents the implementation of a ring oscillator- (RO) based PUF design in two different ICs to generate random numbers. Two different FPGA (Field Programmable Gate Array) cores were used in the proposed structure, and PUF structures were implemented on these hardware elements. The raw random numbers obtained by the generated system were post-processed to be used in applications (e.g. encryption, game programming). The study used Von Neumann and hash functions for post-processing. NIST and Autocorrelation tests were also administered to check the validity of the obtained random numbers.

Keywords: Random number generation; Field programmable gate arrays; physically unclonable function**.**

Generator naključnih števil v realnem času z dvojno funkcijo nekloniranja na osnovi obročnega oscilatorja

Izvleček: Integrirana vezja so narejena na polprevodniški rezini. Kljub enakim kemijskim postopkom izdelave se lastnosti integriranih vezij na mikro nivoju razlikujejo. Na primer, enaki logični elementi imajo različne zakasnitve in drugačno razporeditev silicija. Te razlike so ustvarile koncept fizikalno neklonirane funkcije (PUF). PUF generira vrednosti glede na okolje delovanja. Članek predstavlja obročni oscilator na osnovi PUF v dveh različnih integriranih vezjih za generacijo naključnih števil. Za demonstracijo sta bila uporabljena dva FPGA jedra s PUF strukturami. Za uporabo v aplikacijah so bila naključna števila post procesirana na osnovi Von Neumann študije. Opravljeni so bili tudi avtokorelacijski testi in NIST.

Ključne besede: generacija naključnih števil; FPGA; fizikalno neklonirane funkcije.

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1 Introduction

1.1 Background

The physically unclonable function (PUF) generates a response to the given challenge signals. The basic feature of the PUF is that the generated response is random and unpredictable. In other words, the response is random because the characteristics of the basic hardware (such as LE–Logic Element) used in PUF implementations are different from those of the other structures. Even if a PUF design uses the same challenges, it receives a different response, which indicates that the PUF hardware is unclonable [1].

There are two main implementation categories for PUF: authentication and secret key generation [2]. Au-

thentication is performed in two steps. In the first step, the function generates a response against challenges, and stores it in a database. This phase is called enrolment. The second phase is verification. In this step, the response generated by the PUF for a challenge in the database is compared with the one stored in the database. The secret key generation has two stages: initialization and regeneration. In initialization, responses are generated against challenges, and the same challenge is applied to the PUF in regeneration. In the second phase, a key is generated to create the same response using a hash function and a decoding operation like BHC (Bose–Chaudhuri–Hocquenghem) based on the value generated in the first phase.

There are several PUF structures that have been proposed in the relevant literature. Generally, PUFs are investigated under four groups: arbiter, memory-based, optical, and ring oscillator (RO)-based. The underpinning idea of the arbiter PUFs is to measure the delay times between two signals. The Arbiter PUF structure transmits a pulsing signal to the output via two different routes. There are key blocks such as mux on the route. Although the researcher spent effort to design the two routes symmetrically, the delays in these routes have different times due to the production differences and characteristics. The arbiter gives the output 0 or 1 by examining the route that first sends the pulsing signal [3]. The static random-access memory (SRAM) type PUF is the most common memory-based PUF structure. The SRAM cell outputs consist of two inverters that are parallel to each other. The researcher gave the same characteristics to these inverters to the best ability. Due to manufacturing differences, the output value created by the SRAM cell will be different every time it receives power. These properties enabled SRAM cells to be used as PUF [4]. In optical PUF structure, which is also known as Physical One-Way Functions (POWFs), bubble-filled transparent epoxy is applied on the wafer. The pattern that emerges in this process is polished with laser. Because this pattern depends on the wavelength as well as laser angle, wafer material, wafer thickness and the characteristic of epoxy, each integrator has a unique pattern, and accordingly, a unique identity or signature [1, 5]. The RO-based PUF structure was proposed by Suh et al. [2]. This scheme simply generates a response specific to each challenge input based on the signals addressing the input of delay elements. This difference results from different physical and chemical properties of delay elements that emerge during the production.

It is possible to perform key generation in real random numbers with all PUF structures mentioned above. However, there are certain criteria (e.g. reverse engineering, emulation, man-in-the-middle attack, reconfiguration) that must be satisfied for random key generation to be used in computer science [6]. Past studies have proposed many RO-based PUF structures [6–8]. Indeed, the RO-PUF has very favorable statistical properties (output bias, intra-uniqueness and steadiness) when implemented in both FPGA (Field Programmable Gate Array) and ASIC (Application Specific Integrated Circuit) [7]. A relevant study proposed an RO-based PUF that performed number generation with the help of [9] and Gray coding by counting RO outputs with a counter. There are also other RO-based PUF structures in the literature that aim to increase the quality of random numbers by introducing periodic and non-periodic signals to challenge inputs. Chaos-based maps were used for non-periodic signals while Linear Feedback Shift Register (LFSR) structures were used for periodic signals [6, 10]. In this study, the researcher has suggested an alternative grouping based RO-PUFs for the classic RO-based PUF structure. The output generation mechanism of these systems depends on the frequency order of ROs of a group with two phases [11]. Another study presented a transient effect ring oscillator- (TERO) based PUF structure, and proved that this structure guaranteed high stability [12].

The double PUF structures proposed in the literature are based on arbiter PUF [13-15]. A double PUF structure was proposed to improve the unpredictability of responses [13]. In this study, the researcher used N-XOR Arbiter PUFs for unpredictable structures to sample the numbers from each arbiter PUF output with R-S type flip-flops, and then give them as inputs to an n-input XOR circuit. There were different output functions proposed for n = 2, n = 3 and n = 4 values. Steadiness, randomness, and cost were evaluated for each random number sequence. Another study sampled a double arbiter PUF structure using R-S type flip-flops and gave it as input to a two-input XOR circuit [14]. The difference between this study and the study presented in [13] was that this study applied Von Neumann post-processing to the produced numbers. The study also used Die-hard test suite to measure the randomness of obtained numbers. A previous study [15] suggested a random number generator that had more than two PUF structures. This study has compared the outputs of each PUF circuit in a separate evaluation unit that did not include post processing, and performed number generation.

1.2 Motivation and contribution

This article, unlike the studies in literature, presents a design for random number generation by a RO-based Double PUF structure. The PUF circuits in the proposed structure were implemented on two separate FPGA cores. It is recommended that the characteristics of the Double PUF structure should be investigated so that the generated random numbers can be used as a key.

Thus, researchers should meet the requirements in Table 1. The study administered Diehard, NIST, and FIPS tests in addition to Scale index and autocorrelation to meet these requirements.

In order to meet these requirements, the study applied Von Neumann and hash-based post-processes to the random numbers that were generated by the new structure. The statistical weaknesses of generated numbers were determined by post-processing applications. NIST test suite and autocorrelation coefficients enabled the researcher to examine the quality of the numbers produced in this study. The contributions of this study to the literature are summarized as follows:

- Random number generation with PUF on two different FPGA.
- Transformation of the RO-based PUF structure into Double PUF structure
- Unlike the multi-PUF structures suggested in the literature, Von Neumann and hash-based post-processing procedures were used and the statistical properties of generated numbers were improved.
- Double PUF structure revealed better performance than the PUF structure.

Table 1: The Necessary Security Requirements for The Random Number Generator (RNG)

R1	Random numbers should not show any statistical weakness.
R2	Knowing the sub-array of random numbers should not allow the calculation or estimation of initial and consecutive random numbers.
R3	If the internal state value of the RNG is known, or even if it is unknown, it should not be possible to calculate previous random numbers with the possibility of being estimated.
R4	If the internal state value of the RNG is known, or even if it is unknown, it should not be possible to calculate next random numbers with the possibility of being estimated.

1.3 Study organization

Section 2 presents the basic components for real random number generation and the RO-based PUF structure. The double PUF structure that is proposed in the study as well as its implementation are presented in Section 3 while Section 4 describes the post processing operations. The results of implementation are given in Section 5. In the last section, the researcher evaluated the results.

2 True Random number generation

In real random number generators, random numbers are generated with the help of a physical noise source. The properties and randomness of random numbers generated by true random number generator (TRNG) depend on the randomness of physical processes. The physical noise source is random and its behavior is unpredictable, both of which reveal that the numbers produced are also random and unpredictable. However, the produced bit array may not show high randomness stability, and it may involve statistical weakness. To eliminate these weaknesses and produce more stable random numbers, the study maintained post-processing on the bit array. Post-processing operations reduce the amount of bit and eliminate weaknesses. The disadvantage is that TRNG is slow and costly, and it depends on random noise sources. However, TRNGs are frequently used in key generation because they are unpredictable and non-reproducible, and also achieve good statistical properties required for cryptographic applications [16]. Figure 1 shows the basic structure for generating real random numbers. First, the structure samples the signal obtained from the noise source, and then generates the pure random number by subjecting it to post-processing. Post-processing component is usually benefited to fill the deficiency of DAS(Digitized Analog Signal) in TRNG systems.

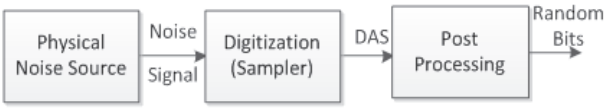


Figure 1: Basic components for TRNG

In RO-based random number generators, the study used propagation delay differences of integrated circuits as the noise source. Figure 2 presents the basic structure of a ring oscillator. RO which consists of an odd number of inverters includes a NAND gate to obtain the delay of the signals given from the input to the output. This structure proposed by Knuth requires a sampling and post processing circuit to produce true random numbers [17]. The quality of random numbers generated by TRNGs depends on the number of oscillators, sampling frequency, and number of inverters in oscillators [17].

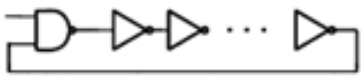


Figure 2: Ring oscillator

Previous studies in the relevant literature proposed RO-featured PUF structures to generate random numbers

[2, 3]. Figure 3 presents the typical RO-PUF content. The system has two 64x1 multiplexers, sixteen counters of 16-bit, one-comparator and one hundred twenty-eight-ring oscillators. Depending on the characteristics of each inverter, such as temperature and propagation delay, inverter outputs have a random quality. Because of these features, ROs create unpredictable variations even when inverters are implemented on the same integrated circuit. If the frequency of RO oscillations is too high, counters may not count oscillations. For this reason, it is necessary to adjust the number of inverters in each RO to ensure proper oscillation frequency. In the RO-PUF design, the frequencies of the output signals with each multiplexer's challenge can be set f_1 and f_2. The oscillation numbers of these frequencies are counted by the *counter*$_1$ and the *counter*$_2$ in the system. As a result of counting, the comparison circuit generates 0 or 1 according to Eq.1 [18].

$$r_{ab} = \begin{cases} 1 & if\ f_1 > f_2 \\ 0 & otherwise \end{cases} \quad (1)$$

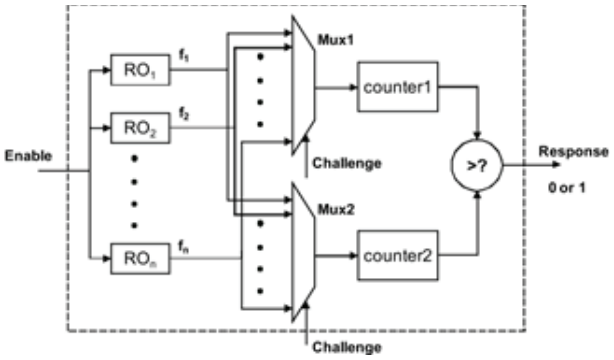


Figure 3: RO-PUF structure

3 Proposed double RO-PUF and implementation

Among all the PUF types, an RO-based PUF structure is most suitable for implementation on an FPGA [17]. Ring oscillator design with inverter and nand gate elements was presented by Sunar el al. Ring oscillators developed for random number generation consist of one NAND gate and 13 inverters. The number of inverters set to 13 so that the entropy of the numbers generated in their designs is high [19]. The 13th inverter output is given to the NAND gate as an input by feedback. The first input of the NAND gate is driven by a multiplexer hardware. With an externally applied excitation signal to the multiplexer's challenge, the RO output becomes a square wave signal. Figure 4 presents the design of a ring oscillator (in a RO-based PUF structure that was explained in Figure 3) in an FPGA environment. Because the propagation delays of the inverters used in each RO are different, each RO output generates a signal at different frequencies. Previous studies implemented the RO-based PUF using 64 or 128 RO. The present study sent the signals obtained from ROs to Mux inputs. The select inputs of the mux are given signals called challenge. The numbers are counted by counters, and the generation of random numbers is completed with a simple comparison.

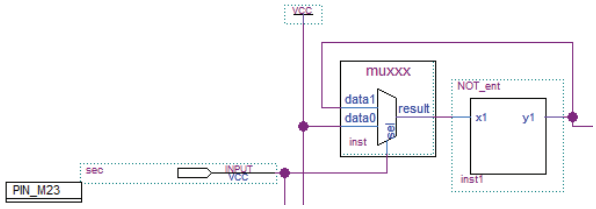
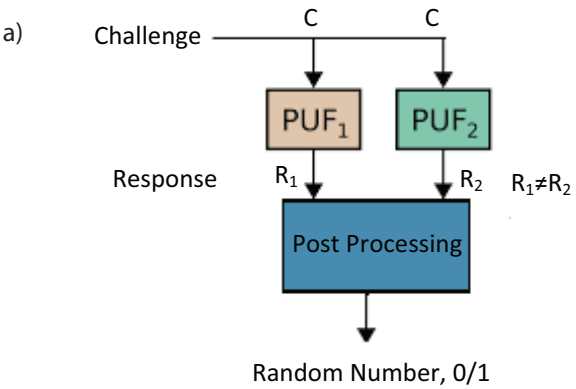


Figure 4: Implementation of RO in the FPGA

In this study, random number generation was implemented in real time using the RO-PUF structure that is described above in general. The proposed system in this study includes two RO-based PUF structures, as shown in Figure 5.a. Each RO-based PUF contains 64 RO and 64x1 Mux as shown in figure 5. b. Each RO-based PUF was implemented on EP4CE115FC7 and EP4CE22 FPGA cores.



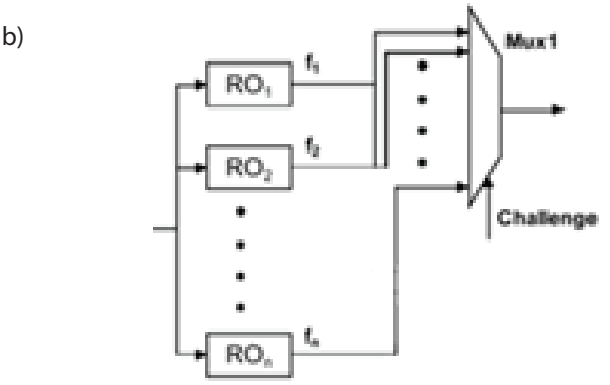


Figure 5: a) The suggested structure b) The PUF1 structure

The frequency of the signals given to challenge inputs enabled sampling the numbers that each PUF would generate at the f_1 and f_2 frequencies. The signals given to the challenge inputs act as the LFSR structures with the characteristic equation $x^{15}+x+1$. The obtained numbers were subjected to post-processing to strengthen their statistical properties and use them as a key. The study administered Von Neumann and hash-based post processing to achieve this goal. The new structure proposed in this study is simple, but very effective. Although the same challenge signals are given to each PUF structure, they produced different responses. The reason of this difference is the chemical properties (e.g. the properties of germanium and silicium elements, and the changes of their atoms in the cubic lattice structure) and the physical properties during integration of the logic elements (the geometry of transistors, oxide thickness, width) that are the main elements of the FPGA hardware.

The researcher recorded the generated numbers in the memory circuit to determine their statistical properties. Also, the system used a 16-bit counter to write the generated numbers on each address of the memory. In each sampling operation, the counter shows the next address of the memory, and a random number is recorded into this address. The sampling frequency and counter frequency in the system were 50 MHz for each. Quartus software allows the system to save the numbers in the memory units into a file with the mif or hex extension. The numbers were recorded in a file with the mif extension. Thus, is was an easy procedure to calculate the statistical properties of these numbers. Figure 6 shows the designed memory hardware.

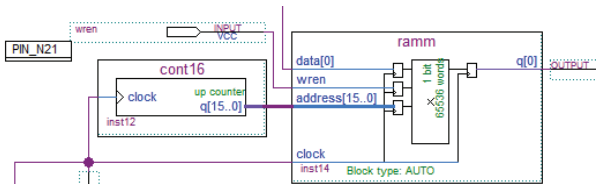


Figure 6: Recording of generated number into the memory unit

4 Post processing

4.1 Von Neumann Post Processing

Post-processing is the oldest and simplest method to eliminate the irregularities in the generated number array. The number generators to which Von Neumann post processing method is applied can generate normally distributed 0 and 1 numbers. The researcher took into consideration the simultaneous pairs that were generated in this post-processing method. If the number is (1, 0), the system generates 1. On the other hand, it generates 0 when the number is (0, 1). (0, 0) and (1, 1) number arrays are ignored. Figure 7 presents the application of Von Neumann post-processing to the generated random numbers. The entropy of the numbers created by this operation is close to the ideal value. However, this method has a disadvantage, which is the slow rate of number generation due to the elimination of the produced bit arrays.

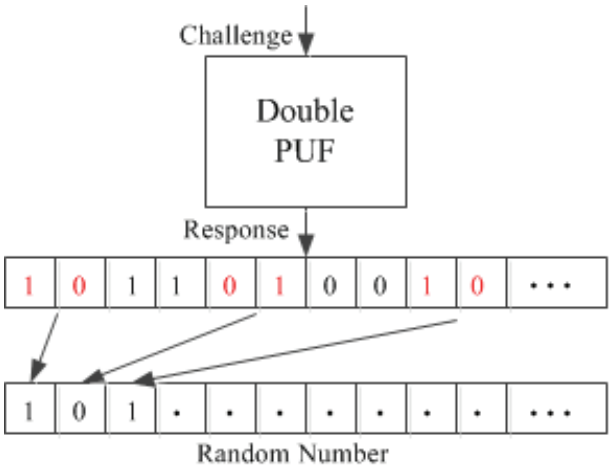


Figure 7: Von Neumann post-processing

4.2 Hash-based Post-processing

The H function is based on XOR gate and a post-processing that achieves more successful results than the XOR. It processes randomly-generated numbers in groups of 16 bits with a base of 2. It subjects the first 8 bits of each 16 bits to the XOR processing. The first eight bits are shifted one left. The result of this operation is subjected to the XOR with the last 8 bits. These operations produce an 8-bit output.

The generated number array for post-processing can be accepted D_0, D_1... D_{15} and considered 16 bit. Then, 16 bit is divided into two blocks; the first 8 bit being A_1 while the last 8 bit being A_2. The A_1 number array is subjected to the XOR by shifting the A_1 by one bit to the left. The resultant array is subjected the XOR with the A_2 number array and the number generation is achieved. Eq.2 shows the hash function.

H(A1,A2)=XOR(XOR(A1,rotateleft(A1,1)),A2) (2)
D=0110111011110100,
A1=01101110, A2=11110100
rotateleft(A1,1)=11011100,
H(A1,A2)= ((11011100 XOR 01101110) XOR 11110100)=
01000110

Figure 8 demonstrates the implementation of Hash post-processing function. The example in this section decreases the number generation rate by 50% with the hash function post-processing.

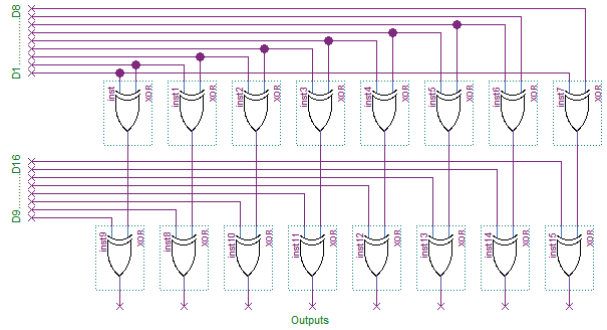


Figure 8: The post-processing of the H function

5 Implementation results

The new double RO-based PUF structure proposed in this study is capable of generating infinite random numbers. The generated numbers were stored in the memory to determine their statistical properties. Figure 9 shows the real-time generated numbers that are stored in the memory as a result of the hash-based post-processing while Figure 10 shows the actual numbers obtained from the output of the memory hardware.

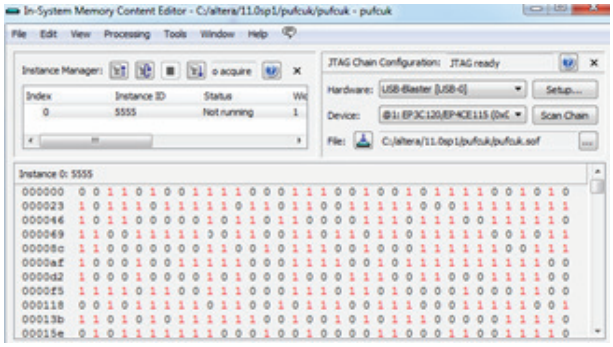


Figure 9: Real-time generated numbers stored in the memory

Figure 11 shows the resource utilization report obtained for the PUF1 implemented in the FPGA. The total numbers of LUTs consumed are 1110. Table 2 shows the comparison of the proposed approach with the literature according to FPGA resource utilization. The resource consumption of the proposed method according to the table.2 is acceptable average level.

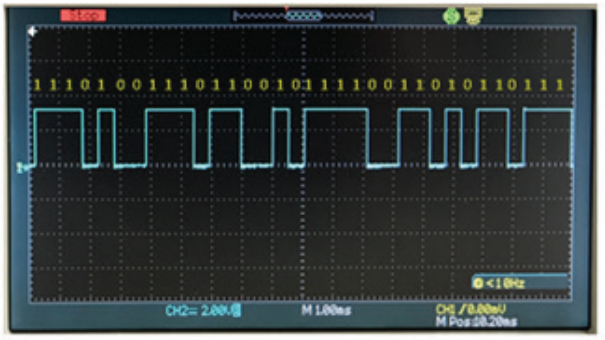


Figure 10: The numbers obtained from memory output

Logic element usage by number of LUT inputs	
-- 4 input functions	226
-- 3 input functions	133
-- <=2 input functions	196

Figure 11: FPGA resource utilization of PUF1

Table 2: FPGA resource utilizations

Reference	Type	FPGA resource utilization
[20]	RO PUF	4096 LUTs
[21]	LUT based on PUF	1280 LUTs
[22]	Arbiter PUF	1428 LUTs
[23]	RO PUF	1288 LUTs
[24,26]	SR Latch PUF	1024 LUTs
[25]	SR Latch PUF	2048 LUTs
[27]	RO PUF	732/1084/1436 LUTs
[28]	RO PUF	1024/1280/2048/ 2560 LUTs
Proposed Double PUF	RO PUF	1110 LUTs

The study investigated the statistical properties of the numbers generated by both Von Neumann and hash-based post-processing according to NIST test suite. P-value is known as randomness measure in the NIST Test suite. If P-value is 0, numbers are not random at all. it is desirable that this value is greater than 0.01 in computer science. With the proposed system according to Table 3, random numbers have produced.

Table 3: The results obtained according to NIST test suite

	Von Neumann	Hash	Raw bits
Frequency Monobit Test	0.715	0.0458	Failure
Frequency Test with a Block	0.709	0.478	Failure

Runs Test	0.141	0.964	Failure
Longest Run of Ones in a Block	0.285	0.715	Failure
Binary Matrix Rank	0.826	0.229	0.642
Discrete Fourier Transform	0.516	0.433	Failure
Non-Overlapp. Temp. Matching	0.611	0.622	Failure
Overlapping Template Matching	0.208	0.738	Failure
Universal Test	0.214	0.696	Failure
Linear Complexity	0.606	0.905	0.393
Serial Test	0.792	0.271	Failure
Approximate Entropy	0.137	0.33	Failure
Cumulative Sum	0.929	0.073	Failure

Moreover, the numbers generated by these procedures were subjected to autocorrelation test. Correlation indicates a linear relationship between two or more variables, and takes values between +1 and −1. If it is equal to or close to 0, there is no linear relationship between the variables. The purpose of this test is to control the correlation between the produced bit array bi and its shift version. When *n* has bit array length, *d* will be a constant integer and $1 \le d \le (n/2)$. The mathematical definitions of the test are given in Eq.3 and 4 [14].

$$A(d) = \sum_{i=1}^{n-d-1} b_i \, xor \, b_{i+d} \tag{3}$$

$$X_5 = \frac{2A(d) - (n-d)}{\sqrt{n-d}} \tag{4}$$

If $\{b_i\}$ is a real random array and $n \to \infty$, this random variable has a normal distribution $N(0, 1)$. If $|X5| < 1.6449$ ($\alpha = 0.05$), then the test is successful. Table 4 shows the autocorrelation test results.

Table 4: Autocorrelation Test Results

	d	Double Puf	Result
Autocorrelation	8	0.0249	Passed
	10	0.0316	Passed

6 Conclusion

It is important to use random numbers in authentication and secret key generation. PUF structures are used for low-cost authentication and in the key generation for symmetric and asymmetric encryption. In such applications, random numbers that are generated for key and authentication are the most important parameters that determine the security of the application. With these issues in mind, we proposed a double PUF structure in this study, which is a unique structure in the relevant literature. We used RO-based PUF content for the new structure because it was suitable for being implemented on FPGA. The system was implemented on two different FPGA cores that were manufactured with 65 nm technology. Used FPGA boards have different characteristics because of core manufacturing conditions. In this case, the proposed system will not be cost-effective. To overcome this disadvantage, we suggest that the system should be implemented with two different cores on a single integrated circuit. The study employed Von Neumann and hash-based post-processing to remove the bit irregularities in the generated random numbers. The statistics of the numbers proved that they were successful with both pre-treatments. Considering the features of the PUF structure and its success in statistical tests, the study concluded that the new structure can be used in key generation and authentication applications.

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Arrived: 06. 01. 2018
Accepted: 29. 05. 2018

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 48, No. 2(2018), 129 – 132

Doktorske disertacije na področju mikroelektronike, elektronskih sestavnih delov in materialov v Sloveniji v letu 2017

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Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
ISSN 0352-9045

Publisher / Založnik:
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Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia
Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, Ljubljana, Slovenija

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