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Relative appraisal of Ultra-Thin Body MOSFETs: An analytical modeling including hot carrier induced degradation

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Abstract: This paper focuses on the physics and modeling of nanoscale ultra-thin body (UTB) single gate (SG) and double-gate (DG) Metal Oxide Field-Effect Transistors (MOSFETs). An analytical modeling for surface potential and threshold voltage of Fully Depleted (FD) DG-MOSFET is proposed by solving the 2-D Poisson's equation. The degradation due to the hot carrier effect, is investigated in short-channel devices. The parabolic potential approximation is utilized to solve 2D Poisson's equation in the channel region. The developed surface potential model includes the effect of both positive as well as negative interface charges. The calculated minimum surface potential is used to develop the threshold voltage model. Based on the model, the interdependence of the device parameters, such as the silicon film thickness (t_{si}), oxide thickness (t_{ox}), channel length (L) are investigated in this paper. A conventional enhancement type n-MOSFET has been studied by developing an analytical model and checking its validity with numerical simulator Sentaurus, by Synopsis Inc.

Keywords: Ultra-Thin Body (UTB) MOSFET; Surface Potential; Threshold Voltage; Short Channel Effects (SCEs); hot carriers; trap charge

Relativna ocean ultra tankih MOSFET: Analitično modeliranje z upoštevanjem degradacije zaradi vročih nosilcev

Izvleček: Članek se osredotoča na modeliranje in delovanje ultra tankih eno- (SG) ali dvo-vratnih (DG) MOSFET tranzistorjev. Na osnovi reševanja 2D Poissonove enačbe je opravljeno analitično modeliranje površinskega potenciala in pragovne napetosti popolnoma osiromašenega DG_MOSFET tranzistorja. Vpliv degradacije zaradi vročih nosilcev je obravnavan na elementih s kratkimi kanali. Za reševanje Poissonove enačbe je uporabljena parabolična aproksimacija potenciala, ki upošteva tako pozitivne, kakor tudi negativne naboje. Minimalen površinski potencial je uporabljen za izračun pragovne napetosti. Obravnavana je povezanost parametrov, kot je debelina oksida, dolžina kanala in debelina silicijeve plasti. N-MOSFET tranzistor je bil simuliran z numeričnim simulatorjem Sentaurus

Ključne besede: ultra tanki (UTB) MOSFET; površinski potencial; pragovna napetost; vpliv kratkih kanalov; vroči nosilci; naboj pasti

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1 Introduction

CMOS devices come to nanoscale regime to acquire higher density and performance and lower power consumption. The inauspicious effects cause threshold voltage variation with higher leakage current in short devices known as short channel effects (SCEs). Due to these SCEs the conventional scaling comes to an end, but to maintain the Moore's law research going towards inventions of novel devices[1–4].

The predictions of International Technology Roadmap for Semiconductors (ITRS) are followed by the device designers to propose various novel device structures and process parameter variations [5]. Non classical silicon MOS structures, such as FinFETs, are replacing the conventional bulk MOS devices because of their capability to attain higher speeds and reduced short channel effects (SCEs) with the added advantage to design highly integrated CMOS circuits[6–9].

For the modern short channel devices, the electric field under the gate oxide can no longer be treated in a single direction. In addition, the velocity of the carriers drifting between the channel and the drain saturates. This result in reduction in electron and hole mobility and thus an increase in effective sheet resistance [10]. The mobility enhancement can be possible through concepts like undoped channel and strained channel etc. [11], [12].

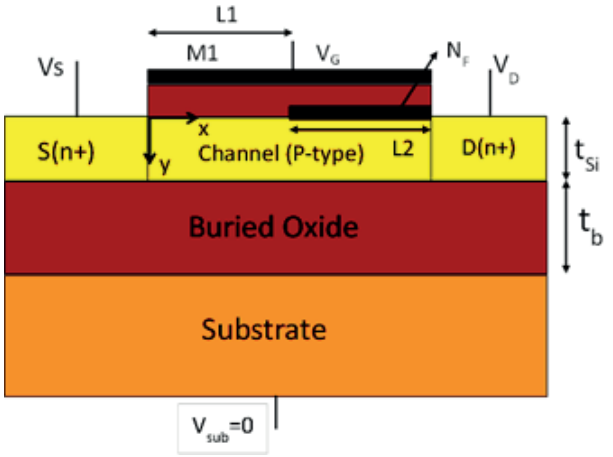
Further the generated hot carriers due to higher electric field may also be trapped in the oxide region of MOSFETs, leading to interface-trap buildup and the trapping of carriers in the oxide. Thus, trapped charges in the oxide region of MOSFETs change the potential profile of the channel and have adverse effects like shifting the threshold voltage. They may compromise operation of the device by generating charged defects in the oxide layer, and by degrading the oxide and the Si-SiO_2 interface. These effects constitute a reliability problem. Hot carriers also generate unwanted current components. Hence, analysis of hot carriers becomes one of the most crucial tasks [13],[14].

This paper presents an analytical model of surface potential, electric field and threshold voltage for short-channel Ultra-Thin Body (UTB) symmetrical Double-Gate (DG) MOSFETs including the effects of the interface charges. The parabolic potential approximation method is utilized while solving the two-dimensional (2D) Poisson's equations along with the assumption that the interface charge distribution is uniform along the channel [3], [15], [16]. The simulation results from Sentaurus are utilized to verify the obtained model.

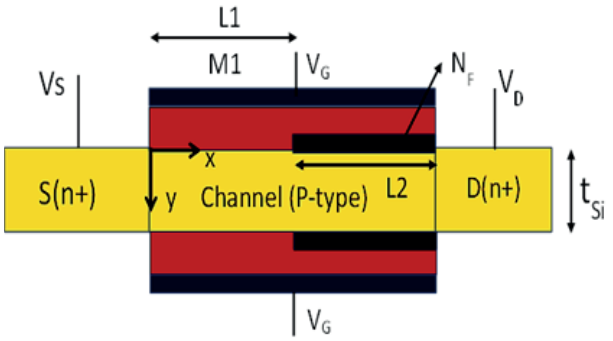
2 Device structure

The schematic diagram of the ultra-thin body (UTB) single gate (SG) and double-gate (DG) MOSFET structures are used for modeling and simulation as shown in Fig. 1. The device has uniformly doped source–drain with doping concentration of $N_D = 1\times 10^{20}$ cm^{-3}. The channel is kept lightly doped with doping concentration of $N_A = 1\times 10^{16}$ cm^{-3}. The gate oxide thickness, buried oxide thickness and the silicon are $t_{ox} = 2$ nm $t_b = 50$ nm and $t_{Si} = 10$ nm, respectively. Damaged region due to the interface oxide traps charges (N_F) is shown in Fig. 1 with black line and labeled as distance $L2$.

The gate length (L=$L1$+$L2$) is divided into two parts to identify the damaged length $L2$. The work function of the gate material is: ϕ_{M1} = 4.6 eV (e.g., Mo). The simulation is carried out by the device simulator Sentaurus, a 2-D numerical simulator from Synopsis Inc. [17]. To



(a)



(b)

Figure 1: Schematic Structure of UTB (a) Single Gate and (b) Double Gate, Fully Depleted Silicon on Insulator MOSFET with Damaged Region

study the surface potential along the channel we have taken the cutline at the surface of the channel and across the thickness of channel of the device. To obtain accurate results for MOSFET simulation we need to account for the mobility degradation that occurs inside inversion layers. The drift-diffusion model which is the default carrier transport model in Sentaurus device is applied. The basic mobility model is used, that takes into account the effect of doping dependence, high-field saturation (velocity saturation), and transverse field dependence. The impact ionization effects are ignored. The silicon band gap narrowing model that determines the intrinsic carrier concentration is also included in simulation. The solution of the device equations are done self-consistently, on the discrete mesh, in an iterative fashion. For each iteration, an error is calculated and device attempts to converge on a solution that has an acceptably small error. The Poisson equation, continuity equations, and the different thermal and energy equations are included in simulation. [17]. All the structure junctions assumed as abrupt, and the biasing conditions considered at room temperature in the simulation.

3 Analytical Model Formulation

3.1 Surface Potential Formulation

Flat band voltage (front channel)

$$(V_{FB,f})_{si} = \phi_M - \phi_{si} \quad (1)$$

where $\phi_{f-Si} = V_T \ln(N_a/n_i)$, $\phi_{Si} = \frac{\chi_{si}}{q} + \frac{E_{g,Si}}{2q} + \phi_{f-Si}$

Back channel flat band voltage (back channel)

$$(V_{FB,b})_{si} = \phi_{sub} - \phi_{si} \quad (2)$$

where $\phi_{sub} = \frac{\chi_{si}}{q} + \frac{E_{g,Si}}{2q} + \phi_{f-sub}$, $\phi_{f-sub} = V_T \ln(N_{sub}/n_i)$

Built in voltage across source-body and drain body junction

$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \phi_{f-Si} \quad (3)$$

Considering the effect of oxide charges in the Si-SiO_2 interface, 2-D Poisson's equation for the potential distribution in the silicon regions can be written as [18]:

$$\frac{\partial^2\phi_1(x,y)}{\partial x^2} + \frac{\partial^2\phi_1(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}} \text{ for } 0 \le x \le L_1, 0 \le y \le t_{Si} \quad (4)$$

$$\frac{\partial^2\phi_2(x,y)}{\partial x^2} + \frac{\partial^2\phi_2(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}} \text{ for } L_1 \le x \le L, 0 \le y \le t_{Si} \quad (5)$$

The potential profile in the vertical direction can be approximated by a parabolic function

$$\varphi_1(x,y) = \phi_{s1}(x) + a_{11}(x)y + a_{12}(x)y^2 \text{ for}$$
$$0 \le x \le L_1, 0 \le y \le t_{Si} \quad (6)$$

$$\varphi_2(x,y) = \phi_{s2}(x) + a_{12}(x)y + a_{22}(x)y^2 \text{ for}$$
$$L_1 \le x \le L, 0 \le y \le t_{Si} \quad (7)$$

Poisson's equation can be solved by following the boundary condition

1. Electric flux(displacement) at the gate oxide/ strained Si film interface is continuous

$$\left.\frac{d\varphi_1(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s1}(x) - V'_{GS1}}{t_f} \quad (8)$$

$$\left.\frac{d\varphi_2(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s2}(x) - V'_{GS2}}{t_f} \quad (9)$$

where $V'_{GS1} = V_{GS} - (V_{FB1,f})_{si}$, $V'_{GS2} = V_{GS} - (V_{FB2,f})_{si}$

and the effect of trapped charges are to be considered as

$$(V_{FB1,f})_{si} = \phi_M - \phi_{si}, \; (V_{FB2,f})_{si} = \phi_M - \phi_{si} - \frac{qN_f}{C_{ox}}$$

2. Electric field at the interface of the buried oxide and the back channel is continuous

$$\left.\frac{d\varphi_1(x,y)}{dy}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{-\phi_B(x) + V'_{SUB}}{t_b} \quad (10)$$

$$\left.\frac{d\varphi_2(x,y)}{dy}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{-\phi_B(x) + V'_{SUB}}{t_b} \quad (11)$$

Where $V'_{SUB} = V_{SUB} - (V_{FB,b})_{si}$

3. Electric flux (displacement) and the electric potential at the trapped charged interface is continuous

$$\left.\frac{d\varphi_1(x,y)}{dx}\right|_{x=L_1} = \left.\frac{d\varphi_2(x,y)}{dx}\right|_{x=L_1} \quad (12)$$

$$\phi_1(L_1,0) = \phi_2(L_1,0) \quad (13)$$

4. The surface potential at the source end is

$$\phi_1(0,0) = \phi_{s1}(0) = V_{bi,si} \quad (14)$$

5. The surface potential at the drain end is

$$\phi_2(L,0) = \phi_{s2}(L) = V_{bi,si} + V_{DS} \quad (15)$$

Using the boundary conditions (8)-(11) we obtain coefficients and obtain the expressions for $\phi_1(x,y)$ and $\phi_2(x,y)$. Substituting $\phi_1(x,y)$ and $\phi_2(x,y)$ into (4) and (5) respectively and subsisting y=0 we obtain

$$\frac{d^2\phi_{s1}(x)}{dx^2} - \alpha\phi_{s1}(x) = \beta_1 \quad (16)$$

$$\frac{d^2\phi_{s2}(x)}{dx^2} - \alpha\phi_{s2}(x) = \beta_2 \quad (17)$$

where $\alpha = \frac{2(C_f C_{Si} + C_f C_b + C_b C_{si})}{t_{si}^2 C_{si}(2C_{si} + C_b)}$,

$$\beta_1 = \frac{qN_A}{\varepsilon_{si}} - 2V'_{GS1}\frac{C_f(C_{si} + C_b)}{t_{si}^2 C_{si}(2C_{si} + C_b)} - 2V'_{SUB}\frac{C_b}{t_{si}^2 C_{si}(2C_{si} + C_b)},$$

$$\beta_2 = \frac{qN_A}{\varepsilon_{si}} - 2V'_{GS2}\frac{C_f(C_{si}+C_b)}{t_{si}^2 C_{si}(2C_{si}+C_b)} - 2V'_{SUB}\frac{C_b}{t_{si}^2 C_{si}(2C_{si}+C_b)}$$

The solution for (16) and (17) are simple second order non-homogenous differential equation with constant coefficients which can be expressed as

$$\phi_{s1}(x) = A\exp(nx) + B\exp(-n*x) - \frac{\beta_1}{\alpha} \quad (18)$$

$$\phi_{s2}(x) = C\exp(n(x-L_1)) + D\exp(-n(x-L_1)) - \frac{\beta_2}{\alpha} \quad (19)$$

where $n = \sqrt{\alpha}$, $p_1 = \frac{\beta_1}{\alpha}$, $p_2 = \frac{\beta_2}{\alpha}$

Using the boundary condition (15)-(18) we solve for A, B, C, and D

$$A = ((V_{bi,si}(1-\exp(-nL)) + V_{DS} + (p_1 - p_2)\cosh(nL_2) + p_2 - p_1\exp(-nL))/(2\sinh(nL)) \quad (20)$$

$$B = ((V_{bi,si}(\exp(nL)-1) + p_1\exp(nL) - p_2 - V_{DS} - (p_1 - p_2)\cosh(nL_2))/(2\sinh(nL)) \quad (21)$$

$$C = A\exp(nL_1) + \frac{p_2 - p_1}{2} \quad (22)$$

$$D = B\exp(-nL_1) + (\frac{p_2 - p_1}{2}) \quad (23)$$

3.2 Electric field formulation

Electric field horizontal component under metal gates M1/M2 can be expressed as

$$E_1(x) = An\exp(nx) - Bn\exp(-nx) \quad (24)$$

$$E_2(x) = Cn\exp(n(x-L_1)) - Dn\exp(-n(x-L_1)) \quad (25)$$

The minimum potential of front channel can be expressed as

$$x_{\min} = \frac{1}{2n}\ln(\frac{B}{A}) \quad (26)$$

$$\phi_{s,\min} = 2\sqrt{AB} - p_1 \quad (27)$$

3.3 Threshold Voltage Formulation

For strained-Si SOI MOSFET the threshold condition under the front gate is modified as

$$\phi_{s,\min} = \phi_{th} = 2\phi_{f,si} \quad (28)$$

$$V_{TH} = \frac{-\eta + \sqrt{\eta^2 - 4\sigma\xi}}{2\sigma} \quad (29)$$

Where $\gamma = \exp(-nL)$, $\sigma = \frac{1}{\gamma} + \gamma - 2 - \sinh^2(nL)$,

$$V_{bi1} = V_{bi,si}(1-\gamma) + V_{DS} - (u-v)\cosh(nL_2) - v + u\gamma$$

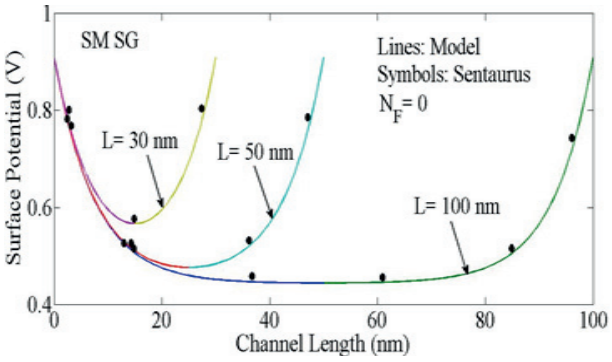
$$V_{bi1} = V_{bi,si}(1-\gamma) + V_{DS} - (u-v)\cosh(nL_2) - v + u\gamma$$

$$u = \frac{C_b}{C_f}V'_{SUB} - \frac{qN_A t_{si}}{C_f} - V_{FB1,si},\ v = \frac{C_b}{C_f}V'_{SUB} - \frac{qN_A t_{si}}{C_f} - V_{FB2,si}$$

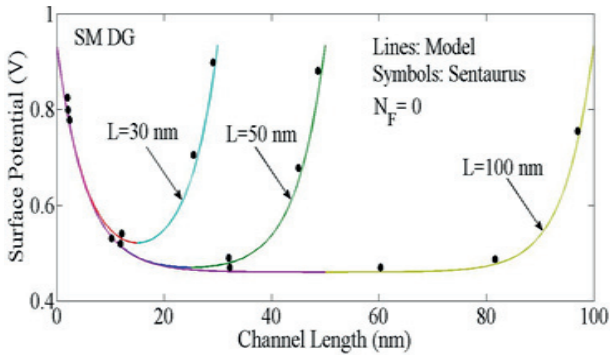
$$\xi = V_{bi1}V_{bi2} - \sinh^2(nL)(\phi_{th} - u)^2,$$

$$\eta = V_{bi1}(-\frac{1}{\gamma} + 1) + 2\sinh^2(nL)(\phi_{th} - u) - V_{bi2}(1-\gamma)$$

4 Results and Discussion



(a)

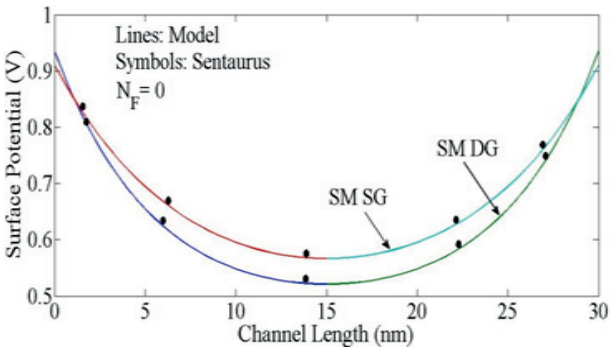


(b)

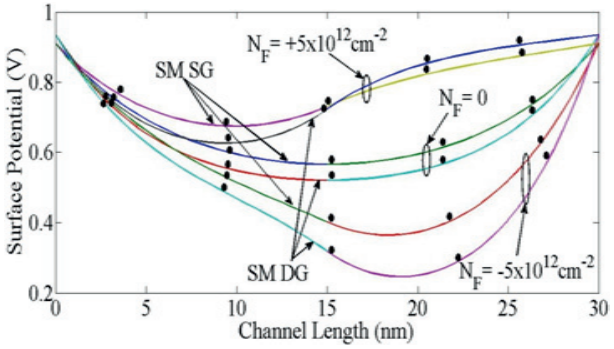
Figure 2: Variation of Surface potential for different channel length (a) Single Gate and (b) Double Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, L=30, 50, 100 nm, t_{ox}=2 nm, V_{DS}=0 V and V_{GS}=0.1 V, N_F =0.

In this section, results obtained from theoretical models of the surface potential, electric field and threshold voltage are compared with the numerical simulation

results. A systematic comparison is made among UTB SG and DG SOI MOSFETs with considering the Si-SiO_2 interface trap charges. Fig. 2 demonstrates the surface potential curve for both SG and DG devices for different values of the channel lengths. From the figure, as channel length decreases, the height of potential barrier increases resulting undesirable short channel effects (SCEs). However, if one closely analyze the Fig. 2(a) and (b), it can be seen that the DG device is less susceptible for SCEs than SG. Fig. 3(a) shows an analogy of surface potential between SG and DG by maintaining all the parameters at constant value. Form the figure it can be clear that the DG device has more control over the channel as compare to SG device. This is because of two gates i.e. front and back gates in case of DG.



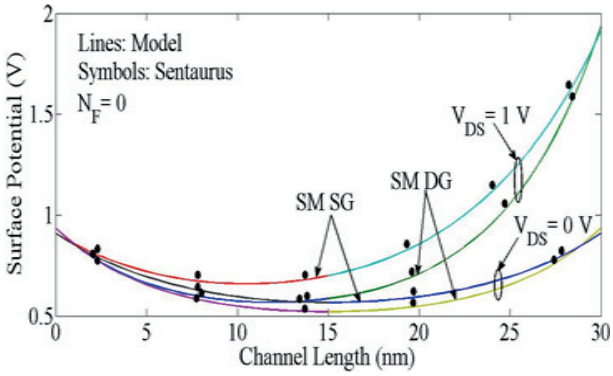
(a)



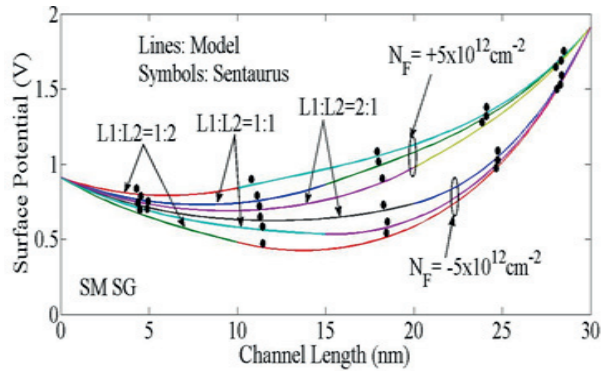
(b)

Figure 3: (a) Comparison of Variation of Surface potential for Single Gate and Double Gate, (b) Variation of Surface potential for different trapped charge for Single Gate and Double Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, L=30 nm, t_{ox}=2 nm, V_{DS}=0 V and V_{GS}=0.1 V.

Fig. 3(b) shows the surface potential variation along the channel length for different amount and polarity of interface trapped charges in the oxide for SG and DG. From the figure, the minimum of the surface potential is at the channel center for device having N_F=0 and is moving towards the source and drain side, for positive and negative interface charge cases, respectively. Positive interface charge will cause higher SCEs on the device than its counterparts due to lower barrier height. However, device having negative interface charges will cause more drain induced barrier lowering (DIBL) as the minimum potential point shifts towards the drain side. So both positive and negative interface charges are undesirable for the device performance. It can be observed that DG device has higher barrier height with less prominent to interface trap charges.



(a)

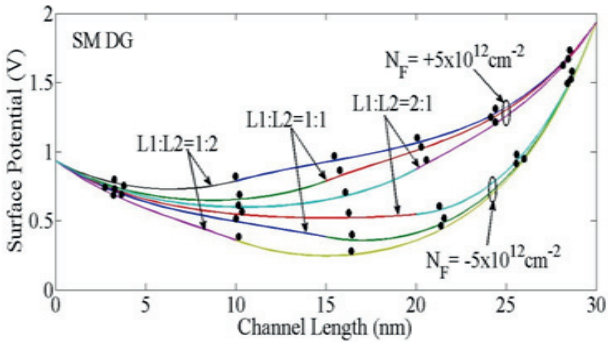


(b)

Figure 4: (a) Variation of Surface potential for different V_{DS} for both Single Gate and Double Gate. (b) Variation of Surface potential for different damaged region length ratios of Single Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, t_{ox}=2 nm, L=30 nm and V_{GS}=0.1 V.

Fig. 4(a) demonstrates the surface potential curve along the channel length for various values of the drain voltage for both SG and DG. Because of the presence of two gates (DG), the variation of channel potential under the undamaged region with respect to drain voltage is much smaller than in SG. As a consequence, V_{DS} has only a small influence on drain current after saturation. Also due to two gates, the variation of channel potential minima with respect to drain voltage is much smaller than SG which minimizes the DIBL effect. Fig. 4(b) depicts the surface potential with the metal gate length ratio variations for different ratio of undamaged ($L1$) and damaged ($L2$) channel length distances,

considering positive and negative charges in the oxide interface for SG device. As seen from the figure in case of positive interface charges, the increase in the length of damaged region i.e. *L*2, raises the minimum surface potential and shifts it towards the source side. The position of the minimum surface potential is closer to source for a greater length of *L*2. This indicates a higher SCE in the device as the *L*2 extends more. This will further lower the source channel barrier height and hence a higher threshold voltage roll-off. However, in case of negative interface charges, the increase of the length of *L*2 region decreases the minimum surface potential. This will give a higher source-channel barrier height and hence a lower threshold voltage roll-off. The shifting of the minimum surface potentials is opposite as that of in the positive interface charge case i.e. the minimum surface potential point shifts towards drain side as *L*2 length decreases. Similar analysis can be predicted from Fig. 5(a) in case of DG.



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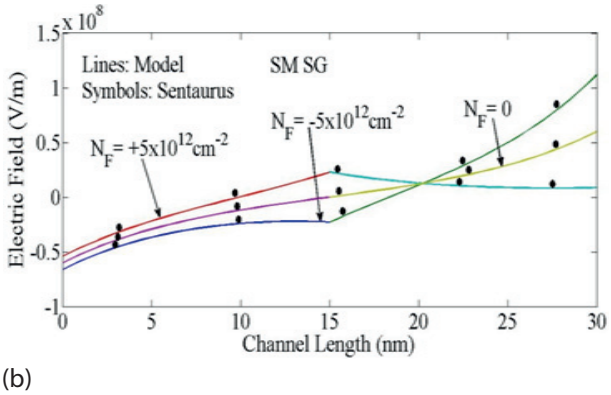
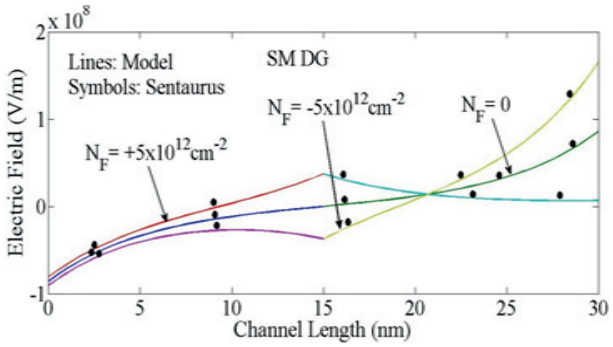


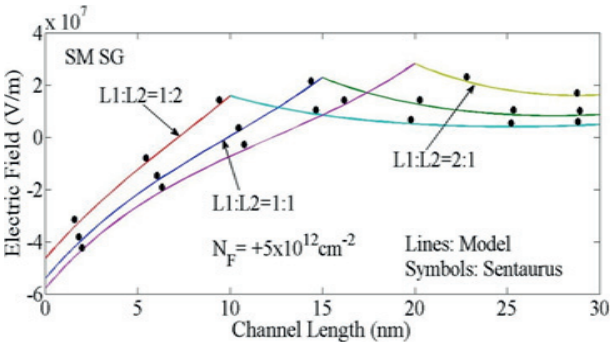
(b)

Figure 5: (a) Surface Potential variation along the channel length for interface charge variations for different damaged region length ratios (*L*1/*L*2=1:2, 1:1, 2:1) of Double Gate device. (b) Electric Field variation along the channel length for interface charge variations of Single Gate device. Parameters used are ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, *L*=30 nm, t_{ox}=2 nm, V_{DS}=1 V and V_{GS}=0.1 V.

Fig. 5(b) shows the variation of the electric field distribution along the channel for different amounts and polarity of interface trapped charges in the oxide for SG case. From the figure, the inflection point of the electric field lies at the interface of the damaged and undamaged regions. The device having positive interface charge will give maximum electric field peak as compare to N_F=0 and N_F negative cases. So, positive interface charge case will cause higher short channel effect on the device than its negative charge counterparts due to high electric field. Similar analogy can be forecast for DG device from Fig. 6(a). However, one can observe a lower electric field in case of DG from SG by comparing the Fig. 6(b) and Fig. 6(a).



(a)

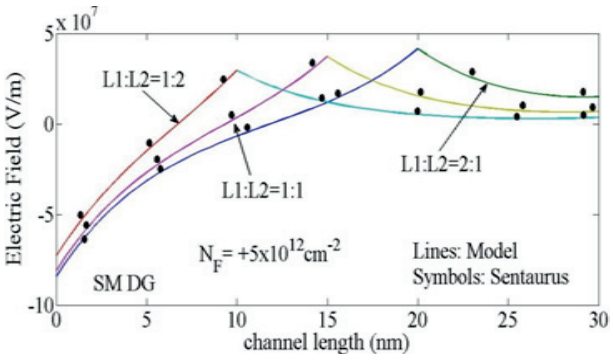


(b)

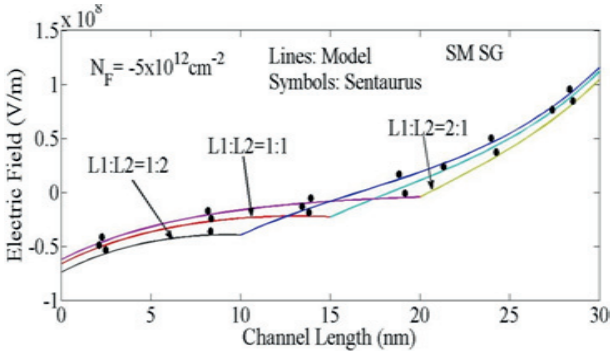
Figure 6: (a) Electric Field variation along the channel length for interface charge variations of Double Gate. (b) Electric Field variation along the channel length for different damaged region length ratios (*L*1/*L*2=1:2, 1:1, 2:1) of Single Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, *L*=30 nm, t_{ox}=2 nm, V_{DS}=1 V and V_{GS}=0.1 V.

Fig. 6(b) shows the variation of horizontal electric field of the UTB-SG SOI MOSFET for different gate length ratios by considering positive interface charges. The point of maximum barrier lies at the intersection point of the damaged and undamaged regions. As length *L*2 decreases or the *L*1/*L*2 ratio increases, the point of peak electric field at the interface is shifted towards the drain side. This causes a higher carrier drift velocity and device speed. The carrier transport efficiency increases with decreasing *L*2, which causes a reduction in hot

carrier effect (HCE) and improvement in DIBL. In case of DG, the Fig. 7(a) can be referred for analysis purpose. Fig. 7(b) and Fig. 8(a) show the variation of the electric field distribution along the channel for different gate length ratios by considering negative interface trapped charges in the oxide for SG and DG device, respectively. From both the figures, as the length of damaged region i.e. *L*2 decreases, the peak of the electric field shifted towards the drain side. By comparing between positive and negative interface charge cases, the device having positive interface charge will give maximum electric field peak as compare to N_F=0 and N_F negative cases. So, positive interface charge case will cause higher short channel effect on the device than its negative charge counterparts due to high electric field. Fig. 8(b) shows the threshold voltage variation along the channel length for N_F=0, negative and positive in the oxide for SG device. From the figure, the threshold voltage is higher in case of negative N_F and it is lower for positive interface charge case. This is due to the lower barrier height in case of positive interface charge as discussed in Fig. 3(b). So, the device having positive interface trap charges are more susceptible to short channel effects.

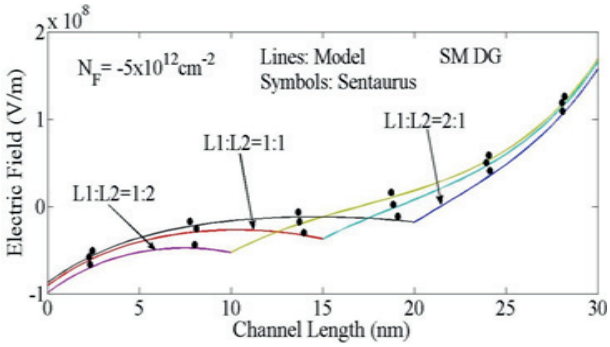


(a)

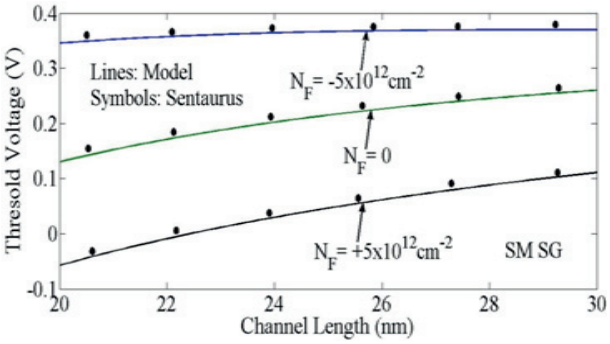


(b)

Figure 7: (a) Electric Field variation along the channel length for different gate length ratios (*L*1/*L*2=1:2, 1:1, 2:1) of Double Gate. (b) Electric Field variation along the channel length for different gate length ratios (*L*1/*L*2=1:2, 1:1, 2:1) for negative trap charge of Single Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, *L*=30 nm, t_{ox}=2 nm, V_{DS}=1 V and V_{GS}=0.1 V.



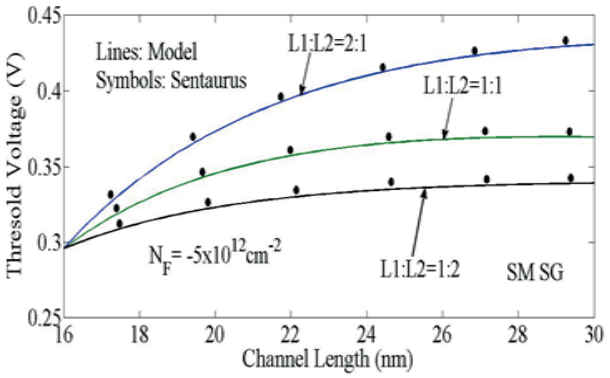
(a)



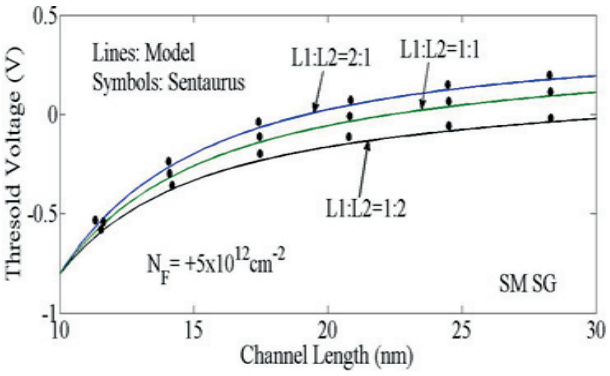
(b)

Figure 8: (a) Electric Field variation along the channel length for different gate length ratios (*L*1/*L*2=1:2, 1:1, 2:1) for negative trap charge of Double Gate. (b) Threshold Voltage variation along the channel length for different gate trapped charges of Single Gate. Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, *L*=30 nm, t_{ox}=2 nm, V_{DS}=1 V and V_{GS}=0.1 V.

Figure 9 (a) and (b) shows the variation of threshold voltage with the channel length for different damaged and undamaged length ratios (*L*1/*L*2= 1:2, 1:1, 2:1) for negative and positive interface trapped charge cases respectively. It is observed that SCE become serious on decreasing the channel length ratios. That means the threshold voltage is higher for the higher undamaged gate length i.e., *L*1. This is because of the higher channel barrier height for higher length ratio (*L*1/*L*2=2:1) as predicted in Fig. 4(b). Further, the roll-off in the threshold curve is higher for the device having smaller length ratio (*L*1/*L*2=1:2). This is attributed to the fact that the control gate loses its control over the channel at smaller *L*1 and higher *L*2.



(a)



(b)

Figure 9: Threshold Voltage variation along the channel length for different gate length ratios (*L*1/*L*2=1:2, 1:1, 2:1) of Single Gate including negative trap charge. (b) Threshold Voltage variation along the channel length for different gate length ratios of Single Gate including positive trap charge Parameters used ϕ_M= 4.6 eV, N_A =1× 10^{16} cm^{-3}, t_{Si}=10 nm, *L*=30 nm, t_{ox}=2 nm, V_{DS}=0.1 V and V_{GS}=0.1 V.

5 Conclusion

The derived model for surface potential, electric field and threshold voltage has been shown the effectiveness of UTB DG SOI MOSFET to suppress the SCEs. Due to the additional gate introduction, there is more control over the channel region and that will be the important factor for suppression of hot carrier effect (HCE) and DIBL. An extensive analysis is carried out to study the effect of various parameters like drain bias, damaged and undamaged length ratio variation, and interface charge variation on surface potential, electric field, and threshold voltage. From the result, the deterioration in the threshold voltage may be improved by increasing the length of *L*1 i.e. decreasing the undamaged region. The DIBL and HCE can be controlled effectively by increasing the gate length ratio (*L*1/*L*2), which can be achieved by proper fabrication methodologies. The device performance is going to deteriorate in presence of the interface trap charges in the oxide. The derived analytical model is compared and found to be in excellent agreement with the simulation results obtained from Sentaurus™.

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