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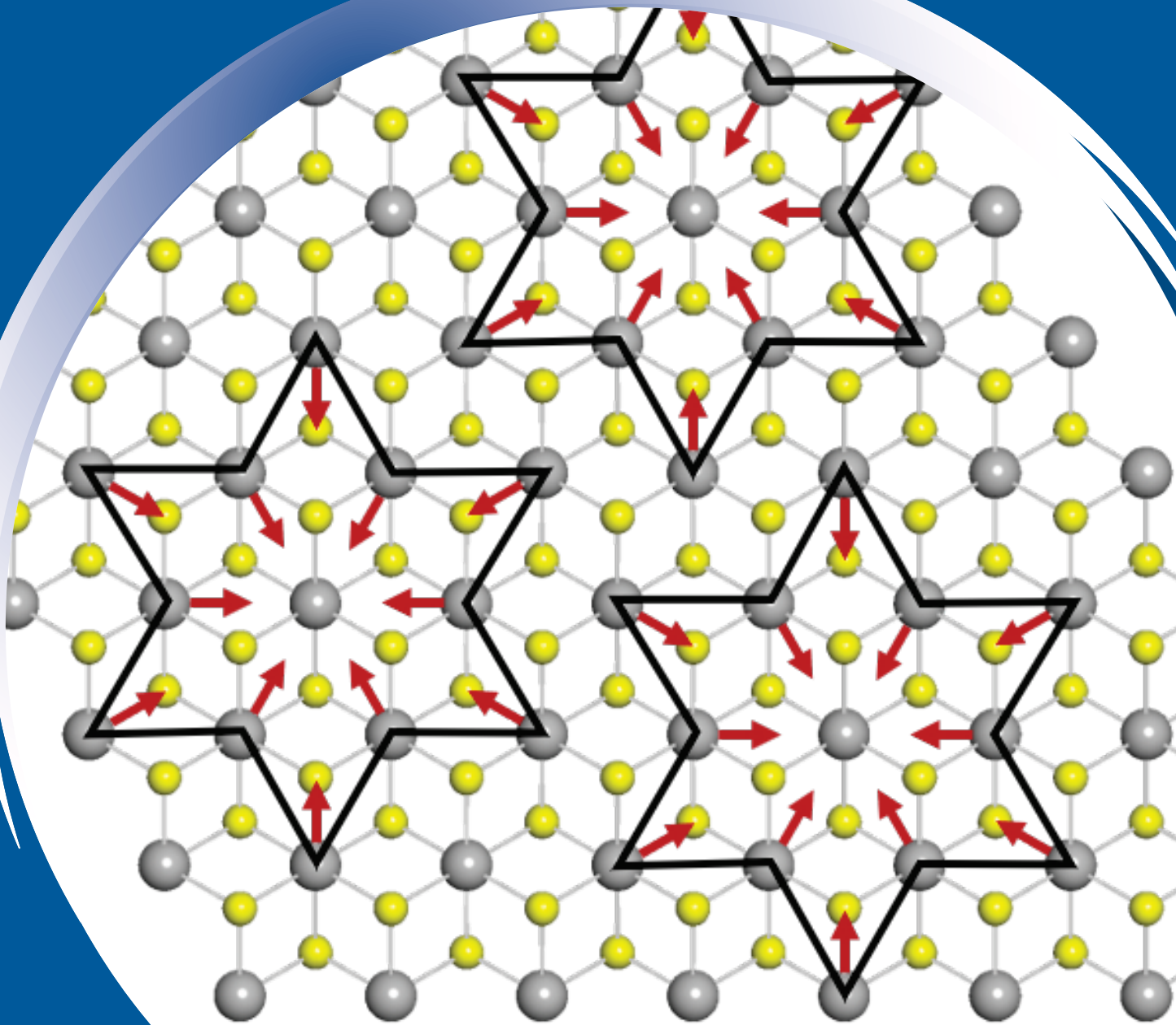

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3D Printed Microwave Clamp Probe Design to Detect Water Level in PVC Pipes

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Abstract: The permittivity of water is considerably larger than that of air. As the amount of water in PVC water pipes increases, the air will be replaced by water. This means that the electromagnetic environment properties inside the pipe will change. In this study, we proposed a microwave clamp probe designed with a 3D printer that can detect the percentage of water in 50 mm diameter PVC water pipes. The clamp probe allows measurement of return loss from a single port for determining the fill rate of water without any physical intervention from outside the pipe. The clamp, which is structurally similar to a loop antenna, operates at a frequency of 2.45 GHz. As a result of simulations and experimental measurements for different fill percentages of the pipe, the input impedance of the clamp was calculated. Then, an impedance-fill rate graph was created, showing the amount of water in the pipe section according to the impedance values obtained. The impedance seen from the clamp input indicated a linear increase between 40-100 Ω, according to the 0%, 20%, 50%, 80% and 100% of the water in the pipe. The clamp has a compact structure that can be used as a plug-and-play anywhere on the horizontal.

Keywords: Microwave Clamp Probe; Impedance Analysis; PVC Water Pipe; Pipe Fill Rate; Loop Antenna Design

3D natisnjena zasnova mikrovalovne sonde za zaznavanje nivoja vode v PVC ceveh

Izvleček: Permisivnost vode je precej večja od permisivnosti zraka. Ko se količina vode v PVC vodovodnih ceveh poveča, zrak nadomesti voda. To pomeni, da se bodo spremenile lastnosti elektromagnetnega okolja v cevi. V tej študiji smo predlagali mikrovalovno sondo s kleščami, zasnovano s 3D-tiskalnikom, ki lahko zazna odstotek vode v vodovodnih ceveh iz PVC s premerom 50 mm. Objemna sonda omogoča merjenje povratnih izgub iz ene same odprtine za določanje stopnje napolnjenosti z vodo brez fizičnega posega z zunanje strani cevi. Sponka, ki je strukturno podobna anteni z zanko, deluje pri frekvenci 2,45 GHz. Na podlagi simulacij in eksperimentalnih meritev za različne odstotke napolnjenosti cevi je bila izračunana vhodna impedanca objemke. Nato je bil izdelan graf impedance in stopnje napolnjenosti, ki prikazuje količino vode v delu cevi glede na dobljene vrednosti impedance. Impedanca na vhodu klešč je pokazala linearno povečanje med 40 in 100 Ω glede na 0 %, 20 %, 50 %, 80 % in 100 % vode v cevi. Sponka ima kompaktno strukturo, ki se lahko uporablja kot priključek „plug-and-play" kjer koli na vodoravni površini.

Ključne besede: Mikrovalovna sonda s kleščami; impedančna analiza; PVC vodovodna cev; stopnja napolnjenosti cevi; zasnova antene z zanko

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1 Introduction

There are several ways to measure the amount of water in a polyvinyl chloride (PVC) water pipe without visual and physical contact. The technique proposed in this study is based on the "Microwave Measurement Method". In terms of electromagnetic waves to penetrate objects, microwave circuits can provide the more sensitivity than low frequency basic electronic circuits cannot reach.

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The distilled water has high permittivity at the microwave frequencies. By the means of this feature, water level detection in a PVC pipe is possible using microwave circuits. The permittivity of distilled water is about 80 times higher than air. This means that the level of the distilled water will change the electromagnetic properties of the medium inside the pipe. By selecting a suitable frequency, different input impedances can be determined by changing this water-air ratio.

There are very few studies in the literature that aim to determine the amount of water from the outside. They generally reported attenuation in amplitude according to the change in the level of water by designing a kind of power transceiver system by placing an antenna on both sides of the water pipe [1]. In some studies, electro-acoustic circuit methods and capacitive sensor applications have been used [2-7]. In a further application, computational estimation methods with radio frequency circuits were used to determine the amount of different liquids in the plastic water pipe [8]. Few studies such as these shows that methods that can measure the amount of water in PVC pipes with microwave circuits are open to development.

In this study, a clamp near field probe was designed. The amount of water in the pipe was tried to be determined by measuring from outside without any physical intervention to a PVC water pipe of known dimensions. Return Loss (RL) obtained from the input of the clamp probe was determined according to the percentage change of water in the pipe. Then, impedance parameters were analyzed.

In the second part of the study, the 3D design of the clamp probe and the calculation of the fullness ratio were mentioned. In the third section, RL-frequency and impedance-frequency analyzes were performed according to the change in the amount of water in the pipe. Simulation and measurement results were compared. In the last section, the importance and originality of the study was emphasized.

2 Microwave clamp probe design

The designed microwave near field probe is in the form of a clamp that will surround the pipe when installed. The edges of the clamp, which can be opened to both sides with the help of a hinge, overlap when the hinge is closed. Thus, discontinuity will not occur circularly. The clamp is similar to a loop antenna whose ground part is outside the probe and the antenna part is also inside. An SMA connector was connected to one side of the clamp to be measured RL.

The clamp was designed for PVC water pipe with 50 mm outer diameter. The inner radius of the clamp is R_{in} = 26 mm and the outer radius is R_{out} = 38 mm. Ground and antenna consist of t = 0.1 mm thick copper strip. The width of the clamp is W_2 = 17 mm and the width of the antenna is W_{probe} = 5. The lengths of the hinge are W_1 = 30 mm and L_1 = 20 mm. The heights of the clamp are L_2 = 93.5 mm and L_3 = 76 mm. Figure 1a shows the design parameters of the clamp.

The clamp was designed in CST MWS program and fabricated in 3D printer. In additive manufacturing for microwave circuits, fill density is a critical parameter in determining substrate dielectric coefficient. Here the density was selected as 90 %. Thus, according to [1], the permittivity is ϵ_{clamp} = 2.7 and tangential loss is tan δ= 0.008. The design and manufacturing of the clamp was given in Figure 1b.

a)

b)

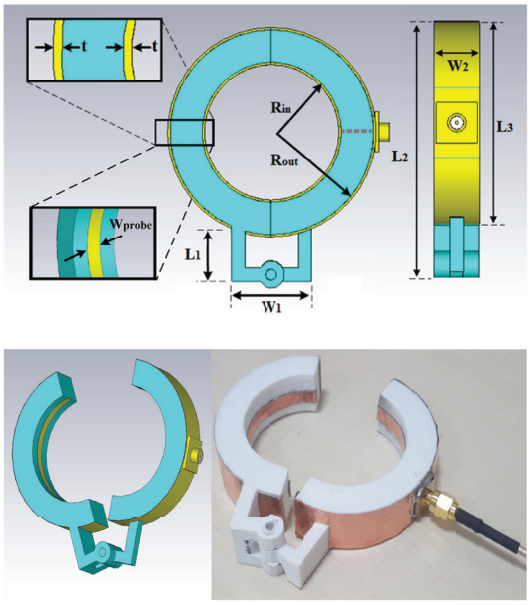

Figure 1: a) Dimensions of Clamp Probe b) Design and Manufactured View of the Clamp Probe.

The height of the water in the pipe, whose outer radius is R_p = 25 mm and the inner radius, is R_W = 23 mm and the dielectric coefficie is ϵ_{PVC} = 2.8 increases nonlinearly with respect to the water fill percentage. In the simulation, "cylindrical tank filling problem" was used to calculate the water height over the cross-sectional area [9]. The area covered by the water was calculated according to Equation (1).

$$A = R_w^{\,2}\cos^{-1}\left(\frac{R_w - h}{R_w}\right) - \left(R_w - h\right)\sqrt{2R_w h - h^2} \quad (1)$$

where, A is the cross-sectional area of the water in the pipe, R_W is the inner radius of the pipe, and h is the

height of the water in the pipe. According to 10 % changes of *A*, the water height was given in Table 1.

Table 1: The water height according to fill ratio in pipe.

Fill ratio (%)	Height (mm)	Fill Ratio (%)	Height (mm)
10	7.16	60	26.59
20	11.67	70	30.33
30	15.60	80	34.92
40	19.40	90	38.83
50	23	100	46

The most decisive parameter for measuring the amount of water in the pipe using a single port clamp is the permittivity (ϵ_{water} = 79.4). As the amount of water increases, the air in the pipe (ϵ_{air} = 1) will be replaced by water. According to this displacement, the RL (S_{11}) seen from the connector of the clamp will increase or decrease. Therefore, the impedance seen from the input will also change. In Figure 2, it is seen that the clamp was applied to the PVC pipe and the water change was measured with Rohde Schwarz FSH6 Spectrum (network) analyzer. In order for the spectrum analyzer to perform network analysis, the device must have a tracking generator. The reflected power must be transferred to the device input with directional coupler. Thus, the RL measurement can be made from the spectrum analyzer.

3 Simulations and experimental results

The clamp was designed for the frequency of f_0 = 2.45 GHz where it provides the inequality of $|S_{11}| < -10$ dB [10]. RL vs. frequency graph of the clamp was shown in Figure 3a. Also in Figure 3b, measured according to the change in the percentage of water in the pipe, $|S_{11}|$ graph is given.

As seen in Figure 3b, magnitude of S_{11} for the clamp could not provide high selectivity in determining the amount of water in the pipe [11]. The complex S_{11} has been transformed to impedance (S_{11}) parameter according to Equation (2). Thus, significant range can be achieved between the impedance values of the pipe in different percentages.

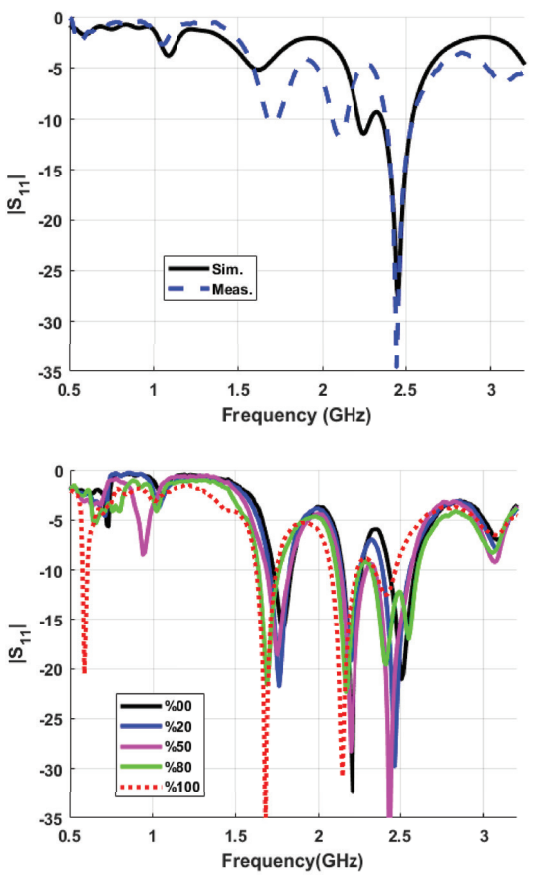

Figure 3: a) Return Loss of the clamp b) Return Loss according to amount of the water in pipe.

$$Z_{11} = Z_0 \times \frac{(1+S_{11})}{(1-S_{11})} \quad (2)$$

Since the probe is designed according to Z_0 = 50 + *j*0 Ω on the frequency f_0, the impedance magnitude ($|S_{11}|$) was calculated according to Equation (3).

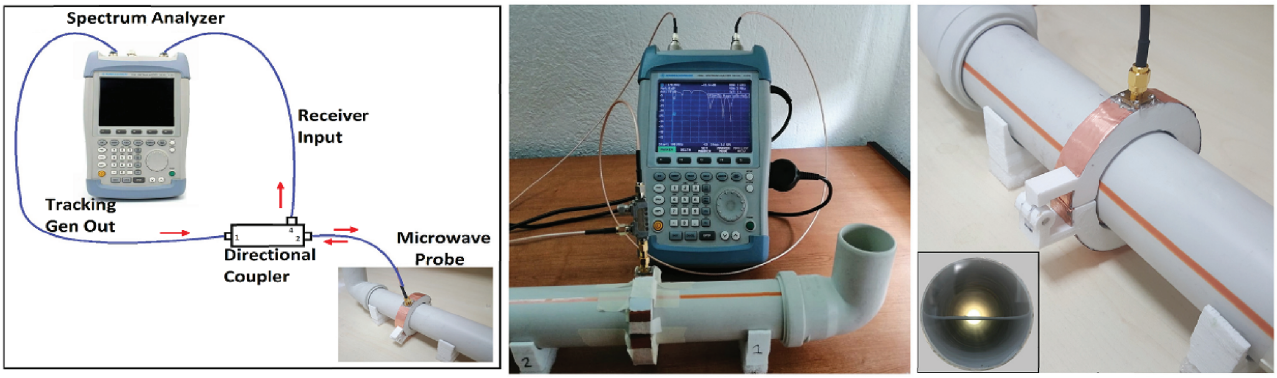

Figure 2: Application of probe to PVC pipe and measurement of water change.

$$|Z_{11}| = \sqrt{\left((Z_{11})_{real}\right)^2 + \left((Z_{11})_{complex}\right)^2} \quad (3)$$

In impedance calculation at f_0, simulation and measurement values were close to Z_0. In Figures 5a and 5b, it is seen that the magnitude of the $|S_{11}|$ changes according to different fullness percentages of the pipe. The intermediate occupancy percentages not shown here were not included in the graphic because they were very close to other values. The clamp provides linearity only for certain percentages given. The points marked on Figures 4a and 4b are at $F_{sim} = f_{meas} = 2.442$ GHz frequency at which the clamp operates.

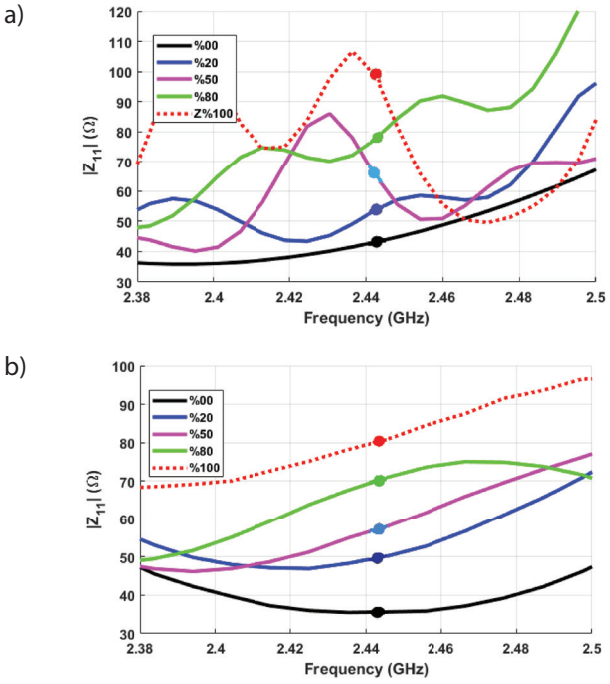

Figure 4: $|Z_{11}|$ vs. frequency graph for simulation (a) and measurement (b).

The measurement and simulation results were combined in Figure 4 which is the graph of the impedance magnitude vs. fill ratio. As shown in the figure, when the occupancy rate is increased from 0% to 100%, $|Z_{11}|$ also increases linearly. The fact that the simulation and measurement were compatible with each other supports this. The minor impedance difference between them consists of connector and path losses in the measurement.

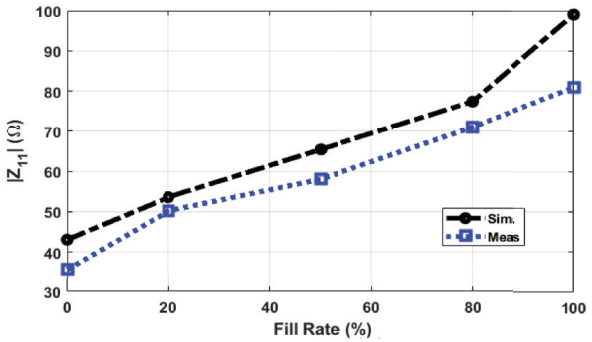

Figure 5: The graph of impedance vs fill ratio.

4 Conclusion

In this study, a near field probe was designed using a 3D printer to determine the amount of water in PVC water pipes. Thanks to the clamp-shaped design of the probe, measurements can be made from outside the pipe without any physical intervention to the pipe. The amount of water in the pipe can be determined without visual contact with the water in the pipe.

The clamp resembles a loop antenna, the ground of which is outside the probe, and the antenna is inside. In determining the filling rate of the water in the pipe, the input impedance was calculated by measuring the return loss.

By making use of the permittivity of the water approximately 80 times more than that of the air, an impedance graph was created according to the filling rate of the water in the pipe. Thus, the amount of water in the pipe can be determined according to the impedance value obtained from the measurement. The clamp exhibits linear impedance increase between 40-100 Ω at 0%, 20%, 50%, 80% and 100% occupancy of the water in the pipe. Measurement and simulation results are very close to each other. The clamp is compact in such a way that it can be used anywhere in the pipe as plug-and-play. The proposed original clamp probe design can also be developed for pipes of different types and thicknesses.

5 Acknowledgement

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6 Conflict of interest

No conflict of interest has been declared by the authors.

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Charge Configuration Memory (CCM) device – a novel approach to memory

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Abstract: Computer technologies have advanced unimaginably over the last 70 years, mainly due to scaling of electrical components down to the nanometre regime and their consequential increase in density, speed and performance. Decrease in dimensions also brings about many unwanted side effects, such as increased leakage, heat dissipation and increased cost of production. However, it seems that one of the biggest factors limiting further progress in high-performance computing is the increasing difference in performance between processors and memory units, a so-called processor-memory gap. To increase the efficiency of memory devices, emerging alternative non-volatile memory (NVM) technologies could be introduced, promising high operational speed, low power consumption and high density. This review focuses on a conceptually unique non-volatile Charge Configuration Memory (CCM) device, which is based on resistive switching between different electronic states in a 1T-TaS_2 crystal. CCM demonstrates ultrafast switching speed <16 ps, very low switching energy (2.2 fJ/bit), very good endurance and a straightforward design. It operates at cryogenic temperatures, which makes it ideal for integration into emerging cryo-computing and other high-performance computing systems such as superconducting quantum computers.

Keywords: Charge Configuration Memory (CCM); 1T-TaS_2; Ultrafast devices; Charge density wave (CDW)

Spominska naprava na podlagi konfiguracije naboja (CCM) – nov pristop do spomina

Izvleček: Računalniške tehnologije so v zadnjih 70-tih letih neverjetno napredovale, predvsem zaradi pomanjševanja električnih komponent na nanometrske dimenzije in posledičnega povečanja gostote, hitrosti in zmogljivosti računalniških vezij. Zmanjševanje dimenzij pa vodi tudi do nezaželenih stranskih učinkov, kot so povečano tokovno puščanje, visoka disipacija toplote in povečani stroški izdelave. Vendar eden največjih vzrokov, ki zavira napredek v visokozmogljivem računalništvu, je vse večja razlika v zmogljivosti med procesorji in spominskimi enotami, oz. t. i. procesorsko-spominska vrzel. Vpeljava novih alternativnih trajnih spominskih (NVM) tehnologij bi lahko povečala učinkovitost, hitrost in gostoto spominskih naprav. Ta pregledni članek opisuje konceptualno novo trajno spominsko napravo na podlagi konfiguracije naboja (CCM), ki temelji na uporovnem preklapljanju med različnimi elektronskimi stanji v kristalu 1T-TaS_2. CCM naprava izraža ultra hitre preklopne čase <16 ps, zelo nizko preklopno energijo (2.2 fJ/bit), zelo dobro vzdržljivost in preprost dizajn. Obratuje pri kriogenih temperaturah, kar jo naredi idealno za integracijo v uveljavljajoče področje krio-računalništva in ostale visokozmogljive računalniške sisteme, kot so npr. superprevodni kvantni računalniki.

Ključne besede: Spomin na podlagi konfiguracije naboja (CCM); 1T-TaS_2; Ultra hitre naprave; Val gostote naboja (CDW)

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1 Introduction

Advances in computer technologies were made possible due to enormous investments of money, time and man-power into research and development of silicon semiconductor technology, which has been very successful with the constant upgrades despite all the problems it has been facing [1], [2]. However, to sustain

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this progress in high-performance computing in the long run, it seems that new alternative technologies have to be introduced to either complement the existing ones or to develop new directions. Augmenting Si CMOS with two-dimensional or memristive materials could produce more efficient 2D transistors, sensors and interconnections [3] or even new technological concepts such as biologically inspired computing and on-chip memory and storage [4]. On the field of memory technologies there is much room for improvement, especially when it comes to efficiency and power consumption. Standard dynamic random-access memory (DRAM) circuits can use up to 30 % of total power consumption [5] of the whole computer system due to constant refreshing and even static random-access memory (SRAM) circuits suffer losses from leakage [6]. Introduction of non-volatility [7] with the combination of a high energy efficient information storing mechanism could result in a memory device of the future. Charge configuration memory (CCM) devices presented here rely on reconfiguration of electronic domains between the ground state and excited metastable hidden (H) state that was recently discovered in a layered transition metal dichalcogenide 1T-TaS_2 crystal [8]. Switching between different electronic states results in a big change of electrical resistance of the device. This review briefly explains the origin of the emergent metastable H state in 1T-TaS_2 and discusses its properties in the content of a novel non-volatile memory device based on reconfiguration of charge.

2 1T-TaS_2 and the phase diagram

The active element in the CCM device is a 1T-TaS_2 crystal, which belongs to the group of transition metal dichalcogenides (TMDs) with a chemical formula MX_2, where M is a transition metal atom (Ta, Mo, W, Ti…) and X is a chalcogen atom (S, Se or Te). One layer of 1T-TaS_2 is made from two triangular lattices of S atoms with a triangular lattice of Ta atoms in between. There are strong covalent bonds inside the layer and weak van der Waals bonds in between the layers. This leads to strong anisotropy of the material which shows in different mechanical, thermal and electrical characteristics. Pronounced quasi 2D characteristic gives birth to interesting new physics not observable in three-dimensional materials [3], [9].

The phase diagram of 1T-TaS_2 is very rich, exhibiting different charge-density-wave (CDW) states, Mott transition, polaronic ordering [10], metastable state [8] and even superconductivity at higher pressures [11]. At temperatures above 540 K, the material behaves as a simple metal, but when cooled down below that temperature it undergoes a phase transition into an incommensurate (IC) CDW due to a combination of Coulomb repulsion [12] and Fermi surface nesting [13]. At this point the charge density inside the crystal is modulated and the crystal lattice is displaced, but the two of them are not aligned. Because of the frustration between the IC CDW and the underlying lattice, the state transforms into a nearly commensurate (NC) CDW at a temperature around 340 K. Electrical resistance of the material in NC state is several times higher than in the metallic state but it is still well conducting [11]. Steady state electrical resistance of the material is shown in Fig. 1a, where

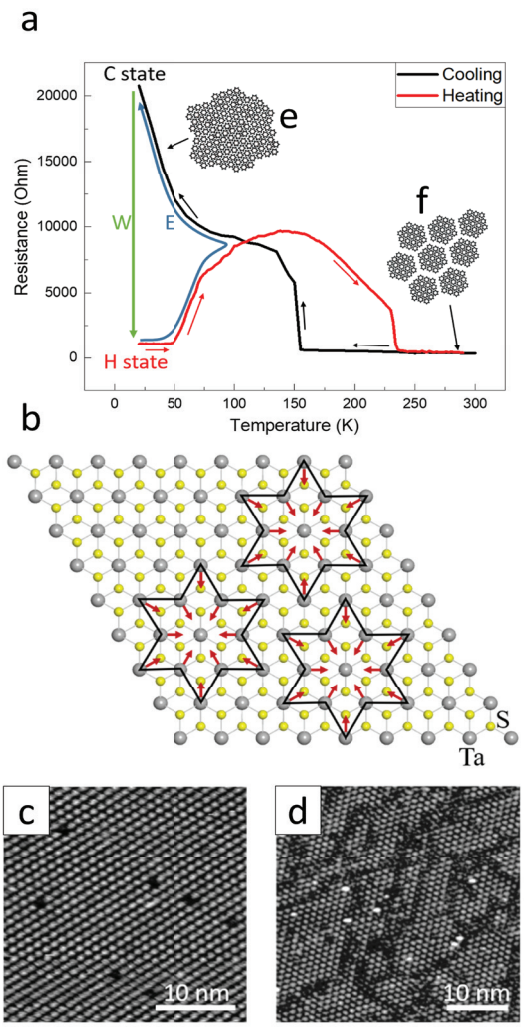

Figure 1: Phase diagram of 1T-TaS_2. a) Plot of resistance versus temperature. Black curve represents cooling of the CCM device and red curve represents heating after switching to the H state. Write (W) process is denoted with a green arrow, erase (E) process is denoted with a blue arrow. b) Formation of a polaron. 12 surrounding Ta atoms are slightly displaced toward the middle one. c) An STM image of the C state with an ordered polaronic structure. d) An STM image of the H state with patches of polarons seperated with domain walls. e) Sketch of the C state. f) Sketch of the NC state.

the black curve represents resistance upon cooling from room temperature. NC CDW state is made from a hexagonal array of polaron clusters, separated with domain walls, as is sketched in Fig. 1f (inset to Fig. 1a). A polaron consists of a central electron localised on a Ta atom with 12 surrounding Ta atoms displaced toward the centre [14], [15], which forms a star formation (Fig. 1b). Upon slow cooling below 160–180 K, domain walls between polaron clusters disappear and a fully commensurate (C) CDW polaronic lattice forms. Fig. 1e (inset to Fig. 1a) shows a sketch of the C state and Fig. 1c shows an image of the C state using a scanning tunnelling microscope (STM). Each bright spot represents an individual polaron and the dark spots are impurities in the lattice. C CDW state is a Mott insulator with a gap of 0.1 eV [13]. This leads to a jump in electrical resistance of the sample at ~160–180 K, which further increases as the temperature is decreased to ~20 K, as can be seen on Fig. 1a (black curve). 20 K or lower is a typical working temperature for CCM devices. If the C state is heated up from 20 K to room temperature, the resistance curve backtracks to ~100 K but then follows the red curve and draws a hysteresis until ~220 K. The material then transitions into a so-called stripped ordered triclinic (T) phase [14] before returning to the NC state at ~280 K.

If the C state is excited by either an optical [8] or an electrical [16] pulse, the material switches to a metastable hidden (H) state, which is stable at low temperatures (<20 K). When this transition occurs, the electrical resistance of the sample drops sharply because the H state is metallic. Transition from the C to the H state is called a Write (W) process, which is denoted with a green arrow in Fig. 1a. The contrast in resistance between the two states is dependent on the sample and on the geometries of the CCM device and can be up to three orders of magnitude big [8].

Upon heating the H state (red curve), the resistance remains approximately constant up to 50 K, at which point it starts to increase and merges with the virgin resistance curve (black) at ~100 K. If the sample is cooled down at that point, the resistance follows the virgin curve, meaning the H state is completely reversed into the C state. The transition from the H to the C state is called an Erase (E) process and is denoted in Fig. 1a with a blue curve. The H state can also be erased via Joule's heating of the material using a train of optical pulses [8] or a longer electrical pulse [16], [17].

Examining the H state microscopically using an STM, a distinct patchy pattern can be observed with domains of polarons and domain walls separating them [18], as seen in Fig. 1d. Domain walls arise because the extra injected charge introduced by the external excitation (optical or electrical) is accommodated in the C CDW structure. The charge periodicity of the metastable state (which determines the domain size) originates from a free energy minimum which arises from the competition of Coulomb interaction between domain walls and the energy of the domain wall crossings in the CDW state [8]. The conduction mechanism of the metallic H state is not yet completely understood, but scanning tunnelling spectroscopy (STS) reveals that both polarons and domain walls are conducting [19]. This means that the conduction is not percolative as in typical memristors [20], but is collective in nature. By analysing the junctions between domain walls in the STM image (Fig. 1d) it is discovered that some of them act as non-trivial topological defects (NTTDs), which means they can only be annihilated by an antidefect with equal and opposite winding number. These NTTDs contribute to the non-volatility of the LO state [17], [18] at low temperatures. The pattern of domain walls in the H state is also always different when switching between the C and the H state. This is important for reproducibility and endurance of the devices, because it means that pinning by lattice defects or impurities does not play a significant role in the switching process. Endurance measurement shows that the devices are very durable and can survive well over 10^6 cycles of W and E with remarkable stability throughout [17].

During the transition from the C to the H state (W process) only the charges are reconfigured. This switching is therefore purely electronic and predicted to occur on an electronic timescale (~300 fs). The transition time of the W process was measured using coherent time-resolved femtosecond spectroscopy by Ravnik *et al* [21] in a pump-probe experiment at 160 K. At this temperature the lifetime of the H state is ~0.1 ms [22]. This allows for a stroboscopic measurement with 1 kHz repetition rate laser, which means that before each next laser pulse, the H state has completely relaxed back to the C state. It was determined that the transition time of the W process is ~400 fs, which confirms the assumption. This shows that the W process is inherently extremely fast and is not the limiting factor when it comes to the speed of the CCM device. The E process on the other hand is predominantly thermal and slower and requires more effort and planning to reach optimal operation.

3 Operational properties of the CCM device

3.1 Current-voltage characteristics

A typical CCM device is shown in Fig. 2a with a 1T-TaS_2 flake on Si/SiO_2 substrate and metal electrodes

fabricated on top using electron-beam lithography. Current-voltage (I-V) characteristics of such a CCM device is shown in Fig. 2b and c for both the Write and Erase process respectively, measured at 20 K. Since the C state is the insulating state, it is denoted as the high resistance state (HI) and H state is metallic, so it is called the low resistance state (LO). For a W process, CCM is originally in the HI state. As the current incrementally increases, the voltage follows the HI curve (black) in Fig. 2b. It is linear at first but becomes non-linear at higher currents. Non-linearity is fitted as

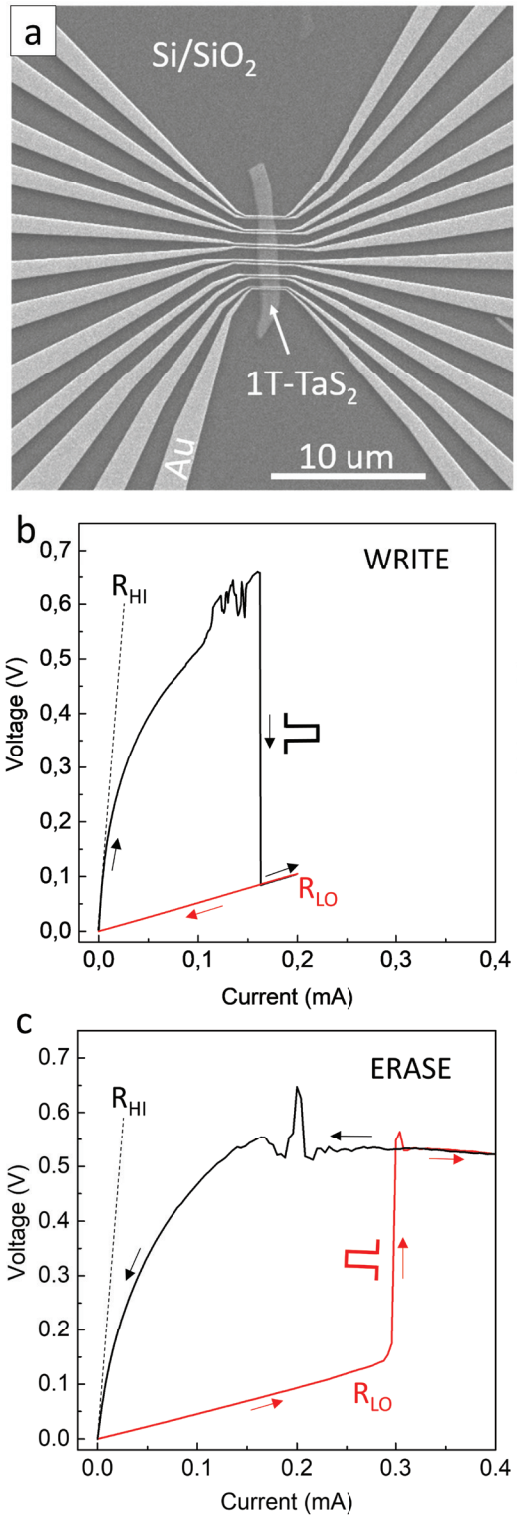

Figure 2: a) Typical CCM device. 1T-TaS_2 crystal on Si/SiO_2 substrate with golden electrodes fabricated on top. b and c) I-V characteristics of the W and E process respectively.

$$\frac{I}{I_0} = exp\left(\frac{V}{V_0}\right) \tag{1}$$

Voltage increases until a certain threshold of current is reached, at which point a switch to the LO state occurs, and the voltage drops. As the current is decreased back to zero, voltage follows a linear LO curve (red). E process is done similarly, only that the device starts from the LO state (Fig. 2c). As the current incrementally increases, the voltage follows a linear LO curve (red) until a certain threshold is reached, at which point a switch to the HI state occurs and the voltage jumps. As the current is decreased the voltage follows the non-linear HI curve back (black). The threshold values for W and E processes can vary slightly between devices but can be controlled with proper planning. Read operation (R) is straightforward, any read current can be used as long as it's low enough to not trigger the W or E operation.

The HI state shows clear non-linear behaviour which cannot be fitted with a tunnelling diode equation or attributed to CDW sliding behaviour [16], [23]. Steps or jumps in voltage in the HI state are case dependant and are attributed to complex tunnelling dynamics between polarons and slight rearrangements of the polaronic structure [16], [24] with similar resistance. However, the CCM device is not meant to be driven in this manner, but rather by using a single W and E pulse above the threshold value to switch between the HI and LO state. In devices that are well characterized, the potentially unknown region of the I-V characteristics can be easily avoided.

3.2 Writing process

W process can be observed in real time with the use of an oscilloscope connected in parallel to a CCM element as shown on a scheme in Fig. 3a. The 1T-TaS_2 flake used was 65 nm thick and 0.9 um wide, with Au electrodes fabricated over the flake and the gap between the electrodes ~280 nm. In Fig. 3b we see the time evolution of voltage across the CCM device when 50 ns long W pulses of varying amplitude are applied on the electrodes at 100 K. At low amplitudes the voltage remains constant over the entire duration of the pulse with the rise time τ_R~7.4 ns defined by the RC constant of

the circuit. At a certain threshold (~0.55 V) the voltage across the CCM drops, which is a result of a W process from HI to LO state and remains there till the end of the pulse. If the area under the voltage curves (coloured in Fig. 3b) is integrated and the W energies are calculated using the equation $E_W = \int_{t1}^{t2} (U^2 / R) dt$, where t_1 is the beginning of the pulse, t_2 is the time where the voltage drops and R is the resistance of the sample, it turns out that the energies for different amplitudes are not the same, meaning the switching does not occur due to cumulative heating. This is also confirmed in Fig. 3c where there is a clear decrease in W energy as the switching pulses are shortened from 400 ns to 9 ns. If switching was only due to heating, the W energy would be constant across all the pulse widths. The mechanism for W switching is not yet completely understood but it seems to be a combination of applied electric field and charge injection into the sample [8], [16], however heating might play a role to a certain degree.

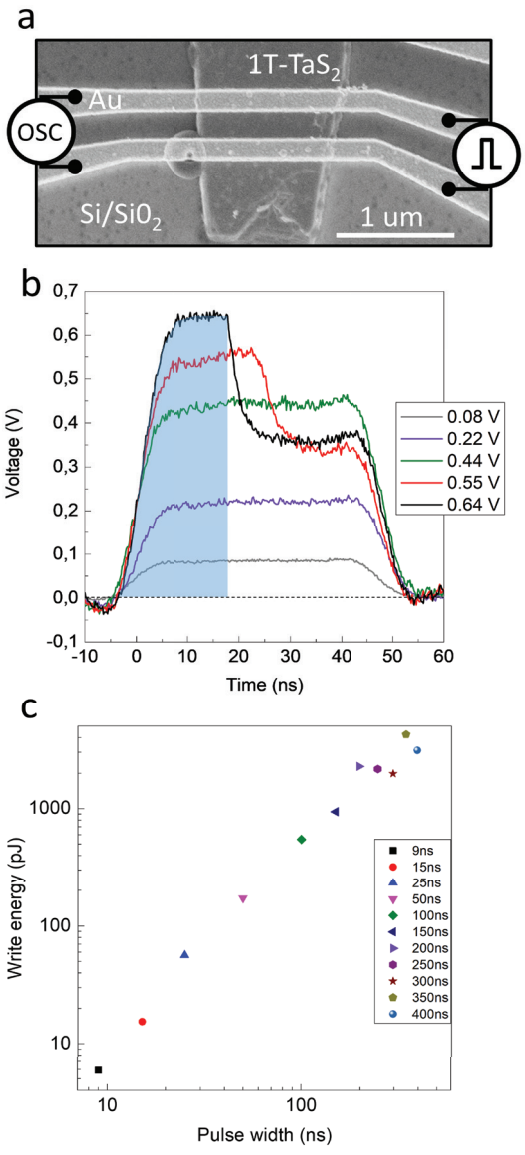

Figure 3: a) Schematic of the experiment with a pulse generator on one side of the CCM device and an osciloscope in parallel. b) Voltage across the CCM device observed during electrical pulsing. The drop in voltage occurs because the CCM device switches from HI to LO state. Shaded area was used in the W energy calculation. c) Scaling of the W energy as a function of applied pulse width.

The same kind of switching dynamics as in Fig. 3b was also observed using longer W pulses [16]. It was shown that the range of possible W pulse width is very wide, from 100 ms down to 16 ps [16], [17]. For ultrafast pulses the electrodes were fabricated in a transmission line configuration to ensure good transmission. W energy calculated with a 16 ps FWHM (rise time ~11 ps) pulse was E_W = 2.2 fJ/bit [17], where the W voltage was 1 V and entire pulse width was used in the equation.

One way to decrease the W energy is scaling of the CCM device. Scaling of dimensions directly affects the voltage needed to switch the state of the CCM device. If the dimensions of the device are smaller, there's physically less polarons or domain walls that are required to reconfigure, meaning less injected charge is needed plus the applied electric field is increased, assuming both are vital. W voltage scales linearly with the gap between the electrodes fabricated on devices on a range of 4 µm – 60 nm, with the smallest W voltage achieved being 0.3 V [17].

3.3 Erase process

When considering a non-volatile memory device, the information stored has to remain unchanged for a long period of time, ideally indefinitely. HI state of the CCM device is not problematic since it is the ground state. The LO state however is a metastable state which occurs under non-equilibrium conditions, but it can still be extremely long lasting under right conditions. The switching of the LO state back into the HI state is presumed to occur due to thermally activated domain reconfiguration, meaning the lower the ambient temperature, the more stable the LO state is, or in other terms, the longer the lifetime of the LO state τ_{LO} is. LO state is completely stable or non-volatile at temperatures below 20 K, so E process is induced by applying an E pulse, which can be on a time scale of µs-ms with an amplitude <0.5 V [16], [17]. E pulse effectively heats up the CCM element, which than switches back into to the HI state. The E process can be greatly optimized with proper thermal management by including an extra heating element as was demonstrated in phase change memory (PCM) devices, where high heating is crucial for operation [25]. It is also presumed that in a bigger

scale CCM device, E process would be done in blocks, meaning that slower E process would not pose such a disadvantage.

At temperatures above 20 K, the LO state slowly relaxes back into the HI state by itself with a certain relaxation rate ($r = 1/\tau_{LO}$) [22]. The relaxation dynamic was investigated by switching a CCM device from HI to LO state and observing the time evolution of the electrical resistance at a fixed temperature, which is shown in Fig. 4a (experiment - dotted line, exponential fit – dashed line). Speed of relaxation increases quickly with increasing temperature and becomes comparable to the measurement time at temperatures above 60 K. At 150 K the relaxation rate is a few µs, which can be observed on the oscilloscope by adjusting the period of W pulse train and observing the voltage across the CCM (similarly to Fig. 3b). This means that the CCM device can be written to the LO state at any temperature bellow the NC-C transition (~160–180 K), however the stability of the LO state is heavily influenced by the temperature. At 150 K it takes only a few µs for the LO state to completely relax back to the HI state after which the CCM device is ready to be written again. CCM device can thus also be used in the volatile regime (above 20 K), but have to be refreshed accordingly, much like dynamic random-access memory (DRAM).

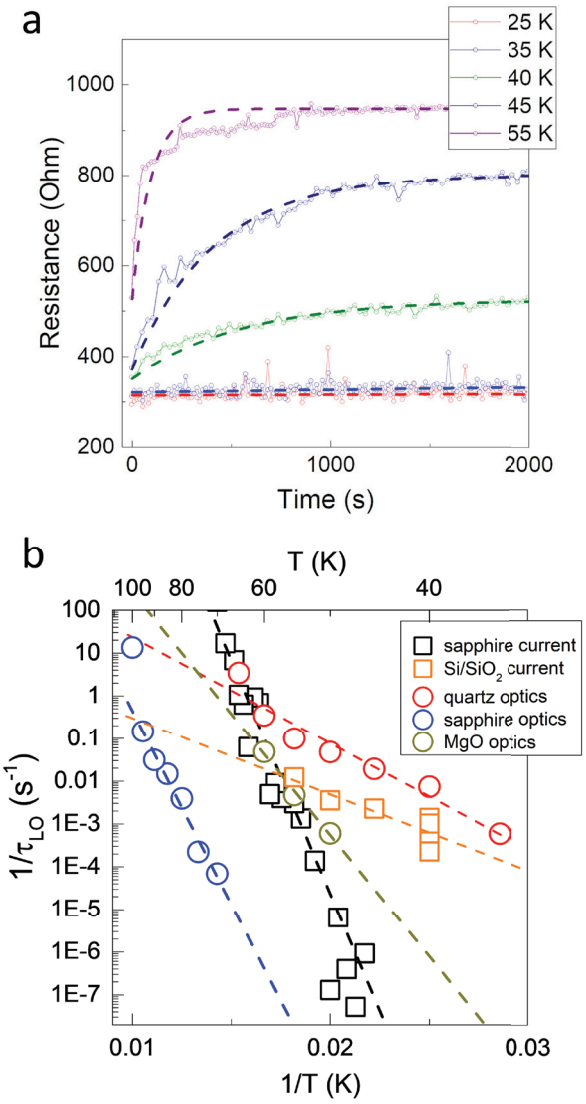

Figure 4: a) Plot of resistance versus time, showing relaxation of the LO state at different temperatures, from which the lifetimes are extracted. The relaxation time at 40 K is ~10 minutes, while at 55 K it's ~2 minutes. Dotted line is the experimental data, dashed line is the exponential fit. b) Arrhenius plot of relaxation rate for different substrates and different excitation methods (optical or electrical).

To obtain relaxation dynamics in Fig. 4a electrical pulses were used. When using laser pulses to write the CCM's state, the relaxation dynamic of the LO state looks similar, however the comparison of the relaxation rate *r* between the two cases shows quite a big difference. This can be seen when comparing the relaxation rate for optical (blue circles) and current (black squares) switching of a CCM device on a sapphire substrate in an Arrhenius plot in Fig. 4b. The *r* of the optical switching is much lower than the *r* of the current switching at a certain temperature. This is most likely attributed to extra heating provided by the current pulse used for switching, which is 5 µs long, compared to a 35 fs laser pulse. This means that the effective temperature is higher in the current switching compared to the optical switching.

Choice of sample substrate also affects the relaxation rate due to different expansion coefficients and consequential strain on the 1T-TaS_2 sample [22] (Fig. 4b). The tested substrates were sapphire, MgO, quartz and Si/SiO_2 with the imposed tensile strain $\Delta\varepsilon$ being 0.19 %, 0.13 % for sapphire and MgO respectively and 0.03 % for quartz and Si/SiO_2 at 50 K. Even though $\Delta\varepsilon$ is quite small, the effect seems to be rather large when comparing the relaxation rate for the case of sapphire and quartz. When the lattice expands because of the tensile strain of the substrate, the CDW has to rearrange to maintain commensurability and that can lead to extra domain walls being introduced. And since the relaxation from the H to the C state involves annihilation of domain walls, a higher tensile strain leads to higher activation energies E_A and consequentially to a lower relaxation rate. Extracting the activation energy E_A from fitting an Arrhenius law $1/\tau_H = e^{-E_A/k_BT}$ in Fig. 4b, the values are between E_A = 280–2300 K, where the highest activation energy belongs to the substrate with the highest $\Delta\varepsilon$ (sapphire). But it appears that the E_A also varies between different samples, implying that some other parameters such as nanofabricated electrodes, local defects and impurities

affect the stability of the H state. By using a proper substrate, one could manipulate and tune the stability of the H state while ensuring a fast E process in an ultrafast non-volatile memory device.

Different substrate strains may have an effect on the way multiple layers of 1T-TaS_2 crystal stack inside a CCM device. It is not yet clear how or to what extent the stacking of layers affects the switching dynamics. The measurements done on a device in a vertical/crossbar (out-of-plane) configuration show qualitatively similar behaviour to a more typical planar (in-plane) device [26]. There is a big discrepancy in the resistivity and the switching threshold for electric field between the two cases, where the vertical device has ~1000 times higher resistivity and ~100 times higher electric field threshold. However, the threshold electrical current is almost the same for both configurations as well as the relaxation rate of the LO state with the extracted activation energy $E_A = 650 \pm 100$ K [26] that matches with previous values for planar devices [22]. This points to the fact that switching between different electronic configurations inside the 1T-TaS_2 crystal combines the effect of in-plane polaronic order reconfiguration as well as re-stacking between individual layers. In the case of typical planar devices [16], [17], [22] (Fig. 2a, 3b) the current is probably not being confined only to the top layer anyway, especially since the electrodes are fabricated over the edge of the crystal and make contact on the side as well. Therefore, both the in-plane and out-of-plane physics contribute to the electrical behaviour of the devices.

Still, the CCM devices in crossbar configuration are very promising for larger scale integration since they allow for bigger density than the planar version. They are also easier to be scaled to lower dimensions, because the gap between the electrodes is determined only by the thickness of the 1T-TaS_2 flake and is therefore not limited by the complicated lithographic procedure. However, very thin flakes (< 10 nm) do not necessarily exhibit the NC CDW – C CDW transition, which means they don't develop the insulating behaviour at low temperatures (Fig. 1a, black curve) and cannot be used as a memory device. Instead their resistance follows a straight line into a so called supercooled NC CDW state as they are cooled down [27]. This problem can be mitigated by ensuring a very slow cooling rate [27] or with capping of the device to prevent oxidation, which could be responsible for pining of the CDW [28] and consequential suppression of the NC-C transition.

4 Conclusions and Outlook

In summary, CCM devices show ultrafast (16 ps FWHM) [17], energy efficient operation (2.2 fJ/bit) [17], non-volatility at cryogenic temperatures [22] and very good endurance (>10^6 cycles) [17], which is very important for electronic applications. The basic memory operation is provided through electronic switching between two distinct resistance states (HI and LO), but intermediate states are also available, potentially allowing one CCM element to be used as a multibit device [16], [26]. The overall structure of the device is also very simple, and it can be fabricated in a planar or vertical configuration to allow for easier integration into bigger systems. Erase process is currently the limiting factor when it comes to speed and energy consumption of the device, however with proper thermal management it can be improved significantly as demonstrated in PCM devices [25]. Role of heating in the switching operation is also not yet understood completely.

Among conventional CMOS memory technologies the most widely spread are the SRAM and DRAM technologies with write times on the nanosecond timescale and write energies from 100 fJ/bit to 1 pj/bit respectively [29]. They have very good endurance and very high level of integration, however their memory operation is still volatile, which makes them inherently more dissipative and less economical. Among non-volatile memory devices, the most popular are the solid state drives (SSD), which usually rely on NAND Flash technology for memory operation, but at this point they are not fast nor durable enough to replace SRAM or DRAM yet [30]. CCM devices are able to achieve faster write times (16 ps) and more energy efficient operation (2.2 fJ/bit)[17] compared to the SRAM or DRAM devices, while also having the advantage of non-volatility. However, CCM devices are currently still in the prototype stage and the level of integration and device density is still much lower compared to conventional CMOS devices.

There are many alternative non-volatile memory technologies besides the CCM, such as Magnetoelectric RAM (MeRAM), Spin-Transfer Torque RAM (STT-RAM) and Phase Change Memory (PCM) devices, among which the lowest energy per bit is reported in electric-field-controlled switching in magnetic tunnel junctions (MeRAM) with $E_W = 30 – 40$ fj/bit [31], followed closely by the spin-tranfer torque switching in CoFeB free layers (STT-RAM) with $E_W = 44$ fJ/bit [32]. PCM devices have higher switching energies (>2.5 pJ) and also slower operational speed (~500 ps) [25], because they rely on relatively slow ionic recrystallization of their active material. Thus, compared to others, CCM seems to be well under way for such a young technology.

Since CCM devices operate extremely well at cryogenic temperatures, they are very attractive to be used in cryocomputer systems such as superconducting Rapid Single-Flux-Quantum (RSFQ) [33], [34] systems and

quantum processors, which are lacking an ultrafast and energy-efficient cryogenic memory device [35]. Integration of CCM into RSFQ logic is possible using a superconducting element called a nanocryotron (nTron) [36] that is sensitive enough to be triggered by extremely small SFQ pulses (~2 mVps) yet can still produce up to 8 V of output voltage in only ~100 ps [36], [37], which is more than sufficient to drive a CCM device. Integrating SRAM or DRAM into superconducting circuits was also reported, but in order to drive CMOS logic, multiple Josephson junction stacks and amplification stages have to be used, which increases power dissipation and can negatively affect cryocomputer's operation [38], [39]. By replacing the typical voltage amplifiers in such hybrid Josephson-CMOS circuits with nTron drivers, the power consumption can be reduced by an order of magnitude [40], however the non-volatility of the memory is still not realized with this approach, while on the other hand it could be solved using CCM devices. Superconducting computer systems are considered as the solution to the power consumption problem current computers are facing and CCM devices could present a boost in their development.

5 Methods

5.1 Synthesis of 1T-TaS_2

Chemical vapour transport (CVT) method [41] is mostly used to grow high quality bulk 1T-TaS_2 and other TMD crystals. This is done in an evacuated and sealed quartz ampule which is inserted into a furnace with a temperature gradient from T_2~850 K to T_1~750 K (Fig 5a) [41]. For 1T-TaS_2, a mixture of solid sulphur, tantalum and iodine is inserted into the ampule. Iodine serves as a transport agent that forms complexes with the evaporated materials and transports them to the colder side of the ampule, where the crystal grows. The ampule is quenched after the growth in order to freeze the 1T polytype of TaS_2 which otherwise isn't stable at room temperature. The result of CVT growth are millimetre big high-quality crystals (Fig. 5b) which have to be mechanically exfoliated in order to acquire thin films used in CCM devices. After that, laser or electron beam (e-beam) lithography is performed to fabricate metallic contacts.

A more scalable and integrable approach to growing TaS_2 for device applications is by the Molecular Beam Epitaxy (MBE) method, which is schematically presented in Fig. 5c [42]. MBE method is used for epitaxial thin-film deposition and is widely used in the fabrication process of semiconductor devices. In the case of 1T-TaS_2, Ta and S source is needed in an ultrahigh vacuum chamber. The LSAT substrate is preheated to ~1000 K to ensure the growth of 1T polytype and the thickness is monitored *in situ*. After the growth of the

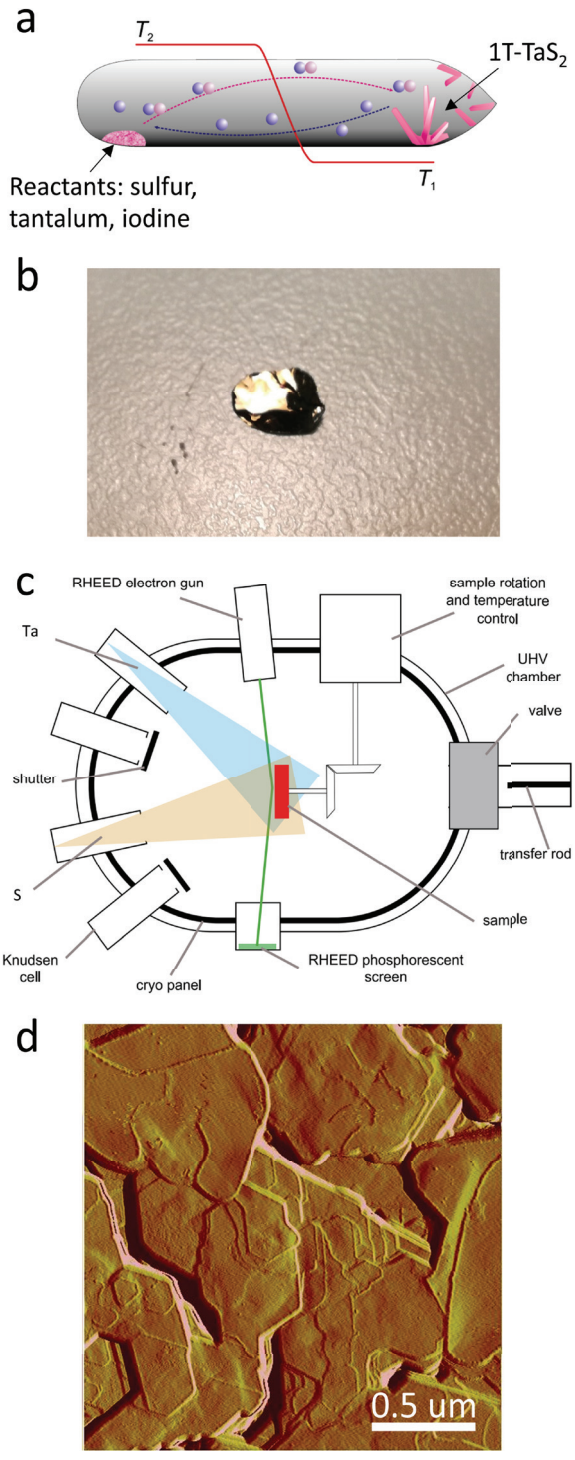

Figure 5: Growth of TaS_2. a) Chemical vapour transport (CVT) reaction in an ampule. Adopted from ref.[41] b) Image of a milimetre big TaS_2 crystal grown by CVT. c) Molecular beam epitaxy reaction in a vacuum chamber. Adopted from ref.[42] d) Atomic force microscope image of TaS_2 surface, grown in an MBE machine.

sample is complete, the sample is quenched to freeze the 1T polytype.

Result of the growth is a thin 1T-TaS_2 film (10–30 nm) fairly uniform over the entire substrate. Atomic force microscope (AFM) image of the MBE grown film is shown in Fig. 5d. To produce CCM devices, the MBE grown films would have to be patterned accordingly using etching and metal contacts would have to be fabricated using laser or e-beam lithography.

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7 Conflicts of interest.

The authors declare no conflict of interest.

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Multi-Objective Optimization Phase-Shift Control Strategy for Dual-Active-Bridge Isolated Bidirectional DC-DC Converter

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Abstract: The dual-active-bridge isolated bidirectional DC-DC converter (DAB-IBDC) is a crucial device for galvanic isolation, voltage conversion, power transfer, and bus connection in the DC power conversion systems. Phase-shift modulation is an effective method to improve DAB-IBDC performance. However, the phase-shift control strategies in the previous literatures mainly focus on optimizing the characteristic of DAB-IBDC in a single aspect. In this paper, to optimize high-frequency-link (HFL) reactive power, current stress, and efficiency simultaneously, a new multi-objective optimization strategy based on dual-phase-shift (DPS) control is proposed. The power characterization, current stress, and power loss of the DAB-IBDC are analyzed. Besides, both the control principle and framework of the proposed control strategy are described in detail. Finally, the experiment results obtained from an established DAB-IBDC prototype are presented to verify the correctness and superiority of the proposed strategy.

Keywords: dual-active-bridge; multi-objective optimization; DPS control strategy; electrical performance

Strategija upravljanja faznega premika z več ciljnimi optimizacijami za dvoaktivni izolirani mostič dvosmernega DC-DC pretvornika

Izvleček: Izolirani dvosmerni DC-DC (DAB-IBDC) pretvornik z dvoaktivnim mostičem je ključna naprava za galvansko izolacijo, pretvorbo napetosti, prenos moči in povezavo vodila v sistemih za pretvorbo enosmerne energije. Modulacija s faznim zamikom je učinkovita metoda za izboljšanje delovanja DAB-IBDC. Vendar se strategije nadzora s faznim zamikom v dosedanji literaturi osredotočajo predvsem na optimizacijo značilnosti DAB-IBDC z enega vidika. V tem članku je za hkratno optimizacijo jalove moči, tokovne napetosti in učinkovitosti visokofrekvenčne povezave (HFL) predlagana nova večpredmetna strategija optimizacije, ki temelji na nadzoru z dvojnim faznim zamikom (DPS). Analizirane so značilnosti moči, tokovne obremenitve in izgube moči DAB-IBDC. Poleg tega sta podrobno opisana tako načelo krmiljenja kot tudi okvir predlagane strategije krmiljenja. Na koncu so predstavljeni rezultati poskusov, pridobljeni iz vzpostavljenega prototipa DAB-IBDC, s katerimi sta preverjeni pravilnost in superiornost predlagane strategije.

Ključne besede: dvojni aktivni mostič; večnamenska optimizacija; strategija krmiljenja DPS; električna zmogljivost

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1 Introduction

With the wide application of direct-current (DC) renewable power sources, DC loads, and storage equipment, DC power conversion systems (PCS) have considerable potential for engineering applications [1-4]. With the development of power electronics, isolated bidirectional DC-DC converters (IBDCs) have become popular for galvanic isolation, voltage conversion, and power transfer in DC PCS [5-6]. Among various IBDCs, the du-

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al-active-bridge (DAB) IBDC with merits of symmetric topology and control structure, the convenience of implement zero voltage switching for switches, bidirectional power transmission, and cascaded modularity, has been studied and applied in the DC PCS. Thanks to the development of novel power devices and technologies, the DAB-IBDC performance is greatly improved under the great efforts of researchers and engineers. The improvements in DAB-IBDC also promote the development of PCS, so bringing lots of technical advantages [7-10].

The improvements of DAB-IBDC in the previous literatures mainly focus on the topology design and optimization, mathematical model derivation, phase-shift modulation strategies, converter control schemes, and soft-switching realization [11-15]. Particularly, the phase-shift control is an effective method to optimize the DAB-IBDC performance [16]. The phase-shift control strategies can be categorized into single-phase-shift (SPS), extended-phase-shift (EPS), dual-phase-shift (DPS), and triple-phase-shift (TPS). With DAB configurations each full bridge is driven with specific phase-shift. While these phase-shifts can differ in DPS they are equal and referred as inner phase-shift, and phase-shift between each full bridge is the outer phase-shift [7]. The SPS has one degree of freedom with outer phase-shift, and the EPS and DPS have two degrees of freedom with inner phase-shift and outer phase-shift, while the TPS has three degrees of freedom with two different inner phase-shifts and an outer phase-shift. In [17], an improved asymmetric modulation for both-side of DAB-IBDC is proposed, enabling the smooth transaction during steady-state operation and minimizing the transient time regardless of equivalent resistance of inductor. In [18], optimized phase-shift modulations are proposed to accelerate the transient response and suppress the DC bias during transient process. In [19-20], a mathematical model of current stress for DAB-IBDC is established, and the minimum current stresses are achieved under DPS and TPS control strategies, respectively. In [21-22], the DAB-IBDCs with soft-switching operation during whole operating range are analyzed, expanding the zero-voltage switching (ZVS) range and promoting efficiency. In [23-24], the power loss and efficiency models are established, and the efficiency optimized modulation schemes based on phase-shift control are developed. Other phase-shift modulation strategies are also proposed in [25-28] to eliminate reactive power, reduce the peak and root-mean-square (RMS) values of HFL current, and enhance light-load performance for DAB-IBDC, respectively. Moreover, the phase-shift strategies with quasi-square-wave, triangle-wave and sine-wave modulation are investigated for improving performance under varied modulation methods [29-30]. Besides, the TPS control strategy is an efficient method to improve the performance of DAB [31-33].

The phase-shift control strategies in the previous literatures have improved the performance of DAB-IBDC effectively. However, most existing phase-shift control strategies only realize the performance optimization in a single aspect (e.g., current stress, reactive power elimination, ZVS behavior, or efficiency performance of DAB-IBDC). The phase-shift control strategy for multi-objective optimization, i.e., simultaneously optimizes various characteristics of DAB-IBDC, has not been considered and discussed yet. Besides, some phase-shift control strategies with optimal phase-shift angle contain lots of electrical parameters, nonlinear equations, or trigonometric calculation, leading to a high computational burden, a complicated process, and a poor real-time characteristic in practical application. In this paper, to address the above problems and achieve the comprehensive optimization for DAB-IBDC, a multi-objective optimization strategy with DPS control is proposed. The proposed strategy can reduce current stress, improve transmission power, and minimize power loss simultaneously. Consequently, the proposed strategy can achieve high efficiency and improve adaptability and practicality for DAB-IBDC, which promotes the application of DAB-IBDC and also accelerates the development of DC PCS.

This paper is organized as follows. The topology, switching behavior based on DPS control, and the performance characteristics including the high-frequency-link (HFL) current stress, power factor, and power loss of the DAB-IBDC are investigated in Section 2. On this basis, a multi-objective optimization based on DPS control is proposed in Section 3. Then, Section 4 provides the experimental results obtained from a built DAB-IBDC prototype to verify the proposed strategy.

2 Performance characteristics of DAB-IBDC under DPS control

The topology of the DAB-IBDC is presented in Fig. 1. The DAB-IBDC is consisted of active full-bridges H_1 and H_2, two DC capacitors C_1 and C_2, an auxiliary inductor L_T and an high-frequency-link (HFL) transformer with a conversion ratio n. $S_1 \sim S_4$ and $D_1 \sim D_4$ are switches and diodes in H_1, respectively, and $Q_1 \sim Q_4$ and $M_1 \sim M_4$ are switches and diodes in H_2, respectively. V_1 and V_2 are DC voltages on two sides of DAB-IBDC, respectively. The energy transfer could be equivalent to the transmission of energy between two modulated voltage sources through equivalent inductor L. i_L is HFL current flowing through the equivalent inductor. v_p is the HFL

voltage on the primary side. v_S is the HFL voltage on the secondary side, which is generated by secondary terminate and equivalent to the primary-side voltage.

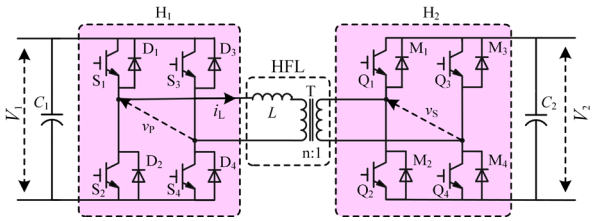

Figure 1: Topology configuration of DAB-IBDC.

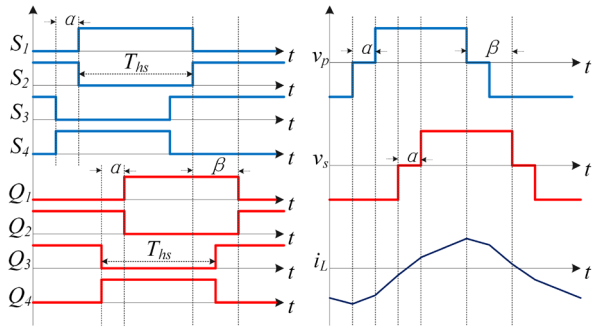

Figure 2: The operation principle, HFL voltages, and currents under DPS control.

Generally, the DPS control has two working modes: the inner phase-shift ratio is larger or smaller than the outer phase-shift ratio, which is determined by the transferred power [7]. Different from EPS and TPS, the inner phase-shift ratios under DPS strategy in active full-bridges on both sides are the same. T_s is the switching period. To avoid the analysis complexity brought from the traditional time-domain segmentation function, the unified model form based on the Fourier series is applied in the analysis and control design. According to the topology of DAB-IBDC, the operation principle, HFL voltages, and currents under DPS control are presented in Fig. 2, where β is the outer phase-shift angle between v_p and v_s, and $\alpha_1 = \alpha_2 = \alpha$ is the inner phase-shift angle.

According to Fourier series, the primary and secondary side HFL voltages v_p and v_s, shown in Fig. 2, are:

$$\begin{cases} v_p(t) = \sum\limits_{k=1,3,5...} \dfrac{4V_1}{k\pi}\cos(\dfrac{k\alpha}{2})\sin(n\omega t) \\ v_s(t) = \sum\limits_{k=1,3,5...} \dfrac{4V_2}{k\pi}\cos(\dfrac{k\alpha}{2})\sin[n(\omega t-\beta)] \end{cases} \quad (1)$$

Since the average inductor current is equal to zero during steady-state, the HFL current i_L in every switching period can be express as:

$$i_L(t) = \int_{t_0}^{t} \frac{v_P(t)-v_S(t)}{L}dt + i_L(t_0) \quad (2)$$

From (1) - (2), the following equations can be obtained:

$$\begin{cases} i_L(t) = \sum\limits_{k=1,3,5...} \dfrac{4}{k^2\pi\omega L}\sqrt{A^2+B^2}\sin(k\omega t+\arctan\dfrac{A}{B}) \\ A = \cos(\dfrac{k\alpha}{2})[V_2\cos(k\beta)-V_1] \\ B = V_2\cos(\dfrac{k\alpha}{2})\sin(k\beta) \end{cases} \quad (3)$$

Thus, the root-mean-square (RMS) value of i_L is:

$$I_{L-RMS} = \sqrt{\sum_{k=1,3,5...} {I_{Lk}}^2} = \sqrt{\sum_{k=1,3,5...} [\frac{2\sqrt{2}}{k^2\pi\omega L}\sqrt{A^2+B^2}]^2} \quad (4)$$

2.1 Transmission power characterization

The average transmission power P can be obtained as:

$$P = \frac{1}{T_{hs}}\int_0^{T_{hs}} v_p(t)\bullet i_L(t)dt \quad (5)$$

Substituting (1) - (3) into (5), the average transmission power P can be further calculated as:

$$P = \sum_{k=1,3,5...} \frac{8V_1V_2}{k^3\pi^2\omega L}\cos^2(\frac{k\alpha}{2})\sin(k\beta) \quad (6)$$

Besides, the reactive power Q can be obtained:

$$\begin{cases} Q_{k_1=k_2=k} = \sum\limits_{k=1,3,5...} \dfrac{8V_1\cos^2(\dfrac{k\alpha}{2})}{k^3\pi^2\omega L}[V_1-V_2\cos(k\beta)] \\ Q_{k_1\neq k_2} = U_{ak_1}I_{Lk_2} = \dfrac{8V_1}{k_1k_2^2\pi^2\omega L}\cos(\dfrac{k\alpha}{2})\sqrt{A^2+B^2} \end{cases} \quad (7)$$

From (6) - (7), the apparent power S is calculated as:

$$S = \sqrt{\sum_{k=1,3,5...} P_k^2 + \sum_{k=1,3,5...} Q_k^2 + \sum_{k=1,3,5...} Q_{k_1\neq k_2}^2} \quad (8)$$

Finally, the HFL power factor λ can be obtained as:

$$\lambda = P/S \quad (9)$$

Based on (6) - (9), Fig. 3 shows the HFL power factors under conventional control strategy. In Fig. 3, the HFL power factor λ is influenced by phase-shift angles, and the HFL power factors under DPS are higher. Besides, under DPS (DPS_1 <DPS_2 <DPS_3), with the increasing of inner angle α, the HFL power factor λ becomes higher correspondingly, decreasing HFL reactive power and increasing efficiency of DAB-IBDC.

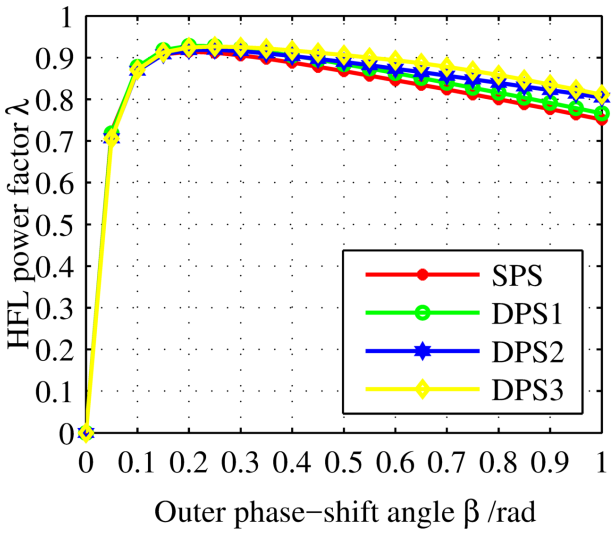

Figure 3: HFL power factors of DAB-IBDC.

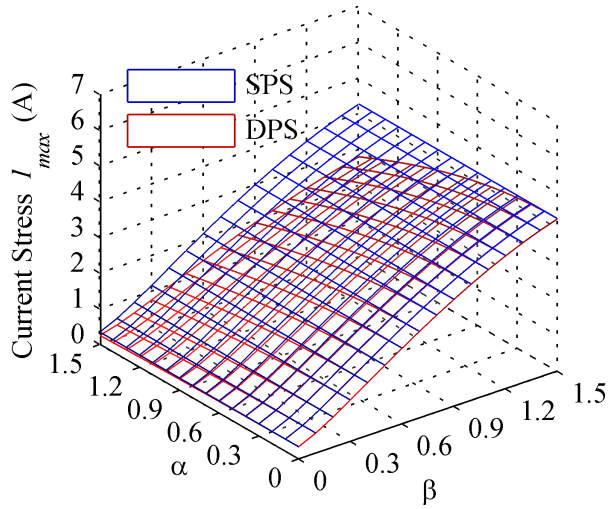

Figure 4: The current stress of DAB-IBDC.

2.2 Current stress characterization

To prolong the service life of switching devices, and improve the efficiency of DAB-IBDC, reducing the current stress is an effective solution. In the DAB-IBDC, the maximum value of HFL current i_L represents the current stress. From (3), it can be observed that the HFL current i_L compromises components with different frequencies under Fourier series analysis. Since the fundamental component in HFL current i_{L1} is approximated with HFL current i_L during operation, the maximum value of the fundamental component of i_L can be considered as the current stress I_{max}:

$$I_{\max} = \max\{|i_{L1}(t)|\} = \frac{2V_2\cos(\frac{\alpha}{2})\sqrt{1+M^2-2M\cos(\beta)}}{\pi\omega L} \quad (10)$$

where $M = V_1 / nV_2$ is the voltage conversion ratio of DAB-IBDC.

According to (10), the current stress is closely related to V_1, V_2, α, β, and M. Fig. 4 presents the current stress I_{max} with the different α and β under the SPS and DPS control. From Fig. 4, it can be observed: 1) with the increase of outer β, the current stress I_{max} increases under these two strategies, 2) under the same outer β, the current stress produced by DPS control is kept smaller. Besides, the current stress can be reduced with the increase of phase-shift α under DPS.

2.3 Power loss characterization

For DAB-IBDC, its total power loss P_{LOSS} mainly contains conducting loss P_{CON}, switching loss P_{SW}, and loss of magnetic components P_{TA} [24].

$$P_{\text{LOSS}} = P_{\text{CON}} + P_{\text{SW}} + P_{\text{TA}} \quad (11)$$

(1) Conducting loss: From the topology of DAB-IBDC, the conducting loss P_{CON} is the sum of conducting losses in switches and diodes namely P_{CONS} and P_{COND}, respectively. For the DAB-IBDC, the dead-band loss should be considered and could not be ignored. As the zero-voltage-switching (ZVS) for DAB-IBDC can be also realized by using the freewheeling of anti-parallel diodes during dead-band time. Thus, the dead-band current is freewheeling in diodes, which means the dead-band loss can be considered as a part of conducting loss. For simplicity, assume that the diodes and switches in DAB-IBDC have the same conducting resistance R_{CON}. Besides, the conducting loss is closely related to the RMS HFL current in primary bridge H_1 and secondary bridge H_2 namely I_1 and I_2, respectively. The relationship between I_1 and I_2 is $I_1 = I_2 / n = I / \sqrt{2}$. Consequently, the conducting loss of switches and diodes in a switching period are:

$$P_{\text{CON}} = 4R_{\text{CON}}I_1^2 + 4R_{\text{CON}}I_2^2 = 2(1+n^2)R_{\text{CON}}I_{\text{L-RMS}}^2 \quad (12)$$

Based on (12), the conduction losses P_{CON} is mainly decided by RMS current $I_{L\text{-RMS}}$ of HFL. Under both SPS and DPS control, the conduction loss P_{CON} for DAB-IBDC are presented in Fig. 5(a), and they are normalized by $P_{CON} = 2(1 + n^2) R_{CON} I_{L\text{-max}}{}^2$. Obviously, with the increase of phase-shift angle β, the conduction loss P_{CON} increases, while P_{CON} under DPS is always smaller. Besides, the conduction loss P_{CON} drops with the increase of inner phase-shift α.

(2) Switching loss: From [24], with the same transfer power, switching loss is relatively smaller compared with the conducting loss and the loss of magnetic components, and it only accounts for a small proportion of the overall power loss of DAB-IBDC. Besides, under soft-switching achievement, the switching loss can be neglected. Thus, for simplicity, the switching loss is ignored here.

(3) Loss of magnetic components: In DAB-IBDC, magnetic components include the transformer and the auxiliary inductor. Typically, the power loss of magnetic component consists of the copper loss and core loss. Assuming that the winding resistance of magnetic components is constant, the copper loss P_{COPP} is closely related to the RMS value of i_L. In addition, the RMS value of i_L also plays a major role in the core loss P_{CORE}. The power loss of magnetic components P_{TA} can be obtained as:

$$P_{TA} = P_{COPP} + P_{CORE} = (R_{tr} + R_{au} + \frac{2mf_s\mu_0^2N^2V_e}{g^2})I_{L\text{-}RMS}^2 \quad (13)$$

where R_{tr} is the transformer winding resistance while R_{au} is auxiliary inductor winding resistance. m represents the specific parameter of core loss, μ_0 represents the permeability of vacuum, N represents the number of turns, V_e represents the effective core volume, and g represents the air gap of magnetic path.

Based on (13), the power loss P_{TA} is affected by the RMS current $I_{L\text{-}RMS}$ of HFL. Fig. 5(b) shows the curves of normalized power loss of magnetic components P_{TA} for DAB-IBDC under DPS, in which they are normalized by $P_{TA}=(R_{tr}+R_{au}+2mf_su_0^2N^2V_e/g_2)I_{L\text{-}max}^2$. It is obvious that, the power loss P_{TA} increases with the raise of outer angle β, which is smaller under DPS compared with SPS. Besides, the P_{TA} reduces with the raise of the inner angle α.

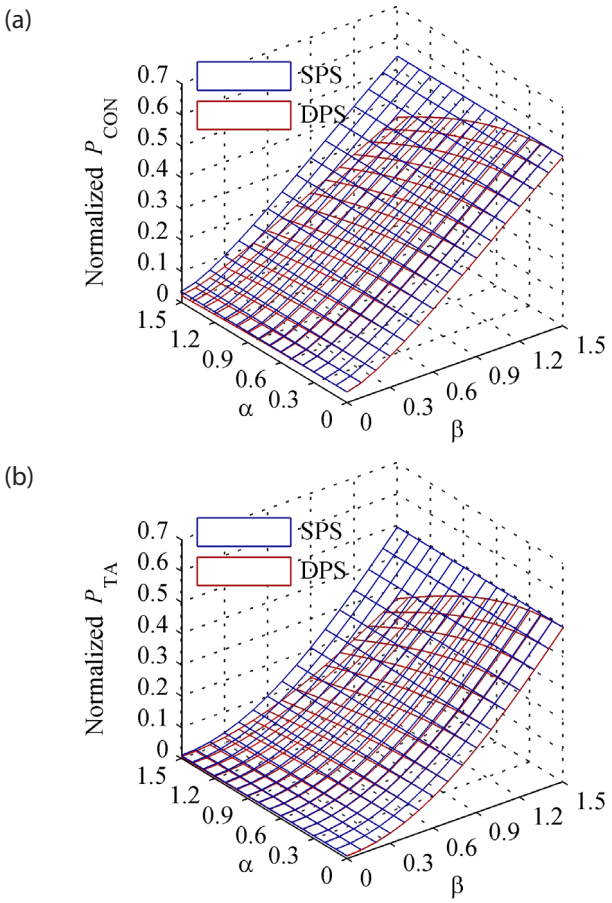

Figure 5: The power loss for DAB-IBDC. (a) Conducting loss, (b) Loss of magnetic components.

3 Multi-objective optimized strategy based on DPS control

From the analysis above, in the DAB-IBDC, all the HFL reactive power, current stress, and efficiency performance could be optimized by DPS strategy simultaneously. Accordingly, an optimized strategy based on DPS control is investigated for DAB-IBDC.

The current stress I_{max}, conducting loss P_{CON}, and loss of magnetic components P_{TA} are:

$$\begin{cases} I_{max} = I_L = \sqrt{2}I_{L\text{-}RMS} \\ P_{con} = 2(1+n^2)R_{CON}I_{L\text{-}RMS}^2 \\ P_{TA} = (R_{tr} + R_{au} + \frac{2mf_s\mu_0^2N^2V_e}{g^2})I_{L\text{-}RMS}^2 \end{cases} \quad (14)$$

From (14), it could be seen that the current stress of DAB-IBDC is affected by the RMS value of HFL current $I_{L\text{-}RMS}$. Besides, the conducting loss P_{CON} and loss of magnetic components P_{TA} are also mainly affected by the RMS current of HFL. Thus, through optimizing the HFL current, the current stress, power loss, and the efficiency can be all optimized. Once the optimal RMS value of HFL current is obtained, the optimization of current stress and efficiency for DAB-IBDC could be realized at the same time.

To obtain the optimal RMS value of HFL current, a Lagrangian objective function is constructed:

$$E(\alpha,\beta,\lambda) = I_{L\text{-}RMS}(\alpha,\beta) + \lambda(P(\alpha,\beta) - P_0) \quad (15)$$

where P_0 is the calculated output power for DAB-IBDC, which is obtained through multiplying the reference output voltage V_{2ref} by the output current I_2. Substituting (6) and (10) into (15), the constraints of the optimal equation can be obtained as:

$$\begin{cases} E = \frac{2nV_2\cos(\frac{\alpha}{2})\sqrt{1+M^2-2M\cos(\beta)}}{\pi\omega L} + \\ \quad \lambda[\frac{4V_1V_2n}{\pi^2\omega L}\cos^2(\frac{\alpha}{2})\sin(\beta) - P_0] \\ \frac{\partial E}{\partial\alpha} = \sqrt{1+M^2-2M\cos(\beta)} + \frac{4\lambda V_1}{\pi}\cos(\frac{\alpha}{2})\sin(\beta) = 0 \\ \frac{\partial E}{\partial\beta} = \frac{M\sin(\beta)}{\sqrt{1+M^2-2M\cos(\beta)}} + \frac{2\lambda V_1}{\pi}\cos(\frac{\alpha}{2})\cos(\beta) = 0 \\ \frac{\partial E}{\partial\lambda} = \frac{4V_1V_2n}{\pi^2\omega L}\cos^2(\frac{\alpha}{2})\sin(\beta) - P_0 = 0 \end{cases} \quad (16)$$

From (15) and (16), the optimal solution (α, β) for DAB-IBDC under DPS control can be obtained by the results of the nonlinear equations in (16), and the DPS-based optimized strategy for DAB-IBDC is presented in Fig. 6. For the proposed strategy, the outer angle β is obtained from the output voltage control loop. An optimized calculation model is used to obtain the inner angle α for reducing the current stress/power loss and improving the efficiency of DAB-IBDC.

From (16), the common solution and Pareto front of optimization for inner angle α is further obtained:

$$\alpha = \arccos\sqrt{\frac{P_0\pi^2\omega L}{nV_1V_2\sin(\beta)}} \tag{17}$$

From (17), since the fluctuations in switching frequency and inductance value are very small compared with the magnitude of normalized transmission power and DC voltages, their influence on optimization result will be very small. Therefore, the optimal inner phase-shift angle α is mainly determined by outer phase-shift angle β, relatively fixed parameters normalized transmission power P_o, the HFL voltage ratio n, and also DC voltages V_1 and V_2.

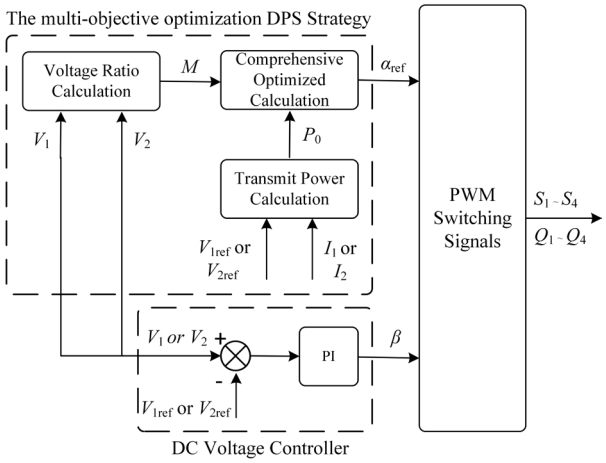

Figure 6: Control framework of proposed multi-objective optimized DPS strategy for DAB-IBDC.

4 Experiment verification

To verify the proposed control strategy, a 1kW rated DAB-IBDC prototype is established, and the load power rating is rated 1kW. The detailed parameters are presented in Table 1, and the prototype is shown in Fig. 7.

Table 1: Parameters of DAB-IBDC Prototype.

Parameters	Value	Symbol
Primary Side DC Voltage	50V ~ 150V	V_1
Secondary Side DC Voltage	50V ~ 150V	V_2
Switching Frequency	20kHz	f_s
Transformer Turn Ratio	1 : 1	n
HFL Equivalent Inductor	30uH	L
DC-link Capacitance	150uF	C_1, C_2
Load Resistance	10Ω ~ 100Ω	R

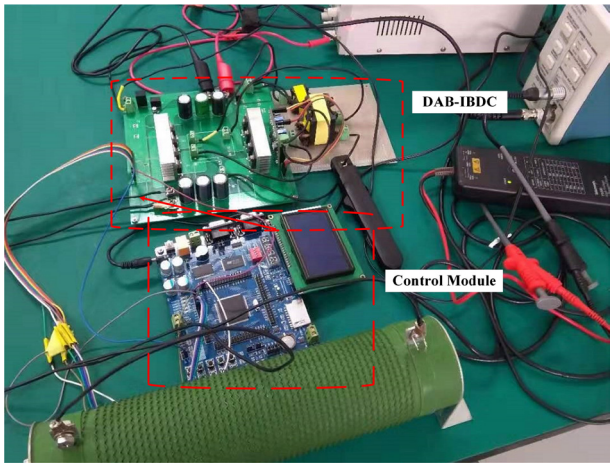

Figure 7: The prototype of DAB-IBDC.

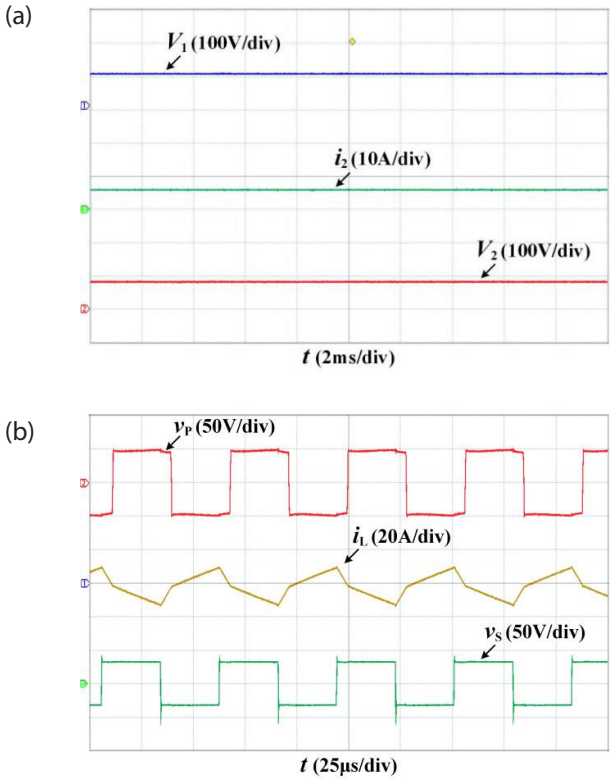

Figure 8: Experiment waveforms under SPS. (a) DC side voltages and current, (b) HFL voltages and current.

For the DAB-IBDC, Fig. 8 shows the steady-state experiment waveforms under SPS control. It can be seen that, the V_1 on the primary DC side is 100V, and the V_2 on the secondary DC side is regulated at the designed 80V. The HFL voltages v_P and v_S are both high-frequency square waves, and the frequencies of v_P, v_S and i_L are 20kHz. Besides, since the DC voltages deviate from the conversion ratio 1:1, the HFL current stress and reactive power become high. However, the SPS control could not solve this issue, and the maximum value of HFL current is 10.1A.

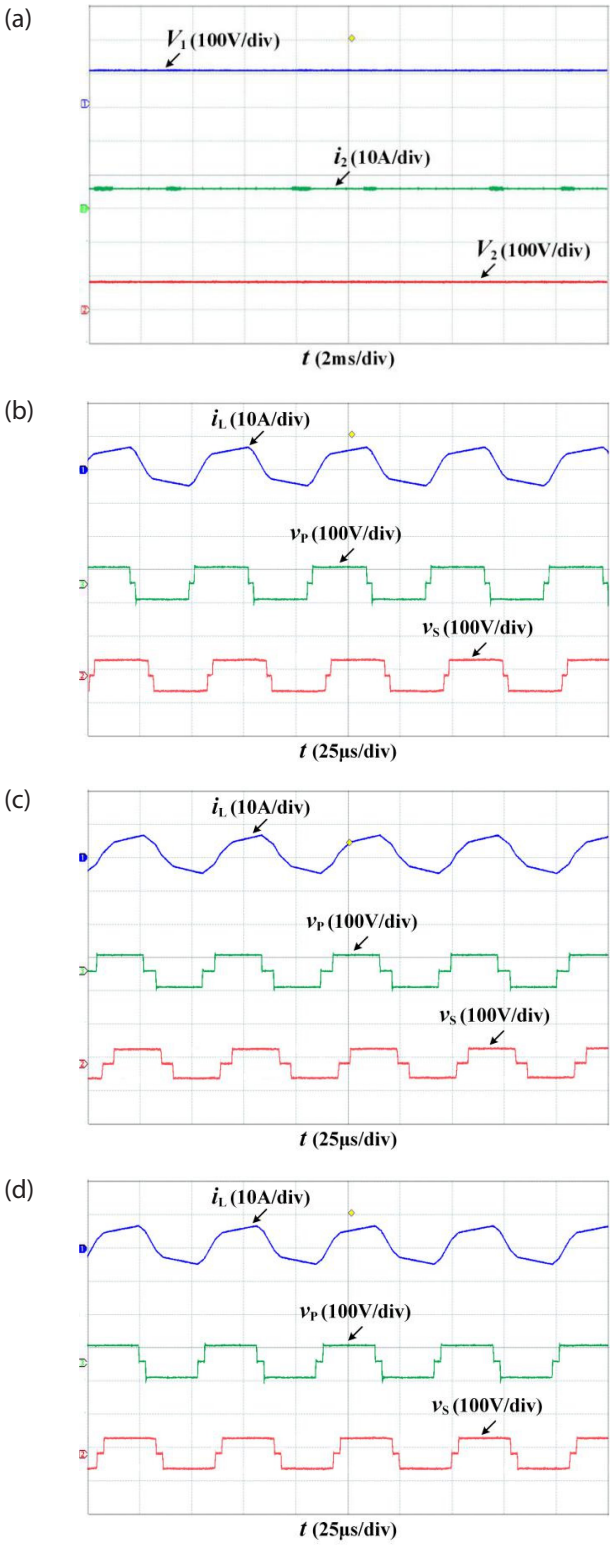

Figure 9: Experiment waveforms under conventional and proposed optimized DPS. (a) DC side Voltages and current of DAB-IBDC, (b) Conventional DPS when α = 0.12, (c) Conventional DPS when α = 0.25, (d) Proposed optimized DPS when α = 0.18.

With the same transmission power, Fig. 9(a) and Fig. 9(b) show the experiment waveforms of DAB-IBDC under the conventional DPS control. It can be seen that the DAB-IBDC operates normally, i.e., V_1 is 100V and V_2 is also regulated at the designed 80V. Besides, the HFL current stress and reactive power under DPS control are lower than that under SPS control. Thus, the DPS strategy is able to improve the performance of the DAB-IBDC by reducing the maximum value of HFL current to 9.4A. Moreover, steady-state experiment waveforms of HFL current under conventional DPS and proposed optimized control are presented in Fig. 9(c) and Fig. 9(d). It can be seen that the conventional DPS with a larger inner phase-shift angle can further reduce the HFL current stress and reactive power, and the value of HFL current under the proposed optimized DPS control can reduce to 8.7A. Accordingly, the HFL current stress and reactive power under proposed optimized DPS control

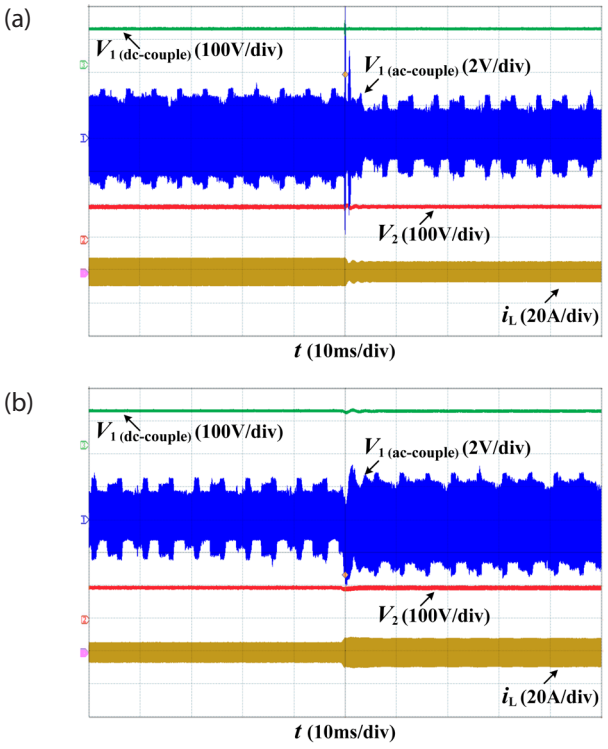

Figure 10: The dynamic-state experiment waveforms of DAB-IBDC under proposed optimized DPS strategy. (a) Load varies from 100% to 50%; (b) Load varies from 50% to 100%.

are lowest compared with that under SPS and conventional DPS.

The dynamic-state waveforms of the DAB-IBDC under the proposed optimized DPS strategy are presented in Fig. 10. According to Fig. 10(a), when the load varies from 100% to 50%, the voltage ripple of V_1 decreases, and V_2 maintains at 100V. Besides, the HFL current stress i_L decreases correspondingly. Similarly, when the load varies from 50% to 100%, the voltage ripple of V_1 increases, and V_2 keeps at 100V. In addition, the HFL current stress i_L increases correspondingly, according to Fig. 10(b). Based on the above analysis, it can be concluded that under the proposed optimized DPS strategy, the DC voltages on both sides of DAB-IBDC maintain at designed value, and the DAB-IBDC operates stably during the dynamic-state.

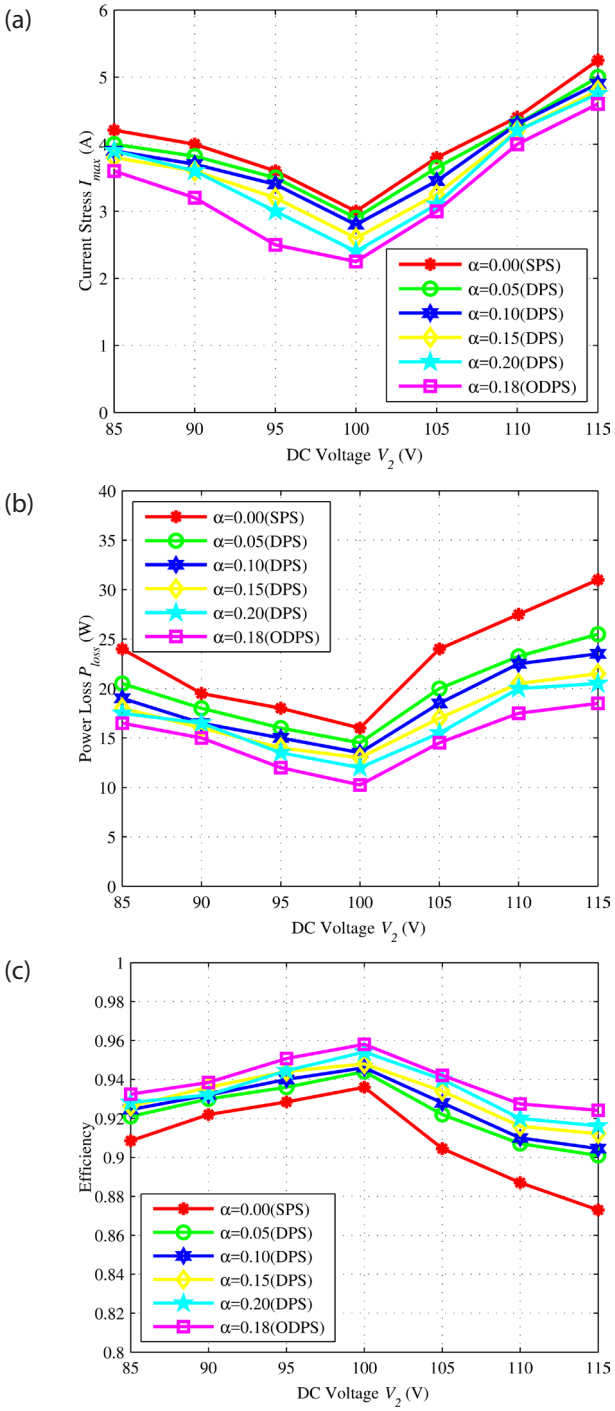

Figure 11: Experimental curves under conventional strategies and proposed optimized DPS (ODPS) strategy. (a) Curves of current stress, (b) Curves of power loss, (c) Curves of efficiency.

With the same transmission power and varied DC voltages, Fig. 11(a) shows the current stress of DAB-IBDC under conventional strategies and proposed optimized control strategy. From Fig. 11(a), it can be observed that: under the three control strategies, the lowest current stress occurs when $V1 = V2 = 100V$. However, the current stress would become higher because the conversion ratio deviates from 1:1 farther (e.g., $V2$ drops from 100V to 85V or increases from 100V to 115V). Also, the current stress under DPS control is lower than that under SPS control, and increasing the inner phase-shift angle can further reduce the current stress. In addition, the proposed optimized DPS strategy achieves the lowest current stress for DAB-IBDC among the three strategies.

Similarly, Fig. 11(b) and Fig. 11(c) present the power loss and efficiency of DAB-IBDC under conventional control strategies and proposed optimized control strategy, respectively. Similar to the results of current stress experiments, under various phase-shift control strategies, the lowest power loss can be achieved when $V1 = V2 = 100V$. Once $V2$ varies and deviates from the conversion ratio 1:1, it would result in larger power loss and lower efficiency. Meanwhile, lower power loss is achieved by the DPS strategy compared with that under the SPS strategy. Increasing the inner phase-shift angle α can further reduce power loss. In addition, the proposed optimized strategy realizes the lowest power loss, so as to obtain the highest efficiency for DAB-IBDC. Thus, the proposed multi-objective optimized strategy improves the efficiency of DAB-IBDC.

5 Conclusions

The DAB-IBDC plays a crucial role in DC distribution networks for realizing galvanic isolation, voltage conversion, power transfer, and bus connection. In this paper, the effect of phase-shift control on power transmission characteristic, current stress, and efficiency of DAB-IBDC is analyzed in detail. Then, to optimize these three features simultaneously, a DPS-based multi-objective optimized control strategy is proposed. The experi-

ment results obtained from a built DAB-IBDC prototype verify that 1) the DPS control realizes less HFL reactive power, lower current stress, and higher efficiency for DAB-IBDC compared with SPS control, 2) the proposed optimized DPS control strategy optimizes the three features of DAB-IBDC simultaneously. Accordingly, the proposed control strategy can effectively improve the performance of DAB-IBDC, which makes it more adaptable and practical in DC power conversion networks.

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7 Conflict of interest

The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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A Placement and Routing Method for Layout Generation of CMOS Operational Amplifiers Using Multi-Objective Evolutionary Algorithm Based on Decomposition

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Abstract: This paper presents a new placement and routing method for layout generation of CMOS operational amplifiers (op-amps). Both circuit sizing and layout generation stages are performed automatically. In the proposed method, layout effects are considered during the layout generation. Layout parasitics and geometry information are extracted from a new automated layout generator. In this method, the multi-objective evolutionary algorithm based on decomposition (MOEA/D) is used as an optimization algorithm. In order to verify the performance of the proposed method, the design of three-stage operational amplifier (op-amp) and two-stage class-AB operational trans-conductance amplifier (OTA) in a 0.18µm process CMOS technology with 1.8 V supply voltage are presented. The simulation results indicate the efficiency of the proposed analog layout generation method.

Keywords: Analog layout generation; Circuit sizing; Automated placement and routing; MOEA/D; Three-stage operational amplifier

Metoda umeščanja in usmerjanja za generiranje postavitve operacijskih ojačevalnikov CMOS z uporabo večciljnega evolucijskega algoritma na osnovi dekompozicije

Izvleček: Članek predstavlja novo metodo umeščanja in usmerjanja za izdelavo postavitve operacijskih ojačevalnikov CMOS (op-amperov). Fazi določanja velikosti vezja in generiranja postavitve se izvajata samodejno. Pri predlagani metodi se med generiranjem postavitve upoštevajo učinki postavitve. Parazitske lastnosti postavitve in informacije o geometriji se pridobijo iz novega samodejnega generatorja postavitve. V tej metodi se kot optimizacijski algoritem uporablja večobjektni evolucijski algoritem, ki temelji na dekompoziciji (MOEA/D). Da bi preverili učinkovitost predlagane metode, sta predstavljeni zasnova tristopenjskega operacijskega ojačevalnika (op-amp) in dvostopenjskega operacijskega ojačevalnika razreda AB (OTA) v tehnologiji CMOS z 0,18 µm procesom in napajalno napetostjo 1,8 V. Rezultati simulacije kažejo učinkovitost predlagane metode generiranja analogne postavitve.

Ključne besede: Generiranje analogne postavitve; Določanje velikosti vezja; Avtomatizirano umeščanje in usmerjanje; MOEA/D; Tristopenjski operacijski ojačevalnik

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1 Introduction

Analog circuit design includes three main steps as follows [1], [2], [3], [4]: topology synthesis / selection, circuit sizing and layout design. In the first step, a proper circuit topology is selected by a designer. The second step is sizing devices with the aim of finding proper width and length of the transistors, passive components values,

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bias voltages and currents. Finally, the layout should be generated from the previous step. In the analog integrated circuit (IC) design, it is often required to optimize different specifications simultaneously. Designing the circuit can be performed manually which is a difficult task and takes lots of time. There are large number of circuit sizing methods in the literature [5], [6], [7], [8], [9]. In the knowledge-based approach, sizes of circuit devices are determined based on some pre-defined design flows and databases. However, this method is time-consuming and there is no guarantee to convergence to the global optimum solution. Optimization-based methods can be divided into three categories as follows: "equation-based", "simulation-based" and "equation and simulation-based" methods [10], [11]. In the equation-based method, mathematical solvers are used to solve the circuit equations and satisfy the target specifications. In the simulation-based method, a circuit simulator is used to evaluate the target specifications for a set of design variables. Finally, to have a compromise between speed and accuracy of the two mentioned methods, equation and simulation-based method was utilized in some designs [12].

Automatic analog layout generation has been considered by analog circuits designers [13]. In the literature, several Computer-Aided Design (CAD) tool [14], [15]. shave been introduced for analog circuits layouts. However, circuit sizing and layout generation steps are not regarded simultaneously. Since circuit performance can be influenced by layout parasitics, the circuit specifications may not be satisfied after post-layout simulation. The behavior of analog integrated circuits is sensitive to layout-induced parasitics. To achieve desired specifications, time-consuming and non-systematic iterations between these circuit sizing and layout synthesis are required [16]. If these issues are not taken into account, circuit overdesign may occur which results in wasting power and area. On the other hand, circuit underestimation may lead to a worsening of post-layout performance. It is useful to perform circuit sizing and layout generation steps automatically.

Some approaches have been proposed in the analog circuit domain to assist the designers. But some procedures should be performed manually. Optimization-based sizing approaches are employed for analog IC design automation using the circuit simulators as evaluation engines [17], [18]. The quality of a design is evaluated by the degree to which constraints are satisfied and also desired specifications are achieved. In order to achieve the better sizing results, the layout effects should be considered. The layout-aware sizing method consists of parasitic-aware sizing and geometry-aware sizing [19], [20]. In parasitic-aware sizing method, parasitics of the layout are extracted continuously and then they are utilized in the sizing process. In the geometry-aware sizing method, the value of geometrical parameters such as width, length, and the number of fingers of MOS transistors are chosen such that the layout area and shape to be optimized. Several analog layout-aware sizing methods have been introduced in the literature.

Parametric generators are used that code the whole layout of the circuit to increase execution speed. However, their definition is time-consuming and the solutions for devices' sizes may differ from the ones intended in the definition step [21], [22], [23]. In Ref [24], a predefined floorplan template supported by a slicing tree is used. To obtain the desired geometric features, the number of fingers of MOS transistors should be adjusted. A similar idea is suggested by minimizing the placement area using convex optimization [25]. However, placement solutions are not compact. In Ref [26], parasitics estimation are performed without actual layout generation. However, these methods suffer from the fixed layout template used for layout generation or parasitic model construction. A method to model the parasitics associated with inductors during RF circuit synthesis is suggested [27]. The post-layout results may not be acceptable since other parasitics are not considered. A method is proposed to estimate parasitics from earlier placement information and includes this during the circuit resizing stage. Since the parasitic information is related to a single design, it does not take the parasitic variation and it may not be sufficient to use in resizing stage [28].

Layout with templates and commercial extractors is used in Ref [29], In this method, symbolic analysis is employed to combine the parasitics with the performance models. But, geometrical information is not taken into account. A parasitic-aware sizing method is suggested in Ref [30], This method is only applicable to a pre-defined floorplan. A placement and routing method for analog layout generation based on a modified cuckoo optimization algorithm (MCOA) is introduced in Ref [31] In this method, layout parasitics are considered to avoid performance deterioration. But, the placement and routing stages have some shortcomings as it will be discussed in this paper. In Ref [32], an automatic method to generate chip floorplans is proposed. The obtained results are superior or comparable to the solutions produced by designers in terms of power consumption, performance and chip area. In order to achieve this aim, chip floorplanning is considered as a reinforcement learning problem. An edge-based graph convolutional neural network architecture is introduced which has the characteristics of learning rich and transferable representations of the chip.

This paper presents a new technique for placement and routing in analog layout generation using the MOEA/D.

Circuit performance and layout effects are considered in the proposed method. In addition, geometrical information is regarded in the proposed method. The rest of the paper is organized as follows: Multi-objective evolutionary algorithm based on decomposition is introduced in Section 2. The proposed automatic analog layout generation method is described in Section 3. Simulation results are provided in Section 4. Finally, the conclusion is given in Section 5.

2 Multi-objective evolutionary algorithm based on decomposition (MOEA/D)

At present, engineering designs are not usually a simple optimization problem. Multiple objectives are usually desired especially when conflicting operations exist between the optimization searching for different design specifications. During the past decades, evolutionary multi-objective optimization (EMO) has been used by many researchers in the area of intelligent computing [33], [34]. EMO algorithms have advantages in exploring a set of Pareto-optimal solutions compared to traditional methods. Many EMO algorithms utilize Pareto dominance for fitness assignment. In these algorithms, the fitness value of each individual is achieved by comparing it with other individuals in terms of Pareto dominance. therefore, all non-dominated solutions in the population should have the best fitness value.

In this paper, multi-objective optimization problems can be considered as follows:

$$\begin{aligned} &\text{Minimize}\,(f_1(x), f_2(x), \ldots, f_M(x)) \\ &\text{Subject to}\, g(x) \geq 0, X_L < x < X_H \end{aligned} \tag{1}$$

where $f_i(x)$, $i = 1 \ldots M$ is the objective function, M is the number of objectives, x includes design variables, and X_L and X_H are their lower and upper bounds, respectively. The vector $g(x) \geq 0$ represents the design constraints.

A multi-objective evolutionary algorithm based on decomposition (MOEA/D) has been proposed for multiobjective optimization problem (MOP) [35]. In MOEA/D, a MOP is decomposed into several scalar subproblems in which the optimization is performed simultaneously. Using the information on solutions of neighborhood subproblems, this method has less computational cost, which has been proved by several numerical tests.

The motivation of MOEA/D is to decompose a multi-objective optimization problem into several scalar optimization sub-problems using a scalar function. In this method, optimization is performed simultaneously by the evolutionary algorithm. In MOEA/D, each non dominated solution of the multi-objective optimization problem is related to an optimal solution of the single objective optimization problem and it is computed using a specific weight vector. MOEA/D uses a set of weight vectors to set up different search directions, and different weight vectors will direct to search the different regions of the objective space. The Tchebycheff method can be used to decompose a multi-objective optimization problem into N sub-problems. In this method, the objective function of the *jth (j=1, 2, ..., N)* sub-problem is as follows:

$$g^{te}(x \mid \lambda^j, z^*) = \max_{1 \leq i \leq m} \left\{ {\lambda_i}^j \mid f_i(x) - z_i^* \mid \right\} \tag{2}$$

where $\lambda^j = \left({\lambda_1}^j, \ldots, {\lambda_m}^j\right)^T$ demonstrates a weight vector, $z^* = \left(z_1^*, \ldots, z_m^*\right)^T$ represents the vector of reference points. For each Pareto optimal point x^* there exists a weight vector so that x^* is the optimal solution of (2). The methods to determine the weight vector can be found in the related references such as Ref [36]. It should be mentioned that each optimal solution of Eq. (2) is a Pareto optimal solution of the problem of Eq. (1).

3 Proposed Placement and Routing Method

In this Section, the proposed placement and routing stages based on the MOEA/D are described.

3.1 Placement

In the placement stage, the area of floorplan is optimized by simultaneous consideration of symmetry and proximity constraints. It is necessary to place the devices by considering symmetry and proximity constraints to alleviate the parasitic coupling effects and also to improve circuit performance. Therefore, they are briefly reviewed here [37]. A set of m symmetry groups can be shown by $S = \{S_1, S_2, \ldots, S_m\}$. The coordinates of the symmetry axes are indicated by $(\hat{x}_i, \hat{y}_i)$. A member of the groups is described as follows:

$$\begin{aligned} S_i = \{&(\mathrm{M}_1, \mathrm{M}_1'), (\mathrm{M}_2, \mathrm{M}_2'), \ldots, (\mathrm{M}_u, \mathrm{M}_u') \\ &, \mathrm{M}_1^s, \mathrm{M}_2^s, \ldots, \mathrm{M}_v^s\} \end{aligned} \tag{3}$$

This group includes u symmetry pairs $(\mathrm{M}_j, \mathrm{M}_j')$ with coordinates centers (x_j, y_j) and (x_j', y_j') and v self-symmetric modules M_k^s with coordinate center (x_s^k, y_s^k). The conditions for symmetry group with vertical symmetric axis are indicated by (4) - (6), and

equations set (7) - (9) are used for those with horizontal axis.

$$x_j + x'_j = 2 \times \hat{x_i}, \ \forall i = 1, 2, ..., u. \quad (4)$$

$$y_j = y'_j, \ \forall i = 1, 2, ..., u. \quad (5)$$

$$x_s^k = \hat{x_i}, \ \forall k = 1, 2, ..., v. \quad (6)$$

$$x_j = x'_j, \ \forall i = 1, 2, ..., u. \quad (7)$$

$$y_j + y'_j = 2 \times \hat{y_i}, \ \forall i = 1, 2, ..., u. \quad (8)$$

$$y_s^k = \hat{y_i}, \ \forall k = 1, 2, ..., v. \quad (9)$$

The proximity condition is described as follows:

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2 \quad (10)$$

where Δ*P* is the difference of an electrical parameter *P*, A_p is the area proportionality constant for *P*, *W* and *L* are the respective width and length of the device, and S_p is the variation of *P* under the device spacing D_x. As can be seen from the above equation, it is necessary to place the symmetry group together as close as possible.

For two groups of modules such as A and B, a common centroid constraint is defined as below:

$$\sum_{a \in A} \left(x_a + \frac{\omega_a}{2} \right) = \sum_{b \in B} \left(x_b + \frac{\omega_b}{2} \right) \quad (11)$$

$$\sum_{a \in A} \left(y_a + \frac{h_a}{2} \right) = \sum_{b \in B} \left(y_b + \frac{h_b}{2} \right) \quad (12)$$

In the above equations, (x, y) and (ω*h*) show the lower left coordinates and the width and height of the modules, respectively.

In addition, design rules should be satisfied at this stage. A method for handling constraints would be to consider them as new objective functions. If g(x) ≥ 0 must hold, for instance, we can transform this to a new objective function $f_{new}(x) = \min\{-g(x), 0\}$ subject to minimization.

The devices to be placed on the floorplan are represented by *k* modules $M_1, \ldots, M_k$. The objective functions are defined for the placement stage as follows:

$$f_P(x) = (f_{oP1}(x), -f_{oP2}(x)) \quad (13)$$

$$f_{oP1}(x) = Width_{floorplan} \times Height_{floorplan} \quad (14)$$

$$f_{oP2}(x) = \frac{Total\ Blocks\ Area}{Width_{floorplan} \times Height_{floorplan}} \quad (15)$$

In the above equation, $x = \{(x_1, y_1), ..., (x_k, y_k)\}$ indicates the coordinates of the left-bottom corners of the modules, $f_{oP1}(x)$ is the area of the floorplan. $Width_{floorplan}$ and $Height_{floorplan}$ represent the floorplan width and height, respectively. The term area utilization is defined by $f_{oP2}(x)$ and it is no greater than 1. It is worth to mention that the $f_p(x)$ is formulated to deal with a minimization optimization problem. In the placement stage, optimization is performed using the MOEA/D.

3.2 Routing

The routing stage aims to electrically connect the terminals of the layout devices such as transistors, capacitors, differential pairs. In this proposed method, each wire is divided into d segments. Each segment is represented by segment direction, segment layer. Segment direction can be defined as up, down, left, and right. Segment is located in the layers from 1 to n, where n is the number of the layers.

Positions of the segments are adjusted automatically so that the wire length between terminal pairs to be minimized. The objective functions for the routing stage are proposed as follows:

$$f_R = (f_{oR1}(x), f_{oR2}(x), f_{oR3}(x)) \quad (16)$$

$$f_{oR1}(x) = \sum_{i=1}^{d} Length_{Segment_i} \quad (17)$$

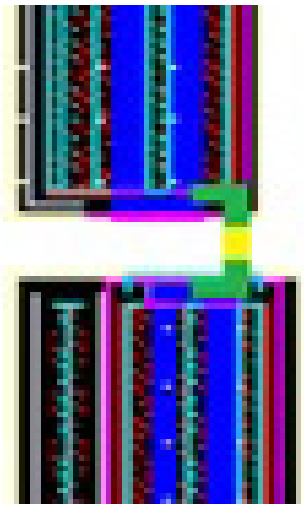
$$f_{oR2}(x) = Number\ of\ Vias \quad (18)$$

$$f_{oR3}(x) = Number\ of\ bends \quad (19)$$

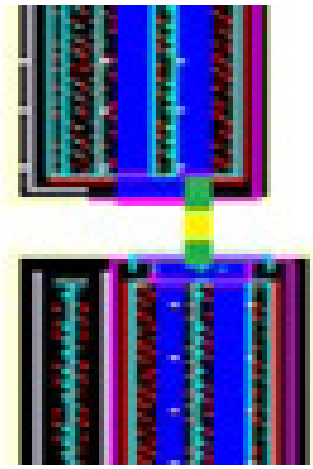
Where $f_{oR1}(x)$ is the sum of the segment lengths from the starting terminal (T_S) to the target terminal (T_E) (See Figure1). $(x_{T_S}, y_{T_S}, z_{T_S})$ and $(x_{T_E}, y_{T_E}, z_{T_E})$ are the coordinates of the starting terminal and the target terminal, respectively. $f_{oR2}(x)$ is the number of vias in the wire. $f_{oR3}(x)$ is the number of bends in the wire and it is defined to avoid unnecessary change of direction between adjacent segments. It is worth to mention that it is not considered in the Ref [31]. Current-density to determine the segment width and design rules are the constraints in the routing stage. An example of wiring progress using the proposed method is demonstrated in Figure 2. In this Figure, different segment colors indicate transition between layers.

Figure 1: Wire segmentation in the proposed method.

(a)



(b)



(c)

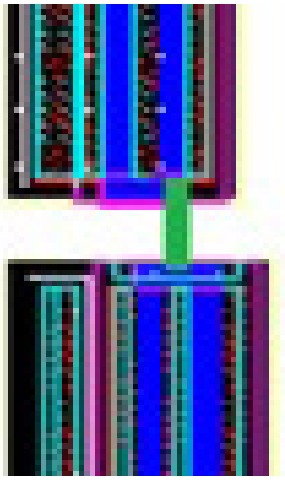


Figure 2: Example of routing stage progress using the proposed method: **(a)** Wiring between two terminals after 1 generation, **(b)** Wiring between two terminals after 10 generations, **(c)** Wiring between two terminals after 100 generations.

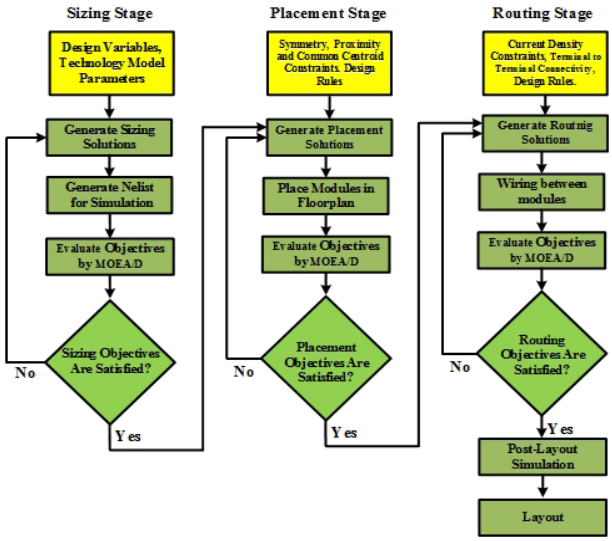


Figure 3: Flowchart of the proposed analog layout generation method.

3.3 Proposesd layout generation method

The flowchart of the proposed analog layout generation method is shown in Figure3. The proposed method details are as follows:

Sizing Stage
Inputs: Design variables such as width, length, and the number of fingers of the MOS transistors, bias voltages, the values of the passive components, and technology models parameters.

Sizing Procedure:
Step 1: Solutions are provided using the optimization algorithm. It this paper, it is performed by the MOEA/D.
Step 2: After providing the solutions by the MOEA/D, a netlist is created. Schematic simulation should be performed to evaluate the circuit specifications. In this paper, simulation is performed using HSPICE software.
Step 3: Specifications of the circuit such as DC-gain, phase margin (PM), power dissipation (P_{diss}), settling time (ST), slew rate (SR) and unity-gain-bandwidth (UGBW), are evaluated from the schematic simulation results.
Step 4: If the specifications are satisfied, the solutions are given to the placement stage. Otherwise, new solutions should be found by the MOEA/D.

Placement Stage
Inputs: Symmetry, proximity and common centroid constraints, design rules, device sizes from the sizing stage.
Placement Procedure:
Step 5: The coordinates of the left-bottom corners of the modules are chosen by the MOEA/D.
Step 6: The modules are placed in the floorplan using the solutions obtained from the previous step.

Step 7: In this step, the placement objectives are evaluated. A compact floorplan should be produced in the placement stage by simultaneous consideration of design rules and the other constraints.
Step 8: If the placement objectives are satisfied, the solutions are given to the routing stage. Otherwise, new solutions should be provided by the EMO.

Routing Stage
Inputs: Current-density constraints, terminal to terminal connectivity, design rules, floorplan from the placement stage.

Routing Procedure:
Step 9: In this step, the obtained floorplan from the placement stage is given to the router. The solutions are generated by the router.
Step 10: Based on the segment positions, wiring between terminals are performed.
Step 11: The routing objectives according to the Section 3.2 are evaluated.
Step 12: If the routing objectives are satisfied, the solutions are given to the next stage. Otherwise, MOEA/D is looking for new solutions.
Step 13: After extracting the parasitics of the obtained layout, post-layout simulation is performed. Parasitics extraction are done using a resistance-capacitance (RC) π model that is suggested in Ref [38]. If post-simulation on routing stage somehow fails, to find new solutions the routing stage should be repeated. It usually takes a few repetitions to get the answer.
Step 14: The final layout of the proposed method is drawn.

4 Performance Evaluation

The proposed analog layout generation method is performed in a 0.18µm 1.8V CMOS technology. An automatic MATLAB toolbox is provided which is connected to HSPICE. MOEA/D is implemented in MATLAB R2016b version and is tested on Intel corei5-4460 CPU @ 3.2 GHz with 16 GB RAM. Operational amplifiers (op-amps) can be considered as an essential block in many mixed-mode systems [39-42].The proposed method is applied to three-stage amplifier and two-stage class-AB operational trans-conductance amplifier (OTA).

4.1 Three-stage amplifier

In Ref [42], optimization of the settling performance of a three-stage amplifier shown in Figure 4 is studied. In the following, designing the three-stage op-amp shown in Figure 4 is presented.

$$f(x) = (f_1(x), f_2(x), f_3(x), f_4(x), f_5(x), f_6(x)) \quad (20)$$

In the above equation , $f_1(x)$=-1xDC-gain, $f_2(x)$=-1xPM, $f_3(x)$=-1xUGBW, $f_4(x)$=-1xSR, $f_5(x)$=-P_{diss}, and $f_6(x)$=ST.x represents the design variables. Designing is performed using minimum channel length transistor (0.18µm), and the widths of the MOS transistors are chosen as 2µm≤ Wj ≤150µm. MOEA/D is executed with a population of 100 individuals with 250 iterations. It should be noted that in each iteration, the z^* in selected as the minimum of the z^* and the cost function. One solution to the sizing result is shown in Table 1. The placement and routing results are done by the layout generator and the result is depicted in Figure 5. The area of the layout is 34µm×32µm. The total number of wires is 23. In this Figure, metal 1 and metal 2 are shown by green and yellow colors, respectively.

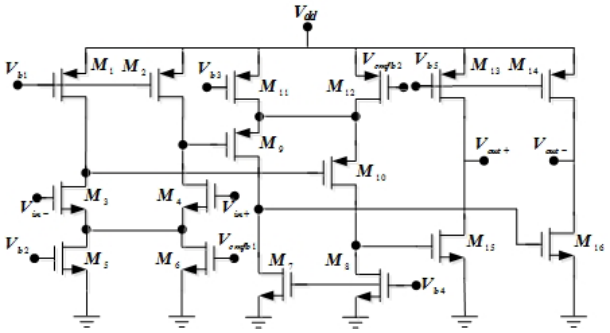


Figure 4: CMOS Three-Stage op-amp [42].

Table 1: Size of transistors for the three-stage op-amps.

Parameter	Value
$(W/L)_{1,2}$	10x10µm/0.18 µm
$(W/L)_{3,4}$	8x6.25µm/0.18 µm
$(W/L)_{5,6}$	10x5µm/0.18 µm
$(W/L)_{7,8}$	16x3.125µm/0.18 µm
$(W/L)_{9,10}$	16x6.25µm/0.18 µm
$(W/L)_{11,12}$	16x12.5µm/0.18 µm
$(W/L)_{13,14}$	10x20µm/0.18 µm
$(W/L)_{15,16}$	10x4µm/0.18 µm

The open-loop frequency responses of the designed op-amp in demonstrated in Figure 6. The results show that the DC-gain is 72 dB after post-layout simulation. UGBW and PM of the Op-Amp are 720 MHz and 82°, respectively. A 0.4 V step voltage is applied to the op-amp and the 1% ST is calculated. The obtained step response is shown in Figure 7. The results shown in the Figures 6 and 7 are also obtained by the Cadence software. It should be mentioned that the proposed method results are consistent with the Cadence software.

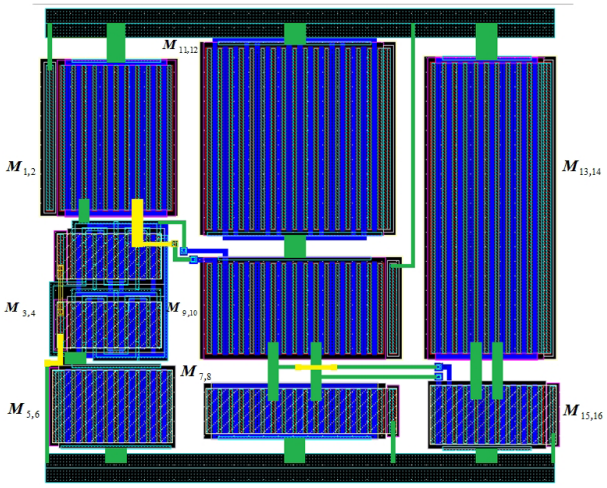


Figure 5: The three-stage amplifier layout generated by the proposed method.

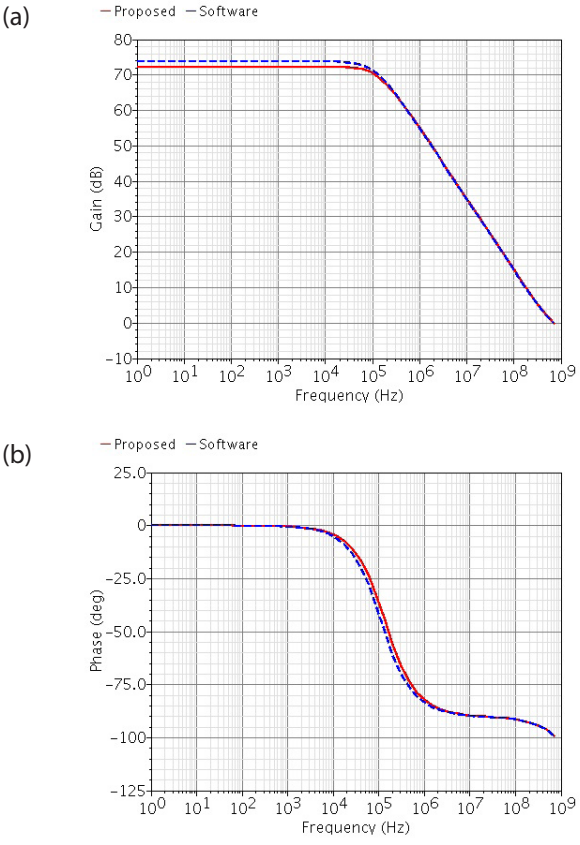


Figure 6: Three-stage op-amp frequency response: **(a)** magnitude, **(b)** phase.

The Pareto optimal fronts (POFs) of the three-stage op-amp including ST versus P_{diss}, DC-Gain versus P_{diss}, SR versus P_{diss} and UGBW versus PM are shown in Figure 8. As can be seen from the Figure 8.a, the proposed method can achieve better ST compared to the existing methods [14], [31]. Table 2 reports the comparisons of post-layout simulation results of the proposed method with the existing methods. The main advantage of the proposed method compared with the existing methods is that the sizing stage is not considered in the existing methods. In addition, a set of solutions are provided by MOEA/D in the proposed method compared to the single solution in the [31]. In the [31], area utilization and number of bends are not included for the placement and routing stages, respectively. It is essential to define initial wires and some operators for the routing stage in the [14]. The ST, layout area and also area utilization of the proposed method is better than the existing methods with the cost of a little increase in the runtime. Therefore, the proposed method is more suitable for automatic analog layout generation.

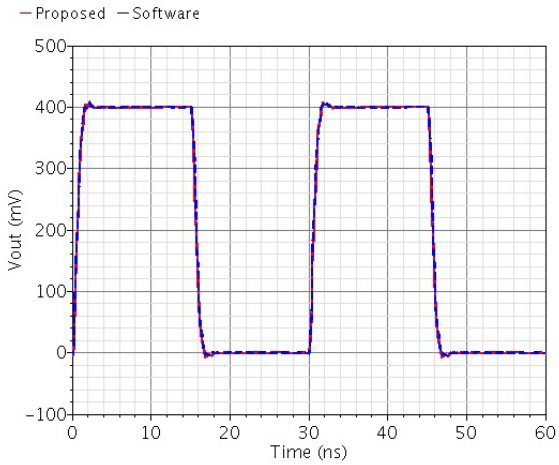


Figure 7: Three-stage op-amp step response.

Table 2: Comparisons of the post-layout simulation results for three-stage amplifier.

No.	Specifications	Post-layout performance		
		This work	[31]	[14]
1	1% Settling time (ns)	<4.4	4.9	5.2
2	Total runtime (s)	1531	1266	1134
3	Layout Area (mm2)	0.0011	0.0013	0.0014
4	Area Utilization (%)	88	82	76

4.2 Two-stage class-AB OTA

In Ref [41], a two-stage class-AB OTA is suggested. By increasing the trans-conductance of the first stage, DC-gain is enhanced. Non-linear current mirror boosts the current of the second stage. As a result, the SR is improved. The OTA is shown in Figure 9. Analytical equations are provided in the Ref. 41. The placement and routing results are obtained from the proposed method and the result is shown in Figure 10. The area of the layout is 130μm×195μm. The POFs of the two-stage class-

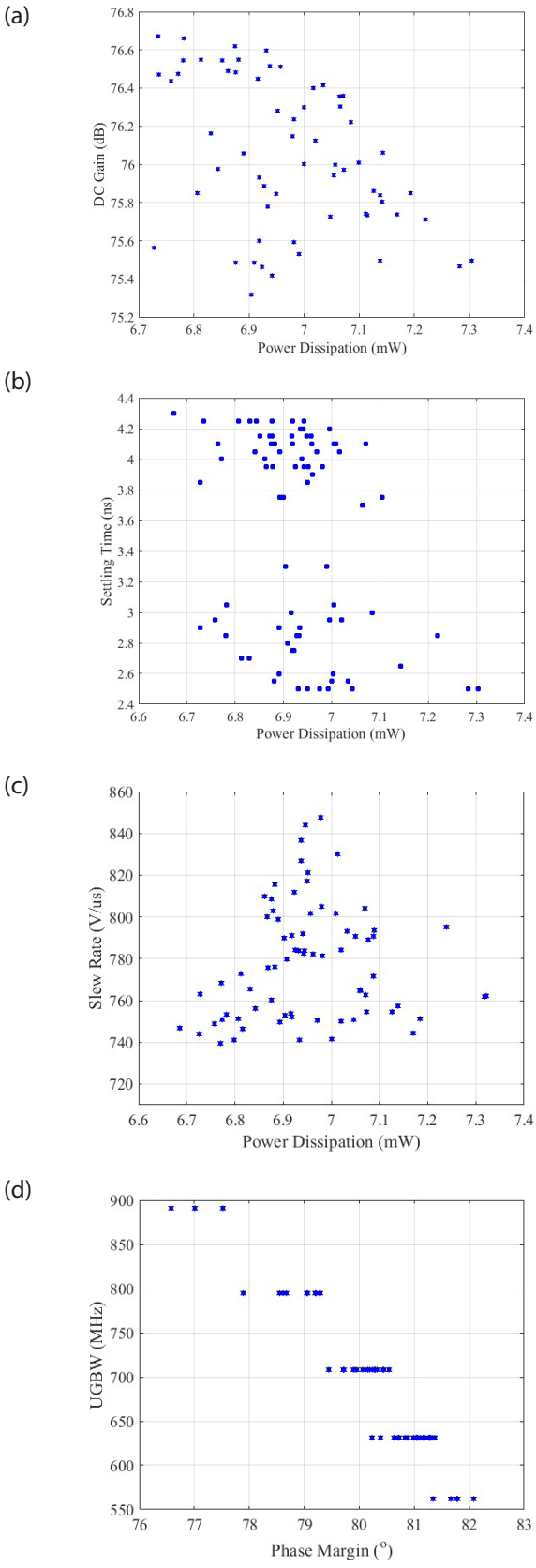


Figure 8: POFs of the three-stage: **(a)** ST versus P_{diss}, **(b)** DC-gain versus P_{diss}, **(c)** SR versus P_{diss}, **(d)** UGBW versus PM.

AB OTA including DC-Gain versus P_{diss}, SR versus P_{diss} and UGBW versus PM are shown in Figure 11. The results show that DC-Gain and UGBW reach 84 dB and 68 MHz, respectively. In addition, according to the PM values, the system is stable. Table 3 indicates the comparisons of post-layout simulation results of the proposed method with the existing methods for the two-stage class-AB OTA. Simulation results indicate that the proposed method outperforms the existing methods in terms of DC-gain, SR, layout area and area utilization.

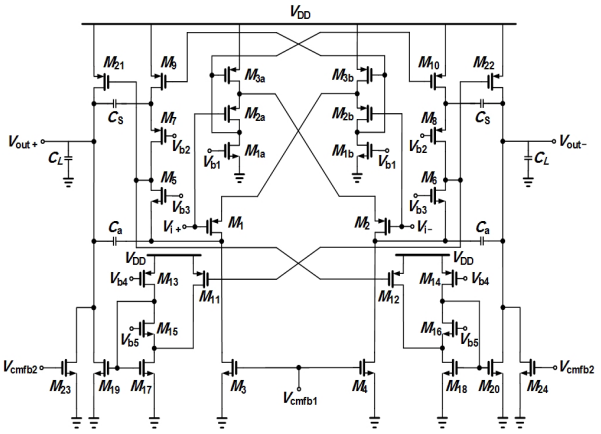


Figure 9: CMOS two-stage class-AB OTA [41].

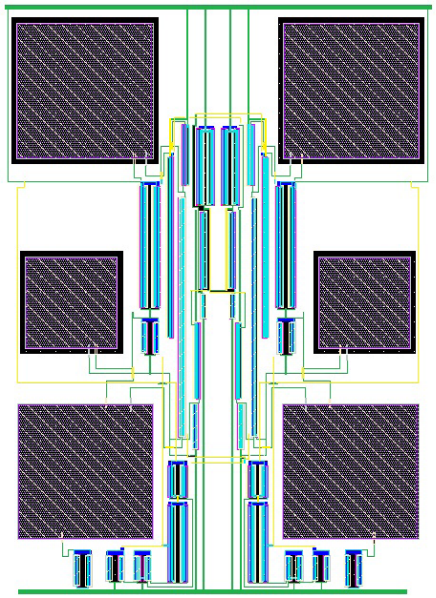


Figure 10: The two-stage class-AB OTA layout generated by the proposed method.

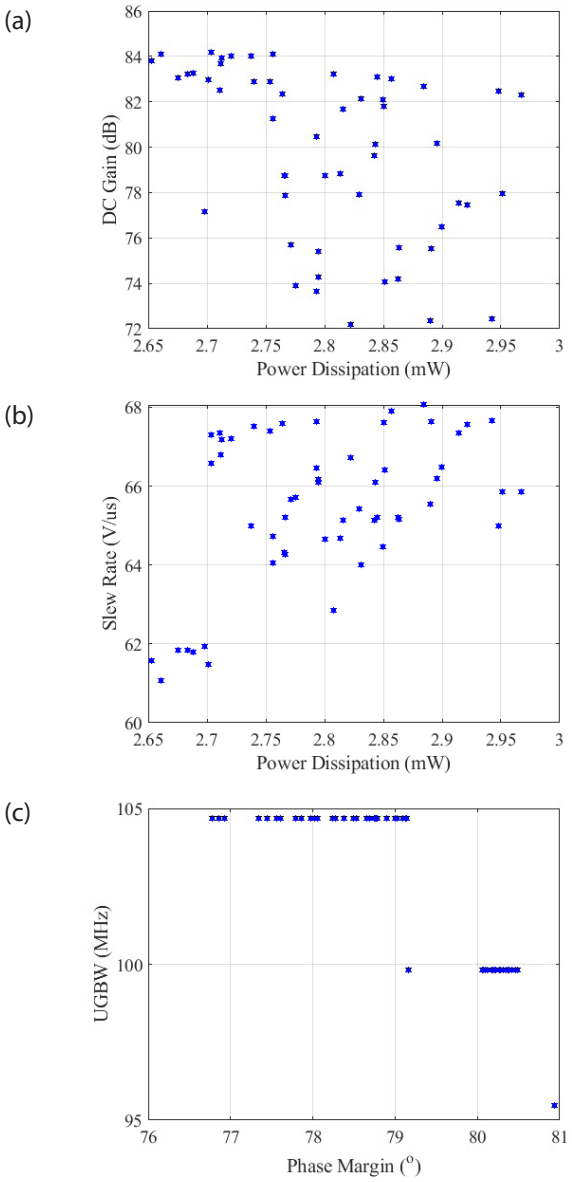


Figure 11: POFs of the two-stage class-AB OTA: (a) DC-gain versus P_{diss}, (b) SR versus P_{diss}, (c) UGBW versus PM.

Table 3: Comparisons of the post-layout simulation results for the two-stage class-AB OTA.

No.	Specifications	Post-layout performance		
		This work	[31]	[14]
1	DC-gain (dB)	84	80	76
2	Slew Rate V/µs	68	65	61
3	Total runtime (s)	2143	1785	1610
4	Layout Area (mm2)	0.025	0.027	0.028
5	Area Utilization (%)	89	84	78

5 Conclusions

A new automatic placement and routing method for layout generation of op-amps has been presented in this paper. In addition, the sizing has been performed automatically. Layout effects including parasitics and geometry effects have been considered. A compact floorplan has been generated in the placement stage by considering a set of constraints. A router has been suggested to generate wires automatically. MOEA/D has been utilized for optimization which is suitable for multi-objective optimization problems. In order to evaluate the performance of the proposed method, some simulations have been carried out and the results indicated the efficiency of the automatic analog layout generation method.

6 Conflicts of Interest

The authors declare no conflict of interest.

7 Acknowledgement

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Analog Circuits Sizing Using Multi-Objective Evolutionary Algorithm Based on Decomposition

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Abstract: Several analog circuit design has been suggested where a layout generator is used after a circuit sizing. But, many iterations between circuit sizing and layout generator stages are needed to obtain desired specifications. This paper proposes a new equation and simulation-based method for circuits sizing of CMOS operational amplifiers (op-amps) by considering layout effects. In the proposed method, layout effects are considered during the sizing step. Layout effects are devices parasitics and geometry information that are extracted from a new automated layout generator. Optimization is performed using multi-objective evolutionary algorithm based on decomposition (MOEA/D). In order to evaluate the performance of the proposed sizing method, the design of folded-cascode and three-stage op-amps are provided in a 0.18µm process CMOS technology with 1.8 V supply voltage. The simulation results exhibit the good performance of the proposed sizing method.

Keywords: Analog circuits sizing; Equation and simulation-based method; Automated layout generator; Multi-objective evolutionary algorithm based on decomposition; Operational amplifiers

Določanje velikosti analognih vezij z uporabo večciljnega algoritma na osnovi dekompozicije

Izvleček: Predlaganih je bilo več načinov načrtovanja analognih vezij, pri katerih se po določitvi velikosti vezja uporabi generator postavitve. Vendar je za pridobitev želenih specifikacij potrebnih veliko iteracij med fazama določanja velikosti vezja in generatorja razporeditve. Ta članek predlaga novo metodo, ki temelji na enačbah in simulaciji, za določanje velikosti vezij operacijskih ojačevalnikov CMOS (op-amperov) z upoštevanjem učinkov postavitve. V predlagani metodi se učinki postavitve upoštevajo v fazi določanja velikosti. Učinki razporeditve so parazitske lastnosti naprav in informacije o geometriji, ki se pridobijo iz novega avtomatiziranega generatorja razporeditve. Optimizacija se izvede z večobjektnim evolucijskim algoritmom, ki temelji na dekompoziciji (MOEA/D). Da bi ocenili učinkovitost predlagane metode za določanje velikosti, so na voljo zasnove zloženih kaskadnih in tristopenjskih operacijskih ojačevalnikov v tehnologiji CMOS z 0,18 µm procesom in napajalno napetostjo 1,8 V. Rezultati simulacije kažejo dobro učinkovitost predlagane metode določanja velikosti.

Ključne besede: Določanje velikosti analognih vezij; metoda na osnovi enačb in simulacij; avtomatiziran generator postavitve; večobjektni evolucijski algoritem na osnovi dokompozicije; operacijski ojačevalniki

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1 Introduction

Designing of analog integrated circuits includes three phases: topology selection, circuit sizing and layout extraction [1-4]. Experience of expert designers can be useful for designing simple circuits containing less number of devices. But, for the complex circuits the search space may be large. Therefore, it may be time consuming and complicated tasks for designers to generate an optimal solution for design variables [5]. Several methods have been proposed for automatic designing of analog integrated circuits using a set of rules depending on the circuits knowledge with respect to desired specifications. But, more effort is required to define new set of rules for different topologies.

Optimization-based methods can be divided into three categories as follows: equation-based [6-7], simulation-based [8-9] and equation and simulation-based methods [10-11]. It should be noted that se-

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vere performance degradation may be occurred after post-layout simulation due to layout parasitics. In the equation-based method, the circuit equations should be solved in order to satisfy the desired specifications. In the simulation-based method, a circuit simulator is utilized and a set of design variables are chosen such that the target specifications are satisfied. Finally, in order to have a trade-off between speed and precision of the two mentioned methods, equation and simulation-based method is employed.

Some works are suggested for dedicated analog blocks [12-15]. But defining the layout template frameworks or custom tools are the main limitation of using these methods. Model-based approach can be applied for automated analog circuit sizing [16-17]. The major advantage of the model-based approach is that the optimization process can be efficiently done by the performance models. In addition, evaluating the models needs much lower computational cost compared to the circuit simulations. This method has the additional advantage of reusing the models. The main drawback of the model-based method is the deviation between the desired circuit performances and the obtained circuit performances.

The gm/ID technique has been proposed in [18]. Its application in the circuit sizing has been shown in [19]. In another method, designer intervention is needed to estimate the gm/ID values [20]. In order to alleviate designer intervention, simulated annealing (SA) is employed to determine length (L) of transistors and gm/ID as variables with repeated reference to the gm/ID curve [21]. In [22], it has been shown that the performance constraints can be satisfied. However, severe performance degradation may be occurred after post-layout simulation due to layout parasitics. Therefore, a large number of iterations are needed between the circuit sizing and the layout generation.

Several Computer-Aided Design (CAD) tools have been proposed for the analog circuits [23-25]. It should be noted that the circuit performance may be influenced by layout parasitics. Therefore, deviation between the desired specifications of the circuit and the post-layout simulation results can be observed. Analog integrated circuits are sensitive to the layout parasitics. As a result, many iterations between the circuit sizing and layout synthesis are essential in order to obtain the desired target specifications [26]. If the mentioned issues are not considered, circuit overdesign may occur with the cost of increasing circuit power and area. On the other hand, circuit underestimation may deteriorate the post-layout simulation results. Therefore, it is required to incorporate layout information during sizing to alleviate the designing complexity and also the time-to-market.

In order to overcome the mentioned problems, sizing step should be performed by considering the layout effects. The sizing method to consider the layout effects includes parasitic-aware sizing and geometry-aware sizing [27-28]. In the parasitic-aware sizing method, layout parasitics are extracted continuously and then they are employed in the sizing process. In the geometry-aware sizing method, the geometrical parameters value such as width and length of MOS transistors are chosen to optimize the layout area. Several analog layout-aware sizing methods have been introduced in the literature. A CAD tools supporting layout aware circuit sizing is introduced in [29]. But, some of the layout parasitics are not considered. In another method, the sizing is performed by a knowledge-based tool using the equations [30]. This method is based on trial and error in which inside each loop the layout tool should be called several times in order to estimate the parasitics. The method introduced in [31] uses a genetic algorithm for circuit sizing. In this method, a cost function is defined based on a set of formula for circuit sizing. But the obtained results might be different from the real simulation results. In [32], multiple floorplan templates are employed in order to optimize the area of the placement. However, the layout parasitics are not regarded explicitly. Another parasitic-aware sizing method is introduced in [33]. This method can only be used for a pre-defined floorplan. An analog layout generation using modified cuckoo optimization algorithm (MCOA) is suggested in [34]. Layout parasitics are extracted to avoid the circuit performance deterioration. But, the layout information is not included in the sizing loop. A two-stage equation and simulation-based method for optimization of CMOS op-amps parameters is suggested in [10]. However, layout effects are not taken into account.

In this paper, an automatic equation and simulation-based methods for circuit sizing by considering layout effects is proposed. In this method, multi-objective evolutionary algorithm based on decomposition (MOEA/D) is used as optimizer. Circuit performance and layout effects are considered in the proposed method. In this paper, an automated method is adopted for placement and routing in analog layout generation using MOEA/D. In addition, both parasitics and geometrical information of the layout are regarded in the proposed method. The rest of the paper is organized as follows: The MOEA/D is described in Section 2. The proposed automatic sizing method is introduced in Section 3. Simulation results are given in Section 4. Finally, conclusion is provided in Section 5.

2 Multi-objective evolutionary algorithm based on decomposition (MOEA/D)

Recently evolutionary multi-objective optimization (EMO) algorithms have been widely utilized in many application fields [35-36]. EMO algorithms can be designed to search for a non-dominated solution set. Therefore, the entire Pareto front of a multi-objective optimization problem (MOP) can be approximated. In this paper, the MOP is introduced as follows:

$$\begin{aligned} &\text{Minimize}\,(f_1(x), f_2(x), \ldots, f_M(x)) \\ &\text{Subject to}\, g(x) \geq 0, X_L < x < X_H \end{aligned} \tag{1}$$

Where $f_i(x)$, $i = 1...M$ is the objective function, M indicates the number of objectives, x includes design variables, and X_L and X_H are their lower and upper bounds, respectively. The design constraints is shown by the vector $g(x)\geq 0$.

Multi-objective evolutionary algorithm based on decomposition (MOEA/D) has been introduced for MOP [37]. In the MOEA/D, a MOP is decomposed into several scalar sub problems so that the optimization is done simultaneously. It has been shown that using the information obtained from the solutions of neighborhood subproblems, the MOEA/D has less computational cost. This characteristic has been proved using many numerical tests.

In the MOEA/D, a scalar function is used to decompose a multi-objective optimization problem into a number of scalar optimization sub-problems. In this method, optimization is performed simultaneously by the evolutionary algorithm. In the MOEA/D, each non-dominated solution of the MOP is associated with an optimal solution of the single objective optimization problem and it can be calculated by a specific weight vector. A set of weight vectors is employed by the MOEA/D to provide different search directions. The different weight vectors can direct to search the different regions of the objective space. The decomposition a multi-objective optimization problem into N sub-problems is possible by Tchebycheff method. In this method, objective function of the j-th (j=1,2,...N) sub-problem is as follows:

$$g^{te}(x \mid \lambda^j, z^*) = \max_{1\leq i\leq m} \left\{ \lambda_i{}^j \mid f_i(x) - z_i^* \mid \right\} \tag{2}$$

Where $\lambda^j = \left(\lambda_1{}^j, \ldots, \lambda_m{}^j\right)^T$ demonstrates a weight vector, $z^* = (z_1^*, \ldots, z_m^*)^T$ represents a reference point. For each Pareto optimal point x^* there can be found a weight vector so that x^* is the optimal solution of (2). It should be mentioned that each optimal solution of (2) is a Pareto optimal solution of problem (1).

3 Proposed sizing method

First, the proposed placement and routing stages for the layout generation are explained. Then, the proposed circuits sizing by considering the layout effects is presented.

3.1 Placement

In the placement stage, the area of floorplan is optimized by simultaneous consideration of the constraints such as symmetry and proximity. It is necessary to place the devices by considering symmetry and proximity constraints in order to alleviate the parasitic coupling effects and also to improve circuit performance. The implementation details of these constraints can be found in [38]. It is worth to mention that the design rules must be satisfied in this stage. The devices to be placed on the floorplan are represented by k blocks M_1 …, M_k The objective function is defined for the placement stage as follows:

$$f_P = f_{oP1}(x) \tag{3}$$

$$f_{oP1}(x) = Width_{floorplan} \times Height_{floorplan} \tag{4}$$

In the above equation, $x = \{(x_1, y_1), \ldots, (x_k, y_k)\}$ indicates the coordinates of the left-bottom corners of the modules, $f_{oP1}(x)$ is the area of the floorplan. $Width_{floorplan}$ and $Height_{floorplan}$ represent the floorplan width and height, respectively. In the placement stage, optimization is performed using the MOEA/D.

3.2 Routing

In the routing stage, the terminals of the layout devices are electrically connected. In this proposed method, each wire is divided into d segments. Each segment is indicated by segment direction, segment layer and

Segment Direction	Segment Layer
Up Down Left Right	Layer 1 Layer 2 ⋮ Layer m

Figure 1: Wire Representation

segment length as shown in Figure 1. Segment direction is defined as up, down, left and right. Segment are located in the layers from 1 to m, where m is the number of the layers.

Positions of the segments are adjusted automatically so that the wire length between terminal pairs to be minimized. The objective functions for routing stage are proposed as follows:

$$f_R = (f_{oR1}(x), f_{oR2}(x), f_{oR3}(x)) \quad (5)$$

$$f_{oR1}(x) = \sum_{i=1}^{d} Length_{Segment_i} \quad (6)$$

$$f_{oR2}(x) = \sqrt{(x_{T_E} - x_n)^2 + (y_{T_E} - y_n)^2 + (z_{T_E} - z_n)^2} \quad (7)$$

Where $f_{oR1}(x)$ is the sum of the segment lengths from the starting terminal (T_S) to the last point on the wire (n). $(x_{T_S}, y_{T_S}, z_{T_S})$ and (x_n, y_n, z_n) are the coordinates of the starting terminal and the point n, respectively. $f_{oR2}(x)$ shows the euclidean distance from the point *n* to the target terminal (T_E) with coordinates $(x_{T_E}, y_{T_E}, z_{T_E})$ (See Figure 2). Objectives $f_{oR1}(x)$ and $f_{oR2}(x)$ are defined based on A^* algorithm [39]. Objectives $f_{oR3}(x)$ is the number of vias in the wire. Current-density to determine the segment width and design rules are the constraints in the routing stage.

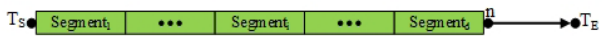

Figure 2: The wire segmentation

3.3 Parasitics Extraction

Interconnect parasitics that are considered here are wire resistance, wire substrate capacitance and wire coupling capacitance. Mathematical representations for resistance and capacitance for a tile on a layer in terms of their length and width are as below [40].

$$R = \rho_{sh} \times (\text{Length}/\ \text{Width}) \quad (8)$$

$$C_{sub} = C_a \times (\text{Length} \times \text{Width}) + C_{sw} \times (2 \times \text{Length}) \quad (9)$$

$$C_{coup} = C_c \times (\text{Length}/\ \text{distance}) \quad (10)$$

Where ρ_{sh} is sheet resistance per unit length, C_a indicates substrate capacitance per unit area, C_{sw} demonstrates capacitance per unit length, C_c shows coupling capacitance per unit length, and distance is defined as the space between two tiles. A resistance-capacitance (RC) π model is utilized to show net resistance and capacitance.

3.4 Circuit Sizing

The flowchart of the proposed circuits sizing by considering layout effects is shown in Figure 3. The proposed method details are as follows:

Step 1: Firstly, design variables such as width, length and the number of fingers of the MOS transistors and the passive components values, bias voltages and currents are selected.

Step 2: Target specifications of the operational amplifiers (op-amps) are defined using equations. Specifications of the circuit such as DC-gain, phase margin (PM), power dissipation (P_{diss}), settling time (ST), slew rate (SR) and unity-gain-bandwidth (UGBW) are evaluated. The optimization of the solutions is performed by MOEA/D.

Step 3: If the desired specifications are not satisfied, new solutions are searched by MOEA/D. In order to provide new solutions, design variables values that are mentioned in the step 1 are changed during optimization process. Otherwise, the solutions are given to the next stage.

Step 4: The netlist of the circuit is generated that is essential for HSPICE simulation.

Step 5: In order to evaluate the target specifications, schematic simulation is performed by HSPICE software.

Step 6: If the desired specifications are satisfied, the solutions are given to the placement step. Otherwise, new solutions are searched by MOEA/D. Solutions are defined similar to the step 3.

Step 7: A compact floorplan is generated in the placement stage by simultaneous consideration of symmetry and proximity constraints and also design rules.

Step 8: After placement stage, the routing is performed. The router generates wires between terminals as well as satisfying the constraints.

Step 9: The parasitics of the layout are extracted in order to perform post-layout simulation.

Step 10: If the circuit post-layout performance satisfies the desired specifications, the algorithm stops. Otherwise, MOEA/D is looking for new solutions.

4 Performance Evaluation

The proposed analog circuit sizing method is performed in a 0.18µm 1.8V CMOS technology. A new MATLAB toolbox is provided which is connected to HSPICE software. It can generate a netlist for HSPICE and also

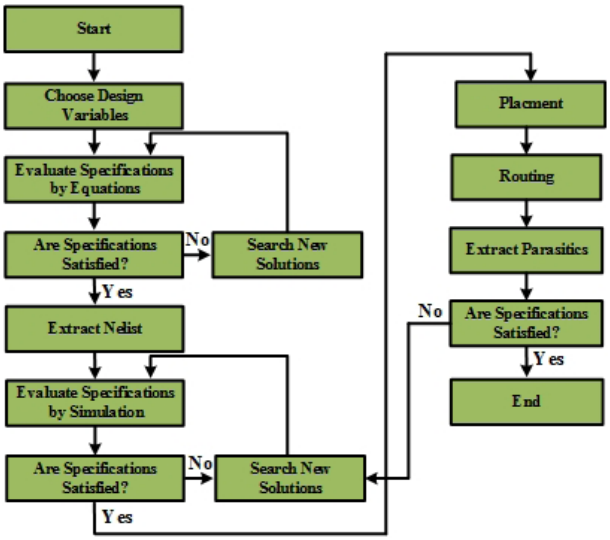

Figure 3: Flowchart of the proposed sizing method

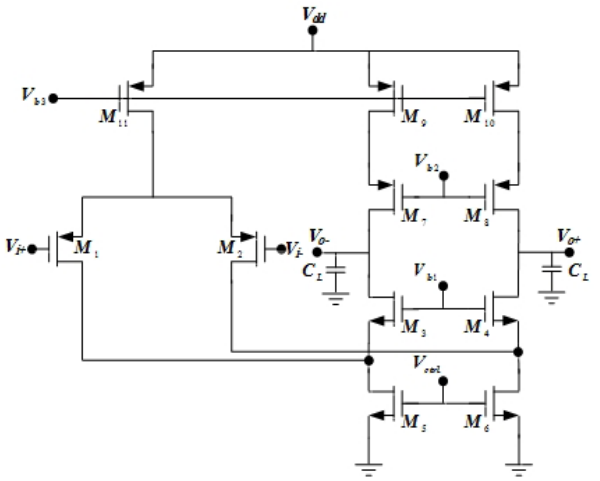

Figure 4: Schematic of the folded-cascode op-amp [5]

run it automatically in order to evaluate the target specifications. MOEA/D is implemented in MATLAB R2016b version and are here tested on Intel(R) core™ i5-4460 CPU @ 3.2 GHz with 16 GB RAM. The op-amps are an essential block in many mixed-mode systems [41-43]. In following, the design of folded-cascode and three-stage op-amps are presented.

4.1 Folded-cascode op-amp

The schematic of the folded-cascode op-amp with a p-channel input pair is shown in Figure 4 [5]. The design variables are the transistor sizes (width and length), the passive components values and the bias voltages values. The target specifications of the circuit are DC-Gain, UGBW, SR, P_{diss} and PM.

This circuit is designed by the proposed circuit sizing method. Designing is performed using minimum channel length transistor (0.18µm), width of the MOS transistors are chosen as 2µm≤ Wj ≤190µm, and bias voltage range is defined as $0.3V \leq V_{bi} \leq 1.5V$. Desired target specifications of the folded-cascode op-amp including DC-Gain, UGBW, SR, PM and Pdiss are shown in Table 1. MOEA/D is executed with a population of 100 individuals with 100 iterations. An example of placement stage progress using the proposed automated layout generator is shown in Figure 5. The Figures 5.a and 5.b show that the results are not compacted and symmetry and proximity constraints are not satisfied. The final result is depicted in the Figure 5.c in which the layout area is optimized and constraints for symmetry, proximity and design rules are satisfied.

The obtained result from the placement stage (Figure 5.c) is utilized for the routing stage. An example of wiring progress using the proposed automated layout generator is demonstrated in Figure 6. The results show that the objective functions defined by the equations (5)-(7) are optimized so that the shortest wire between two terminals is generated. The final result is shown in the Figure 6.c. The final layout after the routing is made by the proposed layout generator and the result is depicted in the Figure 7. The area of the layout is 27µm×43µm. The total number of wires is 26. In the Figure 7, metal 1 and poly are shown by cyan and blue colors, respectively. Design rules are also satisfied in the routing stage. It is worth to mention that in the routing stage the wires length are determined by current-density constraints.

The size of transistors for the folded-cascode op-amp layout shown in the Figure 7 are reported in Table 2. The pareto optimal fronts (POFs) of the folded-cascode op-amp including DC-Gain versus SR, DC-Gain versus UGBW, P_{diss} versus SR and PM versus UGBW are shown in Figure 8. As can be seen from the POFs, the proposed method can satisfy the target specifications well. The comparison results of the proposed method and the existing methods are reported in the Table 3. Two main advantages of the proposed method compared with the methods introduced in [10-11, 34] can be described as follows: 1) Circuit sizing and layout generation steps are not considered simultaneously in the existing methods. Therefore, circuit performances such as PM and UGBW may be degraded due to layout parasitics after post-layout simulation. It should be noted that in [10-11], the floorplan area is estimated approximately. 2) A set of solutions are provided by MOEA/D in the proposed method compared to the single solution in the existing methods [10, 34]. Therefore, the proper circuit can be selected for the specific application in the proposed method. Figure 9 show the POFs of the folded-cascode op-amp when only the simulation stage in

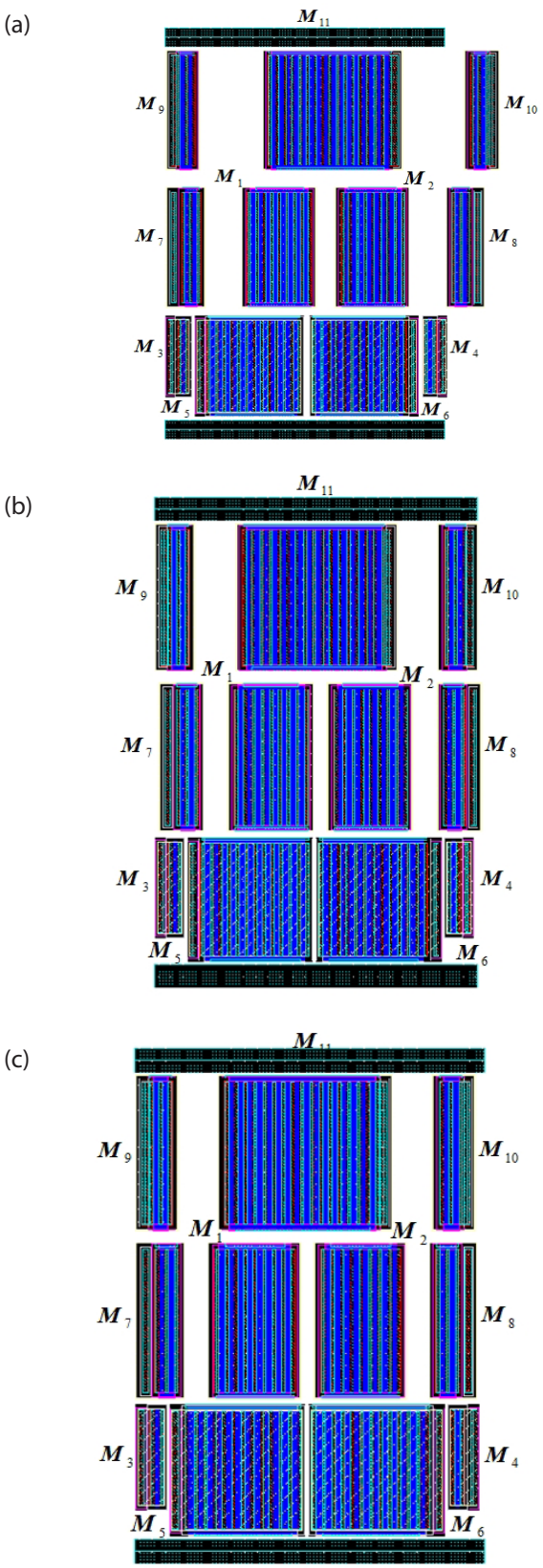

Figure 5: Example of placement stage progress using the proposed automated layout generator: (**a**) floorplan after 1 generation, (**b**) floorplan after 10 generations, (**c**) floorplan after 100 generations.

the Figure 3 is used. As can be seen from the results, the Figure 9.b is less widespread compared to the Figure 8.b. It shows the better performance of the proposed equation and simulation-based method compared to the simulation-based method.

Table 1: Desired target specifications of the folded-cascode op-amp

No.	Target Specifications	Value
1	DC-Gain	>50 dB
2	UGBW	>350 MHz
3	SR	>400 V/µs
4	PM	55°<PM<65°
5	Pdiss	Minimized

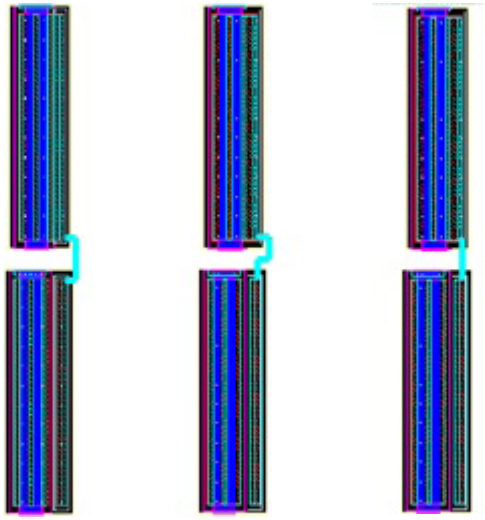

Figure 6: Example of routing stage progress using the proposed automated layout generator: (**a**) Wiring between two terminals after 1 generation, (**b**) Wiring between two terminals after 10 generations, (**c**) Wiring between two terminals after 100 generations.

Table 2: Size of transistors for the folded-cascode op-amp.

Parameter	Value
$(W/L)_{1,2}$	8x11.7µm/0.18 µm
$(W/L)_{3,4}$	1x7.8µm/0.18 µm
$(W/L)_{5,6}$	12x9.7µm/0.18 µm
$(W/L)_{7,8,9,10}$	2x111.7µm/0.18 µm
$(W/L)_{11}$	16x11.7µm/0.18 µm

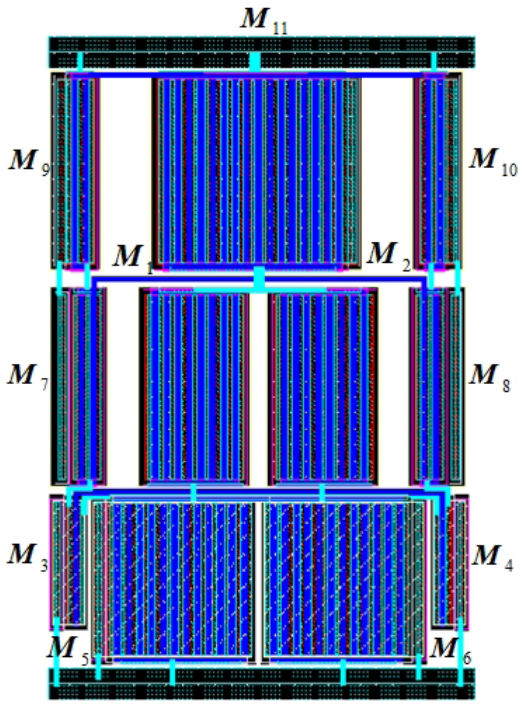

Figure 7: The layout generated by proposed method.

Table 3: The comparison results of the proposed method and the existing methods.

Specifications	This work	[10]	[11]
DC_Gain (dB)	53.9	53.9	53.4
Phase_Margin (°)	62.7	62.9	64.5
UGBW (MHz)	398	398	285
Power_Dissipation (mW)	1.1	1.1	0.79
Slew_Rate (V/µs)	534	470	320
Layout Area (µm^2)	1161	-	-
Total run time (s)	1880	1087	1023

4.2 Three-stage op-amp

In [43], optimization of the settling performance of a three-stage amplifier shown in Figure 10 is studied. This circuit is designed by the proposed method. One solution to the sizing result is shown in Table 4. The placement and routing results are done by the layout generator and the result is depicted in Figure 11. The area of the layout is 33µm×36µm. The total number of wires is 23. In this figure, metal 1 and metal 2 are shown by green and yellow colors, respectively. The POFs of the three-stage op-amp including ST versus P_{diss}, DC-Gain versus P_{diss}, SR versus P_{diss} and UGBW versus PM are shown in Figure 12. Table 5 reports the comparisons of post-layout simulation results of the proposed method with the existing methods. As can be seen from the results, the proposed method can achieve better ST compared to the existing methods [10, 11]. Since circuit sizing and layout generation steps are not considered simultaneously in the existing methods, the ST values are degraded after post-layout simulation

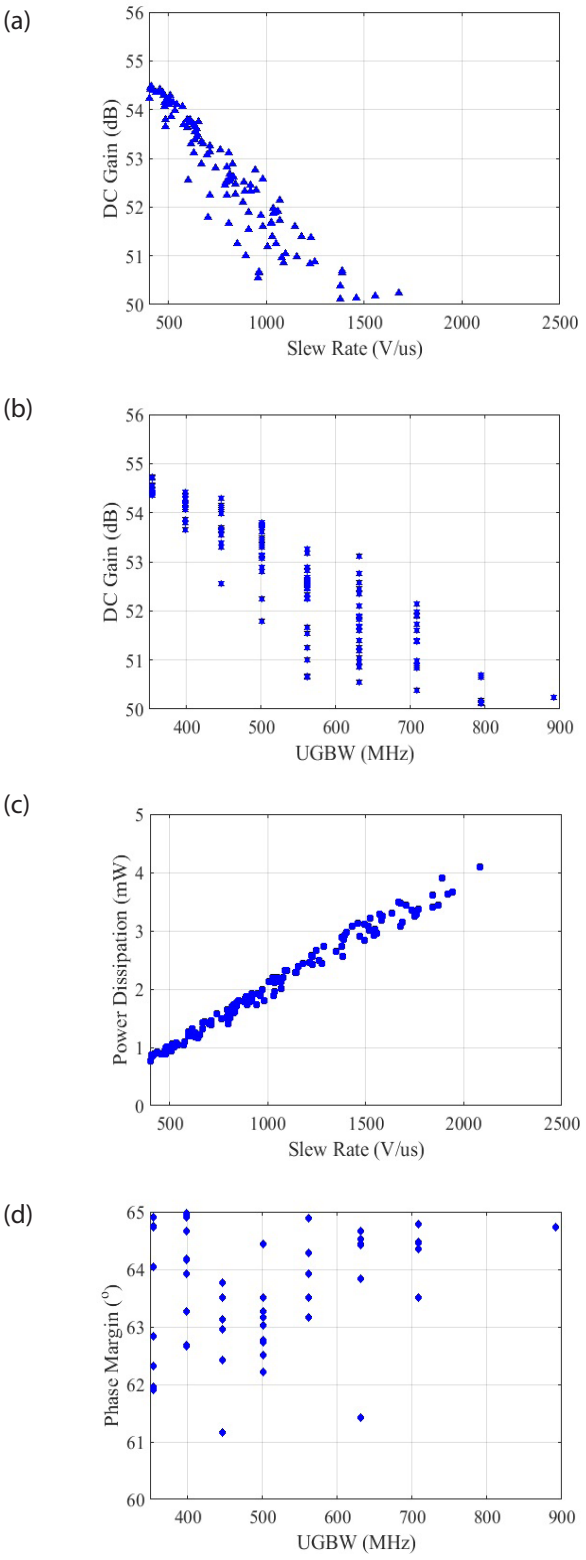

Figure 8: POFs of the folded-cascode op-amp using the proposed method: **a**) DC-gain versus SR, **b**) DC-gain versus UGBW, **c**) Pdiss versus SR, **d**) PM versus UGBW.

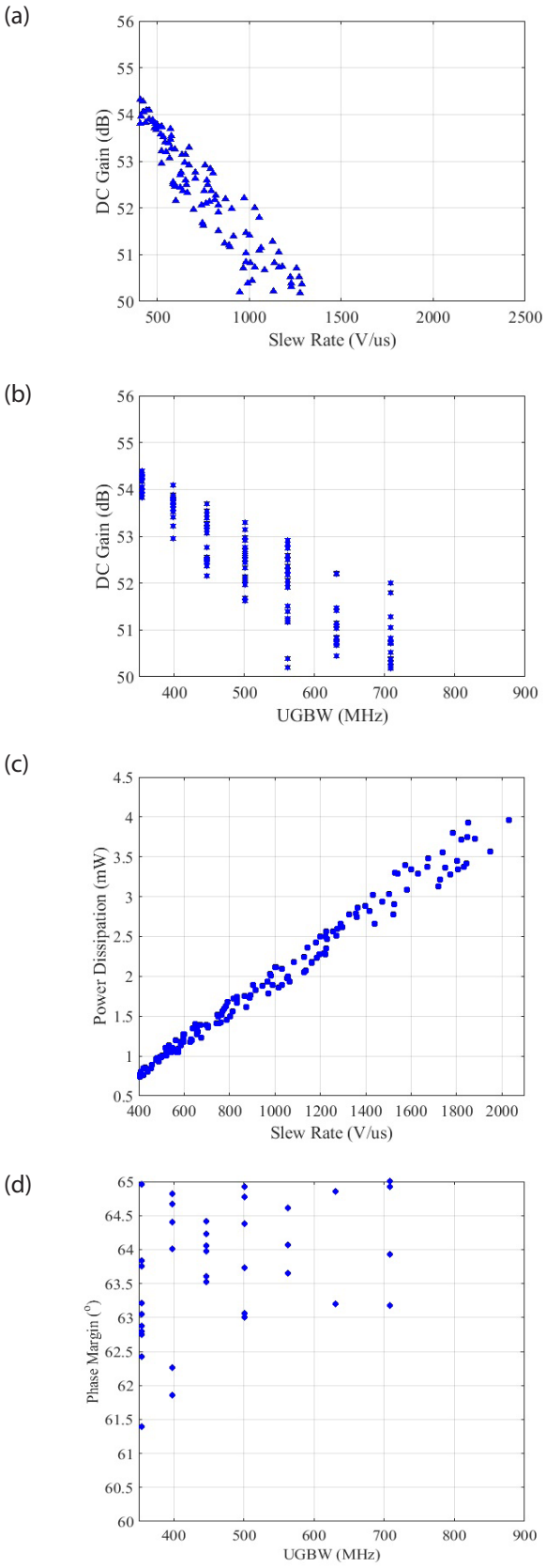

Figure 9: POFs of the folded-cascode op-amp obtained from only the simulation stage: **a**) DC-gain versus SR, **b**) DC-gain versus UGBW, **c**) P_{diss} versus SR, **d**) PM versus UGBW.

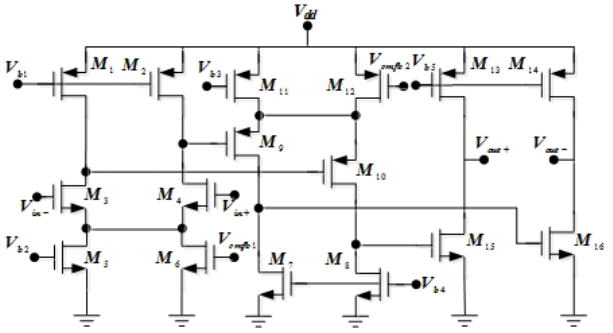

Figure 10: CMOS Three-Stage op-amp [43].

Table 4: Size of transistors for three-stage op-amp.

Parameter	Value
$(W/L)_{1,2,9,10}$	5x10µm/0.18 µm
$(W/L)_{3,4,5,6,7,8}$	5x5µm/0.18 µm
$(W/L)_{11,12}$	5x20µm/0.18 µm
$(W/L)_{13,14}$	5x20µm/0.18 µm
$(W/L)_{15,16}$	5x4µm/0.18 µm

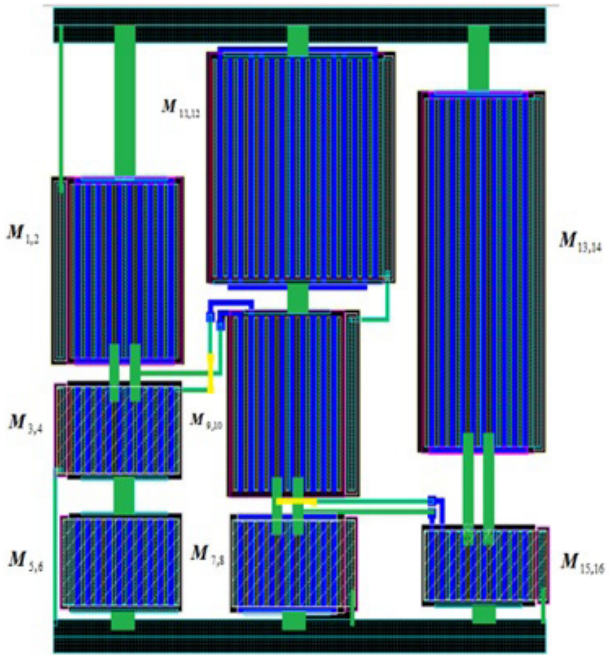

Figure 11: The layout generated by the proposed method.

Table 5: Comparisons of the post-layout simulation results for the three-stage op-amp.

Specifications	This work	[10]	[11]
1% Settling time (ns)	<4.4	4.9	5.2
Total runtime (s)	1531	1266	1134
Layout Area (mm^2)	0.0012	-	-

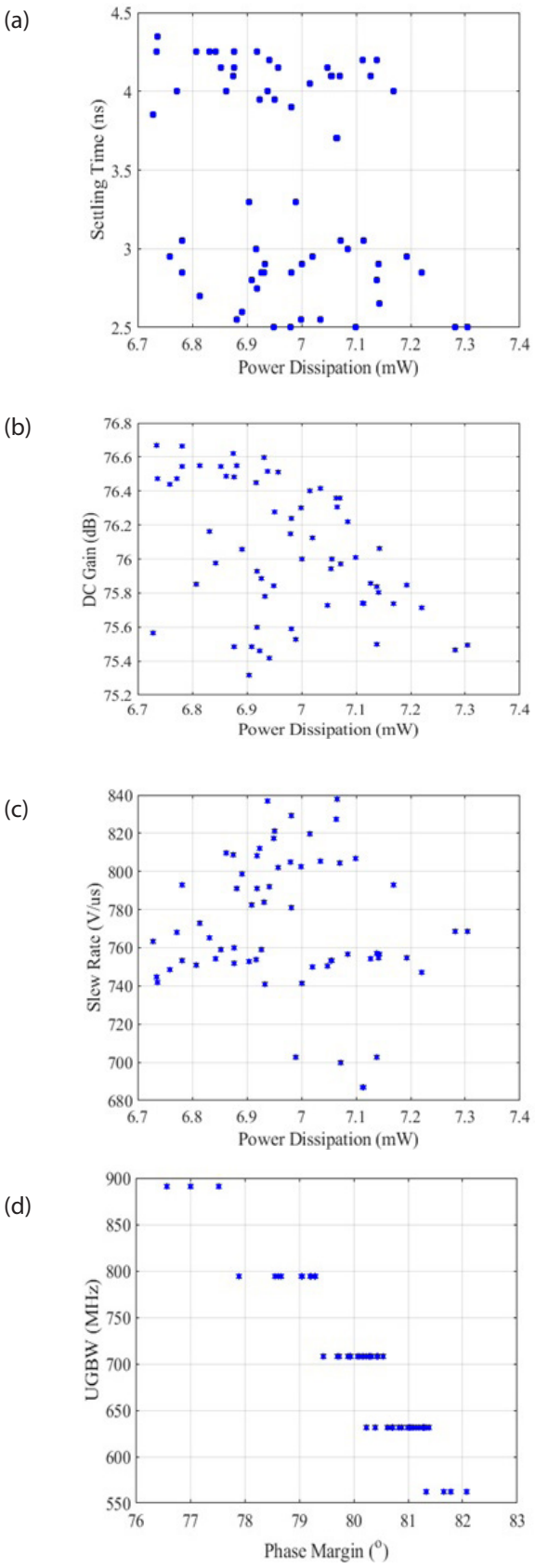

Figure 12: POFs of the three-stage: (a) ST versus P_{diss}, (b) DC-gain versus P_{diss}, (c) SR versus P_{diss}, (d) UGBW versus PM.

5 Conclusions

In this paper a new circuit sizing method has been proposed. During sizing process, layout effects including parasitics and geometry effects have been considered. A new placement method has been suggested in which compact floorplan has been generated by considering a set of constraints. A routing process has been presented to generate wires between terminals automatically. Design rules have been satisfied in the both of placement and routing stages by the proposed layout generator. The MOEA/D has been used for optimization which is suitable for multi-objective optimization problems. In order to evaluate the performance of the proposed circuit sizing method, designing of the folded-cascode and three-stage op-amps have been performed. The results indicated that the proposed circuit sizing method is quite promising.

6 Conflicts of Interest

The authors declare no conflict of interest.

7 Acknowledgement

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