A REVIEW ON THERMAL CYCLING AND DROP IMPACT RELIABILITY OF SOLDER JOINTS IN ELECTRONIC PACKAGES

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Key words: Soldering, thermal cycling, drop impact, failure mode, material requirement

Abstract: Currently, the trend of miniaturization, light weight, high speed and multifunction are common in electronic assemblies, especially, for the mobile electronics. One of the most critical aspects of the package reliability is solder joint reliability. So, in that field, thermal cycling and drop/impact are the primary requirement for solder joint reliability. This paper discusses the reliability of solder joint in term of both temperature cycles load and drop/impact load from view points of failure mode and relevant material properties. High compliance and high grain-coarsening resistance are identified as key material properties for high thermal cycling and drop impact reliability respectively. The paper details the requirements solder joints have to meet to be qualified for the mobile electronics applications. Therefore, this contribution has its value in giving information on suitable material electronic devices under different loading condition.

Vpliv termičnih in fizičnih obremenitev na zanesljivost spajkanih spojev v elektronskih vezjih

Kjučne besede: spajkanje, termične in fizične obremenitve, načini odpovedi, lastnosti materiala

Izvleček: Miniaturizacija, zmanjševanje teže, velika hitrost in večopravilnost so trenutni trend lastnosti elektronskih vezij, še posebej namenjenih mobilnim napravam. Eden najbolj kritičnih vidikov zanesljivosti elektronskega modula je zanesljivost spajkanega spoja. Le-ta mora biti odporen na termične in fizične obremenitve. V prispevku obravnavamo zanesljivost spajkanega spoja ter vpliv materialnih lastnosti na vzroke odpovedi po termičnih in udarnih obremenitvah. Naštejemo vse zahteve, ki jih zanesljiv spoj mora zadovoljevati, da zadosti kvalitetnim kriterijem za uporabo v elektronskih modulih namenjenih mobilnim napravam.

1. Introduction

An electronic package integrates metal conductors, organic/ceramic dielectrics and semiconductors into a functional device. This variety of materials results in a complex system to build and, increasingly, retain high levels of reliability. Reliability is influenced by the operation of the device (e.g., power dissipated, current carried, etc.) and the environment (e.g., ambient temperature, temperature changes and imposed mechanical strains) (Frear et al., 2008). Traditionally, only temperature and power cycling were of concern for board level reliability, and coefficient of thermal expansion mismatch between the package and the board was considered as the primary failure mechanism. However, due to the proliferation of electronic devices across market segments, ranging from automotive to small, hand-held devices; electronic packages experience mechanical loading conditions other than just temperature cycling (Syed et al.). This additional failure mechanism has their implications on package material selection to design a robust package meeting reliability requirements for a particular end use application.

Thermal cycling and mechanical shock are two of major loads that lead to the failure of board-level solder joints for portable electronic product. Board-level package is a multi-material system. These various materials cause the mismatch of Coefficient of Thermal Expansion (CTE). The CTE mismatch between PCB (composed of FR4 material and polymer) and package (composed of substrate, die and mold cap) results in the thermo-mechanical fatigue damage of solder joints when the board-level package is subjected to thermal cycling load. The fatigue crack initiates and propagates through the bulk solder (Zhang et al., 2009). The increasing occurrence of drop-impact failure of portable electronics has been traced to the failure of the solder joints that interconnect the integrated circuit (IC) components to the printed circuit board (PCB). The drop-impact of portable electronics leads to bending of the PCB assembly within the portable electronic device; the interconnecting solder joints undergo severe deformation to accommodate the differential bending deformation between the IC component and the PCB (Wong et al., 2009). The strain rate of solder joint under mechanical shock load (e.g. drop impact) is much higher than that under thermal cycling load. The strength properties of the bulk solder will increase with the increasing of strain rate (Wong et al., 2008b, Zhu et al., 2007). The solder joints have less plastic deformation due to the higher strain rate under drop load compared with that under thermal cycling load, so the stress at the inter-metallic compound (IMC) layers increases and exceeds the fracture strength of IMC. The crack initiates and propagates along the IMC layer (Mattila and Kivilahti, 2005). The failure mode, and therefore the reliability of interconnection, relies on the properties of solder matrix. This paper will discuss the thermal cycling and drop impact reliability of solder joints in electronic packaging from the view points of material properties, failure mechanism and crack propagation.

2. Drop impact reliability

For portable electronic applications, one of the greatest challenges for the package assembly is to survive a challenging use environment that includes being dropped, result at the end in electrical failure (Frear et al., 2008). "Drop-impact" refers to free fall under gravity followed by an impact on a target such as the ground. Upon impact, a fraction of the kinetic energy of portable electronic product will be converted to sound and frictional heat energy, a portion to elastic and plastic strain energy in the product housing, and the rest to elastic and plastic strain energy of the interior components including printed circuit board (PCB), integrated circuit (IC) components and interconnects (mainly solder joints) (Wong et al., 2008a). The literature on drop impact loading of electronic packages and assemblies is starting to grow (Alajoki et al., 2005, K. Mishiro, 2002, Mattila, 2005, Tee et al., 2003). The weak link in the package is the board level solder joint between the package and the printed circuit board.

The failure mode during drop impact loading is manifested in interfacial cracking along the solder joint (either on the package or board side (Suh et al., 2007, Syed et al., 2006) as shown in Figure 1 (M.P. Renavikar, 2008). In either case, shock failure is characterized by a lack of solder deformation and an absence of solder bulk cracking. This is due to the strain-rate sensitivity of metallic materials. Metallic materials including solders typically become stronger with increasing strain rates. Thus, the robustness of a solder joint is influenced by a complex combination of bulk solder and inter-metallic properties (Grafe et al.). Ductile failures through bulk solder typically progress slowly, but crack through brittle inter-metallic progress much faster (Frear et al., 2008). The outstanding question is whether "bulk" properties of solder can be optimized to suppress or delay this essentially interfacial" crack propagation along the solder joints. The so-called extrinsic toughening concept can be invoked to answer the question (Suh et al., 2007). The extrinsic toughening refers to a toughening mechanism by reducing effective crack driving force that the crack tip actually experiences through various energy dissipation processes without increasing inherent fracture resistance of the material or interface (Ritchie, 1988). High compliance (i.e., low elastic modulus) and high plastic energy dissipation (i.e., low yield strength) ability are identified as key material properties to be optimized for extrinsic toughening mechanism (Suh et al., 2007). Hence, solder alloy with low compliance and high plastic energy can help increase the drop performance because softer solder joint can help to absorb more dynamic energy to reduce the dynamic stress transformed from PCB to IMC/solder interface layer (Che et al.). There is a high variation in the life of similar solder joints since the cracks can change from ductile to intermetallic due to random variation in the microstructure of individual joints.

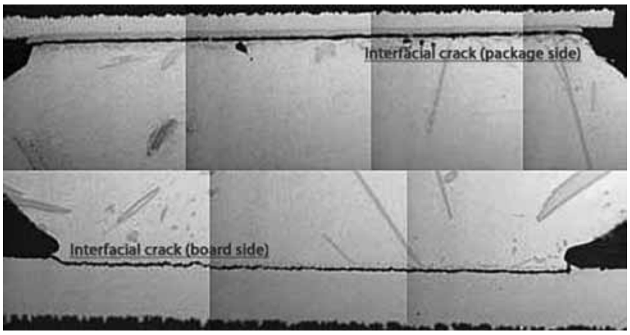


Fig. 1: SAC405 solders joint failure in shock conditions (M.P. Renavikar, 2008)

However, the strain rate experienced by solders joint or the boards during drop/shock testing is estimated to be10^2/sec., which belongs to dynamic-to-impact loading condition. Under these conditions the behavior of the metallic material is denominated by elasticity (Suh et al., 2007). In other words, plasticity is suppressed under these high strain rates; therefore, elastic compliance is becoming a key material property for drop impact performance. A high compliance solder is expected to be favorable for drop impact performance because it tends to lower stress transfer to vulnerable joint region (Garner, 2009, Kim et al., 2007). Figure 2 is a schematic diagram showing two different hypothetical solder joint behaviors during drop

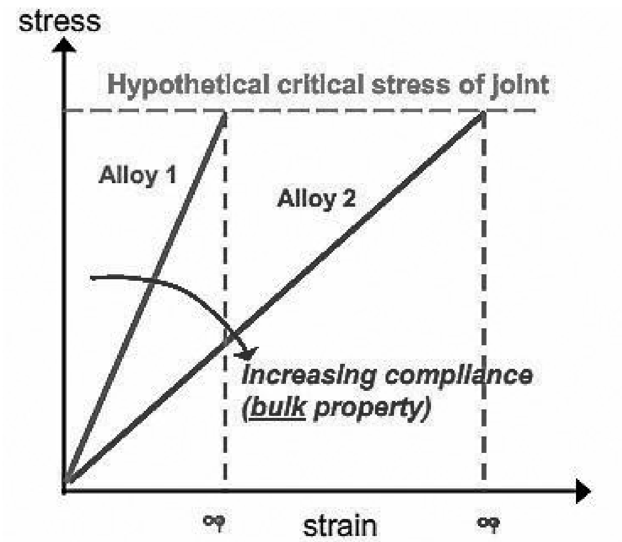


Fig. 2: Schematic stress-strain behavior of solder joint with two hypothetical alloys with different compliances. Note high compliance alloy (alloy 2) has lower stress under the same board displacement or strain (Suh et al., 2007)

testing. Alloy 2 has higher elastic compliance than alloy 1 and as a result, the stress at the solder joint of alloy 2 is lower than that of alloy 1 at the same board deflection (and therefore the same strain). Therefore, the solder joint with alloy 2 takes longer board deflection (or strain) to reach the same critical stress of the joint than the solder joint with alloy 1. In other words, a solder alloy with higher elastic compliance is expected to exhibit longer critical strain to failure (i.e., higher drop resistance) than a solder alloy with lower elastic compliance (Suh et al., 2007).

One of concerns for industry to address solder interconnect reliability under mechanical drop impact is the test methods for qualifying designs/materials and for quality assurance during manufacturing (Newman, 2005, Seah et al., 2006, Wong et al., 2005). Classic mechanical solder joint tests like shock, vibration and drop, result at the end mainly in electrical pass/fail information. More essential for solder joint characterization are test methods that provide more detailed information on the solder joint failure mode occurred. Fast Solder Ball Shear Test (see Figure 3) is recommended to address solder interconnect reliability (Grafe et al.). The interdependence between the various strength characteristics of a solder ball interconnect is depicted in Figure 4. A ductile/elastic solder alloy (1) is able to withstand higher strain rates compared to a stiffer solder alloy (2) before reaching the IMC fracture limit. The ability of a solder joint to deform in its bulk before IMC fracture is basically measured with FBST. The output from the FBST involves two basic parameters: (1) Energy before peak force (mJ) and (2) Fracture mode occurred in testing. The energy before peak is the area below the force plot till the peak force (see Figure 5), which directly correlates to the type of fracture which has happened and hence is useful for solder joint characterization (Grafe et al.).

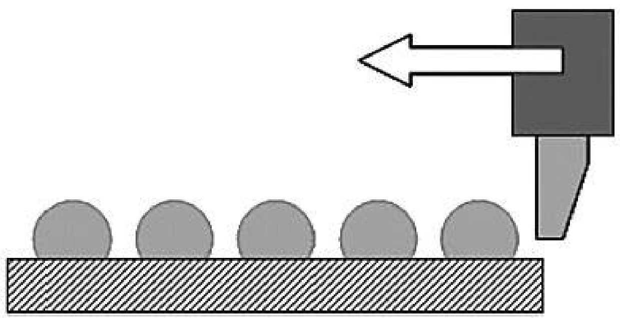


Fig. 3: Fast ball shear test arrangement (Grafe et al.)

The failure of board-level solder interconnects in drop tend to be more extensive in ball grid array BGA packages than land grid array because the joint is thicker and more dynamic strain is imposed (Frear et al., 2008). The drop impact failure behavior of the BGA joints was classified into three types in terms of the crack initiating points (see Figure 6); a crack initiating in the IMC layers (CI), a crack initiating in solder balls (CS), and a failure occurring as a result of large ductile deformation of solder balls (DD). For these three types of the failure, the corresponding three types of

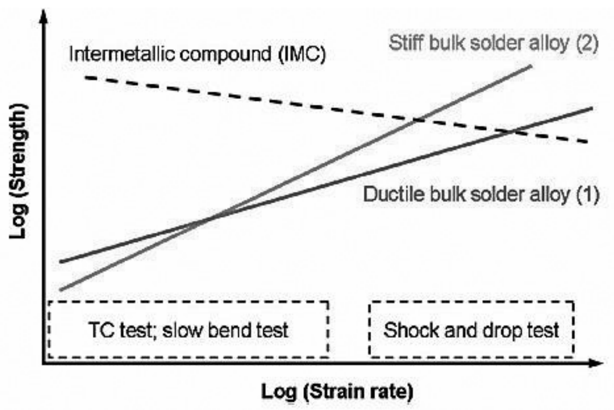


Fig. 4: Joint strength vs. strain rate (Grafe et al.)

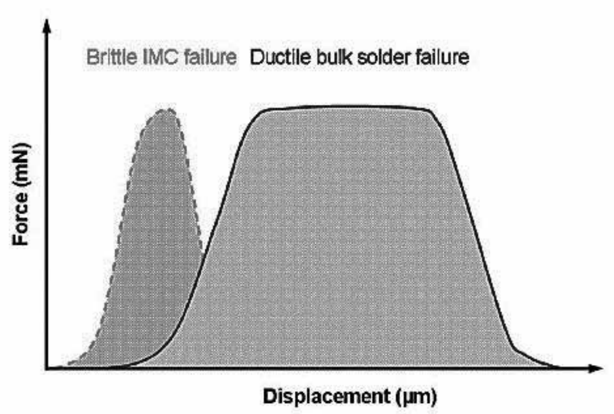


Fig. 5: FBST force vs. displacement (Grafe et al.)

practical failure situations can be considered (Tsukamoto et al., 2010). The CI-failure can occur in the practical situation that the BGA joints are subjected to high speed impact loadings such as drop conditions. The CS-failure can occur in the case that some objects bump into the solder balls in the packages. The DD-failure can occur in the case that the large shear deformation of solder parts occurs under low displacement- rate conditions (Tsukamoto et al., 2010).

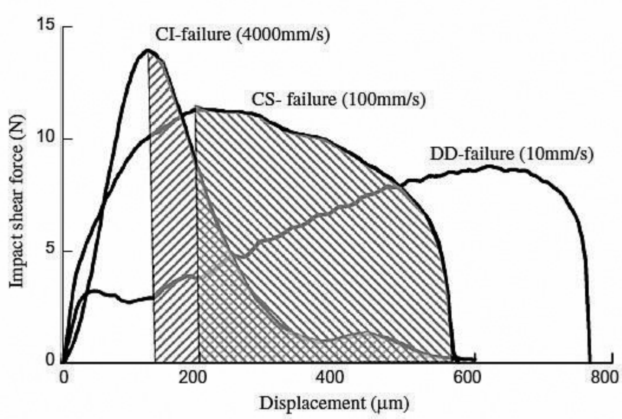


Fig. 6: Failure model of BGA joints subjected to shear loading (Tsukamoto et al., 2010)

3. Thermal cycling reliability

Thermo mechanical fatigue occurs when materials with different CTEs are joined and used in an environment that experiences cyclic temperature fluctuations resulting in imposed cycling strain. Thermo mechanical fatigue is a major deformation mechanism concern for solder joint in electronic packages (Frear et al., 2008). The type and magnitude of strains in solder joints under conditions of thermo mechanical fatigue is often quite complex. For surface mount applications, the strain is nominally in shear as shown in Figure 7. However, tensile and mixed-mode strains can occur due to bending of the chip- carrier or board as shown in Figure 8 (Abtew and Selvaduray, 2000, Frear, 1991, Frear et al., 1989).

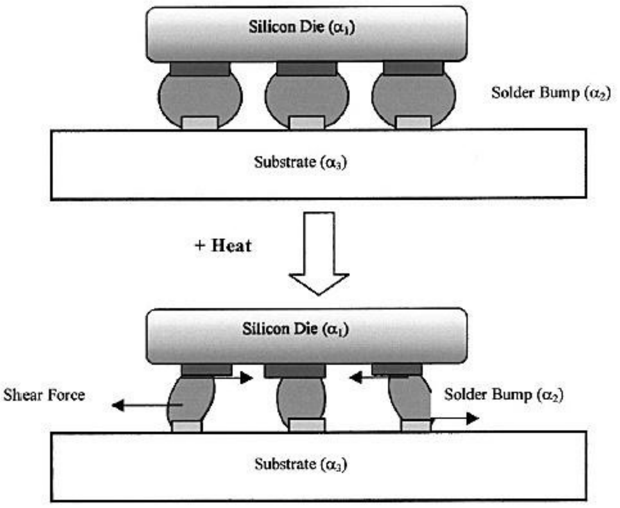


Fig. 7: solder joint subjected to shear strain during thermal cycling due to CTE mismatch (Abtew and Selvaduray, 2000)

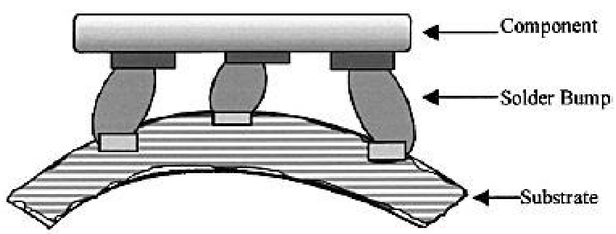
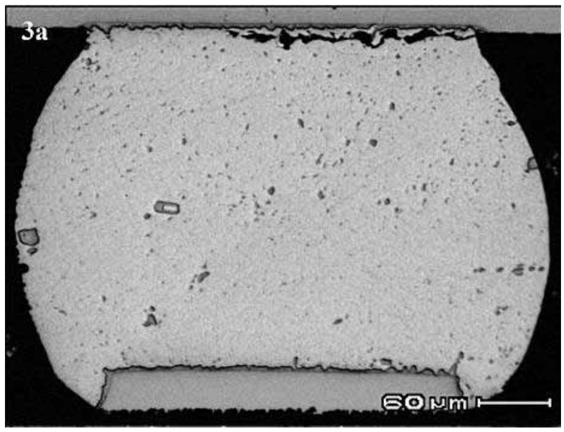


Fig. 8: solder joint subjected to tensile loading due to substrate flexing (Abtew and Selvaduray, 2000)

The combination of strain and temperature during thermo mechanical fatigue has a large effect on the microstructure, and micro structural evolution of solder joints (Frear, 1991, Frear et al., 1989). Strain concentration enhances diffusion leading to micro structural coarsening at elevated temperatures (Abell and Shen, 2002). It has been observed that typically only a fraction of the solder joint cross-section actually participates in cyclic deformation because strain distribution inside solder joints is seldom uniform. Deformation of the most highly strained areas of solder joints leads to localized deformation. The recrystallization or grain coarsening takes place first in the regions where the microstructure is most heavily deformed plastically and then gradually expands. Failure eventually occurs due to cracks that form in the coarsened regions of a joint. The thermal anisotropy of the recrystallized grains enhances the nucleation of micro cracks along their boundaries (Mattila, 2005). The failure mechanism under thermal cycling has been widely studied by many researchers (Hirano et al., 2001, Lee et al., 2002, Sohn, 2002). It was observed that cracks always take place inside the matrix of solder along or close to intermetallic layers closely parallel to the direction of imposed shear strain as shown in Figure 9. The propagation path of the crack shown in Figure 9a is enclosed entirely within the recrystallized region of the interconnection shown in Figure Figure 9b (Mattila et al.). The propagation of cracks, and therefore the reliability of interconnection, relies on the properties of solder matrix. The solder alloy with low strength facilitate plastic deformation of the solder alloy by external stress of solder joint and cracks are generated and grow more easily within the solder and shows poor fatigue resistance (Che et al.).

(a)



(b)

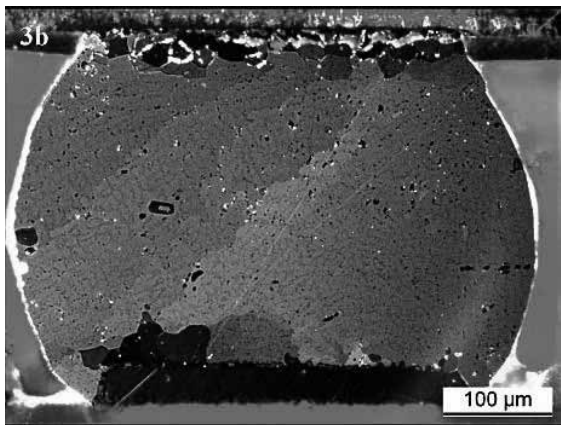


Fig. 9: Thermal cycle results (-40/125 OC) of SAC305 solder bump for a CSP BGA (Mattila et al.)

Standardized accelerated thermal cycling tests (ATC) are commonly used to evaluate the thermo mechanical reliability of electronic assemblies (Laurila et al., 2007, Li et al., 2009, Zhang et al., 2005). During ATC, assemblies are uniformly heated up and cooled down in order to induce thermo mechanical strains and stresses in interconnections and interfaces of the assemblies. The main processing unit of the contemporary handheld multimedia smart Nokia N95 phone (see Figure 10), the Application engine (AE), was chosen for thermo mechanical reliability characterization under accelerated thermal cycling test. The AE component is a stacked-die BGA package-on-package design. The structure of the component is shown in Figure 11. A polarized image of the critical interconnection cross-section after testing is shown on the left side of Figure 12. The image shows that a crack has initiated and propagated through the interconnection close to the intermetallic compound layer on the PWB side of the interconnection. The image also shows recrystallization of the bulk solder. The calculated von Mises stress contour map of the critical interconnection cross-section at the time of the peak stress (at the end of the ATC-40°C low-temperature dwell) is shown on the right side of Figure 12. It can be seen from Figure 12 that the contour map agrees well with the observed crack location (Karppinen et al., 2010).

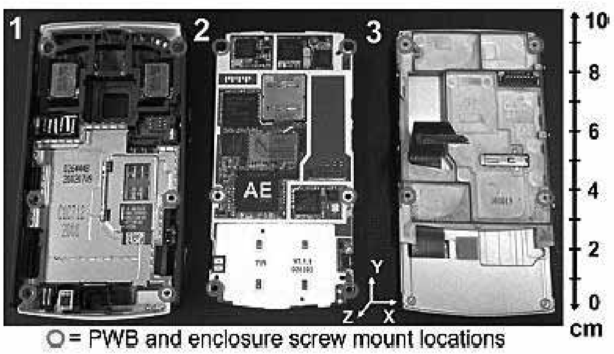


Fig. 10: Construction of the device: (1) lower enclosure, (2) main board and (3) display assembly. The Application engine (AE) component is marked for closer examination (Karppinen et al., 2010)

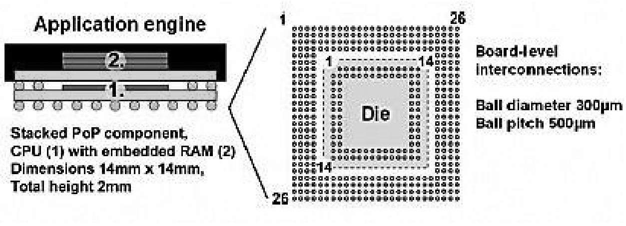


Fig. 11: Application engine component package (Karppinen et al., 2010)

4. Consecutive Multiple Loadings

Since portable electronics are often dropped after working for a period of time, usually interconnections are subjected to consecutive thermo-mechanical and mechanical loadings. The thermal cycling before drop test can introduce two different changes to the microstructure of interconnections: 1) The thermal mechanical strain and elevated temperature induces recrystallization in highly deformed region and fatigue cracks along large angle grain boundaries are developed; 2) The thickness of inter-metallic layers increases and the interfacial structure evolves with time. The first change weakens the mechanical properties of bulk solder under drop impact loading so that the cracking occurs partly through bulk solder (Mattila and Kivilahti, 2006).

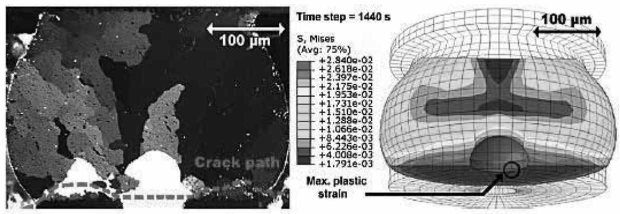


Fig. 12: Left: The polarized light cross-sectional image of the critical interconnection in ATC. Right: The calculated FEA stress contour map of the critical interconnection at the time of peak stress (end of low-temperature dwell at 40oC) (Karppinen et al., 2010)

Without temperature variation, the isothermal annealing has only the aging effects to interfacial microstructure. Since the effective time for inter-metallic growth is approximately only the total time of the upper soak stages in thermal cycling (Xu et al., 2005), inter-metallic layers have much more time to grow during isothermal annealing. If copper UBM is used on the component side, the formations of Cu_6Sn_5 and Cu_3Sn follow the typical growth kinetics (Mei et al., 1992, Paul, 2004, Rönkä et al., 1998). Given adequate time, the formation of "Kirkendall void" in the Cu_3Sn layer (Zeng et al., 2005) is much more severe during isothermal annealing and the rupture of inter-metallic layer becomes the primary failure mechanism, which degrades the drop loading reliability significantly (Mattila and Kivilahti, 2006).

5. Conclusion

Elevated operating temperatures can degrade/change the materials properties/ performance and the reliability of the solder joint.

The dominant failure mode under thermal cycling load is recrystallization-assisted crack nucleation and propagation. Hence, solder joint with a good fatigue resistance can be expected as result of inhibiting recrystallization.

High strength solder joint can exhibit a good fatigue resistance due to suppressing plastic deformation during thermal cycling loading.

The good drop performance can be attributed to extrinsic toughening mechanisms through high bulk compliance and high plastic energy dissipation during crack propagation.

Softer solder joint can help to absorb more dynamic energy during drop impact loading to reduce the dynamic stress transformed from PCB to IMC/solder interface layer.

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