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Journal of Microelectronics, Electronic Components and Materials

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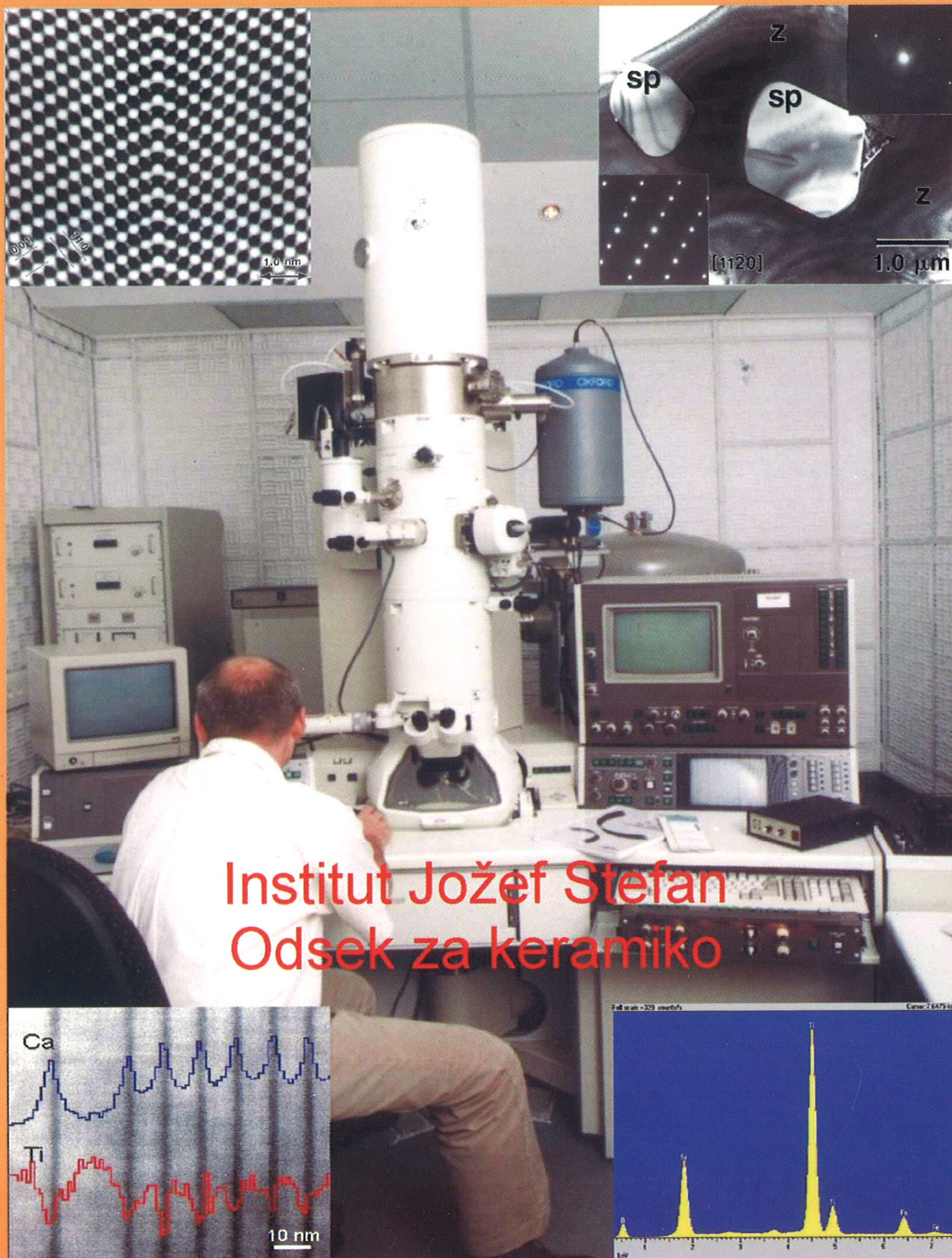

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TRENDI NA PODROČJU HIBRIDNE DEBELOPLASTNE TEHNOLOGIJE

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Ključne besede: fizika, elektrotehnika, elektronika, mikroelektronika, tehnologije hibridne debeloplastne, trendi razvoja, elektronika industrijska, MCM moduli multichip, LTCC tehnologije žganja keramike nizkotemperaturne, HTCC tehnologije žganja keramike visokotemperaturne

Povzetek: Hibridna debeloplastna tehnologija je zrela tehnologija, vendar je, kakor ostale elektronske tehnologije, v zadnjih desetih letih tudi ona doživljala pomembne spremembe. Spreminjala se je zaradi različnih tehničnih in tržnih vplivov, kot so konkurenčne tehnologije, razvoj novih materialov in elektronskih komponent, vrsta aplikacij, zahteve naročnika, globalizacija trga, itd. V Sloveniji pa je na razvoj še dodatno vplivala družbena in gospodarska tranzicija ter izguba "južnih" trgov. V prispevku so prikazani tehnološki in tržni trendi v svetu in v Sloveniji na področju hibridne debeloplastne tehnologije.

Technology Trends Within the Thick-film Hybrid Microelectronics

Keywords: physics, electrotechnics, electronics, microelectronics, hybrid thick film technologies, development trends, industrial electronics, MCM, Multi-Chip Modules, LTCC technologies, Low Temperature Cofired Ceramic, HTCC technologies, High Temperature Cofired Ceramic

Abstract: A thick-film technology is a mature technology. But like other technologies in electronic industry, the traditional market for thick-film hybrid circuits is changing fast. Over the last ten years the market for thick-film hybrid circuits was changed in term of types of market, technology, applications and geographic region. These changes were and are driven by competitive technologies, new materials and technologies, globalisation of the world market, etc.. Additional influence on the market in Slovenia had the social-economical transition and dissolution of former Yugoslavia. In this paper the technology and market changes and trends within the thick-film hybrid microelectronics in general and especially in Slovenia are described.

Uvod

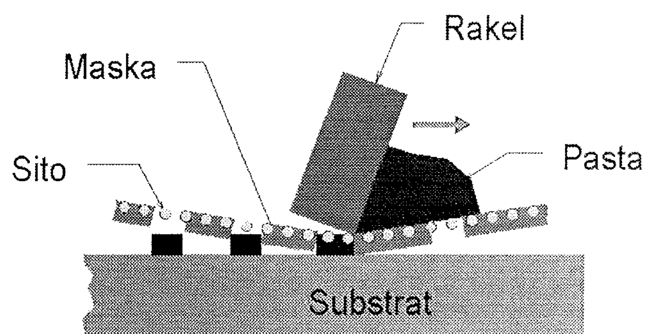
Hiter razvoj in globalni značaj svetovne elektronske industrije je gonilo za prenekatera področja znanosti in tehnologije kakor tudi za nekatere ostale industrijske panoge. Zaradi svoje velikosti pa vpliva tudi na splošen gospodarski razvoj držav, ki sodelujejo v tej industriji. Svetovni trg elektronskih izdelkov je leta 1997 znašal 993 milijard dolarjev in se pričakuje, da se bo do leta 2005 več kot podvojil in dosegel obseg dva bilijona dolarjev letno ter s tem postal največji posamezni svetovni trg /1/. Segment tega trga, ki ga je zavzemal "hardware" je bil približno 700 milijard dolarjev in se naj bi povečal na 1,6 bilijona dolarjev. Posamezni, najpomembnejši delež "hardwera" je vezan na procesiranje elektronskega signala, ki je obsegal 250 milijard dolarjev in se naj bi povečal za 2,6 krat, na 640 milijard dolarjev. Več kot polovico omenjenega tržnega deleža zavzemajo polprevodniške komponente s tržnim obsegom 140 milijard dolarjev v letu 1997 in s predvidenim povečanjem na 400 milijard dolarjev v letu 2005. Preostanek tržnega deleža pa pokrivajo t. i. sklopi (ang. packaging) kamor spadajo različne tehnologije za povezovanje, integracijo, zaščito, zapiranje v ohišje, itd. V ta tržni segment spada tudi hibridna debeloplastna tehnologija, ki se že od prve polovice šestdesetih let uporablja za izdelavo elektronskih vezij v obliki sklopov oziroma modulov.

Nadaljevanje bo posvečeno hibridni debeloplastni tehnologiji, ki je, tako kakor ostale elektronske tehnologije, v zadnjih desetih letih doživljala pomembne tehnološke in tržne spremembe.

Hibridna debeloplastna tehnologija

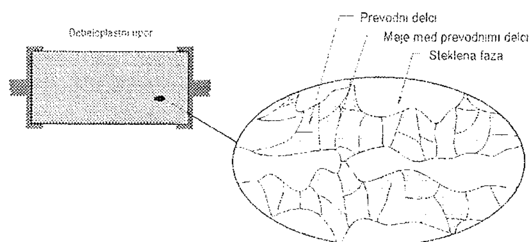
Hibridno debeloplastno vezje lahko opišemo kot majhno elektronsko vezje (sklop ali modul) sestavljeno iz debeloplastnega vezja in diskretnih elektronskih komponent. Ime hibrid ima zato, ker je modul izdelan z dvema ali več tehnologijami.

Osnovna hibridne debeloplastne tehnologija je debeloplastna tehnologija. To je tehnologija, ki z metodo sitotiska, sušenja (150°C) in žganja (850°C) debeloplastnih past integrira na keramičnem substratu (Al_2O_3) prevodne plasti, izolacijske plasti in upore. Princip sitotiska je prikazan na sliki 1. Izdelek imenujemo debeloplastno vezje, ker so debeline posameznih plasti po žganju okoli 15 µm, pri tankoplastni tehnologiji pa so plasti debele pod 1µm.

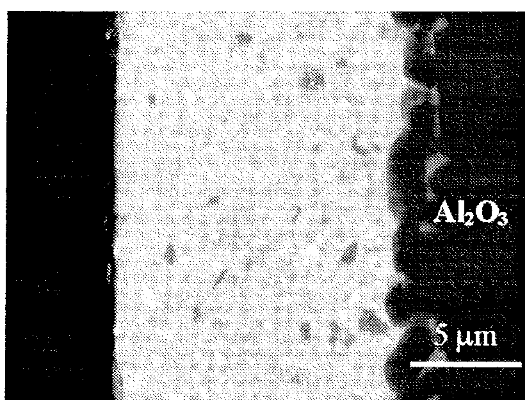


Slika 1: Princip tiskanja debeloplastnih past.

Prevodne linije in plasti so izdelane s tiskanjem debeloplastnih prevodnih past iz plemenitih kovin, kot so paladij, srebro, platina in zlato. Izolacijske plasti za križanje prevodnih linij in za izdelavo večplastnih vezij so izdelane z dielektričnimi pastami, ki so narejene na osnovi mešanice steklo-keramike. Dielektriki z nizko dielektrično konstanto se uporabljajo kot izolacijske plasti pri večplastnih vezjih visokih gostot. Dielektriki z visoko dielektrično konstanto pa se uporabljajo v nekaterih primerih za izdelavo debeloplastnih kondenzatorjev. Debeloplastni upori so izdelani iz uporovnih past z različnimi plastnimi upornostmi (od 10 do 10M ohm/kvadratek). Debeloplastne uporovne paste so sestavljene iz prevodnih kovinskih oksidov (npr.: rutenijev oksid ali rutenati) in steklene faze kot veziva. Depeloplastni upor in njegova struktura sta shematično prikazana na sliki 2. Na sliki 3 pa je prikazana mikrostruktura preseka debeloplastnega upora, posneta z elektronskim vrstičnim mikroskopom. Razmerje prevodnih delcev in steklene faze določa specifično upornost materiala. Končno (želeno) vrednost upornosti pa se dobi z laserskim doravnavanjem. Za zaščito debeloplastnega vezja pred mehanskimi in drugimi vplivi okolice se uporabljajo steklene zaščitne plasti, ki se žgejo pri nižji temperaturi (550°C). Vse debeloplastne paste vsebujejo poleg naštetih materialov še organska polnila, ki določajo pastam lastnosti, ki so potrebne za kvalitetno tiskanje. Ti organski materiali se, med sušenjem tiskanih plasti pri temperaturi od 150°C do 400°C, izločajo iz past.

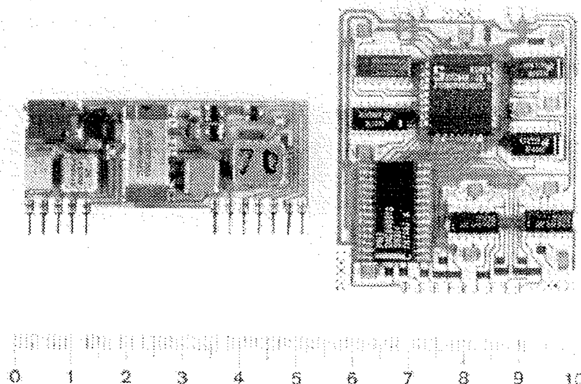


Slika 2: Debeloplastni upor in njegova struktura - shematično.



Slika 3: Mikrostruktura debeloplastnega upora posneta z elektronskim vrstičnim mikroskopom (Vir: Marko Hrovat in Zoran Samardžija).

Druga faza pri izdelavi hibridnega vezja je pritrjevanje diskretnih elektronskih komponent. Elektronske komponente različne po obliki (gole tabletke, SMD (surface mounted device), flip-chip, CSP (chip scale package), itd) in po funkciji (aktivne in pasivne komponente, monolitna integrirana vezja, itd) se pritrjujejo na debeloplastno vezje z različnimi tehnologijami, kot so spajkanje, bondiranje (povezovanje z zlato ali aluminijasto žičko), lepljenje itd. Na koncu pa se običajno hibridno vezje zaščiti z eno izmed izbranih metod, kot so potapljanje v lak ali barvo, potapljanje v epoksidne zalivke, oziroma zapiranje v plastična, keramična ali kovinska ohišja. Primer dveh hibridnih debeloplastnih vezij s SMD komponentami je prikazan na sliki 4.



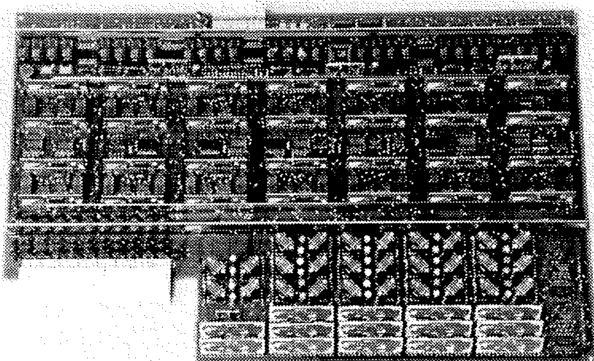
Slika 4: Dva hibridna debeloplastna vezja s SMD komponentami. SIL oblika vezja na levi strani za pokončno montažo in DIL oblika na desni za ležečo montažo.

Položaj hibridne debeloplastne tehnologije

Hibridna debeloplastna tehnologija je zrela tehnologija, saj je bil prvi debeloplastni izdelek narejen že v štiridesetih letih. Vendar se je šele v začetku šestdesetih let hibridna debeloplastna tehnologija razvila kot ena izmed mikroelektronskih tehnologij.

V splošnem je hibridna debeloplastna tehnologija ena izmed elektronskih tehnologij in je glede na stopnjo integracije postavljena med monolitna integrirana vezja in tiskana vezja. Vse omenjene tehnologije se neprestano razvijajo in na ta način medsebojno vplivajo druga na drugo. Hibridna debeloplastna tehnologija po eni strani predstavlja alternativo tako elektronskim vezjem na tiskaninah kot tudi monolitnim integriranim vezjem. Po drugi strani, kar je veliko pomembnejše, pa je komplementarna z obema omenjenima tehnologijama. Hibridna debeloplastna tehnologija omogoča povezovanje integriranih vezij in ostalih elektronskih komponent na keramičnem substratu, oziroma omogoča uporabo v tej tehnologiji izdelanega vezja na tiskanem vezju. Tak primer je prikazanem na sliki 5. Na sliki je naročniška plošča telefonske centrale IS2000, ki ima poleg ostalih komponent še 64 hibridnih debeloplastnih

vezij. Naročniška plošča omogoča priključitev 28 telefonskih linij, medtem ko je prejšnja generacija (brez hibridnih debeloplastnih vezij) omogočala priključitev le osmih telefonskih linij. Proizvajalec centrale pa ima razvoju že nove generacije central s tehnologijo, ki omogočajo še večje gostote.



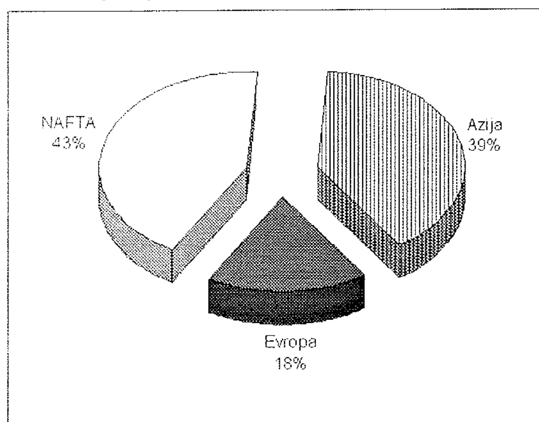
Slika 5: Naročniška plošča telefonske centrale IS2000 (proizvajalec Iskratel, Kranj) s 64 hibridnimi vezji (proizvajalec HIPOT-HYB, Šentjernej).

Glede na področje uporabe ima hibridna debeloplastna tehnologija prednost v sistemih, kjer je potrebna večja stopnja zanesljivosti delovanja in kjer so pomembne mehanske in termične lastnosti. Taka področja uporabe so avtomobilska elektronika, telekomunikacije ter vojaška, letalska in vesoljska elektronika. Poleg tega je debeloplastna tehnologija ena izmed prevladujočih tehnologij za izdelavo senzorjev in/ali pripadajoče elektronike za obdelavo senzorskega signala.

Trg hibridnih debeloplastnih vezij

Svetovni trg

Obseg svetovnega trga hibridne mikroelektronike je leta 1997 znašal približno 6,5 milijard dolarjev z 2,8% letno rastjo /2,3/. Približno 90% tega trga pripada debeloplastni tehnologiji ostalo pa tankoplastni, Regionalna razdelitev trga je prikazana na sliki 6. Največji delež, 2,8 milijard dolarjev, je leta 1997 pripadal združenju NAFTA.



Slika 6: Regionalna razdelitev svetovnega trga hibridne mikroelektronike v letu 1997.

Sledita mu Azija s 2,6 milijard dolarjev in Evropa 1,1 milijard dolarjev.

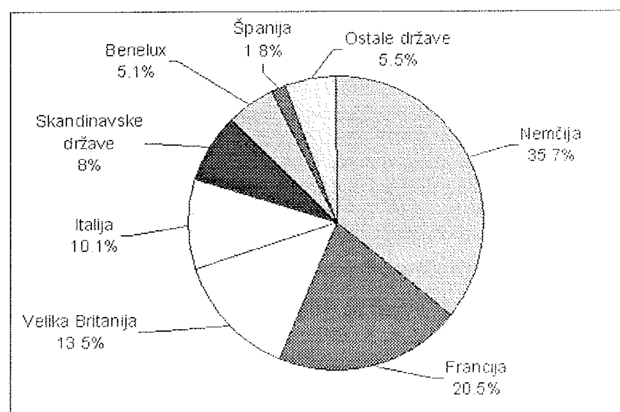
V Tabeli 1 pa je prikazan tržni delež največjih svetovnih proizvajalcev hibridnih vezij in države v katerih so sedeži družb. Očitno je, da so največje svetovne proizvajalke hibridnih vezij družbe s sedežem na Japonskem. Prva večja nejaponska družba je M-MAC s sedežem v Kanadi. Medtem, ko ima največji evropski proizvajalec Bosch manj kot 2% svetovnega deleža.

Tabela 1: Tržni deleži največjih svetovnih proizvajalcev hibridnih vezij

Družba	Država	Delež
Sanyo	Japonska	3,0%
Hitachi	Japonska	2,8%
Mitsubishi	Japonska	2,7%
Sanken	Japonska	2,6%
Rohm	Japonska	2,5%
NEC	Japonska	2,5%
M-MAC	Kanada	2,4%
Fujitsu	Japonska	2,0%
Bosch	Nemčija	1,9%
Philips	Nemčija	1,4%
Teledyne	ZDA	1,2%

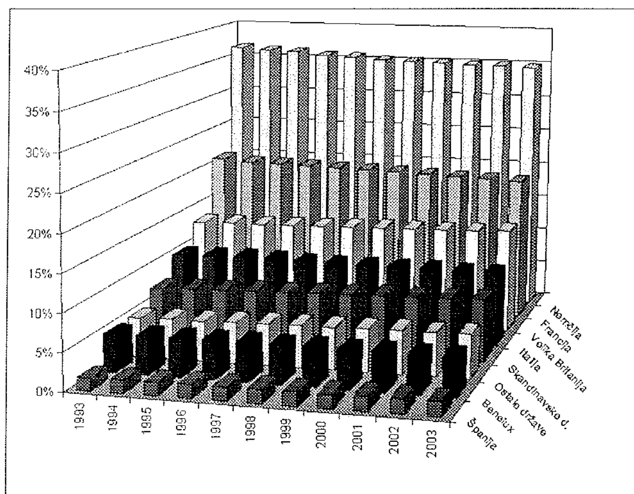
Evropski trg

Obseg evropskega trga hibridne mikroelektronike je leta 1997 znašal približno 1,1 milijard dolarjev s povprečno 2,3% letno rastjo /2,3,4,5,6/. Na sliki 7 so prikazani deleži posameznih držav, ki imajo več kot 2% delež trga. Vidimo, da več kakor tretjina trga pripada Nemčiji, sledijo ji pa Francija, Velika Britanija, Italija, Skandinavske države skupaj, Benelux in Španija. Na ostale evropske države skupaj pa odpade nekaj več kot 5% celotnega evropskega trga. Gibanje in trendi tržnih deležev v odstotkih po državah so prikazani na sliki 8. Večje spremembe se niso dogajale in tudi niso predvidene.



Slika 7: Razdelitev evropskega trga hibridne mikroelektronike v letu 1997 po državah.

Države, ki imajo večje tržne deleže bodo zgubile nekaj odstotkov na račun držav, ki imajo manjše deleže.



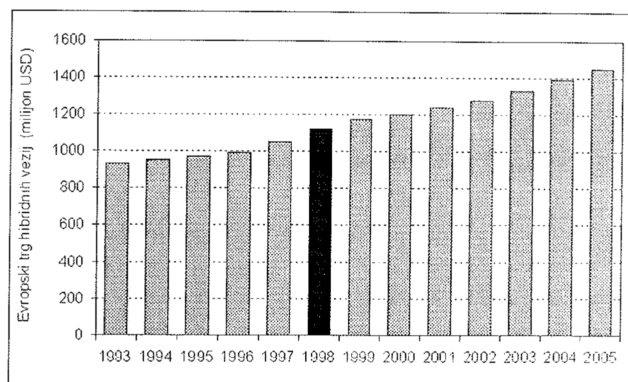
Slika 8: Trendi tržnih deležev hibridne mikroelektronike v Evropi po državah.

Tabela 2: Tržni deleži največjih evropskih proizvajalcev hibridnih vezij

Družba	Tržni delež
Bosch	11,3%
Philips	7,2%
Thomson	4,9%
AB Microelectronics	4,6%
Alcatel	3,1%
Roederstain	3,0%
Siemens	2,9%
MSE	2,0%
Ostali (<2%)	61,0%

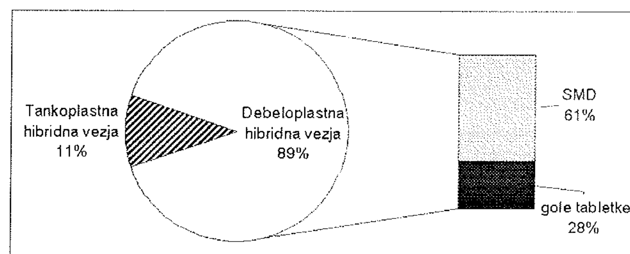
V Tabeli 2 so našteti največji evropski proizvajalci hibridnih vezij in njihov tržni delež. Izrazito velik tržni delež ima družba Bosch, ki mu delno sledi Philips. Za njima je skupina proizvajalcev z tržnim deležem od 2 do 5 odstotka. Velika večina evropskih proizvajalcev je manjših s posameznim tržnim deležem pod 2%. To so: Aspocomp, Aurel, C-MAC, Electromag, Ericsson, Fujitsu, Hybrid electronic, Marelli, Microdul, Mitsubishi, Nokia, Quintenz, Siegert, Telecontrolli,...). Značilno za večino proizvajalcev hibridnih vezij je, da je njihov trg praviloma notranji trg. To pomeni, da so praviloma del večjih družb, ki hibridna vezja naprej vgrajujejo v svoje izdelke in šele z njimi prihajajo na trg.

Celotni evropski trg hibridne mikroelektronike, analiziran leta 1998, je prikazan na sliki 9 /5/. Leta 1993 je ta trg znašal 930 milijonov dolarjev in se je do leta 1998 povečal za 20%. Do leta 2005 pa je predvideno povečanje še dodatnih 30%.

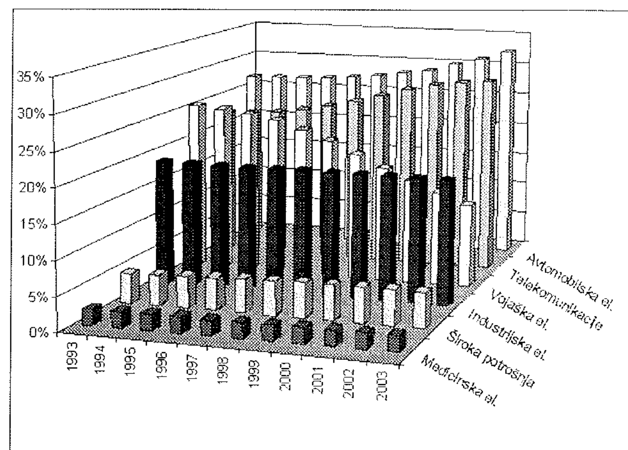


Slika 9: Rast evropskega trga hibridne mikroelektronike po letih.

Tržna analiza obsega debeloplastna in tankoplastna hibridna vezja. Debeloplastna so razdeljena še na hibridna vezja s SMD komponentami in na hibridna vezja z golimi tabletkami (ta segment vsebuje tudi t.i. keramične multičip module MCM-C). Njihovi deleži v letu 1997 so prikazani na sliki 10. V prihodnosti se spreminjanje razmerij med debeloplastnimi in tankoplastnimi hibridnimi vezji ne pričakuje. Do leta 2005 pa se pričakuje povečanje deleža debeloplastnih hibridnih vezij z golimi tabletkami (predvsem MCM-C) do 15 odstotkov na račun tistih s SMD komponentami.



Slika 10: Deleži trga hibridne mikroelektronike po tehnologijah v letu 1997.



Slika 11: Deleži trga hibridne mikroelektronike po področjih uporabe.

Glede na področje uporabe hibridnih vezij je največji tržni delež v avtomobilski elektroniki. Sledijo ji področja telekomunikacije, industrijske elektronike in področja vojaške, letalske in vesoljske elektronike. Spremembe tržnih deležev v letih od 1993 do 2003 so prikazani na sliki 11. Večje spremembe tržnih deležev se dogajajo predvsem v avtomobilski elektroniki (od 26% na 33%) in telekomunikacijah (od 23% na 30%), kjer deleži rastejo. Medtem ko pada delež, ki ga zavzema področje vojaške, letalske in vesoljske elektronike (od 25% na 12%), pa imajo področja industrijske elektronike (19%), široke potrošnje (5%) in medicinske elektronike (2,5%) relativno stabilne tržne deleže.

Tehnološki trendi

Tehnološke trende, ki se dogajajo na področju hibridne debeloplastne tehnologije lahko razdelimo na področje same tehnologije, novih elektronskih komponent, aplikacij hibridnih vezij in ostalo.

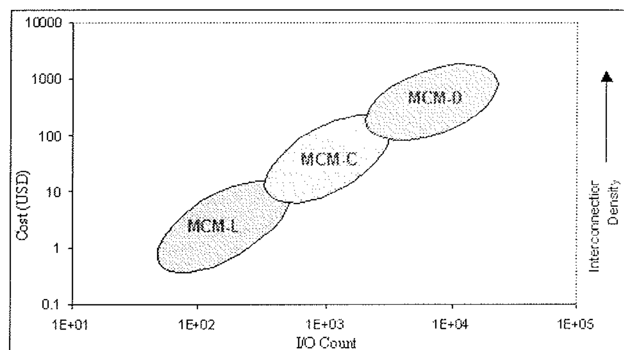
Trendi na področju tehnologije

Največje spremembe je hibridna debeloplastna tehnologija doživela na področju tehnologije povezo-vanja. Spremembe so nastale zaradi zahtev naročnikov po večanju gostote povezav, manjši teži, miniaturizaciji, enaki ali boljši kvaliteti ter nižji ceni /7, 8/.

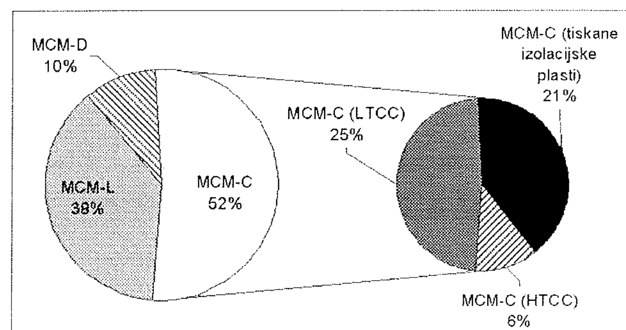
Tabela 3: Primerjava osnovnih lastnosti tehnologij za izdelavo multičip modulov (MCM)

MCM-D	
Prednosti	**Slabosti**
- sotek TCE s silicijem - velika gostota	- visoka cena
MCM-L	
Prednosti	**Slabosti**
- nizka cena - večje dimenzije	- TCE ni skladen s silicijem - nizka zgornja meja tempera. delovanja
MCM-C	
Prednosti	**Slabosti**
- delovanje v zahtevnem okolju - dovolj dober sotek TCE s silicijem - uporaba tudi pri višjih temperaturah - nižja cena od MCM-D	- omejene dimenzije

Za povezovanja visokih gostot so posebej primerni t.i. multičip moduli (MCM), ki so lahko izdelani v različnih tehnologijah: tankoplastni na silicijevem substratu (MCM-D), tiskana vezja na laminatu (MCM-L) in debeloplastni na keramičnem substratu (MCM-C). Osnovne prednosti in slabosti omenjenih tehnologij so prikazane v tabeli 3, komercialno tehnična razmerja pa na sliki 12. Razdelitev trga multičip modulov po tehnologijah je prikazana na sliki 13. Ta razdelitev je narejena po vrednosti trga. Če bi bila narejena po količini izdelkov, bi bila razmerja drugačna. Svetovni trg MCM je leta 1998 znašal 600 milijonov dolarjev in naj bi leta 2001 dosegel 840 milijonov dolarjev. Keramični multičip moduli (MCM-C) skupaj zavzemajo približno 52% delež /3/.



Slika 12: Komercialno tehnični položaj multičip modulov (MCM) po tehnologijah.



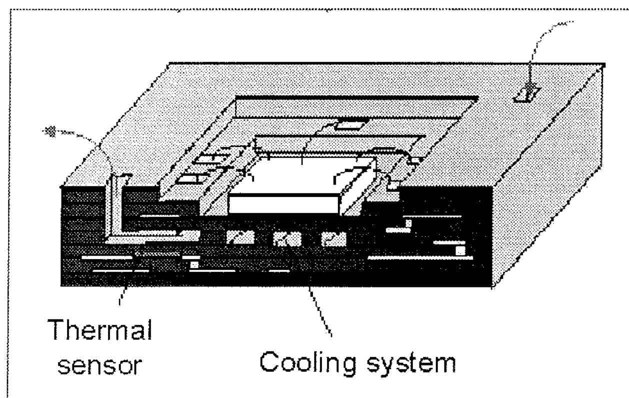
Slika 13: Vrednostni tržni deleži multičip modulov (MCM) po tehnologijah.

Keramični multičip moduli so sestavljeni iz večplastnega povezovalnega vezja in različnih diskretnih elektronskih komponent. Povezovalno vezje običajno vsebuje tudi integrirane pasivne elektronske komponente. Glede tehnologije izdelave povezovalnega vezja obstaja več vrst MCM-C. To so:

- LTCC - Low-Temperature Cofired Ceramic (Izolacijske plasti so izdelane iz keramičnih folij, ki se žgejo pri temperaturi 850°C)
- HTCC - High-Temperature Cofired Ceramic (Izolacijske plasti so izdelane iz keramičnih folij, ki se žgejo pri temperaturi okoli 1350°C)
- Tiskani (Izolacijske plasti so tiskane. Pri tem se uporabljajo različne tehnologije, kot so standardna debeloplastna, tehnologija difuzijskega oz. kemičnega oblikovanja in/ali foto-oblikovanje)

Največji delež keramičnih multičip modulov zavzema LTCC tehnologija. Fleksibilnost te tehnologije omogoča njeno uporabo ne samo v mikroelektroniki temveč tudi na drugih mikrotehnikah, kot so mikromehanika, mi-

krosenzorika, mikroaktorika, mikrofluidika in mikro-optika /9/. Na sliki 14 je prikazan detajl vezja, ki vsebuje poleg bondirane gole silicijeve tabletke še hladilni sistem s kanali in temperaturnim senzorjem, ki so integrirani v večplastni keramični strukturi.



Slika 14: LTCC tehnologija /9/. Detajl vezja z bondirano tabletko in integriranim hladilnim sistemom.

Poleg novih tehnologij povezovanja vpliva na razvoj hibridne debeloplastne tehnologije tudi razmah visokofrekvenčnih in močnostnih aplikacij.

Velika tržna rast mobilne telefonije in znatna rast trga telekomunikacij je vplivala na porast aplikacij hibridnih vezij tudi na visokofrekvenčnem področju. Debeloplastna tehnologija zaradi cenenosti in novih tehnologij (kot je foto-oblikovanje prevodnih linij) deloma prevzema to področje od tankoplastne tehnologije.

Močnostne aplikacije hibridnih debeloplastnih vezij, predvsem v avtomobilski elektroniki, narekujejo čim boljšo toplotno prevodnost substrata, čim boljšo toplotno prevodnost spoja komponenta/substrat in tudi substrat/ohišje ter čim boljšo električno prevodnost prevodnih plasti. V ta nam so različni proizvajalci razvili kar nekaj tehnologij, ki imajo osnovo v debeloplastni tehnologiji.

Nove elektronske komponente

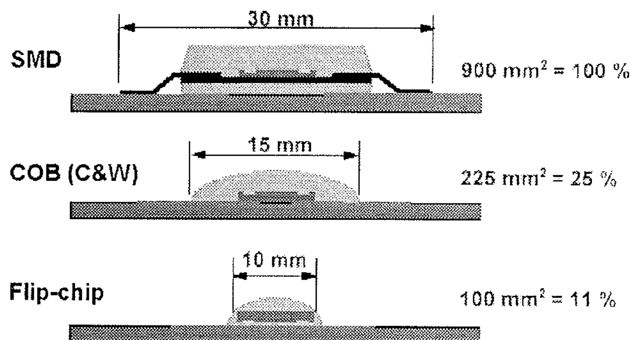
Diskretne elektronske komponente oz. čipi (integrirana monolitna vezja, pasivni elementi, polprevodniški elementi, itd) pomembno vplivajo na tehnologijo izdelave hibridnih vezij. Vplivni so predvsem parametri, kot so stopnja in vrsta integracije pri integriranih vezjih ter oblika (velikost) in način pritrjevanja čipov. Trenutno so najbolj uporabljane tehnologije za pritrjevanje in povezovanje diskretnih komponent sledeče: SMT (surface mounted technology) in bondiranje z zlato ali aluminijasto žičko. Razvoj pa gre v smeri sledečega zaporedja: flip-chip, BGA (ball grid array), CSP (chip scale package) in DCA (direct chip attachment). V tabeli 4 so prikazani svetovni tržni deleži (v milijardah kosov) integriranih vezij različnih ohišij za leto 1997 in predvidevanja za leto 2002 in leto 2007 /10/. V prvi skupini so komponente z žičkami, v drugi so komponente za površinsko montažo, v tretji skupini pa so komponente v modernih ohišjih.

Tabela 4: Svetovni tržni deleži in trendi integriranih vezij glede na različna ohišja (v milijardah kosov)

	1997	2002	2007
DIP	15,9	11,5	6,7
SIP	3,9	3,1	2,7
PGA	0,4	0,6	0,5
Ostali	0,4	0,6	0,8
Skupaj komp. z žičkami	20,6	15,8	10,7
SO	20,8	36,4	51,1
PLCC	2,3	1,4	0,6
PQFP	7,9	17,8	20,8
SMD keramika	0,2	0,3	0,3
BGA	0,2	1,3	2,2
TAB	0,9	1,6	1,9
Ostali SMD	1,0	2,1	3,4
Skupaj SMD komp.	33,3	60,9	80,3
CSP	0,1	1,5	6,5
COB	3,6	6,3	13,1
Flip chip	0,6	3,3	8,3
Skupaj moderne komp.	4,3	11,1	27,9
Vsa integ. vezja skupaj	**58,2**	**87,8**	**118,9**

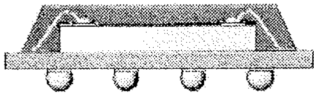
Na sliki 15 je prikazana primerjava uporabe istega integriranega vezja z različnimi tehnologijami pritrjevanja na substrat. Vidimo, da bondiranje golih silicijevih tabletk z zlato ali aluminijasto žičko zmanjša potrebno površini na četrtino, uporaba flip-chip tehnologije pa na dobro desetino površine, ki je potrebna za integrirano vezje v SMD ohišju.

Delo z golimi silicijevimi tabletkami in flip-chip komponentami zahteva poseben način dela glede delovnega okolja in glede opreme. Zato se vedno bolj uveljavlja ohišje CSP (chip scale package), ki je prikazano na sliki



Slika 15: Primerjava različnih tehnologij pritrjevanja elektronskih komponent.

16. Po definiciji komponente naj bi bila velikost ohišja samo 20% večja od gole silicijeve tabletke. Ker je gola silicijeva tabletka zaščitena se lahko komponenta uporablja kot ostale elektronske komponente za spajkanje. Spajka v obliki kroglic je že prisotna na priključkih na spodnji strani komponente. Priključki oz. kroglice so običajno razporejene v več vrstah. Razvoj tehnologije pa gre v smer uBGA (mikro Ball Grid Array).



Definicija:

$$\frac{\text{površina čipa}}{\text{površina ohišja}} >= 80\%$$

Slika 16: Integrirano vezje v ohišju CSP (chip scale package) /10/.

Trendi po področjih uporabe

Že analiza trga hibridne mikroelektronike po področjih uporabe kaže, da se nekatera področja bolj razvijajo, nekatera pa celo nazadujejo. Ti procesi vplivajo tudi na razvoj tehnologije hibridne mikroelektronike po posameznih področjih.

Avtomobilska elektronika

Avtomobilska elektronika je zahtevna elektronika in predstavlja motor pri razvoju tehnologij. Zahteve avtomobilske elektronike so: visoka zanesljivost, vezja srednje oz. velike moči, srednje število priključkov, velikokrat je zahtevana integracija senzorjev, pogosta zahteva po mehatronski združljivosti, izrazita zahteva po elektromagnetni združljivosti, nizka cena in proizvodnja velikega obsega. Debeloplastna tehnologija je primerna za omenjene zahteve.

Hibridna mikroelektronika bo ohranila svoj delež tako v elektroniki za varnost in pogon kakor tudi v najbolj zahtevnem okolju motorja. Poleg te uporabe bo prišlo tudi do decentralizacije in medsebojnega povezovanja elektronike, zaradi česar bo narasla uporaba hibridnih vezij v celoti.

Razvoj bo šel v smeri zmanjševanja števila tehnoloških procesov, zaradi zniževanja cene se bo zamenjala prevodna pasta Ag/Pd (3:1) s pasto, ki ima razmerje 5:1 ali celo 6:1, začela se bo masovna proizvodnja LTCC vezij, ki bodo imela integrirane pasivne elektronske komponente.

Telekomunikacije

Digitalizacija komutacijskih sistemov v osemdesetih letih je povzročila padec uporabe hibridnih vezij na področju telekomunikacij. Velika rast mobilne telefonije zadnjih let je vplivala na porast aplikacij hibridnih vezij tudi na visokofrekvenčnem področju v telekomunikacijah.

Razvoj bo šel v smeri uporabe cenejših LTCC ali difuzijsko oblikovanih vezij ter foto-občutljive paste za prevodnike pri visokofrekvenčnih aplikacijah. Nadaljeval se bo trend za izboljšanje lastnosti in zmanjšanje cene zaščitnih uporov. Uporabljala se bodo močnostna vezja, kot na primer DC/DC pretvorniki. Uporabljati se bo začela srebrna prevodna pasta in kvalitetnejše debeloplastne uporovne paste.

Vojaška, letalska in vesoljska elektronika

Padec tržnega deleža na področju vojaške, letalske in vesoljske elektronike pripisujejo programu COTS (Commercial off the shelf), ki ga je iniciral leta 1994 takratni obrambni minister ZDA dr. William Perry. Cilj programa je bil vključiti komercialne izdelke tudi v vojaško elektroniko. Tako to področje uporabe izgublja svoj obseg, saj se naj bi več uporabljali komercialni izdelki, ki pa so deležni še dodatnih testiranj in običajno zapiranja v hermetično ohišje.

Industrijska elektronika

Hibridna vezja bodo imela še vedno pomembno mesto na področju senzorjev in aktuatorjev, kadar ti zahtevajo uporabo analognih vezij. Hibridna vezja za obdelavo signalov pa bodo delno nadomestila ASIC vezja. Področje senzorjev in robotike odpira nove možnosti za razvoj hibridnih vezij v industrijski elektroniki. Na splošno se stanje v merilni, krmilni in varnostni tehniki ne bo spremenilo.

Elektronika za široko potrošnjo

Elektronika za široko potrošnjo nikoli ni bila pomemben tržni segment za hibridna vezja. Na tem področju so se potreba po hibridnih vezjih drastično zmanjšala v osemdesetih letih, ko se je pojavila tehnologija DMD komponent na tiskanih vezjih.

Medicinska elektronika

V medicinski elektroniki se razlogi za uporabo hibridnih vezij ne bodo spremenili. Na eni strani so visoko zahtevna vezja za različne "implante" (npr. vzbujevalnik srčnega ritma); na drugi strani pa so vezja v raznih napravah in pripomočkih za uporabo v bolnicah in ostalih zdravstvenih ustanovah (npr. različni senzorji).

Senzorji in senzorske tehnologije

Poseben pomen za napredek na področju senzorjev ima razvoj novih tehnologij, kot sta mikromehanika in mikroelektronika, združena v MEMS (Micro-Electro-Mehanical-Systems). Kljub pospešenem razvoju mikrosistemske tehnike, ki predstavlja integracijo številnih področij, kot so senzorika, aktorika, mikroperiferika, mikromehanika, integrirana optika itd., so prevladujoče tehnologije za izdelavo senzorjev in pripadajoče elektronike še vedno monolitne polprevodniške tehnologije ter tankoplastna in debeloplastna tehnologija.

Monolitne polprevodniške tehnologije imajo izrazito prednost v integraciji, miniaturizaciji in velikoserijski proizvodnji, ki omogoča nižjo ceno standardnih izdelkov.

Hibridna debeloplastna tehnologija ima prednost zaradi razvojne fleksibilnosti, ugodnih termičnih in mehanskih lastnosti keramičnega substrata, robustnost, možnost izdelave debeloplastnih senzorskih materialov za različne fizikalne in kemijske veličine, možnosti funkcionalnega doravnavanja pri različnih kompenzacijah ter cenenost proizvodnje pri manjših serijah. Hibridna debeloplastna tehnologija lahko pri izdelavi senzorjev nastopa v dveh vlogah. Prva je izdelava debeloplastnega senzorskega elementa. Druga vloga pa je integriranje senzorskega elementa, ki običajno ni debelopla-

sten (npr. silicijev piezoupornostni senzor tlaka), skupaj s kompenzacijskimi elementi in elektroniko za obdelavo električnega signala.

Ostali trendi

Na razvoj hibridne debeloplastne tehnologije vplivajo tudi nekatere splošne zahteve, kot so kvaliteta in zanesljivost delovanja izdelka, potreben hiter komercialni odziv, ekološke zahteve, dogajanja na trgu surovin, itd.

Kvaliteta in zanesljivost delovanja

Zaradi tržnih usmeritev hibridne mikroelektronike v zahtevnejše pogoje delovanja sta pojma kvaliteta izdelka in zanesljivost delovanja dobila še večji pomen. Z vidika kvalitete izdelka in zanesljivosti delovanja se natančno proučujejo tako posamezni gradniki hibridne mikroelektronike, posamezni detajli, kakor tudi celotni moduli ali celo sistemi. Parametri proučevanja so termo-električne, termo-mehanske, elektro-mehanske, topološke, elektronske funkcije, elementi elektromagnetne združljivosti, itd. Orodja in metode, ki se pri tem uporabljajo, pa so eksperimentiranje ter matematično modeliranje in računalniško simuliranje.

Komercialni odziv

Časi od naročila do izdelave prototipov in do prve proizvodne serije se krajšajo. Če je bil leta 1998 povprečen čas do prototipa 45 dni in dodatnih 15 dni do proizvodnje, bo leta 2009 ta čas 5 dni in dodatnih 5 dni. To naj bi veljalo za običajne izdelke, za zahtevnejše izdelke pa se bo čas skrajšal od 130 dni in dodatnih 74 dni na 50 dni in dodatnih 20 dni /7/. Zaradi zahtevane hitrosti odziva morajo biti proizvajalci na to pripravljeni. Obvladati morajo različna področja, tako da raziskujejo vnaprej oz. "na zalogo". Poleg tega morajo vključevati zunanje sodelavce in se povezovati s partnerji ter uporabljati različna računalniška simulacijska orodja, ki skrajšajo eksperimentiranje.

Ekološke zahteve

Ekološke zahteve tudi vplivajo na razvoj hibridne debeloplastne tehnologije. Ker se letno odvrže velike količine odpadne elektronske opreme, v Evropskem parlamentu uvajajo regulativo, ki bo urejala preventivno delovanje; zbiranje odpadkov; reciklažo odpadkov; izločanje nevarnih materialov in komponent iz novih izdelkov; zmanjšanje okolju neprijaznih snovi, ki se uporabljajo pri proizvodnji v elektronski industriji; ter harmonizacijo meril v državah Evropske zveze. Okolju neprijazni materiali, ki se še vedno uporabljajo v "elektroniki" so: živo srebro, kadmij, svinec, krom VI in nekatere sestavine plastičnih materialov. Velik "pretres" v celotni elektronski industriji bo gotovo nastal ob zamenjavi obstoječe spajke, ki vsebuje svinec, s tako brez svinca. Zaradi zahtevnost in obširnosti projekta so napovedan rok prepovedi uporabe spajk s svincem prestavili s 1.1. leta 2004 na 1.1. leta 2008.

Vpliv surovin

Dogajanja na trgu surovin, ki se uporabljajo v debeloplastni tehnologiji (paladij, srebro, platina, zlato, ...) tudi vplivajo na razvoj hibridne debeloplastne tehnologije. Najbolj drastični primer je cena paladija, ki je osnova prevodnih past, in je zrasla od 4 dolarje za gram leta 1997 na 28 dolarjev za gram sredi leta 2000. Zaradi omenjenega se vse pogosteje uporabljajo debeloplastne prevodne paste na osnovi srebra oz. paste na osnovi paladij-srebra z vse večjim deležem srebra.

Možne strategije delovanja

Strategija delovanja na področju hibridne mikroelektronike je, kakor na drugih področjih, odvisna od mnogoterih dejavnikov. Glede na prej naštete tehnološke in tržne spremembe in trende ter glede na velikost in okolje v katerem deluje, ima lahko proizvajalec hibridnih vezij sledeče strategije delovanja:

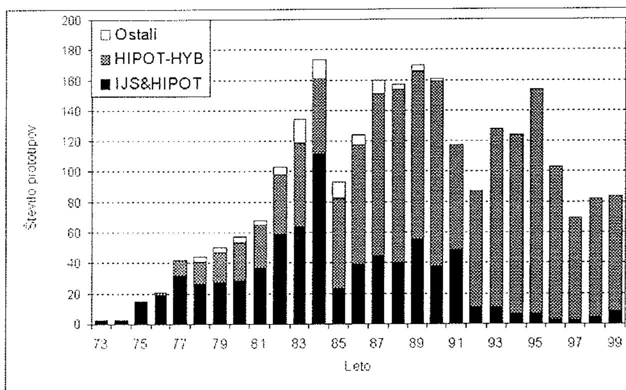
- Strategija masovne produkcije temelji na nizki ceni izdelka.
- Inovativna strategija temelji na hitrem in širokem obvladovanju novih tehnologij.
- Strategija kvalitetnih izdelkov je možna, če obstajajo zahtevnejši naročniki.
- Strategija ponudbe širokega spektra izdelkov lahko v nekem okolju predstavlja prednost, ker je večina izdelovalcev zožilo ponudbo.
- Strategija različnosti izdelkov je zelo razširjena. Pomeni, da poleg tehnologije hibridnih debeloplastnih vezij proizvajalec ponuja tudi druge sorodne tehnologije. Najpogosteje je to tehnologija tiskanih vezij ali/in tankoplastna tehnologija.
- Strategija servisa za naročnika je možna, če je sklenjena dolgoročna pogodba s strateškim naročnikom.
- Strategija tržne niše je primerna za manjše proizvajalce, ki se specializirajo za nek izdelek ali tehnologijo. Preozka specializacija pa je lahko tvegana.
- Strategija dela za večjega partnerja je zadnje čase pogosta pri manjših proizvajalcih. Ti običajno za večjega proizvajalca hibridnih vezij izdelujejo en ali nekaj izdelkov. V takih primerih je običajno razvojno-raziskovalno delo in trženje v popolni domeni naročnika.

Kombinacije nekaterih zgoraj naštetih strategij so možne, nekatere pa se izključujejo.

Dogajanje na področju hibridne debeloplastne tehnologije v Sloveniji

Začetki hibridne debeloplastne tehnologije v Sloveniji segajo v leto 1968, torej nekaj let po rojstvu te tehnologije v svetu, ko se je družba Iskra odločila, da bo osvojila to tehnologijo. Razvoj tehnologije so zaupali Institutu "Jožef Stefan" kjer so leta 1972 ustanovili mešano raziskovalno razvojno skupino v okviru Odseka za keramiko. Leta 1973 je podjetje Iskra Elementi predalo iniciativo svoji hčerinski firmi Iskra IEZE Uporovni elementi (kasneje Iskra IEZE HIPOT in sedaj HIPOT-HYB) iz Šentjerneja. Trenutno v Sloveniji proizvaja hibridna debeloplastna vezja družba HIPOT-HYB in delno tudi družba Iskra Avtoelektrika, ki na že izdelanem debeloplastnem vezju nadaljuje izdelavo hibridnega vezja. Poleg omenjenih institucij so se, praviloma v fazi razvoja, s hibridno debeloplastno mikroelektroniko ukvarjali tudi večji naročniki hibridnih vezij. To so bili predvsem podjetja družbe Iskra, kot so Iskra Telekomunikacije (sedaj Iskratel), Iskra Avtomatika (sedaj Iskra SYSEN),

Iskra Elektrozveze, itd. Sodelovali so tudi naročniki iz tujine, kot so IRET iz Italije in nekaj firm iz Nemčije. Do konca leta 1999 je bilo v tem okvirju razvitih nekaj čez 2500 prototipov hibridnih vezij. Razporeditev teh prototipov v posameznem letu pa je prikazana na sliki 17.



Slika 17: Število prototipov hibridnih vezij na leto.

Analiza podatkov na sliki 17 ponuja tri komentarje:

- Na diagramu vidimo nihanje števila prototipov. Prva dolina leta 1985 je nastala zaradi izpada naročnika iz tujine. Druga dolina leta 1991 in 1992 je nastala zaradi razpada Jugoslovanskega trga. Tretja dolina leta 1997 pa predstavlja zaključek večjega projekta.
- V osemdesetih letih so sodelovali pri razvoju prototipov tudi nekateri naročniki. Običajno so izdelali načrt hibridnega vezja. Procesiranje in izdelava prototipov pa je bila na Institutu "Jožef Stefan".
- V začetku devetdesetih let se je začel industrijski partner reorganizirati, tako da je prevzemal večino razvojnega dela in prepuščal mešani raziskovalno-razvojni skupini le raziskovalno delo in zahtevnejše razvojno delo. Reorganizacija je nastala zaradi spremenjenih pogojev poslovanja in zaradi priprav na standard ISO 9001, ki je bil pridobljen leta 1993.

Trg hibridnih vezij v Sloveniji

Trg hibridnih vezij v Sloveniji je v primerjavi z evropskim majhen. V letu 1997 je bil obseg približno 6 milijona dolarjev, kar je le 0,5% evropskega trga. Letno se izdela približno 2,5 milijona vezij, od katerih se 80% proda v tujino. Značaj trga hibridnih vezij v Sloveniji se je tekom let spreminjal zaradi različnih dejavnikov, kot so: spreminjanja tipa trga, tehnologij področje uporabe, geostrateških pogojev, tranzicije, itd. Vsi našteti dejavniki so običajno soodvisni in vplivajo hkrati.

Sprememba tipa trga:

Skozi osemdeseta leta se je trg hibridnih vezij v Sloveniji počasi spreminjal iz notranjega trga za družbo Iskra v odprti trg za zunanje naročnike. Ta sprememba je nastala predvsem zaradi premajhnega notranjega trga in v povezavi z ostalimi spodaj naštetimi spremembami.

Spremembe zaradi tehnologije:

Razvoj konkurenčnih tehnologij ima stalen vpliv na trg elektronskih tehnologij, tako tudi na trg hibridnih vezij v Sloveniji. Največja sprememba je nastala konec osemdesetih let, ko je SMD tehnologija na tiskanih vezjih prevzela precejšen del trga od hibridne debeloplastne tehnologije. Tipična sprememba, ki je nastala zaradi nove tehnologije, je digitalizacija komutacijskih sistemov v osemdesetih letih na področju telekomunikacij.

Sprememba področij uporabe:

Skozi leta proizvajanja hibridnih vezij v Sloveniji so se področja uporabe počasi spreminjala. V sedemdesetih letih in v začetku osemdesetih je bilo največje področje uporabe telekomunikacije, ki so mu sledila industrijska elektronika in elektronika za široko potrošnjo. V drugi polovici devetdesetih let je največji delež pripadal medicinski elektroniki (senzoriki), sledila pa so področja industrijske elektronike, telekomunikacij, avtomobilske elektronike in elektronike za široko potrošnjo. Trenutno ima največjo rast ravno področje medicinske elektronike (senzorike), sledita mu pa področji industrijske elektronike in avtomobilske elektronike.

Spremembe zaradi geostrateških pogojev:

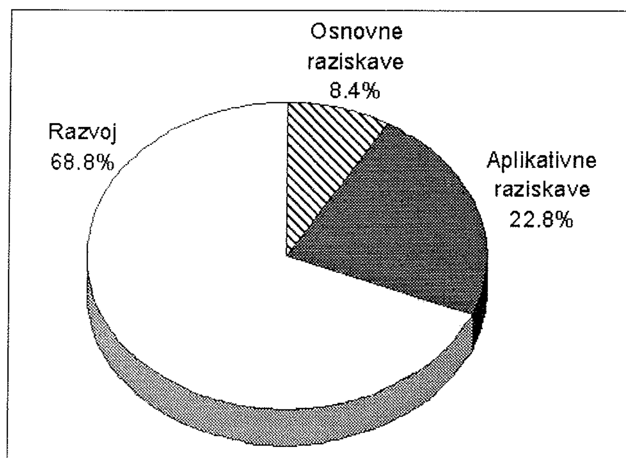
Značaj hibridne debeloplastne tehnologije zahteva tesno sodelovanje med naročnikom, načrtovalcem in proizvajalcem. Zato je bilo kvalitetno sodelovanje geografsko omejeno na radij do 500 km. Z globalizacijo svetovne ekonomije in z razvojem elektronskih komunikacij je ta geografska omejitev izgubila na pomenu. Dodatna pomembna sprememba, ki jo drugi proizvajalci niso imeli, pa je nastala leta 1991 po razpadu Jugoslavije, ko je prišlo neposredno ali posredno do 40% izgube trgov. Obnovitev obsega proizvodnje in iskanje novih trgov je trajalo kar nekaj let.

Raziskovalno-razvojna dejavnost na področju hibridnih vezij v Sloveniji

Raziskovalno razvojna (RR) dejavnost na področju hibridnih vezij v Sloveniji je organizirana v družbi HIPOT in na Institutu "Jožef Stefan". Obe instituciji že vrsto let tesno sodelujeta skozi mešano raziskovalno-razvojno skupino locirano na Odseku za keramiko Instituta "Jožef Stefan". Hkrati pa je razvito sodelovanje s tehnologi industrijskega partnerja HIPOT-HYB. Tesno sodelovanje med raziskovalci, razvojniki in tehnologi, poznavanje raziskovalnih zmožnosti in hkrati industrijskih problemov, omogoča mehak tehnološki transfer med raziskovalno sfero in industrijo. Na osnovi omenjenega je mogoče pripraviti kvalitetne raziskovalne in razvojne projekte, jih organizirati in izvajati z uigranimi projektnimi timi. Tako je razvito projektno sodelovanje z različnimi znanstveno raziskovalnimi institucijami doma in v tujini. Ravno tako razvojni oddelek v HIPOT-HYB sodeluje z razvojnimi oz. tehnično-komercialnimi subjekti doma in v tujini.

Raznovrstnost problematike v hibridni debeloplastni tehnologiji zahteva interdisciplinarni značaj RR dejavnosti. Pomembna področja so: elektronika, znanost o materialih, keramične tehnologije, področja iz fizike in kemije, načrtovanje vezij, in ne nazadnje znanja s področja zagotavljanja kvalitete in produktivnosti. Pomembna panoga RR dela je tudi senzorika, to zato, ker je strateška usmeritev industrijskega partnerja HIPOT-HYB poleg proizvodnje hibridnih vezij tudi proizvodnja senzorjev tlaka. Na zgoraj naštetih področjih so potre-

bne različne kategorije raziskovalnega dela in sicer od osnovnih (temeljnih) raziskav preko aplikativnih (uporabnih) raziskave do razvojnega dela. Ta statistična razdelitev RR dejavnosti je prikazana na sliki 18 /11/.



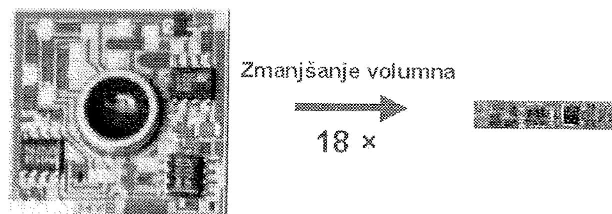
Slika 18: Razdelitev RR dejavnosti na področju hibridne debeloplastne tehnologije.

Največji delež RR dela zavzema razvojni segment (68,8%), ki je pomemben za tekoče delo družbe. Za večje projekte in za dolgoročne cilje RR dela pa sta ravno tako pomembna segmenta aplikativnih raziskav (22,8%) in osnovnih raziskav (8,4%). Segment aplikativnih raziskav se celo poveča na 28,7%, če v statistično analizo vključimo poleg hibridne tehnologije tudi senzoriko.

Relativno raznovrstnost RR dela lahko v polni meri izpeljejo le večji proizvajalci hibridnih vezij ali taki, ki jim je to temeljno poslanstvo (glej poglavje Možne strategije delovanja). Manjši proizvajalci si to lahko privoščijo le, če je njihovo RR delo subvencionirano s strani države ali Evropske zveze. V nasprotnem primeru si poiščejo drugačno strategijo npr. ozko usmerjenost ali delo za večjega partnerja. V državah Evropske zveze imajo to rešeno tako, da države podpirajo raziskovalno delo inštitutov in univerz, ki je usmerjeno v podporo gospodarstva. Veliko vzhodno-evropskih proizvajalcev hibridnih vezij, ki je preživelo tranzicijo, pa je izgubilo samostojnost in sedaj delajo za večje družbe z zahoda. Slovenski proizvajalec hibridnih vezij HIPOT-HYB spada v kategorijo majhnih oz. srednjih podjetij in je še v slovenski lasti. Zato je za njegovo samostojnost pomembno, da država podpira raziskovalno dejavnost javnih raziskovalnih institucij na področju hibridne debeloplastne tehnologije in senzorike.

Ilustrativen primer

Za boljše razumevanje razvoja hibridne debeloplastne tehnologije je ilustrativen primer izdelka na sliki 19. Na sliki sta prikazana dva senzorja tlaka s podobnimi lastnostmi. Prvi je bil razvit leta 1995 s konvencionalno debeloplastno tehnologijo in s površinsko montažo komponent, drugi pa je bil razvit leta 1999 z novimi tehnologijami.



Slika 19: Primerjava senzorja tlaka razvitega leta 1995 na levi in razvitega leta 1999 na desni.

Izrazita miniaturizacija (18 krat) je bila izvedena z uporabo vrste različnih tehnoloških rešitev, ki so opisane v literaturi /12, 13, 14, 15, 16/. V kratkem so te tehnološke rešitve sledeče:

Senzorski element

V obeh primerih je silicijev piezouporostni senzor tlaka uporabljen kot senzorski element le da je v miniaturni izvedbi merilni tlak "pripeljan" s spodnje strani. Taka uporaba senzorskega elementa je zahtevala poseben tehnološki pristop, ki pa ga je omogočilo sodelovanje (v okviru aplikativnega raziskovalnega projekta) z Laboratorijem za mikrosenzorske strukture na Fakulteti za elektrotehniko v Ljubljani

Elektronika za procesiranje senzorskega signala

Večji del elektronike za procesiranje senzorskega signala je izveden v posebnem integriranem vezju – ASIC (Application Specific Integrated Circuit). To vezje je nastalo v sodelovanju s firmo Analog Microelectronics iz Nemčije. Potrebno elektronsko znanje pa je nastajalo v okviru aplikativnega raziskovalnega projekta.

Povezovalno vezje

Integracija in povezava elektronskih aktivnih in pasivnih komponent ter senzorskega elementa je bila izvedena v obliki keramičnega multičip modula (MCM-C). MCM-C modul je bil narejen z metodo difuzijskega oblikovanja. Ta nova metoda je bila razvita v sodelovanju z Odsekom za keramiko na Institutu "Jožef Stefan" v Ljubljani. Osvojitev te tehnologije je bil del mednarodnega projekta z devetimi udeleženci iz petih držav.

Miniaturni upori

Vezje vsebuje osem debeloplastnih uporov. Z uporabo standardnih pravil načrtovanja je minimalna potrebna površina $48mm^2$. V našem primeru smo uporabili miniaturne debeloplastne upore, katerih skupna površina je $18mm^2$. Uspešnost uporabe taki uporov je omogočila predhodna raziskava njihove kvalitete. Raziskava je bila izvedena v sodelovanju s partnerjem s Češke.

Mehanska konstrukcija

Mehanska konstrukcija in uporabljeni materiali skupaj z sestavnimi deli in miniaturnim ohišjem je nastala na osnovi eksperimentiranja in dolgoletnih izkušenj na tem področju. Pokazala pa se je potreba po poglobljenem raziskovalnem delu na tem področju, ki bi rezultiralo v uporabi računalniških simulacij mehanskih, termomehanskih in elektromehanskih lastnosti. To bi precej dvignilo kvaliteto in skrajšalo čas razvojnega dela.

Dobro poznavanje področja senzorjev tlaka

Dobro poznavanje trga in tehnologij na področju senzorjev tlaka in debeloplastne tehnologije pa je pravzaprav prvi pogoj za uspešnost prikazanega projekta. Tu je prišlo do izraza dobro sodelovanje s tehničnimi in komercialnimi sodelavci družbe HIPOT-HYB.

Vsi našteti tehnološki postopki so bili uporabljeni za izdelavo prototipov. Sedaj poteka naslednja faza t.i. optimizacija tehnoloških postopkov, ki se bo potem nadaljevala s prenosom v proizvodnjo.

Zaključek

Hibridna debeloplastna tehnologija se je danes zasidrala na tistih področjih, kjer se zahteva sledeče:

- večja stopnja zanesljivosti delovanja
- boljšem odvajanju toplote (npr. močnostna vezja)
- mehanske in termo-mehanske lastnosti
- integracija po tehnologiji in funkciji različnih elektronskih komponent
- večja gostota funkcij
- zahtevnejših pogojih okolice
- izdelavi uporovnih vezij z ozkimi tolerancami uporov oziroma razmerij upornosti reda 0,1%
- pri vezjih, kjer je potreba po funkcionalnem doravnavanju
- ne nazadnje na področju senzorjev

Primerjava tehnoloških trendov elektronskih tehnologij kaže, da je hibridna debeloplastna tehnologija zrela tehnologija in da ima izglede za bodočnost. V svoji zgodovini je s svojo fleksibilnostjo vedno našla svoj prostor na trgu in dosega približno 2,8% letno rast v svetu.

Zahvale

Zahvaljujem se družbi HIPOT-HYB, d.o.o. Šentjernej, ki je dovolila objavo prispevka ter Ministrstvu za znanost in tehnologijo Republike Slovenije za sofinanciranje nekaterih projektov s področja hibridne debeloplastne tehnologije.

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SOFTWARE TOOL FOR THE SUPPORT OF ON-LINE THERMAL MONITORING OF MICROELECTRONIC SYSTEMS

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Key words: physics, electrotechnics, electronics, microelectronics, microelectronic systems, temperature monitoring, temperature sensors, measuring points, Delaunay triangulation, interpolation, simple algorithms, computer software, computer software tools

Abstract: An approach and the supporting software tool for the construction of isotherms for thermal monitoring of microelectronic systems is described. The approach is based on the triangulation of a set of measuring points corresponding to the positions of temperature sensors within the monitored system. Our implementation easily handles examples with thousands of points which drastically exceeds the number of temperature sensors in currently reported case studies. Construction of iso-lines and their interpolation to isotherms are algorithmically simple, fast and non-demanding solutions appropriate for on-line thermal monitoring implementations.

Programsko orodje za podporo sprotnemu nadzoru temperature v mikroelektronskih sistemih

Ključne besede: fizika, elektrotehnika, elektronika, mikroelektronika, sistemi mikroelektronski, nadzor temperature, senzorji temperature, točke merilne, Delaunay triangulacija, interpolacija, algoritmi enostavni, oprema programska računalniška, orodja programska racunalniška

Povzetek: V članku opisujemo postopek, podprt z izdelanim programskim orodjem, za konstrukcijo izoterm za nadzor temperature v mikroelektronskih sistemih. Postopek je osnovan na triangulaciji množice merilnih točk, ki ustrezajo pozicijam senzorjev v nadzorovanem sistemu. Razvita programska oprema z lahkoto obravnava primere z več tisoč točkami, kar sicer drastično presega število temperaturnih senzorjev v sedanjih eksperimentalnih študijah. Za konstrukcijo izoterm obstaja algoritmično enostavna, hitra in računsko nezahtevna rešitev primerna tudi za izvedbo sprotnega nadzora temperature v namenskih sistemih.

1 Introduction

With rapidly increasing complexity and operation speed of modern VLSI circuits and systems, temperature issues are becoming an important factor that must be considered for fail safe operation. On-line temperature monitoring by means of built-in temperature sensors aims at detecting potential thermal problems. If the temperature of the monitored part of the circuit or system increases and gets close to the given limit, precautions like decreasing the operating frequency, changing the execution of tasks or temporally switching off some parts of the system can be taken.

The common types temperature sensors are thermoresistors, thermocouples and active devices such as diodes and transistors. They can be produced with the same technologies as integrated circuits which makes it possible to integrate a temperature sensor in an IC. Sensors for thermal monitoring of microelectronic structures should have low power consumption (typically in the order 1mW or less), temperature range of 0-150 °C, and they should encompass a reasonably small area. In addition, linearity, accuracy and long-term stability are required. Different innovative approaches to the design of temperature sensors for on-line thermal monitoring have recently been reported /1-4/.

On-line temperature monitoring of a system requires continuous acquisition and processing of temperature measurements. The resulting data flow might slowdown the overall system operation hence some practical solution is needed to overcome the problem. Szekely *et al.* /2/, /4/, proposed the integration of temperature sensors within the bundary-scan (BS) infrastructure /5/. The idea is to integrate within the BS circuitry a frequency-output temperature sensor together with an internal counter and register to store the measurement result and to use the serial BS test data input/output line for the transfer of temperature measurement data. By minor modification of standard BS architecture and the addition of a few BS instructions, a temperature sensor with 2ms sampling time and 0.06 °C resolution has been implemented. The salient feature of this solution is that the existing BS test data input/output line can be employed to transmit temperature measurement data among the parts of system. BS approach, originally defined for digital systems has been extended to mixed-signal circuits /6/, /7/ which further generalises the above solution.

The management and processing of thermal measurement data via BS architecture is further elaborated in /4/. For a given set of subsystem elements (ICs or packages) with built-in temperature sensors a dedicated Thermal Monitoring Master (TMM) chip is proposed for the acquisition of temperature measurements within the subsystems. The reported case study was limited to a small number of sensors. However, if the number of sensors in a system is higher (i.e., 20-30 or even more), some strategy of selective readings of sensors need to be employed to process the data efficiently. Furthermore, problems of calibration need to be considered as well as diagnostic solutions in the case when individual sensors give unrealistic temperature values. The ulti-

mate goal is, of course, to have correct and sufficiently detailed presentation of the surface temperature distribution

The tool described in this paper offers an effective solution for the construction of isotherms. The approach is based on the triangulation of a set of measuring points, which can be performed off-line once the sensor positions are established. The next steps: construction of iso-lines and their interpolation to isotherms are algorithmically simple, fast and non-demanding solutions appropriate for on-line thermal monitoring implementations.

In the following we give a brief introduction to triangulation, construction of iso-lines and isotherms. We present the basic principles and comment the feasibility of the proposed solutions in practice. At the end of each section we describe the main features of our implementation. Finally, in the conclusion, we sketch the idea of the application of the implemented tool in on-line thermal monitoring.

2 Triangulating a Set of Measuring Points

2.1 Background

For a set *S* of 2D points, let us determine the maximal set of edges connecting these points such that the edges do not intersect. The problem is known as a maximal plane subdivision, but in engineering, it is usually referred to as *triangulation* /8/. One can perform, of course, many different triangulations upon the same set of points. Obviously, not all are good for engineering applications and we need a criterion for selecting the most appropriate one. Two criteria are widely accepted today:

- the first seeks for a triangulation whose total length of edges forming the triangulation is minimal (so-called minimal weight triangulation) /8/, and
- the second selects those triangulation whose smallest inner angle of all created triangles is maximal /9/.

There is a strong feeling that a determination of a minimal weight triangulation is NP-hard problem, although also simple approximations in a polynomial time are known /8/. However, these approximations may produce a lot of very thin triangles, which are usually not appropriate for further use in engineering. On the other hand, triangulation which optimises the smallest inner angle in the constructed triangulation creates much "better" triangles and is nowadays a preferred approach. Delaunay (a Russian mathematician) showed that there is a very simple rule - called empty circle property – which ensures that the triangulation is optimal regarding the smallest inner angle of all generated triangles /10/. He proved that every circumference circle determined by any triangle from that triangulation does not contain any other point from the input set of point *S*. Such a triangulation is referred to as Delaunay triangulation. Figure 1 shows an example of Delunay triangulation. For one of the triangles its circumference circle is plotted dashed. We can see that no any other input point falls into the circle.

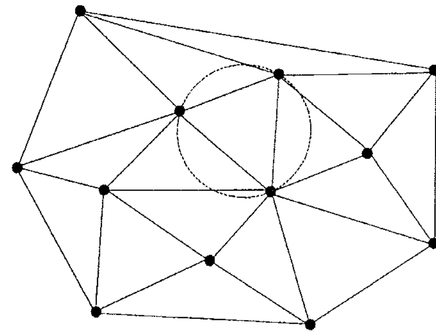

Figure 1 Delaunay triangulation

Different algorithms have been suggested for constructing Delaunay triangulation. One of the most popular today is the so-called *randomised incremental algorithm* described in /10/. The algorithm is fast and works in expected time complexity *O(n log n)*, but it is also memory demanding which often limits its applicability. On the other hand, Fang and Piegl introduced a triangulation algorithm, which is less memory demanding, but still efficient enough to handle huge set of points /11/. For acceleration, the algorithm uses a uniform plane subdivision which is very popular in applications of computational geometry /12/. We followed the Fang-Piegel's algorithm and a detailed description of our implementation can be found in /13/. Figure 2 shows a screen-dump of a 100 points being triangulated by our algorithm. To obtain better measured results and to show that the triangulation algorithm works stable, we have triangulated much larger sets of points. The CPU time measured on PC Pentium 2/266 Mhz, shows Table 1.

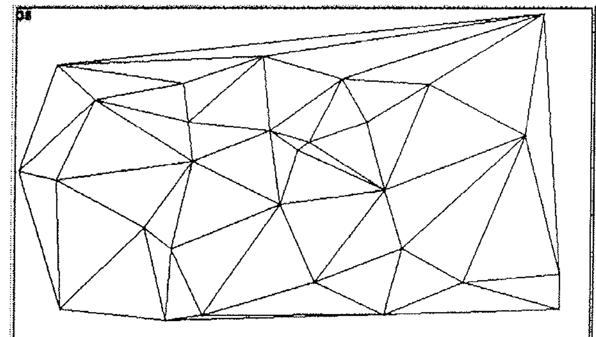

Figure 2 A screen-dump of 30 triangulated measurement points

Table 1 Spent CPU time of the triangulation algorithm

No. of points	Spent CPU (s)
1000	0.2
2000	0.6
5000	2.0
10000	4.4
15000	7.2
20000	10.8

3 Iso-line construction

Having triangulation and triangles arranged in the proper data structures, the next step is to construct the iso-lines (isotherms in our case). To speed up this part of the algorithm, each edge of the triangle has to have an information which triangles it borders (this information is obtained during the triangulation construction). Each edge is shared by at most two triangles (edges belonging to the convex hull border only one triangle). This information can be efficiently stored in the data structure using only two pointers.

The construction of the iso-lines consists of two steps:

- the set of polyline roughly interpolating the desired iso-line is constructed and
- the obtained set of polylines is interpolated by a curve.

3.1 Conctruction of iso-polylines

Let us consider an example shown in Figure 3a. The vertices of the triangles store the values of a scalar field (temperature in our case). Let us, for example, determine the isotherm displaying temperature of 100°C. This isotherm is roughly interpolated by two polylines in Figure 3a. One of them is closed and the second is not.

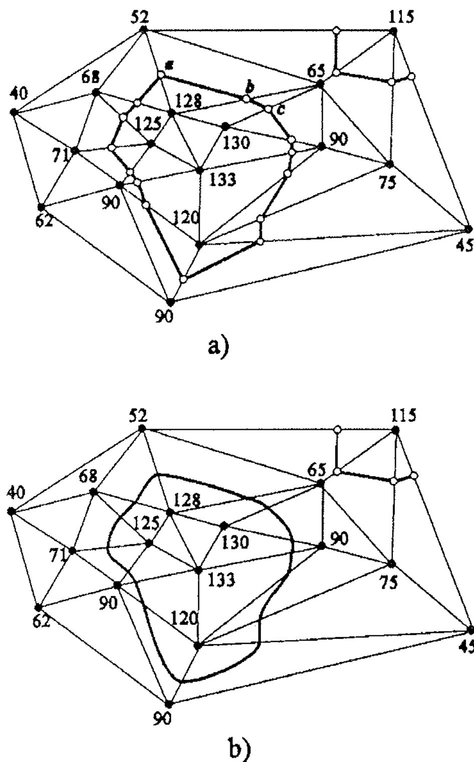

Figure 3 Construction of iso-polylines (a) Isotherms (b)

The algorithm searches at first through the set of triangles until it finds the first triangle whose vertices' temperature values enclose the value (i.e., 100°C). Suppose that it has found the triangle with the temperature value at the vertices (52°, 65°, 128°). The isotherm crosses the edges connecting vertices pairs (52°,128°) and (65°, 128°). The crossing corresponding to 100°C is determined using linear interpolation. When both points on the first triangle are determined (points ***a*** and ***b*** in Figure 3a), we mark the triangle as already used and move to the neighbouring triangle using the corresponding pointer where the next point is determined. The algorithm then continues until the starting triangle is met, or until an edge belonging to the convex hull of the set of point is determined. Such an edge has the pointer to the neighbouring triangle set to *NULL*. In this case, we must start to travel in the opposite direction from the starting triangle until the second boundary edge is met. The algorithm continues until all triangles are examined. Once the iso-polylines are obtained they are interpolated to get the isotherms shown in Figure 3b.

3.2 Interpolating the iso-polylines

There are different methods how to interpolate a given set of points and not all of them are appropriate for our purpose. Namely, the following properties are required: the curve should not oscillate, it should be smooth, the multiply values has to be easy to represented, algorithmically it must be simple and it should be plotted fast. The well-known Lagrange method, for example, does not fulfil these criteria. It oscillates and does not allow multiply values. In computer aided geometric design much better methods have been developed. They are known as piece-wise methods, because the final curve consists from segments smoothly fitting together. The most popular methods are for example: cubic Hermite interpolation, Catmull-Rom spline, Overhauser spline, Akima methods end others /14/. A comprehensive col-

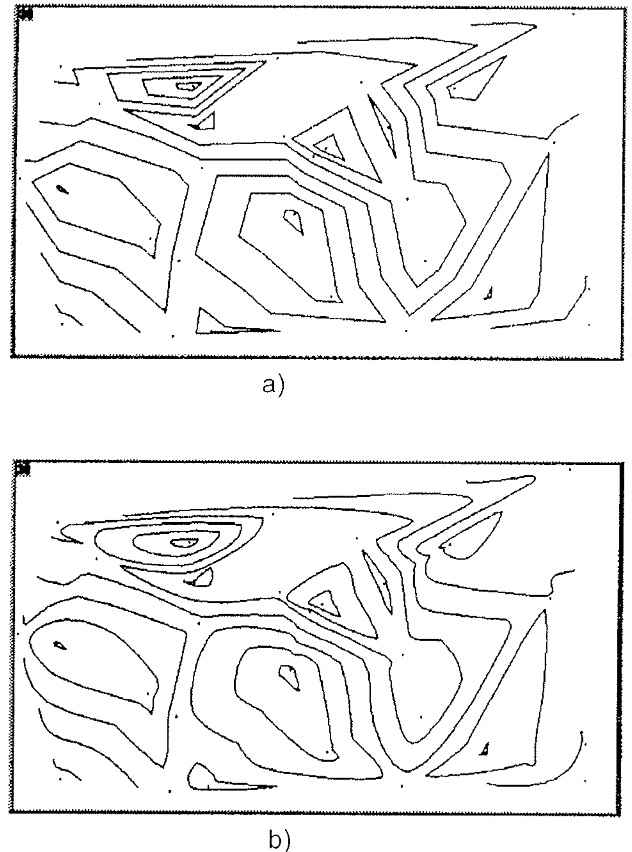

Figure 4 Isothermes showed by polylines (a) Isotherms interpolated by Hermit curves (b)

lection of methods is given in /15/. For our application we have used a variation of cubic C^1 Hermite interpolation. The method uses only polygons of third order therefore the calculations are fast. The result of our program is depicted in Figure 4. At the top (Figure 4a), iso-polylines are shown, while at the bottom, Hermit interpolation was used for the construction of the corresponding isotherms.

4 Conclusion

We have described an approach for the construction of isotherms based on the triangulation that can be applied in thermal monitoring of microelectronic systems. The first step, triangulation, is normally performed off-line due to the fact that sensor positions are defined once and known in advance for the given application. Our implementation easily handles examples with thousands of points /13/ which drastically exceeds the number of temperature sensors in currently reported case studies. After triangulation, the construction of isotherms is algorithmically simple and non-demanding which makes it suitable for embedded system implementations (i.e., on-line thermal monitoring). Linear interpolation that was used in the example in Section 3.1 for determining the crossing corresponding to 100°C serves just as a rough approximation, it can be replaced by other techniques describing more precisely temperature propagation on the employed materials and their geometry in each particular case.

Acknowledgement

The authors are grateful to dr. Franc Novak from Institut "Jožef Stefan", Ljubljana, Slovenia, for his help in preparation of the paper.

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DEVELOPMENT OF A SOLAR CELL MODEL WITH A PROGRAMME FOR CIRCUIT ANALYSIS - SPICE

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Keywords: physics, electrotechnics, electronics, microelectronics, solar cells, solar cell models, spectral sensitivity, computer software, circuit analysis, SPICE computer program, photovoltaic field, photovoltaic field simulation, SEG, Solar Electric Generators, characteristics of solar electric energy generator

Abstract: The paper describes development of a computer solar cell model with the programme for circuit analysis SPICE. The basic goal of the development has been to unify previous simulators of I-V characteristics and to develop a solar cell model with a standard tool (e.g. SPICE) to enable cheaper research of the entire photovoltaic systems. The computer analysis of this problem does not require purchasing of expensive solar modules in the development phase. The results presented in the paper have been prepared using various analysis tools of the circuit analysis programme SPICE.

Izdelava modela sončne celice s programom za analizo vezij - SPICE

Ključne besede: fizika, elektrotehnika, elektronika, mikroelektronika, celice sončne, modeli celic sončnih, občutljivost spektralna, programi računalniški, analize vezij, SPICE program računalniški, polje fotonapetostno, simulacija polja fotonapetostnega, SEG generatorji elektrike sončne, karakteristike generatorja energije električne sončne

Povzetek: V članku je opisana izdelava računalniškega modela sončne celice s programom za analizo vezij SPICE. Osnovno vodilo pri izdelavi modela je bilo, poenotiti dosedanje simulatorje I-U karakteristik oz. z nekim standardnim orodjem (npr. SPICE) razviti model sončne celice in s tem omogočiti cenejše raziskave celotnega fotonapetostnega sistema. Z računalniško obdelavo tega problema namreč odpade v času razvoja nakup dragih solarni modulov. Rezultate sem prikazal s pomočjo analiz, ki jih omogoča program za analizo vezij SPICE.

1. INTRODUCTION

In the recent years there has been ever increasing interest for alternative energy sources, especially for solar energy. To successfully prevent possible energy crises in the future, it is necessary to develop technologies for exploitation of new energy sources.

A special attention is paid to the exploitation of solar energy. There are many advantages of solar energy and its use: The sun is inexhaustible source of energy, the use of solar energy does not pollute the environment (chemically, radioactively or thermally), with the use of solar systems we can save other fuels. However the introduction and exploitation of new energy sources cause a series of problems. The intensity of introduction of these sources depends on energy potential and time required for development of technologies for their exploitation. It will be possible to replace conventional energy sources by solar energy only when it will be cheaper than conventional sources. This energy source is because of certain drawbacks (acceptability, small density, unreliability) expensive and due to meteorological dependence often unreliable.

With the improvement of technologies for manufacturing of solar cells (cheapening) and increase of their efficiencies (better utilisation of solar energy) it is to expect that the technology of direct conversion of solar energy to electricity will become commercially successful.

The paper describes development of a computer solar cell model with the programme for circuit analysis SPICE. The basic objective of the development has been to unify previous simulators of I-U characteristics and to develop a solar cell model with a standard tool (e.g. SPICE) to enable cheaper research of the entire photovoltaic systems. The computer analysis of this problem does not require purchasing of expensive solar modules in the development phase. The results presented in the paper have been prepared using various analyses tools of the circuit analysis programme SPICE.

According to the latest research results the direct conversion of solar energy to electricity should become one of the most important technology for exploitation of alternative energy sources.

2. SIMULATION OF SOLAR ELECTRIC GENERATOR'S CHARACTERISTICS

Often it is practically impossible to carry out experimental work with electric solar systems. This is true especially for high capacity commercial systems where each experimenting can cause unfavourable financial effect. On the other hand it is necessary to conduct research under strictly defined levels of solar radiation, which can only be achieved in laboratories. These problems can be avoided with the use of electronic circuits that enable a simulation of any configuration and capacity of electric solar system with a sufficient accurateness.

Below there is the description of the simulation of photovoltaic field with real electronic circuit, which is followed by the description of solar cell simulation using the programme for circuit analysis SPICE.

2.1 Simulation of Photovoltaic Field with Electronic Circuit

General shape of I-U characteristic of a solar electric generator (SEG), which should be produced by electronic simulator, is given in Figure 1.

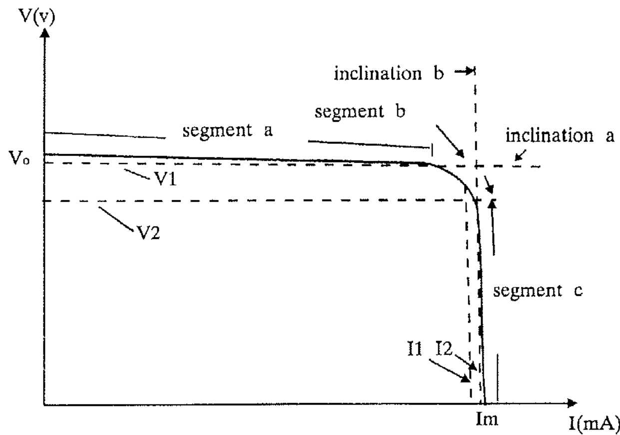

Figure 1: General shape of I-U characteristic of SEG

The distinctive shape of I-U characteristic of SEG consists of the following parts:

a) Straight line that corresponds to the segment „a" between zero current and I_1;

b) Exponential segment of the curve „b" corresponds to current in the range between I_1 and I_2;

c) Second part of the straight line that corresponds to the segment „c" between I_2 and I_m.

The first linear segment is determined by the internal resistance of the SEG, to which corresponds the inclination of the tangent to the curve. The same holds for the third segment, the only difference is different value of resistance due to the changed inclination. In the middle there is the exponential segment "b" that connects both linear segments "a" and "c". In the segment "b" the internal resistance is changing along its entire length.

Because of the above facts the problem of simulation of such curve with electronic configuration leads to the defining of source with controlled variable internal resistance and adaptable feedback, which enables simulation of variable internal resistance of SEG.

2.1.1Block Diagram of the Photovoltaic Simulator

Electronic structure that operates as a simulator consists of the following parts:

a) Source of DC current;

b) Element for shaping of power;

c) Sensor of current;

d) Exponential multiplicator;

e) Control element.

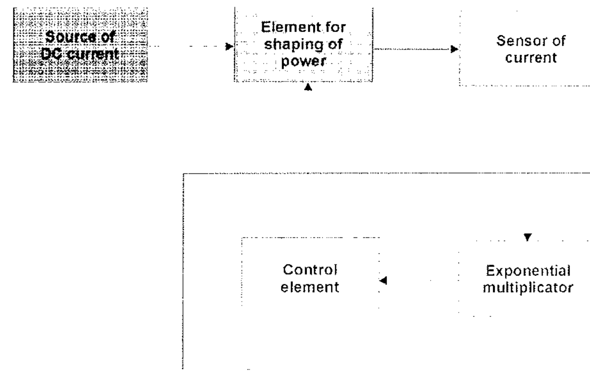

Figure 2: Block diagram of photovoltaic generator

2.2 Simulation of Solar Cell Model with the Programme for Circuit Analysis SPICE

So far, for the simulation of photovoltaic systems special programme packages have been developed. Their drawback was that they were not general programmes but adapted to the needs of each application. Such approach has led to the development of non-standard simulation tools. To overcome this problem it is necessary to apply standard programme package - simulator for simulation of electronic circuits and to build inside it a circuit that will serve as a model. The main advantage of such model is its increased flexibility. When the model is built it is possible to simulate with it any system only with a change of its individual components, according to the parameters of the system.

The simulator itself enables setting of all voltages and currents on its terminals, and also different types of circuit analysis.

2.2.1 Modelling of Components

In the designing phase of the sub-circuit consisting of electronic components in the programme SPICE, which should model the operation of a solar cell, the following parameters have to be taken into account:

a) Area of the cell . . . . (A)

b) Serial resistance . . . . (R_s)

c) Parallel resistance . . . . (R_p)

d) Ideality factor of the diode . . . . . . (n)

e) Short circuit current . . . . (I_{sc})

f) Temperature coefficient for Isc . . . . (Coef. I_{sc})

g) Open circuit voltage . . . . (U_{oc})

h) Energy gap of the junction . . . . . . (E_g)

i) p-layer . . . . (p_{gap})

j) n-layer . . . . (n_{gap})

Material of the solar cell can be either silicon or amorphous silicon.

The values of current I_{sc} and voltage U_{oc} are defined for standard conditions, i.e. irradiation 1 kWm^{-2} (AM 1.5)

and temperature 300K. If we wish to change conditions of irradiation and temperature during the simulation - for instance if the time of simulation is one day or more - we have to plan additional elements inside the sub-circuit and enable access to the terminals of these elements. For this purpose we use controlled voltage generators which allow simulation of constant, cosine or any other shape of changing of irradiation and temperature.

Figure 3 shows block diagram of the structure of the sub-circuit representing solar cell. The input parameters that are shown by arrows have numerical values, while the terminals represent inputs and outputs of the circuit.

Terminals 1 and 2 represent positive and negative output (V), while terminals 3 and 4 represent the following two inputs:

- Input 3 gives changing of irradiation with time (Wm^{-2})
- Input 4 gives changing of temperature with time (°C)

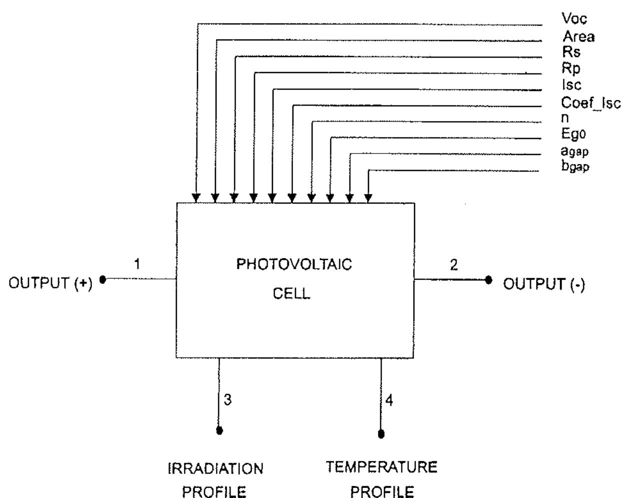

Figure 3: Parameters and input/output terminals of the sub-circuit that models solar cell in SPICE

Figure 4 shows the equivalent electronic circuit. All controlled sources are represented with squares. The controlled sources enable representation of the following quantities:

- Voltage controlled current source (G-irad): represents current, generated by light. Control voltage represents actual radiation profile in (Wm^{-2}) with which we control G-irad
- Voltage controlled current source (G-tidiod): represents dark current of diode, this is the current that flows through the cell when it is not irradiated. If it changes with time we have to control G-tidiod with E-temp.
- Voltage controlled voltage source (E-ininas): represents inverse saturation current of diode.
- Voltage controlled voltage source (E-temp): represents absolute temperature in (K)

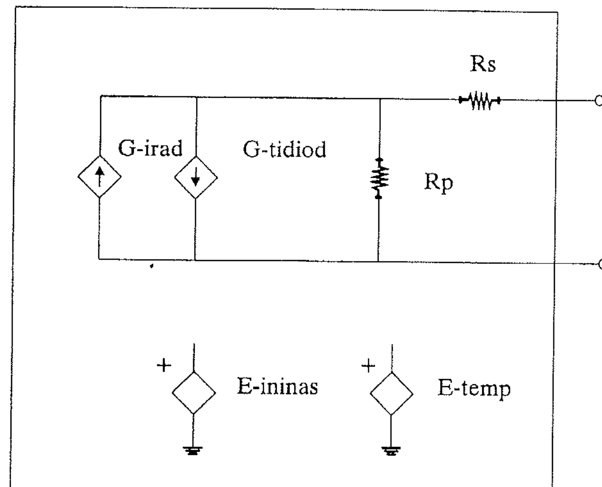

Figure 4: Equivalent diagram of circuit for solar cell

Photovoltaic modules are now modelled in such a way that more equivalent circuits, connected in series, as shown in Figure 4, are used. These composed modules can be connected in series or in parallel, so the solar fields can be composed.

The most important advantage of such approach to modelling, where each cell is modelled separately, is that it is relatively simple to simulate I-U characteristic of a real module or field. In this way different values of irradiation in each cell are taken into account, as well as different serial resistances R_S, parallel resistances R_P in ideality factors of diodes n, which are different for each cell.

2.2.2 Equivalent Model of Circuit

The first step of the designing of the equivalent circuit was designing of the generator or light source. This generator was conceived as a source with which the spectral sensitivity of the solar cell's material was simulated. With the voltage waveform, obtained at the generator terminals, the voltage controlled current source was controlled.

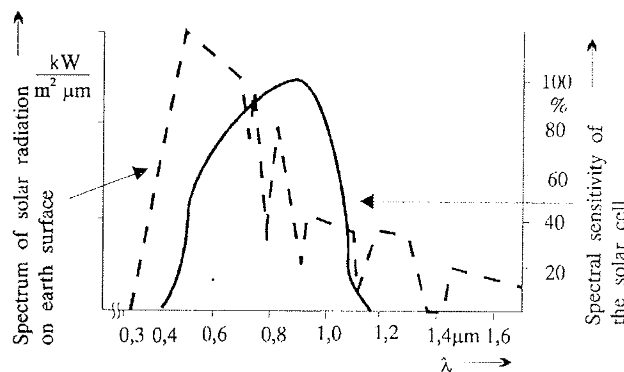

Figure 5: Spectral distribution of solar radiant energy (on the earth surface) and spectral sensitivity of the solar cell

For the solar cell efficiency it would be ideal if the spectral sensitivity of the material was wider than the solar spectrum. With this the entire solar spectrum that penetrates through the atmosphere to the surface would be taken into account. As can be seen from the Figure 5 this is not the case for silicon, therefore the voltage waveform at the generator terminals was shaped in accordance with this diagram.

Generator that represents solar source, with which spectral sensitivity of the solar cell's material was simulated, consists of the following components:

- impulse generator
- resistor attenuator, consisting of resistors and diodes

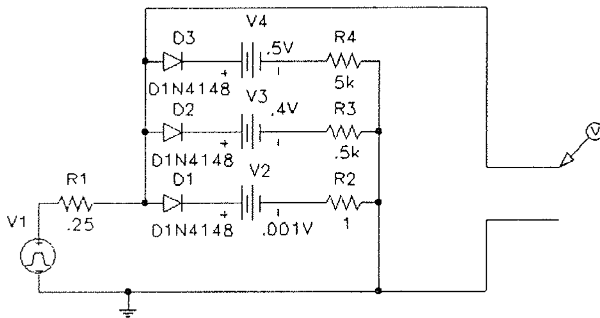

Figure 6: Generator - circuit for simulation of spectral sensitivity of solar cell material

Waveform of output voltage at the terminals of the generator (circuit for simulation of spectral sensitivity of solar cell material) is shown in Figure 7.

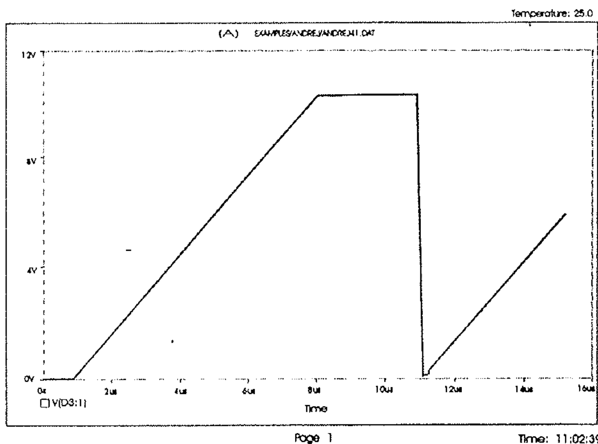

Figure 7: Output voltage on the generator terminals

This voltage was determined with transient analysis of the circuit that is enabled by the programme for circuit analysis SPICE.

In the next stage the equivalent circuit of the solar cell was modelled. Solar cell can be represented as an electronic circuit that is shown in Figure 8.

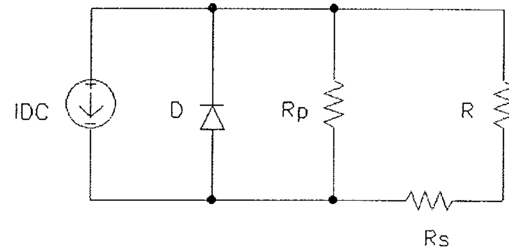

Figure 8: Electric equivalent circuit of the solar cell

The roles of different components of the circuit are as follows:

- source of constant current IDC:
  simulates current that flows when the cell is irradiated
- - diode D:
  simulates the reverse current of the solar cell, it also simulates the following parameters: ideality factor of diode (n), widths of n and p layer of semiconductor (a_{gap}) and (b_{gap})
- - parallel resistance R_p:
  simulates faults in the solar cell material
- - serial resistance R_s:
  simulates resistance of solar cell contacts

Both equivalent circuits have to be connected and an analysis in the programme for circuit analysis SPICE has to be carried out. Generator (equivalent circuit for simulation of spectral sensitivity of solar cell material) is connected to the equivalent circuit of the solar cell via a voltage controlled current generator.

Figure 9 shows the complete model of solar cell.

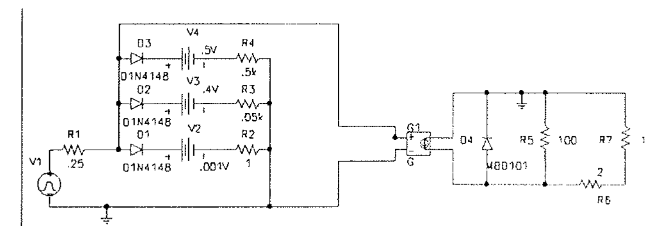

Figure 9: Complete model of solar cell

3. RESULTS

The purpose of these simulations was to obtain with the model such I-U characteristics that will be at the same conditions comparable with measured I-U characteristics of real solar cells.

Below there is a comparison of results for different values of irradiation of solar cells: I-U characteristic of real solar cell against I-U characteristic of the model.

Programme for circuit analysis SPICE was used for the simulation of characteristics of solar cell model. DC analysis was used for analysis of solar cell model.

3.1 Presentation of Simulation Results

For the measurements, a solar cell manufactured by Rade Končar, was used.

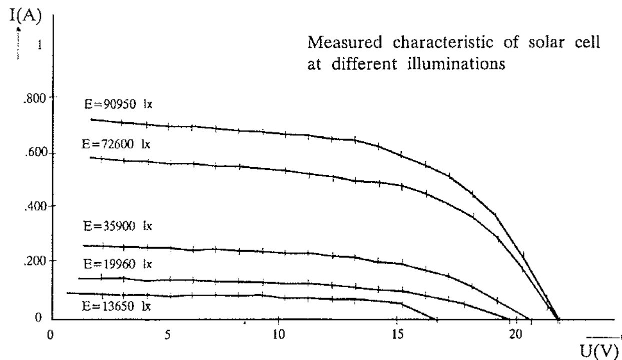

Fig. 10: Presentation of all measured characteristics of the real cell

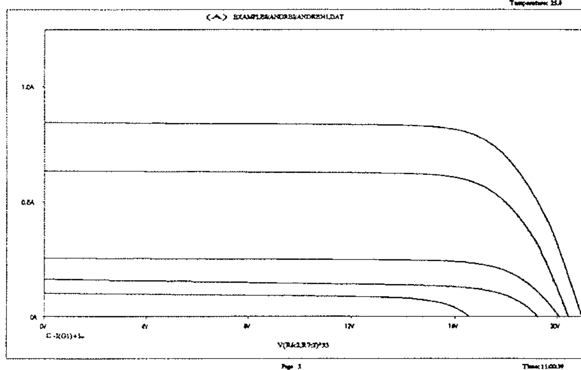

Fig. 11: Presentation of all simulated characteristics of the model

4. CONCLUSIONS

For the development of the solar cell model the MicroSim Corporation's programme for circuit analysis SPICE, development version 6.1a, was used. With this programme the output characteristics of the solar cell model were also analysed. These characteristics were compared with measured output characteristics of real solar cells. The comparison of measured and real output I-U characteristics shows that they are identical.

This analysis showed that the use of the programme SPICE for the simulation of photovoltaic systems gave results, comparable with real systems. Such approach to the analysis of photovoltaic systems also offers a quick insight in all voltages and currents in the system, gives a lot of possibilities for changing of circuit topology and enables an easy connection with standard electronic devices.

The era of cheap and always available energy is slowly coming to an end. In the future the real energy price will also include the costs of processing and storage of radioactive wastes, costs of interventions in the case of natural catastrophes caused by the climate changes, costs of removing the oil spills, etc. Solar energy is friendly for the environment, therefore it is expected that its importance will increase in the future. Standardised computer aided approach will make the development of photovoltaic systems cheaper, since the technological development in this field still does not follow the needs.

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FORMAL VERIFICATION OF DIGITAL CIRCUITS USING SYMBOLIC MODEL CHECKING

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Abstract: This paper presents efficient algorithms for digital circuit verification. The algorithms are based on symbolic CTL (Computation Tree Logic) model checking. We also present an extension of ordinary CTL with fairness constraints. They enable verification of circuits with symbolic model checking regarding only fair paths in the computation tree. The model checking algorithms were implemented as part of a fully home-made program package for manipulating finite state machine descriptions of digital circuits, represented with Boolean functions. The package is also based on a fully home-made program package for manipulating Boolean functions, represented with binary decision diagrams.

Formalna verifikacija digitalnih vezij s simboličnim preverjanjem modelov

Ključne besede: elektrotehnika, računalništvo, vezja digitalna, BDD grafi odločitveni binarni, FSM stroji stanj končnih, relacije prehajalne, funkcije karakteristične, stanja dosegljiva, CTL logika drevesa izračunavanj, omejitve poštenostne, verifikacija formalna, preverjanje modelov simbolično, oprema programska računalniška, paketi opreme programske, rezultati eksperimentalni

Povzetek: V članku predstavljamo učinkovite algoritme za verifikacijo digitalnih vezij. Algoritmi temeljijo na simboličnem preverjanju modelov z logiko drevesa izvajanj ("Computation Tree Logic" - CTL). Prav tako predstavljamo razširitev navadnega CTL s poštenostnimi omejitvami, ki omogočajo verifikacijo vezij samo vzdolž poštenih poti v drevesu izvajanj. Algoritmi za preverjanje modelov so implementirani kot del povsem domačega programskega paketa za obdelavo opisov digitalnih vezij s končnimi avtomati, predstavljenih z logičnimi funkcijami, ki temelji na prav tako povsem domačem paketu za obdelavo logičnih funkcij, predstavljenih z binarnimi odločitvenimi grafi.

1 Introduction

The manipulation of finite state machines (FSMs) is very common nowadays in the areas of digital circuit design like formal verification, automatic synthesis, and testing [12]. One of the main problems that must be solved is the verification of properties of FSMs representing digital circuits.

The properties are often specified by computation tree logic (CTL) because with a properly written CTL formula it can automatically be verified if certain property is valid in a FSM or not. Everything, CTL formulas, the set of states of the FSM, and its transition relation can be uniquely represented as Boolean functions, which can be very efficiently represented with binary decision diagrams (BDDs). Using symbolic state space traversal and model checking, we can avoid combinatorial explosion, which is one of the main problems with enumeration-based methods.

Unfortunately, it is impossible to specify all properties in CTL. A significant part of such properties are those that could be specified in CTL, but we want them to be verified only in a FSM constrained to normal (fair) paths in order to avoid singularities and similar things. The problem is solved by the introduction of fairness constraints, which constrain the FSM to fair paths, so that the properties can be verified in the usual way.

The purpose of this paper is to present the model checking algorithms which we implemented within fully home-made program package for manipulating finite state machine descriptions of digital circuits, represented with Boolean functions. The algorithms have performed very well.

In Section 2 we briefly review BDDs and show how to represent FSMs with them. Section 3 describes the methods of searching reachable states. The main part of the paper is Section 4 where we present algorithms for symbolic model checking in CTL. Algorithms for symbolic model checking using fairness constraints are described in Section 5. Experimental results for benchmark circuits are given in Section 6. We conclude with some discussion and plans for future work.

2 Preliminaries

Binary decision diagrams (BDDs) are compact canonical representations of Boolean functions [2]. Their size is closely related to the variable ordering. The manipulation of Boolean functions represented with BDDs is very efficient. Hence, BDDs have become widely used in various CAD applications, including state space traversal and model checking.

BDDs can also be used for representing and manipulating sets if we represent sets by means of their characteristic functions. If $\mathcal{A}$ is a subset of $\{0,1\}^n$, its characteristic function $\chi_{\mathcal{A}} : \{0,1\}^n \rightarrow \{0,1\}$ is defined by

$$\chi_{\mathcal{A}}(\underline{y}) = \begin{cases} 0; \underline{y} \notin \mathcal{A} \\ 1; \underline{y} \in \mathcal{A} \end{cases} \quad (1)$$

Thus, set operations can be performed by Boolean operations over the corresponding characteristic functions (e.g., $\chi_{\mathcal{A}^c} = \overline{\chi_{\mathcal{A}}}$, $\chi_{\mathcal{A} \cup \mathcal{B}} = \chi_{\mathcal{A}} + \chi_{\mathcal{B}}$, $\chi_{\mathcal{A} \cap \mathcal{B}} = \chi_{\mathcal{A}} \cdot \chi_{\mathcal{B}}$). For the sake of shorter notation we will denote $\chi_{\mathcal{A}}$ by A in the rest of the paper. Since the characteristic functions are Boolean, we can efficiently manipulate them with BDDs.

A deterministic *finite state machine* (FSM) M is a sixtuple $M = (\Sigma, \mathcal{S}, O, \delta, \lambda, s_0)$, where Σ is a finite set of input symbols, $\mathcal{S}$ a finite set of states, O a finite set of output symbols, $\delta : \mathcal{S} \times \Sigma \rightarrow \mathcal{S}$ a state transition function, $\lambda : \mathcal{S} \times \Sigma \rightarrow O$ an output function, and $s_0 \in \mathcal{S}$ an initial state.

If we want to realize a FSM by a digital circuit, we will have to encode the sets $\mathcal{S}$, Σ, and O by binary symbols (e.g., 0 and 1). States are encoded by state variables. At least $n = \lceil \log_2 |\mathcal{S}| \rceil$ state variables, $m = \lceil \log_2 |\Sigma| \rceil$ input variables, and $l = \lceil \log_2 |O| \rceil$ output variables of the circuit are needed. Let $\mathcal{Y}$, $\mathcal{X}$, and $\mathcal{Z}$ represent the set of state variables, the set of input variables, and the set of output variables, respectively.

Once the states and the input symbols of the circuit are encoded, we denote a state transition function as $\delta : \{0,1\}^n \times \{0,1\}^m \rightarrow \{0,1\}^n$. Then, next state variables are functions of present state variables and input variables. We denote next state variables by an added prime (') and write a transition function of a state variable y_i as

$$y_i' = \delta_i(y_0, y_1, \ldots, y_{n-1}, x_0, x_1, \ldots, x_{m-1}) \quad (2)$$

for $i = 0,1,\ldots,n-1$. We rather introduce transition relations

$$T_i = y_i' \Leftrightarrow \delta_i(y_0, y_1, \ldots, y_{n-1}, x_0, x_1, \ldots, x_{m-1}) \quad (3)$$

Namely, relations have much greater expressive power than functions [3]. With relations it is very easy to handle nondeterminism and to perform backward reachability search that is relatively difficult with functions. Transition relations T_i can be combined by taking their conjunction to form the *monolithic transition relation* $T = T_0 \cdot T_1 \cdot \ldots \cdot T_{n-1}$.

3 Searching Reachable States of FSM

First, let us show how we search reachable states of a FSM. Let $\mathcal{S}_i$ denote a set of states reachable in at most i steps. $\mathcal{S}_0$ represents a set of initial states. In our case we have $\mathcal{S}_0 = \{s_0\}$. A set of states reachable in at most one step is given by

$$\mathcal{S}_1 = \mathcal{S}_0 \cup \{s' \mid \exists a \exists s [a \in \Sigma \wedge s \in \mathcal{S}_0 \wedge \delta(s,a) = s']\} \quad (4)$$

After finding states reachable in at most one step we search for those reachable in at most two steps. In general, a set of states reachable in at most i steps is represented by

$$\mathcal{S}_i = \mathcal{S}_{i-1} \cup \{s' \mid \exists a \exists s [a \in \Sigma \wedge s \in \mathcal{S}_{i-1} \wedge \delta(s,a) = s']\} \quad (5)$$

We continue with this procedure until in a step k no new state is reached. In any case, this happens sooner or later, because we deal with FSMs, where the set of states $\mathcal{S}$ is finite. Then, $\mathcal{S}_k = \mathcal{S}_{k-1}$ is a set of all reachable states.

Introducing the characteristic functions for the sets (e.g., the $\mathcal{S}_i$ is represented by its characteristic function $S_i = \chi_{\mathcal{S}_i}$), we can rewrite (5) into the following logical expression:

$$S_i' = S_{i-1}' + \exists_{y \in \mathcal{Y} \cup \mathcal{X}} (S_{i-1} \cdot T) \quad (6)$$

The function S_i' depends on next state variables y_j'. To obtain S_i we have to replace each y_j' with the corresponding y_j. Therewith, next states are considered to be new present states for the next step. The procedure terminates in a step k, when $S_k = S_{k-1}$.

The most time and space consuming operation in (6) is the computation of $\exists_{y \in \mathcal{Y} \cup \mathcal{X}} (S_{i-1} \cdot T)$. The source of problems is usually very large monolithic transition relation T. In order to avoid this problem, we do not build a single BDD for the whole transition

relation T, but rather partition T in some groups of transition relations of individual state variables and represent each group by a smaller BDD. T is then called a *partitioned transition relation* [3][9][5].

Formula (6) can be written in an extended form as

$$S_i' = S_{i-1}' + \exists x_0 \exists x_1 \ldots \exists x_{m-1} \exists y_0 \exists y_1 \ldots \ldots \exists y_{n-1} \left(S_{i-1} \cdot T_0 \cdot T_1 \cdot \ldots \cdot T_{n-1}\right) \quad (7)$$

Although existential quantification does not distribute over conjunction, conjuncts can be moved out of the scope of an existential quantification if they do not depend on any of the variables being quantified. FSMs that represent circuit behaviour exhibit locality, so it is very common that many of the T_j depend on only small number of the input and state variables.

We developed a heuristic algorithm for the partitioning and reordering of functions and variables for existential quantification in (7) that allows us to apply some existential quantifiers before the BDD for the whole transition relation has been built. The function S_{i-1} in (7) represents a set of present states in step $i-1$. Therefore, it may depend on all state variables y_i. So we leave it within the scope of all existential quantifiers of state variables y_j. In contrast to the function S_{i-1}, functions T_j are constant throughout the computation and at the beginning we can determine their place with respect to the existential quantifiers in (7) once and for all.

The dependencies of functions T_j on individual input and state variables are represented by matrix

$$\mathbf{A} = \begin{bmatrix} a_{0,0} & \cdots & a_{0,n-1} \\ \vdots & \ddots & \vdots \\ a_{n-1,0} & \cdots & a_{n-1,n-1} \\ a_{n,0} & \cdots & a_{n,n-1} \\ \vdots & \ddots & \vdots \\ a_{n+m-1,0} & \cdots & a_{n+m-1,n-1} \end{bmatrix} \begin{matrix} \leftarrow & y_0 \\ \vdots & \vdots \\ \leftarrow & y_{n-1} \\ \leftarrow & x_0 \\ \vdots & \vdots \\ \leftarrow & x_{m-1} \end{matrix}$$
$$\begin{matrix} \uparrow & \ldots & \uparrow \\ T_0 & \ldots & T_{n-1} \end{matrix}$$

which is of size $(m+n) \times n$ and $a_{i,j}$ has value 1 if and only if the function T_j depends on the variable that points to row i from the right side, and value 0 otherwise. First, we fill the matrix with 0s and 1s. Then we choose one of the rows (there might be several) with minimal number of 1s and thus one of the variables that the least number of the functions depend on. We put into the scope of its existential quantifier all the functions that depend on this variable. We will be no more concerned with these functions during the partitioning procedure. Therefore, the selected row and all the columns whose functions were taken are no more needed and we delete them. The whole procedure is then repeated over the reduced matrix as long as we do not run out of functions and variables.

A group of functions which find themselves together in one step of this procedure is called a *block*. We denote it T_{ρ_i} if we got it in the i-th step and ρ_i represents the i-th block of partition ρ over the set $\{0,1,\ldots,n-1\}$. Accordingly, the block T_{ρ_i} can be written as $T_{\rho_i} = \bigwedge_{j \in \rho_i} T_j$. Let us denote a set of variables whose existential quantifiers are immediately in front of block T_{ρ_i} by $\mathcal{Y}_{\rho_i}$, where

$$\mathcal{Y}_{\rho_i} = \{v \mid \; v \in \mathcal{Y} \cup \mathcal{X} \wedge \forall j \in \rho_i : T_j \text{ depends on } v \wedge \forall j \notin \rho_i : T_j \text{ does not depend on } v\} \quad (8)$$

Thus, using partitioned transition relation we got the following formula for a general step in computing reachable states:

$$S_i' = S_{i-1}' + \exists_{y \in \mathcal{Y}_{\rho_{k-1}}} \left(T_{\rho_{k-1}} \cdot \exists_{y \in \mathcal{Y}_{\rho_{k-2}}} \left(T_{\rho_{k-2}} \cdot \ldots \cdot \exists_{y \in \mathcal{Y}_{\rho_0}} \left(T_{\rho_0} \cdot S_{i-1}\right) \ldots \right)\right) \quad (9)$$

The algorithm based on (9) has proved itself very well. Just in few cases it was considerably worse (see the example of an up/down counter in Section 6) than the method with monolithic transition relation. However, in many cases it has been shown to be better for many orders of magnitude.

4 Symbolic Model Checking

The logic that we use to specify properties of FSMs is a propositional termporal logic of branching time, called *Computation Tree Logic* — CTL [4]. In this logic each of the usual future time operators of linear temporal logic ($\mathbf{G}$ — *globally* or *invariantly*, $\mathbf{F}$ — *sometimes in the future*, $\mathbf{X}$ — *next time*, $\mathbf{U}$ — *until*) must be immediately preceded by *path quantifier* $\mathbf{A}$ (for all computation paths) or $\mathbf{E}$ (for some computational path). We thus obtain eight different CTL operators: $\mathbf{AG}$, $\mathbf{EG}$, $\mathbf{AF}$, $\mathbf{EF}$, $\mathbf{AX}$, $\mathbf{EX}$, $\mathbf{AU}$, $\mathbf{EU}$.

CTL formulas are constructed from *atomic propositions* using Boolean connectives and CTL opera-

tors. In our case of verifying FSMs, the set of atomic propositions is equal to the set $\mathcal{Y}$ of state variables of the circuit. If y_j is an atomic proposition in $\mathcal{Y}$, the formula y_j is true in a state s (we say that s satisfies y_j and write $s \models y_j$ if and only if the state variable y_j is true in this state.

The formula $\mathbf{AG}\, f$, for example, will hold in a state provided that f holds in all states along all possible computation paths starting from that state, and $\mathbf{EF}\, f$ will hold in a state provided that there is a computation path from that state to the future state where f holds [1][9][5]. The meaning of all CTL operators is shown in Figure 1 in the form of computation trees. In the figure, full circle represents a state where formula f is true. In states that are represented by full square, formula g is true. We know nothing about the truthfulness of formulas in all other states (empty circles).

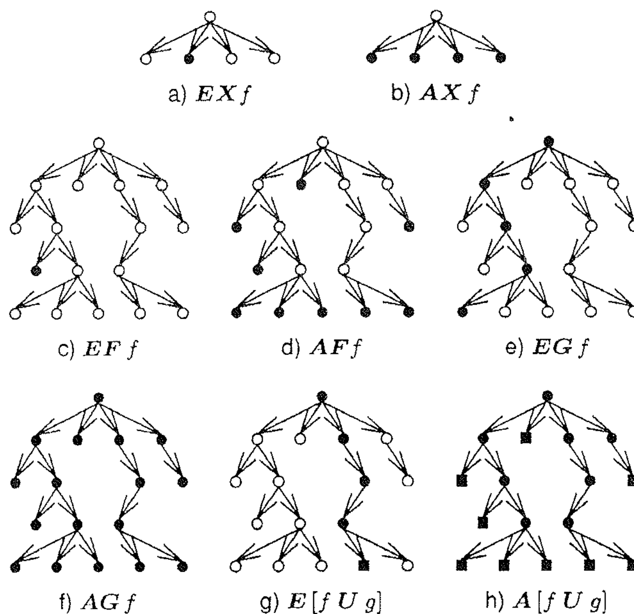

Figure 1: Meaning of CTL operators

Model checking is the problem of determining whether a given CTL formula f is true in a given FSM M. The formula f is true in the FSM M if and only if f is true in all initial states of M. We can say that FSM M is a *model* of f ($M \models f$).

In this section, we present an efficient symbolic model checking algorithm for CTL that recurses over the structure of a given CTL formula f and determines in a bottom up fashion in which states of the model the subformulas of f are true. Finally, it returns the BDD (the function) S that represents exactly the set of states $\mathcal{S}$ of the FSM in which f is true and checks whether $\mathcal{S}_0 \subseteq \mathcal{S}$.

The CTL formulas constructed only from the atomic propositions (state variables) and ordinary Boolean connectives are handled using standard algorithms for computing Boolean connectives with BDDs. The temporal formulas are treated otherwise. Although there are eight different CTL operators, it is sufficient to realize only three of them, since the remaining five can be easily expressed with the three realized. We decided to realize the operators $\mathbf{EX}$, $\mathbf{EU}$, and $\mathbf{EG}$ [7][1].

First, let us have a look at the formula $\mathbf{EX}\, f$, where f represents a characteristic function $S_f = f$ of the set of states $\mathcal{S}_f$ where it is true. Formula $\mathbf{EX}\, f$ is true in all predecessors of states in $\mathcal{S}_f$. The characteristic function of these states is computed by

$$\mathbf{EX}\, f = \exists_{y' \in \mathcal{Y}' \cup X} (f' \cdot T) \tag{10}$$

where f' represents the function f with each state variable y_i substituted by the corresponding next state variable y_i' and T is a transition relation of a given FSM. The relational product (10) is quite similar to the relational product (6) defined in Section 3 except that in (10) we compute one step in a backward reachability search instead of a forward reachability search.

Formula $\mathbf{E}[f\, \mathbf{U}\, g]$ means that either g is true in the current state, or f is true in the current state and there exists a successor state where $\mathbf{E}[f\, \mathbf{U}\, g]$ is true. Consequently, the BDD that represents the states where $\mathbf{E}[f\, \mathbf{U}\, g]$ is true can be computed by finding the least fixed point of the predicate transformer F defined by

$$F(S) = g + f \cdot \mathbf{EX}\, S \tag{11}$$

Formula $\mathbf{EG}\, f$ means that f is true in the current state and there exists a successor state where $\mathbf{EG}\, f$ is true. The BDD that represents the states where $\mathbf{EG}\, f$ is true is computed as the greatest fixed point of the predicate transformer

$$F(S) = f \cdot \mathbf{EX}\, S \tag{12}$$

After determining the set $\mathcal{S}$ of states that satisfy a given CTL formula f, the algorithm checks

whether this set includes all initial states $\mathcal{S}_0$ ($\mathcal{S}_0 \subseteq \mathcal{S}$). Checking the condition $\mathcal{S}_0 \subseteq \mathcal{S}$ is easy in our BDD-based algorithm. It has to be checked whether the Boolean expression $\overline{S_0} + S \Leftrightarrow 1$ is a tautology.

5 Fairness Constraints

Many times we want to check if a given property is true in a given FSM only along the *fair paths* in a computation tree. For example, at checking of a bus arbiter we might be interested only in those paths where none of the devices which the bus was granted to holds the bus to the eternity.[1]

Such properties can not be expressed directly by CTL. To solve the problem, the meaning of CTL should be changed. Therefore, we introduce *fairness constraints*, which are ordinary CTL formulas. A path in the computation tree is *fair* regarding to a set of fairness constraints if every constraint is true *infinitely often* along the path. Path quantifiers in CTL formulas are then constrained to these fair paths [8].

Let the set of CTL formulas $\mathcal{H} = \{h_1, h_2, \ldots, h_r\}$ be fairness constraints. Let us have a look at solving formula $\mathbf{EG}\, f$ with fairness constraints $\mathcal{H}$ (we write $\mathbf{EG}_{\text{fair}}\, f$). Formula f is again characteristic function of set of states where formula f is true, just like with ordinary CTL formulas. Formula $\mathbf{EG}_{\text{fair}}\, f$ says that there exists a path in the computation tree, where f is invariantly true and every formula in $\mathcal{H}$ is true infinitely often. The set of such states $\mathcal{S}$ is the largest of the sets for which the following two properties are true:

- f is true in every state from $\mathcal{S}$ and
- for every fairness constraint $h_k \in \mathcal{H}$ and every state $s \in \mathcal{S}$, there exists a path of length one or more from state s to some state in $\mathcal{S}$, where constraint h_k is true and f is true in every state along that path.

It could be proved that every state in the set $\mathcal{S}$ is the beginning of an infinite path in the computation tree, where formula f is always true and every constraint in $\mathcal{H}$ is true infinitely often. By searching for the greatest fixed point of the predicate transformer

$$F(S) = f \cdot \prod_{k=1}^{r} \mathbf{EX}\, \mathbf{E}[f\, \mathbf{U}\, S \cdot h_k] \qquad (13)$$

where CTL operators $\mathbf{EX}$ and $\mathbf{EU}$ are resolved as ordinary CTL operators without considering the fairness constraints, we get a characteristic function of the set of states where formula $\mathbf{EG}_{\text{fair}}\, f$ is true considering the fairness constraints. The fixed point is evaluated in the same manner as without fairness constraints, but note that each computation of the above expression leads to several nested fixed point computations (resolving of operators $\mathbf{EU}$).

Resolving of operators $\mathbf{EX}$ and $\mathbf{EU}$ with fairness constraints is simpler. Characteristic function of the set of states that can be starting states of fair paths in the computation tree is defined as

$$S_{\text{fair}} = \mathbf{EG}_{\text{fair}}\, 1 \qquad (14)$$

There exists a path from every state in this set along which every fairness constraint in $\mathcal{H}$ is true infinitely often. Formula $\mathbf{EX}_{\text{fair}}\, f$ is true in state s if and only if there exists a successor state s' of s such that f is true in s' and s' is the beginning of a fair path. Therefore, the formula $\mathbf{EX}_{\text{fair}}\, f$ considering only fair paths is equal to the formula $\mathbf{EX}\,(f \cdot S_{\text{fair}})$ over all paths. Thus, let us define

$$\mathbf{EX}_{\text{fair}}\, f = \mathbf{EX}\,(f \cdot S_{\text{fair}}) \qquad (15)$$

This way we transform the problem from dealing with fair paths to considering all paths in the computation tree, and that is something what we already know how to handle with.

Following analogy the formula $\mathbf{E}[f\, \mathbf{U}\, g]_{\text{fair}}$ is equal to the formula $\mathbf{E}[f\, \mathbf{U}\, g \cdot S_{\text{fair}}]$ considering all computation paths. Therefore, we define

$$\mathbf{E}[f\, \mathbf{U}\, g]_{\text{fair}} = \mathbf{E}[f\, \mathbf{U}\, g \cdot S_{\text{fair}}] \qquad (16)$$

and once again the problem is transformed into something we already know how to solve.

5.1 Example

To illustrate symbolic CTL model checking using fairness constraints we took a parametric bus arbiter with n devices (n is parameter) which grants a bus to the device with the highest priority [11]. An instance of such an arbiter for $n = 3$ is shown in Figure 2. All others are constructed in a similar way. Devices with lower number have higher priority.

We want to know if formulas

$$\mathbf{EF}\,\mathbf{EG}\left(IN_i \cdot \overline{OUT_i}\right) \qquad (17)$$

[1] This example shows us, where the name of fair paths comes from. It would be unfair from a device if it held the bus to the eternity and had never released the bus and left it to other devices. By excluding such paths in some way we stay only at fair paths.

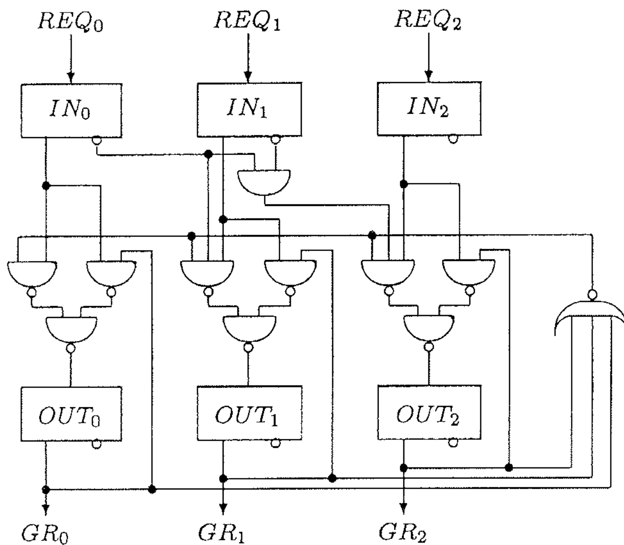

Figure 2: A 3-request bus arbiter

are true, in other words, if there exists a path from the initial state, where at some point device i $(i=0,1,\ldots,n-1)$ would request a bus and bus would never be granted to it. In general case without any fairness constraints the formulas are true, because every other device could hold the bus for itself and never release it again.

Because such behaviour could be described as unfair, we will try to constrain all possible paths to those where the bus is free infinitely often along the path. This is written by fairness constraint

$$\overline{OUT_0+OUT_1+\ldots+OUT_{n-1}} \qquad (18)$$

in the formal language. It could be shown that formula $\mathbf{EF}\,\mathbf{EG}\left(IN_0\cdot\overline{OUT_0}\right)$ is not true any more. If the device 0 requests a bus and it insists on that request, the bus will be eventually granted to it. All other formulas are still true, because every other device might request the bus, but the bus would never be granted to it. Actually, this is the expected behaviour, since fairness constraint (18) has eliminated only those paths where some device would hold the bus to the eternity. Because nothing stops a device to request a bus again immediately after device has released it, there is a possibility that the bus is always granted to device 0 as device with the highest priority. In that case the bus will never be granted to any other device.

The next level of fairness is achieved by preventing the device 0 such aggressive behaviour in spite of its highest priority. It should be required that infinitely often, after the bus is released, it is not granted to device 0. That is, infinitely often along the path we must reach a state where the bus is released (fairness constraint (18) is true) and in all possible successor states the bus is not granted to device 0. Therefore, formula $\mathbf{AX}\,\overline{OUT_0}$ will be true in that state, too. This leads us to new fairness constraint

$$\overline{OUT_0+OUT_1+\ldots+OUT_{n-1}}\cdot\mathbf{AX}\,\overline{OUT_0} \qquad (19)$$

Beside the formula for device 0, now also formula $\mathbf{EF}\,\mathbf{EG}\left(IN_1\cdot\overline{OUT_1}\right)$ for device 1 is false. Since devices 0 and 1 can interchange in possessing the bus, all other devices can stay without the bus forever. So, other formulas are still true.

To prevent interchanging of the bus holding between two most prioritised devices, the fairness constraint should be extended. Infinitely many times it should happen that after the bus was released it is neither granted to the device 0 *nor* to the device 1. So, we get fairness constraint

$$\overline{OUT_0+OUT_1+\ldots+OUT_{n-1}}\cdot\mathbf{AX}\,\overline{OUT_0+OUT_1} \qquad (20)$$

Now device 2 also gets its time slots where the bus is granted to it. Its CTL formula is now also false, but all others for $i>2$ are still true.

In the same manner we could proceed, what leads us to fairness constraint

$$\overline{OUT_0+OUT_1+\ldots+OUT_{n-1}}\cdot\mathbf{AX}\,\overline{OUT_0+OUT_1+\ldots+OUT_{k-1}} \quad \text{for } 0<k<n \qquad (21)$$

where all CTL formulas from (17) with index $i\le k$ are false, while all others are true.[2]

If a device i, $i=0,1,\ldots,k$, requests the bus and it insists on that request, the bus will eventually be granted to it. All other devices could stay without the bus to the eternity.

Well, if $n-1$ is chosen for k, we get as fair system as a priority system could be. Not only that none of the devices may hold the bus forever, but also the bus will be granted to each and every device from time to time.

6 Experimental results

Experiments were done on a *Sun Ultra 30 creator* workstation with 300 MHz UltraSPARC II processor, 256 MB of physical memory and 793 MB of virtual memory under *Solaris 2.5.1* operating system. We have used our own BDD package ([6]) that is an efficient *ite*-based implementation of reduced ordered binary decision diagrams with complemented edges.

[2] If $k=0$, formula (21) becomes formula (18).

Table 1: Computing reachable states for ISCAS'89 circuits and a parametric up/down counter

circuit	# states	# steps	monolithic TR		partitioned TR	
			# nodes	time	# nodes	time
s344	2625	7	11966	0.13	19462	0.19
s349	2625	7	11966	0.14	19462	0.20
s382	8865	151	48580	1.98	46411	0.86
s420.1	65536	65535	278572	7.67	282476	35.86
s444	8865	151	13660	0.14	20863	0.22
s526	8868	151	19610	0.18	36560	0.36
s526n	8868	151	19608	0.18	36558	0.36
s641	1544	7	1299567	170.27	23649	0.36
s713	1544	7	1299622	173.09	23673	0.37
s953	504	11	37187	0.32	11987	0.16
s1196	2616	3	236067	29.87	28788	0.42
s1238	2616	3	236086	29.86	28810	0.40
count3	8	4	66	0.00	56	0.00
count6	64	32	598	0.00	1005	0.00
count9	512	256	3922	0.04	11111	0.11
count12	4096	2048	28558	0.42	44905	1.31
count15	32768	16384	85708	4.32	88920	13.91
count18	262144	131072	427938	36.78	433475	141.48
count21	2097152	1048576	3180807	414.54	3185888	1773.71

Table 1 shows the results obtained by symbolic searching of reachable states on some ISCAS'89 circuits and on the parametric up/down counters. From left to right the columns in Table 1 refer to the circuit name, the number of reachable states, the number of steps needed to compute all reachable states, and the maximal number of BDD nodes whenever generated during the symbolic state space traversal of a given circuit together with the CPU time in seconds both for the search using monolithic transition relation and partitioned transition relation.

Great power of the symbolic state space traversal is demonstrated in the next example. Table 2 shows results on computing reachable states for the previously described parametric arbiter using partitioned transition relation. Although the number of reachable states grows with n extremely fast, the number of BDD nodes and CPU time grow much slower.

Table 2: Computing reachable states for a parametric arbiter

# dev. n	# state variab.	# reachable states	# steps	# BDD nodes	time [s]
100	200	$1.28032710 \cdot 10^{32}$	3	66443	2.39
200	400	$3.22994546 \cdot 10^{62}$	3	203180	13.52
300	600	$6.13147828 \cdot 10^{92}$	3	454743	37.60
400	800	$1.03548220 \cdot 10^{123}$	3	806369	80.66
500	1000	$1.63996869 \cdot 10^{153}$	3	1257932	148.41
600	1200	$2.49385885 \cdot 10^{183}$	3	1809558	246.24
700	1400	$3.68735526 \cdot 10^{213}$	3	2461121	386.41
800	1600	$5.34107956 \cdot 10^{243}$	3	3212747	570.30
900	1800	$7.61589396 \cdot 10^{273}$	3	4064373	809.61
1000	2000	$1.07258011 \cdot 10^{304}$	3	5015936	1100.22

We verified the behavior of the parametric arbiter with symbolic model checking in CTL. The properties being verified together with the corresponding CTL formulas are as follows:

- *Exclusivity.* At most one output is set to '1'. In order to decrease the complexity of the CTL formula we weaken the exclusivity and rather write (as in [11]) that either odd number of outputs is set to '1' or all outputs are set to '0'.

$$\mathbf{AG}\left(\left(OUT_0 \oplus OUT_1 \oplus \ldots \oplus OUT_{n-1}\right) + \overline{OUT_0} \cdot \overline{OUT_1} \cdot \ldots \cdot \overline{OUT_{n-1}}\right)$$

- *Causality.* If device i $(i = 0,1,\ldots,n-1)$ requests the bus, the access will eventually be granted to device i.

$$\mathbf{AG}\left(IN_i \Rightarrow \mathbf{EF}\, OUT_i\right)$$

- *Starvation.* There is a possibility that a request from device i is never serviced. This behavior will happen if another device being granted the bus never releases its request.

$$\mathbf{EG}\left(IN_i \Rightarrow \mathbf{EG}\, \overline{OUT_i}\right)$$

- Allocation. If a request from device i $(i = 0,1,\ldots,n-1)$ is loaded and no higher priority device requests the bus, then the bus is granted to device i at the next state.

$$\mathbf{AG}\left(\overline{OUT_0} \cdot \ldots \cdot \overline{OUT_{n-1}} \cdot IN_0 \Rightarrow \mathbf{AX}\, OUT_0\right)$$
$$\mathbf{AG}\left(\overline{OUT_0} \cdot \ldots \cdot \overline{OUT_{n-1}} \cdot \overline{IN_0} \cdot IN_1 \Rightarrow \mathbf{AX}\, OUT_1\right)$$
$$\vdots$$
$$\mathbf{AG}\left(\overline{OUT_0} \cdot \ldots \cdot \overline{OUT_{n-1}} \cdot \overline{IN_0} \cdot \ldots \cdot \overline{IN_{n-2}} \cdot IN_{n-1} \Rightarrow \mathbf{AX}\, OUT_{n-1}\right)$$

In Table 3 we collected the results obtained from the verification of the parametric bus arbiter.[3] The columns from left to right represent the number of devices (n), the number of state variables (latches) of the circuit (n), the number of CTL formulas being verified for each n $(3n+1)$, and the maximal number of BDD nodes whenever generated during symbolic model checking of a given circuit together with the CPU time in seconds both for the model checking using monolithic transition relation and partitioned transition relation. An overflow on BDD nodes is denoted by a dash '—'.

We did not perform a lot of experiments with fairness constraints. Well, checking of CTL formulas (17) for $n = 4$ with fairness constraint (21) for $k = 3$ took less than $\frac{1}{100}$ of a second.

7 Conclusions

We reviewed two different algorithms for searching of reachable states in FSMs, using either monolithic transition relation or partitioned transition relation. The introduction of partitioned transition relation may decrease the CPU times for large circuits dra-

[3] Although an arbiter with $n = 1$ is a totally senseless circuit, it is included in Table 3 for the sake of completeness. Anyway, a model checking algorithm does not care whether it handles useful or senseless circuits.

Table 3: Checking of parametric arbiter in CTL

# dev. n	# state var.	# CTL form.	monolithic TR # BDD nodes	monolithic TR time [s]	partitioned TR # BDD nodes	partitioned TR time [s]
1	2	4	18	0.00	11	0.00
2	4	7	174	0.00	76	0.00
3	6	10	947	0.01	298	0.01
4	8	13	4403	0.10	929	0.01
5	10	16	19171	0.64	2299	0.01
6	12	19	78044	4.63	7540	0.11
7	14	22	297614	38.37	15095	0.23
8	16	25	1214392	291.79	40247	0.98
9	18	28	4912359	2019.25	40301	1.77
10	20	31	—	—	100861	9.09
11	22	34	—	—	136629	15.55
12	24	37	—	—	616346	100.33
13	26	40	—	—	745319	184.85
14	28	43	—	—	3827900	1534.16
15	30	46	—	—	4303558	3603.01

matically. Then, we showed methods for verifying synchronous sequential circuits by symbolic model checking [7][9]. Properties to be verified were expressed in CTL.

We illustrated the usage of fairness constraints by verifying a parametric bus arbiter which selects the highest priority device from n devices. We checked if it is possible that some device requests a bus and the bus is never granted to it regarding different fairness constraints.

All algorithms are realized as part of a home-made package for manipulating FSMs which is also based on a fully home-made very efficient package for manipulating Boolean functions represented by BDDs [10].

Our future work will consist in the implementation of searching for counterexamples for false properties and then of automatic generation of testing sequences for digital circuits based on found counterexamples.

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ADAPTIVE CURRENT MEASURING CIRCUIT FOR ELECTRIC POWER METERS

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Keywords: physics, electrotechnics, electric power measurement, electric power meters, measuring circuits, Hall sensors, Hall generators, electric current sensors, accuracy classes, measuring ranges, dynamic ranges, accuracy assurance

Abstract: This article presents the current measuring circuit for usage in power meters. The circuit provides a measurement class in a dynamic range over 120 dB with the use of the standard analog-to-digital and digital-to-analog devices. This large dynamic range is achieved with the appropriate setting of the excitation current of the Hall sensor. Experimental results show that the proposed measuring circuit exceeds the requirements for accuracy and the dynamics that are defined by the IEC687 standard.

Adaptiven tokovni merilnik za števce električne moči

Ključne besede: fizika, elektrotehnika, merjenje moči električne, merilniki moči električne, vezja merilna, Hall senzorji, Hall generatorji, senzorji toka električnega, razredi točnosti, območja merilna, območja dinamična, zagotavljanje točnosti

Povzetek: V članku je predstavljen tokovni merilnik za uporabo v števcih električne enrgije. Merilnik zagotavlja merilni razred v dinamičnem obsegu več kot 120 dB z uporabo standardnih analogno-digitalnih pretvornikov. Tako veliko dinamiko dosega z primerno nastavitvijo vzbujalnega toka Hall-ovega senzorja. Eksperimentalni rezultati kažejo, da predlagan merilnik presega zahteve po natančnosti in dinamiki, podane v standardu IEC687.

1 Introduction

Besides the accuracy in the dynamic range over 100 dB, modern power meters are also expected to measure the power in harmonic components. Only digital instruments can manage this. In the measurement of the flow of energy through the network, the change in the voltage amplitude is relatively small. The specified working range for an instrument in the class 0.2, defined by the standard IEC687, is 10% of the reference voltage, but the changes in the current are larger. According to the standard IEC687, an instrument in the class 0.2 must measure power for currents from 0.1% of the nominal current to 120%. Digital instruments for this amplitude range must have at least 20 bits of AD conversion to achieve the measurement range and to provide the declared class of the instrument for the whole measurement range. In that case, the dynamic of the AD converter is 120.4 dB. Because the high resolution AD converters that work on the sigma-delta principle usually have a SNR relation worse than its dynamic, it is necessary to take AD converters with a higher bit resolution. Again, they do not have such attractive prices and the instruments can not be competitive on the market. The natural solution to this problem is the introduction of current sensors with changeable sensitivity. This can be achieved in two ways:

- with the use of fast PGA circuits, for which the gain is based on the measurement strategy,
- with the use of Hall sensors, for which the gain is set according to the excitation current.

In this article the new adaptive current measuring circuit for electric power meters with a Hall sensor is described. Its gain is set according to the amplitude of the measured current to ensure the accuracy class of the measuring circuit. The circuit measures currents of all shapes in a wide measurement range. The setting is formed digitally in the back-loop of the measuring range regulator. That way the measuring circuit reduces the dynamic of the measured values and achieves the ordered accuracy with fewer bits of the AD converter. It is useful in measuring electric power and energy, and in all measuring instruments which measure the electric current with ordered accuracy in a wide measuring range and galvanic separation of the measuring circuit from the measuring current.

The article is divided into five chapters. The introduction is in the first chapter, the summary on the power measuring circuit and Hall sensors follows in the second chapter, and the third chapter describes the measuring circuit. The results of testing the measuring circuit prototype are shown in chapter four and the conclusion is in chapter five.

2 Measurement of electric power and use of the Hall sensors

Electric power meters use current transformers, shunt resistors or Hall sensors to measure current. Because of its many beneficial properties, the use of the Hall sensors is very wide-ranging. The electric power meter MT300 from the manufacturer Iskra Emeco is very similar. The measuring circuit contains a Hall sensor integrated with the circuit for power calculation into the monolithic circuit; that way, better resistance to the climatic influence is achieved. The measuring circuit meets the international recommendation IEC1036 for class 1 and 2 of the electric power meters. The accuracy of the electric power measuring circuit also depends on the frequencies of the voltage and current. Thus the standard IEC1036 defines the standard reference frequency of the voltage, current and the permitted deviation of 5%, within which the measuring circuit must meet

the demands for accuracy. In definite cases, electric power must be measured in a wider frequency band and with larger dynamics (from 3mW to the 1.5kW) [1,2]. Those demands are fulfilled most easily by the use of the Hall sensors [3].

3 Current measuring circuit with Hall sensor

New technology makes it possible to build adaptive current measuring circuits, which are capable of accommodating the measuring range for the flow of the measured signal. From that the amplitude dynamic is enlarged. In [4] is described the solution of the adaptive measuring circuit that uses the model of the measured system to predict the input of the sensor from the known input of the measured system. Calculation of the model requires high calculating power, therefore an efficient digital signal processor is required. A simpler solution is to change the gain of the sensor by setting the excitation current (some measuring circuits for electric power measurement use this current to directly measure power). In [4] the use of the excitation current for this purpose is omitted because of the increased influence of the noise in smaller gains. However, the new technology of the Hall sensors makes it possible to reduce the influence of the noise and offset voltage [5,6] so that this solution is promising again.

3.1 How the Hall sensor works

The principle of how the Hall sensor works is generally known, therefore the only properties that are summarized are those that are used in the proposed measuring circuit.

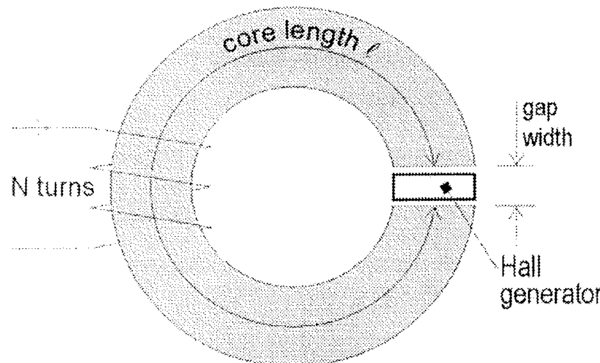


Fig. 1: Principle of current measurement using the Hall sensor

It is a known fact that around the current conductor the magnetic field is formed. If the magnetic field is concentrated in the magnetic core, then the Hall sensor can be put into the core gap, as shown in the Fig. 1.

Voltage on the output connection of the Hall sensor is defined by (1),

$$U(I_m, I_v) = k_h \cdot I_v \cdot I_m \qquad (1)$$

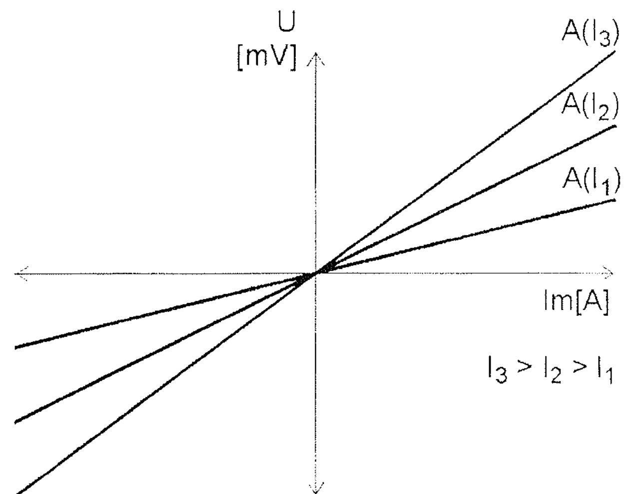
where I_m is the measured current, I_v is the excitation current and k_h is the constant. The factor $k_h\, I_v$ can be used as the changeable gain of the sensor, (2) and (3):

$$A(I_v) = k_h \cdot I_v \qquad (2)$$

and

$$U(I_m, I_v) = A(I_v) \cdot I_m \qquad (3)$$

$A(I_v)$ is the slope of the straight line on which the output voltage of the Hall sensor moves in relation to the measured current I_m. That is the basis of the how the proposed current sensor works. The value of the measured current I_m is determined by the division of the Hall sensor output voltage with the chosen gain. Statical characteristics of the Hall sensor voltage U in relation to the gain $A(I_v)$ and dependence of the gain $A(I_v)$ on the excitation current I_v are shown in the Fig.2. Fig.2 illustrates the ideal course of the characteristics. In the real Hall sensor, the offset voltage must be considered. The offset voltage depends on the sensor temperature and the amplitude of the excitation current.



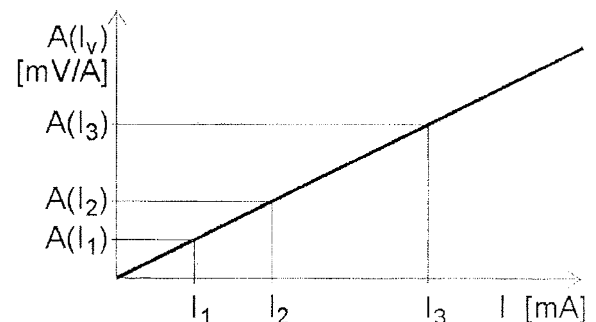


Fig. 2: Static characteristics of the Hall

3.2 Design of the measuring circuit

The project block scheme of the proposed measuring circuit is shown in Fig. 3.

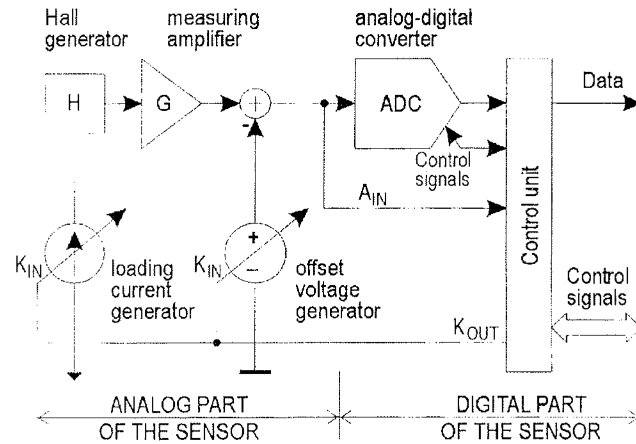


Fig. 3: Block scheme of the adaptive current measuring circuit with the Hall sensor

The temperature compensated current generator, driven by the voltage, excites the Hall sensor. Using the current, the gain of the Hall sensor is set. The output of the Hall sensor is connected to the measuring amplifier, and the offset voltage is subtracted from the amplifier. The resulting signal is then converted with an AD converter. The measured data is then corrected in the control unit to remove the influence of the changeable gain of the Hall sensor. Therefore the measured data is multiplied by the gain of the Hall sensor. If the gain is set in steps by a factor of 2^n, then the multiplication is simplified into a simple bit shift of the measuring result by *n* bits in the direction of the most significant bit. That way the building of the control unit is simplified a lot and is suitable for integration into the programmable unit. The control unit also takes care of settings of the Hall sensor's gain with appended hysteresis, so that uncontrollable switching between the measuring ranges is prevented. The resulting static characteristics are shown in Fig. 4.

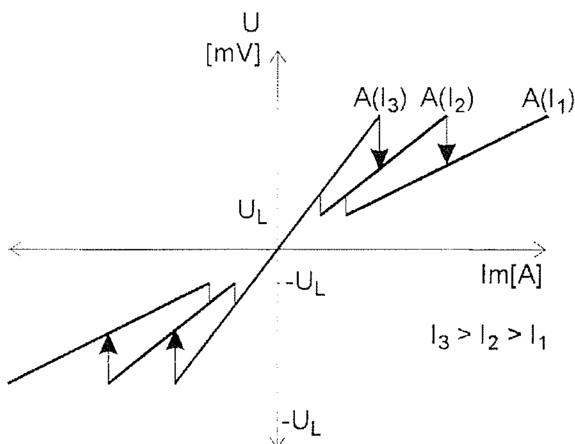


Fig. 4: Results of the static characteristics of the adaptive current measuring circuit with the Hall sensor

4 Measurements and testing

Measurements were made on the analog part of the sensor, as shown in Fig. 5.

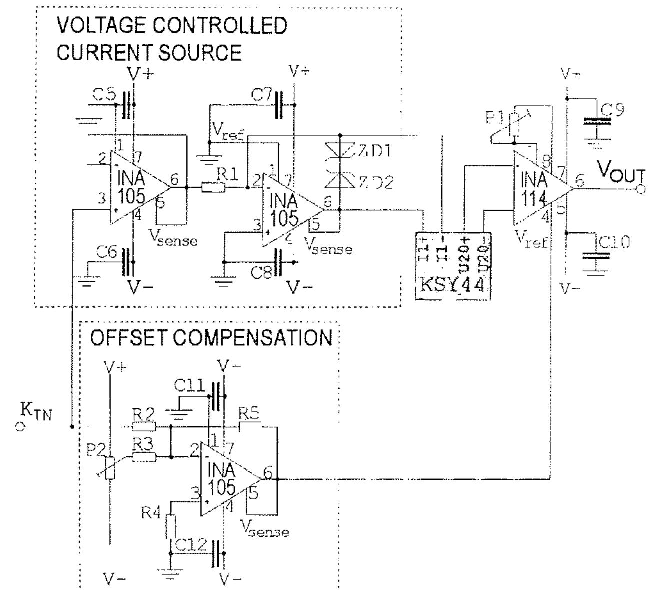


Fig. 5: Analog part of the sensor

The Siemens KSY44 Hall sensor was used. In Fig. 6 the static characteristics of the differential Hall voltages for different gains of the Hall sensor are shown. The gain was set for excitation currents from 4 to 9 mA.

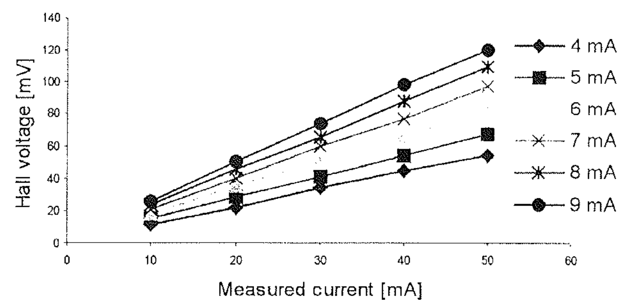


Fig. 6: The static characteristics of the differential Hall voltages for different gains of the Hall sensor

Compensation of the offset voltage can be done with an electronic circuit, however it is better to record the course of the offset voltage in relation to the excitation current of the sensor and the temperature of the sensor, and then store it into the memory. The measured course of the offset voltage at a constant temperature is shown in Fig. 7.

Fig. 8 shows the measured statical characteristic of the sensor with the adaptation of the gain.

For example, there are 5 measuring ranges shown for currents measured from 1 mA to 64 mA. The output voltage of the analog part of the measuring circuit moves in the range from 1 to 7 V. In the case of the ordinary

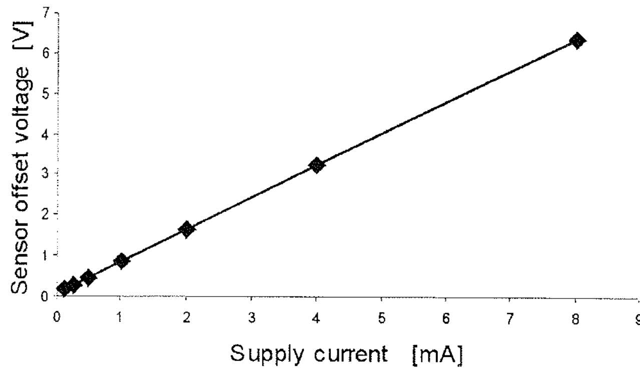


Fig. 7: Measured course of the offset voltage at a constant temperature

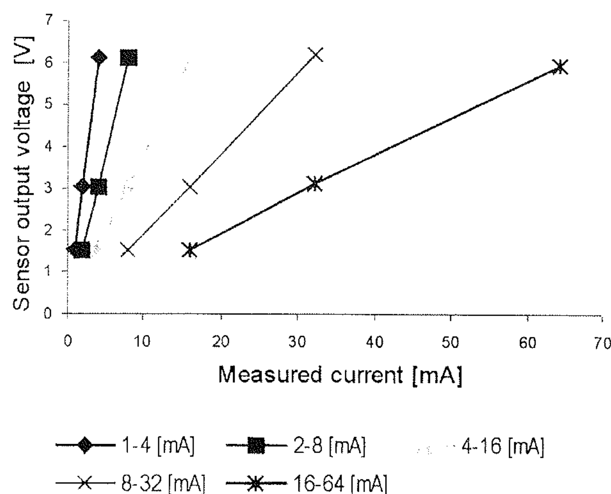


Fig. 8: The measured statical characteristic of the sensor with the adaptation of the gain}

sensor, to achieve the measuring class 0.2, defined by the standard IEC687, a 15 bit AD converter must be used for the range measuring from 1 mA to 64 mA. In the case of the proposed adaptive sensor, only a 12 bit AD converter is required to achieve the measuring class 0.2 by the standard IEC687. The input measuring range of the AD converter is 1 to 7 V. 5 measuring ranges of the sensor are described with 3 bits of the DA converter. Thus there are still 3 additional measuring ranges that can be used to widen the measuring range of the measuring circuit without any change in its measuring class or that of the AD converter. Together there are 15 bits required to describe the measured signal inside the margin of error allowed for a class 0.2 measuring circuit.

5 Conclusion

In this article the current measuring circuit for the use in electric power meters is represented. The current measuring circuit uses a Hall sensor and exploits its properties to dynamically engage the measuring range. With this, it is possible to replace the high resolution and expensive AD converter with the standard, and therefore cheaper, AD and DA converter. In the case of the ordinary sensor, the AD converter must provide enough bits to satisfy the accuracy demands in the entire range of the measured signal. This means that at higher amplitudes of the measured signal there are less significant bits that are not necessary for that measuring range, and at low amplitudes we find the most significant bits which are not used for the measurement. In the case of the proposed adaptive current measuring circuit, this is avoided by the use of the changeable gain of the Hall sensor, so that AD converter must provide enough bits to satisfy the accuracy demands only inside the output range of the measuring circuit. By doing so, the needed bits for the AD converter are reduced. Measurements on the completed prototype of the measuring circuit have shown that the circuit is capable of satisfying all demands for accuracy in a wider current range, as the standard IEC687 requires.

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ANOTHER WAY OF A LIQUID FLOW MEASUREMENTS BY USING A SPECIALLY DESIGNED TURBINE

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Keywords: physics, medicine, liquid flow, liquid flow measurement, measuring turbines, IR light, InfraRed light

Abstract: We designed a special measuring turbine which is suitable for measurements of flow of various liquids in laboratory and animal experimets in medicine. Specifically, the turbine was designed for measurements of blood flow in isolated working pig hearts. The basic principle of measuring of liquid flow through the turbine is based on measurement of the time that elapses when the rotor rotates by one degree. For this purpose, the rotor is equiped with circular and transparent foil having a ring of 360 black lines printed near the circumference of the foil and oriented towards its centre. Sensory part is realized using two infra-red light-emitting diodes mounted on one side of the foil and two photo transistors as sensors of the transmitted infra-red light mounted on the other. By this way, the direction of rotation of the rotor can be identified. The characteristics of electronic part of the turbine are as follows: voltage regulated output ranging from 0 to ± 2.048 V, factor of a transformation described as 1 revolution of a rotor/s = 500 mV at the output (changeable by the programme), calculating time is 2 ms and resolution is 1 mV (11 bits). The electronic part is powered by external power supply of 5V. The turbine showed a linear response at a continuous saline flow up to 3,000 ml min^{-1} at pressure loads of between 20 and 220 cm H_2O. Pressure drop across the turbine depends on the volume flow and was 1 mmHg at 100 ml min^{-1} and 5 mmHg at 7,000 ml min^{-1}. A rotating moment $1.25x10^{-4}$ kg m^2 s^{-1} was calculated. The lowest volume change of a bolus of saline solution, detected by the turbine, was 1.6 ml. Similar, suitable adapted turbine could be used also for measurements of much bigger liquid flows.

Način merenja pretoka tekočin s posebno turbino

Ključne besede: fizika, medicina, pretok tekočin, merjenje pretoka tekočin, turbine merilne, IR svetloba infrardeča

Izvleček: Izdelali smo posebno merilno turbino, ki je primerna za merenje pretoka različnih tekočin pri laboratorijskih in živalskih poskusih v medicini. Pravzaprav smo izdelali turbino za merenje pretoka krvi na izoliranih prašičjih srcih. Osnovni princip merjenja pretoka tekočin skozi turbino sloni na merenju časa, ki preteče ko se rotor turbine zavrti za eno stopinjo. V ta namen je na rotor nameščena okrogla, prozorna folija na kateri je v bližini oboda natisnjenih 360 kratkih, pol stopinje širokih, v središče usmerjenih črnih črtic. Senzorski del je realiziran tako, da sta na eno stran folije nameščeni dve infrardeči svetleči diodi in na drugo stran dva foto transistorja. Tako lahko določimo tudi smer vrtenja turbine. Karakteristike elektronskega dela turbine so: napetostni izhod v območju od 0 do ±2.048 V, faktor pretvorbe 1 obr/s = 500 mV, zgornja meja (programsko določeno) 2.048 V, čas izračuna 2 ms in resolucija 1 mV (11 bitov). Elektronika je preko omrežnega pretvornika napajana z enosmerno napetostjo 5 V. Pri tlakih v območju med 20 in 220 cmH_2O in pretokih fiziološke raztopine do 3000 ml/min je signal na izhodu turbine povsem linearno odvisen od pretoka. Padec tlaka na turbini je odvisen od pretečenega volumna in je pri pretoku 100 ml/min enak 1 mmHg ter pri pretoku 7000 ml/min enak 5 mmHg. Vrtilni moment je bil empirično izračunan in znaša $1.25x10^{-4}$ kg m^2 s^{-1}. Najmanjša sprememba volumna, ki ga zazna turbina je enaka 1.6 ml. Ustrezno predelano turbino je moč uporabiti za merjenje veliko večjih pretokov tekočin.

Introduction

A liquid flow could be measured with flow meters based on different physical principle: an ultrasonic flow meter /1/, laser-doppler flow meter /2/, Venturi flow meter /3/, electromagnetic velocity transducer /4/, pulsed neutron activation /5/, sensing elements based on high-temperature superconductor ceramics /6/ and multiphase turbine flow meter /7/. Some of the above-mentioned flow meters such as the ultrasonic flow meter and laser-Doppler flow meter are not suitable for the measurement of saline liquid flow. One of the possible use of flow meters are also measurements on biologic systems. In experiments on biological systems, when different types of salt solutions are used (such as a heart perfusion), transducers that work on mechanical principles /8/ should be used as one of the proper tools for flow measurements.

The aim of our work was to develop and test a flow transducer based on mechanical principles that could be used as universal equipment for the measurement of continuous liquid flow.

Methods

Description of the mechanical part of the measuring turbine

Both parts of the turbine, the stator, with external dimensions 100 mm x 100 mm x 25 mm, and the rotor are machined from clear plexiglass (Figure 1). The axis and conical bearings are made of pure titanium to prevent the process of corrosion from occurring.

Description of the electronic part of the measuring turbine

The basic principle of measuring the dynamics of liquid flow through the turbine is based on measurement of the time that elapses when the rotor rotates by one degree. For this purpose, the rotor is equipped with transparent foil with a ring of 360 short black lines printed close to its circumference. Two infra-red light-emitting diodes (LED) are mounted on one side of the foil, and two photo transistors as sensors of the transmitted infra-red light are mounted on the other (Figure 2). During rotations of the turbine rotor the printed foil runs

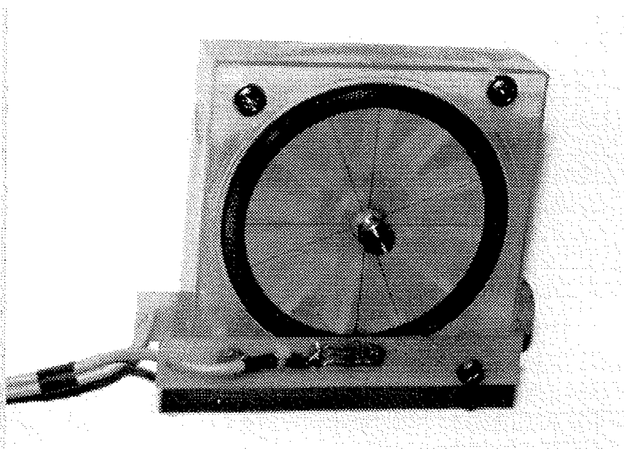

Fig. 1. Picture of the turbine. Both parts of the turbine, the stator with external dimensions of 100 mm x 100 mm x 25 mm, and the rotor, are machined from clear plexiglass.

LEDs and photo transistors and causes interruptions in the transmitted infra-red beam. Since we can expect the liquid to flow also in the opposite direction we used two of each of the afor-mentioned electronic components to enable the micro-controller to define the direction of rotation of the rotor.

Calculation of the turbine rotation moment

The turbine is filled with the saline solution during measurements of saline flow. The rotational moment of the turbine was calculated (estimated) according to a standard physical formula with a few simplifications: a. we proposed that the specific density of both water and plexiglass are of the same value, and b. we assumed that the rotating parts of the turbine and water behave like a rotating cylinder of water.

Calibration of the turbine

Constant pressure of the solution was exerted on the turbine inflow. The time for 3 liters of saline solution (0.9 % NaCl) flow was measured and the speed of the solution flow was calculated /9/. A calibration curve was drawn from the data obtained at certain inflow pressures: 20, 60, 80, 120, 180, 200 and 220 cm H_2O. At the mentioned inflow pressures different flow volumes were reached by using tubes with an inner diameter of 5 mm, 8 mm or 11 mm.

Measurement of pressure drop of the saline solution on the turbine

A pressure drop across the turbine was measured with commercial pressure transducers (Harward Instruments, UK). The transducer for measuring the pressure difference between the turbine inflow and turbine outflow was mounted in parallel to the turbine. One tube connected to one sensor input was mounted inside the inflow part of the turbine and another tube connected to the other inflow of the sensor inside the turbine outflow. Before measurements were taken the transducer was calibrated, so the measured pressure differences could be expressed in mmHg.

Results

Characteristics of the electronic circuitry (Figure 2): Voltage regulated output ranging from 0 to ±2.048 V, 1 revolution per second gives 500 mV at the output (changeable by programming), calculating time 2 ms, resolution 1 mV (11 bits), with an external power supply of 5V.

The turbine showed a completely linear response at a continuous saline flow of 30 – 400 ml min^{-1} at pressure loads between 20 and 220 cm H_2O and tubes with smaller inner diameter of 5 mm. Pressure drop measured across the turbine was 1 mmHg at a saline flow of 400 ml min^{-1}. At a continuous saline flow of 1,000 – 2,000 ml min^{-1}, using tubes of 8 mm inner diameter, pressure drop across the turbine was 1.4 mmHg. With 11 mm inner diameter tubes, higher flow volumes of up to 7,200 ml min^{-1} were produced. A flow dependence of the turbine against the inflow pressures of between 20 to 220 cm H_2O was not linear any more. The pressure drop across the turbine was 2 mmHg at 3,000 ml min^{-1} and 5 mmHg at 7,200 ml min^{-1} (Figure 3). The lowest detected volume flow by the turbine, caused by the bolus of saline solution, was 1.6 ml. That is the volume necessary for the rotation of the turbine by one degree. The calculated rotational moment of the turbine is 1.25×10^{-4} kg m^2 s^{-1}.

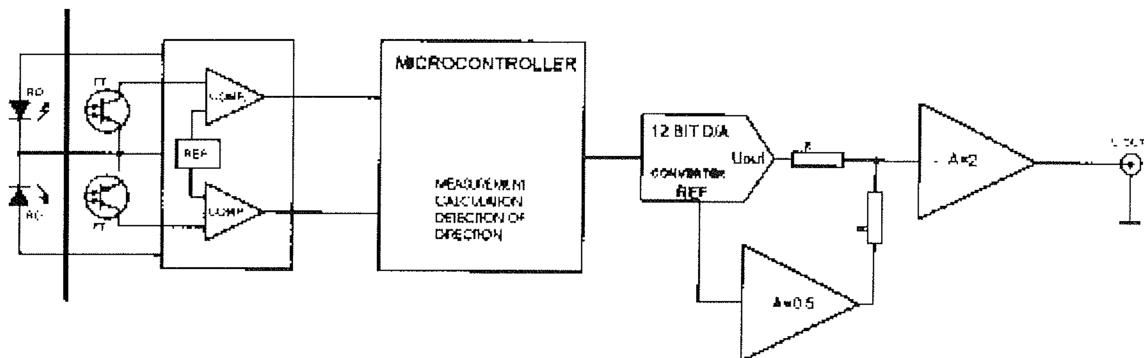

Fig 2. Schematic diagram of the electronic part of the turbine. IRD-infra-red diode, FT-phototransistor, COMP-comparator.

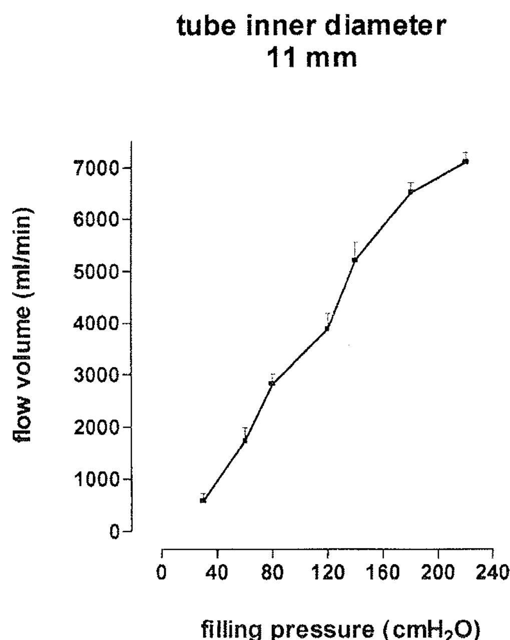

Fig 3. Flow characteristics of the turbine. Constant pressure of the saline solution was created on the turbine inflow. The time for 3 liters of the solution flow was measured and the speed of the solution flow calculated. Each point shows the average of three (n=3) measurements (±SD). A calibration curve was drawn from the data obtained at certain inflow pressures: 20, 60, 80, 120, 180, 200 and 220 cm H_2O. Inner diameter of the tubes was 11 mm.

Discussion

We developed and tested a flow transducer based on mechanical principles that could be used for the measurement of continuous liquid flow. Because of the low rotation moment and high sensitivity, the system is able to measure volume flow changes of only a few milliliters without artifacts. Since the speed of rotation is low, the rotation moment and frequency characteristics of the turbine should have a low influence on the liquid flow through the turbine. The sensitivity of the turbine is quite suitable and is 1.6 ml. There are at least some solutions to improve the sensitivity of the turbine: a. by lowering the volume of the turbine box, b. by making a turbine with more shovels on rotor or, c. by making black lines on the transparent foil even closer together. The turbine is also suitable for the measurements of pulsative fluid flow. According to dimensions and sensitivity, the described turbine is well suited especially for low volume flow measurement. One of the possible use of the turbine are measurements on biologic systems. It is well suited for the experiments on isolated working pig hearts, when different types of salt solutions are used for a heart perfusion. Therefore, transducers that work on mechanical principles /8/ should be used as one of the proper tools for flow measurements. A similar turbine, with adapted dimensions, could be constructed also for making measurements of any volume flow. Our transducer is relatively simple, precise and low in price.

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PREDSTAVLJAMO INSTITUCIJO Z NASLOVNICE
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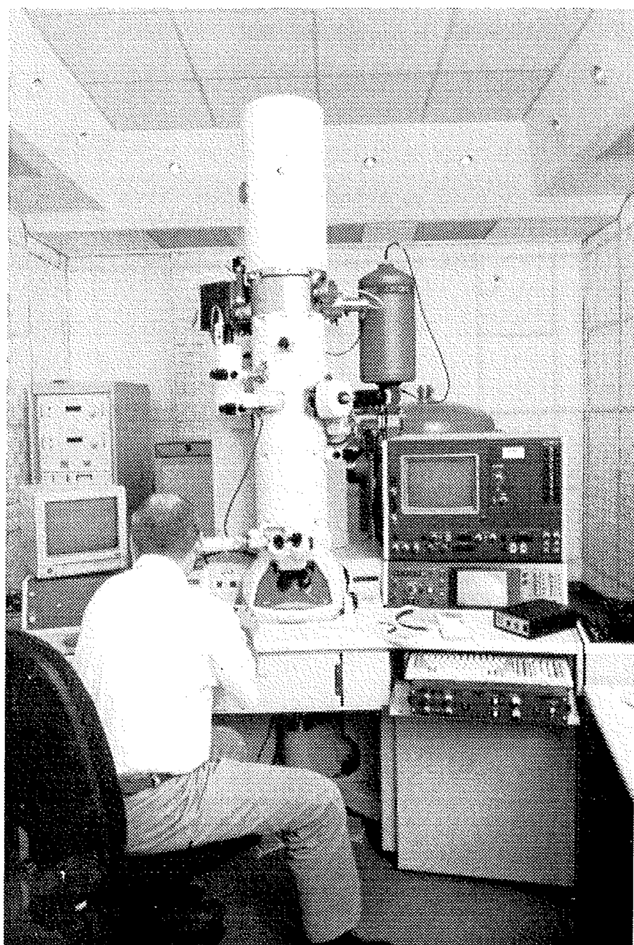
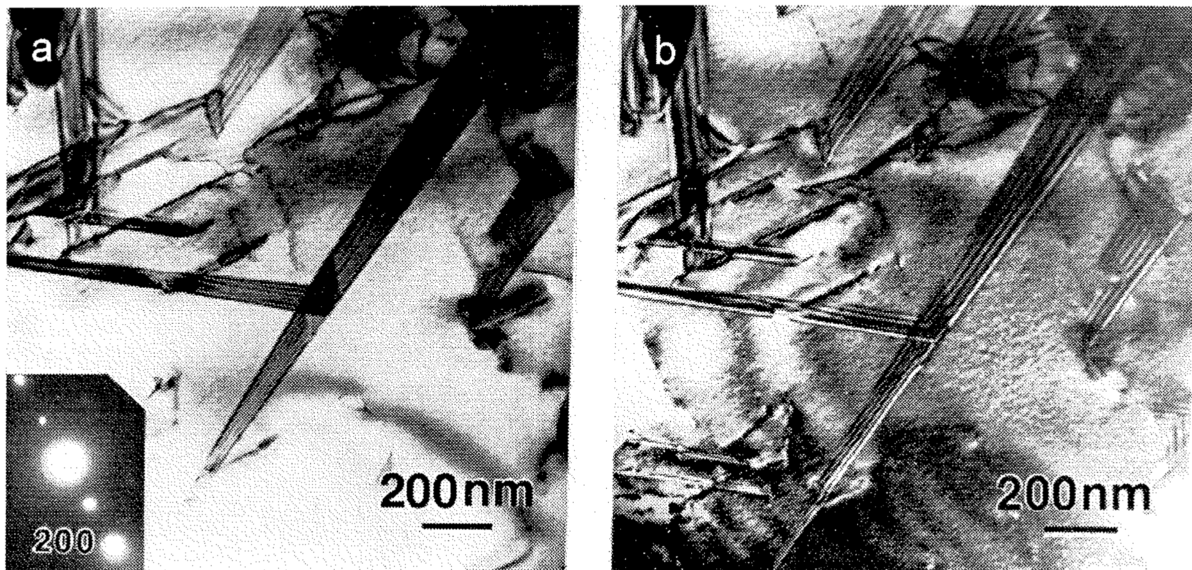
Novi analitski elektronski mikroskop JEM-2010F na Odseku za keramiko, Institut »Jožef Stefan«

Pri preiskavah keramičnih materialov je nujna uporaba različnih metod elektronske mikroskopije, ki omogočajo nedestruktivni pogled v morfologijo in strukturo materialov, kot tudi določevanje njihove kemijske sestave pri zelo velikih povečavah. Zato je Odsek za keramiko že pred petindvajsetimi leti kupil prvi vrstični elektronski mikroskop, ki so mu kasneje sledili še drugi. Leta 1995 pa se je izoblikovala ideja o nujnosti nakupa novega analitskega elektronskega mikroskopa z boljšimi karakteristikami. Po petih letih napornega dela ter pridobivanja podpore in sredstev se je projekt realiziral z nakupom in postavitvijo novega analitskega elektronskega mikroskopa JEM-2010F, ki je bil javnosti predstavljen z uradnim odprtjem 22. junija letos.



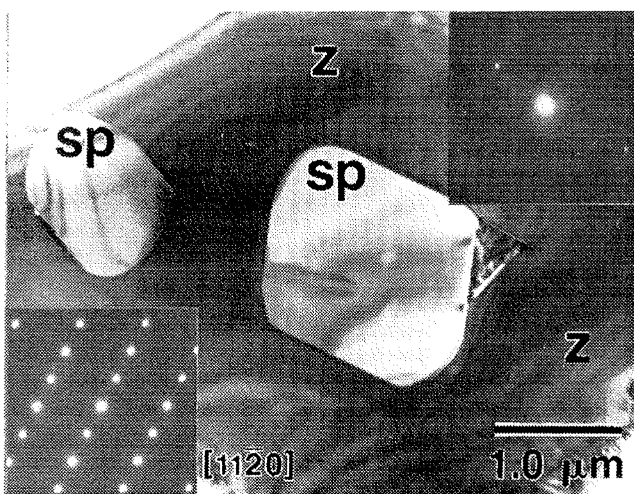
Slika 1: Pogled na analitski elektronski mikroskop JEM-2010F razkriva vso kompleksnost aparature. V ozadju mikroskopa je viden visokonapetostni tank, ki zagotavlja izredno stabilno pospeševalno napetost elektronov 200 kV. Izjemna občutljivost aparature za motnje iz okolice (vibracije, elektromagnetne motnje) zahteva posebno adaptacijo prostora.

Analitski elektronski mikroskop Jeol JEM-2010F spada po načinu delovanja med presevne (transmisijske) elektronske mikroskope in omogoča poleg opazovanja materialov pri zelo velikih povečavah tudi kvalitativno in kvantitativno kemijsko analizo preiskovanega vzorca, tako rekoč na atomarnem nivoju. Kot pri vseh presevnih elektronskih mikroskopih, tudi pri JEM-2010F »opazujemo« material z uporabo pospešenih elektronov v visokem vakuumu. Kot vir elektronov uporablja mikroskop JEM-2010F *field-emission* vir, pri katerem elektroni tunelirajo iz zelo ostre konice monokristala volframa v visoki vakuum. Krivinski radij na koncu igle meri samo nekaj nanometrov. V električnem polju ($2 \cdot 10^5$V) se elektroni pospešijo vzdolž kolone mikroskopa in se z magnetnimi lečami oblikujejo v zelo tanek curek. Magnetne leče imajo podobno vlogo kot brušene steklene leče pri optičnih mikroskopih. Curek elektronov nato usmerimo na ustrezno pripravljeni vzorec materiala. Osnovna zahteva je, da je vzorec preseven za elektrone (od tod tudi ime presevna oz. »transmisijska« elektronska mikroskopija). To pa pomeni, da morajo biti vzorci pravzaprav zelo tanke folije materiala, debele samo nekaj deset nm. Elektroni, ki prodrejo skozi vzorec, na koncu trčijo v fluorescenčni zaslon in s pojavom luminescence tvorijo sliko materiala, ki jo lahko neposredno opazujemo ali posnamemo na negativ, ali pa shranimo v digitalni obliki. Posebnost slik, posnetih s presevnim elektronskim mikroskopom je v tem, da na zaslonu opazujemo dvodimenzionalno sliko tridimenzionalnega vzorca, saj slika predstavlja povprečje skozi celotno debelino vzorca. Povečave, pri katerih lahko opazujemo vzorce z analitskim elektronskim mikroskopom JEM-2010F so res zelo velike, od nekaj tisočkrat pa celo do nekaj milijonkrat. Pri tako imenovani konvencionalni presevni elektronski mikroskopiji je rezultat slika preiskovanega materiala v svetlem oziroma temnem polju ali pa uklonska slika, ki daje podatke o kristalni orientaciji in celičnih parametrih preiskovanega dela materiala. S slikanjem v svetlem in temnem polju lahko tako opazujemo napake v kristalih (dislokacije, planarne napake), meje med zrni v polikristaliničnih materialih, tridimenzionalne precipitate, faze v večfaznih materialih in določamo kristalografske zveze med različnimi fazami v preiskovanem materialu. Povečave, ki jih uporabljamo pri konvencionalni presevni elektronski mikroskopiji, so od nekaj tisoč- pa do



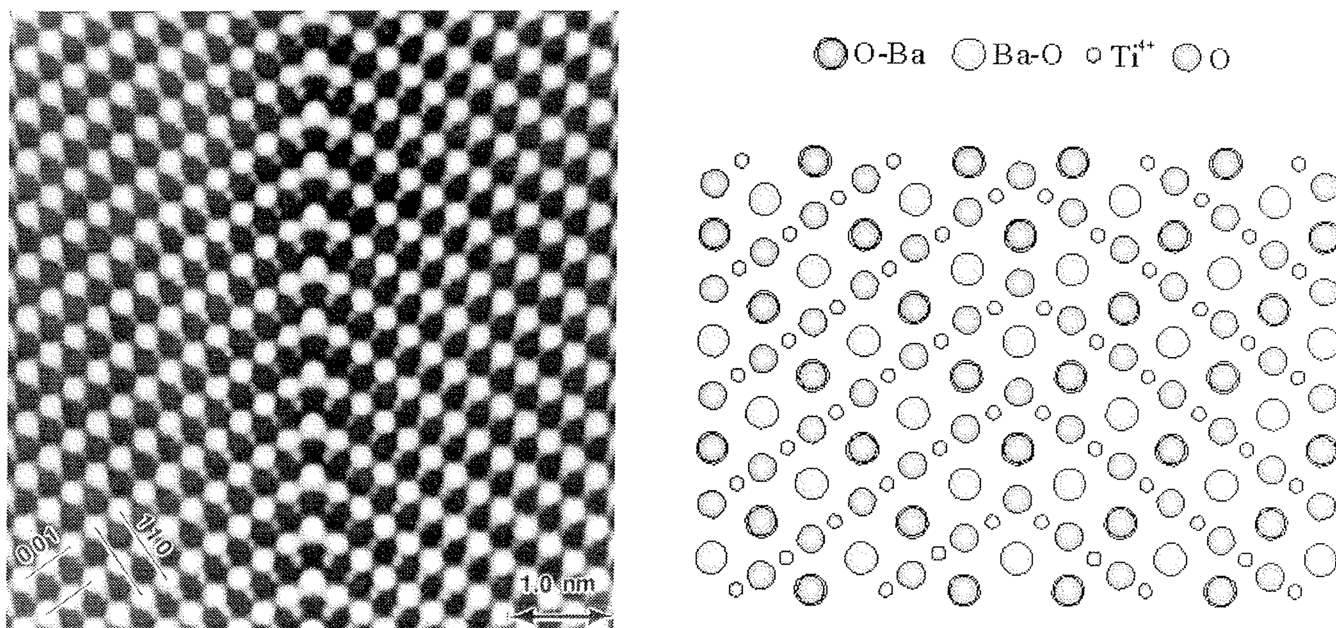
Slika 2: Konvencionalna presevna elektronska mikroskopija ploskovnih izločkov v keramiki $BaTiO_3$. Detajl je bil posnet v svetlem (a) in temnem (b) polju.

nekaj sto tisočkrat, detajli, ki jih opazujemo pa imajo dimenzije nekaj deset nm. Seveda omogoča mikroskop JEM-2010F zaradi izredno kvalitetne izdelave magnetnih leč in zelo stabilnega vira pospeševalne napetosti tudi precej večje povečave, s končno ločljivostjo med dvema točkama pod 0,19 nm. Zaradi tako visoke ločljivosti lahko uporabljamo analitski elektronski mikroskop JEM-2010F tudi kot visokoločljivostni presevni elektronski mikroskop, kar pomeni, da opazujemo atomske kolone v urejeni tridimenzionalni strukturi kristalov. Visokoločljivostna mikroskopija nam tako »pričara« svet urejenosti na atomarnem nivoju in omogoča direktno opazovanje položajev atomov v kristalih, na napakah in mejah med temi oziroma različnimi fazami. Kako pomembne za makroskopske lastnosti materialov so lahko spremembe v samo nekaj atomskih plasteh na površini urejenega kristala oziroma posameznega zrna v polikristaliničnem materialu, kažejo številne novejše



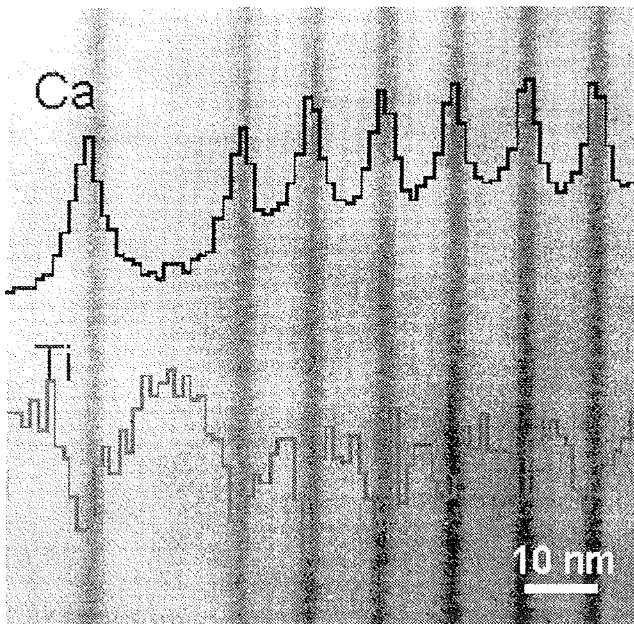
Slika 3: Posnetek vključkov faze spinela (sp) v varistorski keramiki (z). Uklonska slika elektronov pokaže, da so vključki poljubno orientirani v keramiki.

raziskave široko uporabljenih keramičnih materialov, kot so varistorji, pozistorji, feroelektrične in dielektrične tanke plasti, mikrovalovna keramika, superprevodniki. Visokoločljivostni posnetki atomskih kolon pa omogočajo tudi direktno primerjavo z izračunanimi strukturnimi modeli in so lahko eksperimentalna potrditev strukturnega modela. Novi analitski elektronski mikroskop JEM-2010F pa omogoča poleg slikanja materialov pri velikih povečavah tudi določevanje kemijske sestave preiskovanih materialov in situ. Kvalitativno in kvantitativno kemijsko analizo opravljamo z dvema različnima spektroskopskima metodama. Prva je tki. disperzijska spektroskopija rentgenskih žarkov (EDXS). Pri interakciji elektronskega curka z materialom se namreč nekaj energije elektronov porabi za nastanek karakterističnih rentgenskih žarkov elementov, ki material sestavljajo. Z ustreznim detektorjem lahko posnamemo energijski spekter rentgenskih žarkov, iz katerega dobimo podatek o kemijski sestavi. Druga spektroskopska metoda je tki. spektroskopija izgub energije elektronov (EELS). Pri prehodu elektronov skozi material namreč vsi elektroni ne ohranijo enake energije. Z analizo spektra, ki prikazuje, kako so elektroni izgubili energijo pri prehodu skozi material, dobimo poleg podatkov o sestavi tudi pomembne podatke o koordinaciji in valenčnem stanju atomov. Da lahko opravljamo kemijsko analizo z omenjenima spektroskopskima metodama s čim manjšega področja vzorca, je seveda zaželeno, da ima mikroskop čim manjši premer elektronskega curka, ki ga z posebno »vrstično enoto« lahko kontrolirano pomikamo po vzorcu. Premer elektronskega curka je pri JEM-2010F prav neverjetno majhen in lahko pri posebnih nastavitvah mikroskopa meri samo 0.5 nm! To pa pomeni, da lahko postavimo elektronski curek na določeno kolono atomov in določimo njeno kemijsko sestavo. Analitski elektronski mikroskop JEM-2010F je zelo kompleksna vrhunska aparatura, ki omogoča celovito strukturno in kemijsko karakterizacijo materialov v zelo širokem področju povečav in celo na atomarnem nivoju. Z nakupom omenjenega mikroskopa se je bistveno zmanjšal razkorak med opremljenostjo v našem prostoru in tisto v



Slika 4: Visokoločljivostna presevna elektronska mikroskopija dvojčične meje v feroelektrični keramiki $BaTiO_3$ s perovskitno strukturo (a) in strukturni model napake (b). Svetle pike ustrezajo položajem atomskih kolon, ki so paralelne z elektronskim curkom.

Slika 5: Kemijska analiza keramike $SrTiO_3$ z dodatkom železa z rentgensko spektroskopijo (EDS). Slika keramike prikazuje majhna zrna $SrTiO_3$ (a). Na mejah med posameznimi zrni je povečana koncentracija železa, kar je razvidno iz večje gostote svetlih točk (b) in iz EDS spektra, ki je bil posnet v označeni točki na meji (c).



Slika 6: Koncentracijski profili kalcija in titana preko ploskovnih napak v nestehiometrični keramiki. Koncentracija kalcija je veliko večja na 0,2 nm debelih plasteh (temne proge), kot v preostalem vzorcu. Koncentracijski profil je bil narejen na podlagi spektroskopije izgub energije elektronov (EELS) in s kontroliranim pomikom elektronskega curka po preiskovanem področju pri povečavi 8 milijonov.

tujih laboratorijih, ki se ukvarjajo z raziskavami materialov z metodami elektronske mikroskopije. Tako je danes na Odseku za keramiko zbrana vrhunska in edinstvena oprema v Republiki Sloveniji za preiskave anorganskih materialov z metodami elektronske mikroskopije, ki vključuje poleg novega analitskega elektronskega mikroskopa še tri vrstične elektronske mikroskope, en presevni elektronski mikroskop in aparature za pripravo vzorcev. Omenjena oprema je obenem del infrastrukturnega Centra za mikrostrukturno in površinsko analizo (CEMP), ki ga je Ministrstvo za znanost in tehnologijo ustanovilo leta 1992 kot prvi instrumentalni center v Republiki Sloveniji. Z elektronskimi mikroskopi delajo visoko specializirani in kvalificirani raziskovalci, kot tudi mladi raziskovalci v okviru njihovega podiplomskega izobraževanja. Analize z mikroskopi se izvajajo v okviru številnih raziskovalnih in razvojnih projektov nacionalnega programa, projektov za domačo in tujo industrijo ter mednarodnih projektov. Številne pa so tudi raziskovalne in izobraževalne institucije ter domača industrija, ki pogosto uporablja servisne storitve elektronske mikroskopije. Naj jih naštejemo samo nekaj: Kemijski inštitut, Ljubljana; Fakulteta za Farmacijo, Ljubljana; NTF, Oddelek za geologijo, Ljubljana; NTF, Oddelek za materiale in metalurgijo, Ljubljana; Inštitut za kovinske materiale in tehnologije, Ljubljana; Narodni muzej, Ljubljana; Restavratorski center RS, Ljubljana; Lek, d.d., Ljubljana; Swaty, d.d., Maribor; EMO, d.o.o, Celje; Akripol, d.d., Trebnje; AET, d.o.o., Tolmin; Termoelektrarna-Toplarna, Ljubljana; Mehanika, d.d., Trbovlje in Sinter, Ljubljana.

Za nakup analitskega elektronskega mikroskopa JEM-2010F so prispevali sredstva naslednji sovlagatelji: Ministrstvo za znanost in tehnologijo Republike Slovenije, Kemijski inštitut, Ljubljana, Inštitut za kovinske materiale in tehnologije, Ljubljana, Naravoslovnotehniška fakulteta Univerze v Ljubljani in naslednji odseki Instituta »Jožef Stefan«: Odsek za fiziko trdne snovi, Odsek za tanke plasti in površine ter Odsek za fizikalno in organsko kemijo.

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Konferenca z naslovom "23rd International Spring Seminar on Electronics Technology" (ISSE'2000), je bila v Balatonfüred-u, v letoviškem kraju ob Blatnem jezeru- Balaton-u - na Madžarskem. od 6. do 10. maja 2000. Mimogrede, ime "füred" pomeni zdravilišče ali počivališče ali nekaj podobnega, ob Blatnem jezeru. Prva ISSE konferenca je bila leta 1977 v Weissig-u (takrat Vzhodna Nemčija), nato pa se je konferenca vsako leto, z izjemo 1981, ko je ni bilo, "selila" med državami vzhodne in srednje Evrope. Konferenca je tradicionalno v začetku maja. Naslednja, 24. konferenca ISSE'2001 bo v Romuniji, (Calimanesti, Caciulat) predvidoma od 5. do 9. maja leta 2001. Konferenca leta 2002 bo predvidoma na Češkem, leta 2003 pa na Slovaškem.

Konference se je udeležilo preko 120 delegatov iz 17 držav, ki so predstavili 106 prispevkov. Od tega jih je bilo 26 podanih kot "govorjeni" referati, 80 pa kot posterji. Referati so bili razdeljeni v pet sekcij:

- Uvajanje naprednih orodij informacijske tehnologije v izobraževanje
- Neprestano izobraževanje in trening. Izobraževanje in raziskovanje po omrežju
- Raziskave, razvoj in testiranje materialov, komponent in elektronskih modulov
- Procesi in tehnologije elektronskih modulov v elektronskih sklopih.
- Elektronska vezja in multichip moduli. Načrtovanje in lastnosti

Referenti so imeli okrog 20 min časa za predstavitev in za diskusijo. Posterji so bili postavljeni v eni dopoldanski in dveh popoldanskih sekcijah. Avtorji so morali razložiti vsebino posterja v treh minutah, diskusija pa je potem potekala ob posameznih posterjih. Teme, obravnavane na konferenci, so obsegale široka področja, od izobraževanja, preko materialov, načrtovanja in računalniških simulacij do kontrole kvalitete. Vsi prispevki so objavljeni v zborniku, ki je narazpolago tako na Institutu Jožef Stefan kot v HIPOT-HYB. V poročilu bomo opisali nekaj, za nas zanimivejših prispevkov. Po približni oceni pa se je vsaj polovica prispevkov ukvarjala z "informatiko", od izobraževanja po Internetu do raznih simulacij.

P. Wesling (Compaq Computer Corp., Cupertino, ZDA) je v uvodnem predavanju "Models and standards for Internet-delivered courses in electronic packaging" predstavil možnosti in seveda problem pri učenju preko medmrežja. V uvodu je povedal, da stane ameriška podjetja izobraževanje sodelavcev približno 60 milijard dolarjev na leto. Računajo, da bi lahko okrog desetino tega denarja "pobralo" izobraževanje preko Interneta. \e danes je precej tega na razpolago na različnih lokacijah. Tudi univerze ponujajo precej predmetov ali kot samostojne kurze ali pa kot dopolnitev k klasičnemu študiju s predavanji v predavalnicah. Za "Computer based training" je bilo razvito že veliko računalniških okolij, vendar obvezujočih standardov še ni. Pri IEEE so ustanovili komisijo, ki se ukvarja s problemi standardizacije.

Več prispevkov je obravnavalo tudi probleme, kako poenotiti ocenjevanje uspeha študentov z različnimi šolskimi sistemi v različnih evropskih državah v nekaterih imajo, na primer, tako kot pri nas, številčno ocenjevanje pri izpitih za posamezne predmete. V drugih so različni predmeti ali vaje različno točkovanei in študent mora zbrati zahtevano število točk. Poleg tega bodo morali biti posamezni kurzi večjezični. Ena verzija bo angleška, druga pa bo morala biti v materinem jeziku študenta, ker zakoni v večini evropski držav zahtevajo poučevanje v domačem jeziku.

Z. Ilyefalvi-Vitez (Budapest University of Technology and Economics, Madžarska) je s sodelavci v več prispevkih predstavil t.i. virtualni laboratorij. Ta je osnovan na njihovih laboratorijih na Univerzi. Predstavili ga bomo na primeru njihoveha laboratorija z laserji. Ko se v osnovnem menuju odločiš za laserje, se najprej pokaže tloris laboratorija z laserji. Ko klikneš enega od laserjev, se pokaže njegova slika in osnovne tehnične karakteristike. Nato pa prične aminiran del. Če na primer klikneš lasersko glavo, se ta odpre in vidiš shematične sestavne dele. Če nato klikneš lasersko cev, se pojavi shema delovanja; kako fotoni iz svetila vzbujajo molekule laserskega sredstva, v tem primeru CO_2. Molekule CO_2 se "zvijajo" po zaslonu, ko kažejo različne oblike nihanj; nihanje v liniji, vibracije in rotacijo. In tako dalje in tako dalje. Pri vsaki stopnji lahko študent spreminja razne nastavitve in takoj vidi, kaj se zgodi. Če naredi preveliko napako, pač uniči virtualno napravo in ne prave. V diskusiji je nekdo vprašal, koliko časa so

porabili za razvoj. Odgovorili so, da doslej okrog 7000 človek/let, vendar projekt še ni končan.

Ilyefalvi-Vitez je tudi predstavil v referatu "International local network of electronic packaging education" idejo o projektu ENPACKED (Electronic Network for PACKaging EDucation), ki ga želijo prijaviti v 5 okvirni program. Projekt je namenjen izobraževanju in je zamišljen kot stran na Internetu, od kjer bi vodile povezave do partnerjev. V projektu naj bi bilo devet partnerjev iz devetih srednje- in vzhodno evropskih držav. Koordinator bo Univerza v Budimpešti, ki je vključena v svetovno mrežo s sedežem v ZDA (Georgia). Program si je možno ogledati na spletni strani:
http://www.ett.bme.hu/enpacked/start.html.
Naloga oziroma tema odseka za keramiko Instituta Jožef Stefan v okviru projekta bo "Tehnologija, materiali in testiranje debeloplastnih vezij". Ostali partnerji so iz Sofije, Bukarešte, Ukrajine, Poljske, Nemčije, Češke in Avstrije.

D. Leonescu je predstavil referat avtorjev iz Univerze "Politehnica", Bukarešta, Romunija in iz Univerze v Dresdenu, Nemčija, z naslovom "SPICE simulation of a thermoelectric module". V zelo zanimivem uvodu je poljudno opisal delovanje termoelektričnih hladilnikov, ki delajo na principu Peltierovega efekta. Princip delovanja je obraten od delovanja termoelementa, tako da se z električnim tokom, vsiljenim v "napačno smer", toplota na enem koncu absorbira, na drugem pa oddaja. Peltierovi elementi lahko hladijo vezja ali komponente pod temperaturo okolice. Enostopenjski element lahko ustvari do 70 K temperaturne razlike med hladno in toplo stranjo. Mikroelektronska vezja razvijajo vedno več toplote na enoto površine, zato je potrebno tako aktivno hlajenje. Danes komponente že "proizvajajo" do 25 W/cm^2, novi mikroprocesorji pa bodo generirali 50 W/cm^2. Projekcije kažejo na 100 W/cm^2, kar je preračunano, impresivna vrednost 1 MW/m^2. To je ilustriral s pripombo, da je gostota sevanja na površini sonca okrog 50 MW/m^2. V referatu so avtorji podali simulacije delovanja Peltierovih členov pod različnimi pogoji delovanja.

G. Harsanyi (Technical University of Budapest, Madžarska) je v referatu "Sensors' education and related student research projects" poročal o obsežnem delu na njihovi univerzi na področju senzorjev. Večini raziskav in razvoja je bilo opravljeno v okviru študentskih projektov. Predstavil je nekaj primerov. Prvi je bil debeloplastni senzor moči laserskega žarka. Ta se običajno meri s polprevodnimi ali piroelektričnimi detektorji, ki so natančni, vendar jih lahko prevelika energija poškoduje. Debeloplastni senzor je v osnovi narejen iz dveh koncentričnih krogov debeloplastnih uporov z visokim negativnim temperaturnim koeficientom upornosti (NTC). Laserski žarek sveti v središče in iz razlike upornosti, to je posledica različne temperature obeh krožnih uporov, izračunajo moč laserskega žarka. Drugi primer je bil senzor pritiska. Tega so realizirali, namesto z običajnimi debeloplastnimi upori na Al_2O_3 substratih, s polimernimi debeloplastnimi upori na polimernih membranah. Gauge faktorji (odvisnost relativne spremembe upornosti od deformacije) so za oba tipa uporov podobni, občutljivost senzorja na polimernem substratu pa je večja zaradi večje možne deformacije pri istem tlaku in zato večje občutljivosti. Ostalo so bili še senzorji pritiska na osnovi optičnih vlaken, biosenzorji za določanje sečne kisline in polimerni senzorji za redukcijske pline. Elektrode za biosenzerje so bili debeloplastni prevodniki na keramičnem substratu. Referenčna elektroda je bila srebrna, na srebro pa so z elektro mehaničnim kloriranjem (???) nanesli plast AgCl.

A. Pietrikova s sodelavci (Dept. Hybrid Microelectronics, Technical University of Kosice, Slovaška) je v referatu "Methane sensor based on organometallic thick film" predstavila debeloplastni senzor reducirnih plinov. Na keramičnem substratu sta dva simetrična senzorja, narejena iz zlatih elektrod v obliki glavnika, preko katerih je tiskana in žgana senzorska plast. Senzorski material je na osnovi SnO_2, dopiranega z 1% Pt. Eden od obeh senzorjev služi kot referenca. Pokrit je s plastjo stekla, tako da ne reagira z reducirajočimi plini in je njegova upornost odvisna samo od temperature. Na hrbtni strani substrata je natiskan meander z debeloplastnim prevodnikom na osnovi Pt, ki segreje senzor na delovno temperaturo med 420°C in 470°C. Prednost platine kot grelca je, da ima visoko pozitivno linearno odvisnost upornosti od temperature, tako da se pri določeni napetosti napajanja upornost in s tem temperatura ustali pri zaželjeni vrednost.

Nekaj referatov se je nanašalo na meritve šuma in nelinearnost za karakterizacijo debeloplastnih materialov. P. Mach (Czech Technical University, Praga, Češka) je v referatu "Diagnostics of thick film lines for microwave applications" podal meritve šuma in nelinearnost debeloplastnih prevodnih linij, ki naj bi se uporabljale za mikrovalovne aplikacije. Prevodniki na osnovi srebra so bili žgani na Al_2O_3 substratih. Linije širine 50 μm so bile oblikovane s fotopostopkom. Rezultati so pokazali, da se debeloplastne prevodne linije, če je rob prevodnika dovolj ostro definiran, lahko uporabljajo za mikrovalovne aplikacije. I. B. Pelikanova, prav tako s Tehnične univerze v Pragi, je v referatu z naslovom "Nonlinearity of thick film resistors" podala rezultate meritev nelinearnosti debeloplastnih uporov, žganih na substratih na osnovi Al_2O_3 ali AlN. Idealen upor ima linearno odvisnost toka od napetosti. Nelinearni odzivi pomenijo odstopanje od te idealnosti. Ti odzivi so lahko posledica več faktorjev, na primer nehomogenosti v uporovnem materialu (porazdelitev delcev prevodne faze, pore v strukturi itd.), neidealen stik med uporom in prevodnikom, mehanizem prevajanja in tako dalje. Nelinearnost uporov, žganih na AlN sustratih, je bila precej višja. To kaže, da uporovni material, razvit posebej za AlN substrate (uporovna serija Du Pont 9200) še ni optimiziran.

S. Achmatowicz je predstavil prispevek z naslovom "Development of novel dielectric thick films for device and circuit applications". Delo, ki ima kar devet avtorjev, je rezultat sodelovanja petih institucij; Florida State University (Tallahassee, ZDA), Institute of Electronic Materials Technology (Varšava, Poljska), Wroclaw University of Technology (Poljska), Florida A@M University (Tallahassee, ZDA) in Institute of Solid State and Semiconductor Physics (Minsk, Belorusija). Podali so preliminarne rezultate o pripravi debeloplastnega dielektričnega materiala na osnovi kubičnega bor nitrida. BN je zelo trd material s kristalno strukturo, podobno strukturi diamanta. Ima, tako kot diamant, zelo visoko toplotno prevodnost, nekajkrat višjo kot kovinski

baker in je električni izolator. Ker je kovalentno vezana spojina, se sam po sebi praktično ne sintra ne glede na temperaturo. Da bi dobili gosto zasintrano plast pri 850°C, kar je običajna temperatura žganja v debeloplastni tehnologiji, mu je treba dodati vezivno fazo. Preiskusili so nekaj deset različnih steklenih frit. Najboljše rezultate so dobili s steklom na osnovi Bi_2O_3, SiO_2 in B_2O_3. Da bi ohranili dobre toplotne karakteristike dielektrika, morajo še optimizirati sestavo. Dodatek okrog 5% stekla tvori pri žganju film na površini zrn BN in jih poveže v zasintrano, vendar porozno strukturo. Večja vsebnost stekla pripelje do gosto sintrane plast, vendar izolira med sabo BN zrna in "pokvari" toplotno prevodnost.

Nekaj prispevkov, čeprav precej manj kot v prejšnjih letih na tej konferenci, se je ukvarjalo s problemi zamenjave standardne svinec/kositer spajke v vezjih s spajkami brez svinca. Ker je kovinski svinec kot tudi njegove spojine do neke mere strupen, bo predlog nove evropske direktive Evropske skupnosti zahteval od proizvajalcev vezij ali elektronske opreme, da prenehajo uporabljati spajke na osnovi svinca do konca leta 2003, to je čez približno dve leti in pol. Proizvajalci električnih vezij so zaradi tega v precejšni zagati. Problem je seveda, da so "tradicionalne" Pb/Sn spajke, razen za visokotemperaturne aplikacije, skoraj idealne, kar se tiče cene in kvalitete. Zlitine, ki jih bodo morale zamenjati, so za isto kvaliteto oziroma podobne karakteristike precej dražje, materiali s primerljivo ceno pa imajo slabše karakteristike. Nekoliko irelevanten komentar o porabi svinca, ki sicer ne spada v to poročilo; letna potrošnja svinca je okrog 5 miljonov ton. Od tega se nekaj malega čez 80% porabi za akumulatorje. Naslednjih 10% porabe si približno enakomerno razdelijo svinec v vojaški ali lovski municiji ter svinčevi oksidi za različne uporabe (kristalno steklo, kemikalije, barvni pigmenti...). Spajke v elektroniki porabijo manj kot pol procenta vse proizvodnje svinca.

Z. Drozd (Warsaw University of Technology, Poljska) je v referatu "Selected quality characteristics of soldered joints" v uvodu predstavil fazne diagrame možnih zlitin s kositrom, ki bi lahko zamenjale Pb/Sn spajke. Seveda mora imeti vsaj ena kovina v sistemu, to je v tem primeru kositer, nizko tališče (kositer se stali pri 232°C). Dva sistema imata višjo temperaturo tališča evtektika kot Pb-Sn sistem (183°C pri sestavi 61.9 utežnih % kositra), tretji pa nižjo. Sistem kositer-baker ima tališče evtektika pri temperaturi 227°C in sestavi 99,3 utežnega % kositra. Sistem kositer-srebro ima evtektično tališče pri 221°C pri sestavi 96,5 utežnega % kositra in sistem kositer-bizmut evtektično tališče pri 139°C pri sestavi 43 utežnega % kositra. Ternarne zlitine se s temperaturo tališča lahko dovolj dobro približajo zaželeni temperaturi spajkanja. Večina referata pa je bila namenjena evaluaciji različnih načinov staranja in testiranja spojev, narejenih z "običajno" 60Sn/40Pb spajko. Rezultati naj bi služili kot smernice za smiselno in hitro evaluacijo novih spajk. Z. Morawska (Tele and Radio Research Institute, Warshaw; Poljska) je v referatu "Lead-free solderability preservative coatings of PCB's" obravnavala vsaj v izhodišču podobno temo. Na tiskanih vezjih se bakrene prevodne linije običajno zaščitijo s plastjo nečesa, kar preprečuje oksidacijo bakra, medtem ko vezja čakajo na nadaljnje postopke, predvsem na spajkanje komponent. Običajna zaščita je HASL (Hot Air Solder Leveling). Nanesejo plast staljene spajke, ki jo nato spihajo z vročim zrakom, tako da odpihnejo talino in ostane samo tanka prevleka spajke na bakrenih linijah. Testirali so različne zaščite, ki ne vsebujejo svinca. To so bile breztokovno nanešen Ni, na katerega zaradi spajkljivosti nanesejo še zlato, breztokovno nanesen kositer in zaščita z organskim filmom. Prvi dve prevleki sta spajkljivi, organski film pa odpari pri stiku s staljeno spajko. Vse tri zaščite so dale sprejemljive rezultate, vendar je zaščita z Ni/Au verjetno predraga za proizvodnjo tiskanih vezij.

Dva prispevka sta se ukvarjala s problematiko tiskanja pastoznih spajk. A. Paproth (Dresden University of Technology, Nemčija) je v referatu "Model of process capability of solder paste printing" opisal poskus evaluacije parametrov, ki vplivajo na kvaliteto tiskanja pastoznih spajk. Pri vezjih, narejenih s površinsko montažo komponent, je namreč okrog 60% odpovedi povezanih prav s slabo natiskano spajko. Določili so osem parametrov, ki naj bi odločali o kvaliteti sitotiska. To so: operater, parametri sitotiska, sito, rakel, okolje, tiskalnik, plošča tiskanega vezja in seveda pastozna spajka. Vsak od teh parametrov ima še nekaj "pod parametrov". Pri, na primer, pastozni spajki so to topilo, tiksotropija oziroma viskoznost pastozne spajke, organski nosilec, premer in volumski delež kroglic spajke in dodatki. Z metodo umetnih nevronskih mrež so "postavili" analitični model, ki predvidi rezultate pri različnih nivojih nastavitve posameznih parametrov, na primer trdota rakla in hitrost pomika rakla pri sitotisku. Pokazali so, da se lahko s primernim načrtovanjem poskusov z minimalnim številom eksperimentov lahko nastavi parametre za optimizacijo sitotiska glede na geometrijo natiskanih sledi in uporabljeno pastozno spajko. T. D. Savov (Sigma Delta Bulgaria, Sofija, Bolgarija) pa je v referatu z naslovom "Improvement of the solder paste stencil-printing process" poročal o poskusih izboljšanja definicije natiskanih pastoznih spajk. Razmeroma debele plasti pastozne spajke se tiskajo skozi kovinske folije, nalepljene na sitih. Ko se po prehodu rakla sito dvigne, ob robovih maske "odnese" s seboj nekaj spajke in pokvari ločljivost. Če sito zavibrira z ultra zvočno frekvenco v trenutku, ko se dvigne od substrata, te vibracije znatno zmanjšajo viskoznost tiksotropne paste, ki se dotika robov maske, tako da je sito ne odnese s seboj. Ultra zvočne vibracije, prav tako zaradi zmanjšajo viskoznosti tiksotropne pastozne spajke, priporočajo tudi pri čiščenju sita.

L. J. Golonka in sodelavci (Institute of Microsystem Technology, Wroclaw University of Technology, Poljska) so v več referatih obravnavali nekatere teme s področja keramičnih multichip modulov, narejenih z LTCC tehnologijo (LTCC - Low Temperature Cofired Ceramics). Referat z naslovom "Non-convencional application of laser in LTCC and thick-film technology - preliminary results" - z laserjem so izdelali prevodne linije širine 50 μm za grelce ali senzorske elektrode v LTCC strukturah. Uporabili so ga tudi za izdelovanje luknjic (vias) v zeleni LTCC foliji, skozi katere se povežejo prevodne ravnine v večplastnih strukturah. Podali so preliminarne rezultate laserskega doravnavanja uporov, ki so "pokopani" v večplastnih strukturah, skozi zgornjo plast dielektrika. V referatu z naslovom "Identification of the temperature distribution in LTCC multilayer structures by RBF net" pa so avtorji računali temperaturne gradiente v večplastnih keramičnih mul-

tichip modulih. Naredili so testne strukture – večplastno vezje s štirimi nivoji. Dielektrik so bile LTCC folije. Na vsakem nivoju v strukturi so "pokopani" debeloplastni termistorji, ki so bili tiskani in žgani tudi na vrhu večplastnega vezja. Termistorji, ki so služili ali kot grelci ali pa kot senzorji temperature, so bili debeloplastni NTC upori z visokim negativnim temperaturnim koeficientom upornosti. Izmerjeni rezultati so se zelo dobro ujemali z izračunanimi.

Udeleženci iz Slovenije (Institut Jožef Stefan in HIPOT HYB., Šentjernej) smo imeli na koferenci pet prispevkov. "Evaluation of diffusion patterning technology for thick film multilayers (D. Belavič, M. Hrovat, M. Pavlin) je bil predstavljen kot referat. Kot posterji pa so bili predstavljeni "The use of polimeric adhesives in binding power hybrid circuits to heat sinks (S. Maček, D. Ročak, P. Sebo, P. Stefanik), "Industrial pressure sensors: new trends in miniaturisation" (M. Pavlin, P. Luštek, D. Belavič, B. Pavlin), "Packaging aspects of pressure sensors" (I. Lahne, D. Belavič, M. Zarnik, M. Pavlin, S. Šoba, S. Gramc) in "Investigation of some thick film resistors for strain gauges" (M. Hrovat, D. Belavič, M. Jerlah). Zadnji prispevek je dobil priznanje "Excellent Poster Award for Senior Scientist".

Naši strokovnjaki dobivajo priznanja za svoje referate na konferencah v tujini

Referat Marka Hrovata, Darka Belaviča in Mitje Jerlaha z naslovom "Investigation of Some Thick-film Resistor Series for Strain Gauges" je bil predstavljen na " 23rd International Spring Seminar on Electronics Technology" (ISSE'2000), v Balatonfüred na Madžarskem (6. do 10. maja 2000). Delo je dobilo priznanje "Excellent Poster Award for Senior Scientist". Čestitamo in podajamo povzetek referata:

Investigation of Some Thick-film Resistor Series for Strain Gauges

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Abstract: Some commercial thick film resistors with sheet resistivities 1 kohm/sq. and 10 kohm/sq; were evaluated for strain gauge applications. Temperature-coefficients of resistivity, noise indices and gauge factors (GFs) were measured. For the same resistor series GFs and noise indices increase with increasing sheet resistivity. However, both GFs and noise indices are different for resistors with the same nominal sheet resistivity but from different resistor series.

Andreja Benčan se je v juliju 2000 udeležila 4. Evropskega Foruma o gorivnih celicah, ki je potekal v kraju Luzern v Švici. Vzporedno je potekala tudi konferenca »Fuel Cell 2000«. Konferenci sta se odvijali v popolnoma novem »Kultur - und Kongresszentrum Luzern«, francoskega arhitekta Jean-a Nouvela s, po besedah dr. Ulf Bossel-a, »najboljšo akustično koncertno dvorano na svetu«. Konferenc se je udeležilo približno 300 udeležencev iz celega sveta.

Na forumu je predstavila svoje delo kot poster z naslovom: "Compatibility between lanthanum ruthenate as a possible SOFC cathode nad materials for solid oxide electrolyte - preliminary data", (avtorji: Andreja Benčan, Marko Hrovat, Janez Holc, Zoran Samardžija in Marija Kosec). Predstavljeni rezultati so del raziskovalnega dela na področju prevodnih materialov za katode v gorivnih celicah s trdnim elektrolitom (SOFC), ki ga opravlja na odseku za keramiko, pod mentorstvom dr. Marka Hrovata.

Predstavitev je bila zelo uspešna, zanimanje za tematiko pa precejšnje, zato se Andreja Benčan še posebej zahvaljuje kolegoma Kristofferju Krnelu in Alešu Dakskoblerju za pomoč tako pri idejni zasnovi posterja kot pri sami izvedbi. Poster je bil nagrajen s Christian Friedrich Schonberin (znanstvenik, ki je prvi odkril gorivno celico) medaljo kot najboljši poster.

Ponovno čestitamo in podajamo povzetek posterja.

Compatibility between $LaRuO_3$ as possible SOFC cathode and materials for solid oxide electrolytes - preliminary data

Andreja Benčan, Marko Hrovat, Janez Holc, Zoran Samardžija, Marija Kosec, Jožef Stefan Institute, Ljubljana

For an SOFC operating at 1000°C cathode materials are mostly based on $(La_{1-x}Sr_x)MnO_3$. It is a relatively good electronic conductor but its ionic conductivity is low. At lower operating temperatures polarisation losses of manganites are too high for the efficient operation of a SOFC. Therefore other materials with possibly better electrical characteristics are investigated. Some of them, reported in the literature, are either RuO_2 or electrically conducting ruthenates, e.g., $Bi_2Ru_2O_7$ and $Y_2Ru_2O_7$, which are known to be useful electrocatalysts for oxygen reduction.

$LaRuO_3$ compound was evaluated as possible cathode material. Its electrical resistivity is around 20 mohm.cm and is relatively independent of temperature. The compatibility of $LaRuO_3$ with three different materials for solid oxide electrolytes, i.e. YSZ, $LaGaO_3$ and CeO_2, was investigated by XRD, SEM, and EDX of powder mixtures, which were fired for 60 hours at 1050°C. Both X-ray spectra and analysis of microstructures showed that $LaRuO_3$ do not react with other materials.

From these preliminary results it can therefore be tentatively concluded that $LaRuO_3$ based materials could be useful for SOFC cathodes due to a relatively low electrical resistivity and compatibility with the YSZ, CeO_2 or $LaGaO_3$ based solid electrolytes.

VESTI - NEWS

News from AMS

Austria Mikro Systeme International: Ground breaking of the new 200-mm production line

- Total investment cost: EUR 305 million
- Industrial volume production starting in the 1st quarter 2002
- New capacities for producing special technologies in the deep submicron range
- Creation of 150 new, highly-qualified jobs

Unterpremstätten (July 7, 2000). Numerous renowned guests of honour from politics, business and the media as well as the workforce of Austria Mikro Systeme International are today witnessing the official groundbreaking of the new 200-mm production line called "AMS2000" at the Unterpremstatten location.

Over the next few years, Austria Mikro Systeme International is going to invest a total of EUR 305 million into one of the most modern production lines for the production of application-specific integrated circuits (ASICs) and standard products (ASSPs) for automotive, telecommunications and industrial applications. Process and production optimisation with test wafer runs are planned to start in the second half of 2001 after a construction time of 11 months. Industrial volume production is scheduled to begin in the first quarter of 2002. On-time completion of the project, as well as adherence to the budget will be ensured by a project team consisting of experienced members of staff and external consultants. Johann Stritzelberger, member of the Managing Board: "Today's groundbreaking is the culmination of many years of complex strategic, technological and financial planning and takes the implementation phase to a concrete stage."

With 2000 wafer starts per week, "AMS2000" will, in future, provide the in-house capacities so urgently required to satisfy customer demands that have been increasing along with the continuously growing business volume. The new production line makes the production of special technologies developed by Austria Mikro Systeme International, such as high-voltage, BiCMOS and SiGe-BiCMOS with geometries as small as 0.35µm ("deep submicron") possible. In addition, the new production line also offers a solid basis for the short-term development and production of the next technology generations with geometries down to 0.18/0.15µm. Wolfgang Pribyl, member of the Board: "With the new 200-mm production line, Austria Mikro Systeme will be able to offer its customers the best in technologies as low as the deep submicron range for the implementation of future projects. The scheduled production capacity of at least 2,000 wafers per week provides the company and its customers with a sound basis to build on for future growth ".

48% of the overall investment costs of EUR 305 m will be borne by the company itself (equity funding), 11 % by subsidies and 41 % will come from outside funds. EUR 225 m will be spent on building, infrastructure and equipment, EUR 80 m on related investment such as assembly, test facilities and information technology.

"The implementation of the largest Austrian high-tech project ever is the pillar of success for our customers, our workforce, shareholders and financing partners", stresses Hans Jorg Kaltenbrunner, President and CEO of Austria Mikro Systeme International.

With this major investment, the company is going to provide the region with important fresh impetus on the job market. All in all, approximately 150 new, highly-qualified jobs are going to be created over the next few years; several industrial and trade companies from the region will act as suppliers and contractors during the construction phase.

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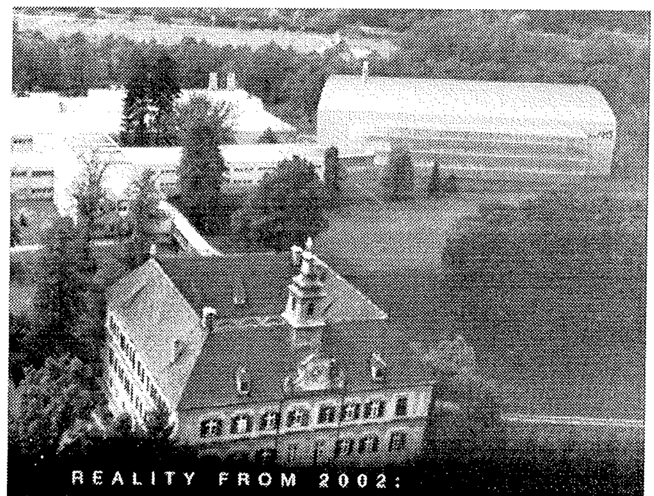


The new
200 mm
Production line

Austria Mikro Systeme International is going to build one of the most modern production lines for the production of application-specific integrated circuits (ASICs) and standard products (ASSPs) for automotive, industrial and communications applications in Unterpremstaetten.

News from IMEC newsletter, july 2000

Novel drying concepts for single-wafer wet cleaning

IMEC recently developed two novel fast-drying methods for single-wafer wet cleaning.

Current IC manufacturing faces major challenges. The transition to 300-mm wafer size has to be accomplished while the overall manufacturing cost continuously needs to be reduced. This leads to different manufacturing concepts and clean room layout. Farm layout clean rooms, consisting of dedicated bays, will be replaced by flow layouts in which different consecutively performed process steps are clustered, resulting in a major reduction of the wafer transport distance. Single-wafer processing becomes gradually dominant in IC manufacturing. Some critical processing steps such as pre-gate-stack formation arid CMP put stringent time constraints on the preceding or subsequent cleaning step. Consequently the introduction of a single wafer clustered clean is the most straightforward approach for such applications. In general, clustered cleans result in a reduction of the standard deviation of the process control parameters and a reduced cycle time. The inspection loop can be considerably shortened which can result in scrap reduction. Moreover, cleaning in single-wafer mode opens new possibilities such as single-side cleans.

Clustered cleans have often been associated with dry cleaning. Currently, wet cleaning is largely outperforming dry cleaning. However, one of the major roadblocks for single-wafer wet cleaning is the lack of a fast and high-performance (i.e. water mark-free) drying technique. Therefore, IMEC developed two new drying methods. The Lineagoni™ concept involves a track setup and is developed in collaboration with Steag as part of the Damasclean platform. In the second concept, called Rotagoni™, the wafer remains at its position during the drying process. This method is developed together with Verteq in the Goldfinger platform.

In the Lineagoni™ technique the wafer is slowly pushed through a relatively narrow box-shaped reactor via a narrow entrance and exits the slit at a controlled velocity. The reactor contains the process fluid. The ambient above the liquid is kept at a lower pressure with respect to the pressure adjacent to the chamber close to the slits. The leaking of the liquid can be prevented by tight tolerances on the slit dimensions. At the exit slit, an ambient is present containing a tensioactive vapour. This results in an effective drying of the outcoming wafer.

The Rotagoni™ method is based on interaction between Marangoni forces and rotational forces. Initially, a continuous flow of rinsing liquid is supplied on the wafer surface through a narrow dispensation tube. The wafer rotates at moderate speed. The dispensation tube slowly moves from the center of the substrate towards the edge. A second nozzle is mounted on the trailing side of the liquid dispense tube. This nozzle dispenses a tensioactive vapour, which reduces the surface tension of the liquid and creates an efficient Marangoni force. The unique interaction between the Marangoni effect and the rotational forces results in a high performance liquid removal.

Both techniques show excellent robustness on particle neutrality and high particle removal efficiency Also excellent cleaning results have been obtained on post Cu-CMP cleaning.

Characterization and implementation of low-k materials, a real challenge

IMEC devoted a lot of research to the implementation and characterization of low k materials towards 130 and 100-nm technology nodes. The investigations provide a good selection for low k materials.

Integration of multilevel metallization in deep-submicron technologies require major changes in material and technological concepts to decrease wiring delays and interline capacitance. It is clear that Cu is needed as alternative for Al in these advanced deep-submicron processes. Low-k dielectrics are required as insulator for critical products, such as high-density and high-speed applications. Low-k materials are still subject to a lot of material characterization. IMEC has devoted a lot of research to the characterization and implementation of both spin-on and CVD dielectrics.

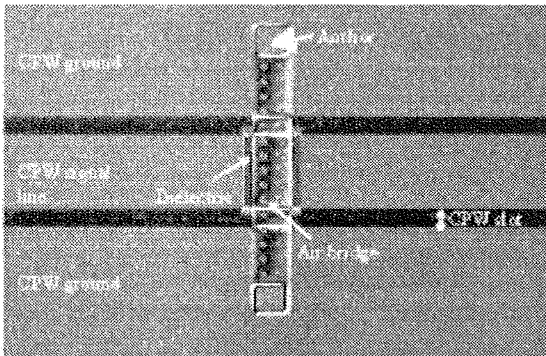
The lowering of the k-value is achieved by the increase of free volume in the matrix material or by adding porosity. Therefore, measurement of the free volume and the characterization of pore distribution, both in size and in shape (open or closed pores), are essential. To do this, IMEC has developed a wafer level porosimetry tool based on spectroscopic ellipsometry. The technique allows a direct study of the effect of process steps on the dielectric film properties, most importantly the effect of plasma and chemical treatments. This wafer level porosimetry has been used to characterize in detail density free volume and interconnectivity of both porous and non-porous materials after deposition and after process steps such as plasma treatment, chemical treatment etc. The relation between the material properties using real processing conditions and the electrical performance at critical dimensions provides valuable information in the debate of the low-k dielectric of choice.

For the research on stress evolution, the dielectric stacks are built up to several layers with various hard masks. SiC is a very promising hard mask material for its good adhesion properties as well as its diffusion barrier properties. The low-k dielectrics are implemented in single-damascene and dual-damascene modules for full electrical characterization. Interline capacitances have been measured for all categories of materials, The obtained k-values within the narrow spacings are related to the structure and/or composition of the low-k material, the dry etch and post dry etch clean processes and the Cu metallization. In addition, the structures are evaluated for leakage current breakdown etc: The investigations provide a good selection for low-k materials for multilevel integration towards the 130 and 100-nm nodes.

RF-MEMS devices for wireless communication

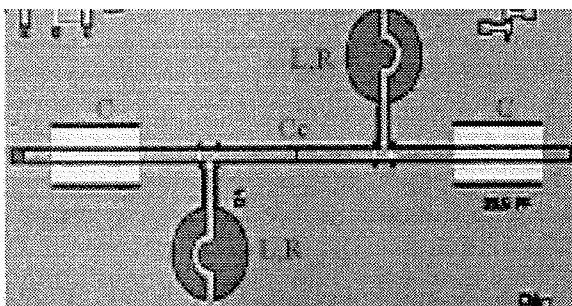
First demonstration of RF MEMS (micro-electromechanical) switches and lumped element LC filters has been made.The devices allow building low-loss high-linearity microwave circuits for wireless communication applications.

Wireless communication is showing an explosive growth. Future communication systems require low size and low weight, ever-increasing frequency and high functionality, which necessitate the use of highly integrated RF front-ends. Today the expensive off chip passive RF components play a limiting role. On-chip passive components however do not, reach the high quality offered by their discrete implementation. A promising alternative is the MEMS technology. IMEC has successfully developed RF MEMS shunt switches and lumped element LC filters. The devices are built on the same substrate using the same process flow. Coplanar waveguides (CPW) are used for the transmission line.



Shunt MEMS capacitive switch implemented on a CPW

The developed shunt switch is implemented on a CPW and behaves as a capacitive switch. The switch consists of a suspended movable metal bridge or membrane, which is mechanically anchored and electrically connected to the ground of the CPW. When the bridge is up, the capacitance of the signal line to ground is low (10 - 100 fF) and the switch is in the RF-ON state. Upon activation, the bridge pulls down onto a dielectric layer placed locally on top of the signal line. The capacitance becomes high and the switch is in the RF-OFF state.



A MEMS second order filter with series capacitive coupling

The area underneath the air bridge is covered with a thin film of tantalum pentoxide with a high dielectric constant. An isolation of 14 dB @ 5 GHz has been demonstrated and values over 30 dB are within the range of the technology. The insertion loss, including both the intrinsic loss of the switch and the loss introduced by the CPW is approximately 0.15 dB @ 5 GHz.

For the lumped-element bandpass LC filters, spiral inductors in combination with air gap capacitors are used. Both half turn coils and multi-turn coils were realized. Half turn loops are implemented in the same metal as used for the CPW. Multi-turn coils use the switch-bridge metal as an air bridge to interconnect the inner part of the inductor to the rest of the circuit. The air gap capacitance can be tuned, and therefore also the center frequency of the filter, by applying a DC voltage across the capacitor plates. The filters were designed to operate at a center frequency between 1 and 10 GHz.

Currently, a single-pole doublet-hrow (SPDT) switch is under development for application in a wireless local area network (WLAN) in the 5-6 GHz band. To establish an integrated system with maximum RF performance, a system-on-a-package (SoP) approach will be used, based on IMEC's MCM-D technology.

High-level simulation of substrate noise generation by large digital circuits

IMEC has developed a high-level simulation methodology (called Substrate noise Waveform Analysis, SWAN) to accurately and quickly simulate the substrate noise generation of large digital circuits on low ohmic substrates.

To make future telecommunication devices smaller and cheaper, more and more functions are integrated on one single chip. Also analog functions, such as analog-to-digital converters (ADC), are integrated on these mostly digital ICs. However, substrate noise, generated by large digital circuits, can severely deteriorate the performance of the analog circuits, integrated on the same IC substrate.

To analyze the impact of substrate noise on the performance of the analog circuits, the amount of noise generated by the large digital part must be known. Due to the large size of the digital circuits, normal circuit simulators such as SPICE can no longer be used to simulate the substrate noise generation. Therefore, IMEC has developed a high-level simulation methodology (SWAN) to estimate the substrate noise in an accurate and time efficient way.

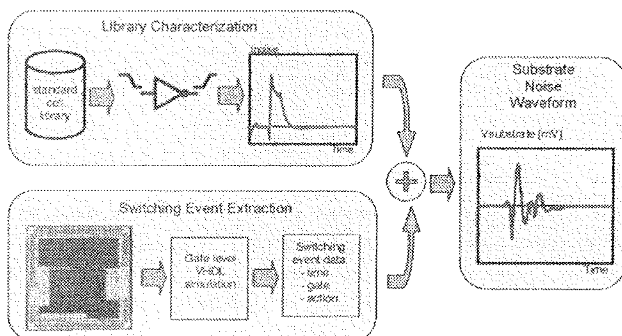
Two major sources of substrate noise generation can be distinguished: noise coupling from the switching gates and noise coupling from the power supply. Which of these two sources will be dominant is determined by the package parasitics. Because the exact package parasitics are not known during the design phase, the SWAN tool can also simulate the substrate noise generation as function of the package parasitics.

The high-level simulation methodology consists of two parts: standard cell library characterization and substrate noise waveform computation. First, the substrate noise generation and power supply current consump-

tion of all standard cells as function of the switching activity of the cell are extracted and recorded in a database together with a macro-model of the substrate of the cell. This step has only to be done once for a given technology. Next, the substrate noise is calculated for a given design. Therefore, all switching events of each gate are extracted from a standard gate-level VHDL simulation. By combining the noise generation of each gate with the switching activity data, an accurate waveform of the substrate noise signal can be calculated.

The SWAN tool is very helpful for the designer to estimate the noise impact on the analog circuits and to develop low-substrate noise digital design techniques. Since the tool takes into account package parasitics, an optimal packaging method can be determined. The tool also allows calculating the power consumption of the digital circuit. The methodology is currently being extended towards high-ohmic substrates.

This research is sponsored by the European Commission and the Flemish IWT (Institute for the Promotion of Innovation by Science and Technology in Flanders).



SWAN methodology flowchart

Poly-SiGe process for post-processing MEMS on CMOS wafers

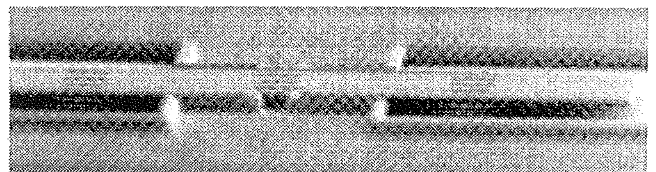
The reduction of the deposition temperature of poly-SiGe and the increase of maximum post-processing temperature on CMOS wafers allow post-processing of MEMS on standard CMOS wafers.

Micro-electromechanical systems (MEMS) such as infrared detectors, accelerometers, gyroscopes, ... are increasingly used. Monolithic integration of MEMS with the driving, controlling and signal processing electronics on the same CMOS substrate can improve performance, yield and reliability as well as lower the manufacturing, packaging and instrumentation costs. The easiest approach for monolithic integration is post-processing MEMS on top of the driving electronics, as it enables integrating MEMS without introducing any changes in the standard CMOS fabrication process. However, post processing limits the maximum fabrication temperature of MEMS in order to avoid any damage or degradation in the performance of the existing electronics. Polycrystalline silicon (poly-Si) has been widely used for MEMS applications, but this material requires a high processing temperature (> 800°C) to achieve a low tensile stress and to activate dopants.

Until now the maximum post-processing temperature on CMOS wafers with Al interconnections is generally considered to be 450°C. IMEC succeeded to increase the temperature up to 525°C without introducing any significant changes in the standard characteristics. The front-end is nearly unaffected, whereas for the back-end an increase in interconnection resistance has been observed. This resistance increase can be taken into account during circuit design and is not considered as a bottleneck.

Polycrystalline silicon germanium (poly-SiGe) is an attractive alternative for poly-Si as it has similar properties, while the presence of germanium reduces the required deposition and annealing temperature. IMEC could reduce the deposition temperature of poly-SiGe below 510°C, which is compatible with CMOS post processing. The grown layers, with 43 % germanium, have a low tensile stress suitable for post processing MEMS on top of the driving electronics.

IMEC's research is currently directed towards deposition of poly-SiGe at a temperature of 400°C. This will allow CMOS post-processing without any modifications into the standard characteristics.



First results of surface micromachined poly-SiGe structures deposited at 400°C and annealed at 450°C.

Development of a 0.35-μm SiGe BiCMOS process for RF applications with 80 GHz Fmax bipolar transistors

IMEC is finalizing the development of a selective SiGe HBT (Heterojunetion Bipolar Transistor) option for the 0.35-μm BiCMOS generation. Implementation of a selective SiGe base layer improved the performance significantly.

The growing demand for RF applications such as wireless communication, together with the need for higher frequency applications, drive the development of mixed analog/digital CMOS processes with integrated high-performance bipolar transistors. High-performance RF applications require high cutoff frequencies combined with a high Early voltage, high Fmax and low noise.

While IMECs implanted base 0.35 μm BiCMOS process reached already a high RF performance, with Ft of 30 GHz at V_{ce} =1V, an Early voltage of 20 V and BV_{ceo}=4V, the additional performance improvement by introducing SiGe for the base layer material is significant. To translate high Ft's also in high circuit performance, low device parasitics are extremely important. Therefore, a selective SiGe growth process was chosen, wifh a double poly inside spacer self-aligned architecture. The process

achieves an Ft of 50 GHz at V_{ce} =3 V and BV_{ceo} =4 V. Because of the low device parasitics, a high Fmax of 80 GHz is obtained. Furthermore, the graded Ge profile increases the Early voltage to 100 V The initially high current gain was traded off against low 1/f noise, by changing the poly emitter process without intentional re-grow of the interfacial oxide.

The selective SiGe base layers were grown in an ASM Epsilon 2000 single wafer reactor at a low process pressure to suppress loading effects. The linearly graded Ge profile has a peak concentration of 15 % and the grown base width is 45 nm.

The HBT is integrated in the analog 0.35-μm CMOS process. The process is extended with a full list of supporting devices such as various types of poly resistors, lateral and substrate pnp's, varactors with high tuning range and high Q factors, and a MIM (Metal Insulator Metal) capacitor with 1 fF/μm^2 specific capacitance. The developed SiGe BiCMOS process allows integration of high-performance RF functions.

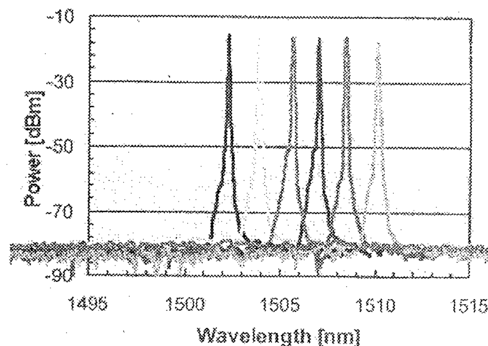
Cross section of 0.35-μm SiGe HBT

Hybrid phased-array multi-wavelength laser for WDM networks

A 7-channel multi-wavelength laser for WDM networks was realized using a new hybrid integration technology.

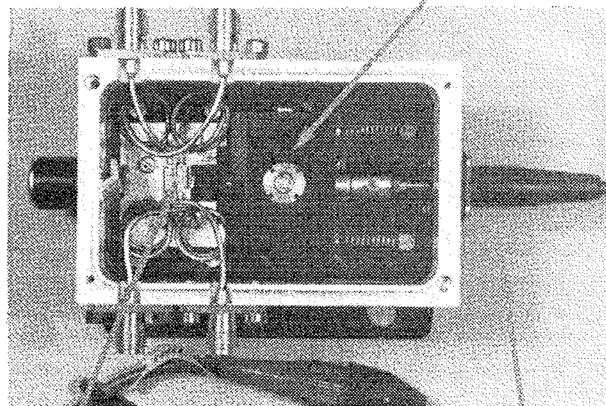
There is a growing tendency in WDM (wavelength division multiplexed) optical telecommunication networks towards the use of smaller channel spacing (down to 50 or even 25 GHz) and larger channel counts (up to 80). This puts very stringent requirements on the wavelength accuracy and wavelength spacing accuracy of the laser sources. Current systems typically use arrays of discrete wavelength distributed feedback (DFB) laser sources. An alternative is a multi-wavelength source, able to emit several channels simultaneously each of them separately modulated. Such a multi-wavelength laser can replace a whole array of discrete lasers or can be used as a wavelength selectable laser.

In the context of the European ACTS-project APEX, IMEC's associated laboratory INTEC (from the Ghent University) has realized such a laser. For that, an optical amplifier array has been integrated together with a phased array multiplexer (fabricated in collaboration with the Delft University of Technology) into one optical cavity. The phased array multiplexer provides for each channel a different wavelength selective amplifier feedback. If the gain of the amplifiers is high enough to compensate for the cavity losses, laser operation is obtained at a frequency determined by the multiplexer.



Superimposed oscillation spectra of a phased-array multi-wavelength laser

To fabricate the device, a hybrid integration technology was developed. The optical amplifier array and the phased array demultiplexer were realized on separate chips and permanently bonded together using an UV curing epoxy. The module was inserted in a suitable laser package to facilitate an easy optical and electronic access. The realized module consists of seven channels, spaced by 200 GHz (1.6 nm) with a threshold current varying between 38 mA and 48 mA. The 3-dB bandwidth is 1600 MHz, which is the highest value ever reported for this type of devices, and is limited by the cavity length. The laser linewidth is very small, namely below 1 MHz.



Photograph of the laser package with the Phased-Array multiwavelength laser

News from European Semiconductor, August 2000

Philips grab capacity

AMONG THE leading European semiconductor companies, Philips is expanding its operations in Southeast Asia and the US. In Singapore, Philips reports progress on its 200mm joint venture with the local Economic Development Board Investments organisation and the leading foundry Taiwan Semiconductor Manufacturing - a company in which Philips has a share. In the US, the Dutch company has bought up a 200 mm facility built jointly by IBM and Cirrus Logic.

Singapore jv steams ahead

The Systems-on-Silicon Manufacturing (SSMC) facility in Singapore is ahead of schedule, according to the joint venture's participants."Construction started less than a year ago with the first pile being driven in June 1999 and now we are installing the first tools," said SSMC's CEO, Peter Yates.

Philips' COO, Stuart McIntosh, adds: "When we first announced our intention to build this fab in late 1998, the semiconductor industry was in recession, but we predicted that we would need the capacity of this fab in late 2000 to meet the next upswing in semiconductor market demand. With the experience from Philips Semiconductors' MOS4 fab in Nijmegen, The Netherlands, which set a world record of 98 days from first equipment to first yielding wafers, the SSMC fab is all set to produce first silicon in September. This will ramp up to 10,000 wafers/month over the following months and will culminate in a maximum monthly output of 30,000 by June 2002."

A team of 150 engineers has received training in submicron processing at Philips' facilities in The Netherlands and TSMC's in Taiwan. The current workforce is 350 employees and by mid 2002 this should be 1050. The first tool on site was an ASM Lithography scanning system. More than 200 processing systems are to arrive in the next couple of months. Initial processing will be at the 0.25 µm node, with 0.18 being introduced next year.

US fab acquisition

In the US, Philips. Semiconductors has bought the 200mm MiCRUS semiconductor operation owned by IBM. The fab in East Fishkill NY . produces 250,000 wafers/year. Philips is to invest about $100 m to increase the facility's capacity and capability. Philips' total capacity is increased 12.5% with the move and BiCMOS capacity is more than doubled (by the end of 2001).

"We benefit from buying a fully operational plant thus getting the benefit of a high-calibre workforce," said McIntosh.

IBM became sole owner of the facility when Cirrus decided to return to a fabless state last year. About 950 people currently work at the facility and there are no plans for reductions. Production will continue to be at the 0.35 µm and 0.25 µm level, with new processes being added for communications chips (currently produced on the QUBiC BiCMOS process at Albuquerque NM).

Philips will supply IBM from the plant until 2002. "First silicon" for Philips is expected within weeks. By the end of this year, Philips will have six fully operational 200mm fabs.

Fully integrated manufacturing

IN 1993, the Tesla Sezam semiconductor fab in Rosnov, the Czech Republic, had 1100 wafer starts per week. Now the figure is 11,000. By the middle of next year the facility's majoriry owner ON Semiconductor is planning for 14,000. To achieve this increase in productivity some $14.4m has been spent upgrading the plant. Of course, the wafer size is 100 mm and the features 1.7 µm, but for analogue IC production this is not rare. The devices being produced are bipolar T0220 discretes and automotive rectifier diodes. Unusually packaging and test is also carried out at the same facility. However the Rosnov site doesn't just produce packaged ICs. Another company there is Terosil - also majority owned by ON: This produces 100, 125 and 150 mm silicon wafers. Some 100 mm wafers go to the Tesla fab in Rosnov but the remainder of the output is largely exported to ON Semiconductor facilities throughout the world.

Further, the Semiconductor Components Group Czech Design Center, also in Rosnov, is a wholly owned ON subsidiary. This designs and develops analogue ICs. Other activities of the centre include schematic and layout design, test development and product characterisation, design library development, and process characterisation and simulation.

Buy-out

The Rosnov facility became part of ON Semiconductor when the Semiconductor Components Group (SCG) came out of Motorola in a management buyout financed by the Texas Pacific Group, in August last year.

CEO Steve Hanson says the company has moved faster towards its objectives in nine months of existence than the industry or ON itself, expected.

Including joint ventures like Rosnov, ON Semiconductor employs 14,000 people, 13,000 of these directly. It has seven design centres and production facilities in the US (Phoenix AZ and East Greenwich), Mexico (Guadalarja), Japan (Aizu), the Czech Republic (Rosnov), the Slovak Republic (Piestany), China (Leshan), Malaysia and the Philippines. Currently 40% of its ICs are foundry-produced, but ultimately ON is aiming for only 20%.

ON is particularly keen on developing what it calls "fully integrated manufacturing" - in other words having facilities that not only produce die, but package and test them on the same site. The company is looking to 40% faster cycle times as a result. The company's Rosnov, Malaysian and Mexican facilities are already working on this basis with others due to combine front- and backend production soon.

The evaluation stage for ON's next worldwide expansion programme is being carried out now. The resulting roadmap is to be finalised this month. Today, 50-60%

of its global production is on 150 mm wafers - claimed by CEO Steve Hanson as the current "sweet spot" for analogue production. In five years time 200mm may take on that role. ON's products are aimed at the power and data management markets and broadband internet. This year, devices for the OC48 optical communication standard are to be produced, with OC192 ICs coming out in 2001.

Emitter-coupled logic

ON claims a 90% market share in devices that use high-speed emitter-coupled logic (ECL). Currently these are produced at 0.65 μm geometries with 0.5 μm coming soon. The development path then goes to 0.25 and 0.18μm.

Using ECL makes silicon better than gallium arsenide for high speed data management, says Hansori, "silicon germanium is a natural progression for us", he adds.

ECL technology is in its ninth generation. In the 1970s, typical switching speeds were 25ns. Now it's 125ps. With SiGe this could be pushed down to 35-40ps.

With respect to SiGe, the company is developing an approach to controlling with the stresses caused by lattice mismatches between the two components, but ON executives were unwilling to comment on the exact nature of this. It will be appropriate to the high-speed-digital rather than the RF market, where carbon doping is being used with some success by the collaboration between Motorola and the IHP semiconductor physics research institute in Frankfurt an der Oder.

At the Slovak Universiry of Technology, ON Semiconductor has set up a Centre for Microelectronics (ON-MiST). The initial collaboration between ON Semiconductor and the universiry will be for five years. The first phase funding is worth about $75,000. (SKK3.1m in the local currency). Joint development projects have been started. The Faculty of Electrical Engineering and Information Technology has already worked on projects connected with ON's facilities in Rosnov and Piestany (Slovak Republic). An internship programme for four fourth year students is to be provided at Piestany. Further sponsorship of SKK400,000 is to be used to upgrade and develop the university's laboratories for design, modelling simulation and characterisation.

KOLEDAR PRIREDITEV - CALENDAR OF EVENTS

September

SEPTEMBER 10-15, 2000
CLEO/EUROPE-IQEC 2000, NICE, FRANCE
A European conference on lasers and electro-optics, featuring the engineering and applications of lasers and electro-optic devices.
Contact Bill Bradbury, Primetek Solutions
Tel: +44 20 8546 0869
e-mail: wbprimetek@aol.com
web: www.cleoeurope.org

SEPTEMBER 14-16, 2000
IIT 2000, ALPBACH, AUSTRIA
Preceded by a three-day ion implantation school, the aim of the conference is to stimulate discussions of various aspects of ion implantation processing, from ion beam system design to device manufacturing.
Contact IIT2000, C/O IIS-B
Tel: +49 9131 761 100
Fax: +49 9131 761 102
e-mail: iit2000@iis-b.fhg.de

October

OCTOBER 16-17, 2000
3RD INTERNATIONAL CONFERENCE ON MATERIALS FOR MICROELECTRONICS, DUBLIN, IRELAND
Co-ordinated by the Electronics applications Division of the Institute of Materials, the conference aims to provide a forum for topics of current interest in the areas of growth, processing and materials device analysis of microelectronics that target devices and integrated circuit developments.
Contact Lisa Bromley IOM Comms
Tel: +44 20 7451 7302
Fax: +44 20 7839 2289
e-mail: lisa_bromley@materials.org.uk
web: www.materials.org.uk

OCTOBER 23-24, 2000
IP 2000, EDINBURGH, UK
A two-day conference and exhibition seeking to provide a forum for the latest developments in SOC design, and to address technology and relevant business issues surrounding the use of IP cores in a system level methodology. A vendor exhibition will run alongside the conference.
Contact Tanya Wakeham, Miller Freeman UK
Tel: +44 20 7861 6369
Fax: +44 20 7861 6247
e-mail: twakeham@unmf com
web: www.IP2000.com

OCTOBER 23-26, 2000
SILICON PROCESSING FOR ULSI CIRCUIT FABRICATION, LEUVEN, BELGIUM
A three-day course focusing on the practice, fundamentals and emerging trends of silicon wafer processing for deep sub-micron devices, including ultra-thin gate oxides, ultra-shallow junctions, low-k and Cu interconnect systems.
Contact: Marianne Van den Broeck, IMEC
Tel: +32 16 28 14 91
Fax: +32 16 28 16 37
e-mail: marianne.vandenbroeck@imec.be
web: www.imec.be

Events organised by IMAPS

The IMAPS Nordic 37th Annual Conference

Marienlyst Hotel,

Helsingřr, Denmark

10 - 13 September 2000

Proposed topics include:
Microelectronics applications
Trends in telecommunications
Ceramics for future electronics
Using unique materials
Manufacturing processes
High frequency packaging
Bare die, MCM and 3D packaging
BGAs in real life production
CSP and Flip Chip
Environmentally sound electronics
3-D moulded interconnect devices
Advanced interconnect, encapsulation
EU ban of Pb and halogens
Future electronics, strategies and R&D
MEMS, Micro Electro Mechanical Systems

For the latest information about the Conference and the Exhibition, visit our homepage at
http://www.imapsnordic.a.se
or email the Exhibitor Host at exhib@imapsnordic.a.se
IMAPS Nordic

IMAPS NORDIC
P.O. Box 277, SE-431 24 Mölndal, Sweden
Organisation no: 802005-3974
Fax: +46 19 56 7070, info@imapsnordic.a.se
http://www.imapsnordic.a.se

Chip Scale Packaging Advanced Technology Workshop

September 22-24, 2000

Sea Crest Oceanfront Resort & Conference Center

North Falmouth, MA

General Chair - Ted Tessier, Ph.D.
Technical Chair - Robert Hubbard

Nearly 30 Papers in the following Sessions -
Chip Scale Technology Development
Chip Scale Infrastructure Development
Wafer Scale CSP Technology Developments
CSP Reliability
New CSP Applications

Details - http://www.imaps.org
888-GO-IMAPS
703-758-1060
Visit IMAPS web site at http://www.imaps.org for the latest information on these and other upcoming IMAPS events

IMAPS Advanced Technology Workshop on Packaging and Integration of MEMS & Related Microsystems

Orlando Airport Marriott
Orlando, Florida
November 10-12, 2000
http://www.imaps.org/mems2k.htm
Sponsored by:IMAPS-International Microelectronics And Packaging Society in conjunction with IMECE 2000 o November 5-10*
*Visit http://www.asme.org/conf/congress00/index.htm for details on IMECE 2000

General Chair: Ajay P. Malshe, University of Arkansas, apm2@engr.uark.edu

Technical Chair: Albert Chiou, Motorola Labs, Albert Chiou@email.mot.com

Message from the Workshop Chairs:

MEMS and related microsystems are used for various mechanical, optical, chemical, biological, etc., sensing and actuation. They are the important elements of concept like system on a package (SOP), where functional spectrum not only includes electrical domain but also various other domains or signals such as mechanical, optical, chemical, magnetic, biological for sensing and/or for actuation. This ATW includes talks featuring advances and challenges of packaging and integration of MEMS and related microsystems. Philosophical difference in packaging IC versus MEMS is that IC really never wants to "touch" media where MEMS and related systems are designed to interact with media for sensing and actuation. Various MEMS and micro-systems packaging related issues are dicing, handling, wafer level packaging, media compatibility, out gassing and vacuum packaging, interconnection, etc. This ATW will discuss related MEMS and microsystem packaging and integration issues. The ATW is an international informal forum conducted by International Microelectronics And Packaging Society (IMAPS) to discuss recent advances and challenges in cutting edge emerging areas and at the same time catalyze technical partnerships between leading organizations. After the success of last year's MEMS ATW, this year's ATW is being orchestrated in the same city and time where ASME is conducting its winter annual meeting (IMECE 2000).

Up-coming Workshops in Electronics Packaging running at Chalmers University of Technology, Gothenburg Sweden in the next two months, chaired by Professor Johan Liu.

003 Conductive Adhesives for Electronics Packaging (1.5 days)
Aug.29-30/Oct.24-25,2000
Johan Liu, Chalmers University of Technology, Sweden

016 Low Cost Flip Chip Processing Based on No Flow Underfills (0.5 day)
Sept.5 (13:00-17:00), 2000
Daniel Baldwin, Georgia Institute of Technology, USA

005 Substrate Based Semiconductor Packaging (1 day)
Sep.8, 2000
Charles E. Bauer, Techlead Corporation, USA

006 Flip Chip Application & Bumping Technologies (1 day)
Sep.14/Nov.14, 2000
Peter Elenius, Flip Chip Technologies, USA

007 Thermomechanical Reliability of Microelectronic Packages (1 day)
Sep.15/Dec.7, 2000
Jianmin Qu, Georgia Institute of Technology, USA

014 An Introduction to the Thermal Design of Electronic Products (1 day)
Sept.19, 2000/Feb, 2001
David Whalley, Loughborough University, UK

015 Microelectronics & Photonics Packaging: Design for Reliability (1 day)
Sept.27, 2000
Ephraim Suhir, Bell Laboratories, Lucent Technologies, Inc., USA

If you need more details, please check our website at http://www.pe.chalmers.se/org/elprod/ ,
or you could contact:
Tel: 46-31-706-6291
Fax: 46-31-706-6289
Email:zhou@pe.chalmers.se