DESIGN CONSIDERATIONS OF LOW POWER MIXED SIGNAL FRONT-END FOR VOICE APPLICATIONS

Drago Strle
Faculty of Electrical Engineering, Ljubljana, Slovenia

Keywords: semiconductors, microelectronics, IC, integrated circuits, telecommunications, CMOS, Complementary Metal Oxide Semiconductors, circuit design, low power design, LV, Low Voltages, mixed analog digital integrated circuits, A/D converters, analog/digital converters

Abstract: Design considerations for low-voltage, low-power mixed signal front-end is presented in the article. Combined with digital decimation and interpolation filters it can be used as an embedded voice CODEC cell. Architecture and circuit design considerations to achieve low-power and low-voltage of important analog and mixed signal modules are described. Simulation and measured results demonstrate that circuit can operate from a single 1.2V supply voltage with quiescent power consumption of less than 4mW. The front-end layout area including periphery occupies about 4mm^2 and is fabricated in 0.35μm double poly, triple metal CMOS technology.

Načrtovanje analogno-digitalnega vmesnika z nizko porabo moči

Ključne besede: polprevodniki, mikroelektronika, IC vezja integrirana, telekomunikacije, CMOS polprevodniki kovinskooksidni komplementarni, snovanje vezij, snovanje za moči male, LV napetosti nizke, IC vezja integrirana mešana analogno digitalna, A-D pretvorniki analogno-digitalni

Povzetek: članek opisuje načrtovalske postopke pri načrtovanju mešanega analogno digitalnega integriranega vezja, ki deluje pri nizki napajalni napetosti in ima majhno porabo moči. Skupaj z digitalnim decimacijskim in interpolacijskim filtrom je uporaben kot "makro" celica CODEC. Predstavljena je arhitektura in načrtovalski postopki nekaterih pomembnih sklopov, ki sestavljajo vezje. Simulacijski rezultati dokazujejo, da predstavljeni moduli lahko delujejo pri napajalni napetosti 1.2V in pri porabi manšji od 4mW. Celotno vezje vključno s periferijo zaseda približno 4mm^2 silicija v tehnologiji CMOS z dolžino kanala 0.35μm, dvemi nivoji polisilicija in tremi nivoji metalov.

1 Introduction

Reducing power consumption in a mixed-signal integrated circuits is usually accomplished by reducing supply voltage as much as possible because in digital circuits power consumption is quadratically related to the supply voltage. Voltage reduction is limited by the analog portion of the circuit because of operating points and because of S/N ratio reduction. Decreasing noise level requires more area and more power consumption unless some clever system and circuit design tricks are used. Supply voltage is optimized in such a way that power is minimized while required characteristics are achieved. Using short channel CMOS process means, that matching accuracy of resistors, capacitors and MOS transistors are improved considerably while noise characteristics remains almost the same.

In this article circuit design considerations for low-power, low-voltage analog front-end that can be used in various voice integrated circuits are presented. The circuit is fabricated in 0.35μm CMOS technology and used together with digital decimation and interpolation filters as an embedded CODEC cell. For portable devices the most important characteristics is low power consumption to support extended life of the battery, so it is important that power optimization is carried out on all levels of the hierarchical design procedure. This includes selection of appropriate technology, architecture of the system and analog and/or mixed signal modules, minimization of power supply voltage and optimized circuit and layout design technique.

Section II describes typical mixed-signal front-end system for voice applications. In section III some basic design considerations for reduction of power consumption in a mixed-signal integrated circuits are presented. For voice frequency signal processing the supply voltage of a digital module can be lower than for analog modules because of small speed demands, so minimum supply voltage is determined by the analog modules requirements if common supply voltage is used. Most of the section III is reserved for describing selection of appropriate architecture and circuit design technique of critical analog modules such as modulator, band-gap reference and low noise microphone amplifier, having in mind low supply voltage and power consumption, while power buffer circuit design issues will be published in a separate article because of complexity of the problem. Some simulation results are presented in this section. Section IV summarizes experimental results of complete analog front-end.

2 System description

Figure 1 shows block diagram of an analog front-end of the embedded CODEC cell /4/. Microphone signal is amplified by programmable gain, low noise microphone amplifier, which adapts weak signal level of the electret microphone appropriately for modulator's 13 bits S/(N+D) ratio and linearity. Supply voltage for electret microphone is extracted from the band-gap reference circuit and buffered. Band-gap circuit also supply Σ - Δ A/D and D/A converters with appropriate differential reference voltages of Vref = $\pm$0.3V. Spectrum of the signal from microphone amplifier is limited by anti-aliasing filter which attenuates out of band spectral components; it is than sampled by input S-C stage of the Σ - Δ modulator, which converts analog signal into the bit-stream and is filtered by hard wired digital sinc^3 decimation filter followed by digital filter for band

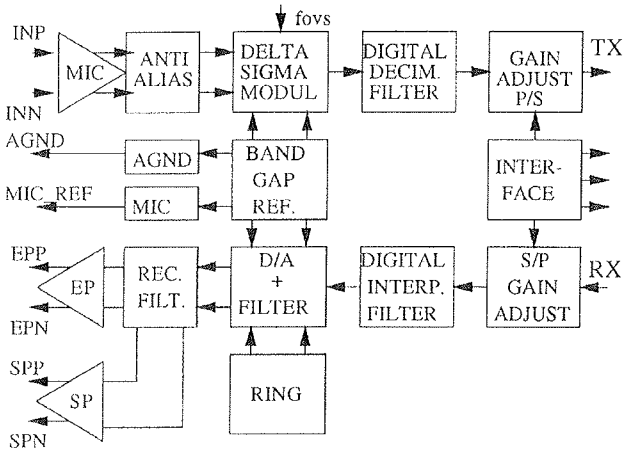

Fig. 1: Block diagram of mixed signal part of the embedded CODEC cell

limiting voice signal to 300-3400Hz band. Digital multiplier provides fine gain adjustment of the transmit gain. Digital voice signal is converted to 8 bit code (A- law or μ - law) and serially sent to the TX output, which can than be processed by appropriate DSP algorithm defined by the application.

On the receive side serial signal is coming from the DSP (dependent on the application) to the RX input where it is converted to 8 bits parallel code and than to 13 bits linear code (A- law or μ - law) running at 8kHz. Fine gain adjustment is followed by digital interpolation filter and digital Σ - Δ modulator, which increase the oversampling rate to approximately 1MHz and reduce number of bits to 1 by appropriate noise shaping; 1 bit D/A and 2´nd order Chebishev S-C filter followed by a 1´st order continuous time reconstruction filter produce voice band signal with correct spectrum, so that S/N ratio requirements of the receive section are full-filed. The signal is than buffered by 2 on chip power buffers; one can drive 300Ω headphones and has a programmable gain, while the other has a fixed gain and is capable of driving 50Ω loudspeaker.

3 Reduction of power consumption in mixed-signal IC

The most efficient way to reduce power consumption in a mixed-signal integrated circuit having big DSP and just small analog or mixed signal front-end is reduction of supply voltage. In a digital part of the circuit power consumption is quadratically related to the consumption approximately following the equation:

$$P = V^2 \Sigma_i C_i \beta_i f_i,$$

where β_i is a factor between 0 and 1 dependent on activity of the digital node i, C_i is the load capacitance of node i, f_i is the frequency of switching at corresponding digital node and V is constant supply voltage. From this equation it is clear that several possibilities exist to reduce power consumption. By using short channel technology and appropriate layout, node capacitances C_i can be reduced, by appropriate algorithm factor β_i and maybe f_i can be reduced. So it is very important to select appropriate architecture. Reduction of supply voltage is the most efficient way to reduce power consumption because its effects are related quadratically.

Using short channel technology forces to use low V_{sup} because of reduced break down voltages. The area of a digital module is directly related to the minimum channel length. Comparing the area needed to draw D type flip-flop cell in a 0.6μm and in a 0.35μm CMOS technology shows that the area is approximately 3 times smaller for later technology. Because the price of processing is not higher for the same factor it is clear that for digital circuits the realization is in favor to the short channel technology. It is not so for the isolated analog portion of the circuit but because the area of analog part is relatively small compared to the on chip digital DSP in a typical "voice" application, total area reduction still follows the rule and using short channel technology and low supply voltage is feasible.

The reduction of supply voltage has its limitations both in digital and analog modules of a mixed signal circuits as it will be presented in next subsections 3.1 and 3.2. Low supply voltage limit is defined by the analog portion of the chip because it needs bigger supply voltage compared to digital circuits. The baseband speed requirements for voice digital signal processing is not very demanding. Low supply voltage limit can be determined from required signal dynamics, speed, driving requirements, technology parameters etc.

3.1 Supply voltage influence on digital modules

Several mechanisms are responsible for power consumption in a digital IC /11/. The biggest contribution is the dynamic current needed for charging and discharging capacitive loads (gates, interconnect and parasitics) than current between supplies when both P and N channel transistors are switched on (careful design can reduce this current below 10% of the total consumption) and sub-threshold leakage which is dependent of the technology. Because power consumption of a digital circuit is quadratically related to the supply voltage minimum possible supply voltage must be used.

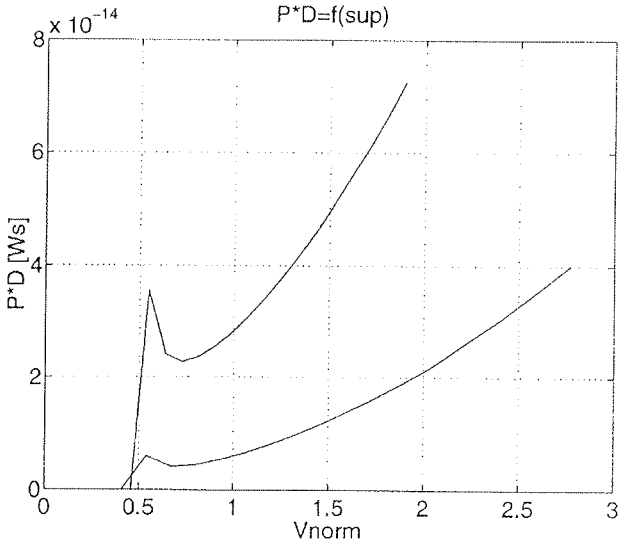

*Fig. 2: P*D product as a function of normalized supply voltage*

To determine appropriate supply voltage for digital part of a mixed-signal circuit for selected technology we performed a simulation of a simple inverter loaded with 3 inverters of the same size (C_{norm} = 3). On figure 2 PD (power*delay) product is plotted as a function of normalized power supply voltage ($V_{norm}=V_{sup}/(V_{THn}+V_{THp})$, with V_{THp} and V_{THn} threshold voltages of P and N channel MOS transistors, V_{sup} is supply voltage and V_{norm} is normalized supply voltage) as a function of supply voltage of loaded inverter for 0.6μm (upper curve) and 0.35μm (lower curve) CMOS technology. The dimensions are scaled in such a way that propagation delays are approximately the same at V_{sup} = 3V. From this figure we can conclude that the smallest supply voltage must be bigger than $0.8(V_{THn} + V_{THp})$ and that this is valid as long as the propagation delay is smaller than t_{pdmax}, which is a design parameter defined by the algorithm which has to be executed on this logic. For real technology with threshold voltages around $V_{THn} = |V_{THp}| = 0.6V$ the supply voltage must be bigger or equal to $V_{sup} \geq 1V$. For analog part of a mixed-signal circuit this supply voltage is not big enough for proper operation as will be explained in next subsection.

3.2 Supply voltage influence on analog and mixed signal modules

Real limitation to a minimum supply voltage is proper operation of analog or mixed signal modules under low voltage constraints. The following modules from the block diagram determine minimum supply voltage: band-gap reference, modulator, power amplifier and low noise amplifier. To avoid on chip supply voltage multipliers (they require additional power and silicon area and possibly external capacitors) careful evaluation of possible architectures and optimum circuit design is needed. The designer must take care of the following design issues when trying to design analog or mixed-signal circuit at low supply voltage:

- architecture of the module,
- dynamic range, noise and power consumption,
- switch ON impedance,
- selection and design of appropriate OTA or OPAMP to optimize power consumption, noise, driving capability etc.

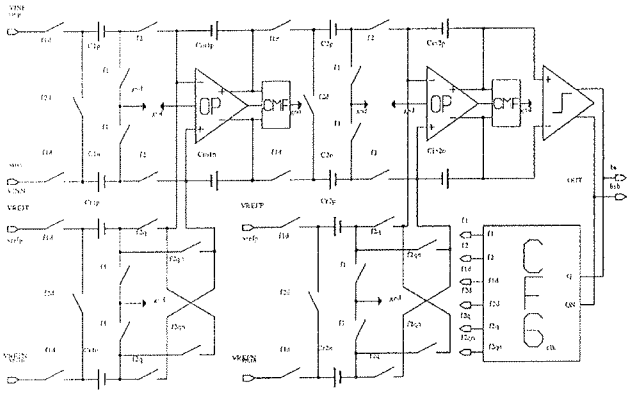

Fig. 3: Simplified circuit diagram of the modulator

Selection of appropriate architecture of the mixed-signal module (for example modulator) is a separate issue, which is beyond the scope of this article. Second order S-C modulator was selected because of reliability and inherent stability of the loop /7/ (figure 3). Its operation is described in literature. At low supply voltage max. signal is limited by proper operation of the circuit and by required dynamic range.

3.2.1 Dynamic range and power consumption of the modulator

Dynamic range is defined as a ratio between signal and noise power: DR = 10 log(S/N). Signal power is proportional to the supply voltage and efficiency factor β (β = 0.....1), which tells us how close to the supply voltage the signal can be (dependent of the circuit): $S=(\beta V_{sub}/\sqrt{2})^2$. Noise power is composed of several sources:

- $kT/C_{in}D_{ovs}$ and $kT/C_{ref}D_{ovs}$ are aliased thermal noise sources of the input and reference feedback S-C stage, which are the dominant noise sources; k is Boltzman´s constant, T is absolute temperature, C is input capacitor, $D_{ovs} = f_{ovs}/2f_0$ is the oversampling ratio and C_{in} and C_{ref} are input and reference S-C stages. The contributions of other S-C stages are smaller because they are multiplied by appropriate noise shaping transfer function weight.
- Noise of the first OPAMP of the modulator
- Noise of the microphone amplifier
- Noise of the band-gap reference circuit

We can assume equal thermal noise contribution from each source, so $N_{S-C}=N_r/5$; where N_r is required noise power obtained from the dynamic range specification of the system (DR from equation 1). If higher dynamic range is required at fixed V_{sup} and β the capacitance C of the S-C stage must be increased to reduce kT/C noise. If we assume simple model of class A OTA where supply current required for proper operation is proportional to $I_{sup} = k_I g_m (V_{gs}-V_{TH})$ (g_m is a transconductance and k_I is a constant, V_{gs} and V_{TH} are gate-source and threshold voltage of the differential stage transistors) and simple dominant pole model of the OTA where $g_m=k_f C f_{ovs}$ (k_f is constant, C is load capacitor of the OTA and f_{ovs} is oversampling frequency) than for higher load capacitance higher g_m is required, which can be achieved only by increased supply current Isup at fixed oversampling ratio and fixed V_{sup}. Power consumption of the S-C stage of the modulator is proportional to (equation 1):

$$P = \gamma\left(\frac{kT2f_0 10^{\frac{DR}{10}+1}}{\beta^2 V_{sup}}\right)(V_{GS} - V_{TH}) \qquad (1)$$

where: k is Boltzman´s constant, T is absolute temperature, f_0 is Nyquist frequency, DR is required dynamic range of the system and γ is a constant dependent on the type of OTA or OPAMP. We have several options to reduce power consumption:

- Higher V_{sup} gives smaller power consumption of the mixed-signal S-C modulator. It is thus recommended to have as big supply voltage as possible to increase

the dynamic range. This is so because by increasing supply voltage we can reduce capacitances of the S-C stages to achieve the same dynamic range and thus reduce the current. The limit of that optimization is the accuracy of the capacitor ratio, which is on the lower side limited by the technology. Because this analog front-end must coexists with big digital circuit where power consumption and supply voltage are related quadratically the optimum is dependent on the application and technology. Usually the V_{sup} is also defined by other components of the system, so careful evaluation of all design constraints and limits are necessary.

- β is important factor because it is squared, so it must be as close to 1 as possible, which means that the signal swing must be as close to the supply voltage as possible ($\beta = 1$ means that $V_{sig} = V_{sup}$). This can be achieved by careful selection of the architecture and circuit design of the modules.
- Power consumption is linearly dependent of γ. By selecting different kind of OTA (for example class AB) we can reduce γ and thus power consumption.

For good power optimization, careful considerations of each S-C stage aliased thermal noise contribution is necessary. For properly designed signal and noise transfer functions of the modulator only the contributions of the first stages enter the loop directly while the others are multiplied by appropriate noise transfer function weights, which means that the capacitances of the following stages of the modulator can be much smaller than in the first stage and limited only by the ratio accuracy requirements defined by the stability of the modulator´s loop and gain accuracy requirements.

3.2.2 Switch ON impedance

To increase signal swing in the S-C circuit, analysis of the switch ON resistance is necessary. Usually the switch is built of P and N MOS transistors of equal dimensions in parallel to reduce clock-feed-through effect /8/. Figure 4 shows setup for measuring ON resistance of the switch. Gate and body are connected to corresponding supply voltages, while input voltage is changing from gnd to V_{sup}. Figure 5 shows a conductance of the NMOS transistor (circles), PMOS transistor (stars) and combined conductances (solid line) as a function of normalized input voltage (V_{in} / V_{sup}) for two

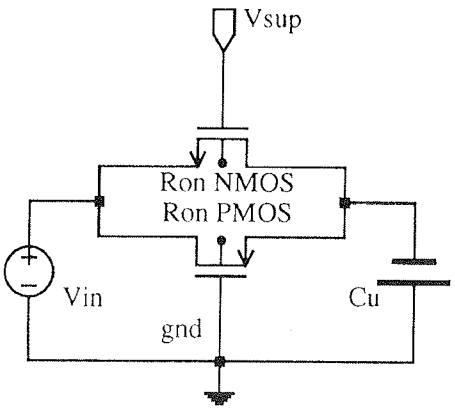

Fig. 4: Circuit for measuring switch ON resistance

supply voltages: V_{sup} = 4V and V_{sup} = 1V. When $V_{sup} \leq V_{THPef} + V_{THNef}$ (V_{THPef} and V_{THNef} are effective threshold voltages including body effects) a range of input voltage exists on the bottom part of the figure 5 where both transistor are off, so correct operation of the switch is not possible. The gate-source voltage must be big enough to prevent OFF condition and to reduce ON resistance according to the settling time requirements, having in mind that the switch dimension must be as small as possible to reduce clock-feed-through effects. This can be achieved on the following three ways: Increasing the supply voltage of the whole analog section, use of different technology with low V_{TH} or use the same supply voltage for analog and digital portion of the chip and increase only the control voltages for the switches. We used last possibility taking into considerations also reliability issues /5/, /1/, which means that terminal voltages V_{gs}, V_{gd} and V_{ds} are limited to rated operating conditions for the technology and controlled by appropriate layout. Clock form generator is realized as suggested on figure 6. Only N-channel MOS transistors are used as switches together with a circuit for clock-feed-through cancellation using MOS transistors

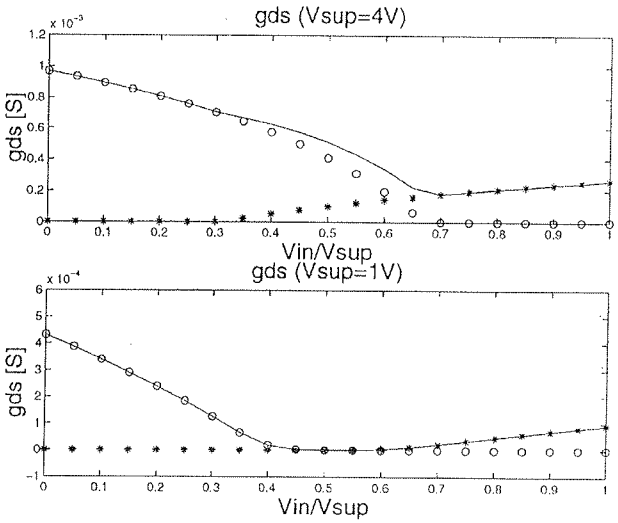

Fig. 5: Conductance of the switch

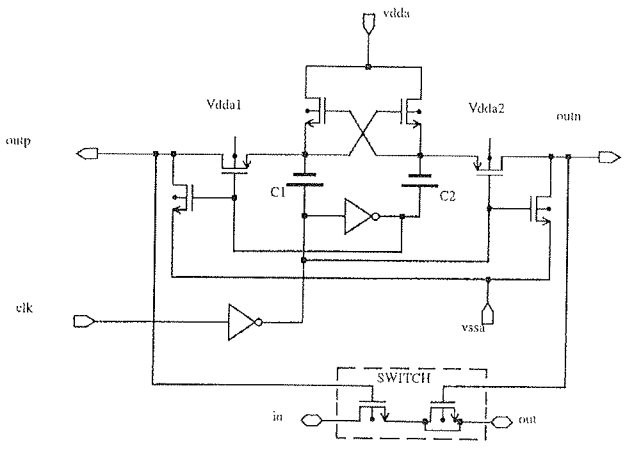

Fig. 6: Circuit for switch gate voltage multiplication

with short circuit between drain and source, driven by opposite clock and having two times smaller dimensions compared to the switch. The gate-source overdrive voltage is limited because capacitors C1 and C2 are selected according to the number of gates and parasitic capacitances connected to the clock phase. Using appropriate layout and careful evaluation of the parasitic capacitances of the clock lines we can assure that clock phase voltage V_{gs} of any switch never exceed allowed maximum voltage (for selected CMOS technology this is: $V_{sup} < 3.6V$). If signal ground is selected at: $V_{agnd} = 0.4V$ and signal swing: $V_{sig} = \pm 0.3V$ the opamp can operate under all conditions and clock voltage of $V_{clk} = 2.4V$ is sufficient to have good over drive of the switch: $0.9 \leq (V_{gs} - V_{THnef}) \leq 2.1V$. Body of MP1 and MP2 are connected to supply voltage Vdda1 and Vdda2 which are generated by similar on chip voltage multiplication circuit as used for the clock phases of the modulator except that these are stable voltages.

3.2.3 Design of modulator´s OPAMP

The modulator´s OPAMP topology can be selected according to the following requirements: $V_{sup} \geq 1.2V$, as big signal swing as possible, low frequency gain $A_0 \geq 60dB$ determined by the modulator´s gain accuracy and stability requirements, as small quiescent supply current as possible, noise better than $100nV/\sqrt{Hz}$ in a 4kHz band (from DR requirements and $V_{sigmax} = 0.3V$) and 0.1% settling time better than $t_{set} \leq 400ns$ for $f_{ovs} = 1MHz$. Because of PSRR requirements (/10/, /3/) fully differential 2 stage topology is selected with P channel folded cascode differential stage and class A common source output stage /9/. Simplified circuit diagram of the modulator´s opamp with cascode compensation is shown on figure 7. Fully differential switched capacitor common mode feedback circuit (not shown on the figure) is driven by similar multiplied clock form generator as used for the modulator. A careful circuit design ensures that signal swing is maximized. A PMOS differential transistors are used for two reasons: to improve PSRR by connecting sources of the differential stage transistors M1 and M2 to their body (N-well) and not to a noisy substrate, while another reason is proper operation of differential stage at low supply voltage. The signal ground voltage V_{agnd} is selected in such a way that transistors M_1 and M_2 are operating in moderate inversion, while M_3 is operating in strong inversion: $V_{agnd} \leq V_{sup} - |V_{THM1}| - V_{dsatM1} - V_{dsatM3} = 0.4V$, assuming $V_{THM1} = 0.6V$ with saturation voltage of 100mV. For

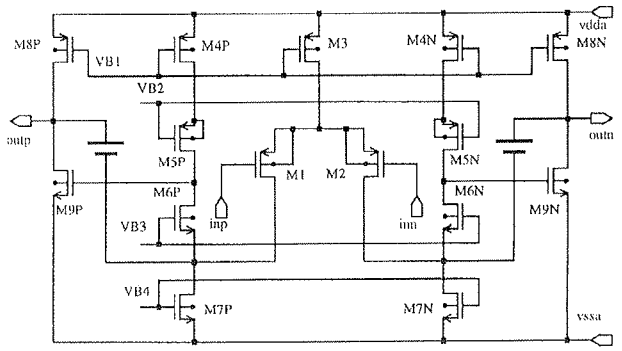

Fig. 7: Opamp of the modulator

voice applications the noise requirements of the modulator´s opamp is not very demanding because 1/f noise is suppressed by digital high-pass filter, while thermal noise requirement is important only for the first OPAMP. Based on noise simulations of the modulator /2/ minimum capacitance of the first S-C integrator was selected as $C_{in} = 0.3pF$, which is sufficient to maintain dynamic range of the modulator´s first integrator. Maximum load on each output of the first opamp (gain of the modulator is 1) is thus $C_{load} = C_{int} + C_{in} + C_{cm} + C_{par} \sim 1.2pF$, where $C_{int} = 2C_{in} = 0.6pF$ is integrator capacitance, $C_{in} = 0.3pF$ is input S-C stage capacitance, $C_{cm} = 0.2pF$ is common mode feedback capacitance and $C_{par} = 0.1pF$ is parasitic capacitance. According to the HSPICE simulations the first integrator consumes approximately 0.2mW at this capacitive load while the second integrator requires only 0.1mW because of 2 times smaller capacitances.

3.2.4 Design of band-gap circuit at low supply voltage

Curvature compensated band-gap voltage is usually built as: $V_{bg} = V_{be} + n\Delta V_{be} \cong 1.22V$ in such a way that temperature coefficient is equal zero at T = 25°C, where: $V_{be} = (kT/q)\ \ln(I/I_S)$, $k = 1.38 \times 10^{-23}$ J/K, $q = 1.6 \times 10^{-19}$C, T is absolute temperature, n is a factor which is selected so, that the TC = 0 at 25°C (usually by resistor ratio), $\Delta V_{be} = V_{be1} - V_{be2} = (kT)/q\ \ln(N)$ and N is the number of forward biased parallel diodes when $I_1 = I_2$ or in other words the ratio of current densities in bipolar transistors Q_1 and Q_2: $N = (JQ_1)/(JQ_2)$. Supply voltage of the original band-gap circuit must be bigger than V_{bg} for proper operation, so $V_{supp} \geq 1.4V$ is required when built in a standard way. Different kind of circuitry must be used for lower supply voltage, which generates smaller reference voltage. Figure 8 shows simplified circuit, which generates reference voltage smaller than 1.22V having similar characteristics as the original band-gap reference circuit (additional circuit for startup and trimming is not shown because of clarity of the figure) and is similar to one described in /6/. The circuit is best described by the following set of equations and assumptions:

- $I_1 = I_2 = I_3$, $V_a = V_b$ (ideal amplifier),
- $R_1 = R_2$,
- $I_1 = I_{1A} + I_{1B}$, $I_2 = I_{2A} + I_{2B}$,
- $I_{1A} = I_s\left(e^{\frac{qV_{be}}{kT}} - 1\right)$, $I_{1B} = \frac{V_{be}}{R_1}$
- $I_{2A} = \frac{\Delta V_{be}}{R_3}$, $I_{2B} = \frac{V_{be}}{R_1}$,
- $\Delta V_{be} = V_{be1} - V_{be2} = \frac{kT}{q}\ln(N)$

and equation 2:

$$V_{ref} = (I_{2A} + I_{2B})R_4 = \frac{R_4}{R_2}\left(V_{be} + \frac{R_2}{R_3}\Delta V_{be}\right) \qquad (2)$$

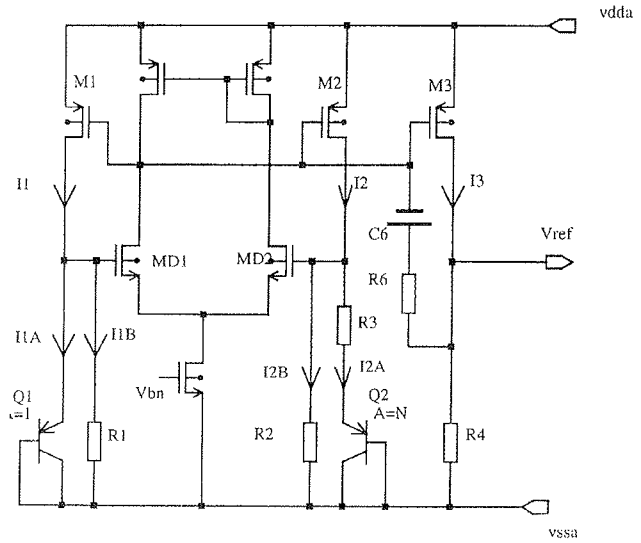

Fig. 8: Band-gap circuit with V_{ref} = 0.6V

This reference voltage is smaller than original reference by a factor R_4/R_2 and has approximately the same characteristics, which is to the first order independent of the absolute values of the resistors. Minimum supply voltage required for this circuit must be bigger than $V_{sup} \geq V_{be}+V_{dsat}$ = 1.0V, where V_{bemax} = 0.85V at T= -40°C and V_{dsat} is minimum saturation voltage of the current source transistor M_1. Another limitation is the amplifier operating point; the only comment necessary is that $V_{be} \geq V_{THMD1} + 2V_{dsat}$, which is possible to achieve with 0.35μm CMOS technology having maximum threshold voltage of V_{TH} = 0.6V and $V_{dsat} \geq$75mV. Because temperature coefficient of forward biased diode voltage is $TC_{Vbe} \cong$ -2mV/°C and temperature coefficient of threshold voltage of the MOS transistor $TC_{VTHn} \cong$ -1.1mV/°C the circuit has 2 limitations: at low temperature forward biased diode voltage is at maximum (for example at temperature -40°C the $V_{be} \cong$ 0.8V)

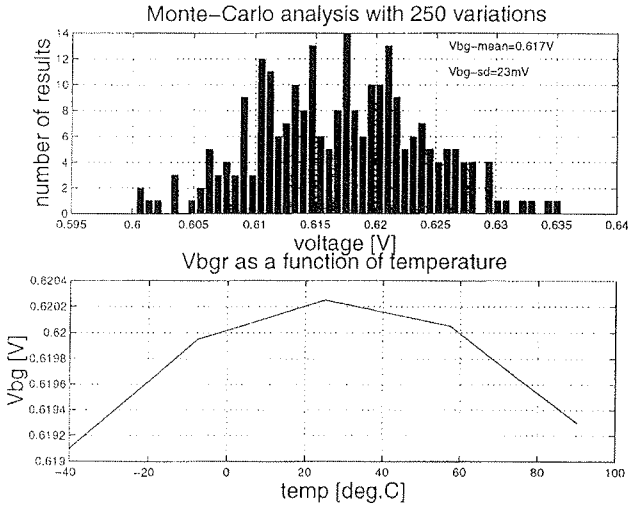

Fig. 9: Temperature behaviour and spread of reference voltage

and at high temperature (for example at T = +90°C $V_{be} \cong$ 0.58V). In first case the limitation is supply voltage and in last case the problem might be proper operation of operational amplifier when threshold voltage of transistor MD1 is at maximum. Carefully designed circuit maintains both conditions.

Having in mind considerations and limitations from the previous paragraph we built band-gap reference circuit which works correctly at $V_{sup} \geq$ 1.2V under all conditions having reference voltage of $V_{ref} \cong$ 0.6V. Figure 9 shows simulation results of temperature behavior and Monte Carlo analysis of the proposed band-gap reference circuit. It has the following characteristics: V_{ref} = 0.6V ± 23mV, TC ≤ 50ppm and current consumption is I_{sup} ≤ 5μA. Compensation of the feedback loop is achieved by pole-zero compensation scheme using R_6 and C_6. A reference voltage must be buffered for further use in A/D and D/A converters.

3.2.5 Low noise programmable gain amplifier

The design of low noise programmable gain amplifier is based on fully differential difference amplifier with programmable resistive feedback circuitry. Required average equivalent input referred rms noise voltage density in a band of interest (B ≅ 3.1kHz) can be calculated according to the equation 3:

$$V_n = \frac{\sqrt{2}V_{sig}}{G\sqrt{B}} 10^{\frac{DR+10}{20}} \cong 18\frac{nV}{\sqrt{Hz}} \qquad (3)$$

where V_{sig} = 0.3V is signal swing, G = 20 is required max. gain of the amplifier, B = 3100Hz is a bandwidth, DR = 76.5dB is required dynamic range of the front-end and √2 is added because of fully differential structure. The architecture of the amplifier is similar to the one used for the modulator with the difference of having 2 big differential stages: one used for feedback and the other for input connection. The common mode feedback is realized by resistive divider, separate differential stage and circuit which controls the current through n-channel folded cascode stage. Simplified circuit diagram of this amplifier is presented on figure 10. To reduce thermal noise, current through the differential stage is 300μA and the transistor sizes are 2000um/2um. The microphone amplifier alone consumes 800uA to achieve required noise characteristics

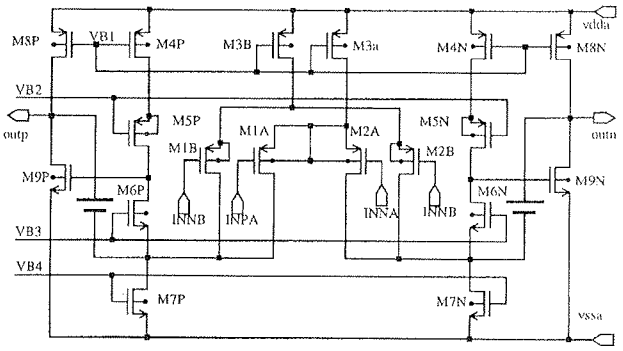

Fig. 10: Simplified circuit diagram of low noise amplifier

(simulation result). The gain is programmable from 0dB to 30dB in 6dB steps. The following characteristics were measured: Vn ≅ 20nV/√Hz which is slightly worse than predicted by the simulations, harmonic distortions at min. gain and max. output signal (0.3V around signal ground) produce HD ≤ -30dB while at bigger gain and smaller input signal the distortions are smaller. Current consumption of amplifier alone was not possible to measure.

4 Conclusions

Design considerations of important modules needed to implement low-power, low-voltage analog front-end, which can be used in various voice integrated circuits are presented in the article. The selection of appropriate architecture and circuit design strategy used during the design phase of some of the modules is presented together with some simulation and measurement results. The operation of the CODEC targeted to V_{sup} = 1.2V is not yet possible for all modules (for example power buffer still need $V_{sup} \geq 1.5V$ for proper operation) and need further innovative effort. The measurement of the complete front-end was thus obtained at $V_{sup} \geq$ 1.5V. Quiescent current consumption is $I_Q \cong 2.5mA$ giving adequate max. dynamic range of DR ≥ 75dB.

REFERENCES

/1/ A.M. Abo and P.R. Gray, "A 1.5V, 10-bit, 14.3 ms/s CMOS pipeline analog-to-digital converter", IEEE JSSC, 34, No.5, 599-606, 1999

/2/ D. Strle, "Noise modeling and simulation of high resolution delta-sigma A/D converters", Proceedings of the 33rd Int. Conference on Microelectronics, Devices and Materials, MIDEM´97, Gozd Martuljek, 157-163, 1997

/3/ D. Strle, "Reduction of Crosstalk in Mixed Signal Integrated Circuits", Proceedings of the International Symposium on VLSI Technology, Systems, and Applications, Taiwan, 74-78, 1997

/4/ D. Strle, A. Pleteršek, K. Riedmuller, T. Karema, "A 2.6V, 20mW, 13-bit CODEC with programmable analogue front-end", Electronic Engineering, 33-36, May 1995

/5/ G.C. Duque, R. Perez, J.M. Valdevere, F. Maloberti, "Fully differential basic building block based on fully differential difference amplifier with unity gain difference feedback", IEEE Trans. on CAS -I, Vol.42, 190-192, March 1995

/6/ H. Banba, H. Shiga, A. Umezava, T. Miyaba, T. Tanzawa, "A CMOS band-gap reference circuit with ssub-1-v operation", IEEE JSSC, 34(5), 670- 226, May 1999

/7/ J.C. Candy, G.C. Themes, "Oversampling methods for A/D and D/A conversion in oversampling delta-sigma converters", IEEE Press, 1991

/8/ R. Gregorian, G.C. Temes, "Analog MOS integrated circuits for signal processing", John Wiley and Sons, 1986

/9/ D.B. Ribner, M.A. Copeland, "Design techniques for cascode CMOS op-amp with improved PSRR and common mode input range", IEEE JSSC, 3, 919-925, Dec. 1984

/10/ B.R. Stanisic, N.K. Verghese, R.A. Rutenbar, L.R. Carley, D.J. Allstot, "Addressing substrate coupling in mixed-mode IC's: simulation and power distribution synthesis", IEEE JSSC, 3, 226-238, March 1994

/11/ Gray K. Yeap, "Practical low power digital VLSI design", Kluwer Academic Publishers, 1998

Dr. Drago Strle
Fakulteta za elektrotehniko in računalništvo
Tržaška 25,
1000 Ljubljana, Slovenia

Prispelo (Arrived): 10.8.99 *Sprejeto (Accepted): 15.9.99*