EXPERIMENTAL DETERMINATION OF THE MOSFET TURN-OFF SNUBBER CAPACITOR

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Key words: turn-off snubber, dc-dc converter, power dissipation, approximation functions, differential evolution method, experiment.

Abstract: This paper presents the analysis and design procedures of snubber circuits for low power dc-dc converters, realised using MOS-FETs. The appropriate design of the snubber circuit can considerably increase the power range, or decrease the total power dissipation of the low-power dc-dc converters available as an integrated circuit. The evaluation of a snubber circuit is based on analysis of the measured currents and voltages, approximated by the continuous functions. The differential evolution method is used to determine the approximation functions unknown coefficients. The results of this proposed method enable the reduction of power dissipation on the transistor while the converter's efficiency remains unchanged. The benefits, drawbacks and limits of the proposed approach are analysed in details. Experimental results are also given, obtained by a laboratory prototype of the boost converter.

Eksperimentalno načrtovanje kondenzatorja v izklopnem razbremenilnem vezju MOSFET-a

Kjučne besede: izklopno razbremenilno vezje, dc-dc pretvornik, preklopne izgube, aproksimacijska funkcija, diferenčna evolucija, eksperiment.

Izvleček: V članku smo predstavili analizo in postopek načrtovanja izklopnega razbremenilnega vezja za dc-dc pretvornike nizkih moči, ki so realizirani z MOS-FET-i. Ustrezno načrtovano razbremenilno vezje lahko pomembno poveča moč ali zmanjša stikalne izgube dc-dc pretvornika nizke moči, ki je na voljo v obliki integriranega vezja. Analiza razbremenilnega vezja temelji na analizi izmerjenih tokov in napetosti, ki smo jih aproksimirali z zveznimi funkcijami. Za določitev neznanih koeficientov izbranih aproksimacijskih funkcij smo uporabili metodo diferenčne evolucije. Iz izraženih analitičnih funkcij smo izračunali potek izklopne energije. Celotna izklopna energija, ki se pretaka med tranzistorjem in razbremenilnim vezjem, je enaka vsoti energije, ki jo absorbira tranzistor in energije, ki jo shrani kondenzator. Potek celotne izklopne energije ima minimum pri izbrani vrednosti kondenzatorja razbremenilnega vezja. Rezultati predlagane metode omogočajo zmanjšanje preklopnih izgub na tranzistorju pri nespremenjenem izkoristku pretvornika. Podrobno smo analizirali prednosti, slabosti in omejitve predlaganega pristopa. Podani so rezultati eksperimenta, ki smo ga izvedli na laboratorijskem prototipu dc-dc pretvornika navzgor.

1. Introduction

Dc-dc converters appear in large numbers of electrical equipment. Most of them are operated in hard switching mode, therefore, they suffer from switching losses. The hard switching operation and reduction of switching losses is discussed in many books and papers relating to these topics (McMurray 1980, Williams 1987, Rashid 1993). Recently basic converter structures such as buck converters, boost converters and buck-boost converters could be realised as chip versions. The switch power losses must be properly evaluated in such cases in order to use the internal chip transistor more efficiently. The snubber circuits are usually placed in the converter structure to adjust the switching-on and switching-off losses. The switching-on snubber circuit is connected in series to limit the *di/dt* at turn-on. The switching-off snubber circuit limits *du/dt* at turn-off.

The approach for evaluation of the switching-off dissipation suggested by (Williams 1987) and (Mohan et al. 1989) is efficiently used in the analysis of BJT-s where current and voltage could be replaced by linear functions. It is, however, less appropriate in the case of MOS-FET, where current and voltage time shapes can not be treated by linear functions.

This paper suggest a modified design approach for a boost converter MOS-FET turn-off snubber circuit based on systematic experimental analysis of losses. The converter's currents and voltages during the switch-off interval are measured for different values of snubber capacitance, and they are approximated by analytical functions to calculate the switching losses. The differential evolution method (Price 1996) is used to determine the approximation functions unknown parameters for currents and voltages. Different energy components in the transistor-snubber system were calculated for different snubber capacitances by analytically given functions for currents and voltages. Analytical functions are also obtained for describing the relationship between calculated energy and snubber capacitance. The obtained analytical relationship enables determination of snubber capacitance according to converter efficiency or transistor dissipation.

2. Description of boost converter and RCD snubber circuit

The boost converter is shown in figure 1. The transistor *Tr* is equipped with a snubber circuit which consists of capacitor C_{CS}, resistor R_S and diode D_S.

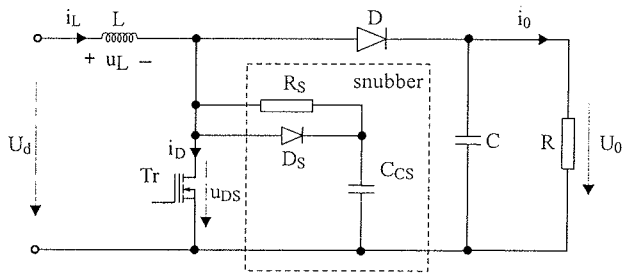

Figure 1. The boost converter with RCD snubber.

The typical waveforms of inductor current i_L, voltage u_L and drain current i_D during the converter operation are shown in figure 2.

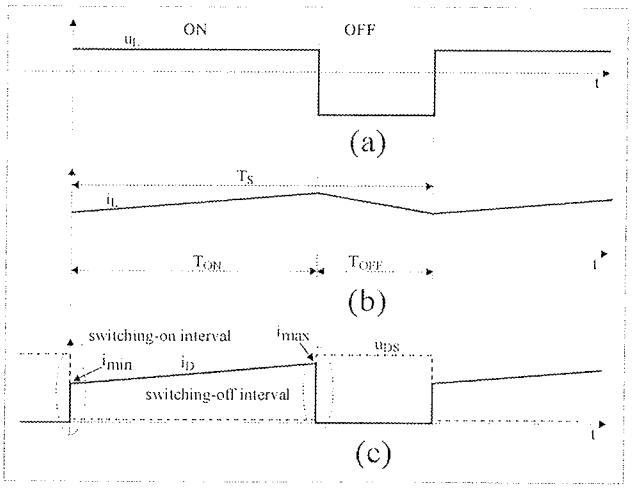

Figure 2. The typical waveforms of the boost converter: (a) the inductor voltage u_L*, (b) the inductor current* i_L*, (c) the transistor current* i_D*.*

A parallel snubber circuit is used to adjust the switching losses during the switching-off interval. The diode D_S connect the capacitor C_{CS} in parallel to the transistor during the switching-off transient. The resistance R_S protects the transistor during switching-on, limiting the discharge capacitor current. On the other hand the R_S must ensure that the capacitor C_{CS} will be completely discharged during the switching-on interval (figure 3b).

The MOS-FET current i_D during the switching-off interval could be considered as constant. At this interval the following can be supposed $i_D = i_{max} = I_D$ (see figure 2). The MOS-FET IRF530, working at the operating point U_{DS} = 8.55 V and I_D = 0.845 A (figures 1 and 2), was used in the experimental part of the analysis. The MOS-FET itself contains some parasitic elements as capacitances C_{GS}, C_{GD} and C_{DS}. The last one must be taken into consideration in the snubber circuit design, although it is not directly stated by the manufacturer in the data sheet. The value of the unknown capacitor C_{DS} is calculated by the suggested method.

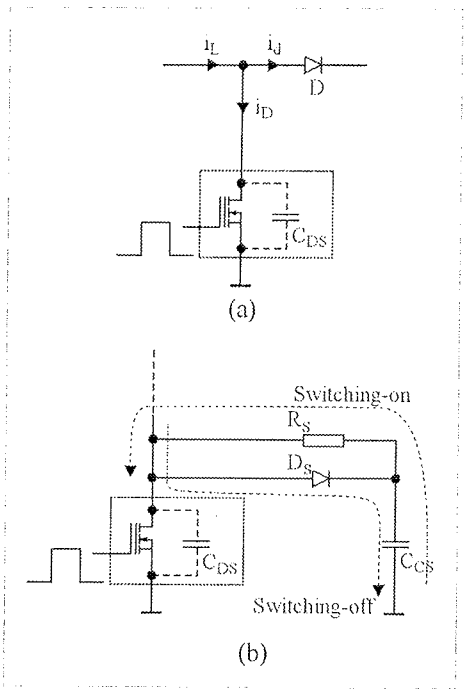

Figure 3. Switching cell of the boost converter: (a) MOS-FET without snubber, (b) the snubber circuit operation.

Measurements were performed by the different values of capacitor C_{CS} (table 1) in the circuit (figure 3b). Current i_D and voltage u_{DS} were measured from the beginning of the switching-off interval at t = 0 to the end of the transition interval at $t_x = 1 \cdot 10^{-6}$ s and they are shown in figure 4.

n	C_{CS}[nF]
1	0
2	2.7
3	3.4
4	7.1
5	10

Table 1. Selected values of snubber capacitors.

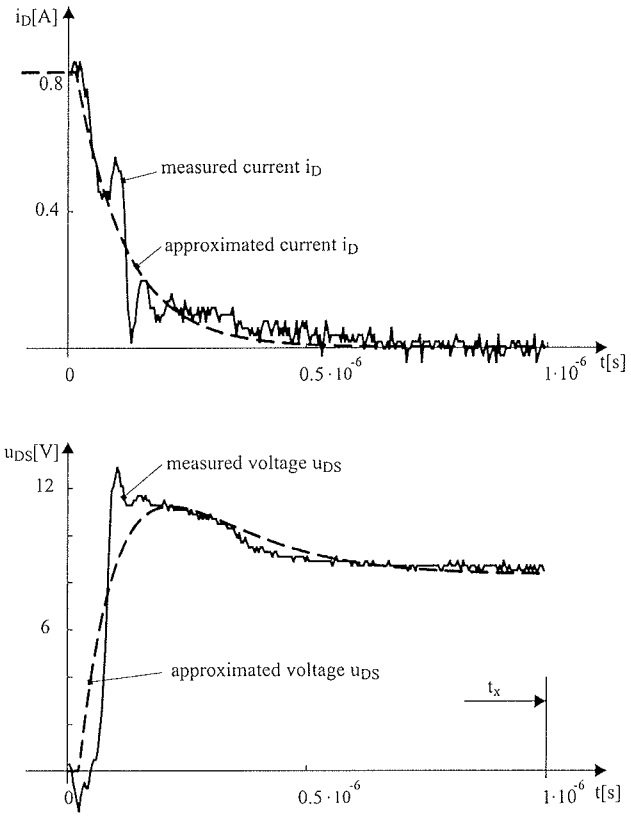

Figure 4. The switching-off transient; measured and approximated currents i_D *and voltages* u_{DS}.

Analytical formulation of measured current and voltage is needed for further analysis of the snubber circuit. It is obvious that both shapes can not be replaced by a linear function, therefore, nonlinear analytical exponential functions with the prescribed structure (1) and (2) are used to calculate the time-dependent current and voltage.

$$i(t) = a_{11} + a_{12}e^{a_{13}t}, \tag{1}$$

$$u(t) = a_{21} + a_{22}e^{a_{23}t} + a_{24}e^{a_{25}t}. \tag{2}$$

The unknown parameters $a_{(.)}$ are calculated separately for the each measured current and voltage pattern using the approximation procedure described in the next section. They are given in Appendix 1. Current i_D and voltage u_{DS} calculated by equations (1) and (2) are shown in figure 4. The agreement between the measured and calculated current and voltage waveforms seems to be acceptable.

The advantage of the analytical description of the measured current and voltage by (1) and (2) is the possibility of further analytical calculation.

3. Calculation of approximation function parameters

Measured current and voltage patterns were approximated by the analytical functions (1) and (2). The parameters $a_{(.)}$ appearing in (1) and (2) were determined by an optimisation method based on differential evolution. Differential evolution is a stochastic search method (Price 1996). The optimisation routine, originally developed for the surface approximation (Težak et al. 2002), was implemented in MATLAB™. The routine inputs are the measured current or voltage patterns. The differential evolution minimisation algorithm is applied to the routine searching the unknown

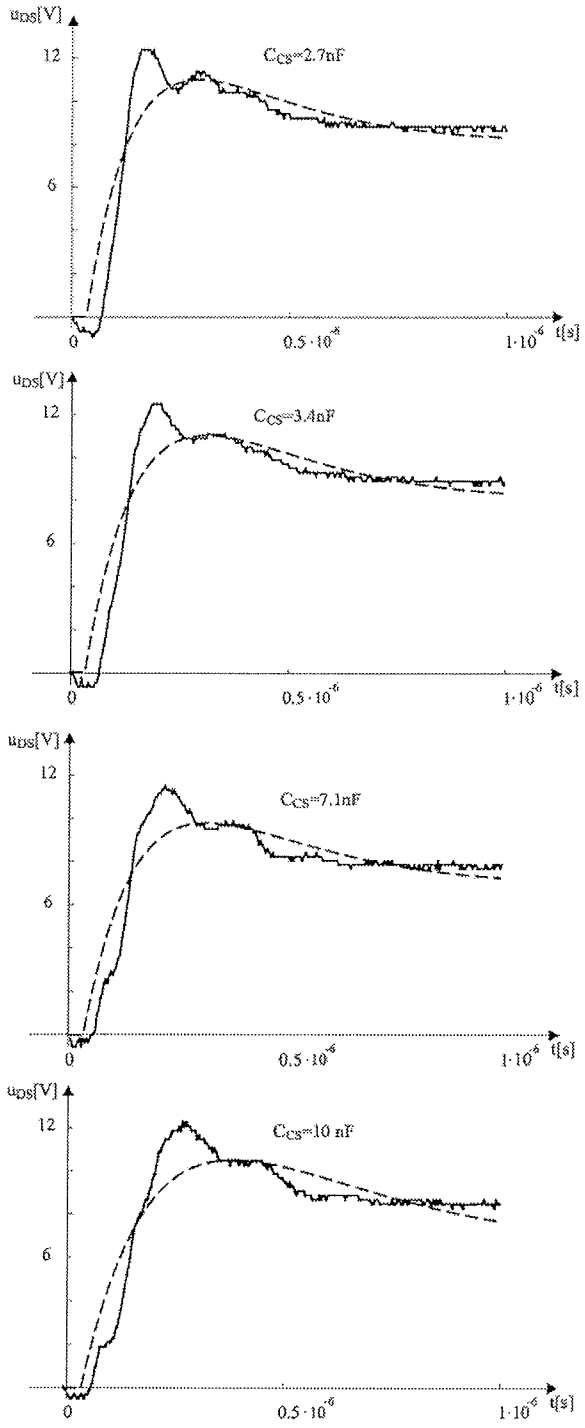

Figure 5. Voltage waveforms for different values of snubber capacitor.

approximation parameters of the selected exponential approximation functions (1) and (2). It is minimising the total error defined as a sum of the squared errors. Error is the difference between the measured and calculated values of current or voltage in the corresponding time sample. The search process is finished when a predefined value of the objective function is reached or when the maximal number of searching steps is achieved. The outputs of the routine are the calculated parameters of equations (1) or (2).

The main advantage of measured results presentation by an analytical function is the possible calculation of function value at any point, and analytical mathematical operations such as multiplication and derivation.

4. Energy consideration

The total switching-off dissipation of the system in figure 3b depends on the value of the parallel capacitance C_S. The capacitance C_S in MOS-FET transistors consists of unknown parasitic capacitance C_{DS} and parallel snubber capacitor C_{CS} , which is given by (3).

$$C_S = C_{CS} + C_{DS} \tag{3}$$

The minimal switching-off dissipation of the whole system can be obtained by the suggested analysis of the total energy absorbed by the MOS-FET and energy stored by the snubber capacitor, which obviously depends on the value of C_{CS}. This energy can be calculated analytically using previously explained approximation functions for the measured currents and voltages, which are measured for the different values of C_{CS}. The first measurement of current and voltage for C_{CS} = 0 nF (n = 1 in table 1) is shown in figure 4. The next four snubber capacitances were chosen around the value C_{CS} = 7.1 nF, which were calculated according to the procedure suggested by (Williams 1987) (n = 4 in table 1). The capacitors were selected so that one of them was higher than it (10 nF) and two of them were smaller than it (2.7 nF and 3.4 nF). The performed calculated energy analyses showed, that the calculated capacitance C_{CS} = 7.1 nF did not minimise the switching-off losses.

Four additional measurements of currents and voltages for the values of capacitance 2.7, 3.4, 7.1 and 10 nF were done afterwards. The current wave-shapes in all cases remained almost equal to the one in figure 4, as was expected. The measured voltage wave-shapes are given in figure 5 and they depend on the connected capacitance C_{CS}. The energy W_S stored in the capacitance C_S at the end of switching-off interval is calculated by equation (4) in the continuous time domain or by equation (5) in the discrete time domain:

$$W_S = \int_0^{t_x} u_{DS} \cdot i_{C_{DS}} dt \tag{4}$$

$$W_S = \sum_{k=0}^{m} u_{DS}(k) \cdot i_{C_{DS}}(k) \cdot T_s,\ T_s = \frac{t_x}{m} \tag{5}$$

where the parasitic capacitance current $i_{C_{DS}}$ was calculated by $i_{C_{DS}} = I_D - i_D - i_d$, as follows from figures 2c and 3a, and T_S is the sampling time. Currents i_D, i_d and voltage u_{DS} are measured instantaneous values of MOS-FET (Tr) drain and diode (D) currents and drain source voltage, respectively. Currents and voltages are measured by Tektronix TDS4000 and are available as data series.

Parasitic capacitance C_{DS} can be determined by equation (6), taking into account that $W_S = W_{DS}$ when $C_{CS} = 0$:

$$C_{DS} = C_S\big|_{C_{CS}=0} = \frac{2\,W_S\big|_{C_{CS}=0}}{U_{DS}^2} \tag{6}$$

where U_{DS} is the steady state value of drain source voltage on the MOS-FET, and C_{CS} is the snubber capacitance.

Further analysis of switching losses is based on the known value of parasitic capacitance C_{DS}, therefore, it has to be determined first. The energy W_S stored in the parasitic capacitance C_{CS} is calculated by (5) which gives $W_S(C_{CS}=0)$=0.04752 μJ; capacitance C_{DS}=1.3 nF is calculated afterwards by (6).

The energy W_{Tr} supplied to the system during the switching-off interval is calculated as energy absorbed by transistor, either by equation (7) in the continuous time domain or by equation (8) in the discrete time domain.

$$W_{Tr} = \int_0^{t_x} u_{DS} \cdot i_D dt \tag{7}$$

$$W_{Tr} = \sum_{k=0}^{m} u_{DS}(k) \cdot i_D(k) \cdot T_s,\ T_s = \frac{t_x}{m} \tag{8}$$

The total energy W_{TOT} absorbed in the system during the switching-off process is obtained as a sum of the energy stored in the snubber capacitor W_{CS}, and the energy absorbed by transistor W_{Tr} using equation (9) for five different values of capacitors C_{CS} (see table 1).

$$W_{TOT} = W_S + W_{Tr}. \tag{9}$$

The above-mentioned energies were calculated using equations (4) to (9). These results are shown in tables 2 and 3. The energy values in table 2 are calculated directly from the measured current and voltages. The energies in table 3 are calculated by using approximation functions of currents and voltages, which are plotted by the dashed lines in figures 4 and 5. The disturbing influence of the measuring noise on the calculated energy has been eliminated using the described method in which the determined analytical functions are used to calculate the energy. The corresponding values of W_{CS} in table 2 and 3 are the same, because they are calculated from the steady state value of voltage U_{DS} , which is the same in all cases (U_{DS}=8.55V). The values of W_{Tr} shown in table 2 differ slightly from that ones in table 3, because they were calculated by the measured currents and voltages containing noise. The differ-

ence between results in tables 2 and 3 is indeed negligible, therefore, the results from table 3 will be used further on.

C_S[nF]	W_S[μJ]	W_{Tr}[μJ]	W_{TOT}[μJ]
1.3	0.04752	0.91034	0.9579
4	0.14621	0.77014	0.9164
4.7	0.17179	0.78189	0.9537
8.4	0.30703	0.69078	0.9978
11.3	0.41303	0.69115	1.1042

Table 2. Calculated values of energy (calculated directly by measured data).

C_S[nF]	W_S[μJ]	W_{Tr}[μJ]	W_{TOT}[μJ]
1.3	0.04752	0.91193	0.9595
4	0.14621	0.78064	0.9268
4.7	0.17179	0.78861	0.9604
8.4	0.30703	0.70085	1.0079
11.3	0.41303	0.68446	1.0975

Table 3. Calculated values of energy (calculated by approximation functions).

The values of total energy W_{TOT} and the energy absorbed by transistor W_{Tr}, taken from table 3, are indicated by the cross marks of the graph in figure 6. The marked energies were approximated by analytical functions (10) and (11) in a similar way as was done by the basic functions (1) and (2) for the measured currents and voltages in section 2.

$$W_{TOT}(C_S) = b_{11} + b_{12}e^{b_{13}C_S} + b_{14}e^{b_{15}C_S} \qquad (10)$$

$$W_{Tr}(C_S) = b_{21} + b_{22}e^{b_{23}C_S}. \qquad (11)$$

The values of the calculated coefficients $b_{(.)}$ for $W_{TOT}(C_S)$ and $W_{Tr}(C_S)$ are given in appendix 2. Calculated functions $W_{Tr}(C_S)$ and $W_{TOT}(C_S)$ from the data in table 3 are shown in figure 6 as solid lines. It is necessary to note that it is impossible to obtain the energy value for the capacitance $C_S < C_{DS}$ by the measurement of current and voltage, because parasitic capacitance C_{DS} in case of MOS-FETs is always different to zero. The values of both functions $W_{Tr}(C_S)$ and $W_{TOT}(C_S)$ at point C_S = 0 nF can be obtained by the extrapolation of functions (10) and (11) to the hypothetical point where $W_{Tr} = W_{TOT}$. The dashed lines in figure 6 were obtained by the above-mentioned extrapolation.

The value $W_{TOT}(C_S = 0)$ = 1.001 μJ is used as a base for normalization further on.

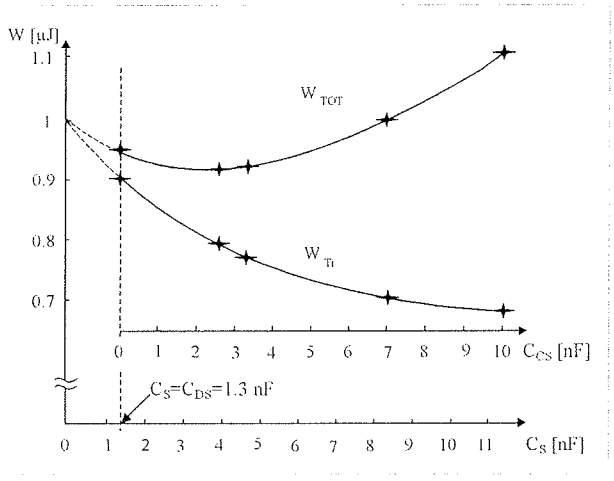

Figure 6. Graph of functions $W_{TOT}(C_S)$ and $W_{Tr}(C_S)$

Per-unit (p.u.) values of energy from table 3 are shown in table 4. The energies are normalised by the energy $W_{TOT}(0) = W_{TOT}(C_S = 0)$ using equation (12).

$$w_{TOT} = \frac{W_{TOT}}{W_{TOT}(0)}, \quad w_{Tr} = \frac{W_{Tr}}{W_{TOT}(0)} \qquad (12)$$

C_S[nF]	w_S	w_{Tr}	w_{TOT}
0	0	1	1
1.3	0.04747	0.9112	0.9585
4	0.14606	0.77986	0.9259
4.7	0.17162	0.78782	0.9594
8.4	0.30672	0.70015	1.0069
11.3	0.41262	0.68378	1.0964

Table 4. Calculated values of normalised energy (calculated by approximation functions).

As the total energy functions $w_{TOT}(C_S)$ and $w_{Tr}(C_S)$ are analytical functions of the form (10) and (11) with the known parameters , the minimum of $w_{TOT}(C_S)$ can be calculated analytically by the expression (13).

$$\frac{d\,w_{TOT}(C_S)}{dC_S} = 0 \quad \Rightarrow \quad C_S = 3.4\,nF \qquad (13)$$

The minimum of the total energy w_{TOT} in point "O" (figure 7) is reached by the capacitance C_S = 3.4 nF which gives the snubber capacitor C_{CS} = 2.1 nF, due to equation (3).

The dissipation decrease Δw_{TOT} at point "O" in figure 7 is around 6%, while the dissipation decrease Δw_{Tr} on the transistor is around 20 %. Moreover, if the snubber capacitance C_{CS} = 6.5 nF is used, the efficiency of the converter at point "P" is exactly the same as in the hypothetical case where C_S = 0 nF. However, the transistor dissipation w_{TOT} is decreased by almost 30 %.

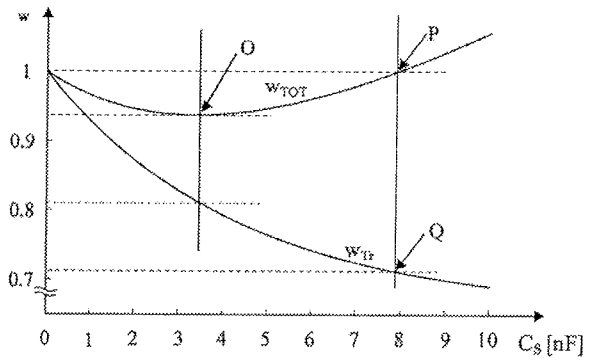

Figure 7.Graphs of normalised functions $w_{TOT}(C_S)$ *and* $w_{Tr}(C_S)$

5. Conclusion

The proper design of a snubber circuit can considerably decrease the total power dissipation on the transistor. The methods for the evaluation of switching-off dissipation suggested in the literature are inappropriate in the case of MOS-FETs, because of the presumption that current and voltage during the switching-off interval can be expressed by a linear function. A new approach to the design of snubber circuits for low power dc-dc converters, based on the experimental analysis of measured currents and voltages is suggested in this paper. Currents and voltages are measured for different values of snubber capacitance and they are approximated by the corresponding analytical functions, in a way that the difference between measured and calculated values becomes minimal in the quadratic sense. The energy values are calculated for the different snubber capacitances by analytically given currents and voltages. The function describing relationship between the energy and the snubber capacitance is also determined by an approximation. The obtained analytical function enables calculation of proper snubber capacitance regardless of whether the MOS-FET switching-off dissipation or total switching-off dissipation of the snubber circuit is minimised. The only disadvantage of the suggested method is that a certain number of current and voltage measurements are required. The objective of future work will be finding out relationships between the parameters of approximation functions for energy and the MOS-FET data from the data sheet directly, to avoid extensive measuring and calculations.

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Appendix 1

Coefficients $a_{(.)}$ of the equations (1) and (2).

a_{11}	a_{12}	a_{13}
0.028357	0.93109	-9452981.3417

n	C_{CS} [nF]	$a_{n+1,1}$	$a_{n+1,2}$	$a_{n+1,3}$	$a_{n+1,4}$	$a_{n+1,5}$
1	0	8.3082	-9177.9403	-8142542.4133	9164.3296	-8127151.164
2	2.7	8.176	-12610.1669	-6149625.3087	12596.7656	-6141240.3854
3	3.4	8.052	-12919.3637	-5613668.9851	12906.3012	-5606118.774
4	7.1	7.5534	-10200.2252	-5376230.2305	10188.0022	-5367087.3051
5	10	6.5299	-9817.926	-4035161.8147	9807.0537	-4027274.4877

Appendix 2

Coefficients $b_{(.)}$ of the equations (10) and (11).

b_{11}	b_{12}	b_{13}	b_{14}	b_{15}
$414.489\ 10^{-6}$	$-413.859\ 10^{-6}$	$-9.2579\ 10^{-5}$	$0.36945\ 10^{-6}$	-0.21646

b_{21}	b_{22}	b_{23}
$0.6561\ 10^{-6}$	0.3429310^{-6}	-0.23016

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