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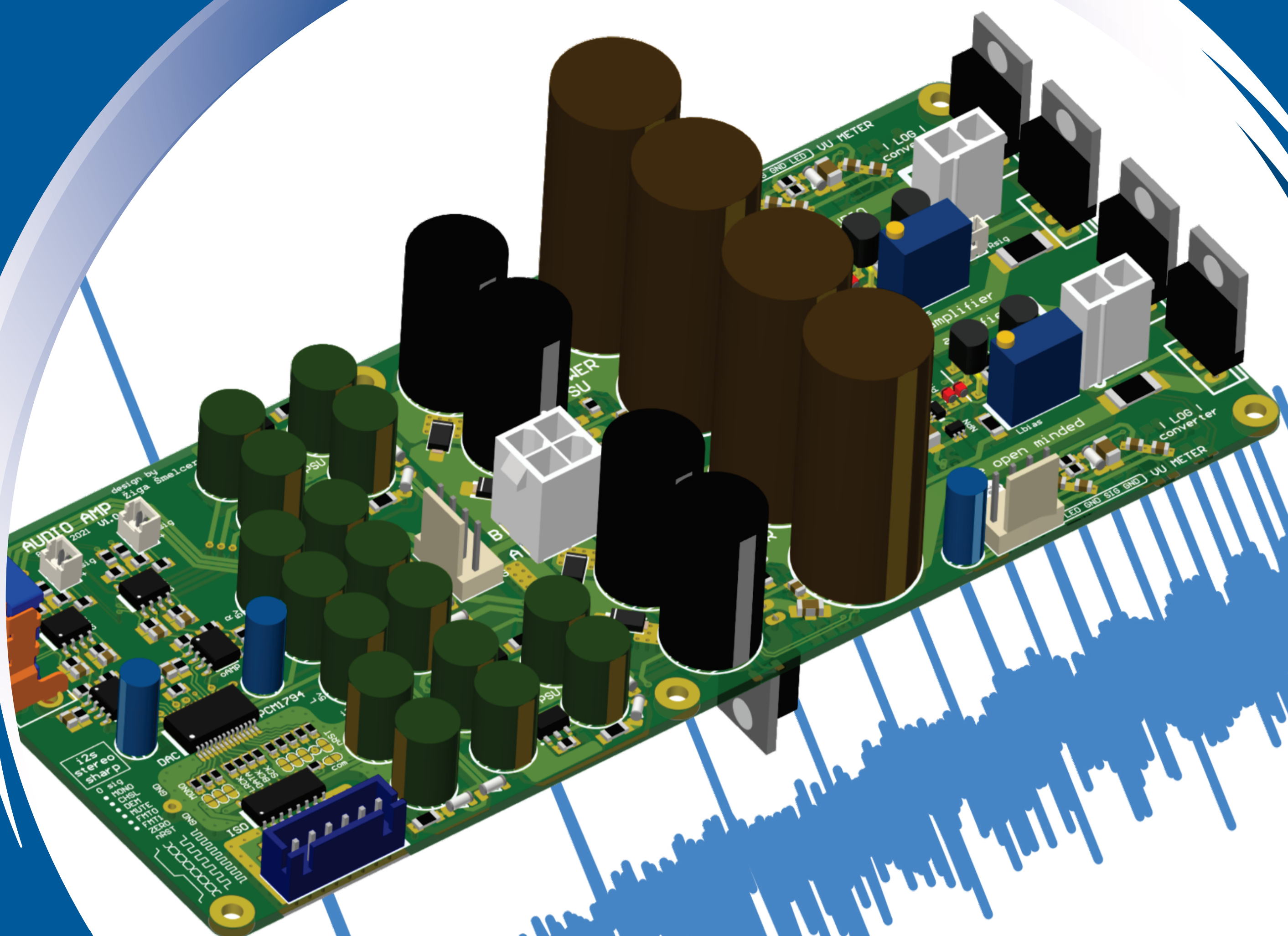

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Five-Level Transformerless Common Ground Type Inverter with Reduced Device Count

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Abstract: In recent days, the transformerless grid-connected PV inverter is paid more attention due to its compactness and high efficiency with low cost. This paper presents a new five-level transformerless switched capacitor type inverter with a reduced number of power components. The proposed topology has a lower number of power components with a common ground connection between the negative terminal of the input side and load that eliminates the leakage current. The switched capacitors do not require any sensors for their balancing. The different modes of operation and control of the PWM technique are discussed. The proposed topology is compared with recent transformerless inverters, and the advantages of the proposed topology are highlighted. The simulation and experimental results are presented. The prototype hardware setup is built for 1.2 kW and has the simulated maximum efficiency of 96.4%. The performance of the proposed topology is measured by applying various load and modulation index variations.

Keywords: Common ground; Leakage current; Multilevel inverter; Transformerless inverter; Switched capacitor

Petstopenjski pretvornik brez transformatorja s skupno ozemljitvijo in manjšim številom naprav

Izvleček: V zadnjih dneh se zaradi kompaktnosti in visoke učinkovitosti ob nizkih stroških več pozornosti namenja breztransformatorskim PV pretvornikom, ki so priključeni na omrežje. V tem članku je predstavljen nov petstopenjski breztransformatorski razsmernik s stikalnim kondenzatorjem z zmanjšanim številom močnostnih komponent. Predlagana topologija ima manjše število močnostnih komponent s skupno ozemljitveno povezavo med negativno sponko vhodne strani in bremenom, ki odpravlja uhajalni tok. Preklopni kondenzatorji ne potrebujejo senzorjev za uravnoteženje. Obravnavani so različni načini delovanja in krmilne tehnike PWM. Predlagana topologija je primerjana z novejšimi breztransformatorskimi pretvorniki, poudarjene pa so tudi prednosti predlagane topologije. Predstavljeni so simulacijski in eksperimentalni rezultati. Prototipna strojna oprema je izdelana za 1,2 kW in ima simulirano največjo učinkovitost 96,4 %. Učinkovitost predlagane topologije je izmerjena z različnimi spremembami obremenitve in modulacijskega indeksa.

Ključne besede: skupna zemlja; uhajalni tok; večnivojski razsmernik; breztransformatorski razsmernik; preklopni kondenzator

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1 Introduction

The PV system is a more promising renewable energy source because of no greenhouse gases, pollution-free, clean, return on investment, and emission-free. Various advantages like reliability, the noiseless operation makes the photovoltaic system a more attractive and promising renewable energy source. Such a photovoltaic system with grid integration can be done generally through galvanic isolation, which is transformer-based and non-galvanic isolation which is a transformerless

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based method [1]. The high-frequency transformer on the DC side and line transformers on the AC side ensures safer operation in the existing system. But the use of transformer leads to decrease in efficiency, more weight, high cost and power losses, need regular maintenance and bulky size. To overcome the drawbacks of transformer-based galvanic isolation, transformerless inverter topologies are developed. The transformerless inverters offer high efficiency, compactness, and low leakage current. However, the power quality concern, output voltage distortion and safety due to the leakage current, isolation capabilities are the main predicament in grid-connected transformerless inverter-based PV systems. Many types of transformerless inverters have been developed to reduce the leakage current [2]. The MLI inverter proposed in [3] has the ability of self-voltage balancing and boosting for the grid-connected renewable energy system. The source of leakage current is a common-mode voltage which can be minimized by proper selection of switching sequence. Parasitic capacitance i.e., stray capacitance is usually appearing between photovoltaic panels negative terminal and neutral side of the grid. In a non-galvanic i.e., transformerless inverters a direct ground current path is developed between the PV and grid grounds. The variable high-frequency common mode voltage (CMV) of the inverter where it can be clamped between the null of ac grid and the parasitic capacitor of the PV arrays negative terminal excites the resonant circuit formed by parasitic capacitor and inverter filer inductor, which produces leakage current. By connecting negative terminal of PV side and neutral of grid side, the CMV will be cancelled out since the parasitic capacitance is clamped to ground potential. Hence, the leakage current can be eliminated [5]. The CMV can be maintained constantly through PWM controlling techniques, decoupling the photovoltaic and grid to reduce the leakage current. There are some methods to mitigate the leakage current.

Suppressing the leakage current problem is possible with the grid neutral terminal's direct connection with the negative PV terminal. This direct connection of grid neutral and PV negative terminal called common ground type transformerless inverters results in zero leakage current. Many topologies have been proposed to minimize the leakage current value. Still, each having has disadvantages like the higher switch count, the high voltage stress on the capacitor and the larger size of the capacitor [6]. The topology developed [7] has four topological variants with high dc-bus utilization and constant total common-mode voltage. By providing the DC and AC decoupling in inverter circuit will reduce the leakage current. A new DC decoupling inverter topology with less power components is proposed to reduce leakage current [9]. However, the complete elimination of leakage current is not achieved by decoupling methods due to its dc bus utilization limit. A switched-capacitor inverter with a common ground type is presented in [11]. The switched capacitor acts as a virtual dc-link, and this is charging in the positive half cycle and discharging at the negative half cycle. A simple peak current controller controls the output current. A common ground type topology with flying capacitor leg plus a half-bridge cell is presented in [12], gives superior performance in terms of harmonic distortion, thus allowing filter reduction. The multilevel transformerless half-bridge topology is presented in [13]. This topology can inject reactive power into the grid, thereby making it low voltage ride-through capability LVRT.

A virtual dc bus concept with feedforward space vector modulation technique is presented in [14]. The modulation strategy decouples the output variables from voltage capacitor oscillations, thus providing a low output current THD, and this is independent of the size of dc capacitors. Asymmetrical T-type common ground transformerless inverter is proposed in [15]. The EMI filter design and the modulation scheme allow the reduction of leakage current with high efficiency. Various methods have been introduced to minimize the leakage current in transformerless inverters. The common ground transformerless inverter topologies are efficiently eliminating the leakage current [5], [11], [14]. Although common ground transformerless inverters have numerous benefits, they also have certain drawbacks, such as the requirement for additional protection circuits due to high inrush current and the discontinuous nature of input current. This article proposes a new six switch one diode five-level 6S-1D-5L transformerless inverter topology with a common ground. The

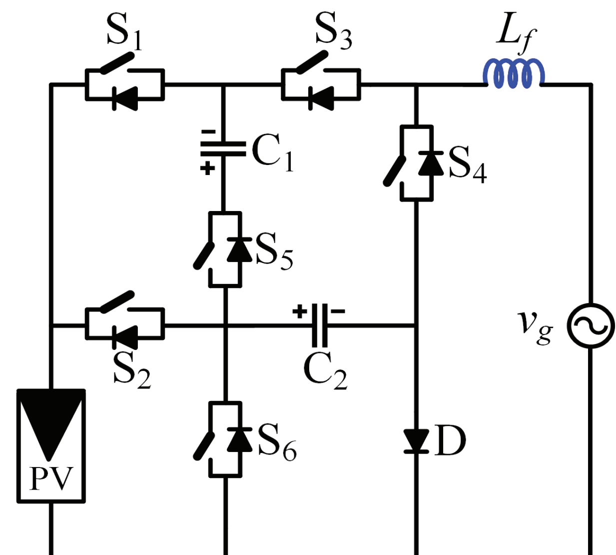

Figure 1: Circuit diagram of proposed 6S-1D-5L Topology.

proposed topology has significant advantages like low capacitor voltage stress and low power device.

2 Description and its operating principle

2.1 Description of 6S-1D-5L inverter topology

The power circuit of the proposed 5L-Inverter topology is shown in Fig. 1. The proposed topology comprises six switches (S_1, S_2, S_3, S_4, S_5 and S_6), two capacitors C_1 & C_2 and one diode D for five-level voltage output. The voltage rating of the capacitors C_1 and C_2 are $0.5v_{in}$ and v_{in}, respectively. The C_1 and C_2 are charging in the positive half cycle and discharging in the negative half cycle. The negative terminal of the load is directly connected to the dc source negative terminal, which is called common ground.

A few highlights of the new 6S-1D-5L inverter are,

- The proposed topology has few power components.
- The capacitors voltages are self-balanced and do ot require any additional sensors.
- The number of ON-state switches is less.
- Maximum voltage stress across the switch is equal to $1.5V_{in}$.
- Total capacitor voltage stress is reduced.
- No leakage currents.

2.2 Description of 6S-1D-5L inverter topology

Different switching Levels (Level 1 to Level 5) that generate five levels of the output voltage waveform of the proposed inverter and the switching sequence are listed in Table 1. The analysis of voltage stress and current stress of all the switches is summarized and shown in Table 2 and Table 3. The switch S_1 blocks the sum of the voltage across the C_1 and dc source voltage, and this S_1 has to withstand the maximum voltage, i.e., 1.5 V_{in}. The maximum current flow through the switch S_3. During the positive half cycle, the C_2 capacitor is connected in parallel to dc source through switch S_3, and it draws more charging current.

Table 1: Operating levels of the proposed topology.

Levels	Conducting Switches						FCs Status	
	S_1	S_2	S_3	S_4	S_5	S_6	C_1	C_2
V_{in}	1	1	1	0	0	0	-	↑
0.5 V_{in}	0	1	1	0	1	0	↑	↑
0	0	1	0	1	0	0	-	↑
-0.5 V_{in}	0	0	1	0	1	1	↓	-
$-V_{in}$	0	0	0	1	0	1	-	↓

Table 2: Voltage stress of switches

Levels	Switches					
	S_1	S_2	S_3	S_4	S_5	S_6
V_{in}	0	0	0	1	0.5	1
0.5 V_{in}	0.5	0	0	0.5	0	1
0	0	0	0.5	0	0	1
-0.5 V_{in}	1.5	1	0	0.5	0	0
$-V_{in}$	1.5	1	1	0	0.5	0

The blue line and red line in Fig. 2 indicate the current flow from source to load and vice versa.

Level 1: ($V_0 = V_{in}$): During this level of operation, the switches S_1, S_2 and S_3 are switched ON. The capacitor C_2 is charged during this output voltage level. The respective level is shown in Fig. 2a.

Table 3: Current stress of switches

Levels	Switches					
	S_1	S_2	S_3	S_4	S_5	S_6
V_{in}	I_{L1}	I_L- I_{L1}	I_{L1}	0	0	0
0.5 V_{in}	0	I_L	I_{L2}	0	I_{L2}	0
0	0	0	0	I_{L3}	0	0
-0.5 V_{in}	0	0	I_{L4}	0	I_{L4}	I_{L4}
$-V_{in}$	0	0	0	I_{L5}	0	I_{L5}

Level 2 :(V_0 = $0.5V_{in}$): The switches S_2, S_3 and S_5 are switched ON to generate the output voltage of V_0 = $0.5V_{in}$. The respective level is shown in Fig. 2b. In this operating level, the capacitors C_1 and C_2 are charged to $0.5V_{in}$ and V_{in}.

Level 3:(V_0= 0): The switches S2, and S4 are ON. The output voltage in this level is V0 = 0. The respective level is shown in Fig. 2c.

Level 4: (V_0 = $-0.5V_{in}$) The switches S_3, S_5 and S_6 are switched ON to generate the output voltage of V_0 = $-0.5V_{in}$. The respective level is shown in Fig. 2d. In this operating level, the capacitor C_1 is discharged.

Level 5: (V_0 = $-V_{in}$): The switches S_4 and S_6 are switched ON to generate the output voltage of V_0 = $-V_{in}$. The respective level is shown in Fig. 2e. In this operating level, the capacitor C_2 is discharged.

3 PWM Modulation technique

Several modulation schemes have been developed to generate stepped output voltage levels in MLIs. The

pulse width modulation technique is classified as a low-frequency switching scheme and a high-frequency switching scheme based on the switching frequency. The multi-carrier level-shifted pulse width modulation technique is one of the familiar modulation methods. For the proposed 6S-1D-5L inverter topology, alternate phase opposition disposition pulse width modulation (APOD-PWM) has been employed, which is shown in Fig. 3a. The carrier signals V_c are compared with a sinusoidal reference signal V_{ref} to generate gate signals. For the proposed inverter topology, the alternate phase opposition disposition pulse width modulation employs four carrier signals, two on the positive side and two on the negative side, compared with the sinusoidal reference signal V_{ref}. The logic scheme to generate the gate

pulses for switches are shown in Fig. 3b. The modulation index is an important factor that supports to control of the load voltage, and it is defined as:

$$\mathrm{MI} = \frac{\mathrm{V_{ref}}}{2 \times \mathrm{V_c}}, \mathrm{V_o} = \mathrm{M} \times \mathrm{Vin} \tag{1}$$

The logical expression for the gating signals is expressed as:

$$S_1 = A_3 \tag{2}$$

$$S_2 = A_1 + A_2 \tag{3}$$

$$S_3 = A_2 + A_4 A_5 ' \tag{4}$$

$$S_4 = A_1 + A_5 \tag{5}$$

$$S_5 = A_4 \tag{6}$$

$$\mathrm{S_6} = \mathrm{A_2 A_3}' + \mathrm{A_4 A_5}' \tag{7}$$

4 Power loss analysis

The equivalent circuit of the proposed 6S-1D-5L topology is shown in Fig. 4a. The equivalent circuit is derived by replacing the switches and capacitors with their equivalent internal resistances. In the equivalent circuit R_{sr}, R_{esr}, R_L and R_d indicate the internal resistance of individual switch, the resistance of the capacitor, the resistance of the load, and the diode resistance.

4.1 Conduction loss

The conduction losses are calculated by multiplying the on-state voltage drop of the switch and the conduction current. The total conduction losses have been calculated with pure resistive load at a steady state. All

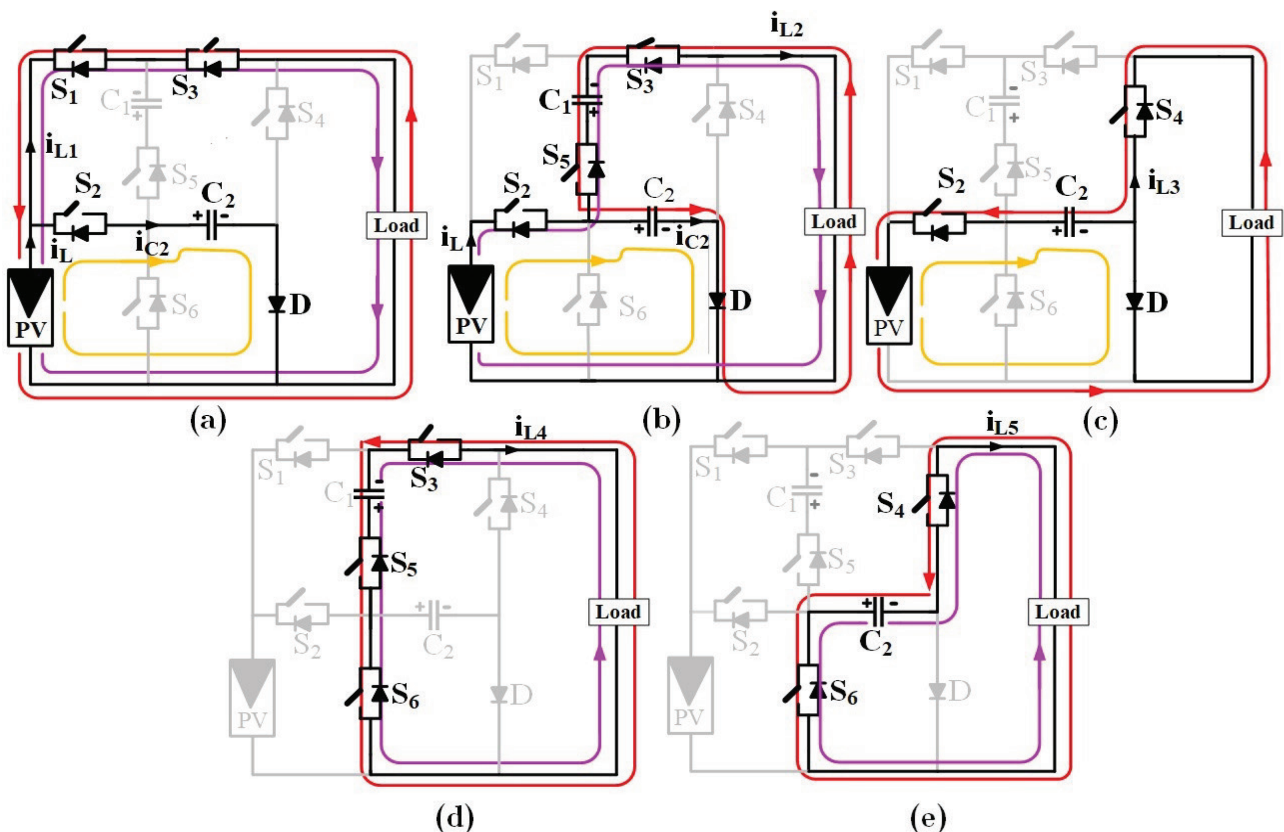

Figure 2: Switching levels of proposed inverter topology.

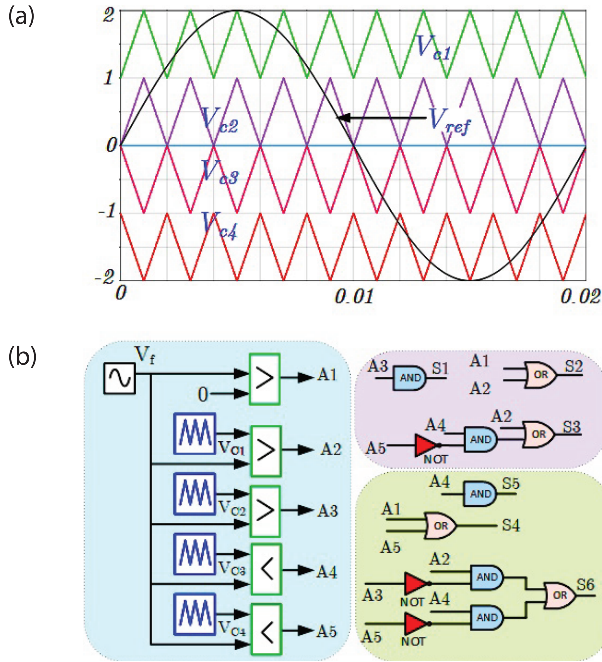

Figure 3: Modulation Technique (a) APOD PWM methods and (b) Logic Diagram

working levels of the proposed topology are considered and its equivalent circuit is shown in Fig. 4(b-e) to calculate the maximum conduction loss. Pure resistive loading condition is considered because there should not exist any auxiliary current path between load current and output voltage to facilitate the charging of capacitors. Therefore, the resistive loading condition is considered the worst condition for calculating losses in switched capacitor-based multi-level inverters [8].
From equivalent circuit of Fig. 4b during V_0=V_{in}:

$$I_{dc} = I_{charging} + I_{L1} \tag{8}$$

Where I_{L1} is the load current during V_0=V_{in}.

From equivalent circuit of Fig. 4c during V_0=0.5V_{in}:

$$I_{dc} = I_{charging} + I_{L2} \tag{9}$$

Where I_{L2} is the load current during V_0=V_{in}.

From equivalent circuit of Fig. 4d:

$$I_{dischargingC1} = \frac{V_{C1}}{R_{esr} + 3R_{sr}} \tag{10}$$

From equivalent circuit of Fig. 4e:

$$I_{dischargingC2} = \frac{V_{C2}}{R_{esr} + 2R_{sr}} \tag{11}$$

By applying Kirchhoff's voltage law and Kirchhoff's current law to equivalent circuits of Fig. 4(b-e), the instantaneous value of conduction losses can be calculated using as follows:

$$P_{C1} = 2R_{sr}\left(I_{L1}\right)^2 + (R_{sr} + R_{esr})\left(I_{charging}\right)^2 \tag{12}$$

$$P_{C2} = R_{sr}\left(I_{dc}\right)^2 + \left(R_{esr} + R_d\right)\left(I_{charging}\right)^2 + (2R_{sr} + R_{esr})\left(I_{L2}\right)^2 \tag{13}$$

$$P_{C3} = (R_{esr} + 3R_{sr})\left(I_{discharging}\right)^2 \tag{14}$$

Where $I_{discharging}$ represents the capacitor C_1 discharging current.

$$P_{C4} = (R_{esr} + 2R_{sr})\left(I_{discharging}\right)^2 \tag{15}$$

Where $I_{discharging}$ represents the capacitor C_2 discharging current.

The average conduction loss for one complete cycle of output voltage waveform is calculated by using related time interval. From Fig. 5, the time interval for V_{in}, 0.5V_{in}, -0.5V_{in} and -V_{in} is (t_3-t_2), (t_2-t_1), (t_7-t_6), and(t_8-t_7). By using the calculated instantaneous conduction loss, the average value of conduction loss is calculated as:

$$P'_{C1} = \frac{2}{T_{f0}} P_{C1}\left(t_3 - t_2\right); P'_{C2} = \frac{2}{T_{f0}} P_{C2}\left(t_2 - t_1\right)$$

$$P'_{C3} = \frac{2}{T_{f0}} P_{C3}\left(t_7 - t_6\right); P'_{C4} = \frac{2}{T_{f0}} P_{C4}\left(t_8 - t_7\right)$$

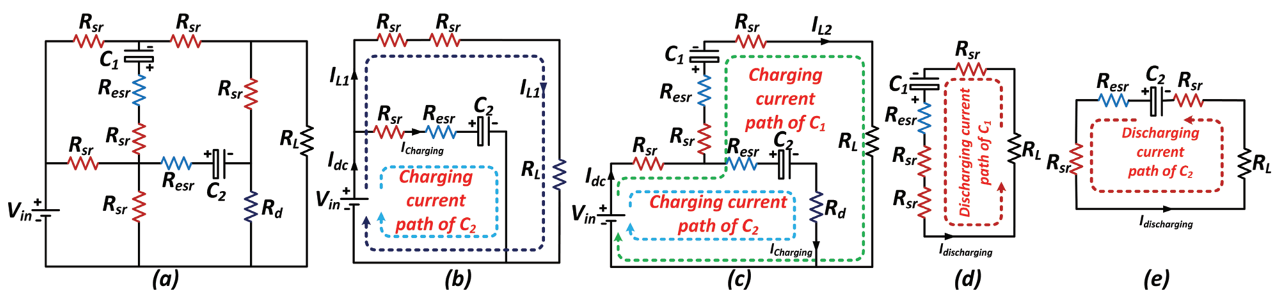

Figure 4: Equivalent circuit (a) Proposed circuit (b) $V_o = V_{in}$ (c) $V_o = 0.5V_{in}$ (d) $V_o = -0.5V_{in}$ (e) $V_o = -V_{in}$

The total conduction loss can be calculated using (16):

$$P_C = P_{C1}' + P'_{C2} + P'_{C3} + P'_{C4} \tag{16}$$

P_{C1}, P_{C2}, P_{C3}, and P_{C4} are instantaneous values of conduction losses and P'_{C1}, P'_{C2}, P'_{C3}, P'_{C4} are average values *of* conduction losses over one complete cycle.

4.2 Switching loss

The switching of semiconducting devices during turn-on and turn-off transitions are termed switching losses. The switching losses can be obtained by integrating the voltage and the current on the particular switching period. Here the switching losses can be calculated using linear polynomial approximation.

The energy dissipated during turn-on period of a semiconductor switch is:

$$E_{on} = \int_0^{T_{on}} V(t) \times I(t)\, dt \tag{17}$$

$$= \int_0^{T_{on}} \left(V_{swon} \times \frac{T}{T_{on}}\right) \times \left(\frac{-I_1 \ (T\text{-}T_{on})}{T_{on}}\right) dt = \frac{V_{swon} \times I_1 \times T_{on}}{6} \tag{18}$$

Where V_{swon} is the on-state voltage on the switch, I_1 is the current through the switch after turning on, T_{on} is the turn-on time of the semiconductor switch.

The energy dissipated during turn off period of a semiconductor switch is:

$$E_{off} = \int_0^{T_{off}} V(t) \times I(t) dt \tag{19}$$

$$= \int_0^{T_{off}} \left(V_{swoff} \times \frac{T}{T_{off}}\right) \times \left(\frac{-I_1 \ (T\text{-}T_{off})}{T_{off}}\right) dt = \frac{V_{swoff} \times I_2 \times T_{off}}{6} \tag{20}$$

Using fundamental frequency switching method, the total switching loss is estimated using (21):

$$P_{switch} = f \times \left(N_{on} E_{on} + N_{off} E_{off}\right) \tag{21}$$

Where , N_{on} is the number of turn ON switches, and N_{off} is the number of turns OFF switches during one fundamental cycle.

4.3 Capacitor Ripple Loss

The difference between capacitor voltage and the input voltage results in capacitor ripple losses [8], [10]. The capacitor ripple voltage is calculated using the equation (22):

$$\Delta V_{c_i} = \frac{1}{C_i} \int i(t)\, dt \tag{22}$$

Where C_i is the capacitance value, *i(t)* is the current flowing through the capacitors. Hence, from the longest discharge duration capacitors, the capacitor ripple loss over a cycle is calculated as:

$$P_{ripple} = \frac{f}{2} \times C \times (\Delta V_C)^2 \tag{23}$$

$$\Delta V_{C1} = \frac{I_p}{C_1 \times f_{sw}} \tag{24}$$

$$\Delta V_{C2} = \frac{I_{pm}}{\pi \times f \times C_2} \left[\cos\left(\frac{\pi}{3} - \theta\right) - \sin\theta\right] \tag{25}$$

4.4 Inductor Loss

In inductors, the total losses are depending on two losses a) copper loss and b) iron losses. For the output filter inductor, the loses are expressed as [14]:

$$P_{cu} = \left(i_L\right)^2 R_L \tag{26}$$

$$P_{core} = k f^{\alpha} V_{cl} B^{\lambda} \tag{27}$$

Where R_L is the inductor's series resistance, f is the frequency, V_{cl} is the core volume, and B is the flux density. K, α, λ are constants which depends on the core material. The inductor loss is expressed as:

$$P_L = P_{cu} + P_{core} \tag{28}$$

The total loss is estimated as follows (26):

$$P_{Loss} = P_C + P_{switch} + P_{ripple} + P_L \tag{29}$$

The overall efficiency is estimated as follows (27):

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}} \tag{30}$$

The proposed topology's efficiency without the output filter inductor is 96%. When the output filter inductor is considered, the efficiency is reduced to 95.43%.

5 Design considerations of passive elements

The voltage balancing of passive elements is important in switched-capacitor inverter topologies. The proposed new topology formed using flying capacitor C_1 and switched capacitor C_2. The capacitors C_1 and C_2 are charged to half of the input voltage ($0.5V_{in}$) and the full (V_{in}) input voltage. Since the capacitor C_2 is charged and discharged using a series-parallel technique, it does not require any separate voltage balancing method. Unlike C_2, capacitor C_1 is charged and discharged during ($+0.5V_{in}$) and ($-0.5V_{in}$) output voltage waveform. The capacitor C_1 currents only during $\pm 0.5V_{in,}$ and the ner charge of capacitor C_1 over a fundamental period is expressed as [16]:

$$Q_{C1,net} = \left(\frac{2V_{C1} - V_{in}}{Z}\right)T \tag{31}$$

Under steady-state conditions the voltage across C_1 will equal $0.5V_{in}$. From (28), the total charge of the capacitor C_1 will be zero in a given fundamental cycle, and it is achieved without any supplementary voltage balancing methods. Regarding the sizing of the capacitor C_1, the required parameters are, allowable voltage ripple ΔV_{C1}, switching frequency f_{sw}, peak value of load current. From this C_1 is calculated as [18]:

$$C_1 = \frac{I_p}{\Delta V_{C1} \times f_{sw}} \tag{32}$$

As shown in Fig. 5, the longest discharge period of C_2 occurs from t_3 to t_2.Where t1, t2, t3 are $T_{fo}/12, T_{fo}/6, T_{fo}/4$ which are expressed from fundamental time period $T_{fo.}$ At R-load during steady state operation the load current flow is given as:

$$I_L(t) = \begin{cases} \frac{V_{in}}{2} & ; \frac{T_{fo}}{12} \le T \le \frac{T_{fo}}{6} \\ V_{in} & ; \frac{T_{fo}}{6} \le \beta \le \frac{T_{fo}}{4} \end{cases} \tag{33}$$

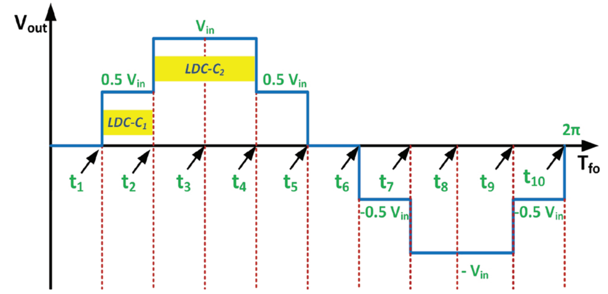

Figure 5: Typical 5 level waveform

The charge of capacitor C_2 during its longest discharging period is expressed as:

$$Q_{C2} = 2 \times \int_{\frac{T_{fo}}{6}}^{\frac{T_{fo}}{4}} I_L(t)\, dt \tag{34}$$

By substituting the equation (33) in (34),

$$Q_{C2} = 2 \times \int_{\frac{T_{fo}}{6}}^{\frac{T_{fo}}{4}} \frac{V_{in}}{R_L}\, dt \tag{35}$$

From the above equation the optimum value of capacitor C_2 is calculated as:

$$C_{2,mx} \ge \frac{\pi}{3 \times R_L \times k \times \omega} \tag{36}$$

Similarly, for resistive-inductive loading the load current is expressed as:

$$I_L = I_{pm} \sin(\omega t - \theta) \tag{37}$$

Using (37) in (34) the capacitance of capacitors C_2 is written as:

$$Q_{C2} = 2 \times \int_{\frac{T_{fo}}{6}}^{\frac{T_{fo}}{4}} I_{pm} \sin(\omega t - \theta)\, dt \tag{38}$$

$$Q_{C2} = 2 \times I_{pm} \int_{\frac{T_{fo}}{6}}^{\frac{T_{fo}}{4}} (\sin \omega t \times \cos \theta - \cos \omega t \times \sin \theta)\ dt$$

$$Q_{C2} = 2 \times I_{pm} \times \left[\cos\left(\frac{\omega T_{fo}}{6} - \theta\right) - \cos\left(\frac{\omega T_{fo}}{4} - \theta\right) \right] \quad (39)$$

$$Q_{C2} = 2 \times I_{pm} \times \left[\cos\left(\frac{\pi}{3} - \theta\right) - \sin \theta \right]$$

From (39), a maximum value of capacitances for C_2 can be calculated as:

$$C_{2,mx} = \frac{2I_{pm}}{\omega \times k \times V_{in}} \times \left[\cos\left(\frac{\pi}{3} - \theta\right) - \sin \theta \right] \quad (40)$$

Where I_{pm} is maximum load current, k is the ripple factor. Fig. 6(a-c) shows the graph between optimum value of capacitance with different load values, different frequencies, and different phase angles. The ripple factor of k=0.01, 0.05 and 0.1 and ω=100π has been taken for calculating the optimum value of capacitances.

Fig. 6b shows the graph between optimum value of capacitance C_2 and frequency. This graph is plotted by considering the load resistance of 200 Ω. Fig. 6c is the graph plotted for different phase angles of θ with allowable voltage ripple of 0.05 and 0.1, I_{pm} = 8 A, V_{in} = 400V, f =50 Hz and ω = 100π at fundamental frequency. It is seen from the Fig. 6c that, as the phase angle increases the capacitance decreases.

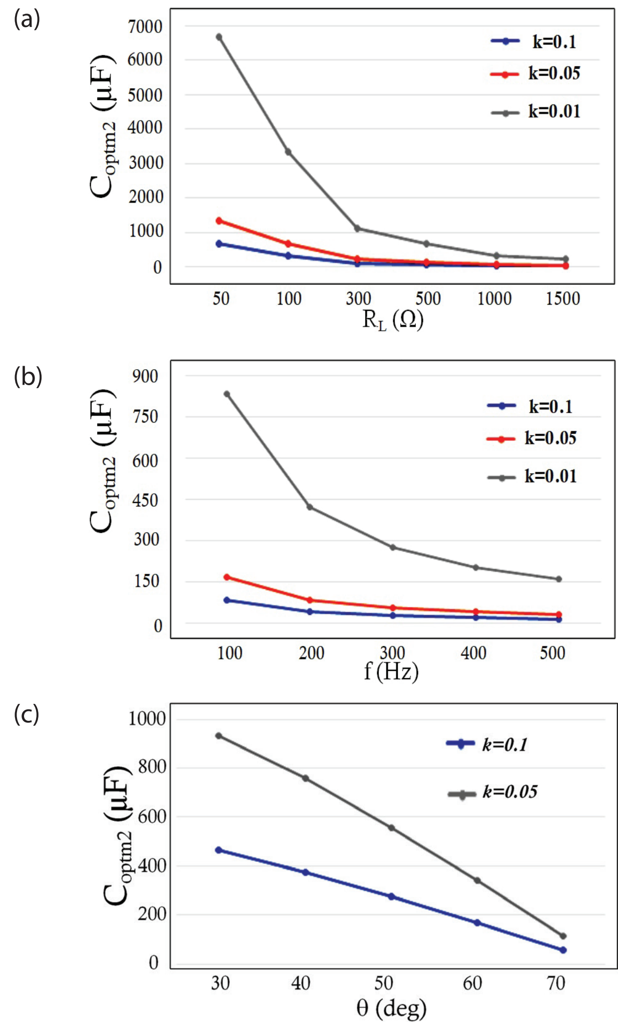

Figure 6: Variation of optimal capacitance versus (a) R_L (resistive load) (b) frequency (Hz) (c) phase angle θ

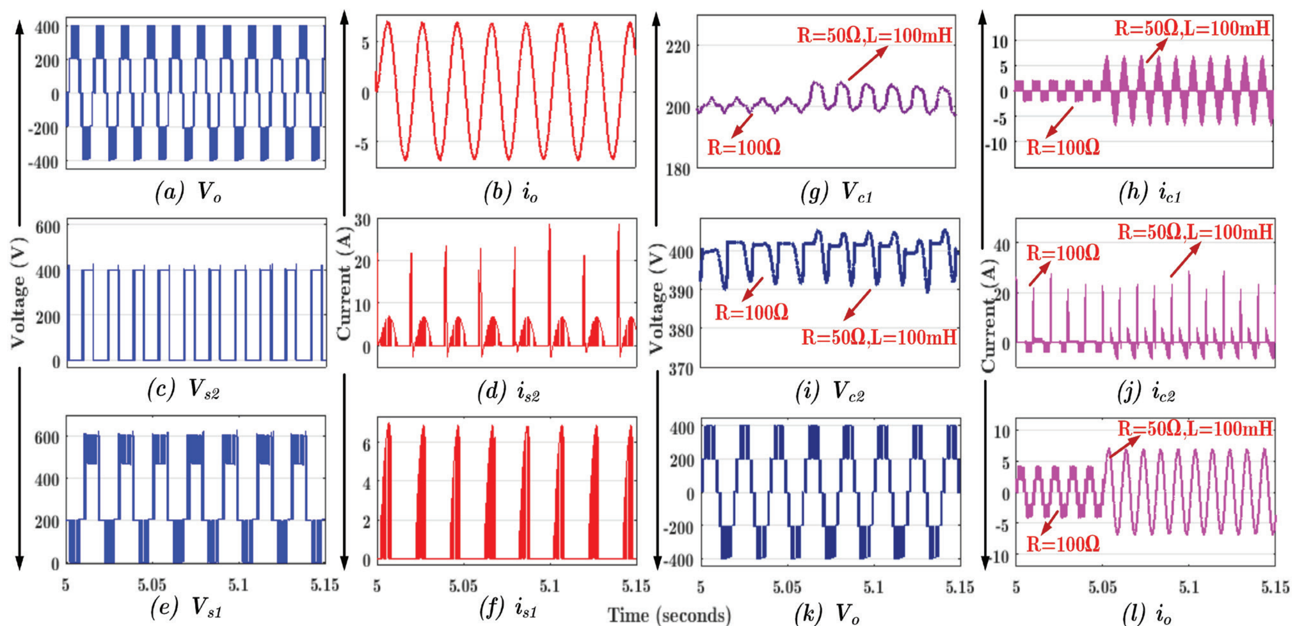

Figure 7: Simulation outputs of proposed 6S-1D-5L inverter topology for 1.2 kW

6 Simulation and experimental results

6.1 Simulation results

The operation of the proposed 6S-1D-5L inverter topology is examined for generating five-level output voltage using MATLAB/Simulink environment. The parameters used for the simulation and values of components used in the proposed inverter topology is tabulated in Table 4. While using alternate high-frequency phase opposition disposition pulse width modulation schemes with R=100 Ω, the load current is observed as 4 A. The load voltage and current waveforms for the RL-Load of R=50 Ω & L=100 mH are shown in Fig. 7a and Fig. 7b respectively. During RL-load, the voltage and current of the switches S_2 and S_1 are obtained and shown in Fig. 7(c-f).

Table 4: Simulation and Experimental Parameters.

Parameters	Simulation	Experimental
Input Voltage	400 V	
Capacitor C1	200 V / 1700 μF	200 V / 2200 μF / LGU2D222MELC
Capacitor C2	400 V / 1700 μF	450 V / 1700 μF / PG6DI
Output Voltage	400 V	
RL Load	R=100 Ω and R= 50 Ω & L= 100 mH	
Switching frequency	5 kHz	
Digital Controller	-	TMS320 F28379D
Gate Drive Circuit	-	TLP 250
IGBT Switch	-	SKM75GB063D

6.2 Experimental results

A laboratory prototype was developed to validate the performance of the proposed topology. The Semikron IGBT switches SKM75GB063D with TLP250 driver circuits were used to develop the 1200 W prototype, as shown in Fig. 9. The Texas Instruments TMS320F28379D were used to generate the gating pulses with a switching frequency of 5 kHz. The direct parallel connection of dc source and capacitors increases the charging current, also called inrush current. This inrush current leads to reducing the power components' life, and higher current rating devices are needed and source able to supply high current. To reduce this inrush current soft charging is used, as shown in Fig. 10. A small inductor with a value of 30 μH is inserted in the capacitor charging loop. In the case of capacitor C_1, it doesn't require because the capacitor is connected series with the load during the charging state. The soft charging path will be provided as long as the RLC circuit operates under damping conditions [17]. Initially, the output results are observed for the pure resistive load with the value of R=100 Ω, and the corresponding voltage and current waveform of load and capacitors are shown in Fig. 11a. Most of the inverters operate in inductive load, so it is necessary to test the proposed topology in resistive and inductive loading conditions. So, the proposed topology is tested with a load value of R=50Ω, L=50 mH and measured. It confirms that the proposed topology can perform for any inductive load, as shown in Fig. 11b. Here worth mentioning that the voltage across the capacitors V_{C1} and V_{C2} are not disturbed for inductive load shown in Fig. 11b. The step input variation shown in Fig. 11c confirms that the proposed topology can generate the 5L during the sudden input variation, as shown in Fig. 11c. The load will not be constant, and it is dynamic. So, the load variations are applied by changing from R=100 Ω & R=50 Ω to L=100 mH and the corresponding waveform shown in Fig. 11d. Further, the modulation index is another important factor in an inverter, and it is worth indicating the performance of the proposed topology with the variations of the modulation index. Varying MI=0.5, MI=0.8 and MI=1 test the effect of the modulation index and the corresponding waveforms are shown in Fig. 11e. Hence, the experimental results are confirmed that the proposed topology can operate in any loading conditions. Finally, the proposed topology simulation and measured efficiency are shown in Fig. 12 for different output power. The maximum efficiency is achieved at low output power and low in high output power.

7 Comparative Study

To evaluate the merits and demerits of the proposed 6S-1D-5L topology, the proposed topology is compared with recent inverter topologies, and it is given in Table 5.

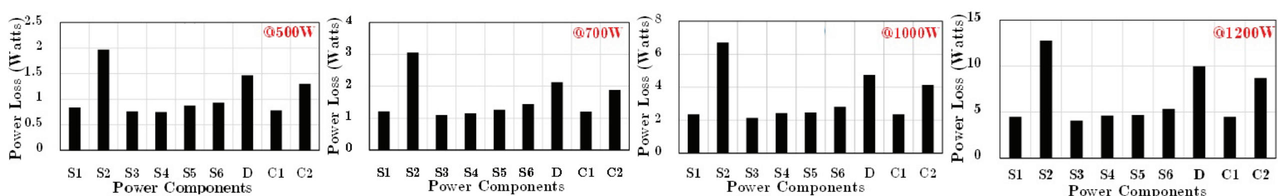

Figure 8: Simulation power loss for various output power (a) 500 W (b) 700 W (c) 1000 W and (d) 1200 W

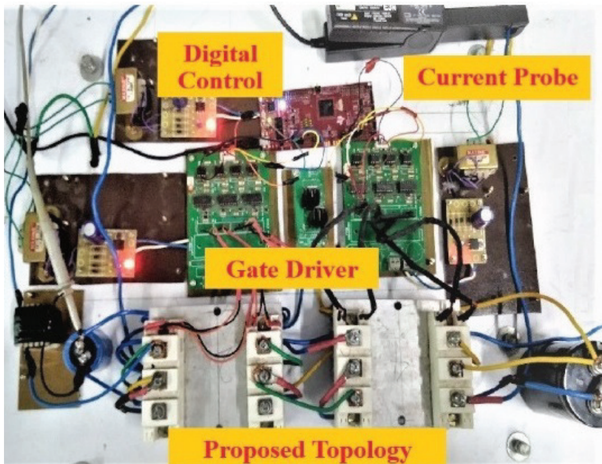

Figure 9: Photograph of prototype hardware setup

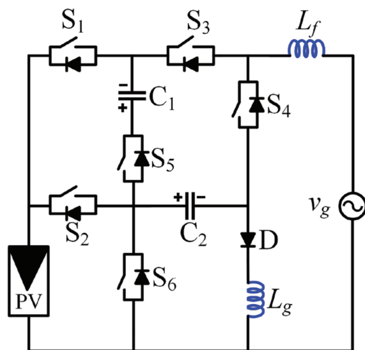

Figure 10: Proposed circuit topology with soft charging inductor

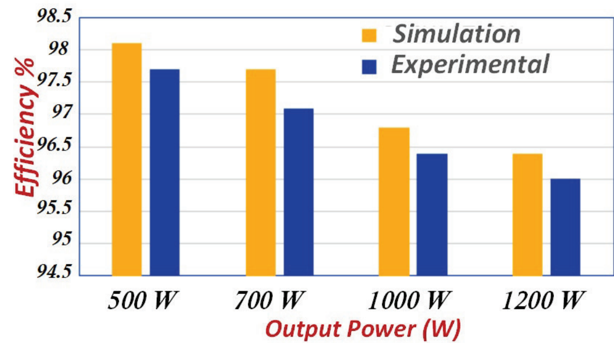

Figure 12: The efficiency of simulation versus hardware result

The comparison is made by considering significant features such as N_S–Number of switches, N_{DR}-Number of driver circuits, N_C-Number of capacitors, N_D-Number of diodes, *TSV* (p.u)-Total standing voltage in per unit, *G*-Gain, V_{Stress}– Maximum voltage stress, V_{Stress}/G, MCS- Maximum number of conducting switches, *CGT*-Common ground type, LC-Leakage Current, P_T-Total Power, η=efficiency. It is observed that the proposed topology has a minimum number of switching components and gate driver units than the topologies mentioned [3], [5], [10], [14]-[15]. The topology [11] offers the same *TSV* (p.u) as that of the proposed 6S-1D-5L inverter topology, but the voltage stress of the topology is very high than the proposed topology. On comparing with the tabulated topologies in the comparative study, it is clear that the proposed topology has the least total standing voltages TSV (p.u) except topologies [12], [14] but the volt-

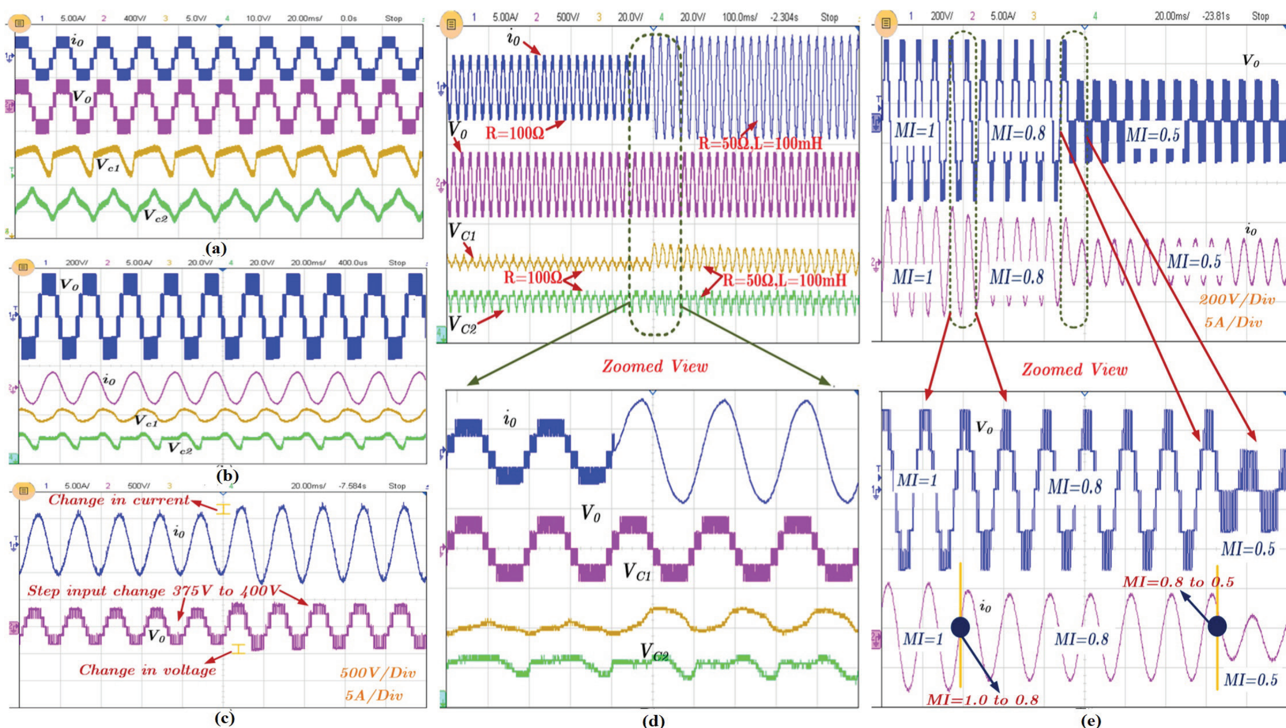

Figure 11: Experimental results of proposed 6S-1D-5L topology (a) for R-Load, (b) for RL load, (c) for step input change, (d) for R to RL load variations and (e) Modulation variation from 1 to 0.8 to 0.5

Table 4: Comparative study with other multilevel inverter topologies

Top	NS	NDR	NC	ND	TSV (p.u.)	G	Capacitor Voltage	V_{Stress}	VStress / G	MCS	CGT	LC /P_T/η%
[3]	9	9	1	0	9	1:2	$2V_{in}$	1	0.5	5	No	NA / 2kW / 97.91
[5]	8	6	3	0	6.5	1:1	V_{in}	1.5	1.5	3	Yes	Zero / 500W / 97.1
[7]	8	8	2	1	12	1:1	$0.5V_{in}$	2	2	4	No	NA / 500W / 96.8
[10]	7	7	2	4	9	1:2	V_{in}	2	1	4	No	NA / 600W / 96.8
[11]	7	6	2	2	6	1:2	V_{in}	4	2	2	Yes	Zero / 600W / 98.1
[12]	6	6	3	1	5	1:1	V_{in}	1	1	3	Yes	Near Zero / 1.2kW / 95.8
[13]	6	6	3	0	8	1:1	V_{in}	1	1	3	Yes	Zero / 1kW / 97
[14]	7	7	3	0	5	1:1	V_{in}	1	1	4	Yes	Zero / 500W / 96.4
[15]	6	6	2	2	10	1:1	$0.5V_{in}$	1.5	1.5	2	No	NA / 400W /97.8
[19]	7	6	3	1	7	1:2	$2V_{in}$	2	1	3	Yes	Zero/750W/98.1
[20]	6	6	3	2	5	1:2	$2V_{in}$	2	1	3	Yes	Zero / 510W/98.1
Pro	6	6	2	1	6	1:1	V_{in}	1.5	1.5	3	Yes	Zero / 1.2kW / 95.43

age stress across the capacitor is very low in the proposed topology which reduces the cost of the inverter. With better TSV (p.u) than other topologies, the proposed topology uses fewer switches. Even with better TSV (p.u) of topology [14], the maximum number of conducting switches is more. On comparing with the topologies [7], [11], the ratio of voltage stress to gain (V_{Stress}/G) of the proposed topology is less. Also, with reference to the comparison Table 5, except for the topology [11], [15] the proposed topology has a smaller number of maximum conducting states than the others. The topology presented in [19] proposes a common ground structure which generates 3L. Despite the usage of two capacitors, the number of ac voltage levels is still three. Also, voltage across one of the capacitors is twice the input voltage. In [20], common ground structure with boosting ability is proposed. But it requires flying capacitor with two times the input supply and also the maximum stress across the switch is equal to twice the input supply. Also, the proposed topology offers high efficiency at low output power.

8 Conclusion

A new transformerless inverter for low power applications is presented in this paper. The proposed topology used two capacitors, and the negative terminal of theload and dc source have a common connection, as discussed. The capacitors voltage is balanced without any additional sensors, and the same is verified in both simulation and experimental results. The output results are discussed, confirming that the proposed topology is suitable for dynamic load variation and modulation index changes. Further, the PLECS analyses the power loss and the various power loss for different output power and the same output power, the measured efficiency is presented. The measured efficiency for the 1.2 kW is 96% without output filter inductor. When including output filter inductor, the efficiency is 95.43% which has a good agreement with simulation efficiency of 96.4%.

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10 Conflict of interest

Authors declaring conflict interest

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Design, Fabrication and Measurement of LDNMOS-SCR Devices with Appropriate ESD Protection Window for 18V HV CDMOS Process

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Abstract: Lateral Double Diffused MOSFET (LDMOS) embedded Silicon Controlled Rectifier (SCR) is a normal way to improve the Electro-Static Discharge (ESD) robustness for smart power technologies, but it doesn't always have the proper ESD window for a given application. In this paper, LDNMOS-SCR of four variants structures have been investigated based on a high-voltage (HV) 0.5µm 18V HV CDMOS process with 2D device simulation and silicon verification. Transmission Line Pulse (TLP) testing results demonstrated that those devices successfully elevate the second breakdown current I_{t2} from original 1.146A to above 3A; source isolated device has a lower trigger voltage V_{t1} (45.79V) than source non-isolated devices; the holding voltage V_h of the four devices is related to their structure, and their holding current I_h are all above 800mA, which is big enough to ensure the latch-up immunity under ESD stresses in HV applications. The device with its source isolated from PSUB is the suitable ESD protection device for HV 18V CDMOS technology owning to its strong ESD robustness, low V_{t1}, small on-resistance Ron and sufficiently big I_h.

Keywords: ESD window; LDMOS embedded SCR; TCAD device simulation; TLP

Načrtovanje, izdelava in merjenje naprav LDNMOS-SCR z ustreznim zaščitnim oknom ESD za 18V HV proces CDMOSI

Izvleček: Vgrajeni silicijev usmernik z dvojno lateralno difundiranim MOSFET (LDMOS) je običajen način za izboljšanje odpornosti proti elektrostatičnim razelektritvam (ESD) pri pametnih energetskih tehnologijah, vendar nima vedno ustreznega okna ESD za določeno aplikacijo. V tem članku so bile raziskane štiri različice struktur LDNMOS-SCR na osnovi visokonapetostnega (HV) 0,5µm 18V HV CDMOS procesa z 2D simulacijo naprave. Rezultati testiranja TLP (Transmission Line Pulse) so pokazali, da te naprave uspešno povečajo drugi prebojni tok I_{t2} s prvotnih 1,146A na več kot 3A; izvorno izolirana naprava ima nižjo prožilno napetost V_{t1} (45,79V) kot izvorno neizolirane naprave; držalna napetost V_h vseh štirih naprav je povezana z njihovo strukturo, njihov držalni tok I_h pa je nad 800 mA, kar je dovolj veliko za zagotovitev odpornosti na zaklepanje pri obremenitvah ESD v HV aplikacijah. Naprava z izvorom, izoliranim od PSUB, je primerna naprava za zaščito pred ESD za HV 18V tehnologijo CDMOS zaradi svoje močne odpornosti proti ESD, nizke V_{t1}, majhne upornosti Ron in dovolj velikega I_h.

Ključne besede: Okno ESD; vgrajeni SCR LDMOS; simulacija naprave TCAD; TLP

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1 Introduction

LDMOS power transistors have been commonly used as output driver and ESD protection device simultaneously in the smart power technologies [1-3]. However, the HV LDMOS doesn't have high ESD robustness after entering its snapback breakdown region. Such device exhibits random and unconstrained failures during the snapback breakdown before reaching its intrinsic limitation [4-7]. LDMOS embedded SCR is a normal way to improve the ESD robustness in high voltage technology. Several works have been done to kinds of LDMOS-SCR for smart power application. Wang discussed ESD charateristics about LDMOS-SCR device including its working mechanism, latchup immunity simulation, and response time analyses, etc [8]. Chang proposed the impact of technology layers and layout parameters on the LDMOS-SCR devices robustness [9]. Ker put forward a modified LDMOS-SCR achieving high holding voltage with the aid of RC detection circuit [10]. Lee found that a P+ strip inserted into drain region can improve the ESD failure threshold of embedded SCR LDMOS device [11]. Some other novel structures and their performance were studied for different application purposes in [12-16].

The purpose of this paper is to design a robust ESD protection device with an appropriate ESD window for 18V HV CDMOS technology with respect to traditional gate-grounded LDNMOS (GG-LDNMOS). Four types LDNMOS-SCR are considered in this paper, and the testing devices are fabricated in a 0.5µm 18V HV CDMOS technology. Their ESD characteristics are evaluated by two dimensional (2D) device simulation and transmission line pulse (TLP) measurement.

2 LDNMOS-SCR Devices and working mechanism

The cross-sectional view of conventional GG-LDNMOS is shown in Figure 1. Four types LDNMOS embedded SCR are designed based on the LDNMOS. As shown in Figure 2(a) is the structure for type I device, a P+ diffusion in conjunction with N+ diffusion is added in the deep N well (NWD) to serve as anode of the embedded SCR. The N+ region used as original drain electrode of LDNMOS shrinks its lateral dimension and is let alone with no voltage applying to it. Thus, there will be two discharge ways in the modified structure. One path for ESD current discharging is LDNMOS, it should pass through the NWD resistor named R_{drain} between the floating drain and anode. The other way is through the embedded SCR, the way is composed by P+ diffusion in the anode region, NWD, PW, N+ diffusion in the cathode region. Whatever discharge routing it goes, the avalanche breakdown junction is still at the NWD/PW junction. The equivalent circuit of Type I is shown in Figure 3. The embedded SCR is composed of a vertical p-n-p BJT and a lateral n-p-n BJT to form a 2-terminal/4 layer PNPN (P+/NWD/PW/N+) structure.

The main difference of the other three LDNMOS-SCR devices from Type I device in Figure 2 is that the source of LDNMOS is not isolated from PSUB by NWD. Hence, the avalanche breakdown of those devices could occur either at the NWD/PSUB junction or at the NWD/PW junction. Among those three types non-isolated LDNMOS-SCR, Type III and Type IV have an additional NW surrounded P+&N+ or P+ only at the anode, which will influence their holding voltage (V_h). The equivalent circuit for device Type II, Type III and Type IV is drawn in their cross-sectional view. Although the different anode structures result in the different resistance between the b-e junctions of vertical PNP transistor, the working mechanism of all the LDNMOS-SCR devices is identical.

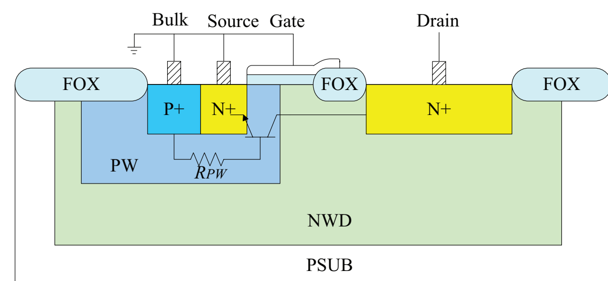

Figure 1: Cross-sectional views of conventional GG-LDNMOS device.

3 TLP testing result and discusions

The above four devices are fabricated as one-finger device with device width of 50µm. The ESD characteristics measurement is performed on the Thermo Celestron I transmission line pulse (TLP) system. It applied a current pulse to the device with a rise time of 10ns, a pluse width of 100ns, and the current stress level increasing continuously until the device failed. The leakage current is measured after each TLP zapping with 19.8V DC voltage on their anode. Once the leakage current is above ~1µA, it is considered that the device under test is failure. The TLP IV curves for LDNMOS with embedded SCR are shown in Figure 4, and corresponding TLP data is summarized in Table 1. TLP measurement data of one-finger traditional GG-LDNMOS with the same device width is also listed in this table for comparison.

It is apparent in Figure 4 that the source isolated LDNMOS-SCR (Type I) has a lower trigger voltage, which

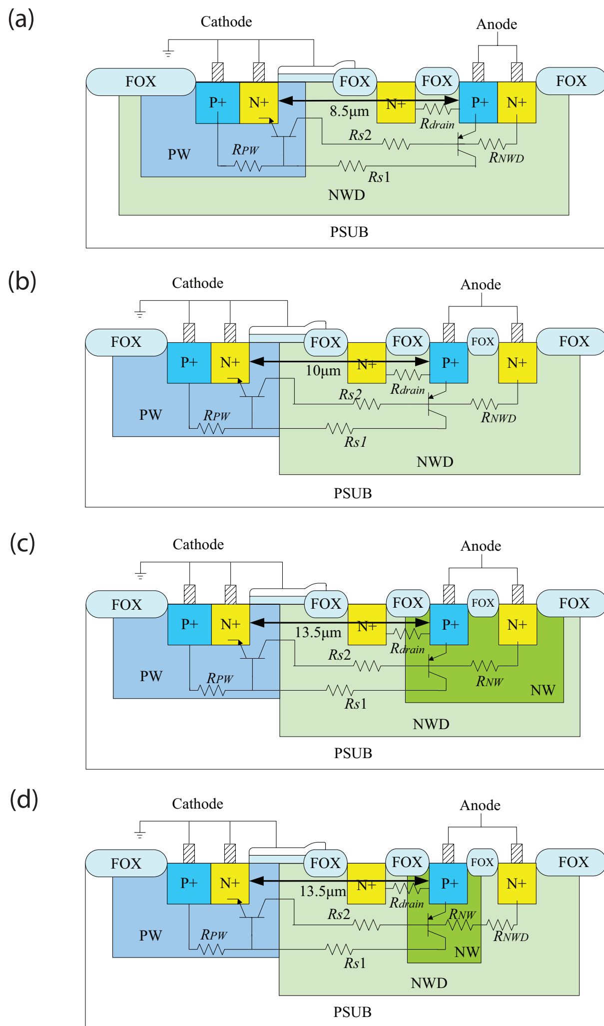

Figure 2: Cross-sectional views of four kind LDNMOS-SCR devices. (a) Type I; (b) type II; (c) type III; (d) type IV.

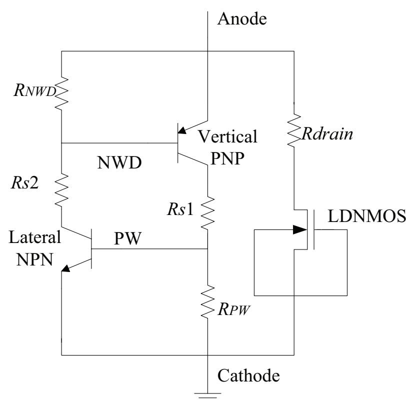

Figure 3: Equivalent circuit of Type I LDNMOS with embedded SCR.

can be triggered into its snapback region earlier. The holding voltages are below 18V, however, they have a relatively high holding current above 800 mA, which ensures the latch-up immunity under ESD stresses in HV applications. Their leakage current is remained at 7~9nA before hard failure, hence, they don't bring considerable impact on the protected core circuit in normal condition.

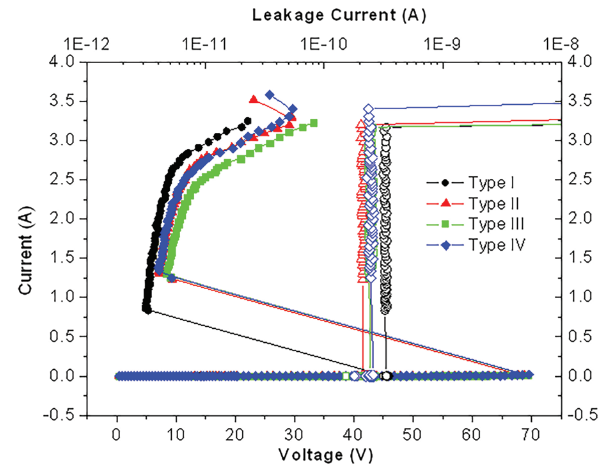

Figure 4: TLP I-V plots for four types LDNMOS embedded SCR with the same device width of 50 µm.

3.1 Trigger characteristics

The trigger voltage of Type I LDNMOS-SCR with its source isolated from PSUB is 45.79V, which is much small-er than that of other three source non-isolated LDNMOS-SCR devices. The different NWD location should take responsibility for the different V_{t1}. A two dimensional (2D) device simulation is performed on a TCAD platform to discover the root cause. Type II is a typical source non-isolated LDNMOS-SCR, whose source is not enveloped by NWD, thus, only Type I and Type II devices are simulated with a 10V voltage applied on their anode electrode. The simulated junction, depletion layer and electric field distribution for those two devices are demonstrated in Figure 5. The red heavy line in the 2D device structure is the edge of depletion layer, the thickness of depletion layer across NWD/PW junction under the poly silicon of Type I is 1.6μm, which is narrower than that of Type II (2.7μm). As the voltage applied on anode is the same, the device with narrower depletion layer will have a stronger electric field. This is proved in Figure 5 that the electric field equal strength line of Type I is denser than that of Type II at this location. Hence, Type I inclines to breakdown more easily than Type II, and a bigger avalanche breakdown voltage is needed for Type II to switch on. Therefore, Type II owns a V_{t1} of 68.78V, which is larger than Type I source isolated LDNMOS-SCR.

Table 1: TLP measured data for conventional GG-LDNMOS and four kind LDNMOS-SCR devices with the same finger width of 50 micrometers.

Device Name	V_{t1}(V)	V_h(V)	I_h(A)	I_{t2} (A)	Efficiency (mA/μm²)	Spacing (μm)
GG-LDNMOS	46.909	8.161	0.907	1.146	0.459	/
Type I	45.794	4.825	0.864	3.169	1.884	8.5
Type II	68.780	7.029	1.332	3.292	2.480	10.0
Type III	69.450	8.368	1.311	3.167	1.735	13.5
Type IV	69.554	7.082	1.379	3.399	2.086	13.5

The DC breakdown voltage (BVD) of the LDNMOS device in the core circuit is 43.5V in our CDMOS technology, and Type I LDNMOS-SCR has the lowest V_{t1} among the four investigated devices, which is only several volts bigger than BVD. And its V_{t1} is closest to the trigger voltage of conventional GG-LDNMOS used for ESD protection at I/O pad. Thus, Type I will be the optimal choice in view of transient V_{t1} measured by TLP.

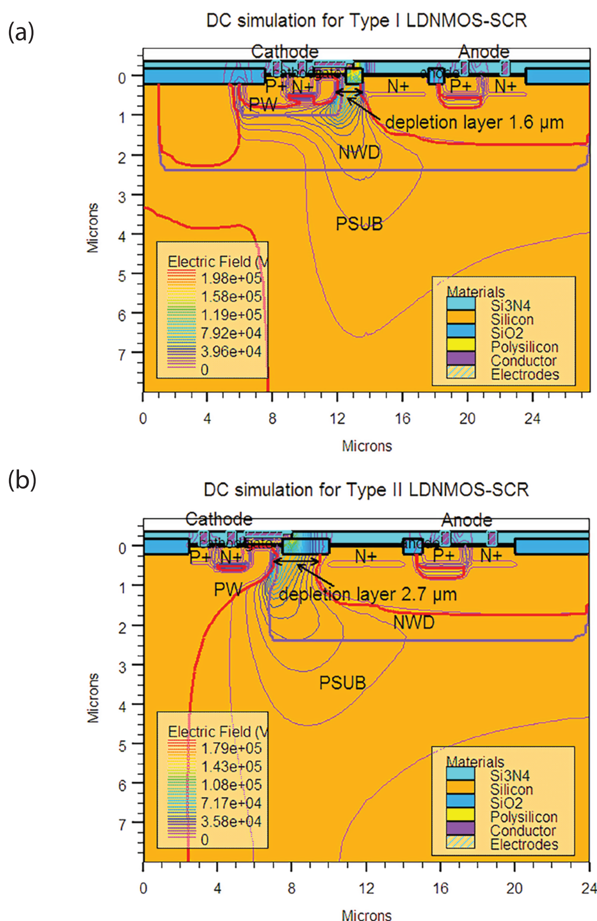

Figure 5: Junction location, depletion layer and electric field (V/cm) distribution in (a) Type I source isolated LDNMOS-SCR and (b) Type II source non-isolated LDNMOS-SCR by DC simulation with anode electrode voltage of 10V.

3.2 Holding characteristics

The V_h of four types LDNMOS-SCR are 4.83V, 7.03V, 8.37V and 7.08V, respectively. The holding voltage difference is result from the anode structure. Formula of V_h can be derived from SCR equivalent schematic in Figure 3,

$$\begin{aligned} V_h &\approx V_{ec-PNP} + (V_{be-NPN} / R_{PW} + I_{be-NPN}) \times R_{s1} + V_{be-NPN} \\ &= V_{ec-PNP} + V_{be-NPN}(1 + R_{s1} / R_{PW}) + I_{be-NPN} \times R_{s1} \\ &= V_{ce-NPN} + V_{be-PNP}(1 + R_{s2} / R_{NWD}) + I_{be-PNP} \times R_{s2} \end{aligned} \quad (1)$$

The spacing between anode P+ and cathode N+ called SCR length of Type I, Type II, Type III, Type IV are 8.5μm, 10μm, 13.5μm and 13.5μm, respectively. The wider the spacing is, the bigger the parasitic resistance R_{s1} and R_{s2} are. And it can be concluded from (e.g. Eq. (1)) that device with bigger R_{s1} and R_{s2} will obtain a lager V_h. Thus, the holding voltage relationship of Type I, Type II, Type III is $V_{h\text{-Type I}} < V_{h\text{-Type II}} < V_{h\text{-Type III}}$. However, there is an exception that Type III and Type IV have the same anode to cathode space, but V_h of Type IV is smaller than that of Type III. This is because the P+ & N+ diffusion regions at the anode of the Type III device are surrounded by NW, so the R_{NWD} in (e.g. Eq. (1)) is replaced by R_{NW}. While the Type IV device is partly replaced by R_{NW}, as only the P+ diffusion area is sur-rounded by the NW. For the doping concentration of NW is higher than NWD, therefore, the RNWD term in (e.g. Eq. (1)) of Type IV device is larger than Type III, so Type IV has a smaller V_h than Type III. It is noted that V_h of all those LDNMOS-SCR devices are below 18V circuit operation voltage, however, the holding current (I_h) of them is all above 800mA, which is big enough for those devices to immune from latch-up at normal operation in HV applica-tions [17-18].

3.3 ESD robustness and turn-on resistance characteristics

Table 1 shows that the second breakdown current I_{t2} of four devices are all above 3A, which is much higher than that of the traditional GG-LDNMOS of 1.146A. Thus, the ESD robustness of LDNMOS is indeed increased by adding a SCR path in it. Among those devices, Type IV has the highest second breakdown current of 3.399A, but for its bigger SCR length (13.5μm), it ocuppies larger chip area. The device has the biggest current discharge effciency is Type II, its current discharge per unit area is 2.48mA/μm², thus, it is an optional device when chip area minimization is taken into consideration.

The on-resistance (R_{on}) of devices is indicated by the slope of their I-V curves after snapback. The R_{on} versus TLP current after snapback and before second breakdown is derived from TLP testing data of those devices and shown in Figure 6. The turn-on resistances differ

from each other for different device structures, Type II & Type IV have the relatively low R_{on}, Type I has the minimum turn-on resistance, which means ESD current is more easily to discharge through it. It is also noted that the device that has a larger holding voltage owns a bigger R_{on}. And it has a trend that R_{on} decreases a little at first, and then increasing apparently as the TLP current growing around ~2.5A. This is because that a bigger current results in a higher lattice temperature, and the carrier mobility will index decrease as the lattice temperature increasing [19]. Thus, R_{on} increases dramatically until the second breakdown occurs.

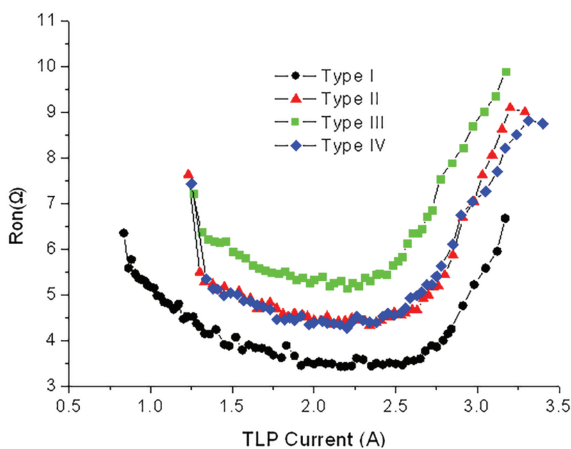

Figure 6: Turn-on resistance Ron of four types LDNMOS-SCR in their snapback region.

4 Conclusions

Four types LDNMOS-SCR ESD protection device have been fabricated in a 0.5µm 18V HV CDMOS process and measured by TLP to examine their ESD windows. The key parameters obtained in TLP I-V curves are compared and discussed.

1) The Type I source isolated device has a lower V_{t1} due to the thinner depletion layer than the non-isolated LDNMOS-SCR. The V_h of the four devices is determined by the anode to cathode SCR spacing and anode structure, and their I_h is big enough to immune from latch-up issue. Further, the second breakdown current I_{t2} of those four devices is much higher than that of traditional GG-LDNMOS, which improve the ESD robustness greatly.

2) From the analysis in section 3, it leads us to conclude that Type I is the appropriate device used for HV 18V ESD protection owning to its low V_{t1} and small R_{on}. Type II will be prior to other two non-isolated LDNMOS-SCR for its high discharge efficiency and relatively low resistance, it can be used to protect circuits with even higher operation voltage.

5 Acknowledgments

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6 Conflict of interest

We declare that we do not have any commercial or associative interest that represents a conflict of interest inconnection with the work submitted.

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Programmable implementation of time-area-efficient Elliptic Curve Cryptography for entity authentication

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Abstract: The rise of wireless technologies, communications and devices, has resulted in the demand for effective security with low hardware requirements and high speed. Among the various cryptographic algorithms, the Elliptic Curve Cryptography (ECC) provides an attractive solution for this demand. In this paper, the Remote Keyless system (RKE) Authentication process using the ECC is implemented in Field Programmable Gate Array (FPGA). The designed ECC processor supports 256-bit point multiplication and point addition on the Koblitz curve secp256k1. The scalar multiplication is performed with the faster multiplier Urdhva Tiryagbhyam (UT). Additionally, pipelining is incorporated in order to speed up the multiplication process of the processor. The proposed ECC processor performs single point multiplication of 256-bit in 1.2062ms with a maximum clock frequency of 192.5MHz, which provides 212.23kbps throughput and occupies 8.23k slices in Virtex-7 FPGA. Incorporating a pipeline in scalar multiplication improves the maximum clock frequency up to 15.12%, which reduces time consumption by 22.36%, which in turn increases the throughput by 22.36%. The proposed pipelined Vedic multiplier based ECC processor outperforms the existing designs in terms of area, operating frequency, area-delay product and throughput. Also, the security evaluation and analysis of the proposed ECC processor are performed, which ensures the safety of RKE systems. Hence, the implementation of the proposed method offers time-area-efficient and fast scalar multiplication with effective hardware utilization without any compromise in security level.

Keywords: Urdhva Tiryagbhyam; Pipeline; Remote Keyless system Authentication; FPGA

Programirljivo izvajanje časovno učinkovite kriptografije eliptičnih krivulj za avtentikacijo entitet

Izvleček: Razvoj brezžičnih tehnologij, komunikacij in naprav je povzročil potrebo po učinkoviti varnosti z nizkimi strojnimi zahtevami in visoko hitrostjo. Med različnimi kriptografskimi algoritmi zagotavlja eliptična krivulja (ECC) privlačno rešitev za to. V tem članku je predstavljen postopek avtentikacije sistema brez ključa na daljavo (RKE) z uporabo ECC v FPGA (Field Programmable Gate Array). Zasnovani procesor ECC podpira 256-bitno množenje in seštevanje točk na Koblitzovi krivulji secp256k1. Skalarno množenje se izvaja s hitrejšim množiteljem Urdhva Tiryagbhyam (UT). Poleg tega je za pospešitev postopka množenja v procesorju vključena cevna povezava (pipelining). Predlagani procesor ECC izvede enotočkovno množenje 256-bitov v 1,2062 ms z največjo taktno frekvenco 192,5 MHz, kar zagotavlja prepustnost 212,23 kb/s in zasede 8,23k rezin v Virtex-7 FPGA. Vključitev cevovoda pri skalarnem množenju izboljša največjo taktno frekvenco do 15,12 %, kar zmanjša porabo časa za 22,36 %, to pa poveča prepustnost za 22,36 %. Predlagani procesor ECC, ki temelji na množitelju s cevovodi Vedic, je boljši od obstoječih modelov glede površine, delovne frekvence, produkta površine in zakasnitve ter prepustnosti. Izvedena sta tudi varnostna ocena in analiza predlaganega procesorja ECC, ki zagotavlja varnost sistemov RKE. Izvedba predlagane metode torej omogoča časovno učinkovito in hitro skalarno množenje z učinkovitim izkoristkom strojne opreme brez kompromisov na ravni varnosti.

Ključne besede: Urdhva Tiryagbhyam; Cevovod; avtentikacija sistema brez ključa na daljavo; FPGA

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1 Introduction

Nowadays, almost all cars are equipped with a smart keyless entry system. This is an electronic lock that controls admittance to a vehicle without utilizing a manual mechanical key. Such frameworks currently have a secret touch-enacted keypad, which is as yet accessible on certain Ford and Lincoln models. This method is termed as Remote Keyless System (RKS). A distant keyless framework can incorporate both a remote keyless entry (RKE), which opens the car door and a remote keyless ignition system (RKI), which turns the engine ON.

On account of the innovative keyless technology, programmers can utilize expert systems to fool the vehicle and to make them believe that the right fob is close by, permitting them access. Such attacks are listed as below [1],

1. **Replay Attack:** A replay attack (otherwise called playback attack) is a type of organized attack in which valid information transmission is perniciously or falsely rehashed or delayed [2].
2. **Rolljam Attack:** The rolljam attack works by recording and blocking the radio signal from the key fob. Because the signal is blocked, the car doesn't unlock and the owner will naturally try again. That creates a second signal that is also recorded and blocked, but this time the attacker replays the first code to unlock the door.
3. **Brute Force Attack:** Brute force attacks are simple and reliable. Attackers let a computer do the work – trying different combinations of usernames and passwords until they find one that works.

Some other attacks are radio jamming attack, scan attack and two-thief attack, which are also major attacks in Remote Keyless Entry (RKE) and Passive Remote Keyless Entry (PRKE) systems, which are shown in Figure 1.

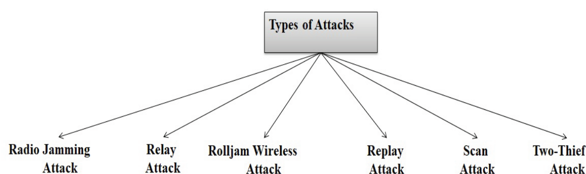

Figure 1: Types of Attacks in Remote Key Fob [1]

In order to overcome these attacks, a high level of security algorithms is needed for secure communication. The public key cryptography based authentication has no secret information to be shared between the entities. A user requesting to authenticate him has to use his private key to digitally sign a random number, which is issued by the verifying entity. This random number is a time-variant parameter and is unique to the authentication exchange. If the verifier completes the verification of the signed response of the user, then authentication would be granted. These kinds of authentication methods are widely popular in sensor networks. In such scenarios, strong encryption algorithms are required to avoid mischief [3]. This kind of entity authentication is to be initiated by the user that can be an equivalent word. This equivalent word checked by the verifier [4].

Elliptic-curve cryptography [5] is a public key cryptography based on the algebraic structure of elliptic curves over finite fields. Elliptic curves are used in key agreement, digital signatures, pseudo-random generators and also in performing other tasks. In contrast to Rivest–Shamir–Adleman (RSA), the ECC approach is based on how elliptic curves are structured algebraically over finite fields. Therefore, ECC creates keys that are more mathematically difficult to crack [6]. Hence ECC is considered to be the next generation public key cryptography and it is more secure than RSA. ECC cryptography can provide strong security with a 164-bit key as other cryptosystems realize the same level of security with a 1024-bit key or more. With the advent of mobile devices being used for highly secured private transactions, low-overhead encryption schemes are becoming highly desirable in today's applications.

The effectiveness of ECC can be improved by modifying its computations process. Vedic mathematics is a collection of procedures to solve complex mathematical functions effectively. It was invented by Sri Bharati Krishna Tirthaji from the Indian Veda scriptures. It consists of 16 sutras, among which Urdhva Tiryakbhayam, Nikhilam Sutram and Anurupye are the most widely used sutras for solving complex functions. The significant gain of the Vedic multipliers is that they have simple procedures for the resource consuming multiplications [7]. The multiplication operation can be extended to n-bits with some minor modifications.

The factual meaning of the Urdhva Tiryagbhyam Sutra is "Vertically and Crosswise". The vertical and crosswise manipulation is performed to generate the partial products; then they are summed for final product generation. 2×2 is the basic module of the Vedic multiplier. The n-bit multiplier could be derived by the repeated arrangement of 2×2 multipliers. This process makes the computation fast and the product is generated with a fewer number of steps [8].

2 Literature survey

Multiple attacks are strategized based on the technology used on the fob. A powerful attack will result in a definite loss to the user. There are many kinds of attacks

that are reported regarding the car locking mechanism. Wireless communication systems used for RKE seem to be more vulnerable to attack. Furthermore, the type of cryptographic algorithms deployed also limits the security in those systems [1].

A simple relay based passive keyless entry was constructed and tested for 10 cars from 8 different manufacturers at various physical distances. This methodology is an initiation towards the remote keyless car. These countermeasures carried against the attack itself act as a hindrance to the keyless operation [9]. In [10], a symmetric key based remote keyless secure transmission between car and fob was demonstrated, which provides secure communication against scan attack, playback attack and forward prediction attack. It requires less computation and consumes less energy with a message length of 80 bits. But, it requires frequent key updates by the user for better security. There is no safety without security in the progressively interconnected nature of a vehicle's control modules.

But, the hackers intercept the car's remote key details while the owner is using them. Then, these intercepted details are utilized to unlock the car door without the knowledge of the owner. Recently, 'Universal Remote' [11], 'EvanConnect', 'keyless repeater' [12] and power amplifier are used to hack Honda, Toyota, Volvo, Volkswagen and Jaguar cars. These hackers capitalized on the communication design flaw present in the design of the protocol. Keeloq system from Microchip has been broken by the University of Bochum or NXP's Hitag-2 system. At Fraunhofer AISEC the effectiveness of ECC in RKE applications was demonstrated. It was prototyped with the support of Field Programmable Gate Array (FPGA) [13].

A remote keyless system is widely used in automobile industries to lock or unlock the vehicle's door. But the security of the remote keyless system is threat prone since the beginning. Initially, Advanced Encryption Standard (AES) based wireless protocol with fixed and variable key length system was introduced [14, 15]. Here, a maximum of 128-bit AES is used for encryption, which could provide effective security against three types of attacks [14]. But, they are implemented in an 8-bit ATMega128L microcontroller, which has a very low speed of operation. Thereafter, FPGA implementation of secured Controller Area Network (CAN) bus communication was developed with AES for internal vehicular communication [15].

An ECC protocol developed in Python can provide security against 9 different attacks, which is economical compared to its predecessors [16]. Thereafter [17], a software protocol was developed based on ECC towards authentication of smart remote vehicle control, which could provide security against 12 kinds of attacks.

In the modern-day scenario, almost all automobiles are equipped with a remote keyless system. Hence the security of the communication system should be effective. Only a few studies focused on this issue. The presently available studies are lacking in,

- Effective Hardware implementation [14-17].
- Proper key size against the attack [14-15].

Also, according to Alan Grau [18], key fob fails due to Encryption keys generated from public data along with insufficient entropy for generating encryption keys, Discoverable encryption keys, and Deprecated key strength. It was suggested that deploying asymmetric encryption with proper key length on suitable hardware will improve the key fob encryption [18].

An effective scalar point multiplication for the elliptic curve is introduced. Then the critical path of the scalar point multiplication for the Lopez-Dahab curve is rearranged and reordered in such a way that parallel processing is enabled and the critical path operations are shifted to non-critical paths [6]. The point multiplication in ECC is a time consuming and slow process. Now, the ECC point multiplication is performed with Urdhva Tiryagbhyam Vedic multiplication [19]. The UT performs significantly better in terms of delay and logic levels compared to the conventional multiplier [20, 21]. Especially, the Vedic multiplier surpasses the performance of the Karatsuba multiplier in terms of area and delay; in addition to that, the UT has 90% less delay compared to the Booth multiplier. Even though the Booth multiplier is occupying less area, the delay for a single product generation is 287ms, which is 10 times higher than the Vedic multiplier [22] as shown in Table 1. Also, UT exhibits smaller path delay, logic delay, routing delay and dynamic power. The size of the UT may be 16-bit [19], 32-bit [23] and can be extended as desired.

Table 1: Performance of Vedic, Karatsuba and Booth multiplier [22]

Parameter	Vedic	Karatsuba	Booth
No. of slice LUTs	51761	103246	1937
No. of IOBs	640	640	643
Time Delay (ns)	27.172	34.123	287.840
Area Delay Product	0.001406	0.003523	0.000558

Hence, a more secured and high performance remote keyless system can be developed using a hybrid of ECC incorporated with Vedic multiplier, which is to be implemented in FPGA.

3 Mathematical background

In this paper, the Koblitz curve is considered with secp256k1 for ECC as shown in Figure 2. This elliptic curve has the form of $y^2 = x^3 + ax + b$, in which a = 0, b = 7, whose Prime Field (p) = $2^{256} - 2^{32} - 977$ and in the random case we have considered,

Order (n) = FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFE FFFFFC2F

Base Point (G) = 04 79BE667E F9DCBBAC 55A06295 CE870B07 029BFCDB 2DCE28D9 59F2815B 16F81798 483ADA77 26A3C465 5DA4FBFC 0E1108A8 FD17B448 A6855419 9C47D08F F

Addition: Let P = $(x_1, y_1) \in (K)$ and Q = $(x_2, y_2) \in E(K)$, where P = ±Q. Then P + Q = (x_3, y_3), where, $x_3 = (y_2 - y_1/x_2 - x_1)^2 - 2x_1 - x_2$ and $y_3 = (y_2 - y_1/x_2 - x_1)^2 - (x_1 - x_3) - y_1$

Point Doubling: Let P = $(x_1, y_1) \in E(K)$, where P = -P. Then 2P = (x_3, y_3), where: $x_3 = (3x_1^2 + a/2y_1)^2 - 2x_1$ and $y_3 = (3x_1^2 + a/2y_1)^2 - (x_1 - x_2) - y_1$

According to Hankerson, Menezes, and Vanstone [24], the primary advantage of the Koblitz lies in the possibility of implementing ECC without point doublings when performing ECC Point Multiplication (ECPM).

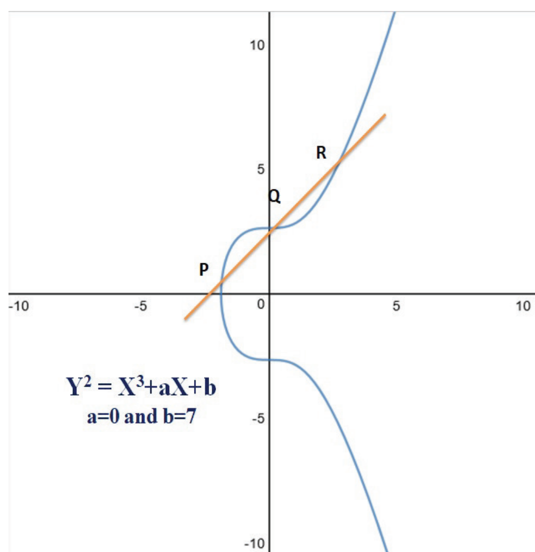

Figure 2: Diagram of Elliptic Curve

The Urdhva Tiryagbhyam (UT) Vedic multiplication is as follows,

Algorithm 1 VEDIC ALGORITHM
  INPUT: n- bit Multiplicand and Multiplier
  OUTPUT: 2n- bit product
    $k \leftarrow 0$
  S(k): 2n- bit vector initialized to 0
  for $i = 0$ **to** n-1 **do**
    for $j = 0$ **to** i **do**
      $S(k) = S(k) + a(i) \times b(i - j)$
    end
    $k = k + 1$
  end
  for i = n-1 **to** 1 **do**
    for j = n-1 **to** i **do**
      $S(k) = S(k) + a(i) \times b(n - (i - j))$
    end
    $k = k + 1$
  end
  for $i = 0$ **to** $(k - 1)$ **do**
    $P = P + S(i)$
  end

4 Main contribution

A time-area-efficient 256-bit ECC processor over prime field is implemented in FPGA. It is aimed to reduce the area and the delay for single point multiplication and increase the frequency and the throughput. In order to reach these objectives, the following major contributions are made in this paper,
An efficient design for ECPM on a Koblitz curve secp256k1 for the 256-bit prime field is proposed.
A faster Urdhva Tiryagbhyam multiplier is adopted for ECPM scalar multiplication, which reduces computation time.
The computing frequency is further improved by incorporating the pipeline technique in the Vedic multiplier.
Moreover, the area-delay product, throughput and efficiency of the proposed method shows improvement compared to the existing similar works in the literature.

5 Methodology

This section presents the algorithms, hardware architectures for point addition, point multiplication, modular multiplication and pipelined Vedic multiplication for ECC based remote keyless system authentication.

5.1 Remote keyless system authentication

The ECC based remote keyless entity authentication system has various processes to be carried out between the key fob and the car. In the key fob, secret key generation, public key calculation and nonce decryption

processes are performed. In the car module, random nonce encryption and verification of decrypted nonce received from the key fob takes place. The overall diagram describing the process is given in Figure 3.

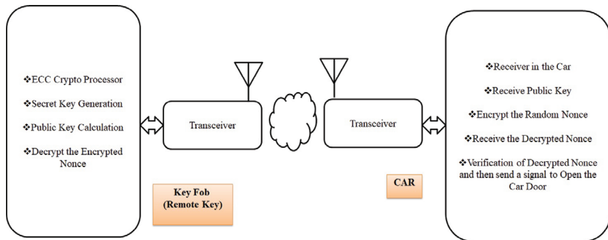

Figure 3: Block Diagram of Remote keyless system authentication Process

The above processes are accomplished in three stages as specified in Figure 4. They are described as follows,

Stage 1: The authentication process starts when the car key fob is pressed.

In Key Fob

In the first stage, when the user wishes to unlock the car door, he initiates the key fob. Two 256-bit random numbers are generated in the key fob with the help of the Linear Feedback Shift Register (LFSR). Among those, one is the Public key and another is the Private Key. The Private Key is kept confidential by the key fob. The 256-bit Public key would be transmitted to the Car through the transceiver module. Both the Public and Private keys are known to key fob alone.

In the Car

The Car receives the Public key and then, it generates a 256-bit random text (cipher text or plain text) using Linear Feedback Shift Register. Thereafter, plain text encryption takes place with the Public key. The sequence of plain text generation process is same for one complete process.

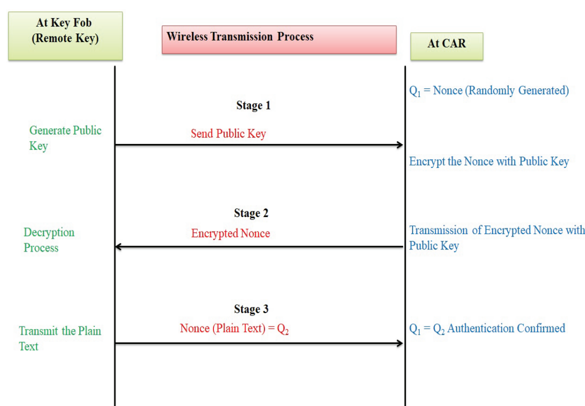

Figure 4: Three stages of Communication between Key Fob and Car

Stage 2: Encrypted Nonce.

In the Car

The Car will transmit the encrypted nonce with the plain text through the Transceiver.

In Key Fob

The key fob receives the encrypted 256-bit randomly generated plain text nonce. Then the Key fob performs the decryption of the nonce using the 256-bit Private Key.

Stage 3: Nonce Transmission.

In Key Fob

After decryption, the key fob transmits the nonce to the Car.

In the Car

The Car compares the received nonce with the original nonce generated at STAGE 1. If they are matched, then the Car door will be unlocked, otherwise not.

5.2 ECC

The ECC core chooses a point on the ECC curve in Koblitz coordinates *P(X, Y, Z)* and finds the point *Q(X, Y, Z)=k × P*. The system controller releases necessary control signals to produce the desired output *Q* as shown in Figure 5.

- Private key: nA, where nA is a 256-bit Random number.
- Public key: PA=nA × G, where nA is the Private key generated by the user (Key fob) and G is the point on the Elliptic Curve.
- Encryption: Cm = {kG, M+K PA} (cipher text), where K is the random integer chosen at the beginning and M is the Mapped point on the Elliptic curve.
- Message=(M+(K × PA)) - (K × G × nA), Because PA=nA × G, M(plaintext)

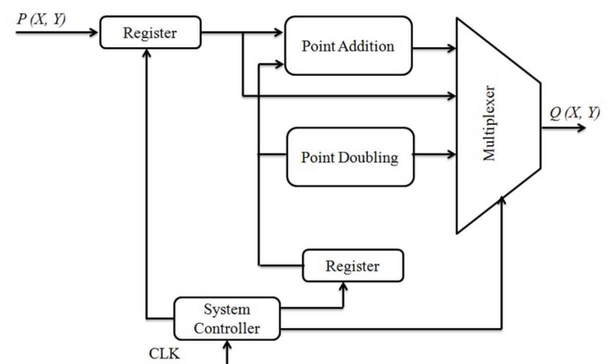

Figure 5: Overall ECC Processor architecture

Where M is the message point corresponding to the message. The Encryption operation generates a pair of points {C1, C2}.

Point addition is a computation method used to add two different points over a finite field. Here, λ is the slope of the two points. Its computation is different for point addition and point doubling as shown in equations (1) and (2). Subtraction is performed employing two's complement addition.

$$\lambda = \frac{Y_2 - Y_1}{X_2 - X_1} \quad (1)$$

$$\lambda = \frac{3x_1^2 + a}{2Y_1} \quad (2)$$

Point doubling is performed using multiplication architecture with both inputs the same. Here also division is necessary to compute point doubling. The point addition has been performed with equation (3) and the hardware architecture is shown in Figure 6. The multiplications are performed with shift and add method with modulus operation.

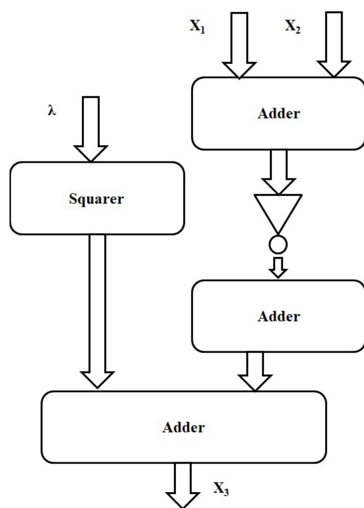

Figure 6a: Architecture for Calculating X_3

$$\begin{aligned} X_3 &= \lambda^2 - X_1 - X_2 \\ Y_3 &= (X_1 - X_3)\lambda - Y_1 \end{aligned} \quad (3)$$

Point Multiplication

Point multiplication [6] is the operation that multiplies a point with an integer. Montgomery ladder technique is used to perform point addition and point doubling in parallel. In this algorithm, two registers are used to store the intermediate results. Initially, one register loaded with an input point and another loaded with doubling

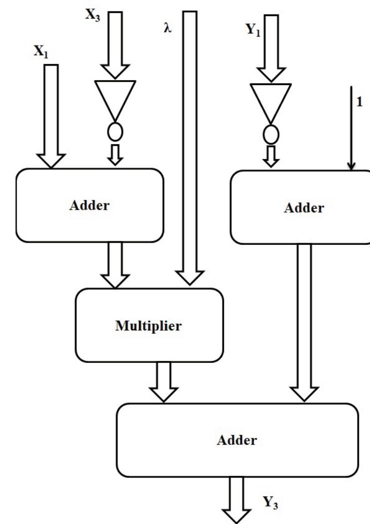

Figure 6b: Architecture for Calculating Y_3

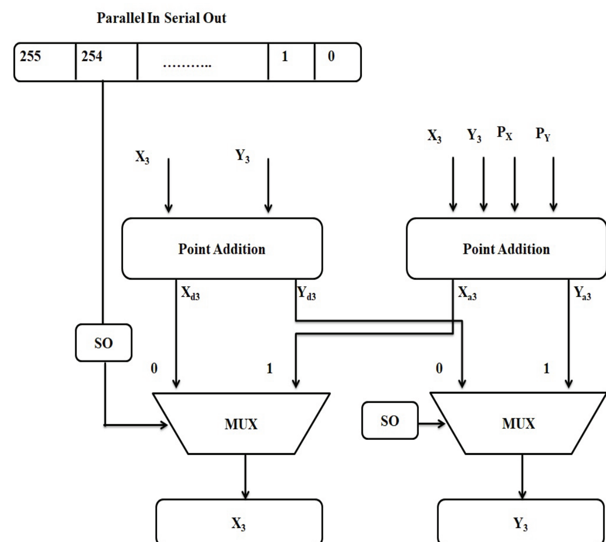

Figure 7: Architecture for Point Multiplication

of the input point. Then a loop is needed to run this algorithm. So, the serial shift register is used during every iteration. The sequence of iterations should be from n-2 to 0. The integer value which needs to be multiplied with the point is loaded into the shift register. Once it gets loaded, shifting should start from (n-2)-th bit to the 0th bit. The shifted bit decides which operation will be performed and what content will be loaded into the registers. If it is 1, the first register is loaded with point addition result and the second register is loaded with point doubling result. If it is 0, then the second register loaded with point addition result and the first register is loaded with point doubling result. Once all bits get shifted out, the multiplication of the point with the integer is stored in the first register.

Point Multiplication Algorithm:

```
Q1 ←P; Q2 ←2P;
for i from n–2 down to 0
    do
    if ki =1 then
    Q1 ←Q1+Q2;    // point addition
    Q2 ←2Q2;    // point doubling
    else
    Q2 ←Q1+Q2;    // point addition
    Q1 ←2Q1;    // point doubling
end if;
end for;
return Q1;
```

Modular Multiplication Algorithm:

```
Formula : C =(A·B) mod p ;
    C ←0;
    T ←B&'1';
        while T(n–1 downto 0) != 0 loop
        C ←2C;
    If Tn =1 then            //nth bit of T
        C ←C +A;
    end if;
        C ←C mod p;
        T←T(n–1downto0)&'0';  //left-shift operation
    end loop;
    return C;
```

The above algorithm is implemented as shown in Figure 8. In order to perform the multiplication of two integers, left shift and adder are used in this architecture. In this method, a multiplier loaded with the shift register and multiplicand is given to the adder circuit as shown in Figure 8. The shift-left register is used to perform a synthesizable loop operation for the left to right bitwise multiplication.

To determine the end of the loop, a (n+1)-bit temporary variable T is used in which T (n down to 1) is precomputed as the multiplier B and the least significant bit (LSB) of T is pre-computed as 1. One extra bit is added at the LSB to cope with the completion of the left-shift operation in the case of b_0 = 0. The multiplicand A is added to the accumulator in each iteration if the most significant bit (MSB) of T is 1. The content of the accumulator is then reduced to *modulo p* after every addition. In order to perform this modular operation, C is subtracted by the prime numbers *p* and *2p*. As the content of the accumulator is always less than *3p*, subtractions by *p* and *2p* are enough to confine the content below the value of *p*. The subtractions C – p and C –2p are performed by adding the 2's complement of the subtrahends *p* and *2p* to the minuend C.

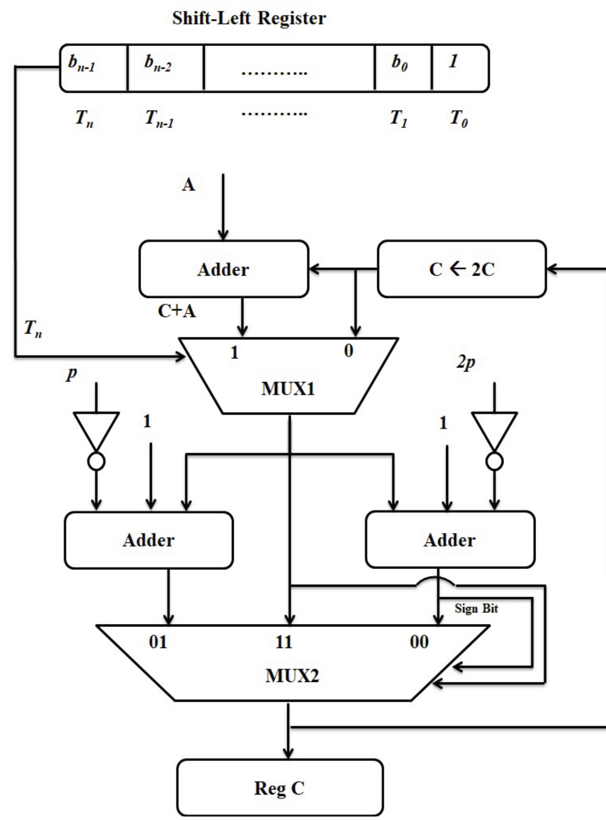

Figure 8: Architecture for Modular Multiplication

The comparisons C ≥ *p* and C ≥ *2p* are performed by checking the sign bits of the differences C–*p* and C –*2p*, respectively. At the end of every iteration, T is shifted to the left by one bit. After performing 'n' iterations, T(n–1 down to 0) is shifted to zero value and the content of the accumulator is stored in register 'Reg C', which is the final modular product of integers A and B. The module comprises two multiplexers, in which MUX1 is used to keep the content of the accumulator unchanged if Tn = 0; or add A to the accumulator if Tn = 1; and MUX2 is used for performing C mod *p*. At $(n+1)^{th}$ clock cycle, the result for multiplication of two inputs is available.

5.3 2*2 Vedic multiplier

Considering two-bit numbers A (A_1A_0) and B (B_1B_0), the 2×2 Vedic multiplication is carried out as depicted in Figure 9. The logical expression of the final product is as shown in equation 4,

$$P_0 = A_0.B_0 \qquad P_1 = (A_1.B_0) \oplus (A_0.B_1)$$
$$P_2 = (A_0.A_1.B_0.B_1) \oplus (A_1.B_1) \qquad P_3 = A_0.A_1.B_0\,B_1 \tag{4}$$

This process consumes 4 AND gates and 2 EXOR gates.

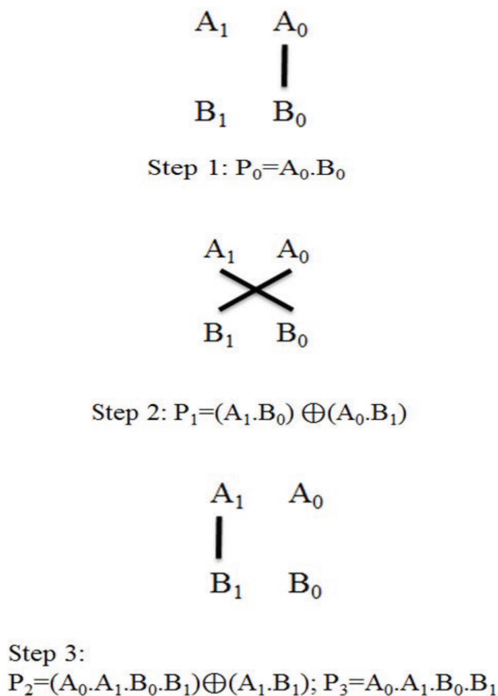

Figure 9: Graphical representation of 2*2 Vedic multiplication steps

*4*4 Vedic multiplier*

The 4-bit Vedic multiplier comprises four 2-bit Vedic multipliers, three 4-bit full adders & one half adder gate. The two 4-bit inputs A_i ($A_3A_2A_1A_0$) and B_i ($B_3B_2B_1B_0$) are applied to the 2-bit Vedic multiplier, and then they are forwarded to the 4-bit adder. The output from the RCA adder consists of 4-bit sum output and a 1-bit carry value. The half adder is used to sum the carry at the first two phases of the ripple carry adder. The output of the 4-bit multiplier consists of an 8-bit product term

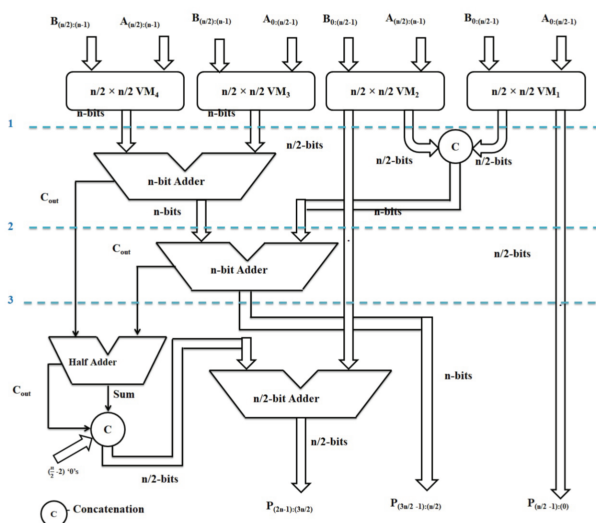

Figure 10: Generalized construction of n-bit Vedic Multiplier

(P_i - P_7…P_0) [25]. Here, the pipeline technique is introduced at 3 levels mentioned in Figure 10 (numbered 1, 2 and 3) by means of inserting registers. Similarly, higher order Vedic multipliers are constructed with the 2-bit VM_i as the base module and RCA adders for summation of the partial products. The n-bit Vedic multiplier uses four n/2-bit multipliers, two n-bit RCA adders, one n/2-bit adder, and one Half adder as shown in Figure 10.

6 Results and discussion

6.1 FPGA implementation and analysis

This section presents the FPGA implementation for the proposed ECC processor architecture. The necessary parameters such as curve order, coefficients and base point coordinates are selected based on the NIST standard. Here, we have considered a 256-bit ECC processor. The ECC processor is designed using Verilog HDL and simulated using ModelSim. It was synthesized, placed and routed using Xilinx ISE 14.6. In the proposed methodology, the used FPGA platforms were Virtex- 6 (XC6VLX240T-1FF1156) and Virtex-7 (XC7VX485T-2FFG1761C) with the goal to achieve optimal speed and area. The implementation results of the proposed 256-bit ECC module are summarized in Table 2. In which, the ECC is implemented with or without pipeline in Vedic multiplier.

The performance factors throughput and efficiency are calculated based on equation (5) [6, 22, 26, 27].

$$\left.\begin{aligned}&Cycle = Time\ for\ one\ ECPM \times maximum\ frequency\\&AT/Bit = Area\text{-}Delay\ product / Number\ of\ Bits\\&Throughput = (maximum\ frequency \times\\&number\ of\ bits) / number\ of\ clock\ cycles\\&Efficiency = Throughput / area\end{aligned}\right\} \quad (5)$$

The Simulation results of point addition, point doubling, public key calculation, data encryption and decryption are shown in Figure 11 (a-e). In Figure 11a, the input points are (a,b) (c,d) and the resultant point addition is available in (x_3, y_3). It is produced in 945 clock cycles. Figure 11b shows the simulation result of point doubling, where (x_p,y_p) are input point and the result (x_3, y_3) is produced in 430 clock cycles. Figure 11c shows the simulation result of public key generation. The complete ECPM simulation is shown in Figure 11d, which is completed in 232.21k clock cycles. When the interim states are having less than 256-bits, then the ECPM gets completed in fewer cycles.

The pipelined Vedic multiplier based ECC implemented on Virtex-7 occupies 8.23k slices, takes 32.2k clock cy-

Figure 11a: Simulation Result of Point Addition

Figure 11b: Simulation Result of Point Doubling

Figure 11c: Simulation Result of Public Key Calculation

Figure 11d: Simulation Result of Encryption

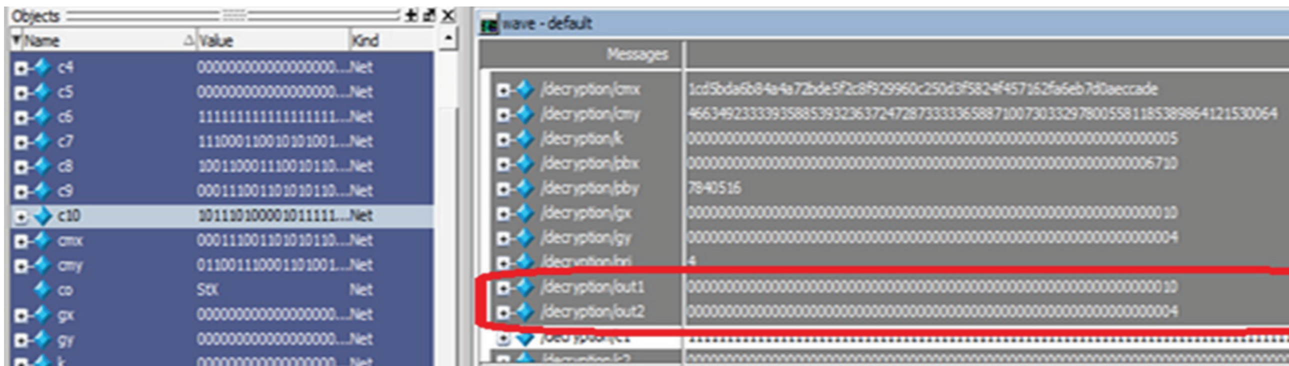

Figure 11e: Simulation Result of Decryption

cles for process completion, the maximum operating frequency is 192.5MHz, and the process takes 0.9365ms to complete. The Area-Delay product and throughput are 7.922 and 273.36kbps, respectively. The pipelined ECC has 32.31% efficiency. The pipelined Vedic ECC has 22.36% and 20.18% improvement in throughput and efficiency with respect to non-pipelined implementation. This is due to the increased frequency of operation (226.8MHz) of pipelined architecture. It leads to additional 2.72% overhead on the area; but the area-delay overhead is reduced by 20.19%.

Table 2: Performance of Proposed Vedic multiplier based ECC

	Platform	Number of bits	Number of Slices (k)	Clock Cycles (k)	Maximum Frequency (MHz)	Time (ms)	Area Delay Product	AT/B	Throughput (kbps)	Efficiency
No Pipeline	Virtex-7	256	8.23	232.2	192.5	1.2062	9.927026	0.0387774	212.23	25.79
Pipeline			8.46	212.4	226.8	0.9365	7.92279	0.0309484	273.36	32.31
No Pipeline	Virtex-6		8.82	232.2	186.2	1.247	10.99854	0.042963	205.29	23.27
Pipeline			9.12	212.4	216.8	0.98	8.9376	0.0349125	261.3	28.65
Percentage of improvement	Virtex-7		2.72	8.53	15.12	22.36	20.19	20.19	22.36	20.18
	Virtex-6		3.29	8.53	14.11	21.41	18.74	18.74	21.44	18.78

Table 3: Performance comparison of Proposed ECC

Ref	Year	Platform	Number of bits	Number of Slices (k)	Clock Cycles (k)	Maximum Frequency (MHz)	Time (ms)	Area Delay Product	AT/B	Throughput (kbps)	Efficiency
Ours	woP	Virtex-7	256	8.23	232.2	192.5	1.2062	9.927026	0.03878	212.23	25.79
	wP			8.46	212.4	226.8	0.9365	7.92279	0.03095	273.36	32.31
	woP	Virtex-6		8.82	232.2	186.2	1.247	10.99854	0.04296	205.29	23.27
	wP			9.12	212.4	216.8	0.98	8.9376	0.03491	261.30	28.65
26	2020	Virtex-7	256	6.5	198.7	104.39	1.9	12.35	0.0482	134.49	20.69
26	2020	Virtex-6	256	6.6	198.7	93.23	2.13	14.05	0.0549	120.12	18.20
28	2019	Virtex-7	256	8.9	262.7	177.7	1.48	13.17	0.051	173.2	19.46
28	2019	Virtex-6	256	9.2	262.7	161.1	1.63	15.00	0.059	157.00	17.06
29	2018	Virtex-6	256	65.6	153.2	327	0.47	30.83	0.120	546.42	8.33
30	2018	Virtex-4	256	9.4 + 14DSPs	610	20.44	29.84	280.5	1.096	8.58	0.91
31	2017	Kintex-7	256	11.3	397.3	121.5	3.27	63.95	0.144	78.28	6.92
32	2017	Virtex-7	256	24.2	215.9	72.9	2.96	71.63	0.280	1816.20	3.57
33	2017	Virtex-4	193	12	459.9	36.5	12.6	151.2	0.783	20.32	1.69
34	2017	Virtex-4	256	20.6	191.6	49	3.91	80.55	0.315	65.47	3.18
27	2016	Virtex-4	256	13.2	200	40	5	66	0.258	51	3.88
35	2016	Virtex-4	192	35.7	207.1	70	2.96	105.67	0.550	86.53	2.42
36	2016	Virtex-5	256	8.7	361.6	160	2.26	19.66	0.077	113.27	13.02

woP – Without Pipeline; wP – with Pipeline; [b]-calculated by author

The same pipelined architecture has 261.30kbps throughput and 28.65 efficiency in Virtex 6. The pipeline structure has 21.44% and 18.78% improvement in throughput and efficiency with respect to non-pipelined implementation with 3.29% area overhead. Significantly, the maximum frequency of operation and time consumption are improved by 14.11% and 21.41% respectively.

The performance characteristics of ECC implementation in FPGA are shown in Table 3. Here, varieties of FPGA families such as Virtex-4, 5, 6, 7 and Kindtex-7 are used for implementation purposes. Most of the researchers designed for the 256-bit size ECC, except in [33, 35], where 192 and 193-bit are considered respectively. The significant performance factors considered for the analysis are Area, the number of clock cycles, maximum operating frequency, area-delay product, throughput and efficiency.

From Table 3, it is observed that higher frequency of operation leads to a reduction in the required number of clock cycles, completion time and increases the throughput. The proposed pipelined Vedic multiplier has an optimized area, speed and throughput. The ECC based security systems are performing well against the attacks [37] such as algebraic attack, brute force attack and statistical attack [38, 39] and protects confidential data hiding in spatial images [40].

In [6], efficiency is calculated using throughput and area, which is represented in the equation (5). The same has been calculated and shown for comparison in Table 3. The efficiency of the proposed method is comparatively better with respect to all the previous works. Moreover, the pipelining of the multiplication process increases the efficiency by another 25%. The earlier FPGA studies using Virtex-I Pro, Virtex-E and Spartan 4 are omitted for comparison in Table 3 due to their nature of high power consumption and the limited number of Input/Outputs.

6.2 Security Evaluation and Analysis

The security evaluation criteria which are essential for the Remote Keyless Entry system are shown in Table 4. In order to illustrate the effectiveness of the proposed ECC scheme evaluation, a comparative assessment of 10 schemes for the RKE system has been done. By evaluating the 10 criteria of security attacks stated in [41, 42, 51] the performance of the proposed Vedic based ECC has been evaluated. The results are summarized in Table 5.

Table 4: Security Evaluation criteria

Short Form	Evaluation Criteria
C1	No password verifier-table
C2	Resist password guessing threat
C3	Defend replay attack
C4	Defend session key temporary information attack
C5	Accurate login and password change phase
C6	Defend user un-traceability attack
C7	Mutual authentication
C8	Facilitates user anonymity
C9	Defend insider attack
C10	Facilitates forward secrecy property

Table 5: Security comparison among the authentication schemes

Ref.	Year	Evaluation Criteria									
		C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
Ours	2022	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
42	2022	✓	✓	✓	✓	×	✓	✓	✓	✓	✓
43	2020	✓	✓	✓	✓	×	×	✓	✓	✓	✓
44	2019	✓	✓	✓	✓	×	×	✓	✓	✓	✓
45	2019	✓	✓	✓	✓	×	✓	✓	✓	×	×
46	2018	✓	✓	✓	✓	×	×	✓	✓	×	✓
51	2018	×	✓	×	✓	✓	✓	✓	✓	✓	✓
47	2018	✓	✓	✓	✓	×	×	✓	✓	×	✓
48	2018	✓	×	✓	✓	×	×	✓	✓	×	✓
49	2018	✓	✓	✓	✓	×	×	✓	✓	×	×
50	2017	✓	✓	✓	✓	×	×	✓	✓	×	×

Table 6: Evaluation of computational cost

Ref.	Year	Authentication		Time Period (Sec)		
		User	Car Sensor	User	Car Sensor	Total
Ours	2022	$T_{be} + 2T_H$	$T_S + 2T_H$	0.0600	0.5733	0.6333
42	2022	$T_{be} + 3T_H$	$T_{se} + 4T_H + T_S$	0.0605	0.583	0.6435
43	2020	$T_{be} + 3T_H$	$T_{se} + TS + 4T_H$	0.0605	0.583	0.6435
44	2019	$T_{PM} + 3T_H$	$2T_{PM} + 4T_H$	1.0518	2.0523	3.1041
45	2019	$5T_H$	$5T_H$	0.0528	0.0528	0.1056
46	2018	$T_C + 3T_H$	$2T_C + 6T_H$	0.5738	1.0973	1.6711
51	2018	$5T_H$	$11T_H$	0.0528	0.0558	0.1086
47	2018	$T_{PM} + 2T_H$	$2T_{PM} + 4T_H$	1.0513	2.0523	3.1036
48	2018	$6T_H$	$5T_H$	0.0533	0.0528	0.1061
49	2018	$8T_H$	$6T_H$	0.0543	0.0533	0.1076
50	2017	$5T_H + T_S$	$7T_H + T_S$	3.0615	0.5758	3.6373

T_H: time complexity of a hash function; T_{PM}: the time complexity of ECC point multiplication operation; T_S: time complexity of a symmetric key encryption/decryption operation; T_{ME}: time complexity of a modular exponentiation operation

In order to evaluate the execution time of the proposed protocol and relevant protocols, we have assumed that the hash function, modular exponentiation operation, a symmetric key encryption/decryption operation and point multiplication operation require 0.0005 seconds, 0.522 seconds, 0.0087 seconds and 0.0503 seconds [51], respectively. The computation cost for the RKE is estimated and compared with the existing literature in Table 6. It is observed that the proposed method is competent in computation cost with the previously published works. The proposed RKE has 1.58% improvement compared to the recently available method [42]. Hence, the proposed pipelined vedic ECC can be incorporated in RKE for effective secured communication of various applications such as smart cards [52], mobile devices [53] and wireless sensor networks [42].

7 Conclusion

In this paper, a high-speed, area-efficient ECC processor is designed on the Koblitz curve secp256k1 for the Remote Keyless Authentication system. It supports 256-bit point addition and point multiplication over a prime field. A novel method of multiplication using Urdhva Tiryagbhyam is adopted for scalar multiplication. The speed of multiplication is improved by incorporating the pipeline technique. The proposed pipelined Vedic multiplier based ECC processor is implemented in the Xilinx Virtex-7 and Virtex-6 platforms for the 256-bit prime field. The implemented processor performs a single 256-bit multiplication in 1.2062ms with a maximum clock frequency of 192.5MHz, which provides 212.23kbps throughput and occupies 8.23k slices in Virtex-7 FPGA. Incorporating pipeline in scalar multiplication improves the maximum clock frequency up to 15.12%, and reduces time by 22.36%, which in turn increases the throughput by 22.36%. The pipeline has an additional area overhead of 2.72% and 3.29% in Virtex-7 and Virtex-6 respectively. Also, the computational cost of the proposed method is evaluated, which shows 1.58% improvement from the most recent literature. The pipelined Vedic multiplier based ECC processor outperforms the existing designs in terms of area, clock cycle count, operating frequency, time, area-delay product, throughput, efficiency and security. Based on the overall performance of the proposed ECC processor, it can be concluded that it is a reliable choice for wireless communication technologies as well as for resource constrained applications.

8 Conflicts of interest

The authors declare that there are no conflicts of interest regarding the publication of this manuscript.

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Electronically Tunable Mixed Mode Universal Filter Employing Grounded Passive Components

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Abstract: A recently developed active element, namely Voltage Differencing Differential Voltage Current Conveyor (VD-DVCC), is employed in the design of electronically tunable mixed-mode universal filter. The filter provides low pass (LP), high pass (HP), band pass (BP), band reject (BR) and all pass (AP) responses in voltage-mode (VM), current-mode, trans-impedance-mode (TIM) and trans-admittance-mode (TAM). The filter employs two VD-DVCCs, three resistors and two capacitors. All the passive components employed are grounded. The attractive features of the filters include: (i) ability to operate in all four modes, (ii) use of grounded passive components, (iii) tunability of Q factor independent of pole frequency, (iv) high input impedance for VM and TIM mode, (v) high output impedance explicit current output for CM and TAM and (vi) no requirement for double/negative input signals (voltage/current) for response realization. The VD-DVCC is designed and validated in Cadence virtuoso using 0.18 µm PDK at supply voltage of ±1 V. The operation of filter is examined at 5.305 MHz frequency. The non-ideal gain and sensitivity analysis is also carried out to study the effect of process and components spread on the filter performance. The obtained results bear close resemblance with the theoretical findings.

Keywords: communication, mixed-mode, current conveyor, filter, signal processing, VD-DVCC

Elektronsko nastavljiv univerzalni filter mešanega načina z ozemljenimi pasivnimi komponentami

Izvleček: Nedavno razviti aktivni element napetostni diferenčni napetostni tokovni transporter (VD-DVCC) je uporabljen pri zasnovi elektronsko nastavljivega univerzalnega filtra z mešanim načinom delovanja. Filter omogoča nizko prepustnost (LP), visoko prepustnost (HP), pasovno prepustnost (BP), pasovno zavrnitev (BR) in vse prepustne odzive (AP) v napetostnem (VM), tokovnem, trans-impedančnem (TIM) in trans-admitančnem (TAM) načinu. Filter uporablja dva VD-DVCC, tri upore in dva kondenzatorja. Vse uporabljene pasivne komponente so ozemljene. Privlačne lastnosti filtrov so: (i) možnost delovanja v vseh štirih načinih, (ii) uporaba ozemljenih pasivnih komponent, (iii) nastavljivost faktorja Q neodvisno od frekvence polov, (iv) visoka vhodna impedanca za način VM in TIM, (v) visoka izhodna impedanca z eksplicitnim izhodnim tokom za CM in TAM ter (vi) ni potrebe po dvojnih/negativnih vhodnih signalih (napetost/tok) za realizacijo odziva. VD-DVCC je zasnovan in preverjen v Cadence virtuoso z uporabo 0,18 µm PDK pri napajalni napetosti ±1 V. Delovanje filtra je preverjeno pri frekvenci 5,305 MHz. Izvedena je tudi analiza neidealnega ojačenja in občutljivosti, da bi preučili vpliv razpršenosti procesa in komponent na delovanje filtra. Dobljeni rezultati so zelo podobni teoretičnim ugotovitvam.

Ključne besede: komunikacija, mešani način, tokovni transporter, filter, obdelava signalov, VD-DVCC

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1 Introduction

The current mode-active elements (CM-AEs) are extensively employed in designing universal frequency filters [1-4]. The CM-AEs exhibits enhanced dynamic range, wide bandwidth, simple structure, low power consumption and greater linearity [2-3]. Numerous filter structures employing CM-AEs can be found in the literature [1, 3]. Most of the proposed filters can work

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only in single mode of operation i.e. voltage-mode (VM), current-mode (CM), trans-admittance-mode (TAM), and trans-impedance-mode (TIM) [1-3,5]. In present day complex signal processing systems, the interaction between CM and VM circuits is required. This task can be performed by TAM and TIM filters that not only perform signal processing, but also provide interfacing between VM and CM systems [6-10]. The development of mixed-mode universal filters that can provide LP, HP, BP, BR and AP responses in CM, VM, TAM and TIM modes of operation are best suited for the task.

Numerous exemplary mixed-mode filter topologies have been developed [6-41] that employ CM-AEs. The mixed mode filters can be categorised into two groups (i) single input multi output (SIMO), (ii) multi input single output (MISO) structures. The filter structures [6-10**,** 12-13, 15-19, 22-24, 28, 31-33, 35, 37-39, 41] employ CM-AEs in excess of two. The designs in [6-7, 10,12,22,28-30, 36, 37, 39] employ more than five passive components. The filter structures in [6, 7, 10-12, 14, 20-22, 25, 27-30, 34, 36, 39, 48-52] does not employ all grounded passive components. The filters in [6-7, 9-13, 18, 19, 21, 24, 25, 27, 30, 32, 33, 36, 39] do not provide frequency control independent of quality factor. The filter topologies [6, 8, 9, 11, 13, 15, 16, 18, 21, 23, 25, 26-28, 32, 34, 41, 50] do not provide all five filter responses in VM, CM, TAM, and TIM operation. The filter structures [6, 7, 10-12, 14, 16, 22, 25, 27-30, 34, 36, 37, 39, 41] lack inbuilt tunability. Some recent designs of the mixed mode filters proposed by the authors [48-52] suffer from one or more of the above discussed drawbacks. A detailed comparison of the state-of-the-art MISO filters with the proposed design is presented in Table 1, based on the following important measures of comparison: (i) number of CM-AEs employed, (ii) number of passive components needed, (iii) employment of all grounded passive components, (iv) no requirement for resistive matching except for obtaining a single response, (v) provision to control quality factor (*Q*) independent of the centre frequency, (vi) ability to provide all five filter responses in all four modes of operation, (vii) low output impedance for VM and TIM modes, (viii) availability of explicit current output in CM and TAM, (ix) no requirement for double/negative input signals (voltage/current), (x) inbuilt tunability, and (xi) test frequency.

It can be inferred from the literature review and table 1 that not all the proposed mixed mode filter structures work in all four modes of operation. It is also deduced from the literature survey that limited number of mixed-mode filters are available and to fill this technological void additional novel mixed-mode filter structures are needed. In this research, a recently developed CM-AE, the Voltage Differencing Differential Voltage Current Conveyor (VD-DVCC) is utilized in design of mixed-mode filter. The design requires two VD-DVCCs, two capacitors, and three resistors. The striking features of the proposed filter are: (i) ability to work in all four modes of operation, (ii) provision for inbuilt tunability, (iii) the filters enjoy low active and passive sensitivities, and (iv) use of all grounded passive components. Beside these the filters enjoy all the properties mentioned in Table 1 except (vii). The design and simulation of the VD-DVCC is done in Cadence Virtuoso using 0.18µm PDK. The simulation results bear close resemblance with the theoretical findings.

2 Voltage differencing differential voltage current conveyor (VD-DVCC)

The VD-DVCC is a newly proposed [42] CM-AE that possess features of Differential Voltage Current Conveyor (DVCC) [41] and Operational Transconductance Amplifier (OTA). The voltage current relations of the VD-DVCC are given in Equations (1)-(4) and the block diagram is shown in Figure 1.

$$I_W = I_{WC+} = -I_{WC-} = g_m\left(V_P - V_N\right) \tag{1}$$

$$V_X = V_{Y1} - V_W \tag{2}$$

$$I_X = I_{Z+} = -I_{Z-} \tag{3}$$

$$I_{Y1} = I_w = 0 \tag{4}$$

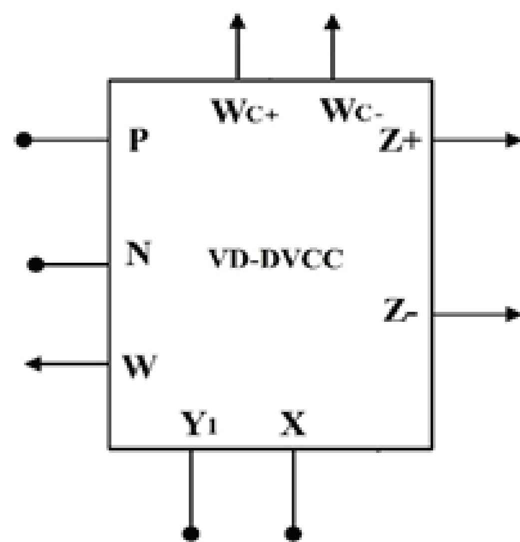

Figure 1: Block Diagram of VD-DVCC

The CMOS implementation of VD-DVCC is presented in Figure 2. The transistors M19-M32 forms the OTA section. The output current of the OTA assuming all tran-

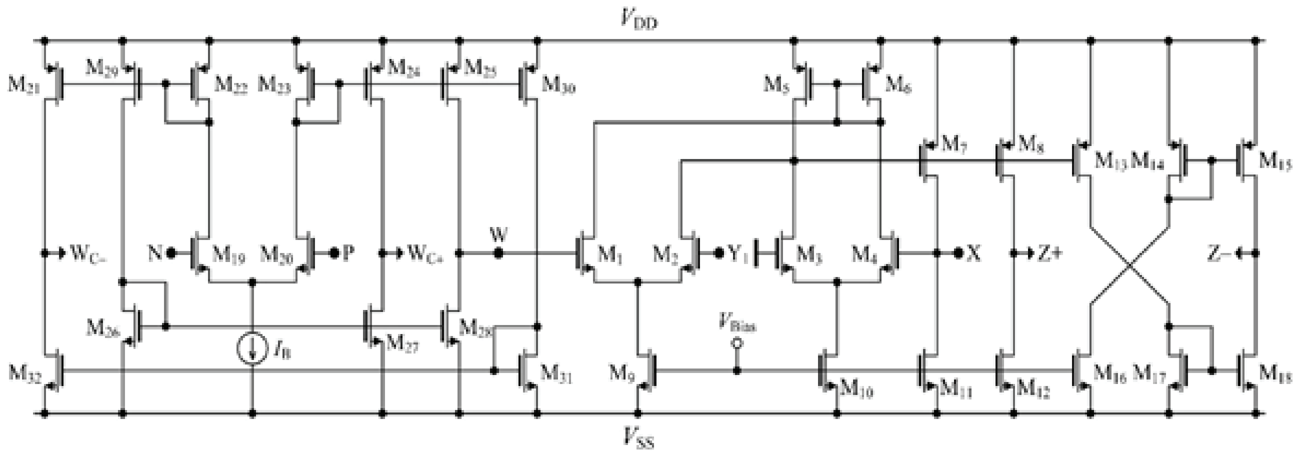

Figure 2: CMOS implementation of VD-DVCC

sistors in saturation region and equal width and length for (M19-M20) will be $I_W = I_{WC} = g_m(V_P - V_N)$. The expression for g_m is given in Equation 5.

$$g_m = \sqrt{\mu_n C_{OX} \frac{W}{L} I_B} \tag{5}$$

Where C_{OX} is the gate oxide capacitance, μ_n is the mobility of electrons in NMOS, g_m denotes the transconductance of OTA set via bias current I_B and W/L is the aspect ratio of the transistors. Extra copies of the OTA current can be utilized, if necessary, for the applications. The second stage comprising of transistors M1-M18 provides algebraic summation of input voltages and current transfer function. The voltage at the X terminal is the algebraic sum of voltages at W and Y_1 terminals. The input current at the X terminal appears at the Z+ and Z- terminals, multiple copies of the current can be easily generated just by adding two extra transistors. The N, P, Y_1 terminals are high impedance voltage input terminals. The W, W_{C+}, W_{C-}, Z + and Z - are high impedance current output terminals. The X terminal is low impedance current input terminal.

3 Proposed electronically tunable mixed-mode universal filter

The proposed filter as presented in Figure 3 requires two VD-DVCCs, two capacitors, and three resistors all grounded for the design. For VM and TAM mode of operation the filter has high input impedance. In addition, the CM and TAM responses are available from explicit high impedance terminals. Furthermore, in the design the capacitors are connected to high impedance terminals so they will absorb the parasitic associated with the terminals. Among the three resistors two are connected to the low resistance X terminal so they will accommodate the parasitic resistance present at X terminal. The important features of the filter include: (i) use of grounded passive components, (ii) employment of minimum number of passive components, (iii) no need for capacitive matching, (iv) no requirement for resistive matching except for AP response, (v) high input impedance in VM and TIM configuration, (vi) ability to provide all five filter responses in all four modes of operation, (vii) availability of explicit current output in CM and TAM, (viii) no requirement for double/negative input signals (voltage/current), and (xi) inbuilt tunability. The operation of the filter in all modes is explained below.

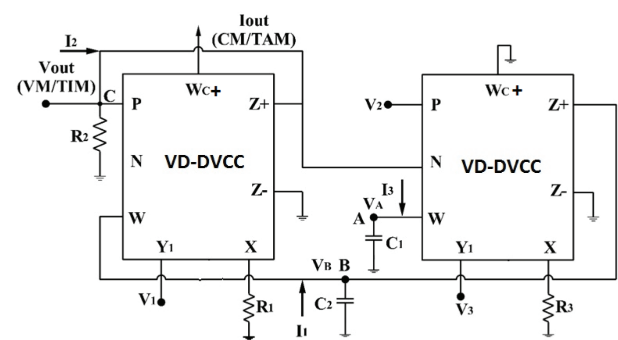

Figure 3: Proposed Mixed-mode Filter

3.1 Operation in VM and TAM mode:

In this mode of operation, the inputs currents ($I_1 - I_3$) are set to zero. The filter is excited with input voltages ($V_1 - V_3$) as per the sequence given in Table 2. The Equations (10-11) give the filter response in VM and TAM modes of operation. The frequency and quality factor are given by Equations (12-13). It can be deduced from the Equations that the Q can be controlled independent of frequency. For all pass response a simple resistive matching of ($R_1 = R_2$) is required which is easy to achieve.

$$V_{out} = \frac{s^2C_1C_2R_2R_3V_1 - SC_1R_2V_3 + R_2g_{m2}V_2}{s^2C_1C_2R_1R_3 + g_{m1}SC_1R_3R_2 + R_2g_{m2}} \quad (10)$$

In Equation 10 the filter gain constants are $H_{oLP} = 1$, $H_{oHP} = \frac{R_2}{R_1}, H_{oBP} = g_1R_2$ by adjusting these parameters the filter gain can be adjusted. As special case for notch pass or bad reject realization if $R_2 > R_1$ then high pass notch (HPN) is obtained and if $R_2 < R_1$ low pass notch (LPN) response is obtained.

$$I_{out\,(TAM)} = g_{m1}V_{out}$$

$$I_{out\,(TAM)} = g_{m1}\left[\frac{s^2C_1C_2R_2R_3V_1 - SC_1R_2V_3 + R_2g_{m2}V_2}{s^2C_1C_2R_1R_3 + g_{m1}SC_1R_3R_2 + R_2g_{m2}}\right] \quad (11)$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{g_{m2}R_2}{C_1C_2R_1R_3}} \quad (12)$$

$$Q = \frac{1}{g_{m1}}\sqrt{\frac{C_2g_{m2}R_1}{C_1R_2R_3}} \quad (13)$$

Table 1: Excitation Sequence for VM and TAM

Response	Inputs			Matching Condition
	V_1	V_2	V_3	
LP	0	1	0	No
HP	1	0	0	No
BP	0	0	1	No
BR	1	0	1	No
AP	1	1	1	$R_1 = R_2$, $R_3g_1 = 1$

3.2 Operation in CM and TIM mode:

In this mode of operation all input voltages () are set to zero. The input currents () are applied according to Table 3. The transfer function for CM and TIM are given in Equations (14)-(15). The complete analysis of the circuit is given below.

$$V_{out(TIM)} = \left[\frac{s^2C_1C_2R_1R_3R_2I_2 - SC_1R_3R_2I_1 + R_2I_3}{s^2C_1C_2R_1R_3 + g_{m1}SC_1R_3R_2 + R_2g_{m2}}\right] \quad (14)$$

$$I_{out\,(CM)} = g_{m1}V_{out}$$

$$I_{out(CM)} = \left[\frac{s^2C_1C_2R_1R_3g_{m1}R_2I_2 - SC_1R_3g_{m1}R_2I_1 + g_{m1}R_2I_3}{s^2C_1C_2R_1R_3 + g_{m1}SC_1R_3R_2 + R_2g_{m2}}\right] \quad (15)$$

In Equation 15 the filter gain constants are $H_{oLP} = \frac{g_1}{g_2}$, $H_{oHP} = g_1R_2, H_{oBP} = 1$ by adjusting these parameters the filter gain can be adjusted.

Table 3: Input current excitation sequence

Response	Inputs			Matching Condition
	I_1	I_2	I_3	
LP	0	0	1	No
HP	0	1	0	No
BR	1	0	0	No
NP	0	1	1	No
AP	1	1	1	$g_1R_2 = 1$, $g_1 = g_2$

4 Non-Ideal and Sensitivity Analysis

The non-ideal model of the VD-DVCC is given in Figure 5. As can be deduced, various parasitic resistance and capacitance appear in parallel with the input and output nodes of the device. The low impedance X node has a parasitic resistance and inductance in series with it. Other non-ideal effects that influence the response of the VD-DVCC are the frequency dependent non-ideal current (), voltage (), and transconductance transfer (γ, γ') gains. These non-ideal gains result in a change in the current and voltage signals during transfer leading to undesired response. Taking in account the non-ideal gains the V-I characteristics of the VD-DVCC in (1) will be modified as follows: $I_W = 0$, $V_X = \beta(V_1 - V_W)$, $I_{Z+} = \alpha_p I_X$, $I_{Z-} = \alpha_N I_X$, $I_W = I_{WC+} = \gamma g_m(V_p - V_N)$, $I_{WC-} = -\gamma' g_m(V_p - V_N)$ where $\beta_m = 1 - \varepsilon_{vm}$, $\alpha_{Pm} = 1 - \varepsilon_{iPm}$, $\alpha_{Nm} = 1 - \varepsilon_{iNm}$, $\gamma_m = 1 - \varepsilon_{gmm}$, (***drugi m subsub***) and $\gamma'_m = 1 - \varepsilon'_{gmm}$ (***drugi m subsub***) for $m = 1, 2$, which refers to the number of VD-DVCCs. Here, ε_{vm} ($|\varepsilon_{vm}| \ll 1$) denote voltage tracking error, ε_{iPm}, ε_{iNm} ($|\varepsilon_{im}|$, $|\varepsilon_{iNm}| \ll 1$) denote current tracking errors, and ε_{gmm}, ε'_{gmm} ($|\varepsilon_{gmm}|$, $|\varepsilon'_{gmm}| \ll 1$) (***drugi m subsub***) denote transconductance errors of the VD-DVCC.

The non-ideal analysis considering the effect of non-ideal current, voltage, and transconductance transfer gains is carried out for MISO (VM, CM, TAM and TIM) configurations to see its effect on the transfer function, f_0, and Q of the proposed filters. The modified expressions of filter transfer functions, f_0', and Q' for the MISO configuration are presented in Equations (16)-(21).

Table 2: Comparative study of the state-of-the-art MISO Mixed mode filter designs with the proposed filter

References	Mode of Operation	(i)	(ii)	(iii)	(iv)	(v)	(vi)	(vii)	(viii)	(ix)	(x)	(xi)
[9]/2003	MISO	6-OTA	2C	Yes	Yes	No	No	No	Yes	Yes	Yes	-
[7]/2004	MISO	7-CCII	2C+8R	No	Yes	No	Yes	No	Yes	Yes	No	-
[12]/2006	MISO	3-CCII	3C+4R+ 2-switch	No	No	No	Yes	No	Yes	Yes	No	-
[13]/2008	MISO	4-OTA	2C	Yes	Yes	No	No	No	Yes	Yes	Yes	2.25 MHz
[19]/2010	MISO	5-OTA	2C	Yes	Yes	No	Yes	No	Yes	No	Yes	1.59 MHz
[20]/2010	MISO	2-MOCCCII	2C+2R	No	Yes	Yes	Yes	No	Yes	Yes	Yes	1.27 MHz
[27]/2010	MISO	CFOA	2C+3R	No	No	Yes	No	No	Yes	No	No	12.7MHz
[24]/2013	MISO	4-MOCCCII	2C	Yes	Yes	No	Yes	Yes	Yes	No	Yes	-
[25]/2013	MISO	1-FDCCII	2C+2R	No	Yes	No	No	No	Yes	Yes	No	10 MHz
[26]/2013	MISO	2-VDTA	2C	Yes	Yes	Yes	No	No	Yes	Yes	Yes	1 MHz
[29]/2016	MISO	1-FDCCII+1-DDCC	2C+6R	No	Yes	Yes	Yes	No	Yes	No	No	1.59 MHz
[37]/2018	MISO	5-DVCC	2C+5R	Yes	Yes	Yes	Yes	No	Yes	Yes	No	1MHz
[40]/2018	MISO	4-CCII	2C+4R	Yes	Yes	Yes	No	No	Yes	Yes	No	31.8 MHz
[38]/2019	MISO	5-OTA	2C	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	3.390 MHz
[39]/2020	MISO	3-DDCCII	2C+4R	No	Yes	No	Yes	No	Yes	Yes	No	3.978 MHz
[48]/2020	MISO/SIMO	2-EXCCTA	2C+4R	No	Yes	Yes	Yes	No	Yes	Yes	Yes	7.622 MHz
[49]/2021	MISO	2-VD-DVCC	2C+3R	No	Yes	Yes	Yes	No	Yes	Yes	Yes	5.305 MHz
[50]/2021	MISO	2-VDBA	2C+2R	No	Yes	Yes	No	Yes	No	Yes	Yes	1.52 MHz
[51]/2021	MISO	3-VDBA	2C+R	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	16.631 MHz
[52]/2022	MISO	1-VD-EXCCII	2C+2R	No	Yes	Yes	Yes	No	Yes	Yes	Yes	8.08 MHz
This Works	MISO	2-VD-DVCC	2C+3R	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	5.305 MHz

** Full nomenclature of the mentioned CM-AEs in Tables 1 and 2 in alphabetical order: CCCCTA: Current controlled current conveyor transconductance amplifier, CCII: Second-generation current conveyor, CFOA: Current feedback operational amplifier, DDCC: Differential difference current conveyor, DPCCII: Digitally programmable second-generation current conveyor, DVCC: Differential voltage current conveyor, EXCCTA: Extra X current conveyor differential input transconductance amplifier, FDCCII: Fully differential second-generation current conveyor, FTFN: Four terminal floating nullor, ICCII: Inverting second-generation current conveyor, MOCCCII: Multi output current controlled current conveyor, MOCCII: Multi output second-generation current conveyor, OTA: Operational transconductance amplifier, VDTA: Voltage differencing transconductance amplifier, VDBA: Voltage differencing buffered amplifier, VD-EXCC: Voltage differencing extra X current conveyor*

$$V'_{out(VM-Mode)} = \left[\frac{s^2 C_1 C_2 R_2 R_3 \alpha_{P1} \beta_1 V_1 - S C_1 R_2 \alpha_{P2} \beta_2 \alpha_{P1} \beta_1 V_3 + \alpha_{P2} \beta_2 \gamma_2 g_{m2} R_2 g_2 V_2}{s^2 C_1 C_2 R_1 R_3 + g_{m1} S C_1 R_3 R_2 \alpha_{P1} \beta_1 \gamma_1 + \alpha_{P2} \beta_2 \gamma_2 \alpha_{P1} \beta_1 R_2 g_{m2}} \right] \tag{16}$$

$$I'_{out(TAM-Mode)} = \gamma_1 g_{m1} \left[\frac{s^2 C_1 C_2 R_2 R_3 \alpha_{P1} \beta_1 V_1 - S C_1 R_2 \alpha_{P2} \beta_2 \alpha_{P1} \beta_1 V_3 + \alpha_{P2} \beta_2 \gamma_2 g_2 R_2 g_{m2} V_2}{s^2 C_1 C_2 R_1 R_3 + g_{m1} S C_1 R_3 R_2 \alpha_{P1} \beta_1 \gamma_1 + \alpha_{P2} \beta_2 \gamma_2 \alpha_{P1} \beta_1 R_2 g_{m2}} \right] \tag{17}$$

$$I'_{out(CM-Mode)} = \gamma_1 g_{m1} \left[\frac{s^2 C_1 C_2 R_1 R_3 R_2 I_2 - S \alpha_{P1} \beta_1 C_1 R_3 R_2 I_1 + R_2 \alpha_{P1} \beta_1 \alpha_{P2} \beta_2 I_3}{s^2 C_1 C_2 R_1 R_3 + g_{m1} S C_1 R_3 R_2 \alpha_{P1} \beta_1 \gamma_1 + \alpha_{P2} \beta_2 \gamma_2 \alpha_{P1} \beta_1 R_2 g_{m2}} \right] \tag{18}$$

$$V'_{out(TIM-Mode)} = \left[\frac{s^2 C_1 C_2 R_1 R_3 R_2 I_2 - S \alpha_{P1} \beta_1 C_1 R_3 R_2 I_1 + R_2 \alpha_{P1} \beta_1 \alpha_{P2} \beta_2 I_3}{s^2 C_1 C_2 R_1 R_3 + g_{m1} S C_1 R_3 R_2 \alpha_{P1} \beta_1 \gamma_1 + \alpha_{P2} \beta_2 \gamma_2 \alpha_{P1} \beta_1 R_2 g_{m2}} \right] \tag{19}$$

$$f_0' = \frac{1}{2\pi}\sqrt{\frac{\alpha_{P2}\beta_2 Y_2 \alpha_{P1}\beta_1 R_2 g_{m2}}{C_1 C_2 R_3 R_1}} \tag{20}$$

$$Q' = \frac{1}{Y_1 g_{m1}}\sqrt{\frac{\alpha_{P2}\beta_2 C_2 Y_2 g_{m2} R_1}{\alpha_{P1}\beta_1 C_1 R_2 R_3}} \tag{21}$$

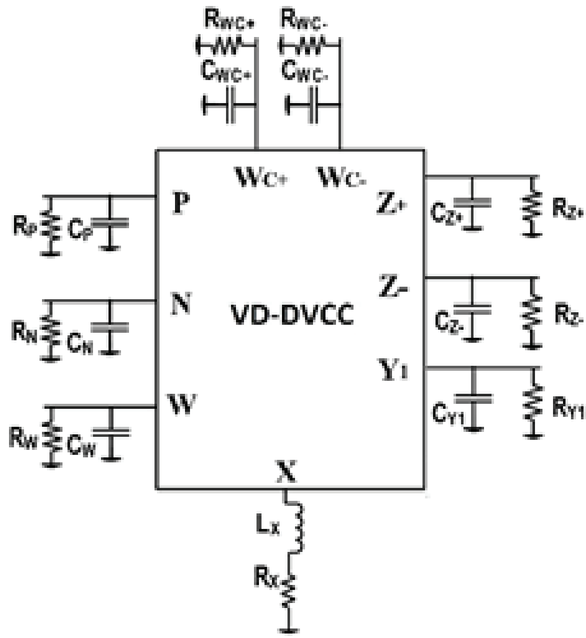

Figure 4: Non-ideal model of VD-DVCC with parasitics

The sensitivities of ω_0' and Q' with respect to the non-ideal gains and passive components are given below.

$$S^{\omega_o'}_{g_{m2}} = S^{\omega_o'}_{\alpha_{P2}} = S^{\omega_o'}_{\beta_2} = S^{\omega_o'}_{\alpha_{P1}} = S^{\omega_o'}_{\beta 1} = S^{\omega_o'}_{R_2} = S^{\omega_o'}_{\gamma_2} = -S^{\omega_o'}_{C_1} = -S^{\omega_o'}_{C_2} = -S^{\omega_o'}_{R_3} = -S^{\omega_o'}_{R_1} = \frac{1}{2} \tag{22}$$

$$S^{Q'}_{\alpha_{P2}} = S^{Q'}_{\beta_2} = -S^{Q'}_{C_1} = S^{Q'}_{\gamma_2} = S^{Q'}_{g_{m2}} = S^{Q'}_{C_2} = -S^{Q'}_{\alpha_{P1}} = -S^{Q'}_{\beta_1} = S^{Q'}_{R_1} = -S^{Q'}_{R_3} = -S^{Q'}_{R_2} = \frac{1}{2}, \tag{23}$$

$$-S^{Q'}_{\gamma_1} = -S^{Q'}_{g_{m1}} = 1, \tag{24}$$

The sensitivities are low and have absolute values not higher than unity.

5 Simulation and validation

To verify the proposed mixed-mode filter it is designed and simulated in Cadence virtuoso design software. The newly proposed VD-DVCC is designed in 0.18 µm Silterra Malaysia technology at a supply voltage of ±1V. The width and length of the transistors used are given in Table 4. The bias current of the OTA is fixed at 47 µA resulting in transconductance of 500 µS. The layout of the VD-DVCC is given in Figure 5 it occupies an area of 50.2*21.50µm^2.

Table 4: Width and Length of the MOS transistors

Transistors	Width (µm)	Length (µm)
M1-M4	4.5	0.36
M5-M6	20	0.36
M7-M8, M13	17.5	0.36
M14-M15	8.75	0.36
M9-M10	8.75	0.36
M11-M12, M16	13.5	0.36
M17-M18	17.5	0.36
M19-M20	1.8	0.36
M21-M25, M29-M30	3	0.72
M26-M28, M31-M32	8	0.36

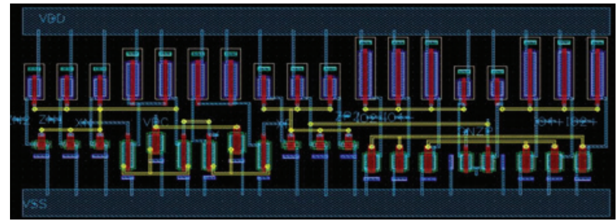

Figure 5: The complete layout of the VD-DVCC

The filter is designed for centre frequency of 5.305 MHz and quality factor of 1 by selecting passive component as $R_1 = R_2 = R_3 = 2k\Omega$ $C_1 = C_2 = 15pF$ and $g_m = 500$ µS. The power dissipation of the filter is found to be 3.48 mW. All five filter responses in VM, CM, TAM and TIM modes are presented in Figures 6-13.

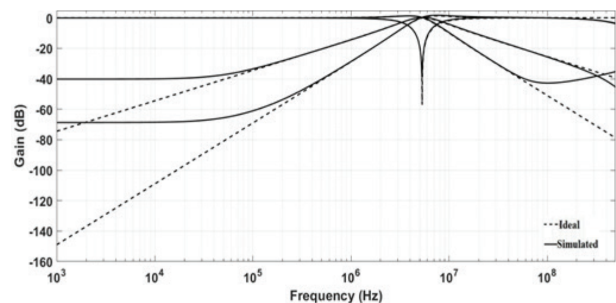

Figure 6: VM MISO configuration: Frequency responses of the LP, BP, HP, and BR filter

To examine the signal processing capability of the proposed universal filter the transient analysis is carried out in VM mode for HP, LP, NP and BP responses. A VM

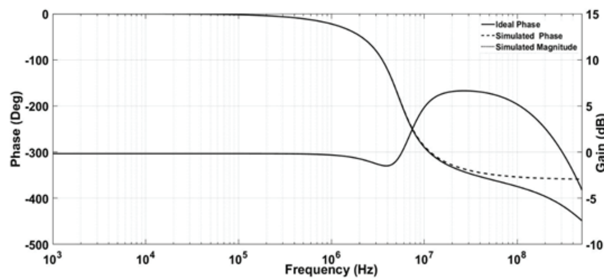

Figure 7: VM MISO configuration: Gain and phase responses of the AP filter

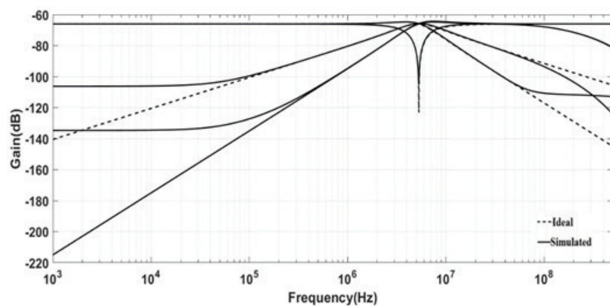

Figure 8: TAM MISO configuration: Frequency responses of the LP, BP, HP, and BR filter

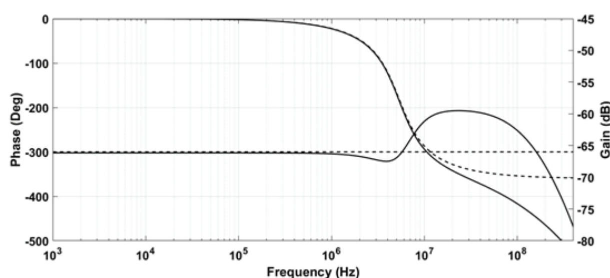

Figure 9: TAM MISO configuration: Gain and phase responses of the AP filter

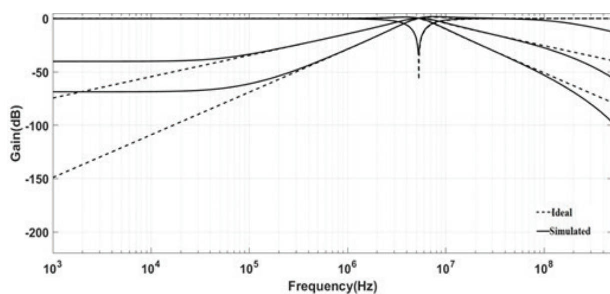

Figure 10: CM MISO configuration: Frequency responses of the LP, BP, HP, and BR filter

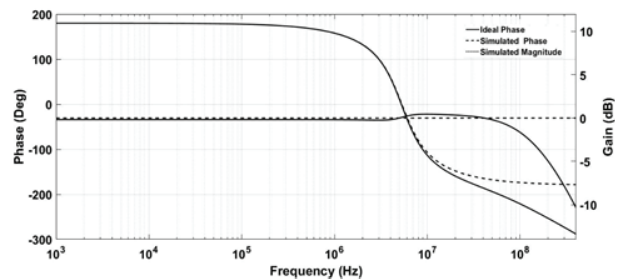

Figure 11: CM MISO configuration: Gain and phase responses of the AP filter

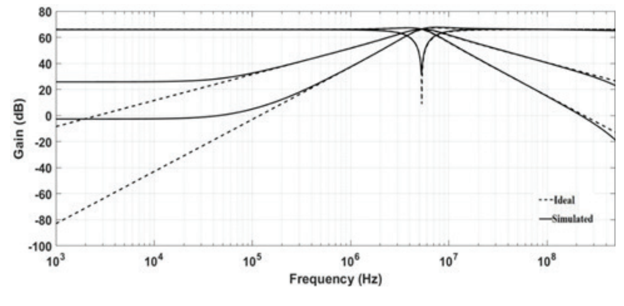

Figure 12: TIM MISO configuration: Frequency responses of the LP, BP, HP, and BR filter

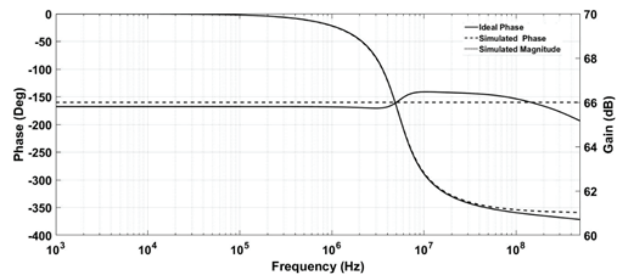

Figure 13: TIM MISO configuration: Gain and phase responses of the AP filter

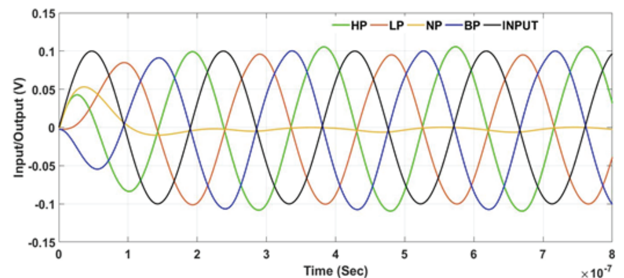

Figure 14: VM MISO configuration: Transient analysis results for BP, HP, LP filter configurations

sinusoidal signal of 100 mV p-p and 5.305 MHz frequency is applied at the input and the output is analysed as presented in Figure 14. Similarly, a CM sinusoidal signal of 50 µA p-p and 5.305 MHz frequency is applied at the input and the BP output in CM and TIM is observed as shown in Figure 15. It can be inferred from figures that the filter works correctly.

In the presented filter the quality factor can be set independent of the pole frequency of the filter. The tunability of the quality factor is verified by analysing BP response in CM and TIM for different values of bias current IBIAS1 as shown in Figures 16-17. It can be deduced from figures that the quality factor of the filter can be tuned independent of the frequency.

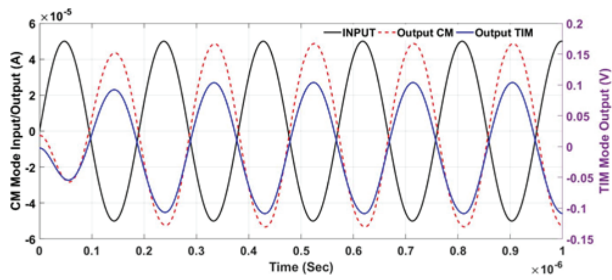

Figure 15: CM/TIM MISO configuration: Transient analysis results for BP filter configuration

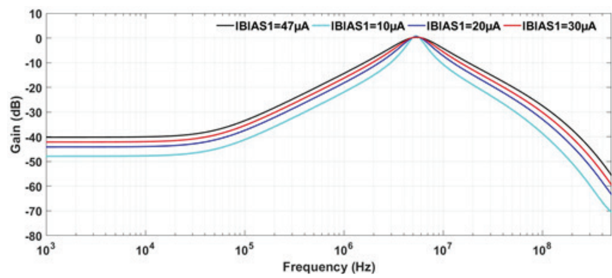

Figure 16: CM MISO configuration: Quality factor tuning for different values of OTA bias current

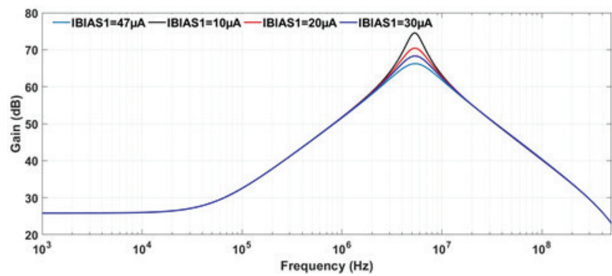

Figure 17: TIM MISO configuration: Quality factor tuning for different values of OTA bias current in BP filter

To study the effect of process spread on the performance of the designed filter Mont Carlo analysis is carried out for 200 runs. The Mont Carlo analysis results for VM BP response are given in Figures 18 and 19. The results for TIM AP configuration are given Figures 20 and 21.

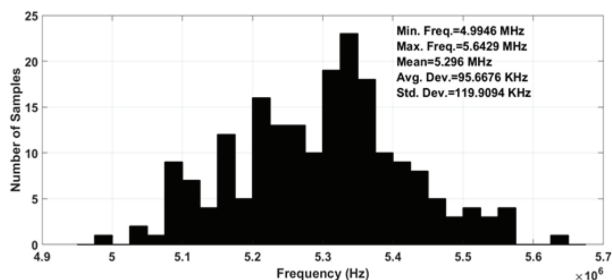

Figure 18: VM MISO configuration: The Monte Carlo analysis results for BP response

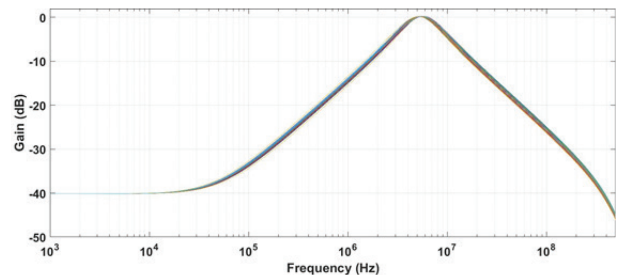

Figure 19: VM MISO configuration: The Monte Carlo analysis results for BP configuration

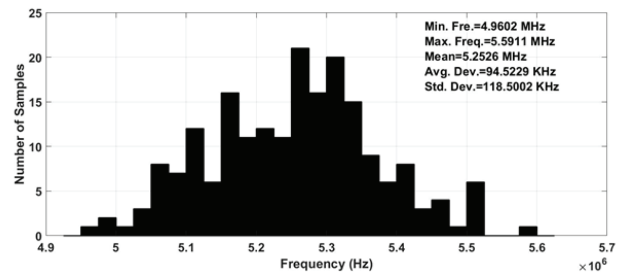

Figure 20: TIM MISO configuration: The Monte Carlo analysis results for AP response

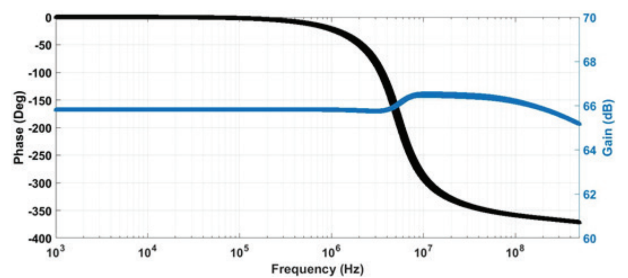

Figure 21: TIM MISO configuration: The Monte Carlo analysis results for AP configuration

The total harmonic distortion (THD) of the filter for LP and BP responses is plotted for different input signal amplitudes for VM as shown in Figure 22. The THD plot for CM-BP is presented in Figure 23. The THD remains within acceptable limits (≤5%) for appreciable input range.

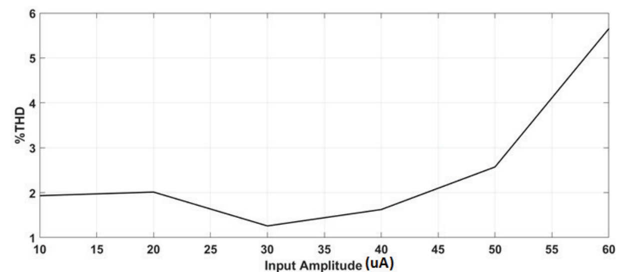

Figure 22: Total harmonic distortion of VM-BP and VM-LP

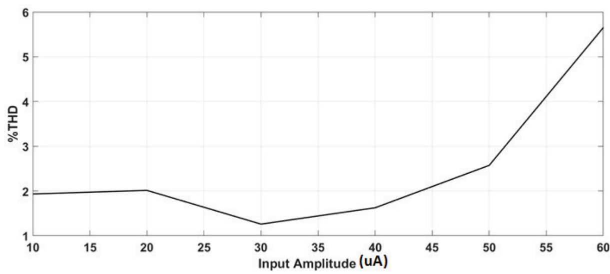

Figure 23: Total harmonic distortion of CM-BP

The pole frequency of the filter decreases due to rise in temperature Figure 24 because of the decrease in OTA transconductance. Two main contributing factors that influence the transconductance are the threshold voltage (V_t) and carrier mobility V_t. is approximated as a linear function of temperature [42,43] given by Equation 25. Where α_{Vt} denotes the threshold voltage temperature coefficient which varies from –1 mV/ °C to –4 mV/ °C and T_O is the reference temperature (300 K).

$$V_t(T) = V_t(T_O) + \alpha_{Vt}(T - T_O) \tag{25}$$

The dependence of carrier mobility on temperature is shown in [42-43].

$$\mu_N(T) = \mu_N(T_O)\left(\frac{T}{T_O}\right)^{\alpha_\mu} \tag{26}$$

where, α_μ is the mobility temperature exponent considered as a constant approximately equal to 1.5. The Equations (25) and (26), show that the threshold voltage (V_t) and mobility (μ_N) exhibit a negative temperature dependence.

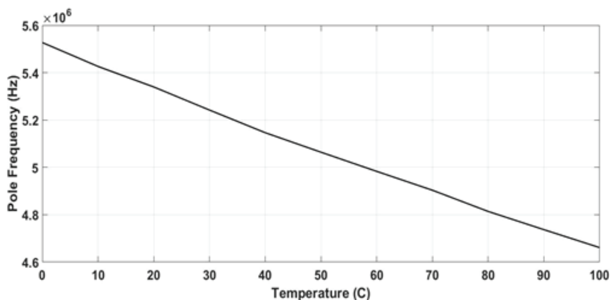

Figure 24: Variation of Filter Pole frequency with temperature

The input and output noise of the filter for VM-LP configuration is shown in Figure 25. The input referred noise magnitude for the VM-LP is found to be below 0.2E-06 $V / Hz^{1/2}$ till 10 MHz frequency. The maximum magnitude of output referred noise is 3.62E-08 $V / Hz^{1/2}$.

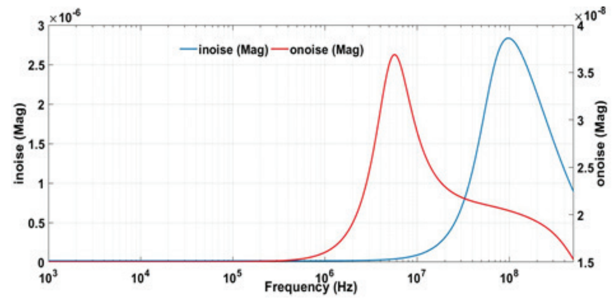

Figure 25: Input and output referred noise for VM-LP filter configuration

To further highlight the merits of the designed filter its performance is compared with some exemplary mixed mode filters as presented in Table 6. It can be observed that filters [46-47] cannot work in all four modes. The filters [24, 47] requires negative/double inputs for response realization. The filters structures [24,38,45] requires excessive numbers of ABBs for the design. It can be inferred from the table that the proposed filter has performance comparable with the existing designs. The power dissipation of the proposed filter can be reduced by designing the VD-DVCC for low supply operation.

6 Conclusion

This paper presents a new VD-DVCC based electronically tunable mixed-mode filter structure. The filter employs two VD-DVCCs, three grounded resistors and two grounded capacitors. Presented MISO filter has inbuilt tunability and can realize all five filter responses in all four modes of operation (VM, CM, TAM, and TIM). The detailed theoretical analysis, non-ideal gain analysis, and parasitic study are given. The VD-DVCC is designed in Cadence Virtuoso software and extensive simulations are carried out to examine and validate the proposed filter in all four mode of operation. The proposed filter has all the advantages mentioned in (i)-(iv). The filter is designed for a frequency of 5.305 MHz with ±1V supply. The power dissipation of the filter stands at 3.48 mW. The Monte Carlo analysis shows that the frequency deviation is within acceptable limits. Furthermore, the THD is within 5% for considerable voltage/current input signal range. The simulation results are found to be consistent with the theoretical predictions.

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A Low Distortion Audio Amplifier

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Abstract: The paper presents a design and assembly of a high-quality audio amplifier. The design is simple, and it can achieve extremely low Total Harmonic Distortion (THD) less than −100 dB for a bookshelf speaker with output power levels up to 10 W. The solution for a high-quality output are transistor pairs used in the input stage along with a simple topology that does not need matched transistor pairs for a power stage. Such input and output stages were closely analyzed at different bias currents. It was found out that there is an optimal power stage bias current of 20 mA for lowest distortion. The THD of the proposed topology was simulated with the LTSpice simulator and measured with the audio spectrum analyzer U8903B from Keysight and by a simple solution using a handheld recorder and an integrated Digital to Analog Converter (DAC). The Keysight was able to measure −104.5 dB THD_R, whereas simple solution did measure −92.8 dB.

Keywords: audio amplifier; feedback loop; transistor pair; THD

Avdio ojačevalnik z nizkim popačenjem

Izvleček: Članek predstavlja načrtovanje in izvedbo visokokvalitetnega avdio ojačevalnika. Načrt je preprost in lahko doseže zelo nizka harmonska popačenja (THD), pod −100 dB za namizne zvočnike z močmi do 10 W. Rešitev za doseganje nizkih popačenj so tranzistorski pari skupaj s preprosto topologijo, ki v izhodni stopnji ne zahteva tranzistorjev z enakimi lastnostmi. Vhodna in izhodna stopnja sta bili analizirani pri različnih delovnih tokovih. Ugotovljeno je bilo, da obstaja optimalni delovni tok 20 mA za doseganje najmanjšega popačenja. THD predlagane topologije je bil analiziran v programu LTSpice in pomerjen z avdio spektralnim analizatorjem Keysight U8903B ter z uporabo ročnega diktafona in integriranega digitalno-analognega pretvornika. Z uporabo Keysight inštrumenta se je izmerilo −104.5 dB THD_R, z enostavno rešitvijo pa −92.8 dB.

Ključne besede: avdio ojačevalnik; povratna zanka; tranzistorski par; THD

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1 Introduction

Audio amplifiers have three main parameters, that are important for listening experience. The first one is **power**. This parameter is important if the speakers will be used for music playback. In home speaker setup people would rarely need sound power in excess of 100 W, whereas in concert halls the power of amplifier systems needs to exceed 10 kW [1].

The second parameter is **Total Harmonic Distortion** (THD). It presents main signal quality characteristics combined in one parameter. The main quality parameters are linearity, slew rate, overshoot and stability.

And third, the **Signal to Noise Ratio** (SNR). This is another quality parameter that compares the audio signal power and the noise power. Because harmonic distortion is counted as a part of the noise in signal, it is included in SNR calculation.

In the paper it was decided to optimize distortion parameter, as it has the biggest impact on the quality and timbre of the amplificated signal. A signal with lower THD offers more music details and higher quality real-life listening experience.

At the beginning, research of audio amplifier market was done, which offers a lot of different audio systems. Many of them are implemented using standard Integrated Circuit (IC) amplifiers and are advertised to be superior without specifying any objective data with the following quotes: *The Way The Artists Truly In-*

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tended, *Purer sound*, *Shut out the noise*, *Wide frequency response for ultra-clear harmonics, etc.* [2]. On the other hand, there are many audiophile amplifiers that specify at least basic amplifier quality numbers (THD, Signal to Noise Ratio (SNR), Crosstalk…) but are significantly more expensive and sometimes they don't offer better performance as cheaper integrated circuit solutions.

A few commonly known audio amplifiers are compared in Table 1. The IC solutions have the worst performance, with the exception of LM3886 that is better than affordable medium class amplifiers from reputable companies Onkyo and Marantz. If a premium quality amplifier is chosen, such as Luxman or Classe Delta Mono, a price rises up to 10,000 € and more.

The development of the proposed high-quality amplifier was done under Master thesis [11], with budget accessible components.

2 Available circuit schematic performance analysis

In the proposed design, bipolar transistors are used for multiple reasons. They are popular in discrete analog circuits, and they have faster and better phase margin because of lower input capacitance compared to MOS transistors. The low input biasing voltage of bipolar transistors increases the swing of output signal to use more supply voltage range and higher current gains call for less components in design. A crucial component for high quality amplifier design with discrete components is the precise transistor pair that is available in the standalone package and can be used for a precise differential input stage formation, assembly of current mirrors, logarithmic amplifiers, etc., which is suitable for the proposed solution. Different topologies from the simplest to the more complex ones were analyzed to find the most suitable solution. These topologies consist of classic amplifier Classes [12]: A, B and AB. Additionally, one of high-quality amplifiers, designed by Linsley Hood in 1969 [13], was studied and analyzed. The design is presented in the next chapter, along with an operational amplifier LM2904 [14].

2.1 Linsley hood simple amplifier (Class AB)

Linsley Hood has published a very simple design with a good performance (THD less than –60 dB) in the magazine Wireless World [13]. Therefore, it is a great candidate for future analysis and to be used as building block for better and more complex architectures. A more thorough description of the simple output stage which uses 2 NPN transistors and was used in the proposed design is described in following chapter.

In Linsley's design, shown in Figure 1, a single PNP transistor (Q33) was used for an input stage and feedback from the output. An NPN transistor Q34 was used for the voltage amplification. The output stage was implemented with a double NPN stage (Q35 and Q36). As the output transistors are the same type (NPN), the matching that is necessary for a classical output stage with NPN and PNP is not needed, since the parameters are very similar between the same type of transistors.

Amplifier was analyzed at signal voltage nodes (N1, N2, N3, N4, Vin, Vout) at different output stage bias currents

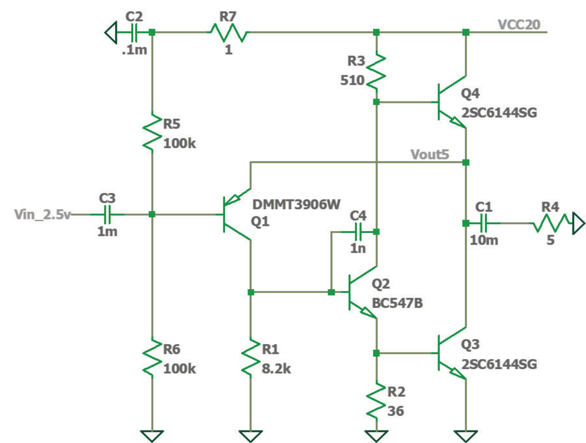

Figure 1: Linsley Hood amplifier simulation design

Table 1: Comparison of some audio amplifiers on the market

Amplifier	THD at 1 kHz [dB]	THD in FS [dB]	PRICE [€]	PRICE [Source]
TI LM4950 (IC) [3]	–55 (5 W, 8 Ω)	–45 (5 W, 8 Ω)	2.50	mouser.com
TI LM3886 (IC) [4]	–80 (30 W, 8 Ω)	–70 (30 W, 8 Ω)	7.66	mouser.com
TI TLV320AIC3268 (IC) [5]	–40 (1 W, 8 Ω)	/	9.49	mouser.com
Onkyo A9110 [6]	–66 (55 W, 8 Ω)	/	249.00	onkyo.com
Marantz PM6007 [7]	/	–62 (/)	640.00	marantz.com
Cambridge Audio Edge A [8]	–94 (100 W, 8 Ω)	–74 (100 W, 8 Ω)	5,999.00	md-sound.de
Luxman L-509x [9]	–83 (/, 8 Ω)	–64 (/, 8 Ω)	9,900.00	soundtemple.eu
Classe Delta Mono [10]	–106 (78 W, 8 Ω)	–96 (78 W, 8 Ω)	11,999.00	afmerate.com

(1 mA, 100 mA, 1.5 A) to see how they affect the performance. The bias is set by adjusting the resistor R40, which applies a bias current to the output transistor Q35.

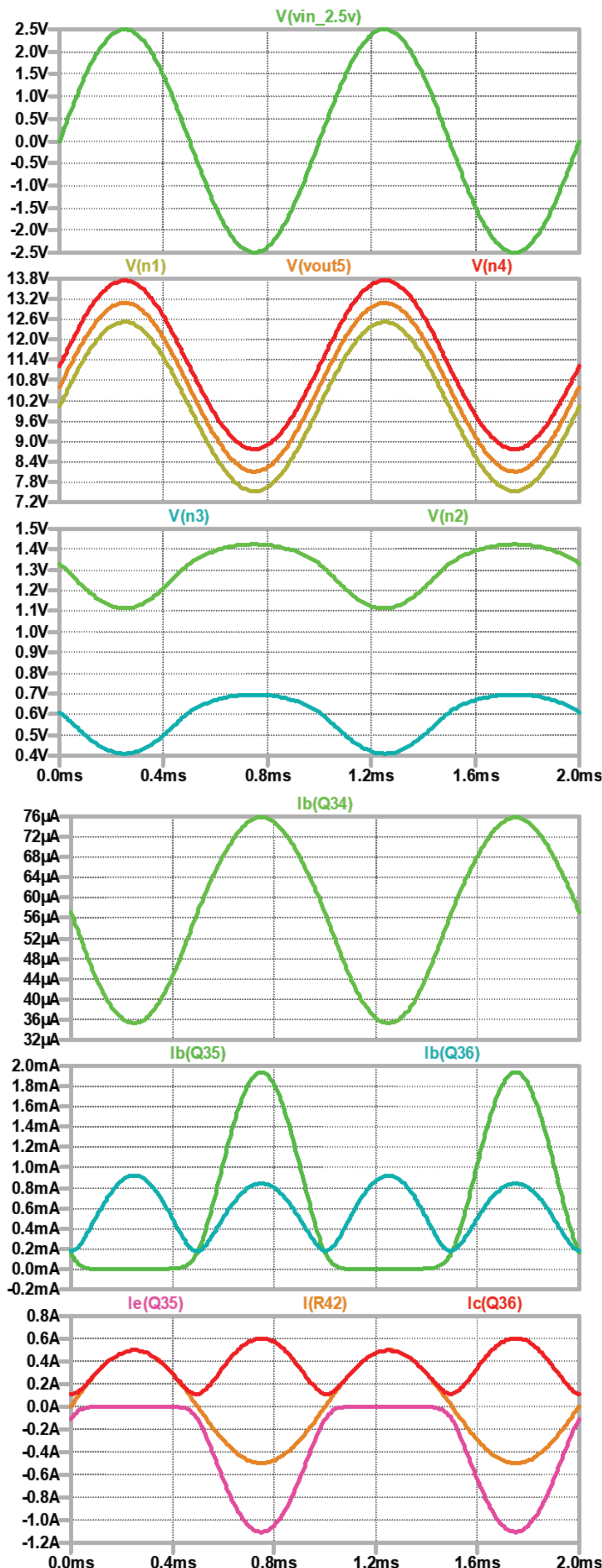

Figure 2: Voltage and current signals of a Class AB configuration (100 mA bias)

A 100 mA bias current was used for the Class AB output stage simulations which results are presented in Figure 2. In the circuit, there are 3 signals at nodes N1, Vout5 and N4 closely matching the input signal. They have offset defined by the transistor bias voltage which is approximately 0.7 V. The lowest voltage is at input of an amplifier (N1, base of transistor Q33) representing a non-inverting operational amplifier input. The output signal that drives speakers is marked with Vout5. This signal is also connected to an inverting input for a negative voltage feedback (emitter of transistor Q33). Another bias voltage higher is a signal driving base of the top output stage transistor (N4, Q36). The input transistor Q33 compensates the output signal (N2, collector Q33) to drive a voltage amplification transistor Q34, therefore signal N2 is not a perfect sine. The collector of Q34 (N4) then matches the sine and drives the upper output stage transistor Q36. The emitter of Q34 (N3) transfers the compensated signal to lower output stage transistor (Q35). The output signal matches input signal very closely with a distortion less than –60 dB, shown later in Table 3.

Looking at the currents of the output stage transistors Q35 and Q36, shown on bottom traces in Figure 2, explains the situation behind the compensated voltage signal. The compensation is needed because transistor Q35 is not always conducting, whereas Q36 needs to conduct current at negative and positive sine wave. The difference in output currents of Q35 and Q36 represents the current that drives the output speakers (R42). The base connections of output transistors are driven in anti-phase. The lower transistor is driven by node N3 and upper transistor by node N4.

It is important to note a time delay of voltage and current signals. If the delay becomes too big, the amplifier becomes unstable, therefore a proper phase compensation is needed. The main reason for delay is an influence of parasitic capacitances and inductances of PCB and components that shift voltage and current signals. The compensation is made with a capacitor and must be optimally chosen. If the compensation is weak, then feedback will respond too fast to the input signal change, and if the compensation is too strong, then feedback will not respond to the input signal fast enough.

A bias current of 1 mA was used for Class B output stage as seen in Figure 3. It can be noticed that some signals (N2, N3, N4, Ib(Q34)) have sharp response at zero crossing resulting in output distortion, shown in detail in Figure 5.

The sharp response is the result of a small output stage bias (1 mA). The input transistor therefore needs to

quickly compensate it and it generates a very sharp output current that flows into base of Q34. An overshoot in regulation is inevitable and results in current spikes when output stage transistors Q35 and Q36 start to conduct.

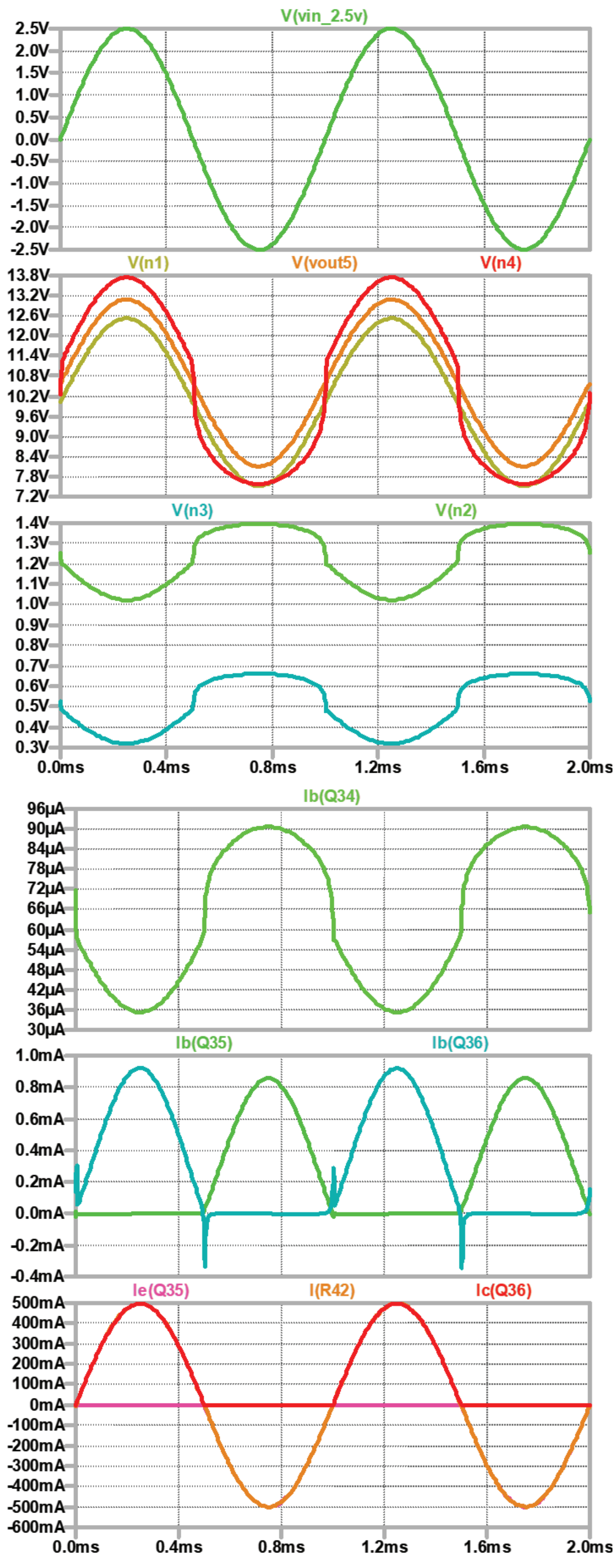

Figure 3: Voltage and current signals of a Class B configuration (1 mA bias)

Also, voltage signals of N1, N4 and Vout nodes are not correlated through the whole sine wave. The negative sine half of N4 node is distorted because feedback loop tries to correct the error in the output signal.

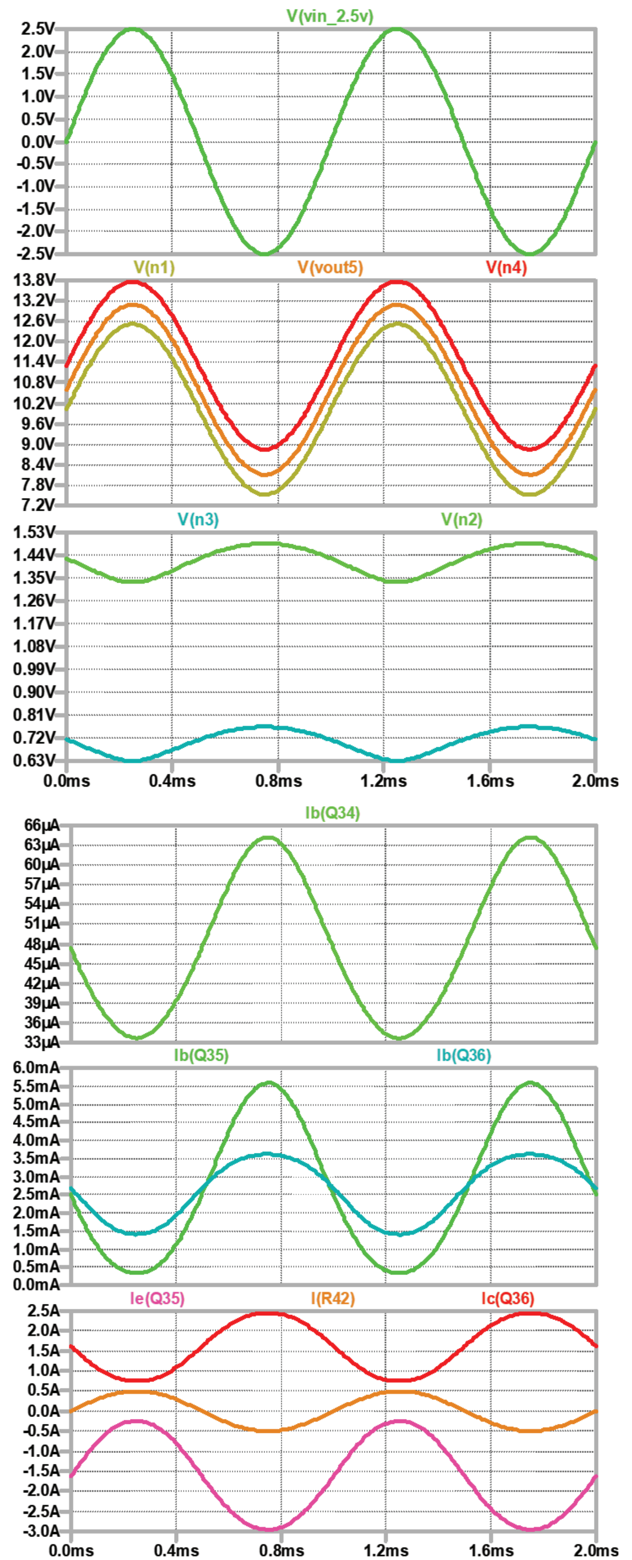

Figure 4: Voltage and current signals of a Class A configuration (1.5 A bias)

For the last simulation, a bias current of 1.5 A was used for a Class A output stage simulation, which results are shown in Figure 4. All signals are sinusoidal as transistors are always in the active region, therefore only a small correction is needed to compensate an exponential $U_{gate}(I_{emitter})$ transistor characteristic. The correction is done by negative feedback loop of the input transistor Q33. The output transistor currents graph shows why a Class A design is not appropriate as both transistors conduct 1.5 A in quiescence. When applying a signal that changes the load current from –500 mA to 500 mA, the current consumption of the output stage is in the from 500 mA to 3.0 A, showing the inefficiency of a Class A topology.

A THD of different amplifier classes were also simulated and are presented in the following chapters.

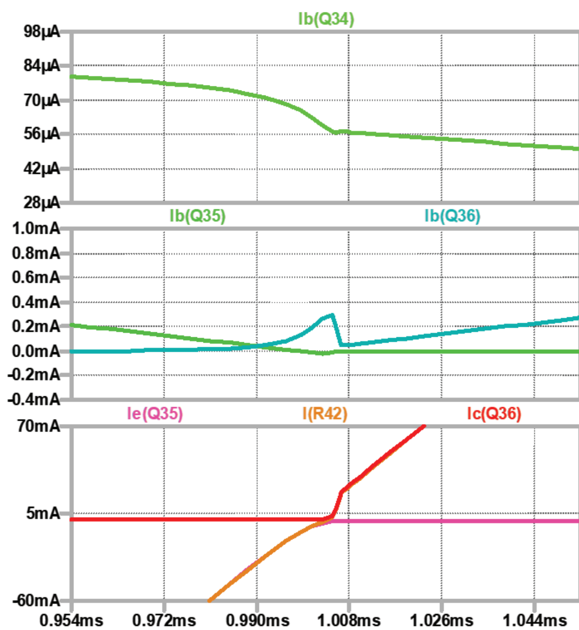

Figure 5: Sharp response at zero crossing with a Class B (1 mA bias)

2.2 Industrial grade off-the-shelf operational amplifier LM2904 (Class AB)

The documentation of integrated circuits is an excellent source of quality and reliable circuit designs, although schematics of complete designs are omitted nowadays. One of reliable integrated solution with included simplified schematic is LM2904 operational amplifier [14]. The design is simple and robust with predictable stability. The schematics of LM2904 is presented in Figure 6.

The input stage consists of the differential input stage using PNP transistors (Q1, Q2, Q3, Q4) biased with current mirrors. For additional amplification and lower input currents the input stage consists of transistors connected in a Darlington configuration.

The second stage (Q10, Q11) has relatively high input impedance, not to distort the signal, and amplifies current from the input stage. For better output utilization, 2 transistors, NPN and PNP, are used in common collector configuration therefore cancelling out the 0.7 V bias voltage of this stage.

The signal from the second stage is feed to the voltage amplification stage (Q12) with a 100 µA bias current.

For the final stage, NPN and PNP transistors (Q6, Q13) are used. For higher current capability the upper output transistor (Q6) is additionally amplified, using transistor Q5 in Darlington configuration. A current protection is done with a shunt resistor (R_{SC}), connected to a gate of transistor (Q7).

The main part of the LM2904 circuit used in the proposed design, is the input differential pair. Performed analysis and comparison of input stages of Linsley's amplifier and LM2904 are presented in the next chapter. The Linsley's input stage was analyzed in Linsley's amplifier circuit and simplified LM2904 input stage without Darlington connection for additional amplification was analyzed in proposed design, show in Figure 7.

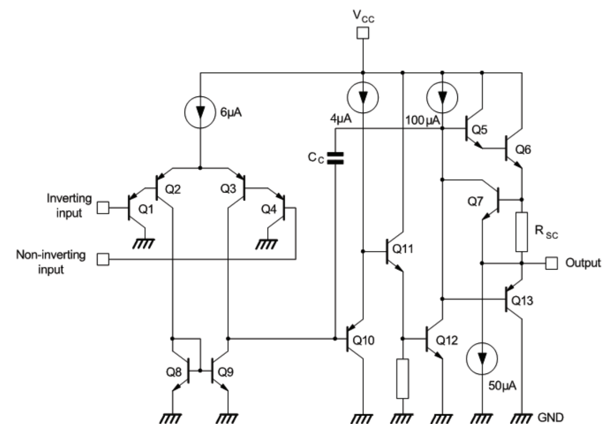

Figure 6: A simplified schematics of LM2904 operational amplifier

2.3 The proposed design (Class AB)

The base of the proposed design presents the LM2904 transistor differential pair input stage, together with a double NPN output stage from the Linsley Hood's amplifier. Between input and output stages, additional components were used to shorten signal path, lower distortion and speed up the feedback path. The schematic of the proposed design is shown in Figure 7.

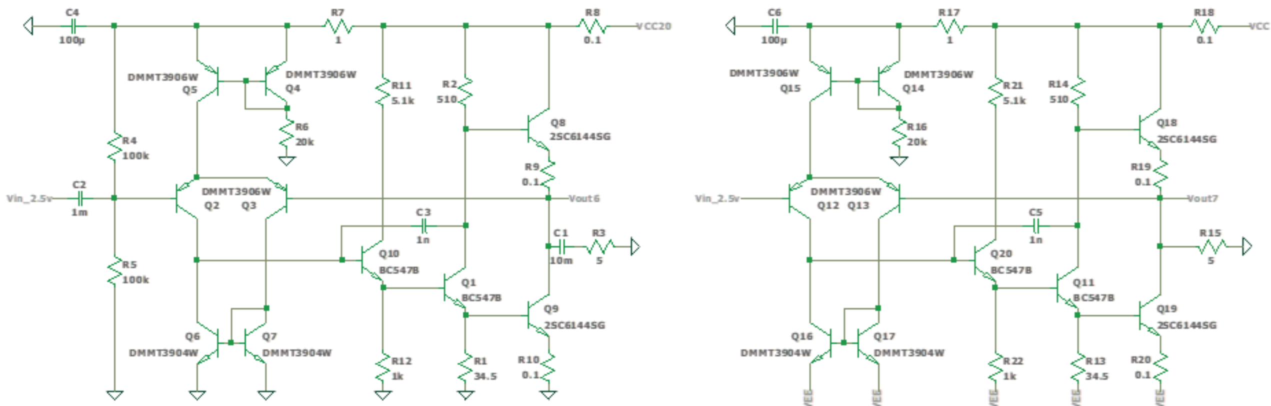

Figure 7: Simulation schematics of proposed amplifier (single supply LEFT, dual supply RIGHT)

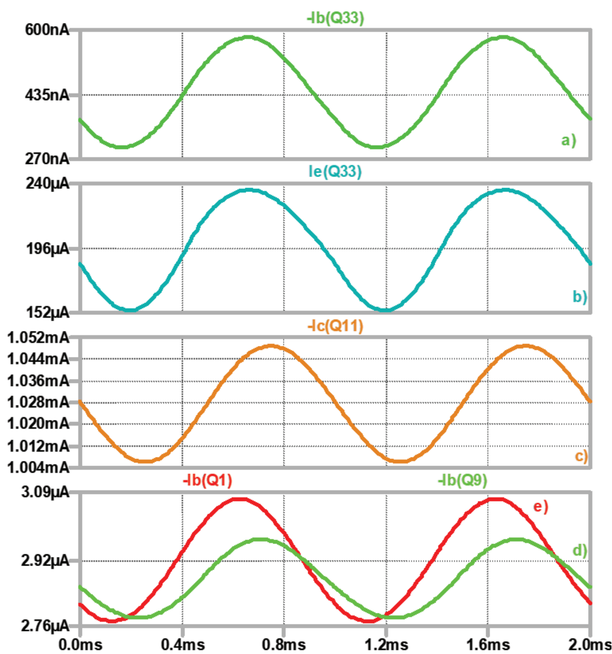

Figure 8: Single vs differential input stage: a) input current into base of single stage, b) current into emitter of single stage, c) current of differential stage, d) inverting differential input stage base current, e) non-inverting differential input stage base current

A signal propagation comparison was made between Linsley Hood single transistor input stage (IS) and differential input stage in the proposed design. The amplifiers' simulation schematics are shown in Figure 1 and Figure 7. The input stage currents (Figure 8) are consisting of DC bias and AC signal.

Interestingly, the base input (Figure 8a) and emitter (Figure 8b) bias currents of single input stage were lower than the differential stage (Figure 8c, e) by 2.5 μA and 0.8 mA. Also, the phase shift of signals is smaller in single IS compared to the differential IS. Despite lower values, the THD was higher in a single input stage of Linsley Hood.

To clarify the issue, Fast Fourier Transform (FFT) analysis was performed at different input stage bias currents. A signal of 1 kHz at 2.5 V amplitude was used for excitation. The bias current did not affect Linsley Hood's amplifier input stage and the second harmonic caused approximate –70 dB distortion, whereas the proposed design with differential input stage, is affected by the input stage bias current – the higher it is, the lower is the distortion. In the proposed design, when the bias current is over 1 mA, the 2nd harmonic decreases, but the 3rd harmonic increases. At 2 mA bias current, the 3rd harmonic is at –94.5 dB and the second at –99.2 dB, showing that this is an optimal relation between supplied bias current and distortion. The bias current comparison results are shown in Table 2.

3 THD simulation of proposed design

Simulations of THD were performed in LTSpice, which is a simple and powerful Spice based program with Graphical User Interface (GUI). All previously mentioned topologies were analyzed to get a good understanding of the circuit operation. The THD was measured by 1 kHz, 5 V sine wave excitation on input. The FFT analysis result of proposed design (topology 11 in Table 3) is shown in Figure 9.

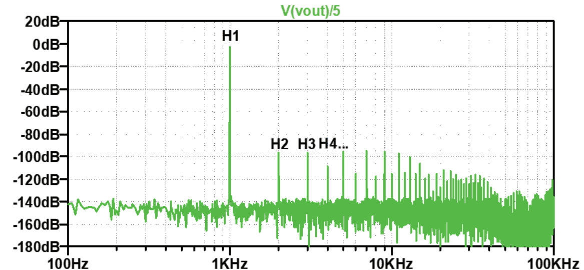

Figure 9: FFT analysis results of proposed design

Table 2: 2nd harmonic comparison between Linsley Hood and the proposed amplifier input stage

	Fundamental to 2. harmonic ratio [dB] (IS bias resistor [kΩ])					
IS bias current [uA]	100	200	500	1000	2000	5000
Linsley	–67.5 (30)	–70.2 (9)	–70.8 (3)	–71.0 (1.4)	–70.7 (0.66)	–70.2 (0.26)
Proposed	–75.7 (200)	–81.8 (100)	–89.4 (41)	–95.0 (20)	–99.2 (10)	–102.2 (4)

Table 3: Harmonic amplitudes at 5 Ω load and 5 V amplitude of in/out signal

Topology		Harmonic [dB]				Bias current of output stage [A]
		2.	3.	4.	5.	
1	MOS follower 6k/10k	–43.1	–48.5	–53.1	–57.6	2.0
2	BJT follower 2.8k	–38.7	–40.6	–42.7	–44.6	2.0
3	BJT follower 2k	–56.0	–61.2	–70.9	–76.1	2.3
4	BJT follower 430	–77.5	–70.6	–90.7	–105.5	10.0, 1 ΩLOAD
5	BJT Class B	–43.4	–24.0	–44.9	–29.2	0.0
6	BJT Class AB 5mA, 2k	–49.9	–65.0	–76.8	–70.2	100 m
7	Linsley Hood AB	–66.1	–79.5	–89.2	–93.8	100 m
8	Linsley Hood B	–67.8	–63.7	–66.1	–63.0	1 m
9	Linsley Hood A	–69.4	–72.4	–79.2	–94.1	2.0
10	Proposed with only + supply	–92.9	–94.3	–106.9	–92.6	100 m
11	Proposed with ± supply	–94.1	–94.2	–106.4	–92.7	100 m

The higher harmonics from the FFT analysis plot were compared with the fundamental tone H1. In Table 3, results for individual harmonic distortion and bias currents are presented. Cells with the worst harmonics are shaded. The performance of Linsley Hood's amplifier and proposed design is shown alongside with basic topologies consisting of single or dual transistors (topologies 1 – 6). The basic topologies are included to show a distortion which is caused by transistor's nonlinear characteristic and an influence of feedback to linearization.

With a simple voltage follower topology (topologies 1 - 4), the amplification quality is solely dependent of a single transistor characteristic. The main transfer characteristic is $I_{OUT}(U_{IN})$. The transistor models used are Infineon BSB012N03LX3 for MOSFET and Onsemi 2SC6144SG for BJT. At 2 A bias current, a BJT transistor had worse distortion as MOSFET by 4.4 dB (–43.1, –38.7 dB). By slight bias current raise to 2.3 A, the BJT distortion was greatly improved to –56.0 dB. In simulation, the bias was increased to unrealistic value 10 A, where a single BJT transistor has distortion –70.6 dB and it could compete with quality amplifiers.

A Class B topology, without feedback (topology 5), has the worst distortion. The odd harmonics contribute most to the distortion, with third being the worst at –24.0 dB. It was found that the THD improves by increasing input signal levels. This is because transistors stay less time in a non-conducting region, therefore the signal is less distorted.

By adding a small bias current through output transistors, the distortion can be lowered (topology 6). Class AB with 100 mA bias, has –49.9 dB distortion at 5 mA voltage amplification stage bias current.

The THD also improves when simple feedback with one transistor is used which is utilized in the Linsley Hood design (topologies 7-9). The distortion from an ordinary AB stage is decreased by 16.2 dB to –66.1 dB. A distortion of Class B amplifier can also be decreased with feedback. A Linsley Hood amplifier in Class B therefore performs 39.0 dB better than a simple Class B amplifier (–24.0, –63.0 dB).

The proposed design achieved the lowest distortion around –92.6 dB, if supplied with a single (positive) or dual (positive and negative) supply voltages (topologies 10, 11). Using dual supply voltages is preferred to omit small signal and power coupling capacitors which realize middle voltage level. The usage of coupling capacitors is not desired because real capacitors have many parasitic elements, occupy space on a PCB and add additional phase delay which affects signal distortion.

4 Measurements

The schematics and PCB of the circuit were drawn in Altium Designer. All appropriate power supplies, isolation, D/A converter and pre-amplification stage were also included on the PCB, as the proposed design (Figure 7 RIGHT) is used in a complete audio amplifier and marked as R AMPLIFIER and L AMPLIFIER in a block schematic of Figure 10.

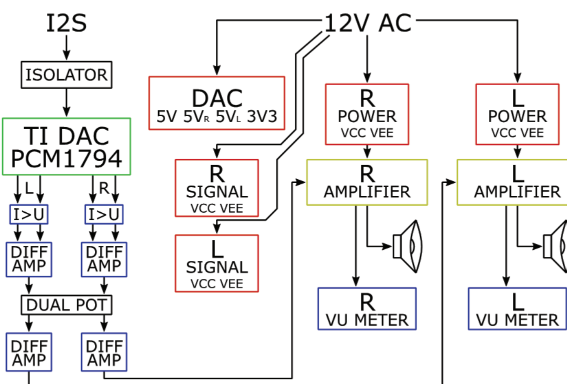

Figure 10: Block schematics of complete circuit with including proposed amplifier

The connection between pre-amplification stage and proposed amplifier was done differentially to limit the noise coupling from an environment. The output signal and ground reference signal from a block DIFF AMP were connected through a twisted pair cable to an input of the amplifier and ground. The connection is summarized in Figure 11. On a PCB circuit, a star connection for ground signals was used as close to the load ground connection as possible shown on Figure 12. Star connection lowers the noise coupling and ensures proper signal integrity.

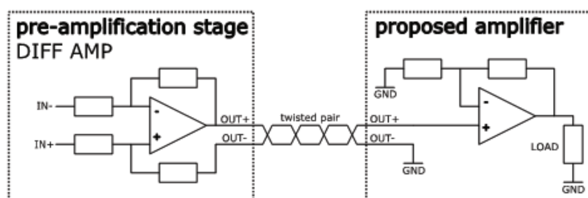

Figure 11: Connection between pre-amplifier and proposed amplifier

The distortion of a proposed design was measured using an industry standard Audio Spectrum Analyzer U8903B from Keysight [15]. A measurement of THD_R and SINAD (Signal to Noise and Distortion) were made at multiple frequencies and amplitudes. A power stage bias was also measured.

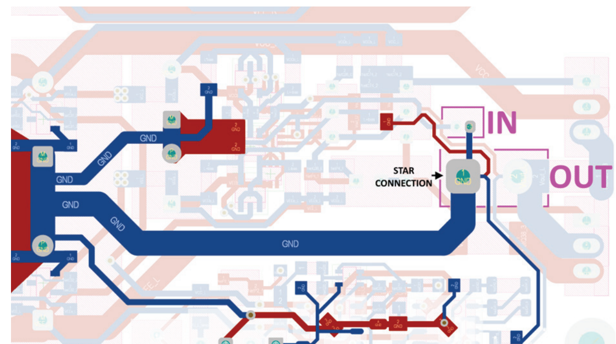

Figure 12: Star connection for ground signal nodes at load output connector of proposed amplifier

Initially, power was supplied with a transformer from an AC grid and rectified on the circuit, but this resulted in a poor SINAD characteristic in the range of 65 dB. To improve this, a 12 V battery supply was used and the SINAD improved to 75 dB.

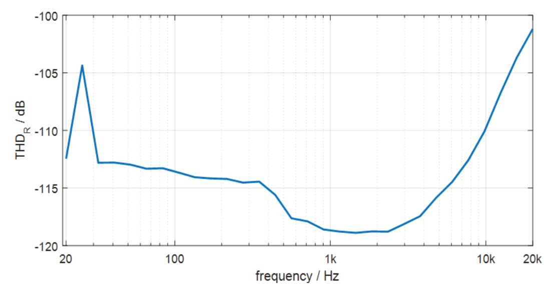

Figure 13: Keysight U8903B input-output characteristics

In Figure 13, an input-output characteristic of an audio spectrum analyzer was measured to set a reference value. The instrument's THD_R is around –100 dB to –120 dB with 50 Hz line noise.

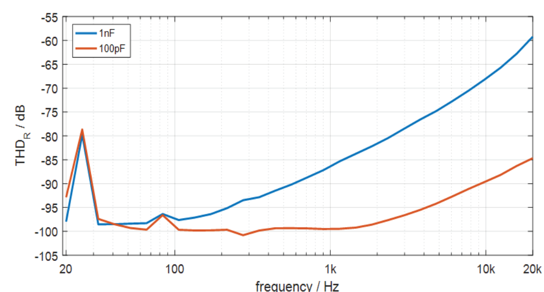

Figure 14: Influence of feedback capacitance

The proposed amplifier was measured using two different compensations in the feedback – 100 pF and 1 nF. The same compensation was used on power stage transistors due to their high bandwidth. It was found that decreasing compensation greatly improves THD_R at higher frequencies by 25 dB. In the region below

1 kHz, the THD_R is even better than simulated where it surpasses –100 dB. The results of measurements are presented in Figure 14.

A distortion comparison was made also with Linsley Hood's design and quality integrated headphone amplifier TI TPA6120A2 and results are shown in Figure 15. The Linsley's design did not perform as good as the proposed design, reaching THD_R around –50 dB. At higher frequencies distortion worsens because of low-cost capacitors used for DC component decoupling. The integrated headphone amplifier also did not perform as good as the proposed design with THD_R around –80 dB to –90 dB, except at higher frequencies where distortion improved under –100 dB. The circuit board and other used elements introduced a frequency pole nearby 10 kHz which resulted in a better THD_R.

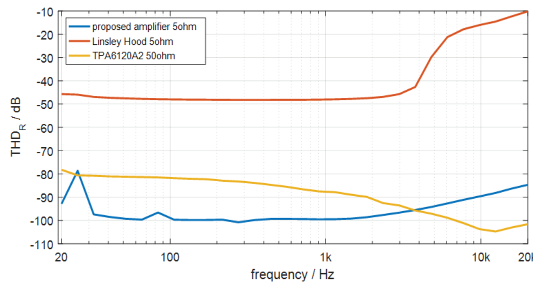

Figure 15: Frequency characteristics at 2 V_{RMS} input

A bias current in the output stage has also impact on the THD_R. A constant sine wave was used as the input and the bias current through output transistors was changed using potentiometer. In Table 4, results of distortion measurements are presented, where it can be found that the highest bias current does not necessarily mean the lowest THD_R. Instead, when bias currents are in the range from 20 to 40 mA, a signal with lowest distortion –108.4 dB was measured.

Biasing is influenced by the temperature of the transistors. The higher temperature will shift the $I_C(U_{BE})$ characteristic up, meaning that the same voltage bias will result in a higher current flow through a transistor. Temperature effect on bias was therefore canceled out by adjusting the bias to precise value before measuring the THD. Despite this, a difference of THD between measurements could be observed at the same bias current. This is due to a different temperature of output transistors between measurements. The current bias was adjusted in a sequence listed in Table 4 – from 4 mA to 320 mA to 5 mA. Consequently, the temperature of transistors before 320 mA measurement was lower than after the 320 mA measurement at the same current bias.

Amplifier was also characterized with and without a load. Results are shown in Figure 16. The THD_R difference is 5 dB. The reason is in higher currents needed for load driving; therefore a higher influence of transistor nonlinearities is present.

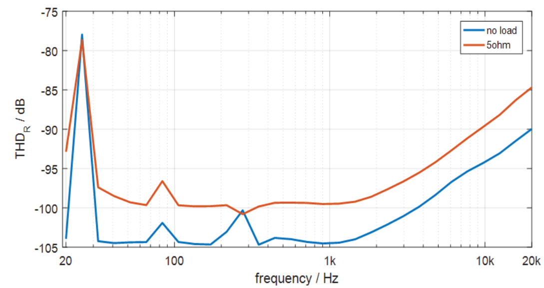

Figure 16: Frequency response of proposed amplifier at different loads

For measurement comparison, a simple and low-cost method for THD_R measurement was used as shown in Figure 17. An integrated high quality DA converter PCM1794 with best case scenario –108 dB THD_R was used as a signal generator. The DA needs a simple pre-amplifying stage that was made using TI operational amplifiers OPA1678 [16] with THD_R of –120 dB. The THD_R at 1 kHz was measured with a handheld voice recorder Tascam DR-22WL which uses a Cirrus Logic CS42L52 [17] codec with –88 dB THD_R. A final THD_R value was obtained from a recorded WAV file with FFT analysis performed within MATLAB program. In the measuring setup, the recorder has the worst distortion so a distortion of –88 dB was expected.

Despite the previous fact, total distortion of –92.8 dB was measured meaning some deviations from the circuit documentation exists. The control measurement was done with the Keysight equipment and a THD_R of –104.5 dB was obtained. Results show that the simple method is not suitable for measuring the distortion of

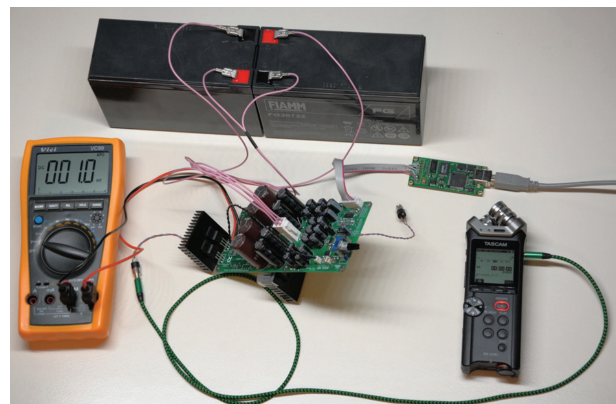

Figure 17: A simple and low-cost method for measuring THD_R

Table 4: Distortion at 440 Hz, 2 V_{RMS} input signal

Bias current with signal [mA]	4	10	20	40	80	160	320	160	80	40	20	10	5
THD [dB]	-98.3	-102.0	-108.0	-107.3	-105.6	-103.7	-102.5	-103.8	-106.4	-107.7	-108.4	-105.0	-100.2

proposed amplifier, as a distortion of consumer recorders using off-the-shelf codecs are decades worse than a high-fidelity audio equipment. The measurement results of this comparison are shown in Figure 18.

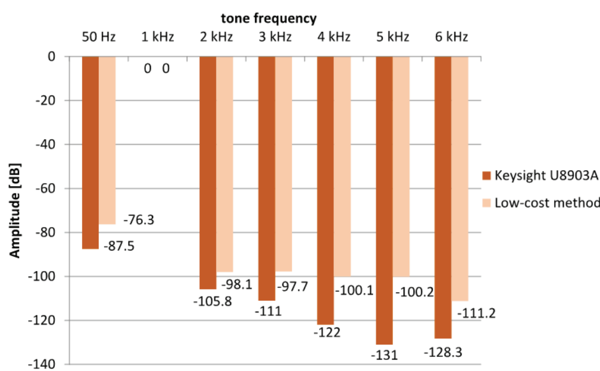

Figure 18: Comparison of harmonics and 50 Hz distortion on proposed amplifier output

5 Conclusions

The paper presents that a high-quality amplifier can be realized using simple schematics and affordable components. The proposed amplifier exceeded –100 dB THD_R. Further feedback transfer function characterization would allow additional compensation optimization, which would result in distortion improvement.

Although the analog amplifier distortion can be additionally improved, firstly the input signal must be improved to higher quality. A noise improvement would also be needed as the noise level is much higher (around 75 dB) than distortion.

The problem is also how to obtain recorded music with –100 dB distortion. All the recording equipment must have low noise and distortion. The recordings must not be poorly compressed and must have lossless quality. Also, the room in which the music is played must have low noise floor to fully enjoy the quality.

All the above is hard to achieve, and yet the total noise and distortion using the proposed design is better than an average consumer amplifier and contributes to an excellent listening experience with a simple design.

6 Acknowledgments

Authors would like to thank a Slovenian distributor of instrumentational devices Amiteh for lending a Keysight U8903B audio spectrum analyzer and therefore enabling comparison between a real-world and simulation results.

7 Conflict of interest

The authors confirm there are no conflicts of interests in connection to the work presented.

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Analysis of effects of dangling-bond defects in doped a-Si:H layers in heterojunction silicon solar cells with different electron affinities of ITO contacts

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Abstract: The effects of dangling-bond defects in doped hydrogenated amorphous-silicon layers (p-a-Si:H and n-a-Si:H) in heterojunction silicon (SHJ) solar cells are studied in relation to applied Indium-Tin-Oxide (ITO) contacts with different electron affinities. A state-of-the-art numerical model of the SHJ solar cell was employed, including ITO contacts as full, volumetric semiconductor layers, applying the trap-assisted, band-to-band and direct tunnelling mechanisms at heterointerfaces in the device. The levels of dangling bond defect concentrations were varied in both p-a-Si:H and n-a-Si:H layers and ITOs with two different electron affinities were considered at both sides of the device. We show that the effects of the defects on the short-circuit current density, open-circuit voltage, fill factor and conversion efficiency of the device become more pronounced if ITOs with non-optimal electron affinities are used. Possibility to reach higher doping levels of the doped a-Si:H layers would mitigate the effects of its dangling bond states, which becomes more important if ITO electron affinity is not optimized to the doped a-Si:H layers. We demonstrate that the reduced efficiency due to the increase in dangling-bond density originates from the decrease of the fill-factor and open-circuit voltage, whereas the short-circuit current density has a small effect on efficiency for the chosen variation span. The reduction of the fill-factor is further explained by a drop in maximum-power-point voltage, which is more pronounced if optimization of ITO electron affinity is not taken into account.

Keywords: Silicon heterojunction solar cell; Opto-electrical simulation; Defect-states, Electron affinities

Numerična analiza učinkov defektov bingljajočih vezi v dopiranih plasteh iz a-Si:H v heterospojnih silicijevih sončnih celicah s kontakti ITO z različnimi elektronskimi afinitetami

Izvleček: Raziskali smo vpliv defektov bingljajočih vezi v dopiranih slojih hidrogeniziranega amorfnega silicija (p-a-Si:H in n-a-Si:H) v kombinaciji s kontakti iz indij-kositrovega oksida (ITO) pri heterospojnih silicijevih sončnih celicah (SHJ). Za raziskovanje notranjih in zunanjih lastnosti celice smo uporabili optoelektrične simulacije. Uporabljeni sodobni numerični model SHJ sončne celice je vseboval kontakte ITO, ki so bili modelirani kot dejanski polprevodniški sloji ter upošteval tuneliranje s pomočjo pasti, tuneliranje med energijskimi pasovi in tuneliranje znotraj energijskega pasu na heterospojih sončne celice. Spreminjali smo koncentracijo defektov bingljajočih vezi v p-a-Si:H in n-a-Si:H slojih pri dveh različnih elektronskih afinitetah kontaktov ITO na obeh straneh celice. Pokazali smo, da je vpliv defektov na izkoristek, polnilni faktor, napetost odprtih sponk in kratkostični tok bolj izražen, kadar elektronska afiniteta kontaktov ITO ni bila prilagojena dopiranim a-Si:H slojem. Ugotovili smo, da je zmanjšana učinkovitost zaradi povečanja gostote defektov bingljajočih vezi posledica zmanjšanja polnilnega faktorja in napetosti odprtih sponk, medtem ko kratkostični tok ni močno vplival na izkoristek znotraj izbranega območja variacije. Zmanjašanje polnilnega faktorja smo obrazložili preko upadanja napetosti pri maksimalni moči, ki se zmanjša še bolj občutno, kadar kontakti ITO niso optimizirani.

Ključne besede: heterospojne silicijeve sončne celice; optoelektrične simulacije; defektna stanja, elektronske afinitete

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1 Introduction

The ever-growing demand for clean and affordable electrical energy opened up a substantial market for photovoltaics and other renewable energy technologies. In Photovoltaics the biggest market share (~95 %) belongs to the crystalline-silicon (c-Si) based solar-cell technology [1]. Of these, silicon heterojunction (SHJ) solar cells are gaining attraction with the potential to achieve high conversion efficiency, low temperature coefficients and competitive production costs. The current world-record efficiency of a c-Si-based terrestrial non-concentrating large area solar cell is 26.7 % [2] and is achieved by the heterojunction structure in combination with interdigitated back contacting [3]. The SHJ cells utilize the benefits of both, conventional (c-Si wafer-based) and thin-film (hydrogenated amorphous silicon - a-Si:H) technologies. A thorough understanding of the governing physical mechanisms in state-of-the-art structures of solar cells, such as SHJ, is crucial when designing cells at the limit of what is theoretically possible (~30 % for single junction devices) [4]. Numerical modelling and simulations are an indispensable part of the R&D cycle as they unveil, often immeasurable, internal quantities of the solar cell, which determine its external characteristics. The study presented in this paper is based on detailed opto-electrical modelling and simulations of SHJ solar cells. In particular, we analyse the effects of dangling bond defects in doped a-Si:H layers in relation to indium tin oxide (ITO) transparent conductive oxide (TCO) contacts with different electron affinities χ. Various numerical models emerged from the research of SHJ cells that vary in complexity and accuracy [5]–[14]. In this contribution we used the Sentaurus TCAD software suite [15] to numerically model and study the device's internal and external performance related to the mentioned effects for applied ITO electrodes with optimized and non-optimal electron affinities. While our previous work [16] was focused on combined effects of defect states at i-a-Si:H/c-Si interfaces and in p-doped a-Si:H (p-a-Si:H) and n-doped (n-a-Si:H) thin layers considering one pre-selected electron affinity of ITO layers, in this work we extend the study to structures where ITO contacts have different electron affinities (optimized and non-optimal). Solar cells with ITO/doped a-Si:H selective contacts have already been studied numerically [11], [17]–[21] however, the authors either used a Schottky barrier as a Dirichlet boundary condition to model the ITO contacts or focused on other parameters of ITO and a-Si:H. Studies have not been performed in relation to specific defect types in a-Si:H doped layers in combination with different work functions or electron affinities of ITO contacts. In our research we use a fully volumetric semiconductor model of ITO, including the accompanying trap-assisted (TAT), band-to-band (BBT) and direct tunnelling (DT) processes in simulations. We focus our analysis primarily on the maximum-power-point (MPP) operation of the solar cell, as this is the common operating condition of solar cells in a real scenario and is often not taken in consideration sufficiently in such modelling studies. Quantitative results of the presented analysis reveal the impact of defects, in particular dangling-bond states in doped a-Si:H layers (especially in the p-a-Si:H layer) when using ITO contacts with different electron affinities. It is necessary to study also the synergy between the defect states and the ITO electron affinity as they both have a big influence on the electronic state of the device (formation of the electric field needed for charge separation), which determines the efficiency of the cell. Additionally, the study aims to improve the physical understanding of the related effects. Simulation results are presented for the a-Si:H based selective contacts, however, the results can be usefully considered also in the design of the SHJ solar cells including novel materials for selective contacts. e.g. metal-oxides and fluorides [8], [22]–[27].

2 Device structure and model

In our analysis we considered the following SHJ solar cell structure (Fig. 1): ITO front cathode (70 nm), p-doped a-Si:H layer (p-a-Si:H, 10 nm), intrinsic a-Si:H passivation layer at p-side (i-a-Si:H, 5 nm), n-doped c-Si bulk absorber (n-c-Si, 150 µm) with interface regions at both i-a-Si:H/n-c-Si interfaces (2 nm), intrinsic a-Si:H passivation layer at n-side (i-a-Si:H, 5 nm), n-doped a-

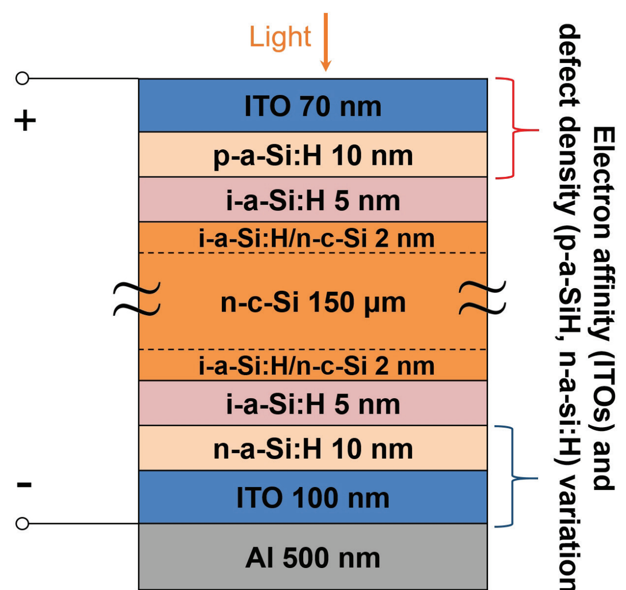

Figure 1: Structure of the simulated solar cell. Optical simulations were done on the entire device whereas electrical simulations used ideal ohmic boundary condition in lieu of the Aluminum layers.

Si:H layer (n-a-Si:H, 10 nm), rear anode ITO (100 nm)/ Al contact layer (500 nm). The ITO/p-a-Si:H and ITO/n-a-Si:H layer stacks enable selective collection of generated holes and electrons at the cathode and anode, respectively. The input parameters of layers and interface regions are described later.

The optical generation profile of the illuminated cell with standard AM1.5g spectrum was simulated with the Sun*Shine* simulator [28]. The coherent and incoherent nature of light was accounted for in the thick and thin layers, respectively, together with the light scattering and antireflection effects at the front and rear side of the device. Light enters into the device through the p-a-Si:H side (front) of the device in our basic case, however, selected simulation tests have been done also for the n-side illumination. In the simulated reference structure, the short-circuit current density (*J*sc), calculated directly from optical generations in the n-c-Si layer under AM1.5g solar spectrum, amounted to 39.06 mA/cm^2. The Optical generation profile was kept unchanged during sweeps of the investigated electrical parameters (peak dangling bond defect density and doping of p-a-Si:H and n-a-Si:H layers, ITO electron affinity) to selectively indicate their effect on the solar cell performance. It should be noted that in this study we did not focus on the optical performance of the device. We chose the presented planar architecture instead of an interdigitated back-contact (IBC) solution to minimize external influences, such as lateral currents, normally present in IBC devices, to more clearly show the effects of defect density and ITO electron affinity on SHJ solar cell performance. Detailed optical simulations can be found elsewhere [10, 29].

Detailed electrical simulations of the device were performed with the Sentaurus TCAD software suite [15], also used and validated for simulation of SHJ solar cell structures in previous publications [9], [10]. The material interfaces were generally considered as geometrically flat in electrical simulations. The simulation domain in electrical simulations of the device was two-dimensional, however, the problem at hand is one-dimensional. Therefore, the results of internal quantities were transformed in a one-dimensional function of the structure depth where applied. The temperature was kept at 300 K in all simulations. In the numerical description of the cell, the Drift-Diffusion model was employed to solve the Poisson equation coupled with the continuity equations for charge concentration inside the investigated solar cell structure. We used both Gummel and Newton solving schemes interchangeably to either ensure, or expedite the convergence of the simulations. The Fermi-Dirac statistics was used to accurately calculate free-charge density also in the regions of high effective dopant concentrations. Band-gap narrowing and mobility dependence on dopant density was not included in the analysis, which shortened the simulation time with negligible effect on results as tested before for selected cases. The recombination of charge in the n-c-Si bulk was based on the parametrization first implemented by Richter et. al. [30], which includes both Auger and Radiative recombination mechanisms and accurately calculates their impact on minority carrier life-times in a broad range of dopant concentrations and injection levels. The Shockley-Read-Hall (SRH) recombination in the n-c-Si bulk was modelled via life-time of minority carriers (10 ms). In a-Si:H layers the defect states were represented by donor-like (don) and acceptor-like (acc) tail and dangling-bond (db) states. The amphoteric nature of dangling bonds was taken into account by two Gaussian functions, describing the so called +/0 and 0/- charged states [31]. The donor-like tail and the +/0 dangling-bond states are positively charged when vacant and neutral when occupied by an electron. The acceptor-like tail and so-called 0/- dangling-bond states are neutral when vacant and negatively charged when occupied by an electron. The defect-density distribution of tail-states (N_{tail}) and dangling-bond states (N_{db}) along the band-gap of the p-a-Si:H layer for the reference cell is presented in Fig. 2.

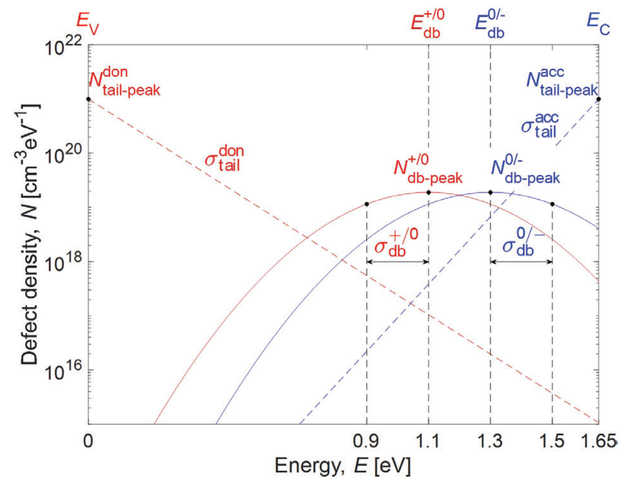

Figure 2: Representation of defect-state distribution in a-Si:H layers of the reference cell (selected case is shown for the p-a-Si:H layer, see corresponding values of the parameters for all a-Si:H based layers in Table I). The red dashed and full lines present the donor-like tail and +/0 dangling-bond states. The blue dashed and full lines correspond to acceptor-like tail and 0/- dangling-bond states.

However, all used defect-state parameters for the p-a-Si:H, n-a-Si:H, i-a-Si:H layers, and the i-a-Si:H/n-c-Si interface regions in the starting, reference cell are available in Table I. Regarding the defect-state variation, in this study we focused only on the values of the Gauss-

ian peak concentrations ($N^{+/0}_{db\text{-}peak}$, $N^{0/-}_{db\text{-}peak}$) and not the tail states, since it was indicated that they have a noticeable effect on device performance [16] including indium-tin-oxide (ITO). The defective n-c-Si surfaces (in simulations 2 nm regions) passivated by i-a-Si:H layers are described by dangling-bonds only, presented by two Gaussian peaks (see parameters in Table 1) and were also kept constant in this study. The ITO layers were modelled as semiconductor layers to fully encompass the band alignment with the a-Si:H layers, thus, taking into account the band-bending in both materials forming the heterojunction [17]. The electrical input parameters for ITO and all other layers are summarized in Table 2 in the Appendix.

Regarding the transport mechanisms at heterointerfaces, the transport through the i-a-Si:H/n-c-Si (encircled 1a and 2a in Fig. 3) heterojunctions is mediated by the inclusion of the built-in thermionic emission model [32], where for particle fluxes across the interface, the condition of continuous quasi-Fermi level and carrier temperature is used [33]. The thermionic emission at these interfaces is also supported by the trap-assisted tunnelling in our modelling approach [34], [35], which is also applied to the ITO/a-Si:H heterointerfaces (encircled 1 and 2 in Fig. 3).

The dominant tunnelling transport depends on the shape of the barrier [11], [21]. The transport through the ITO/p-a-Si:H barrier was modelled accordingly by the trap-assisted and band-to-band tunnelling, whereas at the ITO/n-a-Si:H interface by the trap-assisted and direct tunnelling. We used only non-local tunnelling models (variation of band energies and electric field over depth fully considered, guaranteed zero current at equilibrium). The use of non-local models is necessary since simpler, local models tend to underestimate the tunnelling current at low electric fields [37]. Direct (intra-band) and band-to-band tunnelling are considered as a sum of elastic (momentum of the particle is constant along the tunnelling path) and in-elastic or phonon-assisted (momentum changes across the tunnelling path) mechanisms and are based on [38] and [39]. Trap-assisted tunnelling is modelled similarly as a sum of elastic [34] and in-elastic processes [35].

In the reference cell the p-a-Si:H and n-a-Si:H layers doping densities were set to 2e19 cm^{-3} and 1.5e19 cm^{3}, corresponding to activation energies of 300 meV and 200 meV, respectively. Their electron affinity was set to 3.9 eV and their mobility-gaps to 1.65 eV and 1.72 eV, respectively. All other material and tunnelling parameters used for the reference case are presented in Table 2 in the Appendix.

Table 1: Defect-state parameters for a-Si:H layers and i-a-Si:H/n-c-Si interfaces

Quantity	Symbol	p-a-Si:H	n-a-Si:H	i-a-Si:H	i-a-Si/n-c-Si
Tails					
Tail peak concentrations	$N^{don}_{tailpeak}$ / $N^{acc}_{tail\text{-}peak}$ ($cm^{-3}eV^{-1}$)	1e+21 / 1e+21 [12]	1e+21 / 1e+21 [12]	1e+18 / 1e+18 [12]	/
Tail slopes	σ^{don}_{tail} / σ^{acc}_{tail} (meV)	120 / 70 [12]	60 / 40 [12]	120 / 70 [12]	/
Tail capture cross-sections (charged/neutral)	C^{ch}_{tail} / C^{n}_{tail} (cm^2)	1e-16 / 1e-16 [12]	1e-16 / 1e-16 [12]	7e-15 / 7e-17 [12]	/
Dangling bonds					
Dangling bonds peak Gaussian concentrations	$N^{+/0}_{dbpeak}$ / $N^{0/-}_{db\text{-}peak}$ ($cm^{-3}eV^{-1}$)	1.9e+19 / 1.9e+19 [12] *	2e+19 / 2e+19 [12] *	1e+16 / 1e+16 [12]	2.5e+17 / 2.5+e17 [36]
Dangling bonds std. deviations	$\sigma^{+/0}_{db}$ / $\sigma^{0/-}_{db}$ (meV)	200 / 200 [12]	200 / 200 [12]	150 / 150 [12]	200 / 200 [36]
Dangling bonds capture cross-sections (charged/neutral)	C^{ch}_{db} / C^{n}_{db} (cm^2)	5e-14 / 5e-15 [12] / [5]	5e-14 / 5e-15 [12]	2e-14 / 2e-15 [12]	1e-18 / 1e-19 [36]
Dangling bonds peak energies	$E^{+/0}_{db}$ / $E^{0/-}_{db}$ (eV)	1.1 / 1.3 [12]	0.45 / 0.7 [12]	0.9 / 1.1 [12]	0.46 / 0.66 [36]

* N_{dbpeak} values were changed from the reference in order to obtain realistic activation energies (300 meV and 200 meV) for the p-a-Si:H and n-a-Si:H layers, respectively.

3 Results and discussion

The goal of this analysis is to quantify and understand the effects related to different levels of defect states, in particular the dangling-bond Gaussian peaks ($N_{db\text{-}peak}$), in the p-a-Si:H and n-a-Si:H layers in a SHJ solar cell, for different affinities of ITO contacts as well as different doping levels of the a-Si:H layers.

We start the analysis with the energy band-diagrams of selected structures in thermal equilibrium (Fig. 3). The green, blue and red colours present the vacuum level, conduction and valence bands respectively. The fermi level is presented by the black line. Full lines depict the reference cell (parameters from Tables 1 and 2). Electron affinity of ITO at both sides is marked (double-arrows) for the reference case. The electron affinities of ITOs in the reference cell at the p- and n-sides ($\chi_{ITO\ p\text{-}side}$ = 5.30 eV and $\chi_{ITO\ n\text{-}side}$ = 4.56 eV) of the device have been selected according to [40], presenting realistic values close to the optimum case with respect to the low work function mismatch (ΔWF) between the ITOs and their adjacent doped a-Si:H layers (0.2 eV on both sides of the device) [19]. Please note that for our reference cell, to completely mitigate the mismatch of the work function just by manipulating the ITO electron affinity values, one would have to set them to 5.50 eV and 4.36 eV for the p-side and n-side, respectively. This could be achieved only for the ITO on the n-side of the device, since min. and max. values of electron affinities at the selected doping levels of ITO correspond to 4.2 eV and 5.3 eV [40]. However, besides ITO, there are also other TCO's that could be applied, namely Aluminum doped Zync-Oxide (AZO) and Antimony doped Tin-Oxide (ATO), as they both have high optical transparency due to high band gaps (> 3.1 eV) and can be doped sufficiently to provide a low resistance contact [40]. Regarding the range of possible work functions, AZO work functions range from 3.1 eV to 4.5 eV and for ATO the range is from 3.8 eV to 5.2 eV [40]. Out of these three, ITO offers the highest possible work function of 5.3 eV and is best suited for the ITO/p-a-Si:H contact stack. Other TCOs exhibit lesser optical or electrical parameters in comparison. A review of TCO material characteristics and their application to various solar cells is available in [40] and [41], respectively. The alternative, non-optimal values for the electron affinities of ITOs was the same on both sides ($\chi_{ITO\ p\text{-}side}$ = $\chi_{ITO\ n\text{-}side}$ = 4.93 eV) and resulted in a work-function mismatch of 0.57 eV (same for both sides). This type of symmetric mismatch allowed us to make a fair comparison between the two sides. During the analysis, we changed the electron affinity of ITO from its reference value to the non-optimal case on one side only, while maintaining the reference level on the other side. The dashed lines in Fig. 3 present the energy bands of the case, in which we varied the electron affinity of ITO only on the p-side, while the dash-dot-dot lines present the variation on the n-side. Since similar conditions, with respect to the energetic barriers at the heterointerfaces occur also in the MPP condition, we did not show it in this graph for the sake of simplicity. At the p-side, the two barriers related to the heterojunctions hinder the flow of holes generated in the n-c-Si absorber towards the front ITO, whereas on the n-side they impede the flow of electrons toward the rear ITO contact.

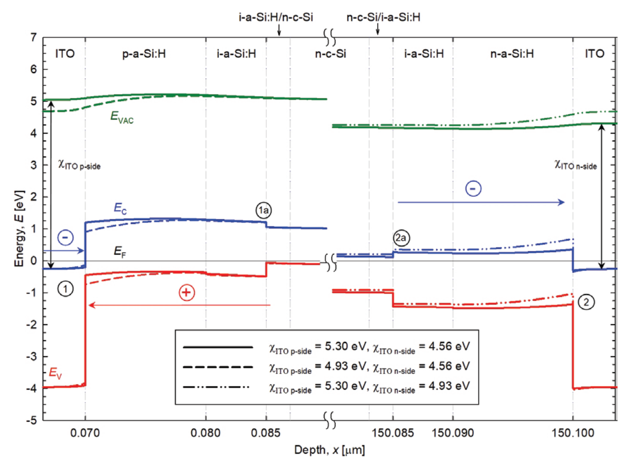

Figure 3: Band-diagrams in thermal equilibrium of the SHJ cell with different electron affinities of ITO layers (χ_{ITO}) at front (p-side) and rear (n-side) of the device (see values in the legend). The reference cell with optimal electron affinities of ITOs is presented by full lines. Symbols E_V, E_F , E_C and E_{VAC} correspond to the conduction-band edge, Fermi level, valence-band edge and the vacuum level, respectively. Circled numbers 1, and 2 mark the ITO/p-a-Si:H and ITO/n-a-Si:H interfaces, respectively. Circled numbers 1a and 2a present the i-a-Si:H/n-c-Si heterojunctions on the p- and n-side of the device, respectively.

In further analysis the $N_{db\text{-}peak}$ parameter of p-a-Si:H and n-a-Si:H layer was chosen for variation since it was pointed out in our previous study that it has detrimental effect on device performance. The variation was done separately for p-a-Si:H and n-a-Si:H layer. In the presented simulation results we varied $N_{db\text{-}peak}$ of both donor and acceptor states (0/- and +/0) simultaneously in a single layer. However, analysis showed that in the case of the p-a-Si:H layer the +/0 type of dangling-bonds affects efficiency the most (see later discussion), whereas the n-a-Si:H layer is affected mostly by the 0/-type.

To illustrate and compare trends related to $N_{db\text{-}peak}$ variation, a series of device simulations were performed where the $N_{db\text{-}peak}$ peak value (height of Gaussian functions) was varied independently of other defect state parameters. Besides the selected reference level of $N_{db\text{-}}$

peak = 1.9e19 cm^{-3}eV^{-1} and 2e19 cm^{-3}eV^{-1} for the p-a-Si:H and n-a-Si:H, respectively, we also included an idealized case with zero $N_{db\text{-}peak}$ (but tail states still present in the material) and the cases with strongly enhanced $N_{db\text{-}peak}$ values up to and including 6e19 cm^{-3}eV^{-1}.

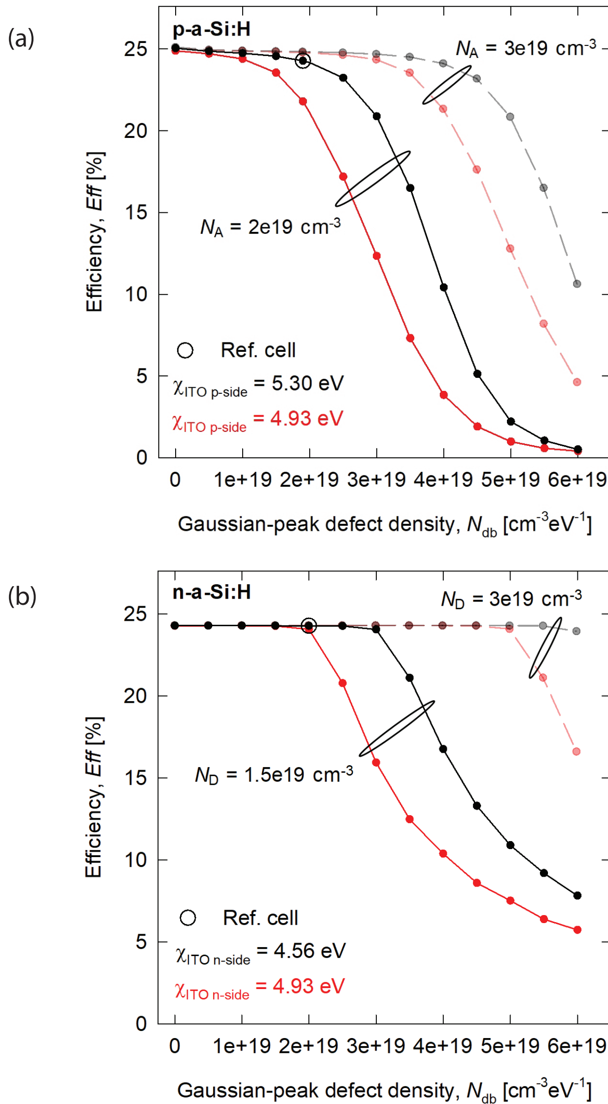

Figure 4: a) Efficiency vs. $N_{db\text{-}peak}$ defect density variation in p-a-Si:H and b) in n-a-Si:H layer. Full lines represent nominal doping concentration of a-Si:H doped layers, whereas the dashed semi-transparent lines represent hypothetical high doping concentration (3e19 cm^{-3}). Cells with optimized values of the adjacent ITO electron affinity are presented by black curves (5.30 eV for the p-side and 4.56 eV for the n-side). Red curves present the non-optimal values (4.93 eV for both p- and n-side of the device). The case for the reference cell (Table 2, Appendix) is circled. It has to be noted that when the electron affinity of ITO is varied on one side of the device, the electron affinity of ITO at the other side is set to the reference (optimized) value.

Besides electron affinities of ITO, two doping levels of p-a-Si:H and n-a-Si:H layers were also included in simulations (reference values and hypothetically high doping values of $N_A = N_D$ = 3e19 cm^{-3} for p- and n-layer respectively). Note that the chosen value for the high levels of doping density presents a purely hypothetical case that cannot be achieved with normal a-Si:H material as they would result in the corresponding activation energy values of ~0.2 eV and ~0.1 eV for the p-a-Si:H and n-a-Si:H layers, which is not achievable in praxis. This hypothetical case is used to indicate the effects related to materials where lower activation energies, and thus, higher effect of doping can be achieved, e.g. nano-crystalline silicon or other meta-materials such as metal oxides. With this hypothetical case we want to stress and quantify the importance of efficient doping of charge carrier selective layers in relation to different ITO contacts.

In Fig. 4a-b the black and red lines present cases with optimal (χ_{ITO} = 5.30 eV and 4.56 eV for the p-a-Si:H and n-a-Si:H layers respectively) and non-optimal electron affinity values of ITO layers (χ_{ITO} = 4.93 eV for both layers), respectively. The hypothetical case of high-doping values is presented with semi-transparent lines. The points on the graphs, presenting the reference case are also encircled.

The results presented in Fig 4a and 4b show that in general the increase of $N_{db\text{-}peak}$ starts to lower the efficiency of the device at all conditions, although the decreases start at different levels of defect states ($N_{db\text{-}peak}$ values).

Focusing first on the p-a-Si:H side of the cell (Fig 4a), in the case with nominal doping level and reference electron affinity of ITO at the p-side (full black line) we can observe that efficiency starts to rapidly drop, when $N_{db\text{-}peak}$ becomes greater than ~2e19 cm^{-3}eV^{-1}. Higher level of doping in this case (dashed semi-transparent black line) shifts this decline of efficiency to $N_{db\text{-}peak}$ values of around 3.5e19 cm^{-3}eV^{-1}. In both cases, reducing the $N_{db\text{-}peak}$ parameter below the reference value will yield an increase in efficiency of less than 1 % when compared to the reference $N_{db\text{-}peak}$. In case of nominal doping we increase the reference efficiency from 24.28 % to ~25 % according to simulations. For higher doping this increase is even less significant. Focusing now on the second case, where the electron affinity of ITO at the p-side is not optimal and doping is nominal (full red line), we can observe that efficiency drops from the reference value of 24.28 % to 21.79 % even at the reference level of the $N_{db\text{-}peak}$ parameter (1.9e19 cm^{-3}eV^{-1}). Additionally, we can see an even faster decline in efficiency as $N_{db\text{-}peak}$ parameter surpasses the 2e19 cm^{-3}eV^{-1} mark. Of note is the observation, that in this case, reducing the $N_{db\text{-}peak}$ significantly below its reference level (1.9e19 cm^{-3}eV^{-1})

mitigates the negative effects of non-optimal electron affinity of ITO. Higher doping (dashed semi-transparent red line) has again a similar effect as before, as it delays the onset and slows down the decline in efficiency until $N_{db\text{-}peak}$ surpasses the 3.5e19 cm^{-3}eV^{-1} mark. Reducing the defect density below 1.9e19 cm^{-3}eV^{-1} does not significantly improve the efficiency also in this case. In general, the negative effects of increasing the defect density are amplified when ITO electron affinity is not optimized (high enough) for the p-a-Si:H layer. The effect can be mitigated by higher doping levels of the pa-Si:H. Additional simulations showed that variation of the ITO band-gap has a much lower effect on efficiency than the electron affinity at different $N_{db\text{-}peak}$ values (not shown here).

The general trends regarding sensitivity of efficiency to the $N_{db\text{-}peak}$ parameter are similar also for the n-a-Si:H layer. Although, it can be observed in the reference case of electron affinities of ITO at the n-side that the efficiency is much less sensitive to defects in the n-a-Si:H layer than that in the p-a-Si:H layer. Further simulation results (not shown in the graphs) revealed that this sensitivity trend remains almost the same when the device is illuminated from either the p- or n-side, and is also independent of the doping type of the c-Si wafer (n- or p-type). Further on, for simulations where non-optimal selection of electron affinities (in this case χ_{ITO} = 4.93 eV) for the ITOs at both p- and n-side of the device (not included in Fig. 4) the sensitivity of the efficiency to variations of $N_{db\text{-}peak}$ in the p-a-Si:H and in the n-a-Si:H layer, surprisingly becomes comparable. It has to be noted that the differences between the reference (close to optimal) and the alternative values of the ITO electron-affinity for both sides are the same but differ in the sign: $\Delta\chi_{ITO}$ = 0.37 eV for the p-side and $\Delta\chi_{ITO}$ = -0.37 eV for the n-side. Additional simulations revealed that using an electron affinity value of 4.36 eV for the ITO at the n-side, which completely mitigates the work function mismatch, does not yield any increase in efficiency because the work function mismatch at the p-side already presents a bottle-neck even when an optimized value of electron affinity (5.3 eV) is used for ITO at the p-side.

A close comparison of the cases where non-optimal electron affinities were applied to ITOs on the p- and n-sides (red lines in Figs. 4a and 4b) and the $N_{db\text{-}peak}$ values were set to their reference values (1.9e19 cm^{-3}eV^{-1} and 2e19 cm^{-3}eV^{-1} for p-a-Si:H and n-a-Si:H respectively) revealed a significant difference between the efficiencies (21.79 % and 24.06 % for the p- and n-side respectively), despite the same work-function mismatch on both sides (ΔWF=0.57 eV). This is due to a difference in the distribution of defect states in p-a-Si:H and n-a-Si:H, with the distribution in p-a-Si:H affecting the cell more severely compared to n-a-Si:H [16]. Additionally, one can observe in Fig. 3, that the conduction band of the ITO and the valence band of p-a-Si:H do not overlap at the heterojunction (encircled 1 in Fig. 3), which means that BBT is not very efficient, thus the transport of charges across the barrier on the p-side is heavily dependent on TAT. On the n-side, however, the transport across the barrier (encircled 2 in Fig. 3) relies on both TAT and Direct tunnelling, which makes the tunnelling on the n-side more efficient compared to the p-side [9], [11], [21] in this case. On a related note, optimal electron affinity of the ITO on the p-side also brings the mentioned energy bands closer together when compared to the non-optimal case (Fig 3.), which not only decreases the work function mismatch, but also improves BBT tunnelling efficiency. The effect is even more pronounced when hypothetically high doping is applied to the p-a-Si:H as activation energy decreases and makes the bands come closer together even more (not shown in Fig. 3). In contrast, on the n-side (encircled 2 in Fig. 3), the lower (optimal) value of the ITO electron affinity separates the conduction band of ITO from the valence band of n-a-Si:H even more, which does not affect the tunnelling noticeably, since BBT is not a factor on this side. However, it does lower the DT barrier height and improves the transport of electrons towards the anode. Similar to the p-side, this effect is even more pronounced when hypothetical levels of doping are applied.

In order to see which tunnelling mechanism is dominant at the ITO/p-a-Si:H and ITO/n-a-Si:H heterointerfaces under various conditions (different electron affinities of ITO and various doping levels of the doped a-Si:H layers), we performed simulations where we applied only one tunnelling mechanism at the time at a specified ITO/a-Si:H heterointerface. The results showed, that TAT is the dominant tunnelling mechanism at the ITO/p-a-Si:H heterointerface for both optimal (5.3 eV) or non-optimal (4.93 eV) values of ITO electron affinity as well as for both realistic (2e19 cm^{-3}) and hypothetical (3e19 cm^{-3}) effective doping density levels of the p-a-Si:H layer. Simulations indicated that the contribution of BBT is negligible compared to TAT in this case. These observations are also in accordance to predictions published in [21]. At the ITO/n-a-Si:H side, however, according to simulation results either TAT or DT on their own can provide a sufficient transport path and yield almost identical efficiencies for both ITO electron affinity values, as well as for both realistic and hypothetically high effective doping levels of the n-a-Si:H layers.

Note, that the change in electron affinity of ITO affects (i) band offsets between the ITO and a-Si:H as well as (ii) the work function mismatch between the materials, that influences the space-charge-region (SCR) prop-

erties of the ITO/a-Si:H heterointerface, which will be discussed later. At the p-a-Si:H side, an increase in electron affinity of ITO also increases band offsets, resulting in higher barriers for electrons and holes (see Fig. 3), which could potentially reduce tunnelling efficiency. However, we observed an increase in efficiency when electron affinity was increased, which means that the possible negative effects of increased band offsets are far outweighed by the positive effects of decreasing the work function mismatch. At the n-side, the reduction of electron affinity results in smaller band offsets as well as a reduction in the work function mismatch and higher efficiency as well. The results indicate, that changes in band offsets due to variation in electron affinity of ITO in the presented range do not significantly affect tunnelling efficiency at the ITO/a-Si:H interface, but the same changes in electron affinity define the work function mismatch, and thus affect the SCR properties of the interface, as will be explained later. Note, that tunnelling must be applied at ITO/a-Si:H heterointerfaces for the cell to function properly, as explained in our previous publication [16]. We would like to state here, that tunnelling is already good enough in both cases of ITO electron affinity on both sides when defect density is not extremely high ($N_{db\text{-}peak}$ < 3e19 cm^{-3}eV^{-1} as efficiency of the cell is above 20 % in those cases. Therefore, the main reasons for the observed efficiency trends when ITO electron affinity is varied and defect density is increased have to be related to other mechanisms.

To further examine and explain the efficiency trends presented in Fig. 4a, we show in Fig. 5a-c also simulation results of the fill-factor (*FF*), short-circuit-current density (J_{SC}) and open-circuit voltage (V_{OC}) of the cell as a function of the $N_{db\text{-}peak}$ parameter in the p-a-Si:H layer. From now on, we will focus on the p-side of the device, recognizing that the defects in the p-a-Si:H layer have a stronger impact on the performance of the device under the given circumstances. Similar to the previous figures, the black and red curves in Fig. 5a-c show cases with optimal χ_{ITO} (5.30 eV on the p-side and 4.56 eV on the n-side), and non-optimal χ_{ITO} values (4.93 eV on both sides). The solid and dashed lines correspond to the nominal (2e19 cm^{-3}) and hypothetically high (3e19 cm^{-3}) doping levels, respectively. The simulation point corresponding to the reference cell (Table 2, Appendix) is circled.

Detailed comparison between the graphs in Fig. 5 reveals that *FF* and V_{OC} are more sensitive to $N_{db\text{-}peak}$, followed by J_{SC}. For the highly doped p-a-Si:H layer one can observe almost no decrease in J_{SC} even for extremely high $N_{db\text{-}peak}$ values, which has to be considered as a hypothetical (idealised) case. These observations also corroborate the statement that tunnelling is sufficient regardless of the chosen ITO electron affinity values. Let us now examine the effects of dangling-bonds in the p-a-Si:H layer on *J*(*V*) curves for some selected cells considering nominal doping levels ($N_{A\ p\text{-}a\text{-}Si:H}$ = 2e19 cm^{-3}) in Fig. 5d. The grey line represents the reference cell (Tables 1, 2) with reference (optimal) electron affinity of ITOs and the reference $N_{db\text{-}peak}$ = 1.9e19 cm^{-3}eV^{-1} in p-a-Si:H. The black curve corresponds to the cell with increased $N_{db\text{-}peak}$ = 2.5e19 cm^{-3}eV^{-1}, the remaining parameters are the same as for the reference cell (Tables 1 and 2). The red curve presents the case with a non-optimal electron affinity of ITO ($\chi_{ITO\ p\text{-}a\text{-}Si:H}$ = 4.93 eV) and increased $N_{db\text{-}peak}$. The selected curves reflect the trends observed for the related parameters (J_{SC}, V_{OC}, *FF*) in the region of moderate increase in $N_{db\text{-}peak}$. J(V) curves indicate that besides lower V_{OC}, the *FF* decreased mostly due to the drop of the voltage at the maximum power point (V_{MPP}) as indicated in the figure. The same general trend is observed for all cells, with different electron affinity of ITO layers, however the scale of change is different. The drop in V_{MPP} is more pronounced when non-optimal electron affinity of ITO is used, and even more-so when defect states are increased. Of note is also the observation that applying non-optimal electron affinity of ITO alone decreases the *FF* in a similar manner as increasing only the defect states since V_{MPP} drops in both cases.

We found that the explanation for the decrease of V_{MPP} and V_{OC} can be related to the Poisson equation and how the total charge (free holes and electrons, ionized dopants and trapped charge) determines the final voltage of the cell when electron affinity of ITO and dangling-bond defect states are varied. In our previous publication [16] we explained in great detail how the voltage drops due to increased defect density and related charge re-distribution as the electric field that is needed for charge separation becomes weaker. We also explained that work-function mismatch dictates the amount of ionized ITO charge that needs to be screened in the adjacent a-Si:H layer in order to obtain a sufficient electric field in the c-Si bulk that is needed for charge separation and good MPP voltages [16]. When ITO with a non-optimal electron affinity is applied, as was the case here, the work function mismatch is increased. Then, higher dangling-bond defect density reduces the charge-screening capability of the p-a-Si:H which leads to an even lower electric field and the observed trends of low V_{MPP} and V_{OC}.

Changes in electron affinity of ITO directly affect the ITO work function. When the work function of ITO is smaller than that of p-a-Si:H (the difference is referred to as work function mismatch), electrons (mediated by tunnelling) flow from ITO toward p-a-Si:H and a positively charged part of the space-charge-region (SCR) is

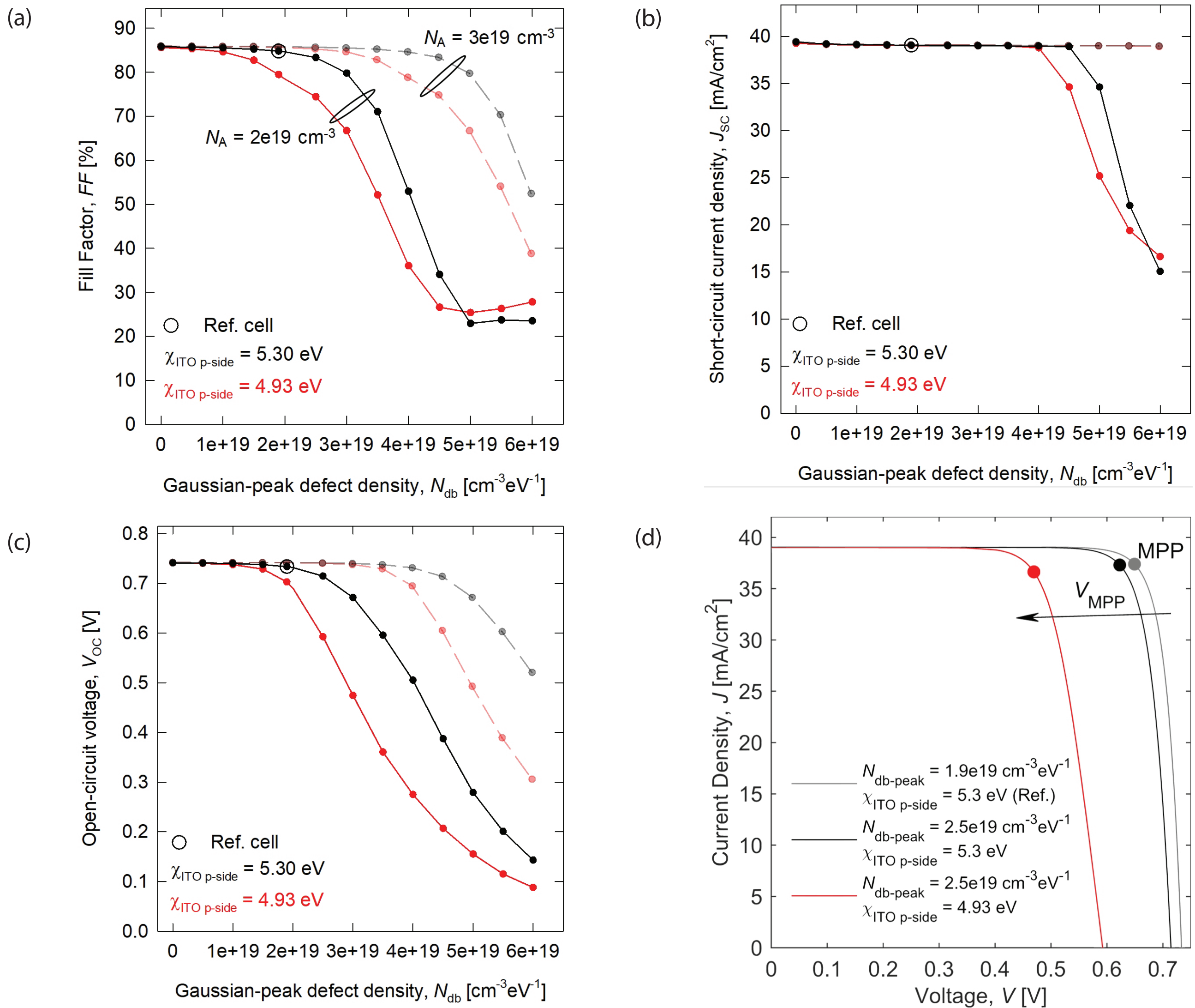

Figure 5: a) *FF*, b) V_{OC}, c) J_{SC} vs. $N_{db\text{-}peak}$ defect-density variation in the p-a-Si:H layer. Full lines correspond to nominal doping density of p-a-Si:H layer (2e19 cm^{-3}), whereas dashed lines represent the device with high doping density $N_{A\ p\text{-}a\text{-}Si:H}$ = 3e19 cm^{-3}). Devices with reference (optimal) values of the ITO electron affinities are presented by black curves (χ_{ITO} = 5.3 eV for the p-side and 4.56 eV for the ITO at the n-side). Red curves correspond to cases where ITOs are not optimal (χ_{ITO} = 4.93 eV for both p- and n-side of the device). The legend in a) applies also to b) and c). d) *J*(*V*) curve for the reference cell (grey) and selected cases with high $N_{db\text{-}peak}$ (2.5e19 cm^{-3}eV^{-1}) and ITO electron affinity at the p-side set to 5.30 eV (black) and 4.93 eV (red). All presented cases were simulated at nominal doping level of the p-a-Si:H layer (2e19 cm^{3}).

formed on the ITO side of the ITO/p-a-Si:H heterojunction (due to ionized donor atoms), whereas the negatively charged part of the SCR forms in the p-a-Si:H due to ionized acceptor dopants and neutralized +/0 states (that are now occupied by electrons that came from ITO and no longer contribute to the positive charge). The resulting electric field is oriented in the opposite direction than the electric field at the i-a-Si:H/n-c-Si heterojunction. As the work function mismatch is increased, the SCR is broadened even deeper into the p-a-Si:H region. The broadening of this SCR is actually depleting the p-a-Si:H layer, which can result in a weaker electric field (needed for charge separation) in the n-c-Si absorber when the SCR is not well contained in the p-a-Si:H. The mentioned changes affect the redistribution of charges throughout the device, which also determines the external voltage.

In order to mitigate the negative effect of the work function mismatch, that lowers the voltage (V_{MPP} and V_{OC}) and *FF*, at the ITO/p-a-Si:H (n-a-Si:H) heterointerface, the negative (positive) charge in the p-a-Si:H (n-a-Si:H) layer must be able to screen the opposite charge in the SCR of ITO. The screening capability of a-Si:H de-

pends on effective doping concentration, defect density and layer thickness. Thicker layers with high doping concentrations and low defect density are capable of screening more ITO charge. The increase in dangling-bond defect density mitigates the positive effect of doping and reduces the screening capability of the layer. In addition, as we discussed in our previous publication [16], an increase in peak dangling-bond defect density ($N_{db\text{-}peak}$) in the p-a-Si:H layer reduced both V_{OC} and *FF*, whereas J_{SC} changed only slightly. The drop in *FF* was explained by lowering of the V_{MPP}, whereas J_{MPP} was observed to be almost unaffected, since at MPP conditions, total recombination was still far smaller compared to optically generated current. We concluded, that an increase in $N_{db,\ peak}$ reduces efficiency especially due to lower V_{MPP} ($Eff = \frac{J_{SC} \cdot V_{OC} \cdot FF}{P_{in}} = \frac{J_{MPP} \cdot V_{MPP}}{P_{in}}$).

To explain the drop in V_{MPP} we followed the Poisson's equation, which relates charge distribution to the voltage between the terminals. A thorough analysis of total charge and all of its components (free charge, trapped charge in defect states and ionized dopant atoms) revealed that the increase in $N_{db\text{-}peak}$ in p-a-Si:H resulted in a reduction of positive charge in the SCR of ITO and a reduction of negative charge in the SCR of p-a-Si:H. The reduction of negative charge in p-a-Si:H was shown to be an increase in positive charge in the p-a-Si:H layer due to unoccupied +/0 dangling-bond states, that are positioned at energies where they are unlikely to be occupied by an electron and remained positively charged. We used the Poisson's equation and showed, that this virtual shift of positive charge from ITO into the p-a-Si:H layer due to an increase in $N_{db\text{-}peak}$ resulted in the observed reduction in V_{MPP}. We also showed, that 0/- states remained neutral and did not significantly affect the total charge in p-a-Si:H. All of the above is true also for all the cases presented in this work (both doping levels and dangling-bond defect densities).

Before moving on to conclusions, we would like to provide a brief commentary regarding the reference efficiency of our simulated device (24.28 %), where both ITO layers have optimal electron affinity values (5.3 eV and 4.56 eV for the p- and n-side, respectively). It has been reported that SHJ cells have the potential to reach efficiencies as high as ~27 % [9]. However, this can be achieved by employing additional layers, such as p-type SiC_x or SiO_x and using the IBC architecture. Without these additional layers, the record cell, made by Kaneka, reached efficiency of 26.7 % [42], thanks to the IBC design, that allows for high J_{SC} = 42.65 mA/cm^2. In comparison, our reference cell, that uses optimized ITO layers, achieves J_{SC} = 39.02 mA/cm^2. Should we calculate the efficiency of our reference cell, by using the J_{SC} of the record cell, we would get efficiency around 26.5 %, which is also in accordance to the simulations presented in other publications that were simulating and optimizing IBC SHJ solar cells [9]. Therefore, the difference between the efficiencies of IBC and planar architectures can be mostly attributed to better J_{SC} of IBC devices. In addition, the V_{OC} and *FF* values of our reference cell simulations are very similar to the ones reported for the record cell and comparable to the ones presented in [9].

4 Conclusion

We applied opto-electrical modelling of a SHJ solar cell to study ITO/doped a-Si:H selective contacts in terms of ITO electron affinity and dangling-bond Gaussian peaks (amphoteric defects) of the doped a-Si:H layers. In the simulation structure, the ITO layer at the p- and n-side of the device was considered as a full semiconductor layer. DT, BBT and TAT tunnelling mechanisms were included in simulations at ITO/doped a-Si:H selective contacts. We demonstrated that optimizing the electron affinity of the ITO layers is critical when the doped a-Si:H layers are insufficiently doped or have high concentrations of dangling-bond defect states. We showed that optimization of electron affinity of ITO is especially important at the p-side of the device due to a less favourable trap distribution and poorer tunnelling efficiency compared to the n-side. We showed that the ITO at the p-a-Si:H layer should have electron affinity as high as possible (~5.3 eV) in order to minimize the work function mismatch (which was only 0.2 eV in this case), as higher values of the work function mismatch can deplete the p-a-Si:H layer to the point, where it is unable to sufficiently screen the positive charge in the space-charge-region of ITO, resulting in a diminished electric field in the n-c-Si absorber, and consequently poor charge separation capability of the cell, leading to a reduction in *FF* and V_{OC}. Conversely, the ITO at the n-a-Si:H layer should have electron affinity as low as 4.56 eV (work function mismatch is 0.2 eV in this case). Lower values of electron affinity enabling lower work function mismatch on the n-side did not further improve efficiency, due to the already present work function mismatch at the p-side (0.2 eV in the optimal case). Low values of V_{OC} also confirmed poor charge-separation capability of the cell, when electron affinity of ITO results in a higher work function mismatch between the ITOs and doped a-Si:H layers. We demonstrated that the work function mismatch between ITO and doped a-Si:H layers makes the solar cell efficiency more sensitive to increased dangling-bond defect states in the doped a-Si:H layers as higher dangling-bond defect density reduces the layers' ability to screen the charge in the SCR of ITO as it negates the positive effect of doping. We also observed that when

ITO electron affinity at the p-a-Si:H (n-a-Si:H) layer is lower than 5.3 eV (higher than 4.56 eV) and doping is nominal (2e19 cm^{-3} and 1.5e19 cm^{-3} for p-a-Si:H and n-a-Si:H, respectively), only the *FF* (and not V_{OC} or J_{SC}) can be improved by lowering the dangling-bond defect density below the reference level (1e19 $cm^{-3}eV^{-1}$). In contrast, J_{SC} was affected only at extremely high levels of defect densities even when electron affinity of ITO at the p-a-Si:H (n-a-Si:H) was lower (higher) than 5.3 eV (4.56 eV). We also concluded that tunnelling efficiency at the ITO/a-Si:H interface is not significantly affected by the changes in the band offsets, caused by variation in electron affinity of ITO, whereas the changes in the work function mismatch, as the SCR properties of the heterointerface were changed, affected the cell significantly. An increase in electron affinity of ITO at the p-a-Si:H layer results in increased conduction and valence band offsets, but the reduction in work function mismatch outweighs the negative impact of increased barrier heights and an increase in efficiency was observed, whereas a reduction in electron affinity of ITO at the n-a-Si:H layer results in even lower band offsets as well as a reduction in work function mismatch. It was also shown that TAT is the dominant transport mechanism at the ITO/p-a-Si:H heterojunction for all presented cases. At the ITO/n-a-Si:H interface, both DT and TAT provide an efficient transport path and yield very similar results when either of the two is applied as the only tunnelling mechanism at that interface. Results presented in this paper give indications for acceptable defect levels in doped amorphous-silicon layers in relation to optimality of ITO electron affinity for the ITO/a-Si:H selective contacts and can serve as a roadmap when designing selective contacts with alternative materials for SHJ cells.

5 Appendix

Table 2: Input parameters for the reference case

Quantity	Symbol	n-c-Si	p-a-Si:H	n-a-Si:H	i-a-Si:H	i-a-Si:H/n-c-Si	ITO
Relative Dielectric Constant	ε_r	11.9 [43]	11.9 [43]	11.9 [43]	11.9 [43]	11.9 [43]	8.9 [44]
Electron Affinity	χ (eV)	4.05 [12]	3.9 [12]	3.9 [12]	3.9 [12]	4.05 [12]	5.3 / 4.56 (p-side/n-side) [40]
Band-gap (Mobility-gap)	E_{gap} (eV)	1.12 [36]	1.65 [12]	1.72 [12]	1.70 [12]	1.12 [36]	3.7 [9]
Effective Doping Conc.	N_D / N_A (cm^{-3})	2e+15 / 0 [12]	0 / 2e+19 [12]	1.5e+19 / 0 [12] *	2.2e+15 / 0 [12]	2e+15 / 0 [12]	1e+20 / 0 [9]
Density of States	N_C / N_V (cm^{-3})	2.8e+19 / 3.1e+19 [43]	2e+20 / 2e+20 [43]	2e+20 / 2e+20 [43]	2e+20 / 2e+20 [43]	2.8e+19 / 3.1e+19 [43]	4.12e+18 / 1.17e+19 [44], [45]
SRH life-times	τ_e / τ_h (ms)	1 / 10 [36]	/	/	/	1/10 [36]	/
Mobilities	μ_e / μ_h (cm^2/Vs)	1342 / 452 [43]	10 / 1 [12]	10 / 1 [12]	10 / 1 [12]	1342 / 452 [43]	50 / 30 [9]
Tunnelling mass (DT, TAT and BBT)	m*	/	0.1 [9]	0.1 [9]	0.1 [9]	0.1 [9]	0.1 [9]
Trap volume (TAT)	V_{trap} (μm^{-3})	/	1e-11 [8]	1e-11 [8]	1e-11 [8]	1e-11 [8]	/
Huang-Rhys con. (TAT)	H_{rhys}	/	2 [8]	2 [8]	2 [8]	2 [8]	/
Phonon Energy (TAT)	E_{ph} (meV)	/	37.78 [8]	37.78 [8]	37.78 [8]	37.78 [8]	/
Coupling factor (DIRECT, BBT)	g_e/g_h	/	1 / 1 [9]	1 / 1 [9]	1 / 1 [9]	1 / 1 [9]	1 / 1 [9]

* Effective doping concentration was changed from the reference to obtain realistic activation energy for the n-a-Si:H layer (200 meV)

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7 References

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MIDEM 2022

57th INTERNATIONAL CONFERENCE ON MICROELECTRONICS, DEVICES AND MATERIALS WITH THE WORKSHOP ON ENERGY HARVESTING: MATERIALS AND APPLICATIONS

September 14th – September 16th, 2022
Hotel City, Maribor, Slovenia

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Abstract submission deadline:
May 1, 2022

Acceptance notification:
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July 31, 2022

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