EFFICIENT BUILT-IN SELF-TEST OF A HIGH-PRECISION ELECTRONIC WATT-HOUR METER

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Key words: built-in self-test, sigma-delta modulator, watt-hour meter

Abstract: To simplify the testing procedure of a mixed signal integrated circuit, which requires low noise equipment and a powerful computer, a built-in self-test is proposed in this paper. The test signal source is integrated in the ASICs and requires only small additional circuitry. The main benefits of using a built-in self-test are shorter testing time, no need for expensive testing equipment and the possibility of performing the test in the field. In this paper we describe an integrated signal generator, an algorithm for accurate evaluation of the system and some simulation results, which prove that conventional FFT analysis can be replaced by RMS function calculations.

Učinkovito vgrajeno testiranje v precizijskem elektronskem števcu električne energije

Kjučne besede: vgrajeno testiranje, sigma-delta modulator, števec električne energije

Izvleček: Za poenostavitev testnega postopka mešanega analogno digitalnega integriranega vezja, ki potrebuje nizko šumno opremo in zmogljiv računalnik, je predlagano vgrajeno testiranje. Test je integriran v ASIC-u in za svoje delovanje potrebuje minimalno število dodatnih komponent. Glavne prednosti uporabe vgrajenega testiranja so zmanjšanje časa testiranja, ne potrebujemo drage testne opreme ter možnost opravljanja testa na terenu ne samo med proizvodnjo ali na servisu. V članku je opisan integriran signalni generator, algoritem za ocenjevanje točnosti sistema in simulacijski rezultati, ki dokazujejo, da je FFT analizo mogoče nadomestiti z uporabo RMS funkcije.

1. Introduction

Watt-hour meters are very accurate devices and include many analog and digital circuits for precise measurement of electrical energy consumption /1/. Because different modules inside the instrument have to work accurately and reliably for a very long time, it is recommended that the instrument is able to monitor its most important parameters, not only during the manufacturing process, but also in the field. One of the most important modules inside the watt-hour meter is a high precision 2nd order sigma-delta modulator, the task of which is to accurately convert analog signal from the sensors to a digital representation, which is further processed and evaluated in the DSP. In general, for a reliable test, a low noise signal generator is needed as the input signal, while the response is usually analyzed using FFT. In the laboratory and during the test, we can use an accurate low noise signal generator as well as a Digital Signal Processor (DSP) to analyze the response characteristics. In field testing such equipment is not available. The solution to the testing problem is a Built-In Self-Test (BIST), where all the necessary equipment is integrated inside the circuit. The measurement accuracy of a BIST must be good enough to fulfill the accuracy requirements of the watt hour meter instrument.

Many different papers have been written about a built-in self-test of the mixed signal circuits. Usually, ramp or sine-wave signals are digitally generated and converted to analog domain /2/, /4/, /5/, /6/. Unfortunately, all such solutions need a lot of silicon area and have a high power consumption which makes them inappropriate for our application.

Different methods may be used for analyzing the output signal; the most accurate and complete is FFT which is very convenient if a powerful DSP is available /2/, /5/. However, this method is not efficient enough for the purpose of the BIST because it requires a lot of computational resources. Other methods are, for example, the sine-wave fitting method /2/, /4/ and the narrow-band filtering method /2/. With the sine-wave fitting method it is necessary to convolve the input sine-wave signal with the output signal. The given results enable the calculation of offset voltage, signal power and total-harmonic-distortion-and-noise (THD-N) values. From signal power and THD-N, one can further calculate the signal-to-noise and distortion ratio (SNDR) and the resolution in a specific frequency band. The ratio between the input and the output signal determines the gain and the accuracy. In the second method the narrow-band digital filter is used, which has two outputs: signal and notch output. At signal output the signal is band-pass filtered and contains only the input spectral component; the signal power can be estimated. At notch output the input signal is attenuated by the stop-band filter and only the noise and harmonic components pass-through the filter; the THD-N and noise power can be computed.

From both outputs the SNDR, resolution and accuracy of the conversion can be calculated.

Both methods are quite efficient, but require a lot of additional integrated digital circuits. In our watt-hour meter, a DSP circuits for calculation of energy consumption and RMS values of voltage and current are already available and therefore, it would be most efficient to use them. In this work we propose to calculate SNDR and accuracy of the measurements from the measurements of the RMS values.

In this paper the efficient BIST methodology used in the watt-hour meter is presented together with some simulation results. Section 2 presents BIST architecture, while a simple on-chip signal generator is presented in section 3. In section 4 modeling details of all important modules in the watt-hour meter are presented. In section 5, the theoretical basis for the BIST algorithm using built in RMS functions are described. Section 6 presents some simulation results that relate most important deviations of circuit parameters to the RMS result. The conclusions are given in section 7.

2. BIST architecture

The system for precision measurements of voltage and current signals consists of two 2nd order sigma-delta modulators; one for each measurement path (Figure 1). After A/D conversion, the digital signals have to be processed by digital filters, after which the RMS values are computed. The current measurement path is almost identical to the voltage measurement path except that it requires a preamplifier to amplify the "current" signal. Since both measurement paths are almost identical, all further descriptions and simulation results will be presented only for the voltage measurements path.

For BIST, the input signal generator has to be integrated in the ASIC. The signal generator consists of a digital generator, a D/A converter (DAC) and the chopper. The signal is connected directly to the ΔΣ modulator input via multiplexer. The result of the conversion is one bit digital bit-stream, which is processed by cascaded filters: a CIC, compensation and a high pass filter. The CIC filter attenuates high frequency components and shaped quantization noise, while compensation filters adjust the signal level in the pass-band. The attenuation of a DC component is accomplished with a high pass filter. The result of digital signal processing is a stream of the 24-bits parallel words. To compute the consumption of energy, the "voltage" and the "current" signals are multiplied and integrated. The RMS value can also be calculated using a built-in RMS function; this function is used during the BIST, which is controlled by the block control BIST (Figure 1). To evaluate the system accuracy, the data from RMS functions are collected. From this data the average RMS value and standard deviation of RMS values are calculated.

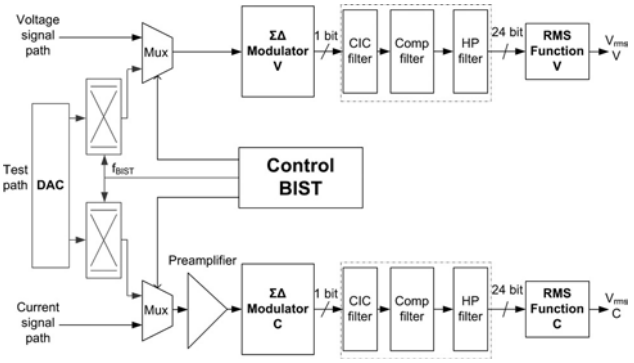

Fig. 1: Block diagram of energy meter ASIC

3. Stimulus generator

A square wave signal generator is used as a test signal source. It consists of a digital block, digital to analog converter (DAC) and a chopper. The DAC generates programmable DC voltages (Figure 2). Voltage levels can be selected to define different amplitudes of the square wave signals. For stable and low noise DC voltage we need a stable supply voltage and small resistance resistor divider. To see the mayor influences due to non-idealities the modulator must be tested at full scale defined by . To transform the DC signal into a square wave a chopper block is used that transforms DC voltage to a square-wave signal with chopper frequency (f_{BIST}). This frequency defines the fundamental frequency of the test signal and is generated in the digital "Control BIST" circuit.

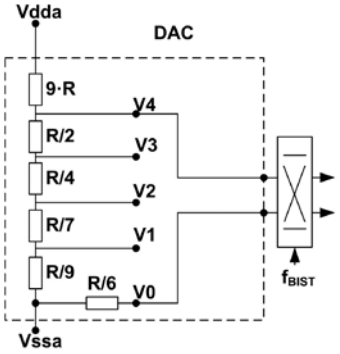

Fig. 2: Scheme of DAC and chopper at the input of modulator

$$V_4 = \frac{253}{2521} \cdot (Vdda - Vssa) \quad (1)$$

4. Modeling the BIST algorithm and circuits

4.1. Modeling and simulation of 2nd order sigma-delta modulator

To test the BIST effectiveness a Matlab model of the 2nd order sigma-delta modulator (Figure 3) /9/ was built. The model includes all important non-idealities /11/: open loop

gain, gain bandwidth, slew-rate, saturation nonlinearity, offset voltage, input noise density of the amplifiers etc.

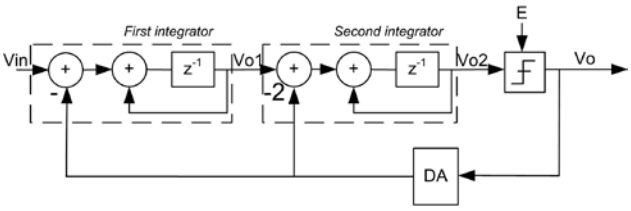

Fig. 3: 2nd order sigma-delta modulator

4.2. CIC filter

Output of the sigma-delta modulator is a digital bit-stream that consists of input signal, which contains all deviations due to eventual problems in the analog part of the circuit and high frequency noise shaped quantization noise. To remove out-of-band shaped quantization noise a 3rd order Cascaded integrator-comb (CIC) filter /7/, /8/ is used. The architecture of the CIC filter is such that the clock rate is reduced by a factor of R after the attenuation of HF part of the quantization noise. Its z-domain transfer function is defined by /9/. The architecture of the CIC filter is presented in Figure 4 /8/. In our simulations a bit-true model is used.

$$H_{CIC}(z)=\left(\frac{11}{R}\frac{-z^{-R}}{1-z^{-1}}\right)^{N} \tag{2}$$

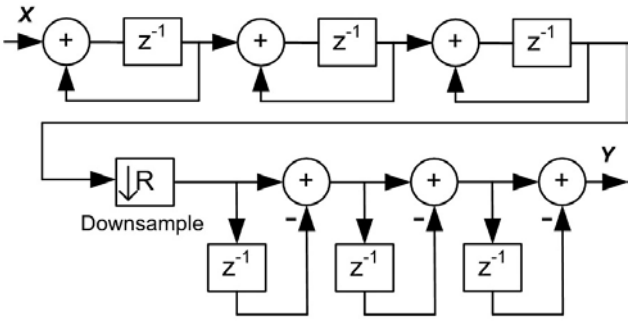

Fig. 4: Decimation using 3rd order CIC filter

4.3. Compensation filter

CIC filter's frequency characteristic is not-flat in the pass band and therefore, a compensation FIR (cFIR) filter is needed. The magnitude vs. the frequency response of the cFIR filter is an inverted function of the CIC filter's pass band response. The result of the two responses is a flattened magnitude characteristic in the signal band (Figure 6).

4.4. High pass filter

Before RMS calculation it is necessary to remove the remaining DC component that occur due to the imperfections of the switched-capacitor circuits and input offset voltage of the amplifiers; they are partly reduced using chopping technique /1/. Unfortunately, due to parasitic capacitances, some DC errors still remain and can be removed using a high pass filter that has the z-domain's characteristics given in. The filter architecture is presented in Figure 5.

$$H(z)=\frac{1-z^{-1}}{1-\alpha z^{-1}} \tag{3}$$

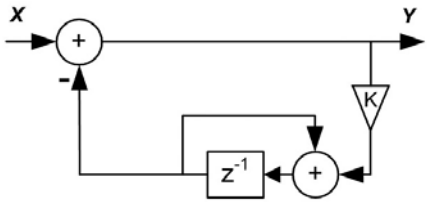

Fig. 5: High pass filter

Frequency responses of CIC, cFIR and high pass filter, together with their combined response, are presented in Figure 6.

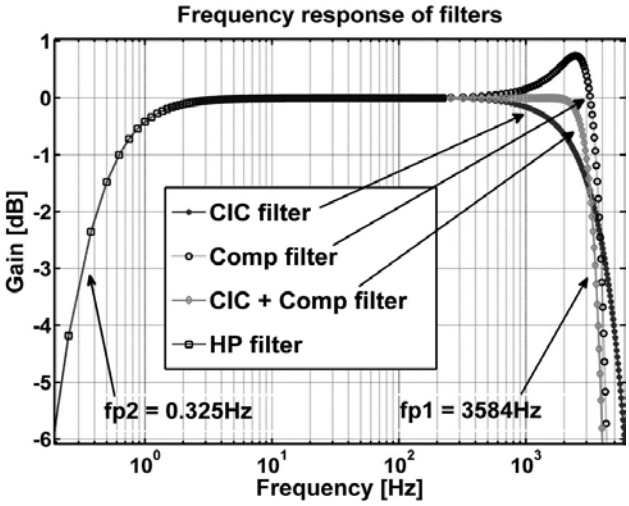

Fig. 6: Frequency response of all digital filters ($f_{clk}=2^{22}$ Hz)

5. RMS calculation, average RMS value and standard deviation

In this section the fundamental equations are presented that relate the FFT spectrum with the RMS result. Equation defines the calculation of RMS value:

$$V_{rms}=\sqrt{\frac{1}{n}\cdot\sum_{0}^{n}x^{2}(iT)} \tag{4}$$

where the meanings of the symbols are as follows: Vrms = RMS value; x(iT) is the sample of the signal after digital filtering; n is the number of samples and is defined with "time" period of input signal divided by the sampling period ($n=T_{signal}/T_{sampling}$).

To calculate the average Vrms value and standard deviation it is necessary to calculate first a series of Vrms values (Vrms(i); i=1,2,…,N).

$$\overline{V_{rms}} = \frac{1}{N} \cdot \sum_{i=1}^{N} V_{rms}(i) \quad (5)$$

Parameter N represents the number of Vrms values included in the calculation. The parameter N is calculated dividing the number of samples used for FFT calculations by the number of data needed for achieving RMS calculations with the desired resolution .

$$\sigma = \sqrt{\frac{1}{N-1} \cdot \sum_{i=1}^{N} \left(V_{rms}(i) - \overline{V_{rms}} \right)^2} \quad (6)$$

Standard deviation shows the variation from average RMS value.

$$V_{rms} = \sqrt{\frac{1}{n} \cdot \sum_{i=1}^{n} x^2(iT)} = \frac{1}{n} \sqrt{\sum_{i=1}^{n} |X(f)|^2} \quad (7)$$

Parseval's theorem /10/ shows the relation between time domain and frequency domain representation of RMS value calculations . The RMS value is calculated from the FFT by summing up the powers of all spectral components in a specified bandwidth. The bandwidth is defined with the digital filters at the output of the modulator according to , where fp1 is the pole frequency of the high pass filter and fp2 is the pole frequency of the combined CIC and cFIR filter (Figure 6).

$$BW = fp1 - fp2 \quad (8)$$

From a series of RMS values, an average RMS value ($\overline{Vrms}$) can be calculated. This average also equals to the sum of the power of spectral components according to Parseval's theorem . The average represents the sum of noise power, signal power and power of higher harmonic components in the specified frequency band. The standard deviation presents the statistical spread of the individual RMS values from the average RMS value. To get the relation between standard deviation and noise density, it is necessary to divide standard deviation with the square root of the bandwidth (BW) defined by the digital filters. The single RMS value is calculated from n_{RMS} samples ($n_{RMS}=T_{signal}/T_{sample}$) and has to be included in the equation that defines the relation between standard deviation and noise density .

$$V_{nd} = \frac{\sigma}{\sqrt{BW / n_{RMS}}} \quad (9)$$

$$BW = fp1 - fp2$$

6. Simulation Results

To verify the proposed methodology of the BIST a Matlab/ Simulink model was built. All blocks were modeled: digital filters, RMS function, voltage generator and 2nd order sigma delta modulator. The model of a sigma-delta modulator consists of the most important non-idealities such as: open loop gain (A0), unity gain bandwidth (GBW), slew-rate (SR), saturation (SAT), input noise density of the amplifiers, kT/C noise, etc., which significantly influences the accuracy, resolution and other parameters of the measurement channel. The results of BIST simulations using RMS calculations in time domain were compared to the FFT analysis results, some of which are presented below.

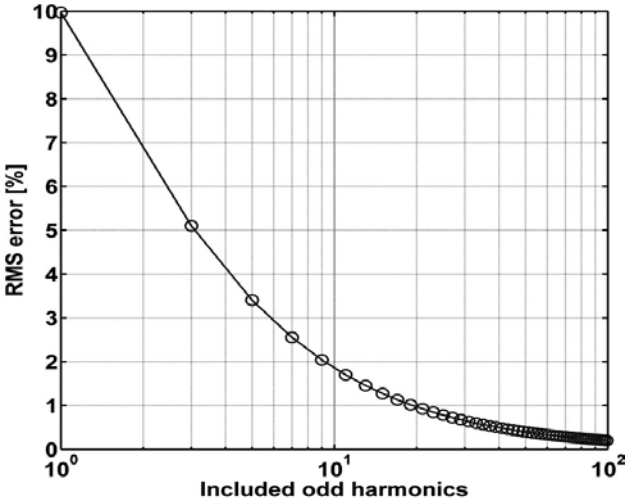

Fig. 7: RMS error in percentage depends on how many harmonics are included in ideal RMS calculation

The upper part of Figure 8 shows RMS value-error calculated by vs. open-loop gain, while the lower part of Figure 8 shows output noise density versus open-loop gain. FFT results are calculated from frequency specter and represented by a black line (marked with circles), while results obtained by RMS calculations are presented by the grey line (marked with X). In Figure 9, Figure 10, Figure 11 and Figure 12 the FFT and RMS values are shown as a function of slew-rate, unity gain bandwidth, saturation and input noise voltage of amplifier in the first integrator.

For easier comparison the average RMS values shown in the following figures are represented as a relative error. To calculate the relative error the ideal RMS value is needed. In theory, the RMS value of a square signal is equal to the amplitude of that signal. The frequency spectrum of a square wave signal is composed of fundamental and infinitive number of odd harmonic components. Digital filters attenuate HF components, so the correction must be included in the calculation of the ideal RMS value. Figure 7 shows the RMS error dependent on the number of odd harmonics included in the calculation.

The digital filters pass-through only 15 odd harmonic components of the square wave signal. Because of this filtering effect the ideal RMS value must be corrected (reduced) by 0.6%. The relative RMS error is calculated using .

$$RMSvalueerror = \frac{[IdealRMS - 0.6\%] - \overline{V_{RMS}}}{[IdealRMS - 0.6\%]} \cdot 100 \quad (10)$$

Figure 8 shows relative RMS error (top figure) and noise density (bottom figure) as a function of an open-loop gain of the first modulator's amplifier calculated from the FFT analysis and RMS calculation.

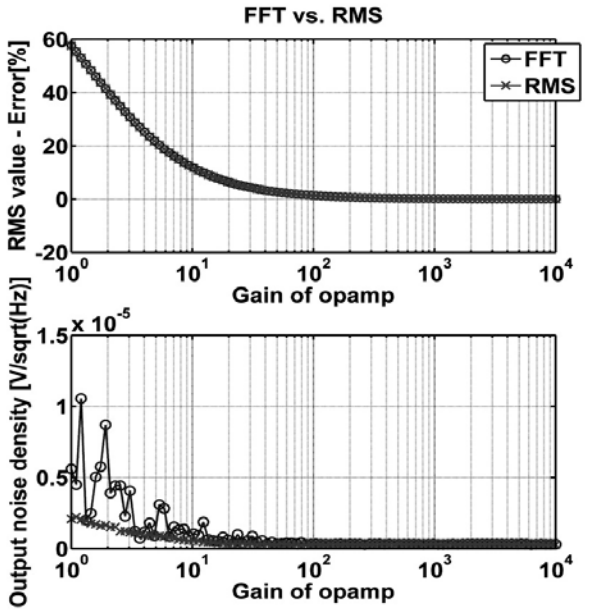

Fig. 8: RMS error and noise density of RMS as a function of open-loop gain (o : FFT results, x: RMS results)

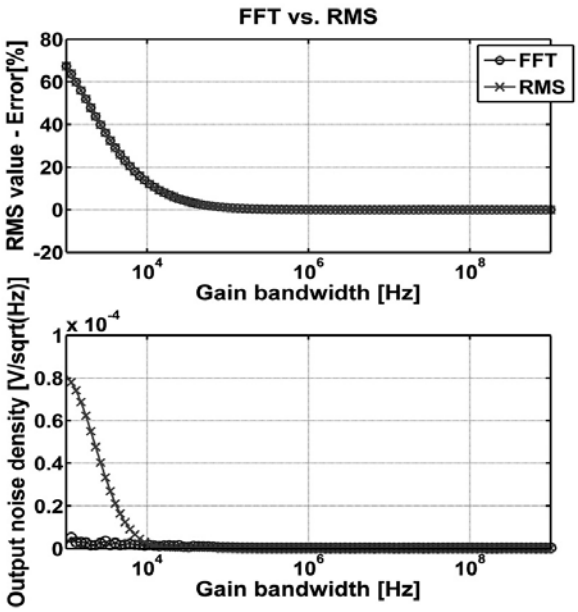

Fig. 10: RMS error and standard deviation of RMS as a function of unity gain bandwidth (o : FFT results, x: RMS results)

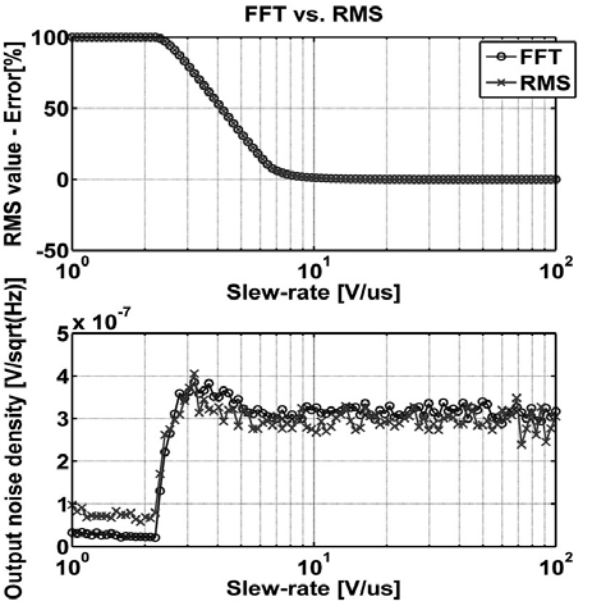

Fig. 9: RMS deviation and RMS noise density FFT as a function of slew-rate (o : FFT results, x: RMS results)

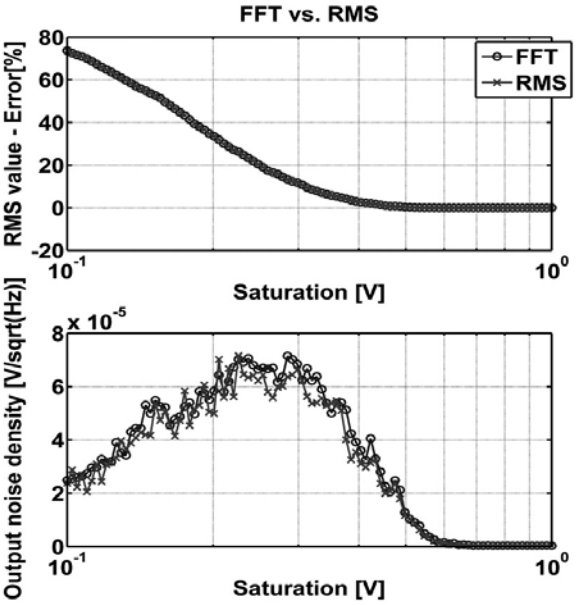

Fig. 11: RMS error and standard deviation of RMS value as a function of saturation region of the output of amplifier (o : FFT results, x: RMS results)

Comparison of the RMS error and noise density of the RMS value as a function of slew-rate is shown in Figure 9. In case that the first amplifier's slew-rate is small, the higher harmonics have big influence to the signal power, which can be seen from the RMS value.

The mismatch between FFT and RMS calculation results is present only for noise density calculations of standard deviation. The main reason for this is a small average RMS value, while standard deviation remains the same.

At maximum input signal the distortions may increase due to the non-linearity of the amplifier. Figure 11 shows the RMS error and the standard deviation of the RMS as a function of saturation limits of the first modulator's amplifier.

Changing the input noise density of the first amplifier does not influence the RMS value but only the output noise density (Figure 12).

In last example the simulation of a real BIST function is presented. In Figure 13 the response at the RMS output

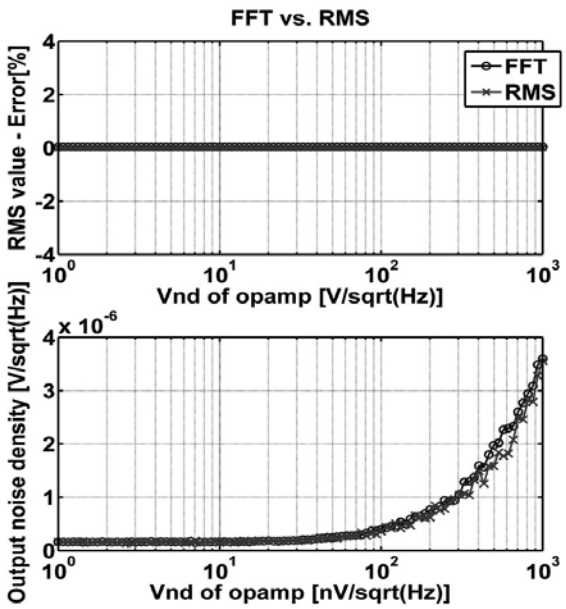

Fig. 12: RMS error and standard deviation of RMS as a function of input noise voltage of the first amplifier of the modulator (o : FFT results, x: RMS results)

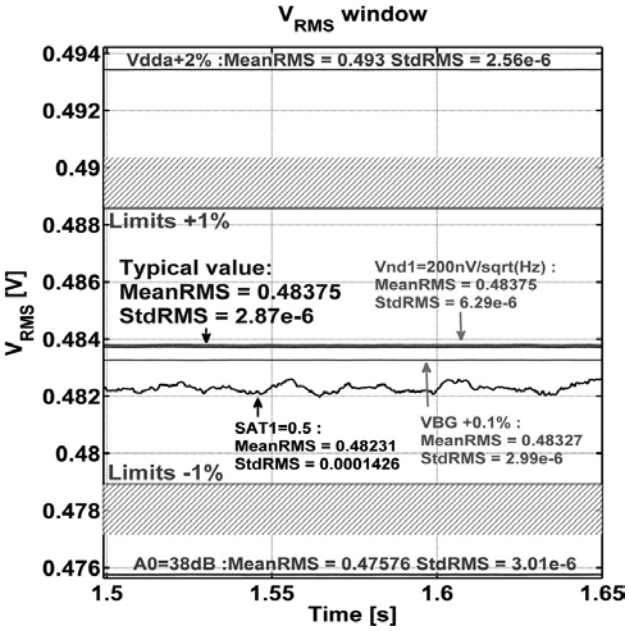

Fig. 13: RMS voltage from system level simulations at different parameters

block is presented together with accuracy limits. Different simulation results are included with different parameters deviated from their nominal values. The response is plotted together with accuracy limits. First, simulation results with typical parameters are shown and from this data the ±1% limits are set. In following simulations, the parameters like supply voltage (Vdda), reference voltage (VBG), open-loop gain (A0), saturation level (SAT1) and input noise voltage (Vnd1) were changed. The effects of these changes were monitored through average RMS value and standard deviation of RMS values and are all presented in Figure 13. If the supply voltage changes by 2% the average RMS value falls out of the desired specification. The same happens when the open-loop gain of the first amplifier decreases below 38 dB. By increasing the input noise voltage of the first amplifier, the average RMS value is the same as with typical parameters but standard deviation drastically increases. This parameter will not have a considerable effect on the accuracy because the data in the watt-hour meter are averaged over a long periods of time. The simulation results prove that most of the changes (like for example the change of reference voltage, saturation levels, slew-rates etc.) can be easily detected.

7. Conclusion

In this work an efficient BIST for a high precision electronic watt-hour meter was proposed. Using a Matlab model and system level simulations we prove that the use of a built-in RMS function gives comparable results to the FFT analysis. This method has many benefits: no testing equipment is required, testing time is reduced and it is possible to test the meter in the field during normal operation. Since new electronic watt-hour meters will have a built-in communication circuitry; so in addition to periodical test, they can also be tested in the field on demand by the distributing company.

Acknowledgments

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References

/1/ Uroš Bizjak, Drago Strle, "IEC 0.5 electronic watt-hour meter implemented with first-order sigma-delta converters", AEU – International Journal of Electronics and Communications, Volume 59, Issue 8, pp. 447-453, Dec 2005.

/2/ M. F. Toner and Gordon W. Roberts, "A BIST Scheme for an SNR Test of a Sigma-Delta ADC", Proc. of the IEEE, Test Conference, 1993. Proceedings., International, pp. 805-814, 1993.

/3/ W. Yong-Sheng, W. Jin-Xiang, L. Feng-Chang, Y. Yi-Zheng, "ΔΣ Modulator Based On-Chip Ramp Generator for ADC BIST", 2005 WSEAS Int. Conf. on Dynamical Systems and Control, pp. 512-516, Italy 2005.

/4/ Hao-Chiao Hong, Sheng-Chuan Liang and Hong-Chin Song, "A Built-in-Self-Test Σ-Δ ADC Prototype", Journal of Electronic Testing: Theory and Applications, Volume 25 Issue 2-3, June 2009.

/5/ Chee-Kian Ong, Kwang-Ting Cheng and Wang, L.-C., "A new sigma-delta modulator architecture for testing using digital stimulus" , Circuits and Systems I: Regular Papers, IEEE Transactions on, pp. 206 – 213, 2004.

/6/ Hao-Chiao Hong, Jiun-Lang Huang, Kwang-Ting Cheng, Cheng-Wen Wu and Ding-Ming Kwai, "Practical considerations in applying Σ-Δ modulation-based analog BIST to sampled-data systems", pp. 553 – 566, 2003.

/7/ Hogenauer, Eugene. "An Economical Class of Digital Filters For Decimation and Interpolation," IEEE Transactions on Acoustics, Speech and Signal Processing, Vol. ASSP-29, pp. 155-162, April 1981.

/8/ Richard G. Lyons, "Understanding Digital Signal Processing, Second Edition", Prentice Hall PTR, March 2004.

/9/ Schreider R.,Gabor C. Themes, "Understanding Delta-Sigma Data Converters", Wiley-IEEE Press, USA, November 2004.

/10/ I. N. Bronštejn, K. A. Semendjajew, G. Musiol, H. Muhlig, "Matematični priročnik", Tehniška založba Slovenije, Ljubljana, 1997.

/11/ Rok Ribnikar, Drago Strle, "Modeling of ΣΔ Modulator Non-idealities", Proc. MIDEM, International Conference of Microelectronics, Device and Materials, vol. 42 pp. 319-324, Strunjan, 2006.

/12/ Drago Strle, "Efficient Testing of High-Resolution Σ-Δ A/D Converters", Proc. MIDEM, International Conference of Microelectronics, Device and Materials, vol. 43 pp. 183-188, Bled, 2007.

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