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AUTOMATICALLY ADJUSTABLE SUPPLY SYSTEM

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Abstract: In the context of complex integrated circuits we are often faced with the problem of supply crosstalk among different parts of the system and requirements for power supply rejection well beyond the level inherently offered by the building blocks of the system. In such cases the only solution is to integrate into the system also the supply controller(s). In case the system is supplied with defined and stable supply voltage the integration of supply regulator(s) is a straightforward task. But if the system is required to operate in a wide range of external supply voltages and if the system performance is dependant on supply voltage (what is often the case) than the supply regulator(s) design becomes a crucial point in the overall system design. The presented paper offers a solution for automatic adjustment of supply regulator(s) to the applied supply voltage. This ensures that the optimum between power supply rejection demand and the demand for as high as possible internal supply voltage is reached for any external supply voltage applied, thus greatly enhancing the overall system performance.

Avtomatsko nastavljivi napajalni sistem

Kjučne besede: regulacija napajalnega sistema, načrtovanje vodenja

Izvleček: V primeru kompleksnih integriranih vezij se pogosto srečujemo s problemom presluha med različnimi deli sistema in zahtevo po odpornosti sistema na motnje na napajanju, ki presega nivo, ki jo nudijo sestavni deli vezja. V takšnih primerih predstavlja edino uspešno pot reševanja dopolnitev sistema z notranjim regulatorjem napajanja. V primeru, ko sistem napaja stabilna in točno določena napajalna napetost, je integracija tovrstnega regulatorja relativno preprosta. Če pa se soočamo z zahtevo po delovanju sistema v zelo širokem področju napajalnih napetosti in so pri tem lastnosti vezja odvisne od napetostnega napajanja (kar običajno drži), potem ustrezno načrtovanje napajalnega regulatorja postane ključnega pomena za načrtovanje celotnega vezja. V prispevku smo predstavili rešitev, ki omogoča avtomatsko uglaševanje napajalnih regulatorjev glede na zunanje napajanje sistema. Takšna rešitev ponuja optimalni kompromis med zahtevo po učinkovitem zmanjševanju neželenih vplivov spremenljivega zunanjega napajanja in zahtevo po visokem napetostnem nivoju notranjega napajanja. Na takšen način učinkovito razširjamo možnost prilagajanja zunanjemu napajanju v zelo širokem področju in s tem tudi bistveno izboljšamo lastnosti delovanja celotnega sistema.

1. Introduction

The presented automatic supply module was developed for systems which demand supply regulators to achieve desired power supply rejection but in the same time require a maximum possible supply voltage level for best performance. A typical system of this kind is an RF transmitter, where the supply voltage level directly defines the maximum output power available (for defined antenna impedance). An RF transmitter is also a system which often needs a supply regulator to ensure adequate PSRR.

This means the supply module must find an optimum between two contradicting system requirements. The demand for high PSRR inherently requires a relatively large voltage drop across the supply regulator, thus significantly lowering the regulator output voltage which is the supply voltage for the rest of the system. This is in direct contradiction with the demand for as high supply voltage (for the rest of the system) as possible to ensure high output power.

The best solution of this conflict is supply system which sets the voltage drop across the regulator to a minimum level which still guarantees the required PSRR /1/. This implies that the supply regulator output is set to a voltage relative to the external supply voltage (regulator input voltage). Assuming that the external supply voltage is not fixed and the system is required to operate at different external supply levels, an automatic adjustment system is needed to reach an optimal voltage drop across the regulator, which offers the best compromise between the contradictory demands described above.

2. System level-solution

The system presented in Fig. 1 is typical application of the system solution described. The block diagram can be divided in two parts. The basic functions of the system are presented in the main system block. The nature of the functions in this block (for instance RF output amplifier stage) requires a supply regulator to ensure proper power supply rejection (PSRR) and as high as possible supply voltage. The rest of the block diagram in Fig. 1 are bocks associated with supply voltage regulator providing the supply voltage for the main block which ensures the optimum compromise between the demand for high PSRR and the wish for highest possible supply voltage.

The operation of supply voltage regulator system can be divided into three steps /1/. In the first step the system detects the start of operation. This can be done by observing the input signals of the system (enable, power-down and similar) and/or by observing the voltage on the input

and output of the voltage regulator. The start of operation is detected when the input voltage is settled after the initial transient. The additional condition is that also the output voltage of regulator settles, thus taking into account the impact of buffer capacitor typically connected to the voltage regulator output. When the start condition is recognized the adjustment step begins.

The adjustment phase starts with the maximum setting of the voltage regulator reference /3/. This results in the output voltage almost identical to the input voltage (minimum voltage drop on across the regulator). At the same time the control block sends a signal to the main system to put the main system in the state of maximum current consumption. This ensures that the automatic adjustment is done in the worst case situation for the supply regulator. The system waits the settling transients to finish and than measures the voltage drop across the regulator. If the voltage drop is lower than the optimum value stored in the control block the control block reduces the adjustable reference for one step thus reducing the output voltage for 100mV. The system waits again for the transient to settle and repeats the measurement of the voltage drop across the regulator. If the voltage is still lower than the optimum value another voltage reduction step is started. If the voltage drop is higher the adjustment phase is finished.

The simulation of the system operation is presented in Fig. 2 and the measurements of actual implementation are shown in Figs. 6, 7 and 8.

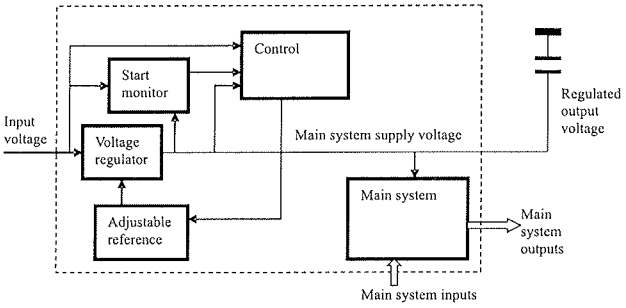

Fig. 1. Schematic system representation

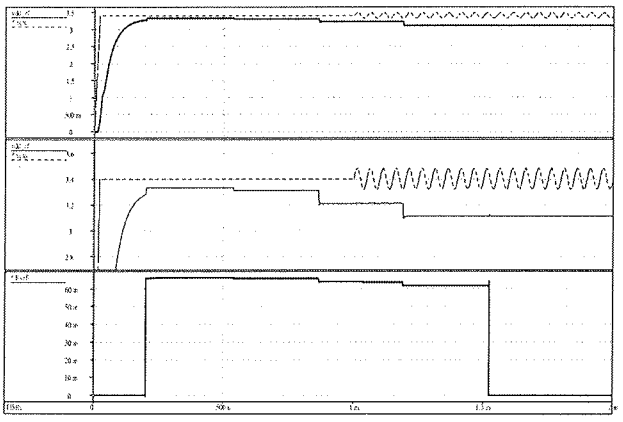

Fig. 2. Simulation results of system operation

Canvas one in Fig. 2 shows the input voltage (external supply voltage) as dashed line and the regulated output voltage as solid line. The input voltage has also an AC component (160mVpp) to high lighten the power supply rejection properties of the regulator. When the regulator input and output voltages settle (at t=200μs), start condition is recognized and the adjustment phase starts. The adjustment step was set to 100mV and a new adjustment is done every 300μs. After the third adjustment the voltage difference between the regulator input and output voltage exceeded the target value of 250mV and the adjustment phase was finished. A voltage zoom of canvas one is shown in canvas two. As described before the main system is put in state of maximum consumption during the adjustment phase. This can be seen in canvas three, presenting the current from external supply.

3. Transistor-level design

Besides the system design as described in section 2, a lot of care was devoted to the design of the supply regulator cell /2/. The demands for this cell were very high. It has to operate with minimum voltage drop (typically 200mV), it has to be stable and provide power supply rejection in a large range of load currents (from 200μA to 100μA) and it has to have adjustable output voltage in the range from 2.7V to 5V. Through the design it was assumed that the external supply blocking capacitor would be typically 2.2μF but the regulator has to operate for any supply blocking capacitor bigger than 1μF.

The dominant pole in the supply regulator loop has to be the output pole defined by the blocking capacitor to ensure fastest regulator response. The position of this pole changes drastically with the choice of blocking capacitor and the load current /2/. Since the second pole, which is typically the result of the gate capacitance of the output transistor (node A1), has to be placed at last an order of magnitude from the dominant pole, this implies the need to have the second pole as high as possible. The position of this pole also limits the minimum value of supply blocking capacitor. This means that the main design goal was to place the second pole as high as possible considering the allowed current budget of 200μA.

The required maximum current capability (100mA) at given minimum supply voltage and requested regulator voltage drop define the size of output transistor (M_out). So the capacitance of the node g_out (Fig. 3) is given and can not be significantly changed. The position of the second pole is thus mainly dependant on the output resistance of the electronic driving the gate of the output transistor (transistors M3 and M4). The chosen topology for the driver was trans-conductance amplifier with short channel devices to additionally reduce the output impedance. The simplified schematic is presented in Fig. 3.

The inputs **rvs1**, **rvs2** and **rvs3** in Fig. 3 are used to adjust the regulator output voltage in 100mV steps. The **Vref**

input is the 1.6V reference voltage and the **I10u** is the current input for bias current.

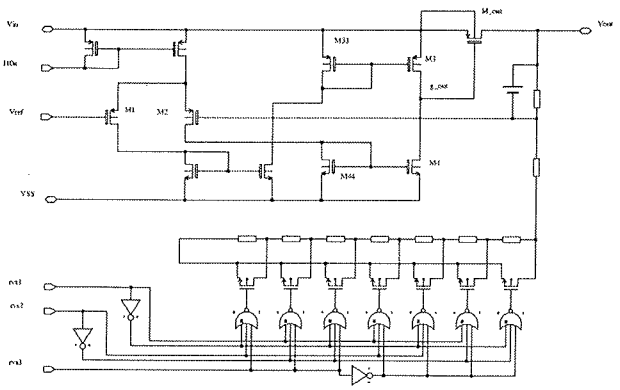

Fig. 3. The simplified schematic of the regulator cell

As discussed the main goal of optimization design is the positioning of the pole on the gate of output transistor (g_out). The optimization parameters are the current in driver transistors (M3 and M4), the length of those transistors and the current mirror ration of M3/M33 and M4/M44 pairs. The main capacitance in this node is the gate to source capacitance of the output transistor M_out. Since this capacitance is between the input voltage Vin and the node g_out it practically acts also as feed-forward system improving the regulator response to rapid changes in input voltage. The simulated response of the regulator to input voltage change (200mV step) and output current change (10mA - 60mA -1mA) is shown in Fig. 4 and 5. Fig. 4 presents a simulation response with 1μF blocking capacitor and Fig. 5 a simulation result with 100mF blocking capacitor. Canvas 1 presents the input voltage Vin, canvas 2 the output voltage Vout, canvas 3 the gate voltage of output transistor M_out (node g_out) and the bottom canvas the current from external source.

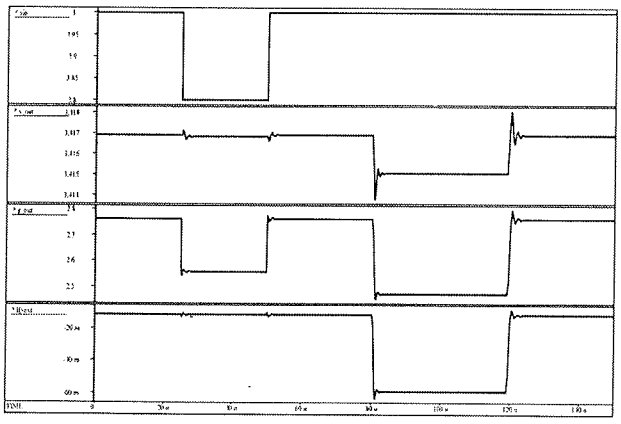

Fig. 4. Simulated reponse of regulator in the case of 1μF blocking capacitor

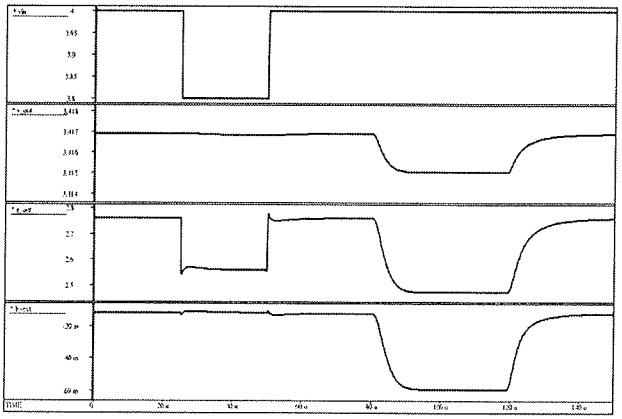

Fig. 5. Simulated response of regulator in the case of 100μF blocking capacitor

4. Implementation

The actual implementation of the described supply system was in a RF chip comprising 200mW RF output stage and receiver stage with AGC /4/. Such system needs supply voltage regulation to ensure PSRR and minimum voltage drop on the regulator to deliver the maximum possible RF output power. This was clearly an ideal case to test the automatic supply adjustment system.

The system was designed with a reasonable level of flexibility which allows the setting (using configuration register) of the desired voltage difference between the input and output voltage of the regulator.

The system performs as designed and ensures the best compromise for any supply voltage used for the system. The measurement of supply regulator system in different conditions is presented in three oscilloscope plots in Figs. 6, 7 and 8.

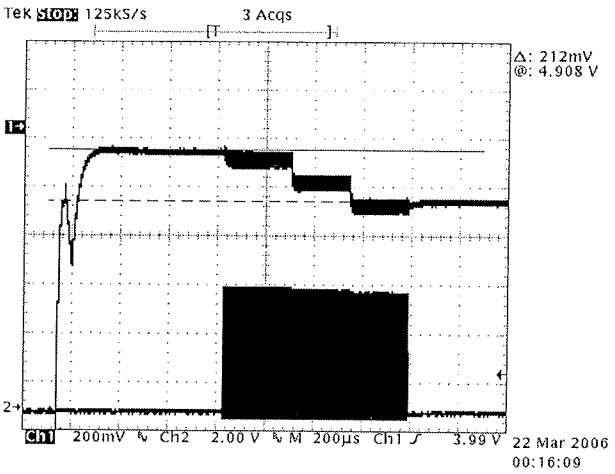

Fig. 6. System response data in the neighbourhood of the ideal conditions

Fig. 6 shows the system operation in the neighbourhood of the ideal conditions. The external supply is clean and

has negligible output resistance. Trace one shows the regulator output voltage. After switching on the input voltage the regulator output is charged to the highest level. This is slightly lower than the input voltage and in any case lower than the maximum allowed voltage for the rest of the system. During adjustment phase the regulator output voltage is lowered for 100mV every 300µs till the voltage difference exceeds the set level (200mV). During the adjustment the RF output (lower trace) is switched on since the rest of the system must be in an operation mode with the highest possible consumption.

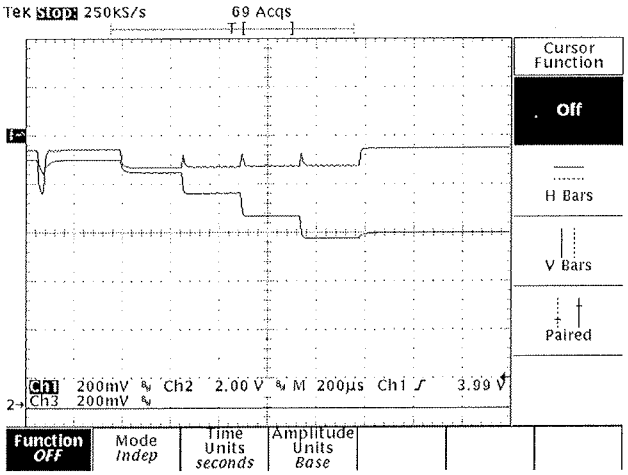

Fig. 7. System response data in case of external supply with a significant output resistance

The oscilloscope shot in Fig. 7 presents the system operation in case of external supply with a significant output resistance (2Ω). The upper trace is the external supply voltage (input voltage) and the lower trace is the regulator output voltage. At the moment the adjustment phase starts the external supply level drops (for approximately 100mV) due to increased power consumption. The automatic supply regulator system adjusts the regulator output voltage taking into account the voltage drop of input voltage in case of highest possible current consumption of the system. A spike seen on the input voltage at each lowering of output voltage results from the reduced current consumption as the system consumption current is supplied from the output buffer capacitor during the transient.

In Fig. 8 the external supply has 2 Ω output resistance and is polluted with 80mVpp 20kHz sine-wave signal. Again the input voltage is the upper trace and the output voltage is the lower trace. We can see the starting point of adjustment phase when the input voltage drops for 100mV as on Figs. 4 and 5. Each adjustment step lowering the output voltage improves the rejection of AC signal in the regulator output signal. It clearly demonstrates the conflict of the demands for high PSRR and low voltage drop across the regulator. This measurement is a good example how the described system searches and finds the optimum compromise between the two conflicting demands.

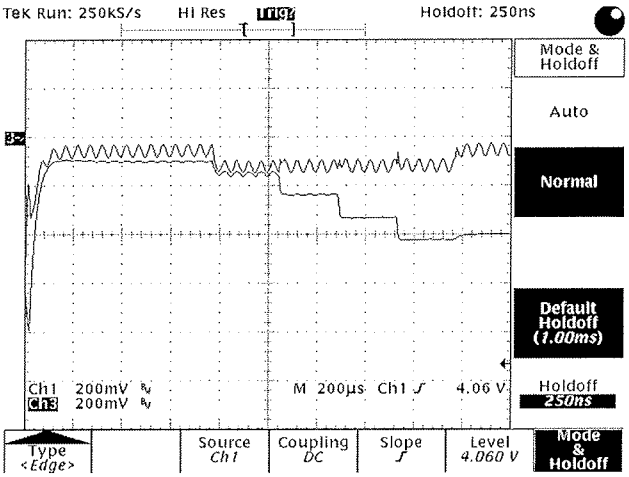

Fig. 8. System response data in case of external supply with 2 Ω output resistance and polluted with sine-wave signal

5. Conclusion

During the design of integrated medium power RF output stages we were faced with the problem how to ensure required PSRR in case of wide range of possible supply voltages without sacrificing more of the supply voltage available as it is absolutely necessary. The presented solution is a system which automatically searches for the best compromise between the conflicting requirements of high PSRR and low drop of supply regulator system.

The system was implemented as a vital part of a RF integrated system and was proved to operate as desired, thus providing intelligent supply system for RF power application. The solution is also patent pending.

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