POWER ELECTRONIC BUILDING BLOCKS: A SURVEY

Žarko ČUČEJ

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

Key words: power electronics, PEBB, Power Electronics Building Blocks, development results, circuit topologies, electronic circuits, THD, Total Harmonic Distortion, PWM switches, Pulse Width Modulation switches, ZVT, Zero-Voltage Transition, ZCT, Zero-Current Transition, ZVS, Zero-Voltage Switching, ZCS, Zero-Current Switching, ARCP, Auxiliary Resonant Commutated Pole, inverters, converters, LMARC, Load Modulated Auxiliary Resonant Current, MCT, Metal-oxide silicon Controlled Thyristors, HM controllers, Hardware Manager controllers, AM controllers, Application Manager controllers, CI, Coordinated Interconnect, control, thermal losses

Abstract: The PEBB program, sponsored by the Office of Naval Research, seeks to develop a general-purpose power controller capable of performing numerous electrical power conversion functions simply through software reconfiguration.

Gradniki močnostne elektronike: pregled

Ključne besede: elektronika močnostna, PEBB gradniki elektronike močnostne, rezultati razvoja, topologije vezij, vezja elektronska, THD popačenje harmonsko totalno, PWM stikala z modulacijo širine impulzov, ZVT prehod pri napetosti nič, ZCT prehod pri toku nič, ZVS preklapljanje pri napetosti nič, ZCS preklapljanje pri toku nič, ARCP pol komutirani z resonanco pomožno, inverterji, pretvorniki, LMARC tok pomožni resonančni moduliran z bremenom, MCT MOS kovina-oksid silicij tiristorji krmiljeni, HM krmilniki kot vodje hardware-ski, AM krmilniki kot vodje aplikacijski, CI povezave medsebojne koordinirane, krmiljenje, izgube termične

Povzetek: V članku je podan kratek pregled rezultatov razvoja gradnikov močnostne elektronike, ki ga je inicializiral Urad za raziskave pri ameriški vojni mornarici (ONR: Office of Naval Research). Za cilj so si zastavili razvoj pretvornikov, ki jih zgradimo s preprosto, standardizirano povezavo standardnih elementov podobni gradnji z lego kockami, katerih funkcionalnost določimo z vpisom ustreznega algoritma delovanja. Iniciativa sicer zrcali potrebe in načrte ameriške vojne mornarice, kot je program »more electric ship« in drugi, vendar je njegov cilj mnogo širši: razviti novo filozofijo načrtovanja, razvoja, gradnje, proizvodnje in uporabe naprav močnostne elektronike, kot tudi distribucije električne energije v raznih avtonomnih sistemih. Program sicer še ni sprožil serijske proizvodnje gradnikov, ne vzpostavil novih standardov na področju močnostne elektronike, je pa že prinesel nove elemente kot so MOS krmiljeni tiristorji, nova paradigma v krmiljenju močnostnih stikal, ki vključuje tudi digitalni komunikacijski sistem, pametne senzorje in digitalno obdelavo signalov.

1. Introduction

The power building block (PEBB), initiated by Office of Naval Research (ONR), is promising enabling technology which will promote future electrical power systems. A PEBB is concept of building a larger power processing system from relatively small number of standardized units which have high degree of intelligence and control autonomy, and which are themselves built from smaller standardized units with some, but less intelligence and autonomy, which in turn also can be but by even smaller, elementary blocks and so on /1-4/. Therefore a PEBB is not some specific block, but rather a building block concept. It starts from the smallest block, i.e. smart switches, smart sensors, etc, which are used to build smart power processing units, e.g. inverters, rectifiers, motor drivers, solid-state circuits breakers, etc. These power-processing units are combined to provide more complex function, or a single function but with higher power rating than each individual unit.

At any level, a PEBB module has form depicted in Fig. 1. This concept makes difference to classical design of power processing devices in following:

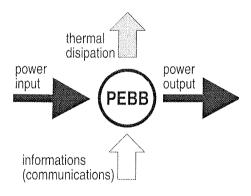


Fig. 1: PEBB module interfaces

- 1. Every, even the simplest module has some intelligence and includes some communications capability,
- Physical properties at each of the four interfaces (connectors, screws, surfaces, etc) are standardized for each PEBB power level. Planed are three power ranges:
 - a. Low Power 10 kW to 100 kW
 - b. Medium Power 100 kW to 500 kW
 - c. High Power 500 kW to 10 MW
- Electrical properties at each interface should be standardized.
- Compatibility of all modules that connect at the some interface is guaranteed a priory.

The initial intent of the PEBB program was to development or fosters the development of a family of power electronic modules that can be used in 80% of the power conversion and power control applications in the commercial and military world. The technical goals for the PEBB were as follows:

- Size and packaging, for example, a 250 kW singlephase PEBB module should be fit in a volume roughly the size of a shoebox without the output filter circuits but with built-in provision for thermal management.
- 2. Power conversion efficiency greater than 98%.
- Output power quality less than 5% Total Harmonic Distortion (THD).
- 4. Electromagnetic Interference (EMI) levels below those specified in Mil Std 46.

It is the objective of the PEBB program to promote innovative development of a family of power electronic devices that satisfy the PEBB goals. Furthermore, this program likes to stimulate and support competing ideas in order to advance the state of the art and produce the best possible PEBB modules /5,6/. Of course, main goal is to have PEBB modules produced in the US by US manufacturers.

2. Topology

For electric power conversion a different kind of switching converters are employed. Their switches are implemented by one of three basic switch topologies (Fig. 2), which together with switching control must guarantee the elementary safety operation: no shorted voltage source, no open current source. Analysis of power converters topologies

show, that medium and high power converters are built up from different interconnected half-bridges (Fig. 3). Further, the control of switches in half bridge is very tied: if one is in on state, the other one has to be in off state.

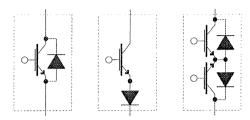


Fig. 2: Basic switches topologies. From left to right: voltage unidirectional, current unidirectional and bi-directional.

2.1. Impact of soft switching techniques

Reduction of thermal dissipation is very important issue in integration of PEBB elements into compact peace of hardware. Meanwhile the contribution of static losses is reducible only by inventing a new semiconductor switches, the switching losses can be reduced also with appropriate modulation techniques as well as with use of soft switching. So far, many soft switching topologies have been proposed to reduce the switching loss and improve the performance of converters. All have been evolved from resonant converters, quasi-resonant converters, multi-resonant converters, soft switching PWM converters including zerovoltage transition (ZVT) and zero-current transition (ZCT). They can be classified be classified into two categories: zero voltage switching (ZVS) and zero-current switching

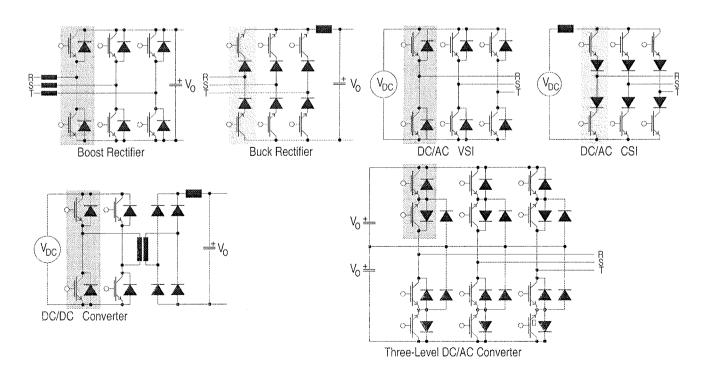


Fig. 3: Identification of a PEBB Switching cell: The commonality in the power converters is presented as the shaded block

(ZCS). ZVS reduces the switch turn-on loss by forcing the switch voltage to zero prior to its current flowing, while ZCS reduces the turn-off loss by forcing the switch current to zero before its collector-emitter voltage increases from zero to turn-off static value. For medium to high power applications, ZVT and ZCT are more suitable than other soft switching techniques, since they combine the advantages of PWM control (i.e. minimum switch static voltage/current dynamic and minimum circulating energy), and the advantages of soft switching techniques, i.e. low switching loss and low dynamic transition.

2.1.1. ARCP inverter

The ARCP (Auxiliary Resonant Commutated Pole) inverter belongs to ZVS family of soft switching inverters /6/. In its topology (Fig. 4), the voltage across each phase switch (S_1 and S_2) is driven to zero just prior to its turn on. This is accomplished by generating a resonant current pulse that drives the voltage across the switch to zero. The resonant pulse is formed when auxiliary switch (AC) consisting from switches A_1 or A_2 is turned on just prior to turning off a phase switch.

A detailed description of ARCP operation can be found in reference /7/. Briefly its operation can be described as follows. When the AC switch is gated on, a current begins to rise linearly through the resonant inductor L_R in the conducting phase switch. When the phase switch is turned off, the current resonates based on the resonant component values and then falls back to zero. The peak resonant current depends on the following (see Fig. 6):

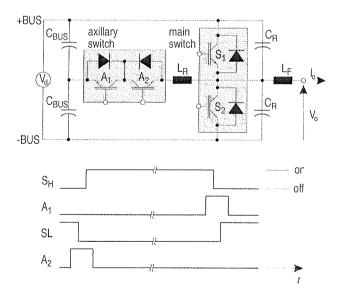


Fig. 4: ARCP schematic and switching timing

- Length of time that both the AC and the phase switch are turn-on simultaneously (overlap time)
- Input bus voltage
- Resonant component values (L_R and C_R)

For AC switches in ARCP inverters the MCT (MOS Controlled Thyristors) have been developed and provided under the ONR PEBB development program. These devices can withstand high dv/dt and di/dt stresses making them ideal candidates for use as AC in the ARCP topology.

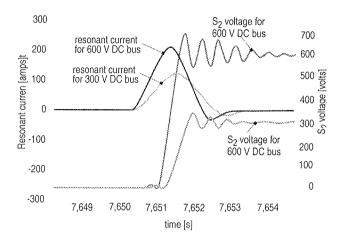


Fig. 5: ARCP Resonant Transitions.

Efficiency of ARCP inverters strongly depends on resonant pulse control. Minimization of resonant energy required for soft switching can be achieved by introducing of a smart control with self-tuning the overlap time to the actual input DC bus voltage and actual load current. Example of smart control is LMARC (Load Modulated Auxiliary Resonant Current) control algorithm reported in reference /6/. LMARC determines overlap time according to the instantaneous load currents. To insure zero voltage transitions the adequate safety margins, i.e. more resonant energy than what is theoretically needed is maintained. LMARC also considers the facts that the magnitude and direction of the instantaneous load current flowing through a main switch or diode can help or hindrance of resonant transitions.

2.1.2. ZCT converters

A ZCT PEBB can be regarded as the combination of two soft switching cells. One of them is shown within the shaded area in Fig. 6. The relationship between the main switch and its corresponding auxiliary switch in one PEBB topology is diagonal. This means the timing control of A_L is related to S_H . On the other hand, A_H is related to S_L . The key waveforms and the control timings are shown in Fig. 7, analysis of improved ZCT can be found for example in /8,9/. Let be emphases, that ZCT only help the switching transition, so the power converters with ZCT operates according to PWM rather than switching transition. So the controller design is almost the same as at the hard switching converters.

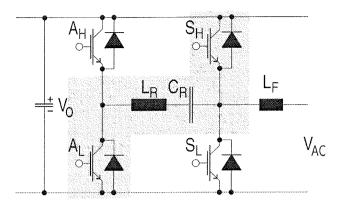


Fig. 6: Topology of one ZCT PEBB power stage for boost rectifier

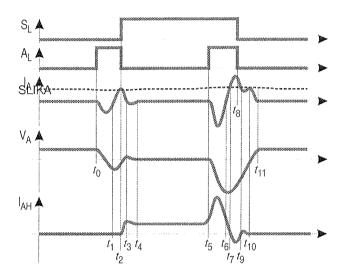


Fig. 7: Operation waveforms for the improved ZCT

3. Control and communication isues

The control of PEBB is divided into two parts:

- 1. Controller of power stage of PEBB, which was named Hardware Manager (HM), and
- 2. Controller of PEBB's applications, which was named *Application Manager* (AM).

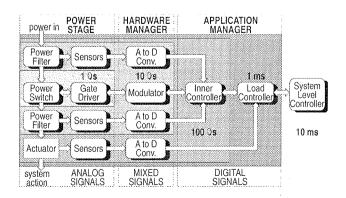


Fig. 8: PEBB module interfaces

In the beginning to HM belongs pulse-width modulator and analog-to-digital converters preparing data for AM (Fig. 8). For AM has been proposed cascade controller structure. The concerns of inner loop are electric variables like input/output voltages and currents, the outer loops concern are load variables, for example motor torque and angular velocity. This solution needs numerous noise sensitive signal lines between HM and elements of PEBB. This was eliminated by further development of PEBB concepts where in PEBB control was introduced smart sensors generating data instead of signals and smart gate drivers capable converting digital commands into adequate drive signals. In this concept modulator and AM vas merged into universal controller (Fig. 9), HM and AM communicate over fast serial bus interface (Fig. 10).

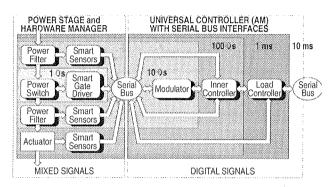


FIG. 9: Universal controller with serial bus interfaces

Serial communication between HM and AM has specifics not found in existed industrial communication systems. As it is on one hand very simple and mostly performs cyclic traffics, on another hand it had to be very fast, has very low synchronization jitter and should be reliable.

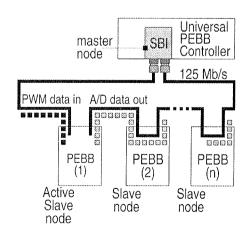


Fig. 10: Inter PEBB and UPC communication

4. Interconnections

Interconnection of a PEBB's components into compact device is one of a major issue of PEBB initiative. There arise lot of problems because only in rare cases it is possi-

ble to connect one component directly to the adjacent component. The stray inductance and capacitance of the interconnection, which are often impossible to determine in advance, consequently accurately modeling of the converter is not possible. This leads to a lot of unnecessary laboratory experimentation during the interconnect development. Furthermore, components are not mechanically interchangeable, requiring sole sourcing of many components. One of solutions for above problems is proposition for a system called Coordinated Interconnect (CI) /10-11/, which by a change in component terminations philosophy can greatly improve converter design and construction. New philosophy emphases the component terminations should not govern the interconnect design, rather the interconnect design should govern the component terminations. Proposed CI eliminates the wiring harness and busses typical of present-day converters. The concept of CI is to integrate a section of laminated bus, or at least a bus-like structure into each component. The bus is terminated with a bus edge connector which mates directly to the bus edge connector of the adjoining component. Consequently all interconnect stray elements are included with the components and are characterized as part of the component data sheets. Therefore modeling of the converter prior to construction is greatly simplified. Furthermore, components of various types are mechanically interchangeable with each other. Finally the concept of CI allows replacement of a single component without disturbing other components or connections.

Designing CI the selection of the number of layers is a key decision. Since CI should be carried throughout the converter, both the ac and dc sections of the converter should use CI. In the dc section buses often require a "+" layer, a "-" layer, and a midpoint or "0" layer. Coincidentally, the ac section of a three-phase converter requires three layers for phases *a*, *b*, and *c*. Therefore was proposed a three-layer system, which could easily be reduced to a two-layer or enhanced to four or more layers. As shown in Fig. 11, a vertical tab terminates each of the three horizontal bus layers. Each tab occupies a width W and is isolated from its neighbor by separation S. The bus thickness determines the tabthickness T. The bus thickness depends on com-

ponent design and can be different for different components. All tabs must extend above the baseplate by a uniform elevation E. Therefore; the tab height H actually can vary depending on the distance between the bus layers and the baseplate. The contact area between the two tabs is the product of W and H. Three-tab bus edge connector has not centerline axis symmetry. Lack of symmetry introduces in the converter layout certain constraints like orientation in component placing. The symmetry is achievable by five-tab bus edge connector (Fig. 12), but requires five connections between adjacent components. Beside of increased it has a total of 4S separation between tabs for the three-tab design. The additional separation reduces the contact area and could be a limiting factor if S is large.

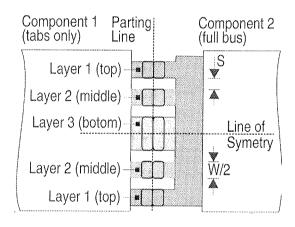
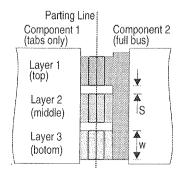
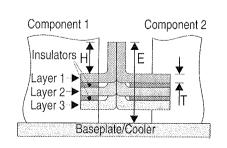


Fig. 12: Five-tab bus edge connector for three-layer bus.

Many different techniques could be used to fasten the tabs to each other. Fig. 13 shows three example methods. Traditional bolt, washers, and nut (Fig. 13a) are not convenient for mounting, more convenient is use of a spring steel clip, which can be inserted from above with minimum clearance on either side (Fig. 13b). Similarly is with the screwdriven wedge (Fig. 13c). By it is possible to connect multiple tabs simultaneously. Those connections can be made and unmade. Permanent connections such as crimping are also easily envisioned.





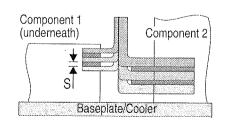


Fig. 11: Three-tab bus edge connector for three-layer bus: (a) top view, (b) edge view with coplanar bus layers, (c) alternate edge view with non-coplanar bus layers and buses of differing thickness.



Fig. 13: Methods to fasten tabs of bus edge connector.

For wide acceptance of CI sine qua non condition is standardization of CI. At least should be standardized measures E, S, H_{min}, W and position of holes in edge connectors. It can be expected that those measurements will be grouped in power classes like PEBB's. Since no currently available components use CI, it would be developed in phases with various components making the transition when possible. Advanced technology components would use CI as an integral part of the component design, for others adapters would be used to make the transition however. Example of it for electrolytic capacitor is illustrated in Fig. 14.

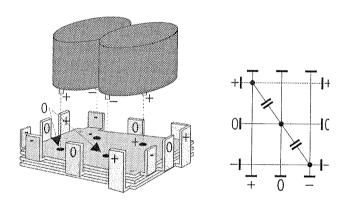


Fig. 14: Three layer bus adapter for electrolytic capacitor. Terminals allow the capacitor to connect to either "+" and "0" layers or "-" and "0" layers.

5. Packaging Issues from a Thermal Perspective

Integration of PEBB's components, determined by circuit topology, into compact device depends very much on voltage, current and the amount of waste heat generated. By CI the problems with voltage and currents influence on package is seems to be efficiently solved, but for wasted heat is likely that the common methods of cooling have already reached their limit. To improve performance the waste heat has to be taken out more efficiently. The sketches below outline the various topologies that can be considered for packaging a power electronic switch. Each of the following drawings is laid out in the same basic manner to emphasize the similarities and differences of the topology. Each is shown with a generic heat sink (heat exchanger, fluid link and final heat exchanger).

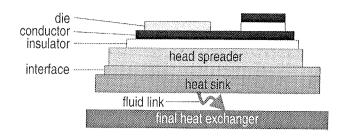


Fig. 15: Conventional heat sink

Fig. 3.1 shows a conventional heat sink topology. It is the most common because of its flexibility. With this topology, the worst is the field interface (on the sketch assigned as interface). Even under the best of circumstances it acts as a thermal barrier. Because of material performance limitations and manufacturing techniques the overall package has a lot of layers in the 'stack', each interface providing a thermo-mechanical problem.

The attached and integral heat sink topology (Fig. 16) are compromise that has been tried a number of times for both single and double side-cooled packages. At integral heat sink the insulator is part of the mechanical structure and overtake the heat spreader functionality, so minimal thermal path from die to heat exchanger seems to make this a near ideal heat management system. Pool and flow boiling as well as spray and impingement using Fluorocarbons all appear to promise very real performance boosts and would be worth development. Therefore the integral heat sink topology is a basis for the temporary phases of PEBB program.

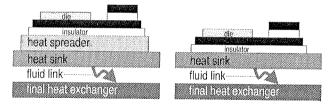


Fig. 16: Attached (left), and integral (right) heat sink.

The double side cooled topologies are complex layout (Fig. 17). They have similar properties as one side cooled counterparts, but with important benefits, that in comparison to them have halved thermal resistance. Unfortunately, those topologies require a new way of connecting the package to the outside world. Fundamental changes in package form, power interface and control connection is required. In thermal sense the best possible thermal performance is feasible by integral liquid cooling (Fig. 18) where the heat exchange liquid is right at the die. Further advantage is that the package does not need to use the expensive ceramics and engineered metals used in conventional high performance module designs. The package can be designed as one large heat exchanger operating at a high temperature. It can be cooled efficiently with forced air. However the performance and size advantages seem to outweigh the need to use special liquids. For future high-

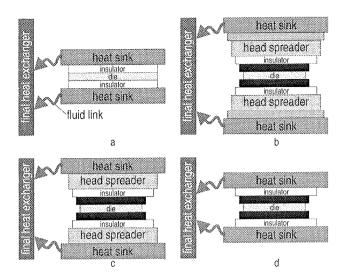


Fig. 17: Double side cooled packages, a: Hockey puck or press pack, b: conventional, c: attached heat sink), d: integral heat sink.

power-density PEBB's this certainly seems to be a promising approach.

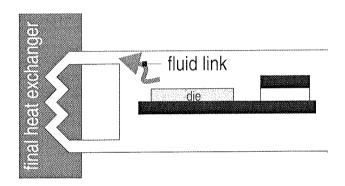


Fig. 18: Integral liquid cooling

Chart in Fig. 19 shows an analysis of efficiency of different cooling systems. In analysis it is assumed that all layers

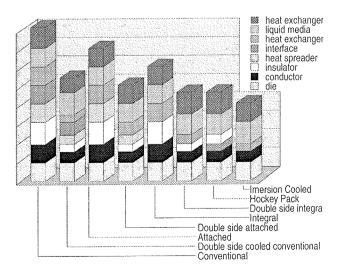


Fig. 19: Comparative Thermal Resistance

have approximately equal thermal resistances. Each single layer in package has full height; doubled layers are half height since they would approximately halve the thermal resistance. This illustration has a lot of simplifying assumptions but hopefully it shows why the 'advanced' module designs are of such interest. This analysis probably understates the performance gains of the more 'advanced' packaging styles. The pivot in packing development is development of packaging materials. For them are many performance parameters of importance, however the primary areas of interest to the PEBB program are thermal issues relating to coefficients, reliability and performance. For reliability the primary driving force is the mismatch of Thermal Coefficients of Expansion (TCE) between layers in a packaging stack. Thermal Conductivity (TC) measured in W/ mK reflects the thermal performance/power dissipation. A list of packaging electronic materials with their TCE and TC considering in PEBB program is in Table 1.

Table 1: Electronic materials

	TCE	TC [W/mK]	Туре
Thermal grease		1	ı
Diamond	1	>2300	I
Si ₃ N ₄	2	270	1
BN	4	600	1
CuGrpht MMC	~4	~250	С
AIN	4	180	l
Si	4	160	S
SiC	4	270	S/I
CuMoCu	7	200	С
Al ₂ O ₃	7	23	1
BeO	8	240	1
Cu	18	395	С
Al	24	205	С
Circuit Board	130	0,24	1
AISIC	180	180	С
Solder (Sn/Pb)	210	36	C/A
Thermal Epoxies	<700	1	I/A

Type codes: I – Insulator, C: Conductor; S – Semiconductor, A – Attach

All numbers are approximate

Conductors have to be directly bonded to the die at least on one face. Electrical conductivity is a prime parameter but because of the close proximity to the die, their TCE needs to be as closely matched as possible. Electrical insulators are relatively good thermal conductors, but the less expensive ones are generally poor performers in this area. Most ceramics insulators have relatively small TCE's while organics have high TCE's. The cheap organic insulators can be inexpensively formed into complex shapes while

the ceramics are all expensive to form into anything beside flat plates.

Attachment materials are solders and organics. The most common solders are tin/lead alloys and although other mixtures are used fairly frequently, they have somewhat similar characteristics. Organic attachment materials are electrical and thermal insulators; though they can be 'loaded' with other materials that can modify either or both the electrical and thermal properties. Organics can be made to adhere to just about any surface and are generally processed at low temperatures that give them a great deal of process flexibility.

Heat spreaders are the relatively thick, flat base-plates of power modules that provide a stable base on which the components are mounted in conventional modules. They are generally made of copper, provide a good path for heat dissipation, and form a "thermal capacitor" to absorb heat spikes and protect the device when a short-term overload situation occurs. Heat sink/heat exchangers are usually just extruded or machined aluminum. The term heat exchanger is generally used for active devices where hot a low temperature and usually different fluid flowing on the other side cool flowing fluid on one side of an interface. Most heat exchangers are made of aluminum.

6. Conclusions

This paper demonstrates the progression in development of PEBB concept and philosophy. From past research and development can be concluded that PEBB will not have unique topology. Regard to application the hard switch and ZVT or ZVT soft switch versions will be available.

The control of power electronics in future will be split into part integrated into PEBB, which in collaboration with smart sensors and gate drivers will control PEBB behavior and will be through fast serial digital communication linked with application control. This communication will have the same importance as have I²C in connections of chips.

The power electronics would benefit enormously if the industry of elements used in power electronics will accept system of Coordinated Interconnect just as the computer and other digital industries benefited from the dual inline package (DIP) and subsequent surface mount devices. But that this will happen many important challenges must be met

Thermal aspects of PEBB's packaging give insight in problems of integrating PEBB into compact device. From brief overview of packing technologies can be concluded, that integral heat sink technology is basis of temporary phases of PEBB program. In future, when high temperature devices like SiC elements will be available at reasonable cost, it seems that integral liquid cooling will prevail. For this cooling a long way of searching for materials with appropriate TCE is still to be passed.

7. References

- /1/ D. Boroyevich: Some control, communications, and modeling Issues for PEBB based power distribution systems. White paper as part of the Control and intelligence systems control of ONR PEBB control technology workshop, 1995
- /2/ K. Drew, "PEBB technology development and cost assessments benchmark as of October 9, 1998, ONR, code 36 (http://pebb.onr.navy.mil)
- /3/ G. S. Thaudi: Modeling, control and stability analysis of a PEBB based DC distribution power system. M.Sc. thesis, VPI&SU Blacksburg, Va., 1997
- 74/ T. Ericson, A. Tucker, D. Hamilton, G. Campisi, C. Whitcomb, J. Borraccini, W. Jacobsen: Standardized power switch system modules (power Electronics Building Blocks). Power systems world '97, 1997 (http://pebb.onr.navy.mil)
- /5/ J. Borraccini, W. Ruby, T. Duong, D. Cochran, E. Roth, D. McLaughlin, T. Ericsen: Demonstration of Power Electronic Building Block (PEBB1) Function, and Plans for PEBB2 and PEBB3. Report (http://pebb.onr.navy.mil).
- /6/ W. Ruby, R. Cooley, J. Borraccini, M. Cannell, J. Sullivan, J. Baker, R. Sigethy, G. McKibben: Power Electronic Building Block design and hardware demonstrator results from December 1996 through May 1998. (http://pebb.onr.navy.mil)
- /7/ R. W. DeDonker: "Resonant Pole Converters". EPE-93, Ch. 4, p 4-1 through 4-44, 1993
- /8/ J. Mayer: Analysis of Zero-Current Switching Topologies and Strategies for the Power Electronic Building Block. Final Technical Report for Naval Surface Warfare Center, February 1998
- /9/ A. W. Kelley, M. Harris, D. Hartzell, and D. Darcy, "Coordi-nated Interconnect: A Philosophical Change in the Design and Construction of Power Electronic Converters, 33rd IAS Annual Meeting, 1998, St. Louis, Missouri, USA, pp. 1105-1110.
- /10/ A. Kelley, M. Harris, J. Cavaroc, M. Jones, R. Linkous, D. Hartzell, D. Darcy: "Bus connector for coordinated interconnect laboratory measurement and finite element simulation" APEC, Dallas, Texas, 1999, pp. 325-331.
- /11/ W. A. Stinnett: Thermal management of power electronic building blocks. M.Sc, thesis, VPI&SU Blacksburg, Va., USA, 1999.
- /12/ J. Borraccini, W. Ruby, R. Cooly, M. Cannel: Calculation of power density of PEBB 1.5 based ARCP electrical power converter. 1998 (http://pebb.onr.navy.mil).
- /13/ P. N. Harrison, R. W. Garman, "PEBB Thermal Baseline Study Test Plan," A&T Engineering Technologies, VECTOR Research Division (July 8, 1998).
- /14/ P. N. Harrison, R. W. Garman, "PEBB Thermal Management Final Report," A&T Engineering Technologies, VECTOR Research Division (May 1999).
- /15/ Jia Wu, Heping Dai, Kung Xing, Fred C. Lee and Dushan Boroyevich: Implementation of a ZCT soft switching technique in a 100 kW PEBB based Three-phase PFC rectifier, IEEE conference PESC'99, reprinted in 1999 Annual Power electronic seminar, Virginia Tech, Blacksburg, USA

Žarko ČUČEJ Univerza v Mariboru Fakulteta za elektrotehniko, računalništvo in informatiko Smetanova 17, 2000 Maribor-SI e-mail: zarko.cucej@uni-mb.si

Prispelo (Arrived): 24.03.01 Sprejeto (Accepted): 01.06.01