Slov Vet Res 2010; 47 (4): 149-54
UDC 621.317

Original Scientific Article

LOW NOISE SIGNAL PROCESSING FOR MEMS/NEMS BASED CHEMICAL/BIOLOGICAL SENSORS: A SYSTEM PERSPECTIVE

Drago Strle

Laboratory for Microelectronics, Faculty for Electrical Engineering, University of Ljubljana, Tržaška 25, 1000 Ljubljana, Slovenia

*Corresponding author, E-mail: drago.strle@fe.uni-lj.si

Summary: The paper presents architecture, design, modeling and implementation of low-noise signal processing electronics needed to implement high-resolution MEMS/NEMS based capacitive sensors interfaces, which can be used for chemical/biological sensor interface. Using double-mixing lock-in amplifier principle with signal processing appropriately distributed between analogue and digital circuitry, using low noise charge amplifier, low-noise programmable gain stage, several low-noise filters, 2nd order ΣΔ modulator and the DSP a very high SnR is achieved. With proposed architecture, it is possible to sense a capacitance difference smaller than 0.5aF/√Hz on a 2pF feedback capacitors with SnR (1Hz) better than 134dB. Because of achieved characteristics it is possible to use proposed interface for sensing capacitance changes of micro/nano scale based chemical and/or biological sensors with ultimate sensitivity. The circuitry is implemented in 0.350μm BCD technology and occupies approx. 2.5 mm^2. Using this electronics together with chemically modified MEMS COMB capacitive sensor the measured detection level is better than 5ppb vapor molecules in the air at room temperature.

Key words: electronic bio sensors interface; noise in bio sensor interfaces; capacitive sensor interface; lock-in-amplifier

Introduction

Many MEMS/NEMS sensors utilize capacitive based transduction mechanism to sense different physical, chemical or biological effects (1-3). Usually, the capacitance change is very small, so the signal processing electronics must be such that SnR from the sensor is not reduced considerably. In addition, temperature drift, power consumption and silicon area must all be as small as possible. The most critical blocks are: the sensor, input amplifiers and ADCs, where thermal and 1\f noise, offset, and quantization noise can degrade the performances. The quantization noise is made negligible compared to other noise sources, thus the main noise contributions are coming from the first stages of the analog signal processing blocks. Different techniques exist for the reduction of offset voltage and 1/f noise: AZ, CDS and CHP (4). In AZ and CDS the offset voltage and 1/f noise are attenuated while thermal noise is increased. CHP (chopping) is better compared to other techniques but also in this case the thermal noise increases approx. by factor of 2. The problem is the residual offset if such signal is amplified. In this work we do not use chopping, instead, sensing signals are square-waves connected directly to the sensing capacitances, so the sensor signals (capacitances) are immediately transferred around multiples of f_s, which must be above corner frequency of 1/f noise. To reduce power consumption the analog HF signal processing is used in first stages only; in later stages the signal frequency is reduced by down-mixing to f_o before the ADC. The DSP reduces signal frequency down-to the DC. In this way a special version of lock-in amplifier principle is implemented.

This paper is organized as follows. In section sensor a capacitive COMB sensor used in our experiments is presented together with estimates of required sensitivity. The architecture of proposed signal processing electronics is given section Architecture and noise together with estimated SnR and most important system level simulation results. Section Modelling and measurements deals with

Received: 30 August 2010
Accepted for publication: 17 September 2010

modeling, some additional simulation results and measurements. In Conclusions a possibilities for further improvements are presented.

Sensor

Figure 1 shows SEM micrograph of a differential COMB sensor. The sensor is connected as suggested on Figure 2. The capacitance is $C_0 = 0.5pF$ and production spread is smaller than $\varepsilon_p \leq 5\%$. Capacitor C_p is modified by appropriate molecule that is self-assembled on C_p, while C_n is unchanged. A compatible molecules in the air or in the liquid are adsorbed on the surface of C_p and its capacitance changes to C_{p1}. Assuming that the thickness of one layer of adsorbed molecules is approx. 0.1nm the capacitor change $\delta C_p = C_{p1} - C_{p0}$ can be calculated using equation (1):

$$\delta C_p = C_0 \left(1 + \frac{\varepsilon_p}{2}\right)\left[\frac{\delta}{(d-\delta)}\right] \leq 33aF \qquad (1)$$

The difference of capacitors $\Delta C = C_p - C_n$ before and after adsorption can be calculated by (2) and is carrying the information.

$$\Delta C_1 - \Delta C_0 = C_0 \cdot \varepsilon_p + \left\{C_0 \left(1 + \frac{\varepsilon_p}{2}\right)\frac{\delta}{d-\delta}\phi\right\} \qquad (2)$$

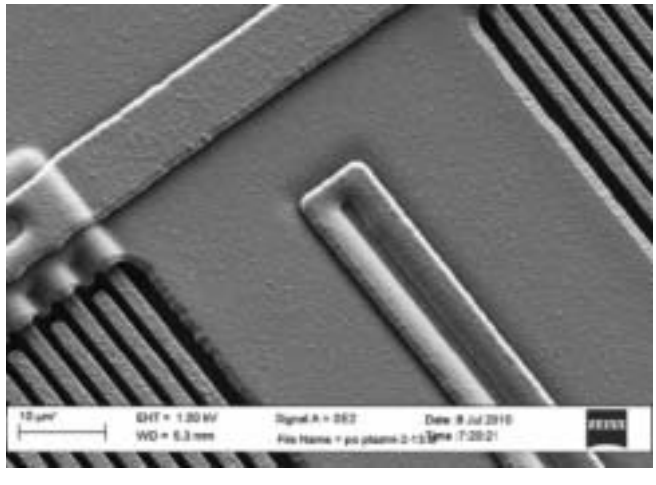

Figure 1: SEM of differential COMB sensor

In reality the detection level must be at least 100 times better than defined by equation (1) because the sensor is not modified 100%, adsorption/desorption is a dynamic process, so not all molecular traps are occupied at the same time and we want to detect minimum possible number of molecules in the air. From this short explanation of the sensor behavior it is clear that ultimate sensitivity is required from the electronics to be able to detect ppb level of selected molecules in the air.

Architecture and noise

To achieve required sensitivity using CMOS electronics at low power consumption many possible solutions exist (1,3,4). All of them are from the noise point of view inferior to the lock-in amplifier principle (5), which is used in this work. Signal processing is divided into analog signal processing (ASP) presented on Figure 2 and digital signal processing (DSP) presented on Figure 3. ASP is used to amplify weak signals coming from the sensor, to perform frequency shaping, down-mixing, filtering and A/D conversion. The DSP performs signal processing in digital domain: decimation filtering, down-mixing, averaging the result and taking care of the coordination. Very high 1/f noise corner frequency of modern MOS transistors require HF operation of the ASP to reach ultimate noise performances. This is achieved by driving differential sensor capacitors by high frequency square-wave signals V_{sp} and V_{sn} with adjustable amplitude A and frequency f_s. The signal at the output of the charge amplifier V_{cho} (equation 3)) is proportional to the difference of both capacitors $\Delta C_1 = C_p - C_n$, amplitude of sensing signals A and is inversely proportional to C_f (feedback capacitance of the CHA) and $H_{CHA}(s)$, that is a HP signal transfer function of the charge amplifier.

$$V_{cho}(s) \cong A\frac{\Delta C_1}{C_f} H_{CHA}(s) \qquad (3)$$

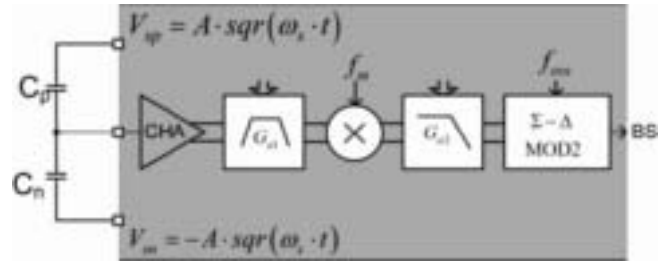

Figure 2: Architecture of the ASP circuit

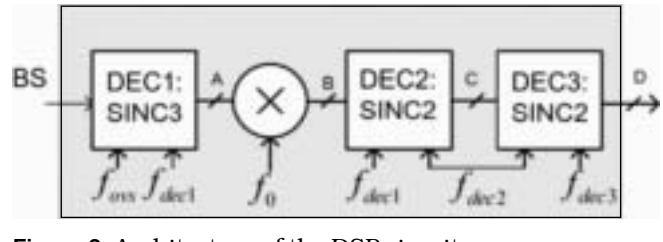

Figure 3: Architecture of the DSP circuit

Noise power density at the input of a first gain stage can be calculated using equation (4), where: $\sum C = 5pF$ that includes all capacitances connected to the virtual ground of CHA, $C_f = 2.1pF$ is a feedback capacitor of the CHA, $C_0 = 0.5pF$ is sensor capacitance and $R_f \cong 50M\Omega$ is the feedback resistor of the CHA. $V_{ndop} = 12nV/\sqrt{Hz}$ is input-referred noise density of the CHA amplifier and of the first gain stage. The noise contributions of sensing generators are negligible because $C_0 \le C_f$. The resulting noise at the input of first gain stage is approx. $V_{ndCHO} = 85nV/\sqrt{Hz}$ and the signal to noise ratio in 1Hz bandwidth for $\Delta C = 1aF$ is $SnR = 12dB$.

$$P_{ndG1\_in} \cong \left[V_{ndOP}\left(1+\frac{\sum C}{C_f}\right)\right]^2 + V_{ndG1}^2 + 2\cdot\left[V_{ndS}\left(\frac{C_0}{C_f}\right)\right]^2 + kTR_f \cdot H_{rf}^2(\omega_s) \quad (4)$$

The spectrum at the output of a charge amplifier including all noise sources is presented on Figure 4. The signal is BP filtered and amplified using low noise programmable gain amplifier with gain $G_{a1} = 11$. To maintain linearity of passive mixer and the following stages G_{a1} is limited because ΔC_0 is big.

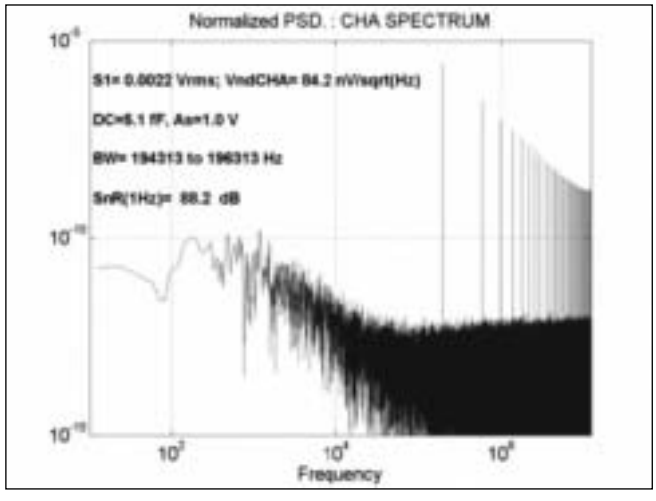

Figure 4: Output spectrum of CHA for $\Delta C = 5\,fF$

Down mixing reduces the frequency to $f_0 = f_s - f_m$ in the region between $f_{knee} < f_0 < f_{Q\,\mathrm{mod}}$, where f_{knee} is the corner frequency of the 1/f noise of CHA and $f_{Q\,\mathrm{mod}}$ is the corner frequency of the modulator shaped quantization noise. The parameters used are:, $f_s = 195.3kHz$ and $f_m = 192.3kHz$. The spectrum at the output of analog passive mixer (Figure 5) is limited by 2nd order continuous time LP filter to reduce out of band components before further amplification by $G_{a2} = 10$. After second gain stage the level is appropriate for A/D conversion using 2nd order ΣΔ modulator. The output of this conversion process is a bit-stream with spectrum presented on Figure 6. The main noise contribution around 3kHz spectral line comes from amplified charge amplifier noise.

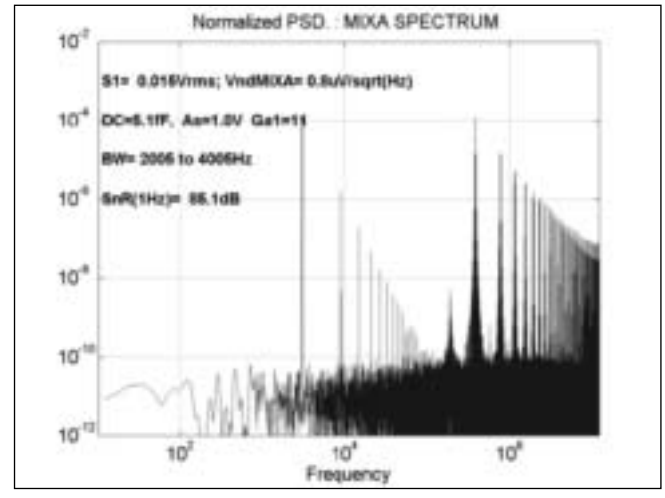

Figure 5: Spectrum at the output of passive mixer for $A = 1V$ and $\Delta C = 5\,fF$ $G_{a1} = 11$

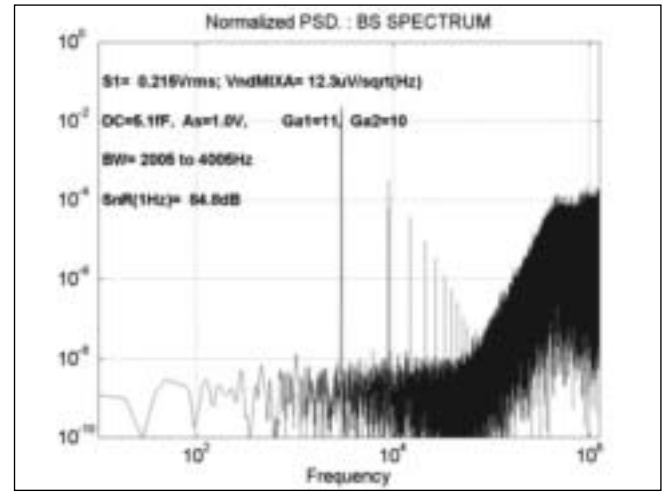

Figure 6: Spectrum at the output of the modulator (BS)

In DSP the BS is first filtered by DEC1 with $R_1 = 32$, $N_{dec1} = 3$ and $WL1 = 16$ that attenuates shaped out of band quantization noise and remains of HF spectral components from MIXA and reduces the sampling frequency down-to $f_{dec1} = 78kHz$. Figure 7 shows the spectrum. 16 bit digital stream is now composed of amplified 3kHz sine-wave with amplitude proportional to ΔC and amplified noise from the CHA. This signal is further mixed by digital mixer driven by square-wave with frequency $f_0 = f_s - f_m$. The result is 16 bit digital signal composed of DC compo-

nent that carries the information, HF spectrum and noise (Figure 8). Further filtering and decimation is performed by DEC2 and DEC3 with the following settings: $R_2 = 520,\ N_{dec2} = 2,\ WL_2 = 32,\ f_{dec2} = 150Hz$

$R_3 = 16,\ N_{dec3} = 2,\ WL_3 = 36,\ f_{dec3} = 9.3Hz,\ WL_{3out} = 24.$ The response to $\Delta C_0 = 5.1fF$ due to manufactured capacitors difference and the effect of one layer of adsorbed molecules ($\delta d = 0.1nm$) is shown on Figure 9 as a time domain response at the output of DEC3.

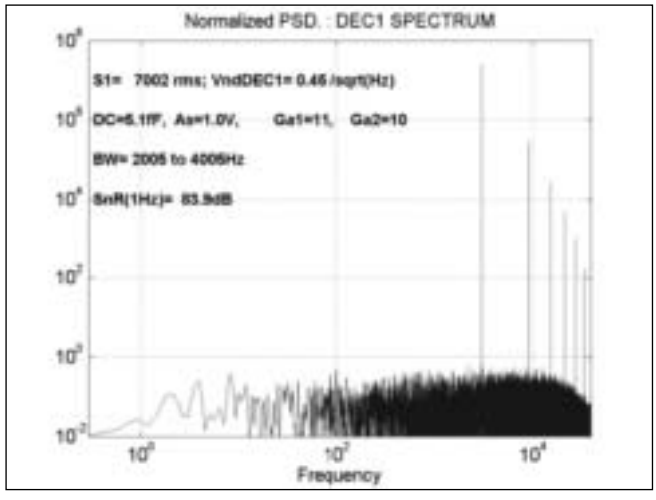

Figure 7: Spectrum at the output of the DEC1

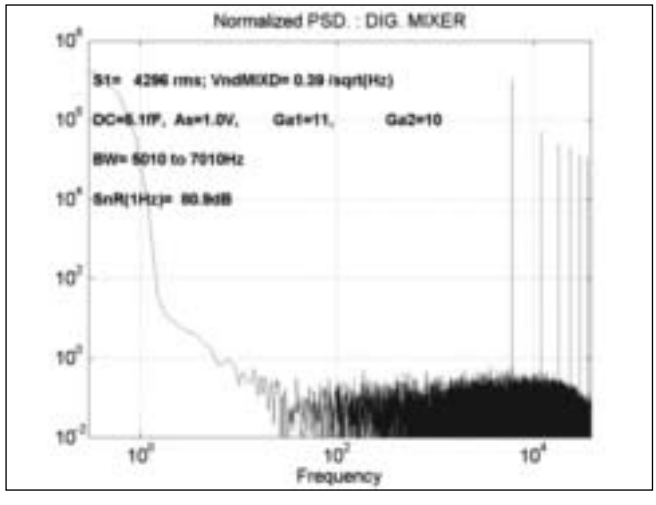

Figure 8: Spectrum after digital mixer

The digital signal is transferred via USB to the PC and presented on the screen in real time (6).

Modeling and measurements

Complete measurement system is modeled in Simulink before implementation. All important parameters as well as non-ideal effects of the ASP

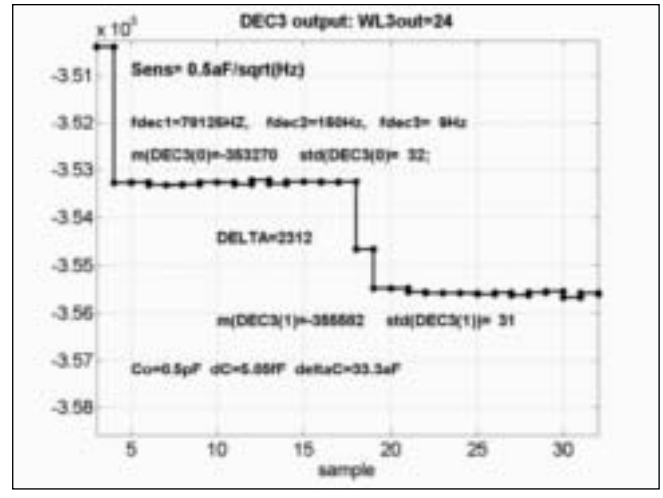

Figure 9: Response at DEC3 output to $\Delta C_0 = 5\,fF$ and $\delta C = 33aF$

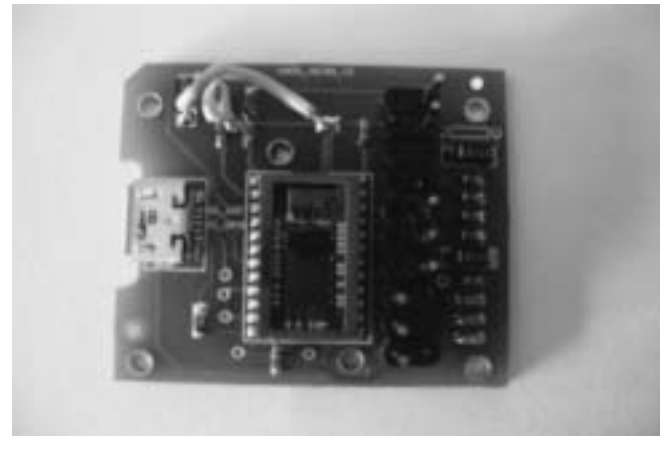

Figure 10: PCB with sensors and ASIC

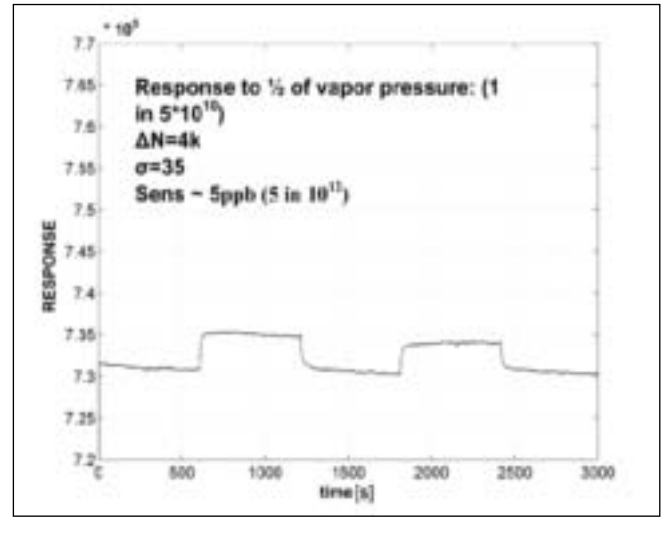

Figure 11: Measured response of the sensor

are included in the model like: GBW, offset voltages, slew-rates, noise power densities (thermal, 1/f, kT/C). At the same time the DSP is modeled as a bit-true model that can be used to compare simulation results with VHDL simulation results. The sensor is modeled as network of capacitors including parasitic and adsorption is modeled as a time and concentration dependent capacitor. Achieved sensitivity is below $0.5aF/\sqrt{Hz}$ that is proven by system level simulations and measurements with the demonstrator. Figure 10 shows a PCB with ASIC and sensors as a system in package (SiP). The response to $^1/_2$ of vapor pressure (the density 0.2 10^{-10}) is shown on Figure 11.

Conclusions

In this work the architecture, design, modeling and implementation of low-noise signal processing electronics needed to implement high-resolution MEMS/NEMS based capacitive sensors interface is described. Using double-mixing lock-in amplifier principle it is possible to sense a capacitance difference smaller than 0.5aF/√Hz on 2.1pF feedback capacitor. The chip is implemented in 0.35um BCD technology with approx. silicon area of 2.5mm^2. Two orders of magnitude improvements are still possible if sensors are implemented on top of the CMOS ASIC (reduced parasitic capacitances), noise of the CHA and gain stages are reduced 5 times and sensing voltages are increased 5 times. Because of achieved characteristics it is possible to use proposed interface for sensing capacitance changes of micro/nano scale chemical or biological sensors with ultimate sensitivity. The proposed improvements are currently in development.

References

1. Zhu Y, Joshua EY, Lee A, Seshia A. A resonant micromachined electrostatic charge sensor. IEEE Sensors J 2008; 8(9): 1499–505.

2. Strle D, Kempe V. MEMS based inertial systems. Informacije MIDEM 2007; 37(4): 199–209.

3. Peng SY, Qureshi MS, Hasler PE, Basu A, Degertekin FL. A charge-based low-power high-SNR capacitive sensing interface circuit. IEEE Trans Circ Syst I 2008; 5(7): 1863–72.

4. Enz C, Themes G. Circuit techniques for reducing the effects of OP-amp imperfections: auto-zeroing, correlated double sampling, and chopper stabilization. Proc IEEE 1996; 84(11): 1584–614.

5. Blair DP, Sydenham PH. Phase sensitive detection as a means to recover signals buried in noise. J Phys E: Sci Instrum 1975; 18(8): 621–7.

6. Nahtigal U, Strle D. Precision measurements of capacitance. In: Proceedings of the 45th International Conference on Microelectronics, Devices and Materials. Postojna, 2009: 371–4.

7. Joo S, Brown RB. Chemical sensors with integrated electronics. Chem Rev 2008; 108(2): 638–51.

NIZKOŠUMNO PROCESIRANJE SIGNALOV ZA MEMS/NEMS BIOLOŠKE SENZORJE: SISTEMSKI POGLED

Strle D.

Povzetek: Prispevek obravnava arhitekturo, modeliranje in implementacijo nizkošumnega elektronskega vezja, ki je uporabno za realizacijo visokoločljivega vmesnika med biološkimi in kemičnimi senzorji, ki temeljijo na tehnologiji MEMS/NEMS in elektronike ob pomoči osebnega računalnika. Uporabljen je princip ojačevalnika »lock-in« s posebnim dvojnim mešanjem, ki je optimalno porazdeljeno med vezjem za procesiranje signalov, in sicer analogno (ASP), in digitalno (DSP). Vezje je sestavljeno iz nizkošumnega ojačevalnika nabojev (CHA), programobilne ojačevalne stopnje, več različnih elektronskih filtrov, analognega mešalnika, ΣΔ analogno-digitalnega pretvornika in ustreznega DSP procesiranja. S temi elementi in takšno arhitekturo je mogoče doseči veliko razmerje signal/šum (več kot 134 dB) ter ločljivost, ki je v razredu 0.5 aF/√Hz pri senzorju s kapaciteto 2pF. Zaradi naštetih karakteristik je mogoče takšen elektronski vmesnik uporabiti kot vmesnik za zaznavo kapacitivnih sprememb pri miniaturnih mikro/nano kemičnih in bioloških senzorjih z veliko občutljivostjo. Vezje je implementirano v 0,35 µm tehnologiji CMOS in zavzema 2,5 mm^2. Izjemna občutljivost kapacitivnega senzorja in opisane elektronike omogoča zaznavo 5 ppb molekul v zraku pri sobni temperaturi.

Ključne besede: elektronski vmesnik za biološke senzorje; šum pri elektronskih vmesnikih; senzorski vmesniki za kapacitivne senzorje; ojačevalniki “lock-in”.