HIGH-SPEED SINGLE D-FLIP-FLOP PSEUDO-RANDOM BIT SEQUENCE GENERATOR

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Abstract: In this article, a new PRBS generation method using a single D-flip-flop is presented. The new method is suitable for the highest data rates, since it allows operation at clock frequencies equal or higher than a shift-register chain, made of the same type of D-flip-flops. Most of the required delays in the new PRBS generator are generated by microwave transmission lines, enabling a higher clock frequency while simplifying circuit design and lowering the cost. A 2.48832Gbit/s PRBS generator was practically implemented using the new method, producing pseudo-random bit sequences corresponding to two standard polynomials $1+x^6+x^7$ and $1+x^{14}+x^{15}$. This efficient design was practically tested at 2.488Gbit/s while its main application is to provide inexpensive 10Gbit/s and 40Gbit/s pseudo-random data sources.

Gigabitni psevdonaključni podatkovni izvor

Kjučne besede:

Izvleček: V prispevku je predstavljena nova metoda generiranja psevdonaključnega binarnega zaporedja (PRBS), ki za delovanje potrebuje le en D flip flop. Nova metoda je primerna za generiranje psevdonaključnih zaporedij zelo visokih bitnih hitrosti, saj deluje z enakimi ali večjimi taktnimi frekvencami kot pomikalni register, izveden z verigo enakih D flip flopov. Večina potrebnih zakasnitev pomikalnega registra je izvedena z mikrovalovnimi linijami, kar omogoča višje taktne frekvence ter cenejšo izdelavo. Praktična izvedba PRBS generatorja z bitno hitrostjo 2,48832 Gbit/s uporablja novo metodo in omogoča dva standardna polinoma $1+x^6+x^7$ ter $1+x^{14}+x^{15}$. Ta učinkovita metoda je bila sicer praktično preverjena pri 2,488 Gbit/s, vendar je njena glavna uporaba namenjena enostavnim in poceni PRBS izvorom z bitnimi hitrostmi 10 in 40 Gbit/s.

Introduction:

Pseudo-Random Binary Sequences (PRBS), usually maximum-length sequences, are widely used in communications systems. PRBS are used as spreading sequences in direct-sequence spread-spectrum systems, like mobile terrestrial CDMA systems or GPS navigation signals. Further, PRBS are used as test data patterns in Bit-Error-Rate test equipment, since they are simple to generate and verify while their mathematical properties resemble random data.

Maximum-length sequences are generated by modulo-2 polynomial division with irreducible polynomials. The latter is practically implemented in the form of linear-feedback

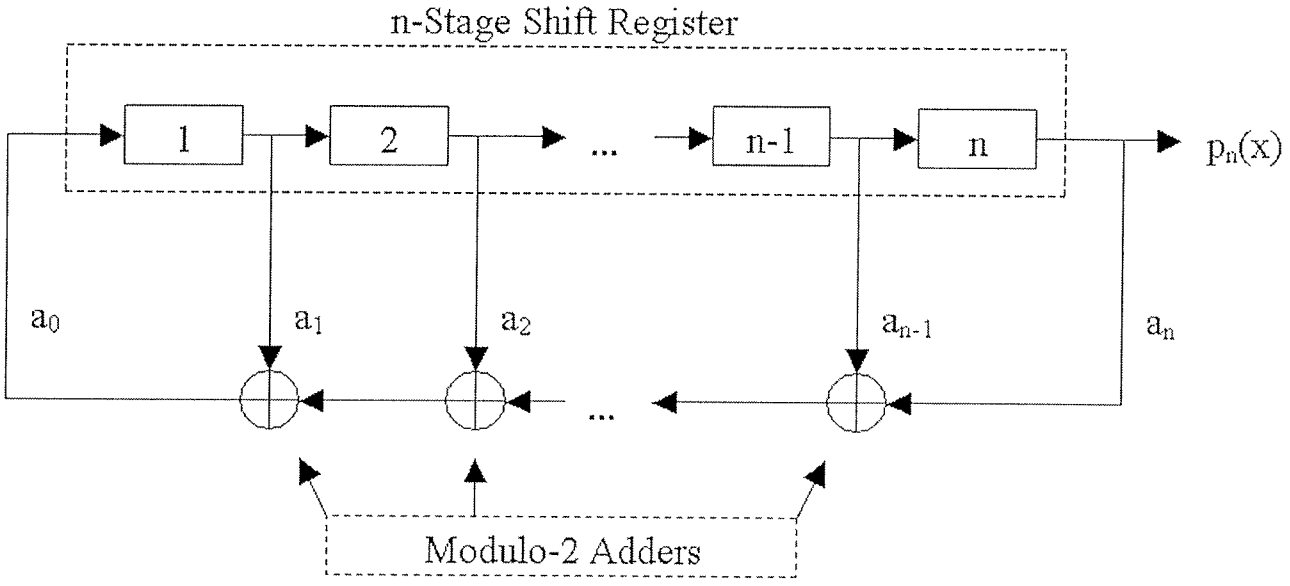

Figure 1: Fibonacci-type n-stage linear-feedback shift register.

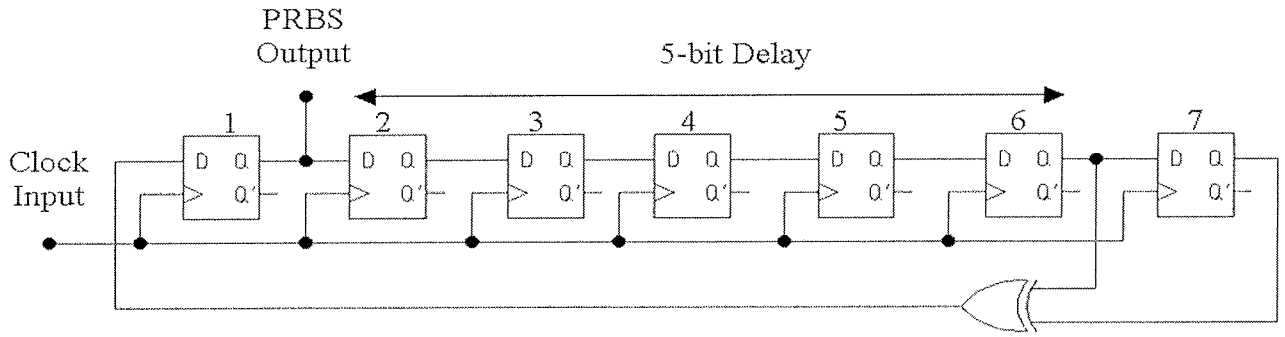

Figure 2: Conventional 7th order PRBS logic circuit generating polynomial $1+x^6+x^7$.

shift registers (LFSR) /1/, where the linearity of the feedback is achieved by modulo-2 addition with EX-OR logic gates as shown on Figure 1. Maximum-length sequences of the length 2^n-1 (where n is the number of shift-register stages) have several interesting mathematical properties, like a precisely-defined pseudo-random distribution of logical ones and zeros, a two-level autocorrelation function and a frequency spectrum including equally-spaced, equal-amplitude spectral lines.

A single D-flip-flop Linear-Feedback Shift Register:

One of the commonly used (modulo-2 irreducible) polynomials in the multi-Gbit/s range communication test equipment is $p(x) = 1 + x^6 + x^7$. Typically such a LFSR comprises seven D-flip-flops and one EX-OR gate as shown on Figure 2.

Ideally, the flip-flops 2 through 6 insert a 5-bit delay (1-bit delay equals $1/f_{clock}$) from the PRBS output tap to the first EX-OR gate tap and the flip-flop 7 inserts a 1-bit delay between the EX-OR gate inputs.

The new method proposed in this article is to replace as many D-flip-flops as possible with transmission lines (microstrip lines, coaxial lines, etc.) to generate delays. However, at least one D-flip-flop is required for signal regeneration (retiming and reshaping) in a PRBS generator. Figure 3 illustrates the new PRBS generator including a single D-flip-flop, an EX-OR gate and additional transmission (delay) lines.

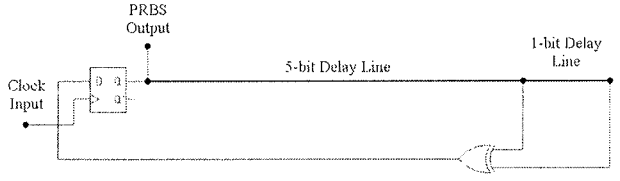

Figure 3: A single-D-flip-flop 7th order PRBS circuit generating polynomial $1+x^6+x^7$.

Note that the circuit from Figure 3 requires an ideal D-flip-flop and an ideal EX-OR gate (without any internal propagation delays) and that the 1-bit delay line is connected directly between EX-OR gate inputs without any additional PCB traces. Of course, both internal D-flip-flop and EX-OR-gate propagation delays have to be considered in the practical high-speed circuit design, where the sum of both delays is subtracted from the ideal 5-bit delay.

When compared to the conventional LFSR circuit of Figure 2, the new PRBS circuit has many advantages: simplicity, less logic elements (integrated circuits) and a lower cost. A single-D-flip-flop design eliminates complex clock distribution circuits required for several D-flip-flops in conventional high-speed LFSR designs. Finally, the clock frequency can be increased to the upper D-flip-flop toggle limit and the latter is usually much higher than the clock-frequency limit imposed by propagation delays in a chain of D-flip-flops, especially in the case of discrete-packaged devices.

Unfortunately, the single-D-flip-flop PRBS design also has some drawbacks: the PRBS polynomial depends on the delay lines and cannot be changed easily, the PRBS sequence length is limited by the insertion loss and dispersion of the delay lines and the design only works for a selected, single clock frequency as defined by the delay lines.

A 2.48832 Gbit/s PRBS data pattern generator core

The new PRBS generation method, using a single D-flip-flop, has been tested on a working prototype using ON Semiconductor's ECLinPS Lite /2/ integrated circuits, MC100EL31 (D-flip-flop) and MC10EL58 (2:1 multiplexer used as an EX-OR gate) at a clock frequency of 2.48832GHz. Besides the two ECL chips, an 1-bit microstrip delay line and two removable coaxial delay lines were used in the core of the 2.48832Gbit/s PRBS data pattern generator to produce two different pseudo-random sequences corresponding to the polynomials $1+x^6+x^7$ and $1+x^{14}+x^{15}$. Both coaxial delay lines were shortened from the ideal 5-bit (for $1+x^6+x^7$ polynomial) or 13-bit (for $1+x^{14}+x^{15}$ polynomial) propagation delays to compensate for the internal propagation delays of the D-flip-flop, of the 2:1 multiplexer and corresponding PCB transmission lines to the SMA connectors, where the coaxial delay lines are connected.

To reduce the output data jitter and clock crosstalk, two more integrated circuits were added to the PRBS generator prototype as shown on Figure 4. An additional MC100EL31 D-flip-flop is used to decrease the output PRBS data jitter. A differential receiver MC10EL16 is used to remove common-mode signals (primarily 2.48832GHz clock) from the output PRBS data.

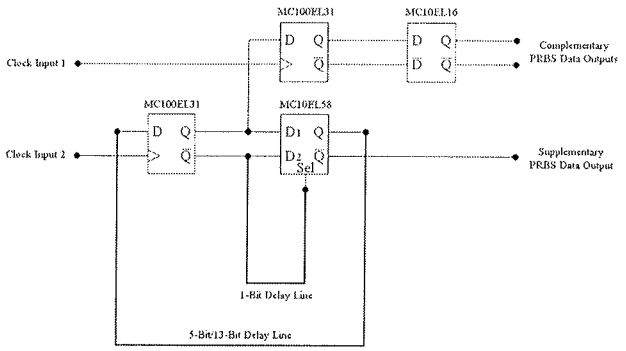

Figure 4: Circuit diagram of the 2.48832Gbit/s PRBS data pattern generator core, with the addition of a second D-flip-flop and a differential receiver.

Bold lines on Figure 4 represent 50Ohm impedance-controlled transmission lines. The circuit has two 2.48832GHz (sinewave) clock inputs driving the clock inputs of the two D-flip-flops. The two complementary ECL PRBS data outputs have to be DC-terminated to Vtt for optimal performance. The supplementary, AC-coupled, PRBS data output is connected to the 7^{th} order polynomial PRBS pattern-sync trigger-generator circuit, to be described later in this article.

The prototype of the 2.48832Gbit/s PRBS generator core, including the second D-flip-flop and differential receiver is built on a 0.8mm-thick, double-sided "Epsilam-10" laminate, with the bottom side acting as the microstrip groundplane and connected to the Vcc. The top side is used for impedance-controlled microstrip transmission lines. All power supply connections are made using thin wire bridges. The 1-bit microstrip delay line was manually trimmed for the optimum length to compensate for the reactive impedance of the "D2" input of the MC10EL58 multiplexer. A photo of the prototype is shown on Figure 5.

The quality of the output PRBS data was evaluated using a 40GHz-input-bandwidth sampling oscilloscope (HP83480A Digital Communications Analyzer with HP83482A Plug-In). A simple resistive divider circuit was used to terminate the ECL outputs to Vtt, while enabling a DC-coupled connection to the 50Ohm input of the sampling oscilloscope. Since differential test equipment was not available, only single-ended measurements were performed.

The eye pattern of the output PRBS data corresponding to the $1+x^{14}+x^{15}$ polynomial is shown on Figure 6. The clock

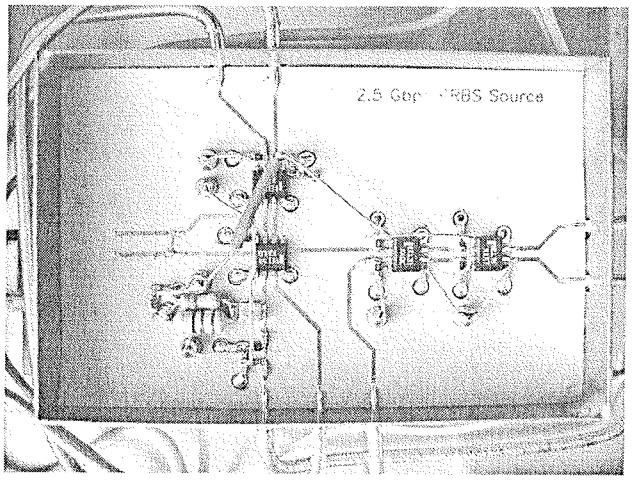

Figure 5: Photo of the 2.48832Gbit/s PRBS generator core circuit prototype.

crosstalk is clearly visible in the PRBS data. The peak-to-peak jitter (of the sampling oscilloscope and the PRBS generator) of approximately 40ps could be further reduced using additional D-flip-flops. The jitter is predominantly deterministic since the measured peak-to-peak value does not grow significantly with time.

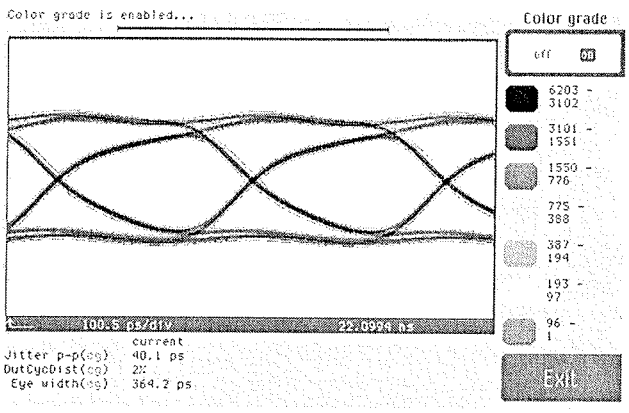

Figure 6: Eye pattern of the $1+x^{14}+x^{15}$ PRBS.

An Agilent 8565EC 50GHz spectrum analyzer was used to measure the frequency spectrum of the output PRBS data corresponding to the $1+x^6+x^7$ polynomial as shown on Figure 7. Again, the 2.48832GHz clock crosstalk is clearly visible in the output PRBS data spectrum. Due to simple NRZ encoding, a sin(x)/x spectrum envelope is expected and can be fairly well recognized on Figure 7.

A pattern-sync trigger-generator circuit for the $1+x^6+x^7$ polynomial

The eye pattern is one of the most popular measurements of data signal quality since it is implemented easily: the oscilloscope is triggered by a synchronous data clock. No knowledge of the exact data content is needed and no frame nor pattern trigger pulses are required for the meas-

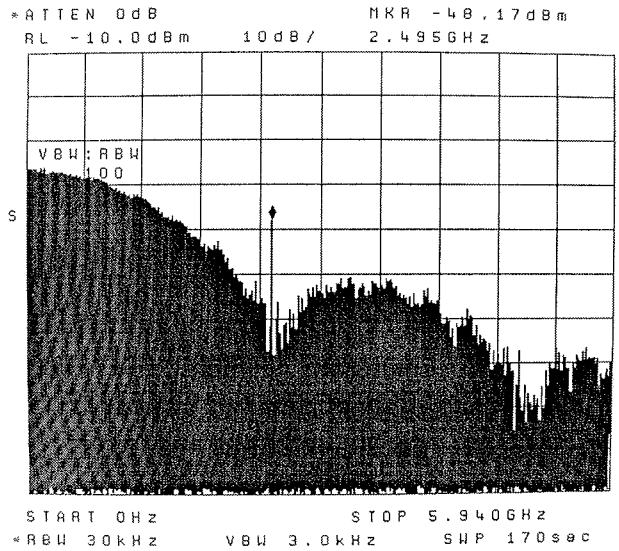

Figure 7: Frequency spectrum of the $1+x^6+x^7$ PRBS.

urement of the eye pattern. However, other measurements like the observation of specific bit distortions may require a frame-sync or pattern-sync trigger pulse. The beginning of a maximum-length LFSR sequence is usually defined with the all-ones state of the shift register. The detection of the all-ones state requires additional high-speed logic circuits and may be very expensive to implement at high clock frequencies. Fortunately, at least for short LFSR sequences there is a simpler, analog way of deriving a pattern-sync trigger pulse.

Since the spectrum of a maximum-length LFSR sequence includes equally-spaced discrete spectral lines, it is sufficient to filter out the lowest-frequency spectral line to obtain a trigger that is synchronous to the whole sequence pattern. In the case of the 2.48832Gbit/s $1+x^6+x^7$ polynomial sequence that has a repetition period 127bits, the lowest discrete spectral component has a frequency of 19.593MHz.

The supplementary, AC-coupled, 2.48832Gbit/s PRBS data is simply fed through a low-pass filter circuit with the cutoff frequency of about 22MHz. The 7th order pattern-sync circuit diagram is shown on Figure 8 and includes an INA-10386 MMIC amplifier and two low-pass filters: a lumped-element 22MHz low-pass and a 400MHz microstrip low-pass to suppress the spurious responses of the lumped-element filter above 1GHz. The prototype photo is shown on Figure 9.

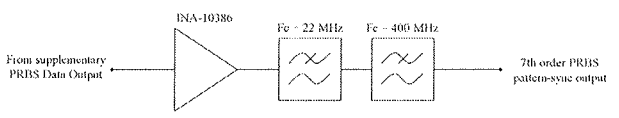

Figure 8: Circuit diagram of the 7th order pattern-sync circuit.

The sinewave output of the analog low-pass pattern-sync circuit is further processed by an additional circuit (description omitted from this article): MC10H102 gate and yet another MC100EL31 flip-flop. MC10H102 gate convertes analog pattern-sync trigger signal to ECL logic levels. Most of the timing jitter of the trigger signal is removed by MC100EL31 D-flip-flop clocked at 2.48832GHz. Such a pattern-sync trigger signal allows a detailed analysis of the PRBS bit pattern. The complete 127-bit PRBS pattern is shown on Figure 10.

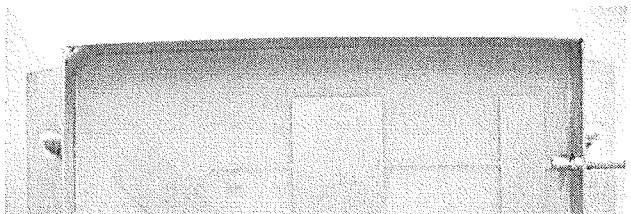

Figure 9: Photo of the 7th order pattern-sync circuit prototype.

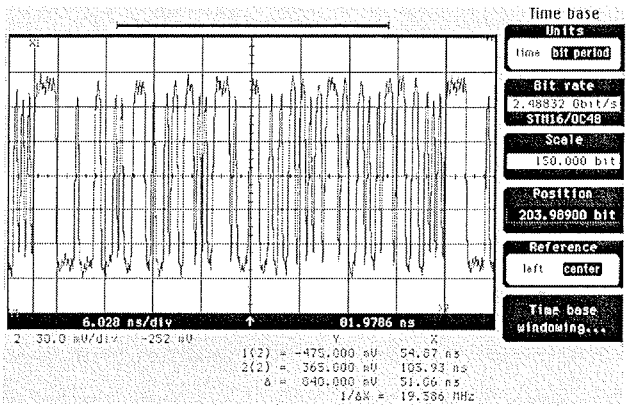

Figure 10: The complete 127-bit PRBS pattern.

An overview of the standalone 2.48832Gbit/s PRBS data pattern generator

The circuits described in this article are parts of the standalone 2.48832Gbit/s PRBS (OC-48/STM-16) data pattern generator. Besides the described PRBS core circuit and PRBS pattern-sync trigger circuit, the generator also includes a 2.48832GHz clock source PLL-locked to an internal crystal reference, a clock-signal distribution circuit (for both D-flip-flops in the PRBS core circuit), a trigger circuit to start the PRBS generator in the case of an all-zero stall and power-supply circuits for the Vbb and Vtt voltages required by ECL circuits.

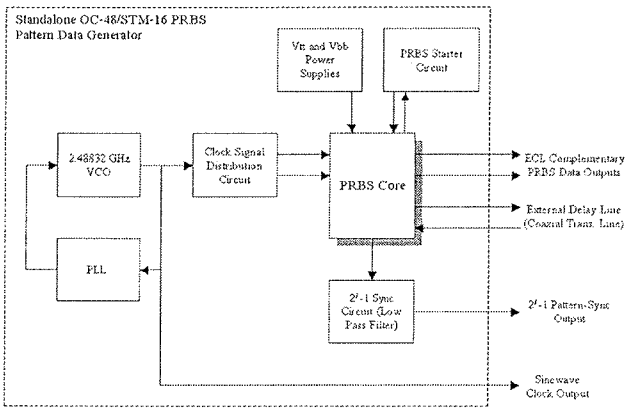

Figure 11: Block diagram of the standalone 2.48832 Gbit/s PRBS generator.

The block diagram of the PRBS generator is shown on Figure 11. The generator has two complementary ECL data outputs (Q and /Q), two connectors for the external delay line, a pattern-sync trigger output for the $1+x^6+x^7$ polynomial and two clock outputs. Descriptions of the additional circuits are beyond the scope of this article, but none of them is not as nearly (relatively) complex as PRBS core circuit. A photo of the standalone 2.48832Gbit/s PRBS data pattern generator prototype is shown on Figure 12.

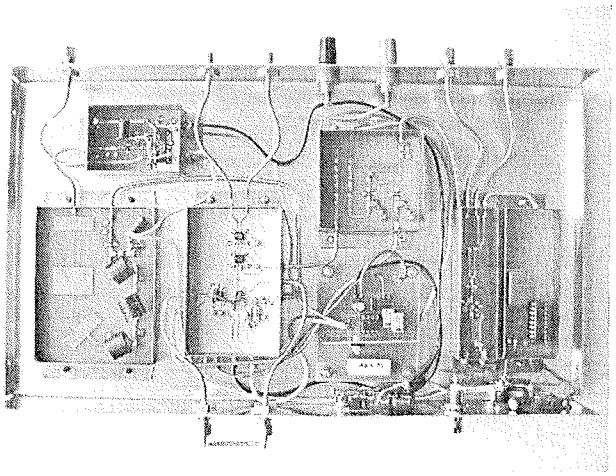

Figure 12: Standalone 2.48832Gbit/s (OC-48/STM-16) PRBS generator.

Conclusion:

The design of a simple and efficient high-speed PRBS data pattern generator was presented in this article. The PRBS generator achieves error-free operation at a clock frequency of 2.48832GHz that is almost twice the limit imposed by device propagation delays for conventional shift-register designs using chains of (discrete) MC100EL31 D-flip-flops. Furthermore, the clock frequency of the single-D-flip-flop design is limited only by the D-flip-flop maximum toggle frequency. A companion Bit-Error-Rate test receiver could be designed in the same way, implementing a polynomial divider with transmission-line delays in place of D-flip-flops.

Knowing the mathematical properties of LFSR sequences even some other circuits can be simplified, like replacing complex digital pattern-sync circuits with simple analog low-pass filters. Although all of our experiments were made at 2.48832GHz, the principles are fully scalable to higher clock frequencies of 10GHz and even 40GHz. This means that a complete Bit-Error-Rate test setup can be built for 10Gbit/s or even 40Gbit/s for a very small fraction of the cost of similar, commercially available OC-196 and OC-768 test equipment.

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