REALIZING A LOW-COST PFC THAT HAS LOW MCU LOAD REQUIREMENTS

Uroš Rupar[1], Franci Lahajnar[1], Peter Zajec[2]

[1]Kolektor Group d.o.o., Idrija, Slovenia

[2] University of Ljubljana, Faculty of Electrical Engineering, Ljubljana, Slovenia

Key words: Active filter, PFC, PWM modulator, microcontroller

Abstract: This article presents the design of a hybrid system for controlling switching power converters in either continuous conduction mode (CCM) or critical conduction mode. The system is particularly suitable for a Boost converter in Power Factor Correction (PFC) applications. It requires low-cost hardware and a minimum of CPU power. The proposed solution is, therefore, very convenient for use in cost-sensitive applications based on 8-bit MCUs, where the use of special integrated circuits or other complex systems remains unacceptable.

Cenovno ugodna izvedba korektorja močnostnega faktorja z minimalno obremenitvijo pripadajočega mikrokontrolerja

Kjučne besede: Aktivni filter, PFC, PWM modulator, mikrokontroler

Izvleček: Prispevek predstavlja zasnovo hibridnega elektronskega sklopa za vodenje močnostnih stikalnih pretvornikov v načinu netrganega toka (CCM) ali v načinu mejnega toka. Sklop je zlasti primeren za »navzgor« oz. Boost pretvornike v sistemih za korekcijo močnostnega faktorja (Power Factor Correction, PFC). Izvedba zahteva poceni in enostavno vezje ter minimalno procesorsko moč. Predlagana izvedba je zato primerna za vgradnjo v cenovno občutljive aplikacije, kjer uporaba namenskih integriranih vezij ali drugih kompleksnih rešitev ni smotrna.

1. Introduction

Power Factor Correctors (PFCs) and active filters for harmonic current reduction are becoming a necessity in most power-supply designs. In motor-control applications, for example, the use of PFCs continues to grow. A PFC satisfies the harmonic-current-reduction requirements, and at the same time ensures a sufficiently high DC link voltage to supply a power inverter. However, a PFC adds a considerable cost to an application, and without any benefit to the customer.

The consequence of this is that there is a great deal of research in an attempt to develop a low-cost, functionally optimized solution. On the one hand, there has been considerable growth in special, analog ICs, while on the other hand, many control methods based on digital circuits have been developed; this is because of their improving performance and reducing costs. Analog ICs with the required set of external components are still too expensive, while the use of an extra programmable digital circuit for the control of the PFC in a cost-sensitive application is also not reasonable.

An interesting solution is the use of a microcontroller (MCU) or a digital signal processor (DSP) that is already present in the system and is able to perform the whole, or just a part, of the PFC algorithm as a sideline. Many digital systems and methods have been developed for PFC-converter control, realized by DSP's or MCU's /1-4/, some even use FPGA technology /5/. However, due to their complexity, they all require a lot of computational power and/or sampling rates, while some methods /6-7/ also require zero crossing detection and pre-calculated look-up tables. As such, algorithms are mainly too complex to run in a sideline with main application algorithms, as with induction-motor (IM) control, for example. So, particularly when using low-cost 8-bit MCUs, a different strategy is required.

The main idea is the realization of a part of the PFC algorithm, in particular the fast, inner current control loop, with a simple analog circuit, while the slower voltage control loop is still running on the MCU. A simplified block scheme of a hybrid system is shown in Figure 1.

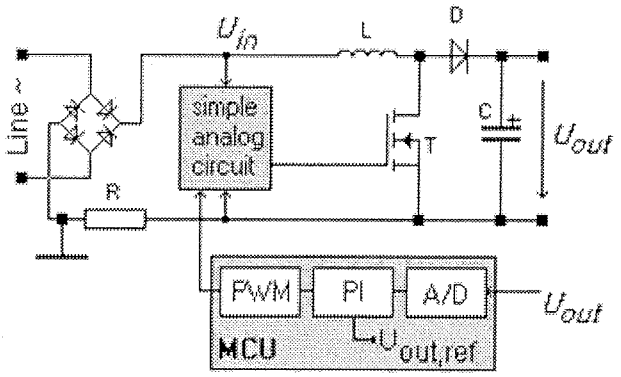

Figure 1: Hybrid Boost-PFC design

A possible solution is the use of the One (Single) Cycle Control (OCC) method, /8/,/9/, which is particularly sim-

ple and inexpensive because the multiplier and the input-voltage measurement is eliminated. A PFC realization example using the OCC control method is shown in Figure 2.

The critical point when using the OCC method in this way is the requirement that the integrator time constant and the clock period must be equal. To achieve this term, more complex circuits are required.

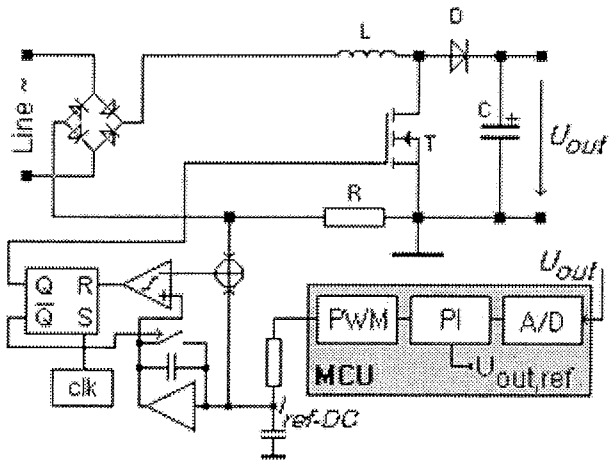

Figure 2: Hybrid Boost-PFC design using the OCC control method

Another, even simpler, solution is described in /10/, with its modification described in /7/. It is a simple and frequently used PFC controller based on a free-running hysteresis current-mode control. The realization block scheme is shown in Figure 3.

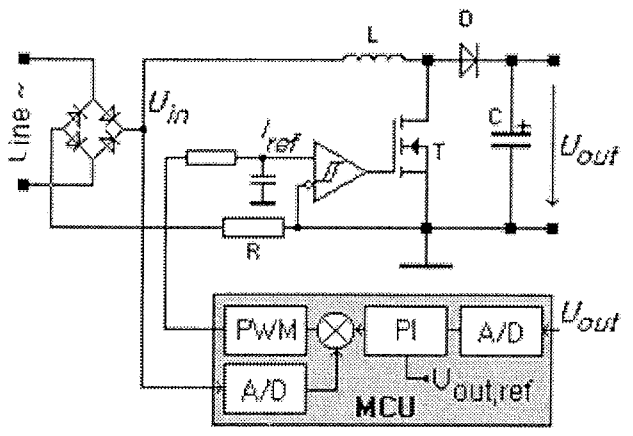

Figure 3: Boost-PFC with hysteresis current-mode control

The realization /10/ requires a lot of computational power and high sampling rates, due to the input-voltage measurement, while the second one, /7/, requires a zero crossing detection circuit and a synchronization algorithm.

This article describes an improved single-phase PFC control strategy based on a hysteresis current-mode control suitable for use with an 8-bit MCU with a minimum of free resources available. The PFC algorithm occupies a small amount of memory and CPU time, and can therefore be executed in a sideline with the main application tasks, like motor control and lamp ballasts algorithms, while the additional analog circuit is easy to understand and implement.

In this paper only the basic PFC functionality is described, in order that we can clearly present the proposed control-method realization. The final application should include some additional functions to ensure safe and reliable operation. These functions, like soft start, over-current protection, under- and over-voltage protection etc., are not the essence of this document, and are therefore not described in detail.

The paper is organized as follows. The basic principle of operation is described in Section 2, this is followed by a practical realization example in Section 3. In Section 4 the proposed realization is verified with a simulation and experimental results. Finally, there are some conclusions in Section 5.

2. Basic operating principle

The basic idea of the proposed solution is the relocation of the input-voltage measurement circuit and the multiplier into a simple low-cost analog circuit. This is in contrast to the applications in /7/ and /10/, where these two functions are running on the MCU, resulting in considerable CPU load. The proposed realization, where both functions are combined in a single PWM modulator and an analog switch, is given in Figure 4.

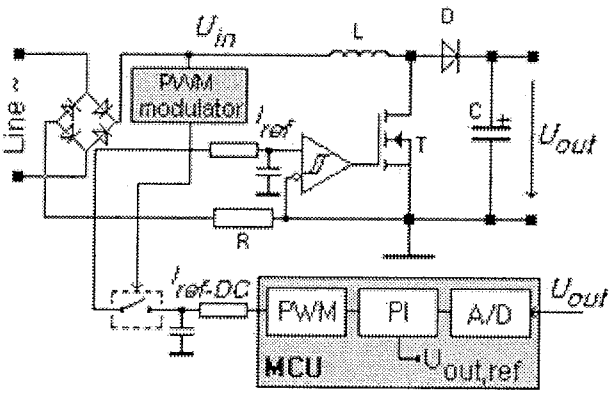

Figure 4: Proposed Boost-PFC control method

As a result, minimal CPU load is achieved as the MCU performs only the output-voltage measurement and a PI controller computation, both with a sample time equal to the line voltage period. In addition, the MCU is occupied with only one analog input, and the PWM output that is used as a D/A converter generating the DC current reference signal I_{ref-DC}. I_{ref-DC} is the voltage-control loop output value.

An analog multiplier is realized with an analog switch being driven by an input-voltage-modulated PWM signal. With this solution, the input current reference I_{ref} has the same si-

nusoidal shape as the input line voltage and an amplitude proportional to the DC current reference $I_{ref\text{-}DC}$.

A trailing-edge modulator (Figure 5) is used as a PWM modulator. Its operating principle is evident from Figure 6.

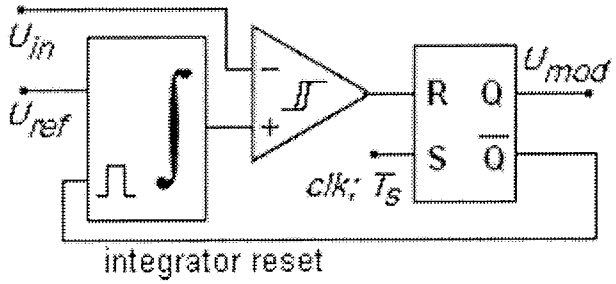

Figure 5: Basic PWM modulator block scheme

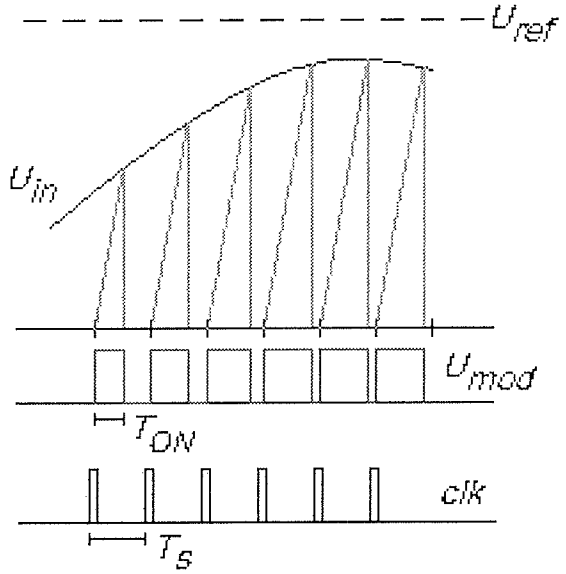

Figure 6: Operating principle of the PWM modulator

In the case that the PWM frequency is much higher than the line frequency and the integrator time constant $T_S' \approx T_S$, the modulator ON-time can be expressed as

$$T_{ON}(t) = \frac{U_{in}(t)}{U_{ref}} \times T_S$$

where $U_{in}(t)$ is the input voltage, U_{ref} is the reference voltage and T_S is the clock signal period. The PWM duty-cycle is then equal to:

$$D(t) = \frac{T_{ON}(t)}{T_S} = \frac{U_{in}(t)}{U_{ref}}.$$

The average modulator output voltage is then proportional to the input voltage U_{in} and the PWM amplitude U_{mod}:

$$\overline{u_{\mathrm{mod}}}(t) = D(t) \times U_{\mathrm{mod}} = \frac{1}{U_{ref}}(U_{in}(t) \times U_{\mathrm{mod}}).$$

The reference voltage U_{ref} must satisfy the equation:

$$U_{ref} \geq U_{in,\max},$$

where $U_{in,max}$ is the maximum input-voltage amplitude.

By using the analog switch we ensure that the PWM signal amplitude is equal to $I_{ref\text{-}DC}$, representing the output-voltage controller command value. The input-current reference is then equal to:

$$\overline{I_{ref}}(t) = \frac{1}{U_{ref}}(U_{in}(t) \times I_{ref-DC}) = k \times (U_{in}(t) \times I_{ref-DC}).$$

It is obvious that the input-current reference amplitude is proportional to the voltage-controller output value ($I_{ref\text{-}DC}$), while the input-current shape is determined by the input line-voltage shape ($U_{in}(t)$).

The fast current controller is realized in the same way as in /10/, using a hysteresis comparator with a reference signal I_{ref}, as shown in Figure 7.

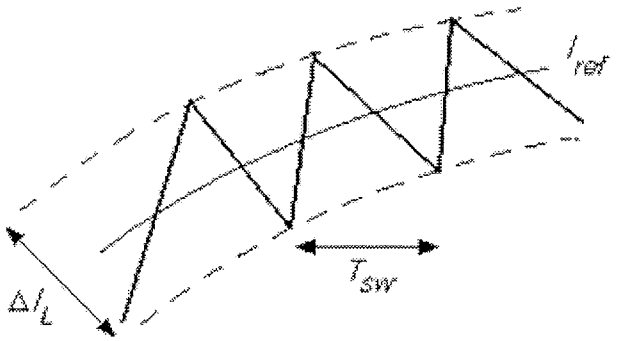

Figure 7: Hysteresis current-mode control principle

The comparator hysteresis ΔI_L directly determines the input-current ripple and the converter switching frequency, which is determined as follows:

$$f_{SW}(t) = \frac{1}{L \times \Delta I_L} \times \frac{U_{in}(t)}{U_{out}} \times (U_{out} - U_{in}(t)).$$

The equation is given assuming that the switching frequency is much higher than the line frequency.

3. Practical realization example

A simple and low-cost PWM modulator is realized employing the well-known 555 timer and an additional integrator circuit. This IC already consists of two voltage comparators, the RS-latch and the discharge transistor. The proposed PWM modulator scheme is shown in Figure 8.

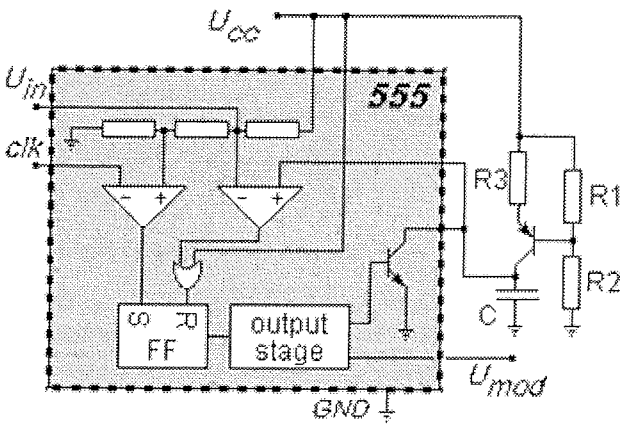

Figure 8: Proposed PWM modulator

The capacitor value is determined as:

$$C = \frac{I_C \times T_S'}{U_{in,\max}},$$

where *Ic* is a charging current, defined as:

$$I_C = \frac{1}{R_3}\left(U_{CC}\frac{R_1}{R_1+R_2} - U_{EB}\right),$$

where U_{EB} is the emitter-base voltage of the transistor used in an current-source circuit.

The MCU PWM signal was used as a clock signal (*clk*) to trigger the PWM modulator. So this signal carries double the information. The PWM's frequency determines the PWM's modulator frequency, while the PWM's duty cycle determines the input current amplitude. The PWM's frequency must be chosen to be sufficiently high to achieve sufficient resolution and to eliminate a phase shift between the input voltage and the input current. In our case, the PWM's frequency was 50 kHz.

4. Simulation and experimental results

The simulation results were acquired using the Boost converter model and the proposed controller model developed in Matlab-Simulink. A 200-W system with a 380-V output DC voltage and a 230-V input voltage was simulated to prove the proposed realization regularity. The experimental results were acquired using a 200-W PFC prototype board and a Motorola-HC08 evaluation board.

Figure 9 shows the simulation results for stationary (constant-load) operation. The input current directly mirrors the input-voltage shape, which reflects the resistive behavior of the whole system at the line terminals. The experimental measurement results under the same conditions are shown in Figure 10.

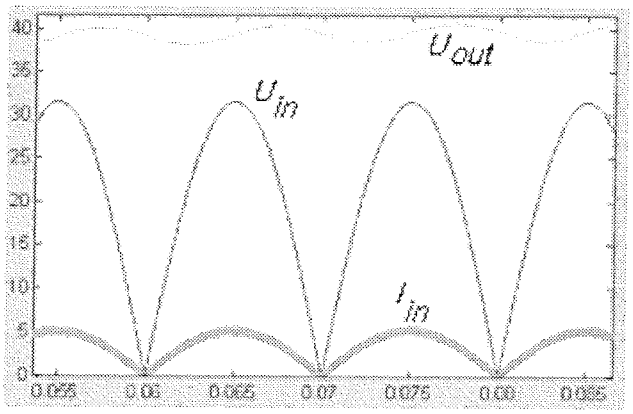

Figure 9: Typical simulation waveforms: DC Bus voltage U_{out}, rectified input voltage U_{in} and rectified input current I_{in}

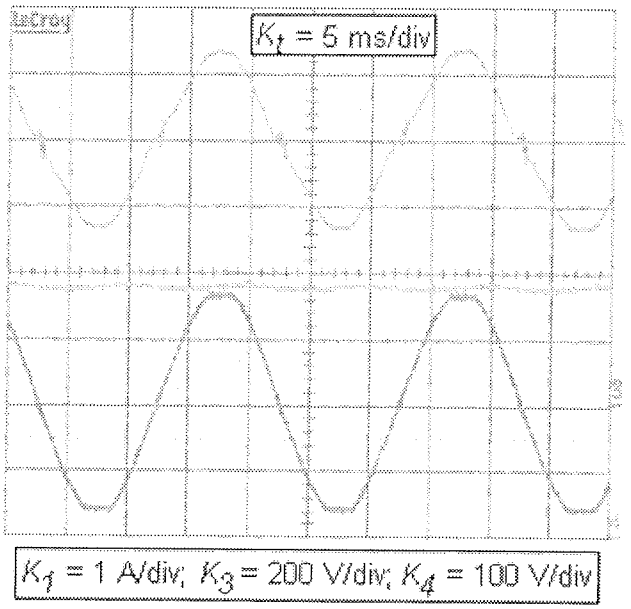

Figure 10: Typical experimental waveforms: DC Bus voltage U_{out} (ch 4), input voltage U_{in} (ch 3) and input current I_{in} (ch 1)

The measured waveforms from Fig 10 directly confirm the simulation results.

Another very important property of the PFC converter is its stable behavior under load variations. Experimental results acquired from a step load change from 140 W to 210 W are shown in Fig 11. It is obvious when comparing with the results in /1/,/5/,/10/ that the proposed PFC controller solution does not adversely affect the dynamic behavior of the closed-loop system.

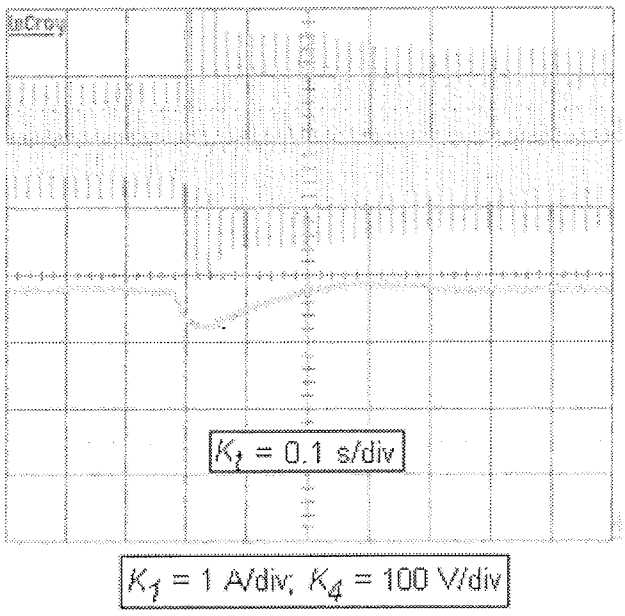

Figure 11: Input-current (ch1) and output-voltage (ch4) waveforms during a step load change from 140 W to 210 W

The switching frequency changes over a line period, as shown in Figure 12. This special course has a very important preference. While the switching frequency decreases in phase with the highest input current, the switching losses are, as a result, considerably reduced. In practice, the switching frequency does not really reduce to zero, as seen in the simulation results. In our case, the minimum switching frequency around the zero crossing point was 50 kHz.

The line-current harmonics measurement results are the same as in /10/, because of the equal current controller realization.

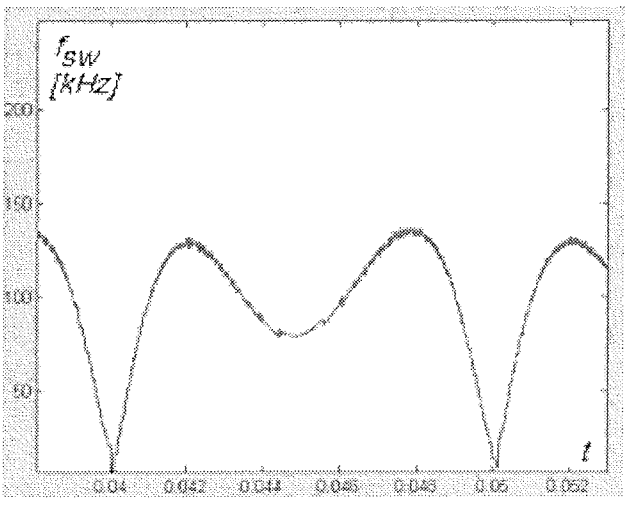

Figure 12: PFC switching frequency over a line half period - simulation results

The real benefit is obvious from the MCU load. The proposed solution requires about 100 A/D samples and multiplication instructions per second, while in /10/ this rate was 5000 A/D samples and multiplications per second. The PFC functions, written in C-language, occupy 150 program bytes, 10 RAM locations, and are executed in approximately 200 µs at an 8-MHz MCU bus-frequency, i.e., 1% of the total execution time of the benchmarked MCU.

5. Conclusion

The proposed PFC control method is particularly suitable for the Boost PFC converter design in cost-sensitive applications where the use of special ICs or extra MCUs (DSPs) is not practical. The whole system is designed as a hybrid system, as a combination of a programmable digital circuit and an additional analog circuit. The microcontroller performs only the outer voltage-control loop, while the faster inner current-control loop is realized using a simple and low-cost analog circuit - a PWM modulator, an analog switch and a hysteresis comparator. The PFC algorithm can be executed in a sideline, together with the main application tasks, like motor control and lamp ballasts algorithms.

The proposed realization is suitable for critical conduction mode as well as continuous conduction mode Boost PFC converters.

With this solution, a good compromise between the CPU load and circuit complexity is achieved. The proposed PFC control method can be implemented in low-cost applications based on slower 8-bit MCUs, where previously proposed methods become too complex.

A soft-start function, for example, can easily be implemented by writing an additional program module. This module generates the current reference signal during start-up and switches to the PI-controller when the output voltage reaches its final value. Alternatively, just the PI-controller's output saturation level can be slowly raised to its upper limit during start-up, like in /1/. Over-current protection, which is also very important, can be implemented using an additional voltage comparator and (optionally) an input MCU pin. When using an IC with multiple comparators inside there is no additional hardware cost. Also, the current reference can be software limited. These additional functions result in an MCU program-code extension of up to 50 bytes when it is written in C-language.

6. References

/1/ S. Buso, P. Mattavelli,et al., "Simple Digital Control Improving Dynamic Performance of Power Factor Preregulators", *IEEE Transaction on Power Electronics*, vol. 13, no .5, pp.814-823, 1998

/2/ J. Chen, A. Prodic, R. W. Erickson, D. Maksimovic, "Predictive Digital Current programmed Control", *IEEE Transaction on Power Electronics*, vol. 18, no. 1, pp.411-419, 2003

/3/ De Mari Y., "Easy power factor correction using a DSP", *PCIM '99, Proceedings of 39th Intern. Conference on Power Conversion*, Nuernberg, pp. 585-592, 1999

/4/ W. Zhang, G. Feng, Y.F. Liu, B. Wu, "DSP Implementation of Predictive Control Strategy for Power Factor Correction (PFC)", accepted by *IEEE Applied Power Electronics Conference*, *APEC* 2004

/5/ A. Castro, P. Zumel, O. Garcia, T. Riesgo, J. Uceda, "Concurrent and Simple Digital Controller of an AC/DC Converter With Power Factor Correction Based on an FPGA", *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 334-343, January 2003

/6/ B. Strzalkowski, et al.: µP control of single phase PFC boost converter supplying PWM inverter using single microcontroller", *PCIM 2001, Proceedings of Intern. Conference on Power Electronics*, Nuernberg

/7/ "Design of Indirect Power Factor Correction Using DSP56F80X", Motorola Application Note AN1919/D

/8/ K. M. Smedley, S. Cuk, "One cycle control of switching converters", *IEEE PESC Conf. Rec.*, pp. 1173-1180.

/9/ Z. Lai, K. Smedley, "A Family of Power-Factor-Correction Controllers", *APEC'97*, New York, USA, IEEE, pp.66-73, vol.1, 1997

/10/ A. Hofmann, A. Baumüller, T. Gerhardt, M. März, E. Schimanek: "A robust digital PFC control method suitable for low-cost microcontroller", *3rd International Conference on Integrated Power Systems 2003*, Nürnberg, pp.387-391, 2003

Uroš Rupar, univ. dipl. ing. el.
Kolektor Group d.o.o.,
Vojkova 10, 5280 Idrija
tel.: +386 5 3750 510, e-mail: uros.rupar@kolektor.si

dr. Franci Lahajnar, univ. dipl. ing. el.
Kolektor Group d.o.o.,
Vojkova 10, 5280 Idrija
tel.: +386 5 3750 134, e-mail:
franci.lahajnar@kolektor.si

doc. dr. Peter Zajec, univ. dipl. ing. el
Univerza v Ljubljani, Fakulteta za elektrotehniko,
Tržaška 25, Ljubljana
tel.: +386 1 4768 479, e-mail: peter.zajec@fe.uni-lj.si

Prispelo (Arrived): 10.03.2005 *Sprejeto (Accepted): 12.06.2005*