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# Content | Vsebina

# *Editorial | Uvodnik*

Dear Reader,

This issue brings one review scientific paper and 11 original scientific papers. A focus of the last (4th) issue used to be on state-of-the-art papers by invited speakers at the MIDEM conference that we organize in late September every year. Although the 52nd MIDEM Conference under the Chairmanship of Dr. Danilo Vrtačnik and Dr. Drago Resnik was a big success with the highlight on Biosensors and Microfluidics Workshop, distinguished invited speakers could not commit themselves to write a full paper for our journal except Dr. Guillaume Tresset and Dr. Ciprian Iliescu. To compensate the loss, the conference programme committee made a selection of the best regular papers that have been peer-reviewed and published mainly in the previous issue. As the last papers from the conference you can find in this issue the papers by Patrizia Malpignano et al..

Year 2016 is rapidly running out and this editorial should reveal some statistics about manuscripts. In 2016 we have received more than 182 manuscripts, out of which only 27 have been accepted for publication and more than 140 manuscript were rejected. Despite clearly defined title of our journal and on-line instructions for authors we receive each year a dozen of manuscripts that are out of our journal's scope. In 2016 we published 2 review scientific papers and 28 original scientific papers. The success rate below 20% in 2016 reflects determination for quality that will path long-term quality growth. An increase in the JCR impact factor and SNIP for 2015 is certainly a proof for that. I would like to sincerely thank all reviewers and Editorial Board Members for their valuable contribution to the journal quality growth.

In 2015 we have worked hard to switch to an on-line submission and review process of manuscripts. Thanks to Dr. Kristijan Brecl and Dr. Matija Pirc who mastered the Open Journal Systems and prepared it for our journal, we have successfully passed the initial phase with the on-line submission starting 1st Jan 2016. We are pleased that the system enables shorter review times, better support for reviewers and higher satisfaction of authors.

December is time for recognition and celebration, as elsewhere also in Slovenian science arena. We are happy to congratulate Prof. Dr. Janez Krč to be honoured with the "Zoisovo priznanje" – the second highest Award of the Republic of Slovenia for Scientific and Research Achievements – that he received for important achievements in Photovoltaics and Optoelectronics.

Let the festive days bring joy and peace in each home, office or research laboratory. It is the time to look ahead and make ambitious plans for the coming year. This brings me to editorial wishes for 2017. As a part of your success we look forward to receiving your next manuscript(s) on our submission page (http://ojs.midem-drustvo.si/).

Merry Christmas and a Happy and Prosperous New Year!

Prof. Marko Topič
Editor-in-Chief

P.S.
We look forward to receiving your next manuscript(s) in our on-line submission platform:
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Review scientific paper

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# A Comprehensive Review on Perfusion Cell Culture Systems

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**Abstract:** The enormous cost and time required for launching of a new drug on the market request a redesign of testing approaches and validation strategies. Here, microfluidics, micro and nanotechnologies can play an important role, impacting the cell culture model or the delivering strategies. We will review the recent lab-on-a-chip strategies for cell culture models with potential application for drug screening platforms. Moreover we will overview also the materials involved in the microfluidic assisted cell culture models.

**Keywords:** microfluidics; cell culture; bioreactors; biomaterials

# Sistematičen pregled pretočnih sistemov za celične kulture

**Izvleček:** Uvedba novih zdravil na trg zahteva veliko razvojnega časa in je povezana z ogromnimi stroški. Za znižanje stroškov in časa se nujno pojavlja zahteva po preoblikovanje pristopov testiranja in strategij za validacijo ustreznosti zdravil. Tukaj lahko mikro in nanotehnologije ter uvajanje mikrofluidnih pristopov odigrajo pomembno vlogo pri izgradnji modelov celičnih kultur ali pa so v pomoč pri razvoju strategij za vnosa zdravil. Pregledni članek predstavlja določene nove strategije, ki temeljijo na lab-on-a-chip mikrofluidnih pristopih in njihovo praktično uporabnost pri predkliničnem testiranju zdravil. Poleg tega je v članku podan tudi pregled biomaterialov, ki se uporabljajo pri izdelavi mikrofluidnih platform, namenjenih raziskavam modelov celičnih kultur.

**Ključne besede:** mikrofluidika; celične kulture; bioreaktorji; biomateriali

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## 1 Introduction

The cost of developing of a new drug is rising exponentially along with every phase of development, reaching US$800 million per drug [1]. In this direction, the identification of the drug potential toxicological profile in the earlier development stage became a necessity. On the other hand, combinatorial chemistry as well as molecular biology and genomics understanding have led to a rapid growth of the group of novel compounds [2]. As a result, *in vitro* drug metabolism testing platforms are gaining increasing importance compared to animal model counterpart in the early stage drug screening given the high throughput testing capacity. It is not surprising to find that tremendous efforts have been put into developing suitable *in vitro* tissue model for the perusal of drug development. The main focus is on liver, the main organ involved in drug metabolism. *In vitro* models such as isolated perfused livers or liver tissue slices are difficult to use in high throughput applications despite their close imitation to *in vivo* hepatic tissue. The isolated primary hepatocytes, strike a balance between high throughput and intact cellular architecture [3]. However, isolated primary hepatocytes rapidly lose their differentiated functions when cultured using standard cell culture conditions [4]. Therefore numerous culture models have been developed

to prolong their functions. The cell culture models can be divided in two major groups based on the modality of media refreshing: static culture models and perfusion culture models. For the perfusion culture models the media is continuously replaced. As such, $O_2$ and nutrients transport, as well as waste removal from cellular local environment improved [5]. For example, it has been shown that under perfusion the viability, life span and metabolic performance of primary hepatocytes improved [6]. The phase I and phase II enzymes also showd long term stability in perfusion culture [7]. Perfused-cultured hepatocytes responded well to inducer and have shown stable induction of CYPs up to 7 days [8]. However, the main drawback of the perfusion culture system relies in the shear stress induced by the flow. A high value of the shear stress could be detrimental to cell viability and cell functions *in vitro* [3, 9].

Used on a large scale for application related chemical synthesis [10-12], cell manipulation and analysis [13-19], or drug discovery [20-23], microfluidics can be an interesting support for application related tissue engineering [24-26].

This article gives an overview on microfluidic related cell culture models and focuses on the system dedicated to drug screening. It also succinctly presents the materials involved in the construction of the microfluidic bioreactors.

## 2 On chip cell culture models

'Organ-on-a-chip' models allow restatement of *in vivo* tissue-tissue interfaces, biochemical cues and mechanical microenvironment. These models offer the opportunity of *in vitro* drug screening and could be alternatives to animal experimentation [27, 28]. On-chip models present the advantage of using less cells and reagents. In the next sections we will review the main cell culture models underlining the contribution of microfluidic and microtechnology in this direction.

### 2.1 Cell lines

Cell lines are well-established cell culture model. Under suitable conditions the cells will proliferate indefinitely. Cell lines are not restricted by limited number of cell divisions due to mutations. The limitation is also known as Hayflick's limit [29]. Liver cell lines are a popular choice for studying liver function and toxicity mechanism *in vitro*. They are, however, not suitable for drug metabolism and toxicity predictions because not all metabolizing enzymes are present in cell lines and the ones present are not at their normal physiological levels. One merit of human cell lines is that they can be used to gather information relevant to human body functions. Moreover, they are easy to handle and can help reduce the use of animals. Disadvantages occur because their dependence of gene expression, on passage number, unstable cells and dedifferentiated cells with phenotype no longer resembling that of the cells *in vivo*. Cell lines are also prone to contamination by other cell types, which happens with 15-20% of cell lines [30].

### 2.2 Liver cell lines

HepG2 cell line is the most commonly used human liver cell line. It is derived from hepatocellular carcinoma. Compared with isolated primary hepatocytes, its level of CYP is lower. Another commonly used cell line is HepG2/C3A, it is selected for its improved differentiated hepatocyte phenotype. Both of these cell lines have been cultured on chip [31-33]. Another liver cell line HepaRG was recently generated. It is reported to be more metabolically competent, however it has yet to be studied in microfluidic devices [34]. HepG2 was first integrated into microfluidic device in 2003 by Leclerc *et al.*[35]. They showed that the cells function properly for at least 12 days on their perfusion device. In microfluidic studies of HepG2 cells, the cells were treated with various compounds of different concentrations to study toxicity. Their viability was determined by live dead staining and optical imaging [36-38]. By using microfluidic devices, it is possible to achieve multiple incubations in one chip and generate concentration gradients easily. For high throughput screening of cells, this is especially useful. For instance, the PDMS chip developed by Ye *et al* [38], (Figure 1), incorporated eight identical structures with integrated gradient generator based on the principle reported by Jeon *et al* [39]. Two inlets are present on chip, for medium and for drug mixed with medium respectively. The two liquids were mixed in a wide channel then split multiple times to generate mixture having different concentration ratios with the initial solution. The HepG2 cells can therefore be exposed to various concentrations of drugs, and are able to be observed directly under a microscope. Eight identical structures ensured that eight different compounds can be tested on chip concurrently. The device was set up in an incubator at 37 °C with 5% $CO_2$. PDMS is gas permeable such that a stable microenvironment can be established.

However the expression of metabolic enzyme in HepG2 is low, making it unsuitable for toxicity prediction. Both biotransformation process of drugs and toxicity profiles are altered compared with *in vivo* situations [40]. In the mean time it is generally accepted that, cell lines can be used to investigate molecular pathways due to

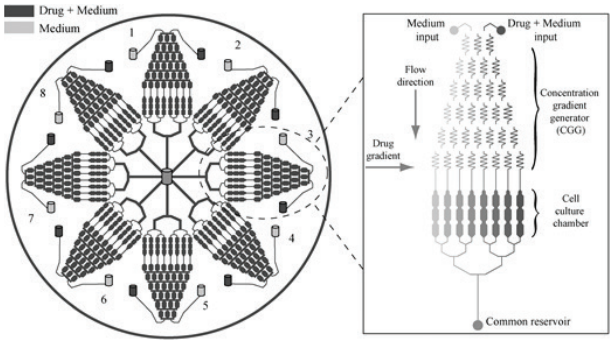


**Figure 1:** Schematic of the chip developed by Ye *et al* [38], with eight identical structures and gradient generators. (Copyright 2007 Royal Society of Chemistry).

their robustness. Another example is the system developed by Sung *et al* [41] to monitor CYP activities optically. It has a green light emitting LED for excitation and a photodiode for detection. HepG2/C3A were cultured in Matrigel on chip. It has been reported that cells maintain their functions better in a 3D configuration [42]. Metabolic activities of CYP1A1 and CYP1A2 were assessed by ethoxyresorufin and were shown to have improved functions compared with conventional monolayer cultures. Continuous perfusion of medium was applied to the cells, to ensure that the cells are constantly exposed to fresh medium with fixed nutrient concentration. This device is useful for real time monitoring of CYP activities for primary hepatocytes as well. Moreover, Carraro *et al* [43] developed a PDMS device to mimic the human hepatic microvascular bed. HepG2/C3A cells were maintained up to 10 days. Phase I and phase II metabolites were detected during this period. The incorporation of primary hepatocytes was also feasible. The hepatocytes were not exposed to medium flow directly as is the case of in vivo situation and the exchange of medium took place by diffusion through polycarbonate membrane with pore size of 0.4 mm.

### *2.3 Primary cells*

Primary hepatocytes are generally accepted as a better *in vitro* model to predict *in vivo* metabolism than cell lines [44]. They can be isolated from liver tissue by collagenase perfusion, which digests the connective tissue [45]. In primary hepatocytes, metabolizing enzymes are present at their natural physiological levels. Thus they can be used to predict hepatic metabolism quantitatively. Although metabolic enzymes are initially at their physiological levels, CYP-mediated metabolism gradually decreases during extended cultures. To prevent this, the cells can be cultured in Matrigel with supply of inducers. Alternatively, non-parenchymal cells can be co-cultured with primary cells [46-48].

Furthermore, liver anatomy was mimicked by Lee *et al* [49] who fabricated a PDMS device (Figure 2a). The device featured an artificial liver sinusoid with an artificial barrier layer mimicking endothelial barrier layer. Primary rat and human hepatocytes were maintained for 7 days. A similar structure was used by Nakao *et al* [50] for bile canaliculi formation. The microfluidic structure allowed the rat primary hepatocytes to align, to form two rows like a hepatic cord. This way the bile canaliculi can be formed at the interface between cells (Figure 2b).

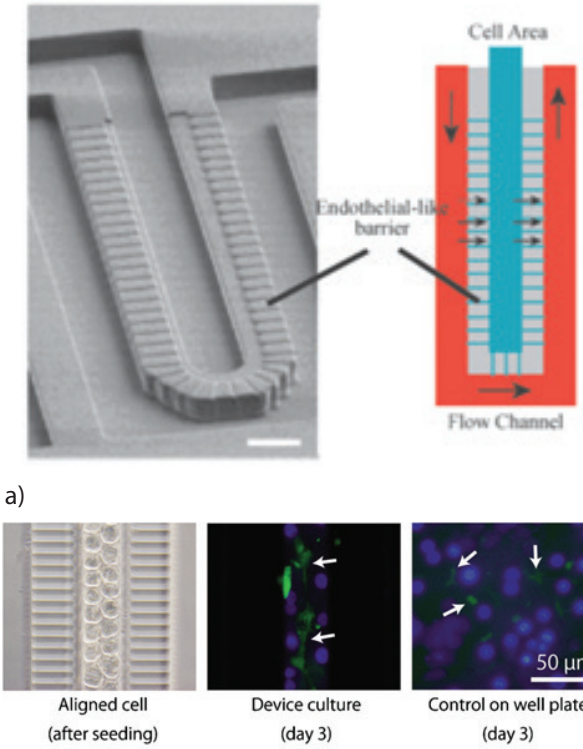


**Figure 2:** a) Optical image and schematics of the device resembling a liver sinusoid, cells are cultured in the cell area, medium flows around outside of the barrier. (Copyright 2007 John Wiley and Sons, Inc.) [49] b) Bile caniculi formation in a microfluidic structure: aligning of the cells in two lines like a hepatic cord, bile caniculi (green color) formation, control in static cell culture [50].

Another primary hepatocyte culture chip was fabricated by Griffith lab using microfluidic techniques. Hepatocyte metabolic activities was tested with the chip [51]. The 3D culture scaffold was fabricated in silicon with deep reactive-ion etching. Primary hepatocytes were cultured in the bioreactor for 2 weeks. The level of mRNA expression of CYP enzymes, transcription factors and phase II drug metabolizing genes were retained. A higher throughput version of their device was recently developed. It incorporates a pneumatic micropump

and fluidic capacitor to achieve pulseless flow (Figure 3) [52]. Hepatocytes remained viable and retained capacity for albumin synthesis during culture. The device was placed in a humidified incubator with controlled pH and $O_2$ content. The flow rate was set to 250 µL/min.

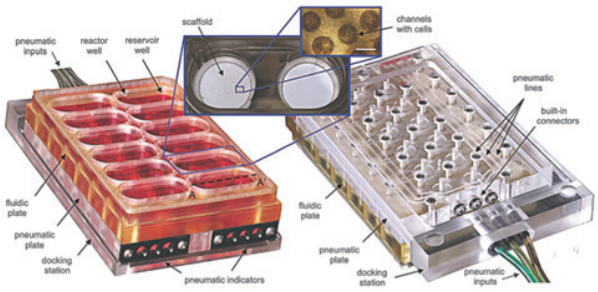


**Figure 3:** Perfused microwells for culture of hepatocytes with integrated pneumatic pump (Copyright 2010 Royal Society of Chemistry) [52].

### *2.4 Spheroid cell culture model*

Hepatocytes form aggregates when they are weakly adherent or non-adherent to the culture substrate. The presence of the 3D cytoarchitecture through the re-establishment of 3D cell-cell contacts, together with the secretion of extracellular matrix material within the spheroid, had been hypothesized to contribute to better maintenance of differentiated function compared with the traditional matrix overlay [53] and matrix monolayer culture [54]. Studies have shown the maintenance of the drug metabolizing enzymes in extended cultures of spheroids [55] as well as induction of some key enzymes in response to prototypical inducers [4]. However the presence of necrotic/ hypoxic cells in the center of the spheroid due to oxygen diffusional limitations in large sized spheroids [56] as well as the difficulty to handle floating spheroids in conventional wells have limited their used in long-term metabolism, enzyme induction and cytotoxicity studies [57]. An overview of the methods to achieve 3D cell culture models using microfluidic systems was presented by Choudhury *et al* in [58]. Currently, different techniques are used for cell assembling into spheroids. Their key point is promoting cell-cell interaction and limiting cell-substrate interaction. A well known technique is hanging drop method [59]. This method is relatively simple, but the exchange of cell media is challenging [60]. Moreover, the limited volume of the drop (50 µL) made this culture method less suitable for drug screening applications and difficult to be translated into large-scale production. Another commercially available method (AggreWell™ by Stem Cell Technologies) consisted in centrifugation of the well-plate [61-63]. Despite the relatively high cost of the well-plate, the method also required incubation for spheroid formation. Rotational bioreactors (spinner flasks) can also be use for spheroid formation, but the large shear stress generated limits its application to primary hepatocytes [64]. Another classical method, liquid overlay involved cell culture on a low adhesive layer. The method was simple and inexpensive, but induced a large variation of the spheroids' diameter [65-67]. Another method consisted in micropatterning of selective-adhesive structures on a non-adhesive substrate [68, 69]. The main advantage of the method was the uniform size and distribution of the 3D cellular aggregates. Other microfluidic methods involved cell trapping barriers [70], bubble or droplet-based methods [71], microwells in which rotational flow of a cell suspension was induced [72, 73], and cell assembling by ultrasonic actuation in microwells [74]. An ultrafast microfluidic method for cell aggregation in spheroids was recently reported by Alhasan *et al* in [26]. The method consisted of combining surface acoustic wave (SAW) microcentrifugation with the use of fast gelling hydrogel. The method was demonstrated with human mammary gland carcinoma cells (BT-474) and with mesenchymal stem cells (MSCs). It is relevant to mention that the formation of spheroids was performed in standard tissue culture plasticwear. Moreover, the size of the spheroid can be simply tuned by selecting the power input to the SAW. Another relevant approach in spheroid cell culture is the concept of "constrained spheroids"(CS) presented by Tong *et al* in [25]. The CS cell culture model overcame one of the most relevant problems related to spheroid cell culture. In the static culture, due to the turbulence generated by culture media change, the spheroids lose their adhesion on the substrate. Under perfusion, due to their relatively large diameter and fluid velocity, the spheroids are exposed to a momentum generated by the Stokes force. This momentum removes the spheroid from the substrate causing cell loss. In order to overcome this problem, in the CS model, the spheroids are trapped and stabilized by sandwich configuration between a PEG-AHG-modified glass and an ultra-thin Parylene C membrane. This allowed to maximize mass transfer, and to overcome uneven cell count and spheroids size-related issues. The glass substrate was modified for more uniform and rapid hepatocytes spheroids formation within 1 day, allowing for earlier drug testing and perfusion culture initiation. The membrane was specifically modified so that the hepatocytes in the spheroid will preserve their cytoskeleton distribution. The results showed not only a better conservation of the cell count but also an improvement of the cell function.

### *2.5 Intact tissue*

Primary cells can be co-cultured with non-parenchymal cells to mimic the natural hepatic architecture after isolation from intact liver tissue. Instead of using isolated

cells, it is also possible to collect intact tissue directly from the body and perform *in vitro* assessments. Compared with isolated cells, intact tissues have intact cell matrices as well as all cell types and their enzymes, cofactors and transporters. Thus, they highly resemble the *in vivo* architecture. Intact tissues can be obtained from animals or humans by surgery. Two ways have been exploited so far, namely liver biopsies and precision-cut liver slices. Liver biopsies can be obtained by cutting liver sample by hand or using biopsy punch, whereas precision-cut liver slices are obtained by using Krumdieck tissue slicer or Brendel-Vitron tissue slicer.[75] Tissue slices of thickness from 100µm can be obtained by tissue slicers, the thickness of the slices obtained are usually small enough for nutrients and oxygen to diffuse to inner regions. During culture period, the level of metabolic enzymes also decreases gradually, as in the case of primary hepatocytes. The rate of decline is slower compared with primary hepatocytes [76]. Recently, several groups have incorporated precision-cut liver slices [77] and biopsies [78].

### *2.6 Biopsies*

For biopsy, Hattersley *et al* [78] designed a device which consisted of a Y shaped channel with two inlets and one outlet. Three chambers with inner diameter of 3 mm were present for insertion of the biopsy. Tissue chambers were located on top of microfluidic channels to avoid the direct exposure of tissues to media stream. The nutrients were delivered mainly by circulating medium. Regarding the tissue biopsy, the cells further away from the medium flow are exposed to lower concentration of $O_2$ and nutrients. Since, the hepatocytes in vivo are located just a few microns from the blood stream, it becomes difficult for cells to survive when they are more than a few hundred microns from the blood stream [79]. To regulate pH and $O_2$ content, the chip was put into an incubator. Lactate dehydrogenase and DNA were measured through the outlet of the device. Morphologies of the cells were also assessed.

### *2.7 Precision-cut liver slices (PCLS)*

PCLS was first integrated to micro-bioreactor in 1996, PCLS were first fixed on a microscope slide with plasma clot, while perfusion was performed directly on the slide [80]. Fluorescence confocal laser cytometry, facilitated the assessment of cytochrome P450 distribution in PCLS. However, only one side of the slice was exposed to medium, which hindered the transport of nutrients and gases. In addition, enzyme activities were not quantified with the help of this device. Consequently another microfluidic device fabricated by Khong *et al* [81] was used to perfuse thick liver slices of 0.3-1 mm thick. The tissue slice was placed directly in medium flow and 7 needles were inserted to the tissue slice to facilitate mass transport inside the tissue slice. CYP1A and UGT were reported to be stable for up to 3 days. This device could be used for induction and inhibition studies with PCLS. More recently, van Midwoud *et al* [77] developed a micro-perfusion bioreactor to study the rat liver metabolism. The device was fabricated out of PDMS with incorporation of polycarbonate filter and PDMS membranes. In each chamber, PCLS of 3 to 4 mm diameter were cultured in a continuous flow of medium. The PCLS functionalities remained for 24 hours, human PCLS were integrated and tested, the metabolism and viability were comparable to those of conventional well-plate system. Thus, microfluidic bioreactor helps to reduce the use of animals for preclinical testing by using scarce human material.

The continuous flow applied to the slices ensured that direct analysis of the outflow. An HPLC device equipped with UV detection was coupled with the bioreactor to achieve real time detection of metabolites [82]. Metabolites could immediately be measured upon exposure of a slice to medium. Retention of viability could be demonstrated. By increasing substrate concentration over time, the device was also used to measure inhibition constant. Only three tissue slices were used, which would allow studied to be performed with scarce samples. Moreover, the device can detect unstable metabolites instantaneously. This is difficult to achieve in conventional well-plate system.

### *2.8 Organs-on-a-chip*

Conventional 2D and 3D cell culture models have demonstrated their values in tissue specific biomedical research. However they may not accurately predict *in vivo* tissue behavior and drug activities due to their difficulties in recapitulating multi-scale tissue architecture, tissue-tissue interface and mechanical cues. Microfluidic organs-on-chips have the possibility of overcoming these limitations [83]. Organ-on-a-chip devices also enable high resolution, real-time imaging and various assays of biochemical, genetic and metabolic activities. The first major step in organ-on-chips for drug development happened in 2004, when the Schuler group designed a microfluidic chip for pharmacokinetic studies of multiple cell types interconnected by microchannels [84]. The device featured three cell culture chambers for lung, liver and other cell types on a single silicon chip. It targeted the examination of the adsorption, distribution, metabolism, elimination and toxicity (ADMET) profile of chemicals *in vitro.* By achieving physiological liquid-to-cell ratio, shear stress and liquid residence time, this device paved the way for using microfluidic devices to reduce or even replacing animal testing in the pharmaceutical industry. An-

other organ-on-a-chip devices to investigate crosstalk between different organs was designed by Zhang *et al* [85]. This multi-channel 3D microfluidic cell culture system features compartmentalized microenvironments for drug screening. Liver, lung, kidney and adipose cells were simultaneously cultured in 4 compartments. The four cell types represent the drug-metabolizing and storage capabilities in the human body. This kind of multiorgan system can potentially be used for drug testing, food safety testing as well as pathogen testing.

Over the past decade, a lot of devices have been developed to support PK-PD modeling. Acetaminophen is one of the commonly studied drugs in microfluidic devices. In a study done by Mahler *et al* [86], HepG2 cells were coupled with intestinal cells. They demonstrated that administration of acetaminophen caused glutathione depletion in intestinal cells. A dose dependent hepatotoxicity response was also observed. The result obtained from the microchip was similar to *in vivo* experimental results.

In spite of the swift advances of microfluidic devices, certain hepatic functions such as bile duct clearance or sustained production of metabolic enzymes (as compared with the 1-year lifespan of hepatocytes *in vivo*) still cannot be completely modeled using chips. The presence of flow might not always be beneficial either, some metabolites accumulate in small static microenvironments that are undetectable in flow conditions due to sensitivity issues [87].

### *2.9 Fish-on-a-chip*

Zebrafish and especially its embryo, is a vertebrate model for study in embryogenesis, development biology, cell biology and genetics and is becoming an important model for preclinical drug discovery applications. The overall drug toxicity in Zebrafish embryo is comparable with that observed in mammals [88]. Due to shorter development time and cheaper maintenance, Zebrafish model is cost-effectiveness. Zebrafish embryos are small, easily obtained in large numbers, accessible immediately after fertilization, they are optically transparent and pigmentation mutants exhibit extended period of transparency [89]. The embryos are permeable to peptides, drugs and dyes. Also, specific genes can be inhibited or mutated and the entire genome of Zebrafish has been sequenced and can be accessed online [88, 90]. The drug studies on embryos, mostly performed on 96 well microtiter plates [91] were not suitable for dynamic long-term culturing and imaging of embryos. For this reason "fish-on-chip" solution are desirable. Martin *et al* [92] proposed a high-throughput vertebrate screening platform (VAST) in which the fish embryos were manipulated and oriented for cellular resolution imaging. Their platform permitted large-scale chemical screens. Drug studies on Zebrafish and Medaka embryos [93],[94] have already found their way into microfluidic systems. A study related to the delivery of foreign compounds into the embryos by electroporators is presented in [95]. Research on Zebrafish embryonic development using microfluidic devices are presented in [96] and [97]. A programmable and automated chip-based platform, which facilitated the accurate and reproducible *in vivo* drug dynamics and studied Zebrafish embryos is presented in [98]. Akai *et al* [99] proposed a 3D microfluidic embryo array for real-time developmental analysis of transgenic Zebrafish embryos. The PMMA chip allowed automatic loading, docking and exposure to micro- perfusion treatment of the embryo. An optomicrofluidic device that combined a light modulation system with a microfluidic circuit was developed to detect the oxygen consumption rate of a single developing Zebrafish. It was presented by Huang et al in [100]. Erickstad *et al* [101] proposed microfluidic system to observe different behavioral responses of Zebrafish larvae to different levels of hypoxia. A review of fish on chip platforms is presented in [102].

## *3 Materials for bioreactor fabrication*

A key point in the correct design of the microfluidic bioreactor is the correct selection of the materials involved in its fabrication. A detailed analysis of the materials involved in cell culturing can be found in [103]. The selection of these materials is critically connected with the application. For drug screening applications, for example, fabrication of the microfluidic reactor in glass/silicon technology can be more suitable due to the low absorption of drug and metabolites. Otherwise, for application such as cell proliferation or cell migration polymeric materials are more suitable. Three main groups of materials can be identified: polymer, silicon-based materials and metals.

### *3.1 Polymers*

Poly(methyl methacrylate) (PMMA), polycarbonate (PC), polystyrene, polyurethane, and poly(dimethyl siloxane) (PDMS) are common polymers found in microfluidic technologies [104, 105]. PDMS is the most used polymer. Soft lithography, developed by the Whitesides group [106] is usually used to fabricate PDMS devices. Advantages of PDMS include cost effectiveness, fast prototyping ability, good adhesion to glass, good gas permeability and transparency [107]. On the other hand, PDMS is a hydrophobic material. This makes it easy to absorb organic solvents, hydropho-

bic drugs and metabolites. The aspect ratio achievable with PDMS is 2:1. There are methods to enhance the surface properties of PDMS. Some of the approaches are: surfactants modification, polyelectrolyte modification, covalent modification, chemical vapor deposition, phospholipid layer modification and protein coating modification [108, 109]. Consequently, various PDMS microbioreactors have been developed for hepatocyte culture. Leclerc *et al.* developed a PDMS microbioreactor for perfusion culture of fetal human hepatocytes [110]. During the one-week perfusion period, the cells showed good attachment and proliferation. The albumin expression was higher than that of static culture by about 4 times. PDMS bioreactors have been demonstrated as a good option for large-scale hepatocyte culture due to its good gas permeability. One of the first PDMS perfusion bioreactors demonstrating large-scale culture of HepG2 was developed by Leclerc *et al* [111]. They achieved culture of HepG2 with density similar to that of a macro-scale bioreactor [49]. Cyclic olefin copolymers (COCs) have been used by Raasch *et al* [112] for manufacturing of a microfluidic devices for endothelial cell culture in order to overcome limitations of PDMS material. Besides PDMS devices, PMMA material is also commonly used in MEMS fabrication. Patterns and microchannels can easily be fabricated onto PMMA surfaces using electron beam lithography [113] or laser ablation [114].

### *3.2 Silicon-based materials*

Silicon-glass technology is one well established process for microfluidic devices [115, 116]. Their biocompatibility and applications in cell culture have been studied extensively. Silicon [117], silicon dioxide [117], silicon nitride [118-120], silicon carbide [121, 122] and SU-8 substrate [123] have all been shown to be non-cytotoxic. Amorphous silicon, for example, has been demonstrated as a good substrate for growth of renal proximal tubule cells [124, 125]. After pretreatment of ECM proteins, single-crystal silicon and polysilicon chips are shown to promote attachment of renal tubule cells. Cell functions and behaviors are also similar to cells cultured in plastic cell culture flasks. Renal cells cultured on silicon chip showed good expression of tight junction proteins like ZO-1 and high level of trans-epithelial resistance (TER), a measure of tight junction formation function [126]. Porous silicon is also frequently used in cell culture and cell adhesion studies. The surface of porous silicon can be modified by oxidation, salinization and collagen coating to promote cellular attachment. Porous silicon also has unique biodegradable property compared with single-crystal silicon, property that makes it useful for a number of *in vitro* and *in vivo* applications. For instance, porous silicon films can induce hydroxyapatite growth and promote bone healing *in vitro* [127]. Silicon nitride and silicon carbide are deposited with CVD or PECVD techniques respectively [128]. The hydrophilic property and small thickness of silicon nitride made it a good option for the study of cell-cell interaction *in vitro.* Ma *et al* developed a silicon nitride membrane for the study of blood-brain barrier (BBB) model [129]. In this model, they co-cultured endothelial cells and astrocytes on different sides of an ultra-thin silicon nitride membrane. The close proximity of the two cell types promoted cell-cell interactions and led to formation of tight cell barrier.

### *3.3 Metals*

Metals are also frequently utilized in biodevices and microfluidic bioreactors, especially for devices with electrodes and electric circuits [130]. Gold, platinum and titanium were commonly used metals for electrodes. Their biocompatibility made them safe for *in vivo* applications [131]. To enhance cell survival and tissue regeneration, Kim *et al* designed an implantable electrical bioreactor [132]. It provided electrical stimulation to the human mesenchymal stromal cells (hMSCs) seeded in the device. Cells stimulated with electrical currents showed increase in proliferation.

## *4 Conclusions*

We presented an overview of cell culture models, which in conjunction with microfluidic setup can further move the *in vitro* cell culture models towards replicas of *in vivo* environment. As practical experience, the selection between static and perfusion models is driven by the application. For liver based models for example cell functions are similar in the first week for both static and perfusion models. The difference becomes relevant after 2 weeks culture. As a result, for applications that require up to one-week cell culture the static model is more suitable. Otherwise for long-term cell culture the perfusion system is more relevant. The perfusion system is more complex and in most cases its use requires special skills. Meanwhile, the cost of the perfusion system cannot be neglected.

For the cell culture model the organization of cell in spheroids is a better mimic of *in vivo* environment. The spheroid model presents more cell-cell interaction than cell-surface interaction (characteristic of 2D models). Organ-on-a chip models start to be more and more attractive for drug screening.

The main requirements of the perfusion chip can be summarized as follows:

- conserved the cell count over the testing period,

- good mass transfer allowing diffusion of $O_2$ and nutrients from media to the cell culture model to remove the metabolites and by-products,
- low shear stress to the cells,
- low risk of contamination (reduced number of microfluidic connections, tubes and fluidic elements),
- maintenance of stable temperature and pH,
- ease to handle,
- low drug and metabolites absorption.

Coupling the spheroids cell culture model with microfluidic setup is for our point of view the future step for the long term drug screening platforms with main application on chronic toxicity testing.

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# Lithography-Free, Crystal-Based Multiresonant Lamb Waves for Reconfigurable Microparticle Manipulation

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**Abstract:** Acoustic wave microfluidic devices, in particular those that exploit the use of surface acoustic waves (SAWs), have been demonstrated as a powerful tool for driving microfluidic actuation and bioparticle manipulation. A limitation of these devices, however, is the requirement for the fabrication of interdigital transducer electrodes on the piezoelectric substrate, which upon excitation of an AC electrical signal at resonance, generates the SAW.

Not only is the lithographic fabrication a costly and cumbersome step, the necessity for driving the interdigitated transducers (IDTs) at resonance means that the device typically operates at a single frequency at its fundamental resonant state; the higher harmonics that may be available are often weak and negligible. As such, reconfiguring a device for different operating frequencies is usually difficult and almost always avoided. Here, we show a Lamb wave device which can mimic the microfluidic actuation and particle manipulation of SAW devices, but which can be fabricated without requiring any lithographic procedures. Moreover, we show that a large number of resonances are available, whose modes depends on harmonics associated with the substrate thickness, and, in particular, demonstrate this utility briefly for reconfigurable particle patterning.

**Keywords:** acoustics; microfluidics; particle manipulation; concentration

# Generiranje multi-resonančnih Lamb akustičnih valov za manipulacijo bioloških delcev

**Izvleček:** Mikrofluidne platforme ki uporabljajo za aktuacijo zvočno valovanje ter še posebej tiste, ki izkoriščajo uporabo površinskih zvočnih valov (angl surface acoustic waves - SAW.), so se izkazali kot zelo primerno orodje za manipulacijo bioloških delcev. Omejitev pri teh napravah je zahteva za izdelavo prstastih elektrod, t.j. elektroakustičnih pretvornikov na osnovni piezoelektrični podlagi, ki ob vzbujanje z izmeničnim električnim signalom v resonanci generirajo površinske akustične valovanje. Uporaba fotolitografskega postopka pri izdelavi vzbujevalne prstaste elektrodne strukture je eden bolj zahtevnih korakov. Poleg tega prstasta struktura deluje le na osnovni resonančni frekvenci, višji harmoniki, ki so lahko na voljo, pa so pogosto šibki in zanemarljivi. Preoblikovanje prstastih struktur, ki bi omogočalo delovanje na različnih delovnih frekvencah na isti mikrofluidni platformi je ponavadi težko izvedljivo in se ne uporablja. V tem prispevku bomo predstavili enostaven način generiranja Lamb valovanja, ki omogoča transport in manipulacijo bioloških delcev na piezoelektrični podlagi in ga je možno realizirati brez fotolitografskega postopka. Poleg tega bomo v prispevku pokazali, da je možna vzpostavitev različnih resonančnih frekvenc in višjih harmoničnih komponent v povezavi s spreminjanjem debeline substrata. Obenem bomo demonstrirali uporabnost takega pristopa za poljubno manipulacijo delcev.

**Ključne besede:** akustični valovi; mikrofluidika; manipulacija delcev; koncentracije

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## 1 Introduction

The ability to manipulate (e.g., concentrate, sort and separate) particulate suspensions, particularly those pertaining to biological substances such as cells, is indispensable to microfluidic operations, where applications pertaining to biomedicine and biotechnology such as point-of-care diagnostics, biosensing, drug

development, drug delivery and tissue engineering feature prominently [1-3]. Many microfluidic strategies have been proposed for manipulating such microparticles, including the use of inertia [4], electrokinetic [5], optical [6], magnetic [7] and acoustic [8] forces, among others.

While many *bulk* acoustic microfluidic methods for particle manipulation have been proposed [8], their long wavelengths associated with the kHz order frequencies typically employed, and the necessity for large ultrasonic transducers place considerable limitations to miniaturisation and integration into chip-scale devices. More recently, surface acoustic waves (SAWs), which are the high frequency (MHz order) *surface* counterpart of *bulk* ultrasonic waves, have been shown to be an extremely powerful tool for microfluidic actuation and particle manipulation [9-12]. In the latter, standing SAWs have primarily been used for trapping particles at nodal or antinodal positions in microchannels for a myriad of applications including single cell and organism focusing, patterning and separation [13,14], even in three-dimensions [15,16]. Additionally, travelling SAWs have also been recently shown to be highly useful for particle manipulation [17-19]. Besides the above, which rely on the acoustic radiation force imparted on particles to manipulate them, particle concentration and sorting have also been demonstrated by exploiting the hydrodynamic drag force imparted on the particle by SAW-driven microcentrifugation flows [20-23].

Nevertheless, high frequency (MHz order) SAWs require cumbersome processes associated with lithography, typically achieved by metal deposition, photoresist coating, UV-exposure and wet etching, in order to fabricate the interdigitated transducers (IDTs) on the piezoelectric substrate that are required to generate the SAWs. These long multi-step procedures are not only time consuming and require skilled technicians, but also involves the additional expense of operating within a cleanroom environment. Moreover, as the SAW frequency is increased closer towards GHz order [24,25], the IDT dimensions become progressively smaller given that they correlate with the SAW wavelength, necessitating even more elaborate fabrication such as electron beam or nanoimprint lithography if robust devices are desired. Furthermore, once a device is fabricated, it typically runs on a single SAW resonant frequency, thus limiting many potential microfluidic applications, especially for reconfigurable particle manipulation within liquid drops. We note the possibility of exciting multiple frequencies on a SAW device using a single tapered IDT (TIDT) design [26] (also known as slanted-finger interdigital transducers (SFITs) [27]), although the limitation with such devices is that the width of the SAW that can be produced for a given frequency is confined to a lateral dimension that is on the order of its wavelength—typically too narrow to drive any meaningful microfluidic actuation on the scale of a droplet or channel in most cases.

Here, we briefly demonstrate the possibility for on-chip reconfigurable microparticle actuation using a simple fabrication step that does not require lithographic procedures. This extends on our previous work that showed, quite counterintuitively and contrary to long-standing practice, that it is possible to generate Lamb waves for microfluidic actuation on a piezoelectric (lithium niobate; $LiNbO_3$) substrate simply with the use of aluminium foil placed in contact with the substrate [28-30].

## 2 Method

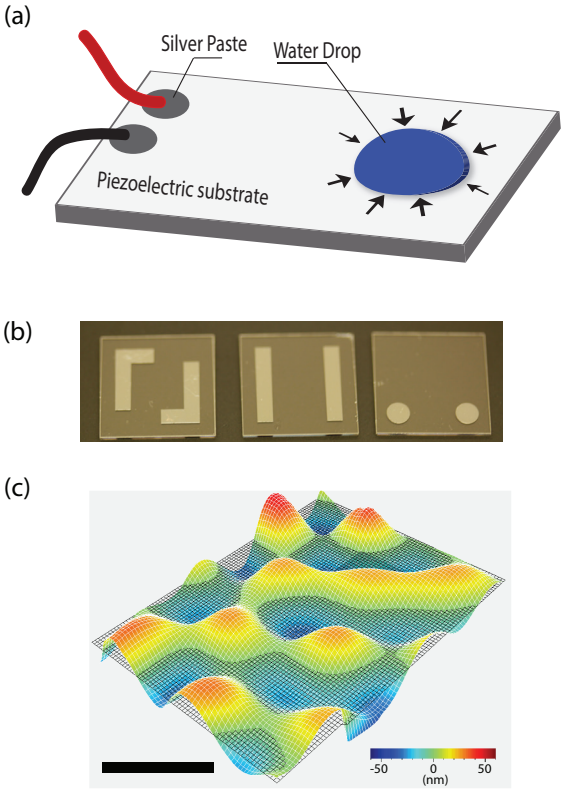


**Figure 1:** (a) Schematic illustration and (b) images of various electrode patterns on the lithography-free $LiNbO_3$ chip. (c) Laser Doppler Vibrometer (LDV) scan of the chip at 3.5 MHz; the scale bar denotes a length of approximately 1 mm.

The simple lithography-free setup is shown schematically in Figure 1a, wherein either conductive silver paste was spotted, or an arbitrary electrode pattern (such as the straight, L-shaped or circular patterns in

Figure 1b) comprising a conductive aluminium layer deposited with the aid of masking tape, onto the $LiNbO_3$ chip. To generate the Lamb wave in the substrate, we simply connect these electrodes to an AC source at an appropriate resonant frequency, a number of which exists, as will be discussed below. To demonstrate the possibility for reconfigurable microparticle manipulation, we placed a 5 µl sessile liquid drop comprising 3 µm polystyrene particles suspended in water at a concentration of $10^5$ onto the device and observe its behaviour as a function of the applied frequency using a DSLR camera (Canon D50, Tokyo, Japan) which was connected to a long working distance microscopic lens (K2/SC, Infinity, Boulder, CO). The mechanical vibration displacement was acquired using laser Doppler vibrometry (LDV; MSA-400 and UHF-120; Polytec, Germany) whereas electrical characteristics of the device, namely the insertion loss parameter $S_{11}$, was measured using a vector network analyser (VNA; ZNB4, Rohde & Schwarz, Germany).

## 3 Results & Discussion

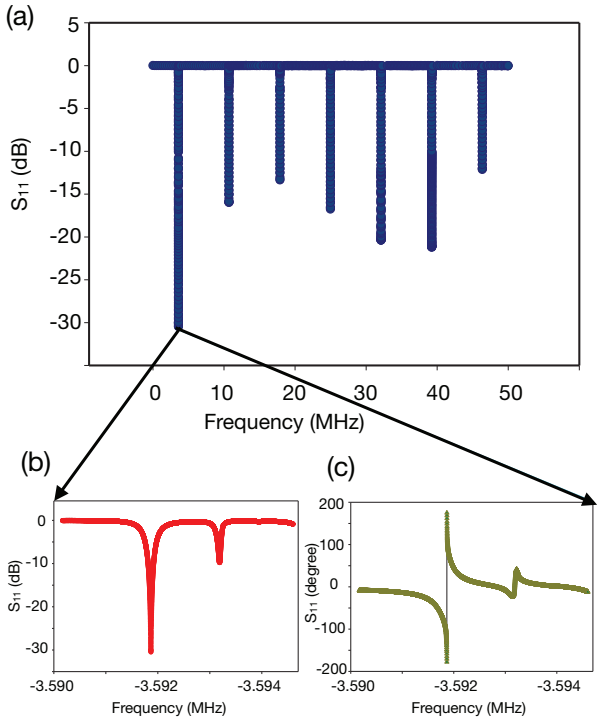


**Figure 2:** (a) Results from the VNA frequency sweep to measure the insertion loss parameter $S_{11}$ of the device, which clearly shows multiple resonances starting from the fundamental resonance at 3.5 MHz, as determined from the magnification of (b) the magnitude and (c) the phase angle, and higher harmonics at every additional 7 MHz.

The VNA measurement for the insertion loss parameter $S_{11}$ in Figure 2 shows that the device possesses multiple resonant frequencies, starting from the fundamental frequency at 3.5 MHz, and additional higher resonant modes at increments of approximately every 7 MHz. While we only show results for the frequency sweep across a range from 1 to 50 MHz in Figure 2 for clarity, discernible resonant peaks were observed even beyond 300 MHz. It is worth noting, that these resonances are insensitive to the electrode shape (dot, straight, L-shaped, circular, etc.) or their dimension, since the electric field, which is coupled to the mechanical field, traverses *vertically* through the chip thickness; the resonances are therefore only sensitive to the thickness of the substrate. Reducing this by lapping the device using a rotating wheel covered with abrasive slurry led to increases in the fundamental resonant frequency. In particular, given the speed of sound through $LiNbO_3$ $c$ = 3500 m/s and for a substrate thickness $T$ = 500 µm, the fundamental resonant frequency that arises can be computed from $f = \lambda c$ in which the wavelength $\lambda/2$ corresponds to $T$ such that $f$ = 3.5 MHz. Subsequent higher harmonics can then be obtained for $3\lambda/2$, $5\lambda/2,\ldots,(2n+1)\lambda/2$ ($n = 0, 1, 2,\ldots$) leading to resonances at every interval of 7 MHz, i.e., 10.5 MHz, 17.5 MHz,…, etc.

We also note that the proposed chip configuration in Figure 1 possesses an outstanding quality factor $Q$ of approximately 13,000 (in contrast to that of typical SAW devices where $Q$ factors as low as 100 are not uncommon), which not only makes it a very efficient device for microfluidic manipulation, as will describe later, but also renders it as a very sensitive platform for biosensing. Given the optical smoothness of the $LiNbO_3$ substrate and the uniformity of its thickness, which sets the wavelength, it is perhaps of little surprise that the resonant band (and hence the high quality factor) is very sharp and almost comparable to those of quartz crystals. Such crystals with high quality factor, although extremely sensitive to mass loading (which makes them very efficient sensors), however possess extremely low electromechanical coupling coefficients $k_t^2$, and therefore, a low figure of merit FOM = $Qk_t^2$. Remarkably, however, the present device, when excited at the fundamental resonant frequency, shows a reasonable value for $k_t^2$ of 0.8%. Although other piezoelectric substrates such as lead zirconium titanate (PZT) possess $k_t^2$ values up to 20%, we note that the FOM = 13,000 x 0.8% ≈ 10,000 surpasses any other piezoelectric material we know of; for example, a typical SAW on 128 YX $LiNbO_3$ with $Q \approx 100$ and $k_t^2 = 5.3\%$, has an FOM ≈ 500, considerably below that here. This suggests that the Lamb wave device is not just simple and low cost to fabricate, but also satisfies a rare requirement for any

piezoelectric substrate of being *both* a very sensitive as well as a very effective actuator.

Upon excitation of the device at the fundamental resonant frequency, i.e., 3.5 MHz, standing Lamb waves in the form of a checkerboard pattern are generated in the device with a wavelength of 1000 μm as seen in Figure 1c. We note that the presence of the liquid drop will distort this standing wave pattern due to its mass loading given that the liquid thus acts as a sink in absorbing the waves along its circular periphery [29]. Unlike previous investigations where we showed that these Lamb waves led to the generation of poloidal flows in the drop, which, in turn gave rise to the formation of toroidal particle rings [29,30], the low excitation powers (<50 mW) primarily used in this study rendered acoustic streaming in the drop insignificant, and, as such, the particles suspended in the liquid were only subjected to acoustic radiation forces instead of the dominant hydrodynamic drag.

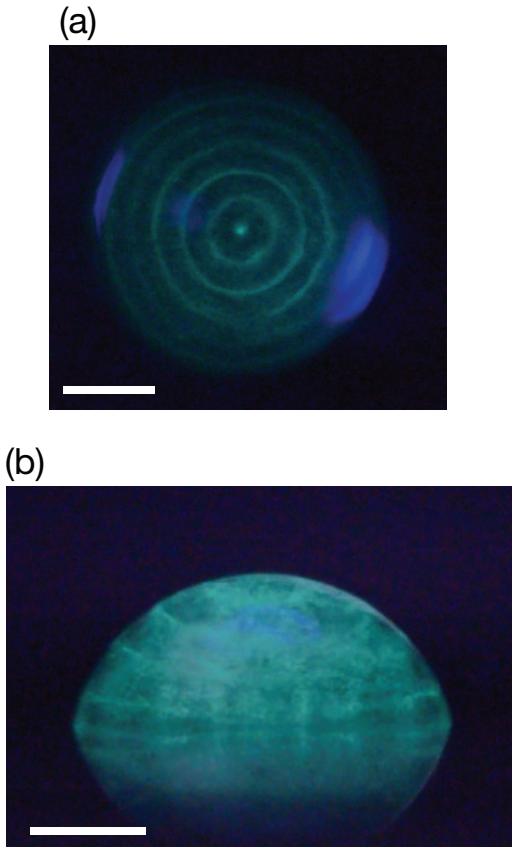


**Figure 3:** (a) Top and (b) side view of the three-dimensional concentric particle patterns that arise under Lamb wave substrate excitation of a 5 μl sessile liquid drop comprising 3 μm particles suspended in water at the fundamental resonant frequency, i.e., 3.5 MHz. The spacing between the concentric rings is approximately 270 μm. Scale bars denote a length of approximately 1 mm.

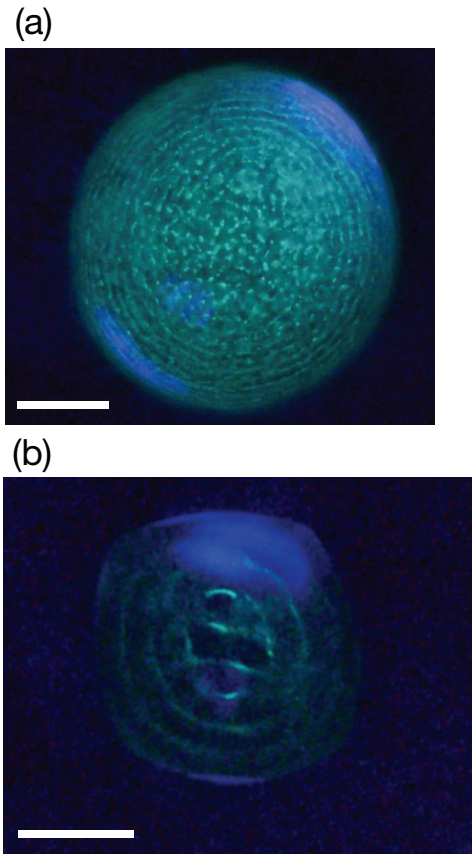


**Figure 4:** Top view of the three-dimensional concentric particle patterns that arise under Lamb wave substrate excitation of (a) a circular, and, (b) a roughly square 5 μl sessile liquid drop comprising 3 μm particles suspended in water at 10.5 MHz. The spacing between the concentric rings is approximately 90 μm. Scale bars denote a length of typically 1 mm.

Figure 3 shows the resultant particle patterns that arise on the free surface of the drop as well as within its bulk due to their alignment along nodal lines or planes of the standing acoustic wave that is generated as a consequence of the radiation force it imparts on the particles; the standing wave arising due to the reflections at the drop boundaries. The concentric patterns, in particular, reflect the radial nodes associated with the breathing mode of the drop, and the 270 μm spacing between the concentric particle rings correspond to a separation length of λ/2, as expected.

What distinguishes the present devices from other acoustic devices, however, is the possibility of triggering a large number of higher harmonic frequencies with reasonable efficiency, thus allowing the possibility of reconfiguring the spacing and assembly of the particle patterns *in situ*. As a brief example, Figure 4a shows the concentric particle patterns when a higher harmonic (10.5 MHz) is excited in the same device

wherein the spacing between the concentric rings has decreased to approximately 90 μm, again corresponding to λ /2 at this harmonic frequency. Higher harmonics led to smaller spacing, although the pattern cannot be resolved spatially while imaging the whole drop and is hence not shown. Such reconfigurability is in sharp contrast to SAW devices, whose excitation relies on the IDT dimensions, or bulk acoustic wave (BAW) devices in which the excitation is achieved by coating electrodes on the top and bottom surface of the piezoelectric ceramic, e.g., PZT. In those cases, the resonant excitation is predominantly limited to the fundamental resonant frequency set by the IDT (in the case of the SAW) or the substrate thickness (in the case of the bulk piston vibration). Although, theoretically, PZT can support higher harmonics effectively, the poor surface roughness of the material leads to much broader resonance (and hence low *Q* of approximately 100 and even down to about 10) for the higher harmonics, and therefore the coupling is extremely ineffective.

To illustrate that the standing waves within the drop that arise due to the reflection off its boundaries, and that it is these that assume the dominant role in determining the particle pattern rather than the underlying vibration pattern on the substrate, we rendered the $LiNbO_3$ substrate surface hydrophobic (with a Teflon coating) save for a roughly square region (with the aid of a mask during coating) on which we placed the drop. As seen in Figure 4b, the resulting particle pattern within the roughly square shaped drop is altered and closely resembles the drop contour.

Finally, we demonstrate the possibility of efficiently generating acoustic streaming, and, in particular, microcentrifugation flows, in these devices even at these higher harmonics, which cannot be achieved either using the SAW or BAW devices given the extremely weak higher harmonics in those devices, particularly given the ineffective higher harmonic coupling evident (both *Q* and $k_t^2$ exponentially decay with frequency). Figure 5 shows the particle concentration as a consequence of the azimuthal acoustic (Eckart) streaming within the drop, whose underlying mechanism we have discussed elsewhere [20-23], when the substrate is excited at much higher harmonics, i.e., 150 MHz, at large applied powers (approximately 500 mW) that give rise to larger substrate vibration displacements. In addition to the large streaming velocities, typically on the order of 0.5–1 mm/s observed, it can be seen that the bipolar vortex gave rise to particle concentration in two distinct islands. The ability to trigger these higher frequencies even with such a simple device then constitutes a considerable advantage given the need to date for elaborate lithographic procedures (e.g., electron beam or nanoimprint lithography) to fabricate sufficiently robust electrodes for high frequency operation [24,25].

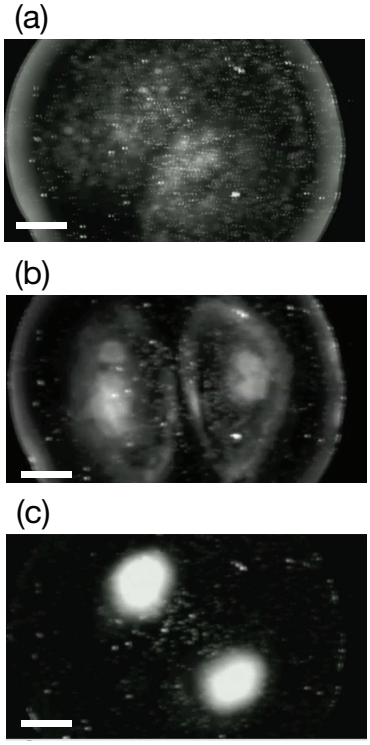


**Figure 5:** Bipolar vortex acoustic streaming flow is generated in a 5 μl sessile liquid drop comprising 3 μm particles suspended in water by exciting vibration in the substrate at a harmonic resonant frequency of 150 MHz with large input powers (approximately 500 mW). This leads to rapid concentration of the particles into two particle islands through particle shear induced migration [20-23]. The left image (a) shows the drop prior to excitation at time $t = 0$ wherein the particles are dispersed throughout the drop, the centre image (b) shows the bipolar vortices in the drop at $t = 1$ s during Lamb wave excitation, and the right image (c) shows the drop immediately after excitation at $t = 5$ s wherein the particles have concentrated and the substrate vibration relaxed. Scale bars denote lengths of approximately 0.5 mm.

## 4 Conclusion

By exploiting the large number of resonances associated with the Lamb wave vibration through the thickness of a substrate comprising a piezoelectric material, namely, lithium niobate, and its extremely high quality factor and hence figure of merit, we show the possibility of reconfigurable microfluidic actuation and particle manipulation on a single device. In doing so, we not only demonstrate the possibility of replicating the capabilities of surface acoustic wave devices with a simple electrode design that does not require lithographic

processes for fabrication but also circumvents the need for distinct devices whenever a different frequency and hence wavelength is desired.

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# Microfluidics-Directed Self-Assembly of DNA-Based Nanoparticles

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**Abstract:** The 'bottom-up' paradigm of nanofabrication mostly relies on molecular self-assembly, a process by which individual components spontaneously form ordered structures with emerging functions. Soft nanoparticles made up of therapeutic DNA condensed by cationic lipids or surfactants hold a great potential for nonviral gene delivery. Their self-assembly is driven by strong electrostatic interactions. As a consequence, nanoparticles formulated in bulk often exhibit broad size distributions not suitable for practical delivery applications. We will review the recent strategies we developed to control the self-assembly kinetics by using microfluidic devices. This combined approach may open attractive opportunities for the directed self-assembly of complex soft nanomaterials in particular for biomedical purposes.

**Keywords:** microfluidics; self-assembly; DNA; nanoparticle; nonviral gene delivery

# Nadzorovano samourejanje DNA nanodelcev na osnovi mikrofluidike

**Izvleček:** Paradigma nanoizdelave „od spodaj navzgor" (angl. 'bottom-up') v glavnem temelji na molekularni samosestavljanju oziroma samourejanju, to je procesu, s katerim posamezne komponente spontano tvorijo urejene strukture s specifičnimi funkcijami. Mehki nanodelci, sestavljeni iz terapevtskih DNK, dobljenih z metodo kondenzacije kationskih lipidov ali površinsko aktivacijskih snovi (surfaktantov), predstavljajo velik potencial za nevirusno dostavo in vnos genov. Njihovo samourejanje je posledica močne elektrostatične interakcije. Posledica tega je, da imajo nanodelci, ki s samourejanjem tvorijo kompleksne strukture, pogosto široko porazdelitev velikosti, kar pa ni vedno primerno za praktične aplikacije. V članku je podan pregled razvoja novih strategij za nadzorovan proces kinetike samourejanja s pomočjo uvedbe mikrofluidnih pristopov, s katerimi lahko odpravimo zgornjo pomanjkljivost. Predstavljeni novi kombinirani pristopi omogočajo kontrolirano samo-sestavljanje kompleksnih mehkih nanomaterialov, zlasti primernih za biomedicinske namene.

**Ključne besede:** mikrofluidika; nanodelci; samourejanje; DNA; nevirusni vnos genov

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## 1 Introduction

Microfluidics is a developing field with applications covering tissue engineering [1-3], cell analysis [4-7], drug discovery [8-9], bioassays [10] and chemical synthesis [11-15]. Technology has arrived at a stage where it is now possible to handle and to shape the molecular constituents of matter with nanometer accuracy, whether they are inorganic or biological. As George M. Whitesides put it [16], "the physical sciences offer tools for synthesis and fabrication of devices for measuring the characteristics of cells and sub-cellular components, and of materials useful in cell and molecular biology; biology offers a window into the most sophisticated collection of functional nanostructures that exists." Two paradigms have emerged for the fabrication of nanometer-scaled materials: the 'top-down' approach – widely used in the microelectronics industry through lithography – enables to pattern bulk materials such as silicon with features size down to one nanometer and with high batch-to-batch repeatability. The technol-

ogy is limited so far to two-dimensional structures at the surface of a substrate. The 'bottom-up' approach in turn has been successfully exploited by nature to build up the most complex systems with high throughput, namely, living organisms. The limitation mostly arises from our inability to tune the interactions between constituents in such a way that they self-assemble into desired structures in a repeatable manner. Our present scientific knowledge gives us access to only a small set of architectures and functions, while nature has benefited from billion years of evolution to learn how to make the most elaborate devices such as the human brain with a low error rate. A third paradigm is subsequently emerging and consists of combining the two others. In other words, it aims at fabricating complex three-dimensional structures via self-assembly with high reproducibility.

DNA-based nanoparticles are such complex structures and hold a great potential in medicine. Their architecture and their function are inspired from virus in the sense that they carry genetic information encoded in compacted nucleic acids – either DNA or RNA – in view of its delivery into target cells [17]. As a matter of fact, a number of viruses have been engineered in such a way that they deliver therapeutic genes with the efficiency of a viral infection. Indeed, the regular function of a virus is to inject its genes into an infected cell, which will then express viral proteins and nucleic acids to make up new viruses. The strength of viruses is that they can circulate inside an organism while being not recognized by the immune system and targeting specific cells. However, they can induce inflammatory responses and provoke cancer through uncontrolled gene insertion. By contrast, nonviral vectors are safer and more versatile than engineered viruses, even though their efficacy is still insufficient. The objective of nonviral gene delivery [18] is therefore to devise nanometer-scaled synthetic particles containing nucleic acids to deliver into specific cells with high efficacy. The particles must be nontoxic, easy to fabricate, and with excellent batch-to-batch repeatability.

This article reviews our recent works on the self-assembly of DNA-based nanoparticles for use in nonviral gene delivery. It shows in particular how the third paradigm of nanofabrication can be used through different microfluidic strategies to produce surfactant-DNA nanoparticles with a good control on their morphological properties.

## *2 Supramolecular structure: the case of lipid-DNA nanoparticles*

The architecture of simple viruses consists of the genome encoded in nucleic acids, which are compacted and protected inside a protein shell called the capsid. Remarkably, the capsid alone [19] or the capsid with genome [20] can self-assemble *in vitro* from purified components. Nonviral DNA-based nanoparticles try to mimic this architecture. Likewise, they result from a self-assembly process, which is driven by a delicate balance between weak (H bond, hydrophobicity, entropic effects) and strong (electrostatics, van der Waals forces) noncovalent interactions [21]. DNA is a negatively-charged polyelectrolyte and undergoes a coil-globule transition upon the addition of positively-charged agents, which can be synthetic polyelectrolytes, peptides, lipids or surfactants. This compaction process can be further enhanced by attractive interactions between positively-charged agents via hydrophobic forces as is the case with the alkyl chains of lipids and surfactants. Resultantly, the self-assembly of such DNA-based nanoparticles is driven both by electrostatics and by hydrophobic interactions, and it can give rise to a rich phase diagram.

Lipids have played an important role in nonviral gene delivery because they are the main constituents of cell membranes. A lipid-based vector has thereby the ability to fuse with the membranes of host cells and to release efficiently its DNA. Lipids are organic molecules made up of a hydrophilic charged head and a hydrophobic alkyl tail [22]. When dispersed in water, they self-assemble into 4~5 nm-thick bilayers in such a way that the alkyl tails are protected from the aqueous environment. At high volume fractions, the bilayers become stacked into a lamellar phase denoted $L_a$. More importantly, when cationic lipids are mixed with DNA, they form nanoparticles with local liquid-crystal order. Depending on the shape of the lipid molecule, i.e., cylindrical or conical, we mostly observe complexed lamellar $L_a^C$ and complexed inverted hexagonal $H_{II}^C$ phases [22]. The $L_a^C$ phase consists of alternating monolayers of DNA rods and lipid bilayers. In the $H_{II}^C$ phase, DNA rods are coated by a lipid monolayer and arranged on a two-dimensional hexagonal lattice. Very interestingly, lipid-DNA nanoparticles in $H_{II}^C$ phase transfer their DNA to cells much more efficiently than those in $L_a^C$ phase. However, cationic lipids are toxic to cells because they interact strongly with the negatively-charged membranes and disturb their biological functions. An alternative option is to use natural anionic lipids associated with DNA via multivalent cations [23]. The cations, in weak amounts, are intercalated between lipids and DNA [24], and the complexed lamellar and inverted hexagonal phases are recovered. The transfer efficiency of DNA is similar to that obtained with cationic lipids but the toxicity level is significantly lower.

At large scale, lipid-DNA nanoparticles exhibit a certain degree of disorder. When cationic lipids and DNA are

mixed manually in a test tube, the typical size of the resulting nanoparticles ranges from 30 to 500 nm and each nanoparticle contain plenty of DNA chains. Cryo-transmission electron microscopy images of $H_{II}^{C}$ lipid-DNA nanoparticles revealed a local hexagonal packing of DNA [25]. However, we could also see striations, which were hexagonal bundles of DNA bent under the collapsing effect of hydrophobic interactions, and which suggested that DNA bundles took different orientations within the nanoparticles (Figure 1).

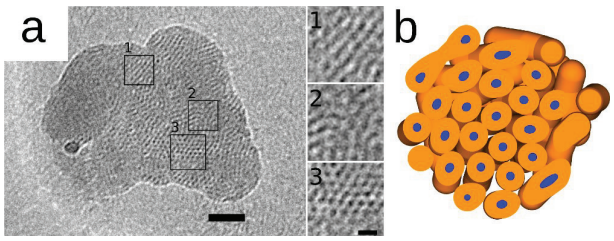


**Figure 1:** (a) Cryotransmission electron micrograph of a single lipid-DNA nanoparticle. The scale bar of the large view is 50 nm and that of the magnified views is 10 nm. (b) Cross-section of a coarse-grained model of a lipid-DNA nanoparticle calculated by Monte Carlo simulation. DNA is represented in blue and lipids in orange. Adapted with permission from [25] and [26]. Copyright 2011-2012 American Chemical Society.

The morphological properties of lipid-DNA nanoparticles affect their transfer efficiency. Large particles (>200 nm) cannot penetrate deeply into tissues and are less prone to be internalized into cells by endocytosis. Besides, high degree of local order is related to large internal energy and to thermodynamic state close to equilibrium. As a result, the nanoparticles are very stable and do not release their DNA readily inside the host cells. The transfer efficiency is therefore low. This trend is generic and was reported also with polyelectrolyte-DNA nanoparticles for which small size and internal disorder yielded high transfer efficiency [27].

## *3 Control of the mixing kinetics by hydrodynamic flow focusing*

DNA-based nanoparticles with large size are not suitable for *in vivo* gene delivery for three reasons [28]: (i) they have poor circulation properties and are easily recognized by the immune system; (ii) the hydrodynamic and shear forces are greater and subsequently work against attachment to cell membrane; and (iii) they cannot penetrate deeply into tissues. Furthermore, high polydispersity of nanoparticle size gives rise to nonrepeatable results. Consequently, there is a need to develop methodologies enabling to control finely the morphology and the size distribution of DNA-based nanoparticles. Since the self-assembly process involves molecules interacting at the nanoscale, microfluidic devices are well suited for controlling the kinetics of mixing between DNA and condensing agents. Through the control of the mixing kinetics, the size distribution of the resulting nanoparticles can be tuned with a better flexibility than manually in bulk (Figure 2).

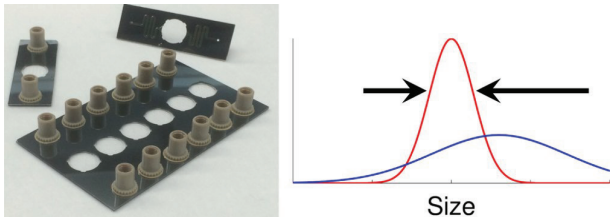


**Figure 2:** Illustration on the use of microfluidic devices (left) for the control of the size distribution of DNA-based nanoparticles (right).

In a seminal article, Johnson and Prud'homme [29] demonstrated that the time for a solution of copolymer in a good solvent to be mixed with a poor solvent, could control the diameter of the resulting micelles. More precisely, they reported that when the mixing time $\tau_{mix}$, which is the typical timescale for homogenizing the solvents, was shorter than the aggregation time $\tau_{agg}$, which is the average time for a copolymer molecule to diffuse and bind to another one, the diameter of micelles was minimal. Above $\tau_{agg}$, the diameter increased as a power law of $\tau_{mix}$. $\tau_{agg}$ was around 40 ms and to achieve mixing times smaller than this value, the investigators used a turbulent mixer. For applications involving DNA or other fragile macromolecules, turbulent mixer is not suitable because the applied shear stress is so strong that it tears apart the molecules and breaks them into small pieces. That is why Karnik and coworkers [30] used hydrodynamic flow focusing in a microfluidic device to achieve millisecond mixing times. The principle is depicted on Figure 3: a central stream containing copolymer is focused by two lateral streams of poor solvent. As a result, the poor solvent diffuses through the focused central stream within a timescale that can be tuned through the flow rates. Assuming that the fluids are incompressible and the flows laminar, the mixing time can be approximated by [31]

$$\tau_{mix} \approx \frac{w_o^2}{9(1+R)^2 D_s} \quad (1)$$

where $R=2Q_B/Q_A$ is the flow rate ratio and $D_s$ the diffusion coefficient of the poor solvent or of the molecules to mix. In a microfluidic device, the width of the outlet stream $w_o$ can be typically 60 µm or less, the flow rate ratio $R$ is at least 10 for a good focusing effect and $D_s$, in the case of pure water, is $10^{-9}$ m$^2$.s$^{-1}$, which yields a mix-

ing time of 3.3 ms. As a rule of thumb, the aggregation time can be estimated from the diffusion-limited reaction rate between the associating molecules,

$$\tau_{agg}^{-1} \approx 16\pi\rho D R_H \quad (2)$$

where $r$ denotes the density of the molecules, $D$ their diffusion coefficient and $R_H$ their hydrodynamic radius. The product of the two last quantities is given by the Stokes-Einstein relationship, i.e., $DR_H=k_BT/6\pi\eta$, with $k_B$ the Boltzmann constant, $T$ the temperature, and η the viscosity of the solvent. For molecules at a density of $10^{19}$ $m^{-3}$ dispersed in pure water (η≈ 1 mPas at 20 °C), the aggregation time is around 9 ms.

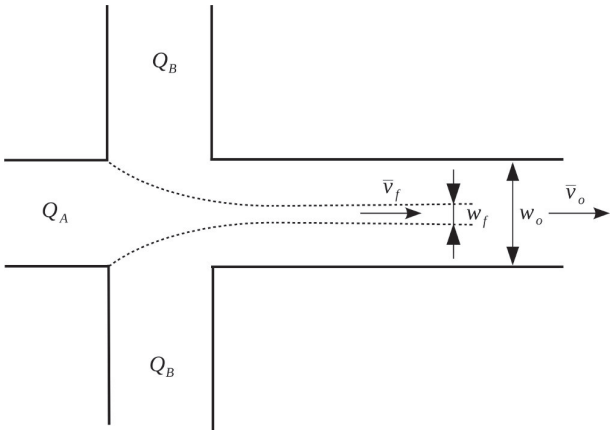


**Figure 3:** Schematic illustration of hydrodynamic flow focusing in a microfluidic device. $Q_A$ and $Q_B$ are the flow rates of the central and lateral streams respectively, $w_f$ and $w_o$ denote the width of the focused and outlet streams, and $v_f$ and $v_o$ are the average flow velocities in the focused and outlet streams. Adapted with permission from [31]. Copyright 2014 American Chemical Society.

We have exploited hydrodynamic flow focusing for the self-assembly of DNA-based nanoparticles. Unlike copolymers in poor solvent, the association of DNA with condensing agents is driven by strong electrostatic interactions, which, in bulk, lead to kinetic traps and metastable states with broad size distributions of nanoparticles. The microfluidic strategy ensured homogeneous electrostatic attractions at the mixing interface between DNA and condensing agents in addition to a good control over the mixing time. We designed and fabricated a series of microfluidic devices with different layouts in order to achieve either a rapid or a slow mixing. The device structure was generic and is depicted on Figure 4. We opted for a combination of glass and silicon rather than poly(dimethylsiloxane) (PDMS) because the channels were thus hydrophilic, which minimized the nonspecific interactions with the alkyl chains of condensing agents. The microfluidic structure was patterned in a silicon die by deep reactive ion etching and the channels were sealed by bonding a glass die on the top of the silicon die. Prior to sealing, a 150 nm-thick $SiO_2$ layer was thermally grown on the silicon so as to produce a hydrophilic surface. The flow rates were adjusted by a MFCS-FLEX pumping system (Fluigent, France) equipped with a mass flow controller for each channel.

The principle was validated on the self-assembly of cationic surfactants (dodecyl trimethylammonium bromide; DTAB) with semi-flexible anionic polyelectrolyte (sodium carboxylmethylcellulose; carboxyMC) [32]. Numerical calculations solving the Cauchy equation of motion in three-dimensional geometry confirmed that the width of the focused stream scaled as $(1+R)^2$ as predicted analytically. Instead of focusing the central stream from the two lateral sides, we also tried to focus it from only one side. In that case, the mixing time varies differently with the flow rate ratio and we can demonstrate that it scales as $\tau_{mix} \infty R^{-1}$. Therefore, we carried out microfluidic-directed self-assembly of DTAB-carboxyMC nanoparticles in the two configurations, with carboxyMC flowing in the central stream and DTAB flowing in the lateral streams. Remarkably, we observed that the nanoparticle sizes were systematically smaller when the central stream was focused from two lateral sides, which was in good agreement with the fact that the mixing time was much shorter for any given $R$. Unfortunately, this method failed to compact efficiently DNA and the nanoparticle sizes were always larger than 100 nm. This was due to the fact that the lin-

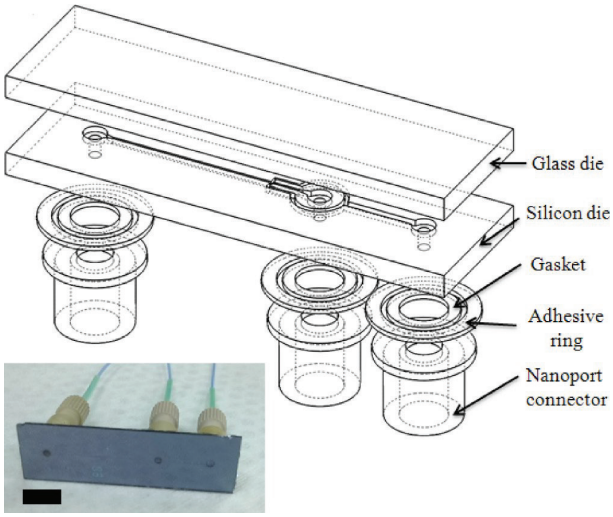


**Figure 4:** Microfluidic device for hydrodynamic flow focusing with an exploded view showing the various parts made in a combination of glass and silicon. The photograph shows the bottom of the device. The scale bar is 1 cm. Adapted with permission from [32]. Copyright 2013 American Chemical Society.

ear charge density of DNA is more than twice as large as that of carboxyMC. The surfactants were strongly attracted by DNA and the aggregation time was consequently shorter than in the case of carboxyMC. As a result, the process gave rise to large nanoparticles with uncontrolled size distribution.

## 4 Towards monomolecular DNA-based nanoparticles

Consequently, we adopted an alternative method: since the aggregation time was reduced with DNA, we had to find a way to shorten further the mixing time. The diffusion coefficient *Ds* appearing in Equation 1 is that of the solvent or of the molecules in the lateral streams. When DNA was compacted by surfactants in the lateral streams, $\tau_{mix}$ was a few tens of milliseconds because surfactants diffused slowly through the focused stream ($Ds \sim 10^{-10}$ m$^2$/s). We therefore pre-mixed DTAB and DNA in 35% ethanol in such a way that surfactants were loosely bound to DNA without compacting it. Indeed, 35% ethanol is a good solvent for DTAB, which does not form micelles at our working concentrations (~1-10 mM). By rapid mixing with pure water, surfactant-bound DNA molecules collapsed into globules due to the change of solvent quality, just like the copolymers mentioned before [30]. Since the diffusion coefficient of pure water was an order of magnitude higher ($Ds \sim 10^{-9}$ m$^2$/s) than that of surfactants, we could achieve a mixing time of a few milliseconds. The nanoparticle size was generally below 100 nm for a broad range of DNA concentrations [31]. The polydispersity index measured by dynamic light scattering was lower than 0.2 and sometimes below 0.1, which indicated a good monodispersity of the nanoparticles. However, a monomolecular DNA-based nanoparticle, that is, which contains only a single DNA chain of a few thousands of base pairs, should be around 30 nm in size. This method was therefore not efficient enough to produce the smallest nanoparticles permitted in theory.

In the last approach, we proceeded by increasing dramatically the aggregation time [33]. Instead of associating rapidly DNA and surfactants, the two reactants diffused slowly through a stream of pure water (Figure 5a). As a result, they encountered each other almost one molecule at a time, as if they were in a very dilute regime. Nanoparticle sizes as small as 30 nm and with a polydispersity index below 0.1 were obtained as shown on Figure 5b. By raising the surfactant flow rate from 20 µL/min to 35 µL/min – the water flow rate being fixed at 50 µL/min – the nanoparticle size increased in an exponential manner. Similarly, we observed a very strong effect of the surfactant concentration: below 5 mM of DTAB, the nanoparticle size was smaller than 80 nm but at 7 mM, the nanoparticle size was close to 600 nm. These findings emphasized the sensitivity of the assembled nanoparticles on the initial conditions: a small variation of concentration can have dramatic effects on the morphology. They fully justify the use of elaborate methods based on microfluidics.

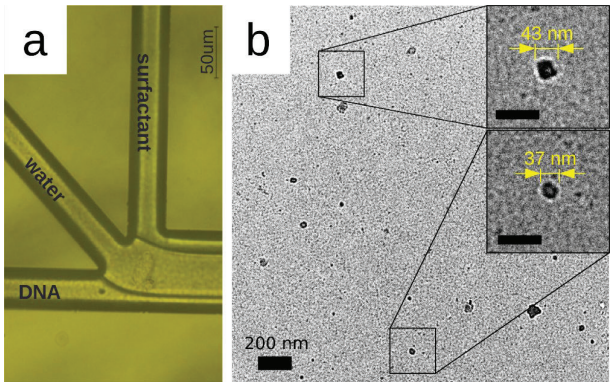


**Figure 5:** Assembly of DNA-based nanoparticles by slow diffusion. (a) Optical image of the microfluidic device. (b) Transmission electron microscopy images of DTAB-DNA nanoparticles. The scale bars of insets are 100 nm. Adapted with permission from [33]. Copyright 2015 American Chemical Society.

## 5 Conclusion

DNA-based nanoparticles play an important role in biomedical sciences as vectors for nonviral gene delivery. Their efficiency of gene transfer strongly depends on their morphological properties. In particular, small size allows them to diffuse deeply into tissues and not to be recognized by the immune system, while a narrow polydispersity ensures a good batch-to-batch reproducibility. Formulation in bulk does not respond satisfactorily to these criteria and elaborate strategies are therefore necessary to achieving a fine control over the size distribution.

If DNA-based nanoparticles result from a self-assembly process, further control can be obtained by using microfluidics, and accordingly, by taking advantage of the third paradigm of nanofabrication, which combines 'bottom-up' and 'top-down' approaches. Microfluidics enables to direct the self-assembly by tuning the convective-diffusive mixing of reactants at the nanoscale. The resulting objects are kinetically frozen and trapped in nonequilibrium state. They still evolve but over timescale sufficiently long (several days) with respect to the time required for a typical gene deliv-

ery experiment (several hours). Thereby, we devised a series of microfluidic devices based on hydrodynamic flow focusing, which allowed us to finely tune the mixing kinetics of DNA with surfactants. We managed to obtain surfactant-DNA nanoparticle size as small as 30 nm with a good monodispersity, which means that only one or two DNA molecules were packaged within each nanoparticle.

The microfluidics strategy is versatile and can presumably be applied to any complex soft nanomaterials. By following different kinetic pathways, we can access a wide range of states – albeit metastable – and produce nanomaterials with structures and functionalities that cannot be obtained solely at equilibrium. It also opens up the route to elaborate assembly schemes where multicomponent nanoparticles can be assembled sequentially within a microfluidic 'factory' on chip.

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# *Effect of a new methacrylic monomer on diode parameters of Ag/p-Si Schottky contact*

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**Abstract:** 1-[4-(prop-2-yn-1-yloxy)phenyl]ethanone-O-methacryloyloxime (POEMO) is a new methacrylic monomer with side chain alkyne. In this study, Ag/POEMO/p-Si Schottky metal-interlayer-semiconductor (MIS) diode was fabricated and its diode parameters were investigated. Using the forward bias current-voltage (I-V) characteristic, the ideality factor and barrier height of the MIS structure were found as 2.81 and 0.70 eV, respectively. The barrier height value of 0.70 eV obtained for Ag/POEMO/p-Si MIS diode was higher than the value of 0.64 of conventional Ag/p-Si Schottky diode. Cheung-Cheung and Norde methods were also used to extract ideality factor, barrier height and series resistance values, and the obtained results were compared.

**Keywords:** Schottky diode; electrical characterization; methacrylic monomer.

# *Vpliv novega metakrilnega monomera na diodne parameter Ag/p-Si Schottky kontakta*

**Izvleček:** 1-[4-(prop-2-yn-1-yloxy)phenyl]ethanone-O-methacryloyloxime (POEMO) je nov metakrilni monomer s stransko alkilno verigo. V tem delu smo izdelali in analizirali lastnosti Ag/POEMO/p-Si Schottky-jeve MIS (kovina-vmesna plast-polprevodnik) diode. Idealni faktor in višina bariere diode pri priključeni prevodni napetosti je 2.81 in 0.70 eV. Dobljena višina bariere v dani strukturi je višja od 0.64 eV pri klasični Schottky-jevi diodi. Za natančno določitev idealnega faktorja, višine bariere in serijske upornosti smo uporabili Cheung-Cheung in Norde metodi. Rezultate obeh metod smo medsebojno primerjali.

**Ključne besede:** Schottky-jeva diode; električna karakterizacija; metakrični monomer

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## *1 Introduction*

Organic electronic has drawn significant attention due to interesting optical, electrical, photoelectric, and magnetic properties of organic materials in the solid state. The advantages of thin-film formation, light weight, large area and mechanical flexibility provided by organic materials are other reasons of this increasing interest [1]. Furthermore, organic chemistry can tailor the materials properties according to the demand. Electronic devices based on organic materials have found a wide variety of applications including; light emitting diode, organic field effect transistor, Schottky diode, photovoltaic and solar cells [2, 3].

The metal/semiconductor (MS) contacts have crucial importance in electronic devices. However, many of these contacts are not fabricated as barely MS contacts; they are fabricated as metal-interlayer-semiconductor (MIS) contacts [4]. MIS structures are fabricated by covering a semiconductor substrate with an organic/inorganic layer on which a metal electrode is deposited. In an MS contact, the characteristic quantity is the Schottky barrier height which measures the energy distance between the Fermi level and the edge of respective majority carrier band of the semiconductor at the interface. The barrier height of an MS contact can be modified by inserting an interlayer between the metal and

the semiconductor. Therefore, numerous studies have been carried out to implement barrier height modification using organic/inorganic interlayer. In these studies, either increasing or decreasing of the barrier height have been reported [5-9].

The ability of acrylic monomers in copolymerizing to produce variety of structures make it possible to produce the desired properties for a wide range of applications. Therefore, methacrylate polymers are one of the most important commercial polymers [10]. 1-[4-(prop-2-yn-1-yloxy)phenyl]ethanone-O-methacryloyloxime (POEMO) is a new functional methacrylic monomer with side chain alkynes [11]. It is thought that investigation of further application areas for this new methacrylate monomer bearing an important group such as alkynes would be useful. For example, using the monomer as an interlayer at the interfaces in the MS contact may be interesting.

The aim of this study was to investigate diode parameters of a new diode fabricated using a new functional methacrylic monomer, i.e. Ag/POEMO/*p*-Si MIS diode. The current-voltage (*I-V*) measurement was carried out to obtain barrier height, ideality factor and series resistance of the device using *I-V*, *Cheung-Cheung* and *Norde* methods.

## 2 Experimental

The synthesis of 1-[4- (prop-2-yn-1-yloxy) phenyl] ethanone-Omethacryloyloxime (POEMO) monomer is shown in Fig. 1. Detailed description of synthesizing method can be found elsewhere [11-12].

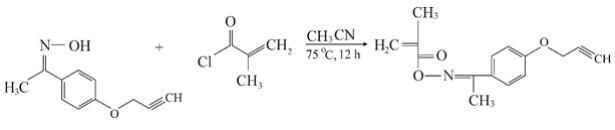



**Figure 1:** The synthesis of POEMO monomer

Ag/POEMO/*p*-Si MIS diode was prepared using a one side polished *p*-type Si (100) wafer. The wafer was chemically cleaned using the RCA cleaning procedure (i.e., a 10 min boil in $NH_3$+$H_2O_2$+6$H_2O$ followed by a 10 min boil in HCl+$H_2O_2$+6$H_2O$). Low resistivity ohmic contact to *p*-type Si substrate was made by Al metal, followed by a temperature treatment at 570 °C for 3 min in $N_2$ atmosphere. The native oxide on the front surface of substrate was removed in HF:$H_2O$ (1:10) solution and finally the wafer was rinsed in de-ionised water for 30 min. Subsequently, *POEMO was coated onto front surface of clean silicon substrate directly by dropping POEMO-acetone solution and waited for the evaporation of the solvent at room temperature.* The contacting metal dot was formed by silver paste with a diameter of about 1.0 mm (diode area=7.85 $10^{-3}$ $cm^2$). Ag/POEMO/*p*-Si MIS diode is thus obtained. The current-voltage (*I-V*) measurements of MIS diode were carried out by a Keithley 6487 picoammeter/voltage source at room temperature.

## 3 Results and discussion

The non-linear *I-V* characteristic of a typical diode behavior is described by the thermionic emission theory as follows [13, 14]:

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(\frac{-qV}{kT}\right)\right] \quad (1)$$

For bias levels larger than 3*kT/q*, Eq. (1) can be expressed as:

$$I = I_0 \exp\left(\frac{qV}{nkT}\right) \quad (2)$$

Here *V, q, n, k* and *T* and represent the applied voltage, the electron charge, the ideality factor, Boltzmann's constant and the absolute temperature in Kelvin, respectively. $I_0$ is the reverse saturation current which can be derived from the straight-line intercept of *lnI* by extrapolation at zero voltage and is given by:

$$I_0 = AA^*T^2\exp\left(\frac{-q\phi_b}{kT}\right) \quad (3)$$

where *A* is the effective diode area and $A^*$ is the effective Richardson constant of $32Acm^{-2}k^{-2}$ for *p*-Si [14-16]. $\phi_b$ is the effective barrier height. Once $I_0$ is obtained, then effective barrier height can be calculated as follows:

$$\phi_b = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \quad (4)$$

The ideality factor or the emission coefficient (*n*) is typically used to measure how the practical diodes deviate from the ideal thermionic emission model or to take into account the contributions of other current transport mechanisms [17]. This parameter can be calculated from the slope of linear region of semi-logarithmic *I-V* plot. Using Eq. (2), ideality factor can be obtained as follows:

$$n = \frac{q}{kT}\left[\frac{\partial V}{\partial (lnI)}\right] \quad (5)$$

Fig. 2 illustrates the experimental *I-V* characteristic of Ag/POEMO/*p*-Si MIS diode at room temperature. Well-known characteristic features of rectifying contacts are the weak voltage dependence of reverse-bias current and the exponential increase of the forward-bias current [4, 18, 19]. It is obvious that the device exhibits a good rectification behavior. The downward curvature (non-linear region) in the semi-log *I-V* characteristic at high forward bias values is arisen from the series resistance ($R_s$) associated with the contact wires or the bulk resistance of the organic interlayer and the inorganic semiconductor.

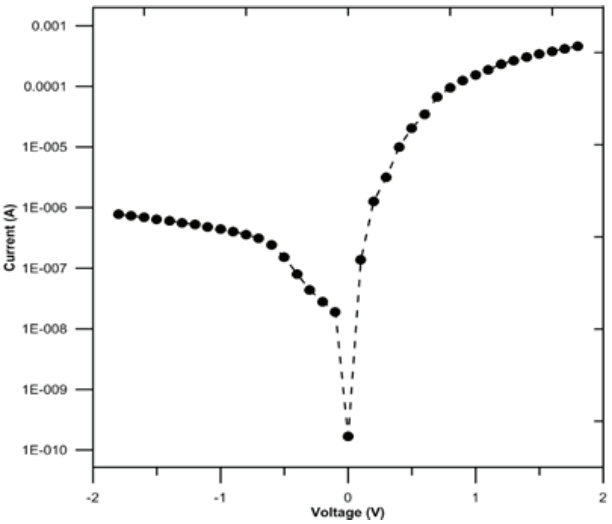



**Figure 2:** The experimental current-voltage characteristic of the Ag/POEMO/*p*-Si MIS diode at room temperature.

On the basis of *TE* theory, the experimental values of the effective barrier height and the ideality factor were determined from the intercept and the slope of the linear portion of the forward-bias *I-V* plot, respectively. The obtained values of effective barrier height and ideality factor were 0.70 eV and 2.81, respectively. For an ideal diode, ideality factor should be close to unity; but for reel diodes it is usually higher than one as we obtained [20-22]. Ideality factor which is greater than unity shows the deviation from thermionic emission theory. In the literature this case is assigned to the interface states, as well as fabrication-induced defects at the surface [18, 20-24]. In addition; interface state density distribution, quantum-mechanical tunneling, image-force lowering, the lateral distribution of barrier height inhomogeneities, the leakage current, series and shunt resistance are also proposed to explain the deviation [13, 18, 23, 25, 26]. Among these, the series resistance ($R_s$) is an important and influential parameter on the electrical characteristics of Schottky barrier diodes. Therefore, determination of series resistance ($R_s$) value deserves attention for understanding the mechanism of diodes.

The barrier height value of 0.70 eV obtained for the Ag/POEMO/*p*-Si device is higher than that achieved with conventional MS contact of Ag/*p*-Si whose barrier height value was 0.62 [27]. By means of the POEMO interlayer; a physical barrier is formed between the metal and the inorganic substrate, preventing the metal from directly contacting the Si surface. The POEMO organic interlayer affects the space charge region of the inorganic substrate [18, 28]. Thus, the change in barrier height can be explained by an interface dipole induced by the organic layer [4]. In the literature, many studies have been performed to modify the barrier height of Schottky barrier diodes by forming an interfacial layer between the metal and the semiconductor using the organic thin films [9, 18, 29, 30]. Here, we showed that POEMO could also be used to modify barrier height of Ag/*p*-Si diode.

As the series resistance can be negligible at low voltage ranges of a forward bias region, the variation of current with voltage shows linearity. However for higher voltages, the current is deviated considerably from linearity by the series resistance, as can be seen in Fig. 2. Cheung and Cheung proposed a method for the determining the series resistance ($R_s$) from the high voltage range of an *I-V* characteristic of a diode [31]. According to Cheung and Cheung, the forward bias current-voltage characteristic of a Schottky barrier diode with a series resistance is given by:

$$I = I_0 exp\left[\frac{q(V - IR_S)}{nkT}\right] \quad (6)$$

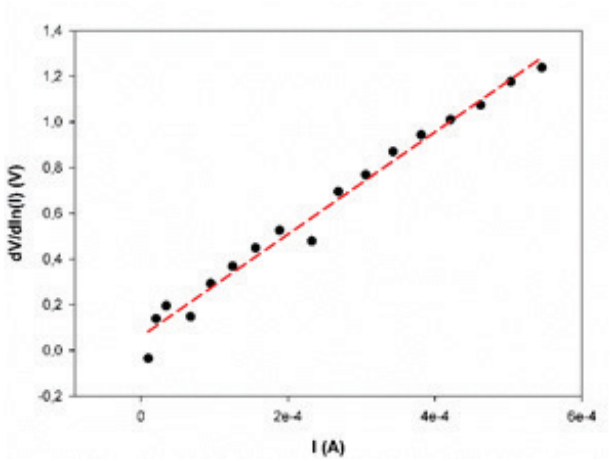
Here $IR_s$ denotes the voltage drop across series resistance of the diode. Using Eq. (6), the electrical parameters viz. series resistance, ideality factor, and barrier height can be determined from the following equations:

$$\frac{dV}{dln(I)} = IR_S - n\left(\frac{kT}{q}\right) \quad (7)$$

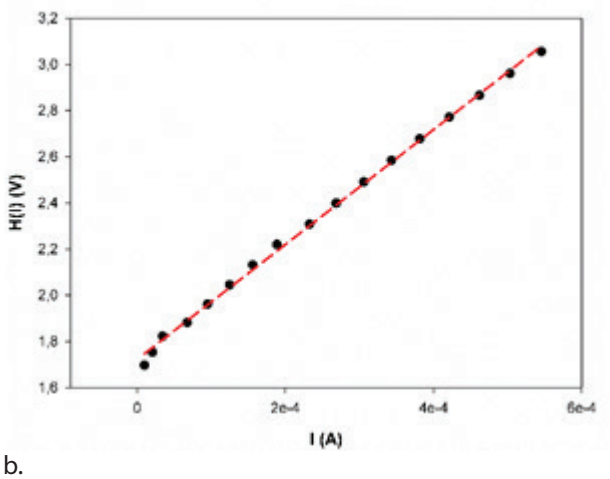
$$H(I) = V - n\left(\frac{kT}{q}\right) ln\left(\frac{I}{AA^*T^2}\right) \quad (8)$$

$$H(I) = IR_S + n\phi_b \quad (9)$$

The plot of *dV/d*(ln*I*) vs. *I* gives a straight line for the data of downward curvature region (Fig. 3a). According to Eq. (7), this plot gives $R_s$ as the slope and *nkT/q* as *y*-axis intercept. Hereby, *n* and $R_s$ were calculated as 2.33 and 2.24 kΩ, respectively. The plot of *H(I)* function is given in Fig. 3b. The slope of *H(I)-I* plot is equal to series resistance ($R_s$), whereas the intercept of the *y*-axis gives $n\phi_b$ Accordingly, using the value of ideality factor obtained from Eq. (7), the barrier height ($f_b$) and series resistance values were calculated as 0.74 eV and 2.49 kΩ, respectively. The series resistance values determined by two different equations of *Cheungs'* are close to each other.




a.




b.

**Figure 3:** Plot of Cheung's fuctions; *dV/d*(ln*I*) vs. *I* (a), *H(I)* vs. *I* (b)

On the other hand, there are differences between the ideality factors and barrier heights obtained from *I-V* and *Cheungs'* methods. These differences are attributed to the differences of extraction region in the forward bias of *I-V* plot. In the *I-V* method, linear region is used for calculation, while *Cheungs'* functions are related to the nonlinear region of *lnI-V* plot in which the interfacial layer thickness between the metal and the semiconductor, the interface states and bulk series resistance are effective [19, 32, 33].

The barrier heights and series resistance of the Schottky diodes can also be calculated using modified Norde method [18, 34]. The following function has been defined in the modified Norde method:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q} ln\left(\frac{I(V)}{AA^{*}T^{2}}\right) \tag{10}$$

Where γ is the first integer (dimensionless) greater than *n*. *I*(*V*) is current obtained from the *I-V* curve. Fig. 4 shows the change of *F(V)* versus *V* for Ag/POEMO/*p*-Si diode. After determining the minimum value of *F(V)* by employing the data in Fig. 4, barrier height and series resistance of the diode can be determined by the following equations:

$$\phi_b = F(V_0) + \frac{V_0}{\gamma} - \frac{kT}{q} \tag{11}$$

$$R_s = \frac{kT}{qI}(\gamma - n) \tag{12}$$

In Eq. (11), $F(V_0)$ is the minimum point of *F*(*V*) and $V_0$ is the corresponding voltage. From the *F*(*V*)-*V* plot and Eqs. (11) and (12), the barrier height and series resistance were found to be 0.72 eV and 3.78 kΩ, respectively. The diode parameters, which were obtained via different methods, were summarized in Table 1. As can be seen in the table, there are differences in values of series resistance obtained from *Cheng-Cheung* and *Norde* methods. These differences were originated from the fact that the full-voltage range of forward bias ln(*I*) – *V* data is used in *Norde* method, whereas only the

**Table 1:** Diode parameters of Ag/POEMO/*p*-Si MIS Schottky diode calculated from *I-V*, *Cheung-Cheung* and *Norde* methods

| Diode parameters | I-V Method | Cheung-Cheung Method | | Norde Method |
|---|---|---|---|---|
| | d(lnI)-V | Dv/d(lnI)-I | H(I)-I | F(V)-V |
| Ideality Factor ( $n$ ) | 2.81 | 2.33 | - | - |
| Barrier Height ($\phi_b$ eV) | 0.70 | - | 0.74 | 0.72 |
| Series Resistance ($R_s$ kΩ) | - | 2.24 | 2.50 | 3.78 |

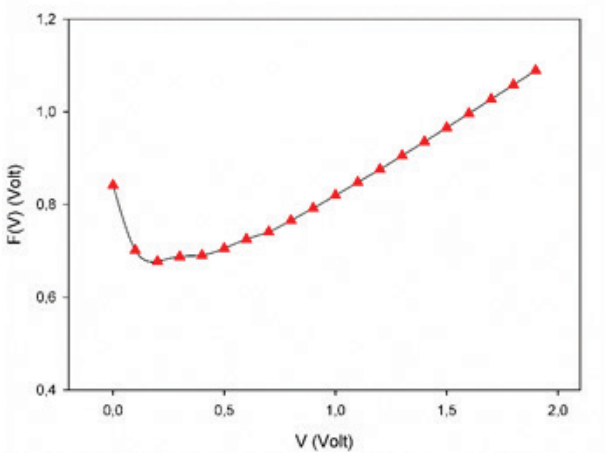



**Figure 4:** Plot of Norde function; F(V) vs. V

high-voltage region (viz. non-linear part of the plot) of the forward bias ln(*I*) – *V* data is used in *Cheung's* method [35, 36]. High series resistance value is accepted as current-limiting factor for the diodes. Gullu et al. attributed the high series resistance to space-charge injection into POEMO thin layer at higher forward bias voltage. As the tunneling process is especially important for a thin interfacial layer, it is assumed that tunneling starts to control the current flow [18, 37].

## 4 Conclusions

In this study, we fabricated an Ag/POEMO/*p*-Si Schottky Barrier diode and investigated its diode parameters by *I-V* measurement. The ideality factor, series resistance and barrier height values were calculated by different methods and were compared. Based on the results the following conclusions could be deduced;

- The Ag/POEMO/*p*-Si Schottky Barrier MIS diode showed good rectifying behavior indicating POEMO organic layer could be used as an interlayer.
- The forward current-voltage characteristics indicated a nonlinear behavior because of the series resistance, as verified by the *n* value was larger than unity.
- We observed that the $\phi_b$ value of 0.70 eV obtained for the Ag/POEMO/*p*-Si device was different than the BH value of the conventional Ag/*p*-Si contact. This case could be attributed to the POEMO organic interlayer which modifies effective Schottky barrier by affecting the space charge region of the inorganic substrate.
- The differences between barrier heights values obtained from different methods were attributed to presence of series resistance, interface states and the voltage drop across the interfacial layer

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# *Area and Energy efficient CORDIC Accelerator for Embedded Processor Datapaths*

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**Abstract:** A proven approach to enhance the performance of an embedded processor is to add specialized hardware accelerator blocks. We present two novel CORDIC accelerator units based on mixed hardware/software approach. These CORDIC accelerators are integrated with an embedded processor datapath to enhance the processor performance in terms of execution time and energy efficiency. The first accelerator design is based on the Standard CORDIC algorithm. The Standard CORDIC based accelerated embedded processor datapath is 35% more cycle efficient than a datapath lacking Standard CORDIC accelerator. This design also leads to 34% energy reduction. The mixed hardware/software implementation of Standard CORDIC algorithm is area efficient as it saves two 16-bit adders. The second accelerator design is based on a Modified CORDIC algorithm. Our evaluation shows that a Modified CORDIC accelerated embedded processor datapath is 14.5 times more cycle efficient than a datapath lacking Modified CORDIC accelerator. This design leads to 14 times energy reduction with a very small area overhead. The mixed hardware/software Modified CORDIC accelerator is area efficient as it saves four multipliers and two adders. The Modified CORDIC hardware accelerator block has 4.3 times less latency and takes 4 times less area as compared to Standard CORDIC Time Shared implementation. The novelty of the design in the use of Modified CORDIC accelerator is that it takes a single iteration to compute the values of sine and cosine as compared to the Standard CORDIC algorithm, which requires N iterations. This provides effective use of the accelerator in programming systems where a series of values of sine and cosine are required to be computed.

**Keywords:** CORDIC; Accelerator; Codesign; FPGA; MicroBlaze Processor

# *Prostorsko in energijsko učinkovit CORDIC pospeševalnik za podatkovne poti vgrajenega procesorja*

**Izvleček:** Dodajanje specializiranih pospeševalnih blokov v vgrajen procesor je uveljaljena metoda povečevanja njegove učinkovitosti. Predstavljamo dve novi pospeševalni enoti za CORDIC na osnovi mešane programsko strojne rešitve. Ti pospeševalniki so integrirani v podatkovne poti procesorja za zagotavljanje krajšega izvajalnega časa in energijske učinkovitosti. Prvi pospeševalnik temelji na standardnem CORDIC algoritmu in omogoča 35 % višjo učinkovitost cikla kot brez njegove uporabe. Poraba energije je 34 % nižja. Programsko/strojno mešana implementacija je prostovno učinkovita in prihrani dva 16-bitna seštevalnika. Drugi pospeševalnik temelji na modificiranem CORDIC algoritmu. Vrednotenje modificiranega algoritma je pokazalo 14.5 kratno izboljšanje učinkovitosti cikla. Istočasno se je za 14 krat zmanjšala poraba energije. Programsko/strojno mešana rešitev prihrani štiri množilnik ein dva seštevalnika. Strojno izveden modificiran CORDIC pospeševalnik ima 4.3 krat manjšo latenco in potrebuje 4 krat manj prostora kot standardna CORDIC rešitev s delitvijo časa. Prednost modificiranega CORDIC pospeševalnika je, da potrebuje le eno iteracijo za izračun sinusa in kosinusa v primerjavi s standardnim CORDIC algoritmom, ki potrebuje N iteracij. To omogoča njegovo učinkovito uporabo v programskih sistemih s potrebo po računanju velikega števila izračunavanja funkcij sinus in kosinus.

**Ključne besede:** CORDIC; pospeševalnik; Codesign; FPGA; MicroBlaze procesor

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## 1 Introduction

The CORDIC (Coordinate Rotation Digital Computer) algorithm first introduced by Jack E.Volder [1], [2] in 1959 is used for the computation of trigonometric functions, multiplication, and division. It was extended further by John Walther [3], [4] in 1971 for the computation of a wide range of elementary functions such as logarithms, exponentials, and square roots. During the same period, Cochran [5] showed that the CORDIC algorithm is a suitable technique for scientific calculator implementation. CORDIC algorithm is used in a broad range of areas including signal processing, communication systems, robotics and computer graphics. During the past 50 years, a lot of research has been carried out on CORDIC in the area of algorithm and architecture design to achieve high performance and area efficient hardware solutions [6-8]. Angle recording CORDIC [9] solves the repetitive rotation issue of Standard CORDIC by recoding the latest inserted item into the angle set. This technique is helpful in the implementation of Discrete Fourier Transform and Discrete Cosine Transform but has a drawback of unpredictable scale factor [10]. Extended Elementary Angle Set (EEAS) CORDIC uses searching techniques such as Greedy Searching and Trellis-based Searching Algorithm (TBS) to find the required angle from an angle set [11], [12]. Pipelined CORDIC architectures [13-15] are widely implemented in digital signal processing for sine wave generation, orthogonal discrete transform, and adaptive filtering. Radix-4 [16], [17] and BCD [18], [19] CORDIC architectures are applied in situations where high precision is required. Vachhani et al. [20] implemented CORDIC design by eliminating ROM and barrel shifters, resulting in huge resource reduction. CORDIC architecture with reduced ROM has also been reported in [21]. Aggarwal et al. [22] implemented Scale-free hyperbolic CORDIC processor for waveform generation. Caro et al. [23] implemented digital synthesizer/mixer with hybrid CORDIC multiplier architecture.

CORDIC algorithm is used in many real-time applications including direct digital frequency synthesis (DDFS) having critical latency issue. The Standard CORDIC algorithm has fixed latency in which the number of iterations is directly proportional to bit precision. A lot of research has been carried out in past to improve the latency of CORDIC for the calculation of sine and cosine of an angle. Rodrigues and Swartzlander [24] proposed a 50% reduced iterative CORDIC algorithm, by using dynamic angle selection which recodes the angle. Aytore and Alkar [25] used additional logic and control circuitry to reduce the number of iterations, by involving diversified iterations. Hu and Naganathan [26] also proposed a 50% reduced iterative CORDIC algorithm, but it works only for fixed number of angles which should be known in advance. Higher Radix CORDIC algorithms have also been used for the reduction in iterations. Antelo et al. [27] proposed a radix-4 representation for $\sigma_i$ in which the rotations are chosen from a set {+2,+1,0,-1,-2} of four possible iterations, but has more area overhead. Phatak et al. [28] proposed a double rotation technique in which the values of $\sigma_i$ and $\sigma_{i+1}$ are set using a prediction technique. Parallel angle coding is also reported in the literature at the cost of an increase in micro-rotations compared to Standard CORDIC algorithm [29-31]. Kao et al. [32] proposed the use of encoded angle to directly compute the initial iterations using look-ahead approach at the cost of area overhead. Kamboh and Shoab [33], [34] proposed an IS-CORDIC architecture which computes the values of sine and cosine in a single cycle.

The CORDIC algorithm can be implemented in software on an embedded processor. But software solutions running on a processor takes a lot of clock cycles compared to the dedicated hardware implementations. The research on the sources of inefficiency in various applications showed that 90% of the program runtime and energy is utilized by only 10% of application code [46]. This small portion of the applications which becomes a performance bottleneck can be efficiently managed by implementing them in hardware as specialized accelerator blocks [35-38]. High data rates in modern signal processing and communication systems can only be delivered by dedicated hardware solutions. Today's embedded systems use processor core with different hardware accelerators in order to speed up certain portions of the application code. This heterogeneous approach reaps the benefits of programmability of an embedded processor and efficiency of specialized hardware accelerator blocks. Most of the embedded processors today contain various dedicated hardware blocks to perform a wide range of communication system tasks efficiently. These include MAC, TCP/IP, Ethernet, CRC, and CAN etc. Implementing CORDIC as a hardware accelerator will be effective in programming systems where a series of values of sine and cosine are required to be computed.

The rest of the paper is organized as follows: in the next section, the theoretical background of Standard CORDIC algorithm is presented. Later, we describe the implementation of hardware accelerator based on the Standard CORDIC algorithm. Subsequently, we describe a Modified CORDIC algorithm and we use this technique to implement a more efficient CORDIC accelerator. Finally, we summarize our conclusions.

## 2 Standard CORDIC Algorithm

In Standard CORDIC algorithm we start with a unit vector and rotate it to the desired angle θ. When the unit vector reaches the desired angle the x and y co-ordinates of the unit vector give us cos θ and sin θ, respectively. Mathematically, this can be shown with the expression below.

$$\theta = \sum_{i=0}^{N-1} \sigma_i \Delta\theta \quad where \quad \sigma_i = \begin{cases} +1 & \text{for positive rotation} \\ -1 & \text{for negative rotation} \end{cases} \tag{1}$$

First, the unit vector is rotated by an angle $\theta_i$ and then by an angle $\Delta\theta_i$ again. This brings the unit vector to angle $\Delta\theta_{i+1}$, as depicted in Fig. 1. Mathematically, this can be expressed [34] by Equations (1) and (2).

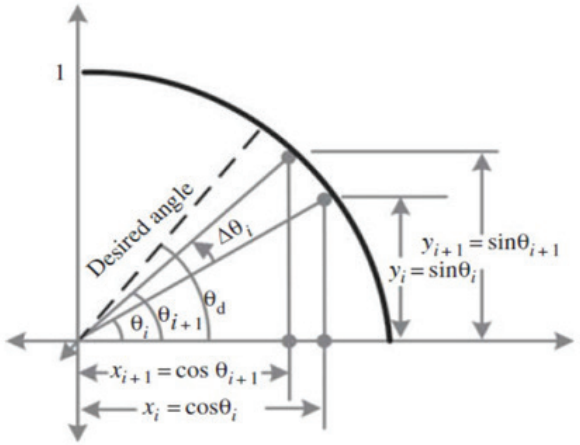


**Figure 1:** Standard CORDIC algorithm iterations

$$\cos\theta_{i+1} = \cos(\theta_i + \sigma_i\Delta\theta_i) = \cos\theta_i \cos\Delta\theta_i - \sigma_i \sin\theta_i \sin\Delta\theta_i \tag{2}$$

$$\sin\theta_{i+1} = \sin(\theta_i + \sigma_i\Delta\theta_i) = \sin\theta_i \cos\Delta\theta_i + \sigma_i \cos\theta_i \sin\Delta\theta_i \tag{3}$$

From Fig. 1. we can see that $x_i = \cos\theta_i$, $y_i = \sin\theta_i$ and similarly $x_{i+1} = \cos\theta_{i+1}$, $y_{i+1} = \sin\theta_{i+1}$

Substituting these in Equations (2) and (3), we get Equations (4) and (5) as given below.

$$x_{i+1} = x_i \cos\Delta\theta_i - \sigma_i y_i \sin\Delta\theta_i \tag{4}$$

$$y_{i+1} = \sigma_i x_i \sin\Delta\theta_i + y_i \cos\Delta\theta_i \tag{5}$$

Equations (4) and (5) can be expressed in matrix form as

$$\begin{bmatrix} x_{i+1} \\ y_{i+1} \end{bmatrix} = \begin{bmatrix} \cos\Delta\theta_i & -\sigma_i \sin\Delta\theta_i \\ \sigma_i \sin\Delta\theta_i & \cos\Delta\theta_i \end{bmatrix} \begin{bmatrix} x_i \\ y_i \end{bmatrix} \tag{6}$$

By taking $\cos\Delta\theta_i$ common, we get Equation (7)

$$\begin{bmatrix} x_{i+1} \\ y_{i+1} \end{bmatrix} = \cos\Delta\theta_i \begin{bmatrix} 1 & -\sigma_i \tan\Delta\theta_i \\ \sigma_i \tan\Delta\theta_i & 1 \end{bmatrix} \begin{bmatrix} x_i \\ y_i \end{bmatrix} \tag{7}$$

By using the trigonometric identity

$$\cos\Delta\theta_i = \frac{1}{\sqrt{1+\tan^2\Delta\theta_i}}$$

To avoid multiplication we get Equation (8)

$$\tan\Delta\theta_i = 2^{-i} \tag{8}$$

Equation (8) can also be expressed as $\Delta\theta_i = \tan^{-1}2^{-i}$.

Substituting Equation (8) in (7) we get the following Equation.

$$\begin{bmatrix} x_{i+1} \\ y_{i+1} \end{bmatrix} = \frac{1}{\sqrt{1+2^{-2i}}} \begin{bmatrix} 1 & -\sigma_i 2^{-i} \\ \sigma_i 2^{-i} & 1 \end{bmatrix} \begin{bmatrix} x_i \\ y_i \end{bmatrix} \tag{9}$$

Let,

$$k_i = \frac{1}{\sqrt{1+2^{-2i}}} \quad , \quad \sigma_i = \begin{bmatrix} 1 & -\sigma_i 2^{-i} \\ \sigma_i 2^{-i} & 1 \end{bmatrix}$$

Then Equation (9) can be expressed as

$$\begin{bmatrix} x_{i+1} \\ y_{i+1} \end{bmatrix} = K_i \sigma_i \begin{bmatrix} x_i \\ y_i \end{bmatrix} \tag{10}$$

Initially, the index i=0, thus the Equation (10) can be given for i=0 as

$$\begin{bmatrix} x_1 \\ y_1 \end{bmatrix} = K_0 R_0 \begin{bmatrix} x_0 \\ y_0 \end{bmatrix} \tag{11}$$

and for index i=1, we have

$$\begin{bmatrix} x_2 \\ y_2 \end{bmatrix} = K_1 R_1 \begin{bmatrix} x_1 \\ y_1 \end{bmatrix} \tag{12}$$

Substituting the value of $\begin{bmatrix} x_1 \\ y_1 \end{bmatrix}$ from Equation (11) into (12) we get

$$\begin{bmatrix} x_2 \\ y_2 \end{bmatrix} = K_0 K_1 R_0 R_1 \begin{bmatrix} x_0 \\ y_0 \end{bmatrix} \tag{13}$$

Thus Equation (10) for indices i=N-1 becomes

$$\begin{bmatrix} x_N \\ y_N \end{bmatrix} = K_0 K_1 K_2 ... K_{N-1} R_0 R_1 R_2 ... R_{N-1} \begin{bmatrix} x_0 \\ y_0 \end{bmatrix} \quad (14)$$

All the $K_i$ are constants and their product can be computed as a constant k, so we get

$$K = K_0 K_1 K_2 ... K_{N-1} = \prod_{i=0}^{N-1} \frac{1}{\sqrt{1+2^{-2i}}} \quad (15)$$

Finally we get Equation (16) as given below

$$\begin{bmatrix} x_N = \cos\theta \\ y_N = \sin\theta \end{bmatrix} = R_0 R_1 R_2 ... R_{N-1} \begin{bmatrix} K \\ 0 \end{bmatrix} \quad (16)$$

### *2.1 Hardware Mapping of Standard CORDIC*

For efficient hardware implementation the Standard CORDIC algorithm is listed as follows:

- To simplify the hardware $\theta_0$ is set to the desired angle $\theta_d$ and $\theta_1$ is computed as given below

$$\theta_1 = \theta_0 - \sigma_0 \tan^{-1} 2^0$$

Where, $\sigma_0$ is the sign of $\theta_0$ and initialize as $x_0 = k$ and $y_0 = 0$.

- The algorithm then performs N iterations for i = 1,2,...,N-1 and computes the following set of Equations

$$if\,(\theta_i > 0) \quad \sigma_i = 1 \quad else \quad \sigma_i = -1$$

$$x_{i+1} = x_i - \sigma_i 2^{-i} y_i \quad (17)$$

$$y_{i+1} = y_i + \sigma_i 2^{-i} x_i \quad (18)$$

$$\theta_{i+1} = \theta_i - \sigma_i \tan^{-1} 2^{-i} \quad (19)$$

All the values for $\tan^{-1}2^{-i}$ are precomputed and stored in an array.

- The final iteration generates the desired results given below in the two equations

$$\cos\theta_d = x_N$$

$$\sin\theta_d = y_N$$

The Standard CORDIC algorithm is naturally suitable for hardware mapping. The *ith* iteration of the algorithm can be implemented as a CORDIC Processing Element (PE), shown in Fig. 2. The CORDIC PE implements the Equations (17), (18) and (19) of Standard CORDIC algorithm in hardware and its internal implementation


**Figure 2:** Standard CORDIC Processing Element (PE)

is shown in Fig. 3. These CORDIC PEs can be cascaded together for a fully parallel hardware implementation of Standard CORDIC algorithm as shown in Fig. 4. Depending on the number of cycles available for computing sine and cosine values the Standard CORDIC algorithm can also be folded and implemented as a time-shared architecture with these CORDIC PEs.

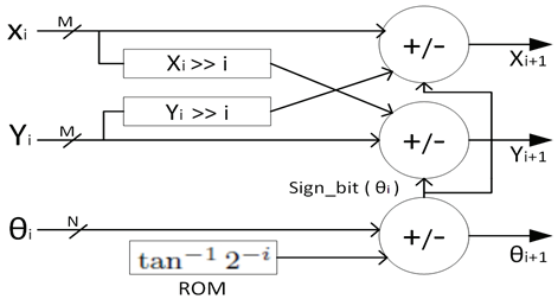


**Figure 3:** Internal implementation of Standard CORDIC PE

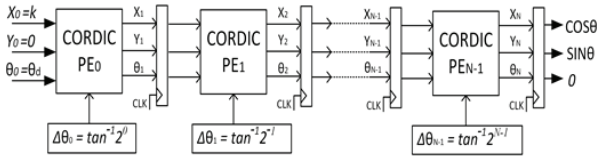


**Figure 4:** Pipelined fully parallel architecture of Standard CORDIC algorithm

### *2.2 Standard CORDIC Hardware Accelerator*

We have developed a novel mixed hardware/software CORDIC accelerator unit using the Standard CORDIC algorithm. Equations (17) and (18) of Standard CORDIC algorithm are implemented in hardware using Verilog HDL hardware description language. While Equation (19) is implemented in software. We used Xilinx Spartan-6 FPGA SP605 Evaluation Kit [41] and Xilinx Embedded Development Kit (EDK) [39] for the implementation. Xilinx Microblaze soft core processor system [40] is used to execute the software part of Standard CORDIC accelerator. There are two ways to integrate a hardware accelerator core into a MicroBlaze based embedded processor system. One way is to connect the accelerator through the Processor Local Bus (PLB). The second way is to connect it using a dedicated Fast Simplex Link (FSL) bus system [42]. First, PLB was tried but

it was taking more cycles. The reason for this is the fact that it is a traditional memory-mapped transaction bus. Later, it was decided to integrate our Standard CORDIC accelerator block with the MicroBlaze processor system using a dedicated FIFO style FSL bus as shown in Fig. 5.

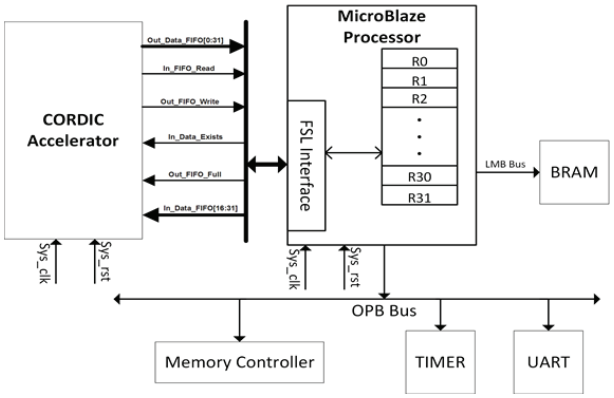


**Figure 5:** CORDIC Accelerator with MicroBlaze Processor System

First, the Standard CORDIC algorithm was implemented in C programming language. It was executed on MicroBlaze processor using Xilinx Software Development Kit (SDK) [39]. The cycle count for the software implementation of Standard CORDIC algorithm was measured using the XPS hardware timer block. The MicroBlaze processor takes 933 cycles to compute the values of sine and cosine. While executing the complete software implementation of Standard CORDIC algorithm. In the next step, Verilog HDL code of the hardware part of Standard CORDIC accelerator was implemented. It was verified and synthesized using Xilinx ISE design suit [39]. Table 1 shows the Synthesis results of Time Shared Standard CORDIC algorithm and Standard CORDIC hardware accelerator block. Standard CORDIC algorithm having N iterations has a latency of N times the delay of a single iteration. Here, N represents the internal word length. The Time Shared Standard CORDIC algorithm and Standard CORDIC hardware accelerator block were synthesized on 7vx485tffg1157-3 Virtex-7 FPGA device. This FPGA device uses a 28nm technology

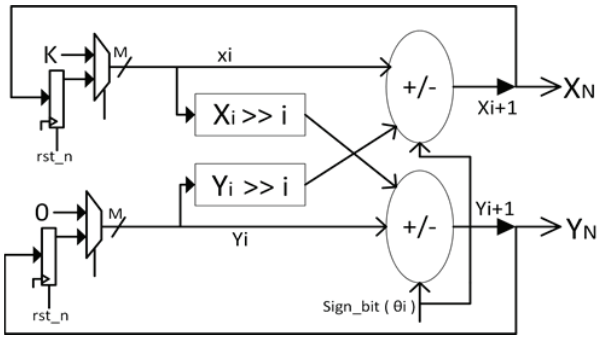


**Figure 6:** Standard CORDIC Hardware Accelerator Block

and gives a critical path delay of 51.52ns and 51.408ns respectively. As in the case of Standard CORDIC hardware accelerator block we have implemented $\theta_i$ Table in software. Thus no RAM is used. The mixed hardware/software implementation of Standard CORDIC algorithm is area efficient as it saves two 16-bit adders as shown in Table 1.

**Table 1:** Synthesis results of Time Shared Standard CORDIC algorithm and Standard CORDIC Accelerator

| | Time Shared Standard CORDIC | Standard CORDIC Accelerator |
|---|---|---|
| Max Freq | (310/16)=19.3 MHz | (311/16)=19.4 MHz |
| Latency | 3.220x16 = 51.52ns | 3.213x16 = 51.408ns |
| RAMs | 16x16-bit RAM | 0 |
| Adders | 2x16-bit, 4x22-bit | 4x22-bit |
| Counters | 1x4-bit | 1x4-bit |
| Multiplexers | 6 | 4 |
| Logic Shifters | 2 | 2 |
| Slice Registers | 108 | 92 |
| Slice LUTs | 344 | 282 |
| Slices | 148 | 139 |

Fig. 6 shows the architecture of Standard CORDIC hardware accelerator unit. The Standard CORDIC accelerator was attached with the Microblaze processor system via FSL bus using Xilinx Platform Studio (XPS) [39]. Later the software part of Standard CORDIC accelerator was implemented in C programming using Xilinx SDK. The predefined C functions of SDK were used to communicate with hardware part of Standard CORDIC accelerator via FSL bus. In the software part of Standard

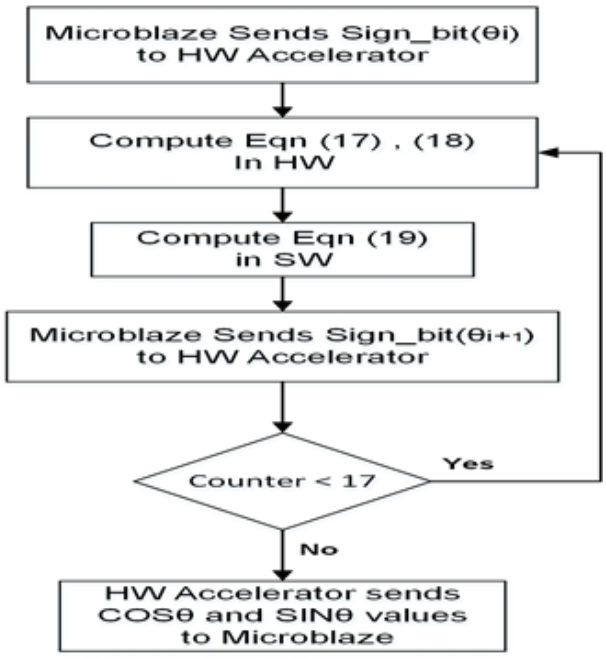


**Figure 7:** Flow chart for Standard CORDIC Accelerator Implementation

CORDIC accelerator the values for $\tan^{-1}2^{-i}$ are precomputed and stored in an array. Equation (19) is executed for every iteration of Standard CORDIC algorithm using C programming language. The sign bit of $\theta_i$ is sent via FSL bus to the CORDIC hardware accelerator which executes Equations (17) and (18) in hardware. For every iteration of Standard CORDIC algorithm as shown in Fig.3. After the final iteration, we get values of sine and cosine via FSL bus from the Standard CORDIC accelerator by using predefined C functions in SDK. Fig.7 shows the steps involved in the computation of sine and cosine using mixed hardware/software Standard CORDIC accelerator.

The cycle count for mixed hardware/software implementation of Standard CORDIC algorithm was measured using the XPS hardware timer block. The mixed hardware/software implementation of Standard CORDIC algorithm takes 601 cycles to compute the values of sine and cosine. The energy dissipation was calculated for both the implementations, shown in Table 3. Our evaluation shows that an accelerated embedded processor datapath is 35% more cycle efficient, than a datapath lacking Standard CORDIC accelerator. The design also leads to 34% energy reduction. This mixed hardware/software implementation is also area efficient as we implemented the Equation (19) of Standard CORDIC algorithm in software on a MicroBlaze processor, which resulted in saving two 16-bit adders. Obviously, if we implement all the three Equations (17), (18) and (19) of Standard CORDIC algorithm in hardware it will be a faster solution. Thus it's a trade-off between area and execution time.

## 3 Modified CORDIC Algorithm

The Standard CORDIC algorithm is dependent on $\sigma_i$ for making a decision of whether to do addition or subtraction, in Equations (17), (18) and (19). This algorithmic limitation is the reason for taking more cycles for computation of desired results. To make this algorithm fast and suitable for parallel implementation we need to make some modifications in the Standard CORDIC algorithm. In Standard CORDIC algorithm we assumed that θ is the summation of N positive and negative micro-rotations of angles $\Delta\theta_i$ as shown in Equation (1). The θ can also be represented in a binary form for micro-rotations [34] as shown in Equation (20) below

$$\theta = \sum_{i=0}^{N-1} b_i 2^{-i} \quad for \quad b_i \in \{0,1\} \tag{20}$$

Here, bit $b_i$ decides between a positive rotation of $2^{-i}$ or a zero rotation, for each term in the summation. To make this expression useful for hardware implementation we need to make the constant K in Equation (15) data independent by recoding the Equation (20) to only use +1 or -1. For fixed point implementation of CORDIC, the desired angle $\theta_d$ is represented as $\theta_{1.\,N-1}$. Here the most significant bit (MSB) is used for representing the sign of integer value and *N* - 1 bits are set aside for fractional part of N-bit θ. The expression (20) can be represented after recording by Equation (21) as

$$\sum_{i=0}^{N-1} b_i 2^{-i} = \sum_{i=0}^{N-1} r_i 2^{-(i+1)} + 2^{-0} - 2^{-N} r_i = 2b_i - 1, \quad where \quad r_i \in \{0,1\} \tag{21}$$

To manage the constant factor ($2^{-0}$ -$2^{-N}$) in the recoding of Equation (21), an initial fixed rotation $Q_{init}$ is given. The recoding of $b_i s$ as ±1 helps in making K a constant and its value is equal to [34].

$$K = \prod_{i=0}^{N-1} \cos(2^{-1})$$

The initial rotation is applied first offline given below by the three equations

$$Q_{init} = (2^{-0} - 2^{-N})$$

$$x_0 = k\cos(Q_{init})$$

$$y_0 = k\sin(Q_{init})$$

The following equations are computed for i = 1,2,3 .... N-1 iterations as

$$x_{i+1} = x_i - r_i \tan^{-1} 2^{-i} y_i$$

$$y_{i+1} = r_i \tan^{-1} 2^{-i} x_i + y_i$$

Here, the values of $r_i$ are precomputed. Unlike $\sigma_i$, these iterations don't need to compute $\Delta\theta_i$ as was required in Standard CORDIC algorithm. The final iteration generates the desired results as

$$\cos\theta_d = x_N$$

$$\sin\theta_d = y_N$$

One issue in modified CORDIC algorithm which needs to be solved is the elimination of multiplication by tan $2^{-i}$ in every iteration. As $\tan\theta \approx \theta$ for small values of θ, this results in converting multiplication into simple shift by $2^{-i}$. So we get

$$\tan 2^{-i} \approx 2^{-i} \quad for \quad i > 4 \tag{22}$$

This approximation does not affect the precision of desired output results [29], [44]. We can precompute the values for the first four iterations and store them in a ROM. In the hardware implementation of the algorithm, we can use these precomputed values for initial M iterations from a ROM. The ROM address for these

precomputed values is calculated using M most significant bits (MSBs) of θ as given below

$$index = \theta_0 2^{M-1} + \theta_1 2^{M-2} + ... + \theta_{M-1} 2^0 \quad (23)$$

x[M-1] and y[M-1] values are accessed from ROM and the remaining values of x[k] and y[k] are computed with the help of approximation of Equation (22). This results in converting multiplication by tan $2^{-i}$ into simple shift by $2^{-i}$. This transformation helps in fully parallel hardware implementation of the algorithm for better performance. We can combine various iterations in the CORDIC algorithm to increase the performance and reduce the hardware [45]. As the iterations are not dependent on the values of $\Delta\theta_i$ in the modified CORDIC. Thus, we can substitute the values of previous iterations into the current iteration. For M=4 indexing into the tables, we get values of $x_4$ and $y_4$. Substituting these values for i=5, we get Equations (24) and (25) as given below

$$x_5 = x_4 - r_5 2^{-5} y_4 \quad (24)$$

$$y_5 = r_5 2^{-5} x_4 - y_5 \quad (25)$$

For i=6, we get Equations (26) and (27) as provided below

$$x_6 = x_5 - r_6 2^{-6} y_5 \quad (26)$$

$$y_6 = r_6 2^{-6} x_5 - y_5 \quad (27)$$

Substituting the expressions for $x_5$ and $y_5$ from Equations (24) and (25) into Equations (26) and (27), we get the following equations

$$x_7 = (1 - r_5 r_6 2^{-11} - r_5 r_7 2^{-12} + r_6 r_7 2^{-13}) x_4 - (r_5 2^{-5} - r_6 2^{-6} + r_7 2^{-7} - r_5 r_6 r_7 2^{-18}) y_4 \quad (28)$$

$$x_7 = (r_5 2^{-5} - r_6 2^{-6} + r_7 2^{-7} - r_5 r_6 r_7 2^{-18}) x_4 + (1 - r_5 r_6 2^{-11} - r_5 r_7 2^{-12} + r_6 r_7 2^{-13}) y_4 \quad (29)$$

The terms $2^{-k}$ with $k > P$ for a P-bit data path makes the expressions (28) and (29) outside the required precision and can be discarded. Ignoring these terms and substituting previous equations into current iteration we get the value $x_N$ and $y_N$, expressed in terms of $x_4$ and $y_4$ [33, 34]. For P=16, we have

$$x_{16} = x_4 + \sum_{n=5}^{17} r_n 2^{-n} y_4 + \sum_{n=11}^{17} r_5 r_{n-4} 2^{-n} x_4 - \sum_{n=13}^{17} r_6 r_{n-4} 2^{-n} x_4 - \sum_{n=15}^{17} r_7 r_{n-4} 2^{-n} x_4 \quad (30)$$

$$y_{16} = y_4 - \sum_{n=5}^{17} r_n 2^{-n} x_4 - \sum_{n=11}^{17} r_5 r_{n-4} 2^{-n} y_4 - \sum_{n=13}^{17} r_6 r_{n-4} 2^{-n} y_4 - \sum_{n=15}^{17} r_7 r_{n-4} 2^{-n} y_4 \quad (31)$$

Expressions (30) and (31) can be reduced to the following equations

$$\cos\theta = (1 - \sum_{i=M+1}^{N-1} \sum_{j=i+1(i+j)\le P}^{N-1} r_i r_j 2^{-(i+j)}) x_M - (\sum_{i=M+1}^{N-1} r_i 2^{-i}) y_M \quad (32)$$

$$\sin\theta = (1 - \sum_{i=M+1}^{N-1} \sum_{j=i+1(i+j)\le P}^{N-1} r_i r_j 2^{-(i+j)}) y_M + (\sum_{i=M+1}^{N-1} r_i 2^{-i}) x_M \quad (33)$$

We can further optimize the modified CORDIC algorithm by using reverse encoding and mapping the expressions in $r_i$ into two binary constants, which will require four parallel multipliers and two adders to compute the desired results in a single cycle. The expressions (32) and (33) have two constants given below

$$const_1 = (\sum_{i=M+1}^{N-1} r_i 2^{-i}) \quad (34)$$

$$const_2 = (1 - \sum_{i=M+1}^{N-1} \sum_{j=i+1(i+j)\le P}^{N-1} r_i r_j 2^{-(i+j)}) \quad (35)$$

The following Equations (36) and (37) gives the desired results in a single cycle by using these constants.

$$\cos\theta = const_2 \times x_M - const_1 \times y_m \quad (36)$$

$$\sin\theta = const_1 \times x_M + const_2 \times y_m \quad (37)$$

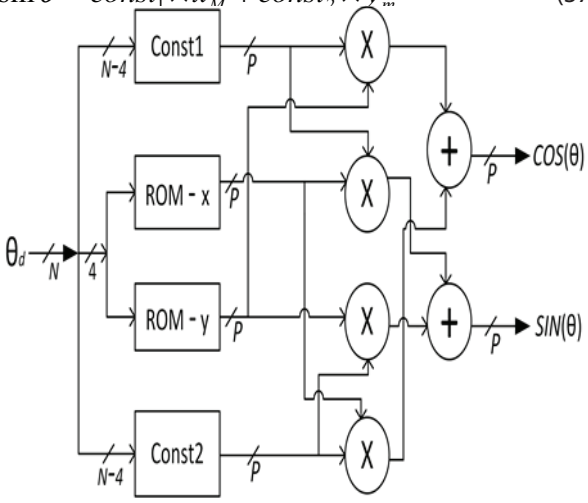


**Figure 8:** The optimal hardware design which computes sine and cosine in a single cycle

The single cycle modified CORDIC design [33, 34] is shown in Fig. 8. The constants in Equations (36) and (37) can be inverse coded using Equation (21). The const1 can be inverse coded as

$$\sum_{i=M+1}^{N-1} r_i 2^{-(i+1)} = \sum_{i=M+1}^{N-1} b_i 2^{-i} - 2^{-M} + 2^{-N} \quad (38)$$

The $b_i$ s are used for computing the constant without modification. The $2^{-N}$ term is eliminated by appending 1 to b. MSB of $b_N$ and the term - $2^{-M}$ is eliminated by flipping $b_{M+1}$ bit and assigning negative weight to it. Thus const1 can be expressed as

$$const_1 = -b'_{M+1} 2^{-M} + \sum_{i=M+2}^{N} b_i 2^{-(i-1)} \quad (39)$$

The complement of the bit $b_{M+1}$ results in the bit $b'_{M+1}$. We can implement Equation (39) in hardware by concatenating the bits $b_i$. The const2 can be implemented by computing $t_k s$ for $i + j = 2M + 1,\ldots,P$ as $t_k s = r_i r_j$, where $k = i+j$ and $k \leq P$. The Equation (38) can be used to inverse code the $t_k s$ and Equation (34) is used to compute its equivalent as const1. Let N=16 and P=16 holds. For this the values of $t_k s$ are computed for i=5,6,7. For i=5, $t_k$ are inverse coded as constant value $t_k = r_5 r_j$, for j=6,7,...,11 where $k = 5+j$ and $k \leq P$.

$$\sum_{j=i+1}^{\leq P} t_5, j 2^{-(j+1)} = \sum_{k=2M+1}^{N-1} c_k 2^{-k} \quad (40)$$

Here, $c_k = b_5 \sim \wedge b_j$ and $k = 5+j$ hold. Then values of $t_6$, $j$, $t_7$, $j$ are computed for every index i. The $t_k s$ are inverse coded using $b_k s$ as

$$beta_0 = \sum_{k=2M+1}^{N-1} t_k 2^{-(k+1)} = \sum_{k=2M+1}^{N-1} b_k 2^{-k} - 2^{-2M} + 2^{-N} \quad (41)$$

Equation (41) after some manipulations can be written as

$$beta_0 = -b'_{2M+1} 2^{-2M} + \sum_{k=2M+2}^{N} b_i 2^{-(i-1)} \quad (42)$$

Similarly, the values of *beta1* and *beta2* can also be computed following the same steps for i=6 and i=7, respectively. The const2 can be computed as

$$const_2 = 1 - beta_0 - beta_1 - beta_2 \quad (43)$$

The inverse coded constants const1 and const2 can be implemented in Verilog HDL for the desired angle $\theta_d$, by the simple concatenation of bits as given below

$$Constant1 : const_1 = \{6\{\sim b[5]\}, b[10:0], 1'b1\}$$

$$Constant2 : c_0 = \{6\{b[5]\}\} \sim \wedge b[11:6]$$

$$c_1 = \{4\{b[6]\}\} \sim \wedge b[10:7]$$

$$c_2 = \{2\{b[7]\}\} \sim \wedge b[9:8]$$

$$beta_0 = \{12\{\sim c_0[5]\}, c_0[4:0], 1'b1\}$$

$$beta_1 = \{14\{\sim c_1[3]\}, c_1[2:0], 1'b1\}$$

$$beta_2 = \{16\{\sim c_2[1]\}, c_2[0], 1'b1\}$$

$$const_2 = 16'h4000 - (beta_0 + beta_1 + beta_2)$$

### *3.1 Modified CORDIC Hardware Accelerator*

We have developed a second novel mixed hardware/software CORDIC accelerator unit using the Modified CORDIC algorithm. In Modified CORDIC algorithm based accelerator we implemented the two constants const1 and const2 in hardware using the Verilog HDL. The four multiplications and two additions in Equations (36) and (37) are implemented in software. Fig. 9 shows the block diagram of Modified CORDIC hardware accelerator unit. We used Xilinx Spartan-6 FPGA SP605 Evaluation Kit [41] and Xilinx Embedded Development Kit (EDK) [39] for the implementation. Xilinx Microblaze soft core processor system [40] is used to execute the software part of Modified CORDIC accelerator. The hardware part of Modified CORDIC accelerator is attached to the MicroBlaze processor system using Fast Simplex Link (FSL) bus system [42].

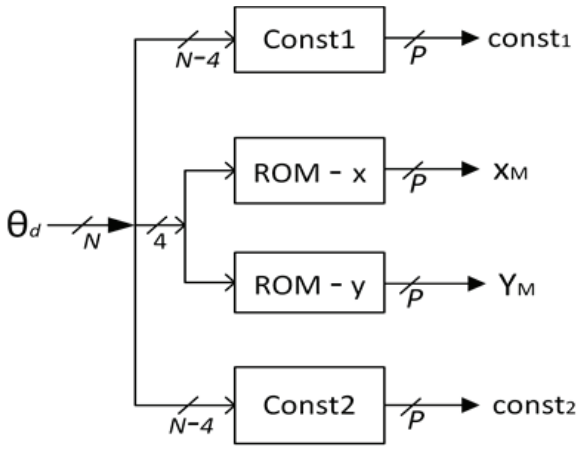


**Figure 9:** Modified CORDIC HW Accelerator

First, the Modified CORDIC algorithm is implemented in C programming language and it is executed on MicroBlaze processor using Xilinx Software Development Kit (SDK) [39]. The cycle count for the software implementation of Modified CORDIC algorithm was measured

using the XPS hardware timer block. The MicroBlaze processor takes 2971 cycles to compute the values of sine and cosine while executing the complete software implementation of Modified CORDIC algorithm. Most of the processor time is spent while computing the two constants of Modified CORDIC algorithm. The two constants can be implemented more efficiently in hardware using Verilog HDL by simple concatenation of bits, compared to software implementation. This is the reason for implementing the two constants in hardware and doing the four multiplications and two additions in software. In the next step, Verilog HDL code of hardware part of Modified CORDIC accelerator was implemented and verified using Xilinx ISE design suit [39]. The 16 precomputed values of $x_M$ and $y_M$ each for $M = 4$ in Q2.16 format was generated using MATLAB. These values are stored in a lookup table (LUT) in hardware using Verilog HDL for implementing the Equations (36) and (37) of Modified CORDIC algorithm. The last four bits of theta desired $\theta_d$ [15 : 12] form the address of this LUT. The Modified CORDIC hardware accelerator was attached with the Microblaze processor system via FSL bus, using Xilinx Platform Studio (XPS) [39].

**Table 2:** Synthesis results of Modified CORDIC Algorithm and Modified CORDIC Hardware Accelerator

| | Modified CORDIC Algorithm | Modified CORDIC Accelerator |
|---|---|---|
| Max Freq | 212 MHz | 954 MHz |
| Latency | 4.704ns | 1.048ns |
| RAMs | 16x36-bit RAM | 16x36-bit RAM |
| Adders | 5 x 18-bit | 3 x 18-bit |
| Multipliers | 2x(13x18-bit), 2x(18x18-bit) | 0 |
| Xors | 3 | 3 |
| Slice Registers | 52 | 64 |
| Slice LUTs | 129 | 82 |
| Slices | 57 | 35 |

Later, the software part of the Modified CORDIC accelerator was implemented in C programming using Xilinx SDK. The predefined C functions of SDK are used to communicate with the hardware part of Modified CORDIC accelerator via FSL bus. First, the Microblaze sends theta desired $\theta_d$ through FSL bus to the hardware part of Modified CORDIC accelerator. This computes the two constants const1 and const2 in hardware and sends it along with $x_M$ and $y_M$ values, obtained from the LUT to the MicroBlaze processor via FSL bus. Later the four multiplications and two additions are performed in software on the MicroBlaze processor, using the Equations (36) and (37) of Modified CORDIC algorithm. Fig. 10 shows the steps involved in the computation of sine and cosine using the mixed hardware/software Modified CORDIC accelerator.

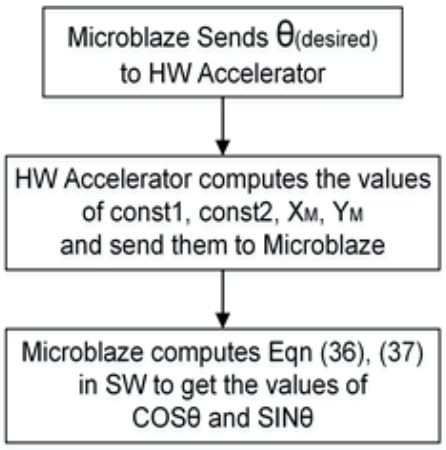


**Figure 10:** Flow chart for Modified CORDIC Accelerator Implementation

**Table 3:** Cycle count and Energy dissipation at clock period 20ns

| Architecture | #Cycles | Power (mW) | Energy* (µJ) |
|---|---|---|---|
| SCORDIC SW | 933 | 178 | 3.3214 |
| SCORDIC Mixed | 601 | 181 | 2.1756 |
| MCORDIC Mixed | 64 | 183 | 0.2304 |

*: Energy dissipation = #cycles × clock period× power.

The cycle count for mixed hardware/software implementation of Modified CORDIC algorithm was measured using the XPS hardware timer block. The mixed hardware/software implementation of Modified CORDIC algorithm takes 64 cycles to compute the values of sine and cosine. The energy dissipation was calculated for the Modified CORDIC mixed hardware/software implementation as shown in Table 3. Our evaluation shows that a Modified CORDIC accelerated embedded processor datapath is 14.5 times more cycle efficient than a datapath lacking a Modified CORDIC accelerator. This design leads to 14 times energy reduc-

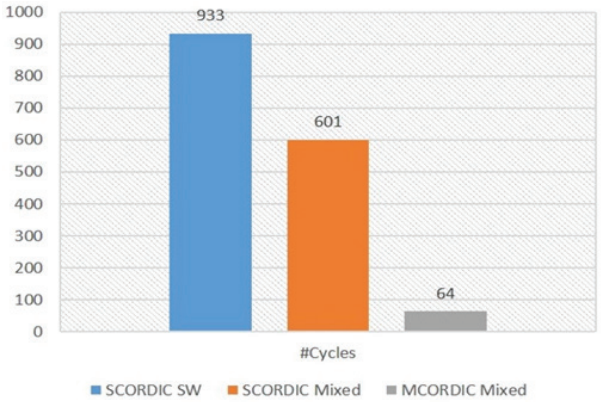


**Figure 11:** Cycle count of different architectures

tion with a very small area overhead. Fig.11 and 12 shows the cycle count and energy dissipation of different architectures, respectively.

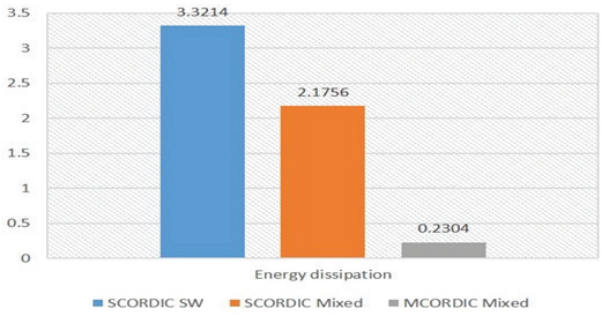


**Figure 12:** Energy dissipation of different architectures

The Modified CORDIC mixed hardware/software implementation is also area efficient as we performed the four multiplications and two additions of Modified CORDIC algorithm in software. This code is executed on the MicroBlaze processor system which results in saving 2x(13x18-bit), 2x(18x18-bit) Multipliers and 2x(18-bit) Adders as shown in Table 2. The Modified CORDIC algorithm and Modified CORDIC hardware accelerator block were synthesized on 7vx485tffg1157-3 Virtex-7 FPGA device. This FPGA device uses a 28nm technology and gives a critical path delay of 4.704ns and 1.048ns respectively as shown in Table 2. The Modified CORDIC hardware accelerator block has 4.5 times reduced latency compared to Modified CORDIC algorithm. Because the four multiplication and two addition operations in the critical path delay have been removed and these operations are performed in software. The Modified CORDIC hardware accelerator block has 4.3 times less latency and takes 4 times less area compared to Standard CORDIC Time Shared implementation. The novelty of the design in the use of Modified CORDIC accelerator is that it takes a single iteration to compute the values of sine and cosine as compared to the Standard CORDIC algorithm, which requires N iterations.

**Table 4:** Delay and Area comparison for FPGA implementations

| Reference | Slices | Clock(MHz) | Latency(ns) |
|---|---|---|---|
| Volder [1] | 1111 | 21.43 | 46.66 |
| Xilinx [43] | 1057 | 37.70 | 26.52 |
| Perwaiz [47] | 978 | 139.87 | 7.15 |
| Zaidi [45] | 769 | 151.73 | 6.59 |
| Ramesh [48] | 373 | 198.27 | 5.04 |
| Aguirre [49] | 276 | 83.99 | 11.90 |
| SCORDIC TS | 148 | 19.3 | 51.52 |
| MCORDIC Proposed | 35 | 954 | 1.048 + $SW_{time}$=11.96 |

Table 4 compares the area and latency of proposed Modified CORDIC mixed hardware/software implementation with other referenced CORDIC FPGA implementation designs. Our proposed technique has reduced area and latency requirements. The latency of proposed Modified CORDIC mixed hardware/software implementation is 1.048ns in addition to the time required to perform the four multiplications and two additions in software. This software code is executed on an embedded processor system using the Equations (36) and (37) of Modified CORDIC algorithm.

## 4 Conclusion

We have presented two novel CORDIC accelerator units using a mixed hardware/software approach. These CORDIC accelerators were integrated with an embedded processor datapath to enhance the processor performance in terms of execution time and energy efficiency. We used Xilinx Spartan-6 FPGA Evaluation Kit and Xilinx Embedded Development Kit (EDK) for the implementation. Xilinx Microblaze soft core processor system was used to execute the software part of CORDIC accelerators. These CORDIC hardware accelerators were attached with the MicroBlaze processor using FSL bus system. The first accelerator was implemented using the Standard CORDIC algorithm. Our evaluation shows that the Standard CORDIC accelerated MicroBlaze processor datapath is 35% more cycle efficient than a datapath lacking Standard CORDIC accelerator. This design also leads to 34% energy reduction. The mixed hardware/software implementation of Standard CORDIC algorithm is area efficient as it saved two 16-bit adders. The second accelerator is implemented using a Modified CORDIC algorithm. Our evaluation shows that a Modified CORDIC accelerated MicroBlaze processor datapath is 14.5 times more cycle efficient than a datapath lacking Modified CORDIC accelerator. This design leads to 14 times energy reduction with a very small area overhead. The mixed hardware/software Modified CORDIC accelerator is area efficient as it saved four multipliers and two adders.

## 5 Acknowledgments

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# Fault Detection in State Variable Filter Circuit Using Kernel Extreme Learning Machine (KELM) Algorithm

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**Abstract:** Electronic applications have become important in industry, science, and everyday life. Modern applications demand greater complexity and smaller packaging, which makes testing more critical. Testing of analog circuit contributes major cost in IC manufacturing. This paper proposes a new method for fault classification in analog circuits using Extreme Learning Machine (ELM) and Kernel ELM algorithms.ELM is a single hidden layer feed forward neural network (SLFN) which chooses the input weight randomly and computes the output weight analytically. The features of the benchmark circuit are extracted by simulating the transfer function of the circuit. The fault dictionary constructed from the features of the circuit is used as the inputs to the ELM and KELM algorithm. Simulation results show that KELM algorithm has better performance at faster learning speed than the ELM algorithm. KELM algorithm outperforms BP-NN-based and ELM-based approaches significantly with effective classification.

**Keywords:** Analog circuits; Neural network; fault detection; Extreme learning machine

# Iskanje napak v filtru na osnovi spremenljivk stanja z algoritmom ekstremnega strojnega učenja na osnovi jedrne funkcije (KELM)

**Izvleček:** Elektronske naprave so postale pomembne tako v industriji kot v vsakdanjem življenju. Moderne naprave zahtevajo večjo kompleksnost in manjše ohišje, kar otežuje njihovo testiranje. Testiranje analognih vezij predstavlja največji strošek proizvajalcev integriranih vezij. Članek predlaga novo metodo klasifikacije napak v analognih vezjih s pomočjo ekstremnega strojnega učenja (ELM) in ELM algoritma na osnovi jedrne funkcije. ELM je skrita enonivojska naprej usmerjena nevronska mreža (SLFN), ki vhodno utež izbere naključno in analitično izračuna izhodno utež. Lastnosti ocenjevalnega vezja so izluščeni s pomočjo simulacij prenosne funkcije vezja. Nabor napak na osnovi lastnosti vezja predstavlja vhod ELM in KELM algoritmu. Simulacije nakazujejo, da ima KELM algoritem boljše lastnosti in izkazuje hitrejše učenje kot ELM algoritem. KELM algoritem močno presega BP-NN in ELM pristope z učinkovito klasifikacijo.

**Ključne besede:** Analogna vezja; nevronske mreže; odkrivanje napak; ekstremno strojno učenje

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## 1 Introduction

The System-on-chip (SOC) technology has raised the importance of analog circuitry, moving it more into mainstream integrated circuit (IC) design. The advancements in IC technology and co-existence of analog and digital signals make testing, a challenging task. Therefore, electronic tests are system dependent and there are different fault diagnosis methods based on the signal nature[1].There are very limited number of testing tools available for analog and mixed signal circuits. Analog and mixed signal IC's have complex functions in which traditional functional testing methods cannot be applied. Analog fault diagnosis is complex and challenging because of the absence of efficient fault mod-

els, component tolerance, and non-linearity [2]. The fault diagnosis of analog circuits is generally classified into Simulation After Test (SAT) and Simulation Before Test (SBT). SBT is suitable for recent research work and is the most preferred [3]. Fault in analog circuits is classified into hard faults and soft faults. Among the various approaches, the approximation methodology can be used for modeling the dynamic system and its failure. Some important approximation models are spline, radial bias function, Artificial Neural Network (ANN), and adaptive fuzzy system. ANN has gained more importance recently in soft fault diagnosis as it has high learning capability [4].

Analog testing includes two parts: Test pattern generation and fault diagnosis. There are many researches in both the parts of the analog testing Pan and Cheng (1999) proposed a novel and cost effective technique for Linear Time Invariant (LTI) analog circuits by deriving hyperplanes in the multidimensional space formed by CUT's parameters. This method has superior classification performance, but has an inadequate testing accuracy [5]. Test generation algorithm based on Support Vector Machine (SVM) is proposed by Long *et.al* which is used for classification [6]. Balivada et.al method of test generation is based on deriving amplitude and phase error from the steady state sinusoidal waveform which is used for fault detection [7]. Hamida et.al proposed and developed software for sensitive testing and generation of test patterns for soft and hard faults [8].

Devanarayanadurg and Soma developed a dynamic programming method based on minmax formulation which is used to construct, test waveforms for on-chip test scheme and this method requires high time cost for large circuits [9]. Long et al proposed a Simulation Before Test (SBT) based method on analog circuits in 2011[10].Yang et.al proposed a method based on the heuristic graph selection approach for the selection of test points to construct fault dictionary [11].Yang et al proposed a continuous fault model using the component connection model (CCM). CCM can find fault location, but the size of CCM increases as the circuit becomes complex [12]. Li and Xie proposed a fault diagnosis method based on Kalman filter. This method is used for diagnosing both parametric and catastrophic faults [13].

Nowadays fault diagnosis based on the machine learning is used for analog circuits. Support Vector Machines (SVM) are widely used as a fault classifier in analog circuits [14-20]. The SVM algorithm maps the lower-dimensional non-linear space into high dimensional feature space for effective classification and provides high accuracy. However, this algorithm involves higher complex computation and time consumption. To solve the above problems, a new fault detection model based on machine learning called Extreme Learning Machine (ELM) [21-25] with lower time consumption and simple process has been proposed in this paper. The accuracy of classification is not sensitive to trade-off parameters and so has good classification performance without optimization of trade-off parameters in compressing the sampled space. ELM provides better generalization performance at a faster learning speed with less human intervention.

The main contributions of this paper are summarized as follows:

(1) The Kernel ELM classifier is proposed to detect faults in analog circuit in an efficient and effective way.
(2) The proposed diagnostic system has achieved excellent classification results compared with the existing methods in previous studies.

The organization of the paper is as follows. Section 2 deals with a brief review of the system description. Section 3 provides a basic description of ELM method. Section 4 describes the Kernel based ELM algorithm and the fault classification by ELM and KELM algorithm. Section 5 discusses simulation results. Section 6 presents the conclusion of the paper.

## 2 System description

The proposed method consists of a sequence of steps as shown in Figure 1. The transfer function with the nominal component value is derived and simulated to obtain the features gain, pole selectivity, and frequency. The faults are injected by varying the component value with step size of 10% within the limit of ±50% and it is simulated. Then, a fault dictionary is created and normalised in the range -1 to 1 and it is then split into training and testing samples and these samples are given as an input to the ELM and KELM algorithms for fault classification.

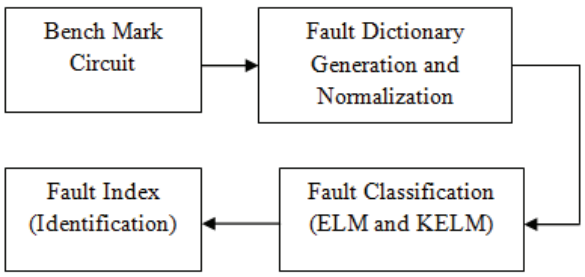


**Figure 1:** Fault detection framework

### *2.1 State Variable Filter*

The State Variable Filter (SVF) is a multiple-feedback type filter circuit that is capable of producing all three filter responses, Low Pass, High Pass, and Band Pass responses simultaneously from the same single active filter design. State variable filter as shown in Figure 2a is a second-order RC active filter consisting of two identical op-amp integrators with each one acting as a first-order, single-pole low pass filter, and a summing amplifier around which the filter gains can be set.

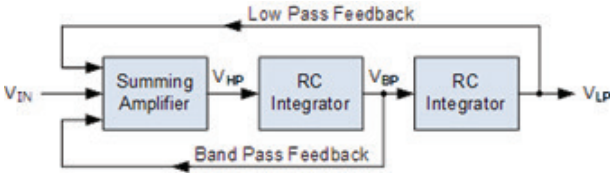


**Figure 2a:** State Variable Filter Block diagram.

The output signals from all the op-amp stages are fed back to the input, allowing one to define the state of the circuit. The main advantage of a state variable filter design is that the main parameters of the filters such as Gain (K), corner frequency ($f_o$) and the filter pole selectivity (Q) can be adjusted or set independently without affecting the filter performance.

The transfer function is the ratio of output voltage to the input voltage. Any Linear time invariant system can be described as a state-space model, with 'n' state variables for an $n^{th}$ order system. The low pass and high pass outputs are phase inverted while the band pass output is maintained in phase relationship. The gain of each output is an independent variable. Due to temperature variation, the component value may vary but must be within the tolerance limit.

The nominal values of the circuit components are:

R1 = R2 = R3 = R4 = R5 = 10kΩ; R6 = 3kΩ; R7 = 7kΩ;
C1 = C2 = 20nF.

The voltage transfer function of the second-order SVF (Figure 2b), considering its low-pass output ($V_o$) is given by

$$\frac{V_o}{V_i}=\frac{-R_5}{R_1}\left[\frac{\frac{R_2/R_5}{R_3C_1R_4C_2}}{S^2+\frac{\left(1+\frac{R_2}{R_5}+\frac{R_2}{R_1}\right)s}{\left(1+\frac{R_7}{R_6}\right)R_3C_1}+\frac{R_2/R_5}{R_3C_1R_4C_2}}\right] \quad (1)$$

Comparing the equation with second order low-pass filter transfer function, following relations for K, Q and $f_o$ is obtained as follows:

$$K=\frac{R_5}{R_1};\ f_o=\frac{1}{2\pi}\sqrt{\frac{R_2/R_5}{R_3C_1R_4C_2}};\ Q=\sqrt{\left(\frac{R_3C_1}{R_4C_2}\right)\left(\frac{R_2}{R_5}\right)}\frac{1+\frac{R_7}{R_6}}{1+\frac{R_2}{R_5}+\frac{R_2}{R_1}} \quad (2)$$

Therefore, the Low Pass Output (LPO) of filter with nominal values of the components yields K= 1.0, Q = 1.11 and $f_o$ = 796HZ.

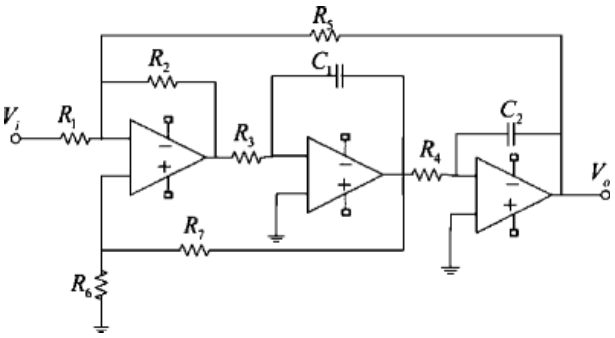


**Figure 2b:** State Variable Filter

The transfer function is simulated with faults injected into the components. The fault injection is done to the extent of ±50% deviation from the nominal value with a step size by 10%. Single fault is introduced to one component at a time ($R_1$) with other fault free components ($R_2$…$R_7$), ($C_1$, C2) taking different random values within their tolerance and then evaluating the parameters K, Q and $f_o$. The feature sets obtained contains 200 samples identified with the fault index $F_1$.The procedure are repeated by fixing the fault level to other components in turn and fault dictionary is generated. A sample fault dictionary is given below in Table 1 for component $R_1$ with 20% fault injection, which is identified with fault index $F_1$

**Table 1:** Fault dictionary

| ANN Input | | | |
|---|---|---|---|
| Fault injected in Component | Gain (K) | Pole selectivity (Q) | Pole frequency ($f_o$) in Hz |
| (10K+20%) R1+20% | 0.872328 | 1.164124 | 795.1364 |
| | 0.872123 | 1.159479 | 794.6936 |
| | 0.867851 | 1.159794 | 796.7802 |
| | 0.869872 | 1.157294 | 796.8162 |
| | 0.870619 | 1.169578 | 795.3414 |
| | 0.870069 | 1.161836 | 795.8468 |
| | 0.872095 | 1.162064 | 795.1361 |
| | 0.869524 | 1.162294 | 795.1274 |
| | 0.870863 | 1.156976 | 794.5657 |
| | 0.834129 | 1.169535 | 796.9395 |

There are totally nine components in the circuit, so that the total fault index is nine for a single fault. The features correspond to component values, gain, pole selectivity, and frequency. The data set obtained contains 1403 samples for training and 450 samples for testing with four features and nine fault indexes for nine components. The fault dictionary sample for $R_1$+20% includes features of gain, pole selectivity and pole frequency and their corresponding sample values are 0.872328, 1.159479 and 794.6936 respectively. A similar procedure is followed to all the components for assigning fault index corresponding to the faulty component and creating a fault dictionary.

## 3 Extreme Learning Machine (ELM)

Extreme Learning Machine (ELM) is a single hidden-layer feed forward neural network learning algorithm. ELM randomly chooses hidden nodes and determines the output weights connected to the hidden neuron in the output of the network analytically. It is to be noted that the ELM algorithm takes less training and testing time and provides good performance. The ELM algorithm is applied to several benchmarking problems and in many cases provides results that are a thousand times faster than the traditional learning algorithms [20].

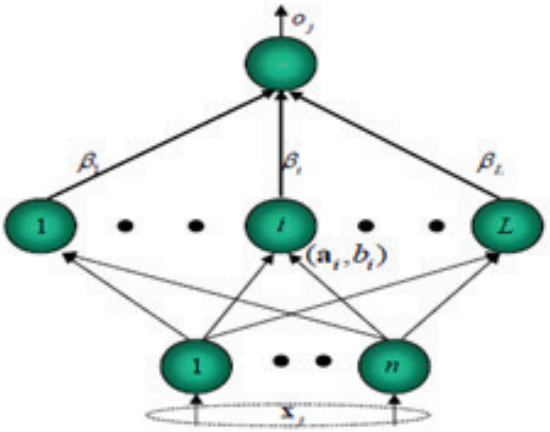


**Figure3:** ELM Architecture

Figure 3 shows the general ELM architecture with a single hidden layer. $X_i$ and $O_j$ are the input and output nodes of the network. $\beta_i$ represents the weight connecting the hidden layer and the output node.

Consider a data set with N samples ($x_i$, $t_i$) where

$x_i = [x_{i1}, x_{i2}, \ldots \ldots, x_{in}]T$
$t_i = [t_{i1}, t_{i2}, \ldots \ldots, t_{im}]T$

The classification problem with SLFN is solved with Ñ hidden nodes and activation function g(x). The output nodes are linear and the output $o_j$ can be expressed as:

$$\sum_{i=1}^{\tilde{N}} \beta_i g_i\left(x_j\right) = \sum_{i=1}^{\tilde{N}} \beta_i g_i\left(w_i x_j + b_i\right) = o_j \; for \; j = 1,2,\ldots.N \qquad (3)$$

Where $w_i = [w_{i1}, w_{i2}, \ldots \ldots, w_{in}]T$ is the weights between the input nodes and the $j^{th}$ hidden node, $\beta_i = [\beta_{i1}, \beta_{i2}, \ldots \ldots, \beta_{im}]T$ is the output weight vector existing between the hidden layer and the output layer, $b_i$ is the threshold of the $i^{th}$ hidden node. The network can approximate the given problem with N samples with zero error if there are N hidden nodes which mean that the following exists.

$$\sum_{i=1}^{\tilde{N}} \beta_i g_i\left(w_i x_j + b_i\right) = t_j \; for \; j = 1,2,\ldots.N \quad \text{where t is the target} \qquad (4)$$

The above N equations can be written as specified below

$$H\ \beta = T \qquad (5)$$

Where

$$H = \begin{bmatrix} g\left(w_1 x_1 + b_1\right).\ldots\ldots g\left(w_{\tilde{N}} x_1 + b_N\right) \\ . \\ . \\ . \\ g\left(w_1 x_N + b_1\right).\ldots\ldots g\left(w_{\tilde{N}} x_N + b_{\tilde{N}}\right) \end{bmatrix} \quad \beta = \begin{bmatrix} \beta_1^T \\ . \\ . \\ . \\ \beta_{\tilde{N}}^T \end{bmatrix} \quad T = \begin{bmatrix} t_1^T \\ . \\ . \\ . \\ t_N^T \end{bmatrix}$$

Given a training set $D = \{(X_i, t_i) : X_i \in R^n, t_i \in R, i=1,2.....N\}$, the number of hidden nodes and hidden node activation functions for extreme learning machine, the algorithm steps are given as follows:

Step 1: Random assignments of the weights between the hidden nodes and the input nodes $w_i$ and the bias of the hidden nodes.
Step 2: Calculation of the hidden layer output matrix H
Step 3: Calculation of the output weight β using: $\beta = H^{\dagger}T$

The $H^{\dagger}$ is generalized Moore-Penrose inverse matrix. The output weight gives the smallest norm least-squares solution for the linear system and gives the unique solution.

## 4 Kernel ELM

Kernel based Extreme Learning Machine (KELM) is a single hidden-layer feed forward neural network learn-

ing algorithm. In KELM, the numbers of hidden nodes are not chosen; it is arbitrarily determined by the algorithm based on the application. The ELM algorithm determines the initial parameters of input weights and biases randomly with simple kernel function. The stability and generalization performance of the KELM algorithm is determined by these input parameters. KELM improves the stability and performance by eliminating feature mapping of hidden neurons and with the group of activation functions. KELM has kernel parameters which are optimized to improve the generalization performance. KELM is used to overcome the drawbacks of ELM algorithm.

The KELM algorithm with fast learning speed and good generalization performance is widely used in many fields. In KELM, the initial parameters of the hidden layer need not be tuned and all nonlinear piecewise continuous functions can be used as the hidden neurons. Considering the N arbitrary distinct samples $\{(x_i, t_i) \mid x_i \in R^n, t_i \in R^m, i=1,2,.....,N\}$ the output function in KELM with L hidden neurons is

$$f_L(x) = \sum_{i=1}^{L} \beta_i h_i(x) = h(x)\beta \quad (6)$$

$\beta = [\beta_1, \beta_2, ....., \beta_L]$ is the vector of output weights between the hidden layer of L neurons and the output neuron and $h(x) = [h_1(x), h_2(x), ....., h_L(x)]$ is the output vector of the hidden layer with respect to the input x and it maps the data from input space to the ELM's feature space.

In order to improvise the generalization performance and to decrease the training error the output weight and training error should be minimized at the same time.

Minimize $\left\|H\beta - T\right\|, \left\|\beta\right\|$ (7)

Where $||H\beta-T||$ is the training error and $||\beta||$ is the output weight.

The least square solution based on Karush-Kuhn-Tuker theorems (KKT) conditions the output weight β which can be written as

$$\beta = H^T\left(\frac{1}{C} + HH^T\right)^{-1} T \quad (8)$$

where H is the hidden layer output matrix, C is the regularization coefficient and T is the expected output matrix of the input samples.

The output function of the KELM learning algorithm is

$$f(x) = h(x)H^T\left(\frac{1}{C} + HH^T\right)^{-1} T \quad (9)$$

If the feature mapping of h(x) is unknown and the kernel matrix based on Mercer's conditions is defined as

$$M = HH^T : m_{ij} = h(x_i)h(x_j) = k(x_i, x_j) \quad (10)$$

The output function of KELM can be defined as

$$f(x) = [k(x, x_1), ....., k(x, x_N)]\left(\frac{1}{C} + M\right)^{-1} T \quad (11)$$

Where $M=HH^T$ and k(x, y) is the kernel function of the hidden neurons of a single hidden layer feed-forward neural networks.

There are many kernel functions such as linear kernel, polynomial kernel, Gaussian kernel, and exponential kernel which satisfy the Mercer condition available from the existing literature. It is observed that different types of kernel activation functions have great influence on the performance of KELM. In this kernel-based ELM, the hidden layer feature mapping $h(x)$ need not to be known to the user. In addition, the number of hidden nodes $L$ need not be specified.

RBF kernels can be randomly generated instead of being tuned. This allows the centers and impact widths of RBF kernels to randomly generate and analytically calculate the output weights instead of iterative tuning. The kernel function of ELM can be any nonlinear bounded integral function which is almost continuous anywhere.

### *4.1 Fault detection and classification using ELM and KELM*

The flow diagram of the proposed ELM and KELM algorithm is shown in Figure 4.The training and testing samples are obtained from the fault dictionary. Seventy five percentages of data are chosen for training and twenty five percentages of data is chosen for testing. The testing and training data are chosen randomly and are normalized in the range -1 to 1.The normalized training and testing data are given as an input to the algorithm. As described earlier, the four dimensional feature vectors consisting of component value, gain, pole selectivity, and frequency are taken as an input for ELM to classify faults. Twenty hidden nodes with various activation functions are used for the ELM. ELM has five input parameters such as training data, testing data, number of hidden nodes, activation function and a parameter to determine regression or classification. The output of the algorithm implementation is the correct detection of the fault index as per the target defined.

The input weights and the bias of hidden neurons are generated randomly. The hidden layer output matrix is calculated from the generated input weights and the bias matrix based on the activation function. The output weight is calculated from the pen-rose inverse of a hidden layer matrix and the target.

In KELM, the kernel matrix is computed using the kernel function and varying the kernel parameter. The output weight is computed from kernel matrix and target. The output weight is the least square solution of the system which produces a minimum error. Minimum error results in high accuracy of fault classification.

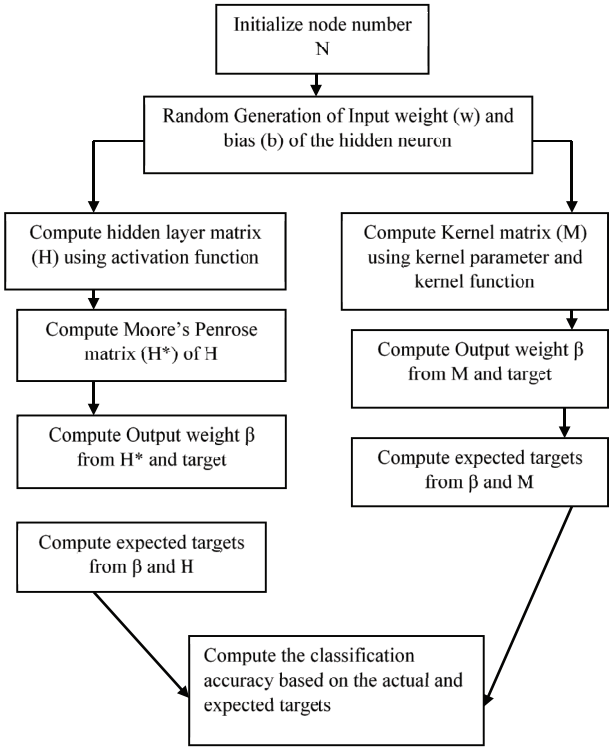


**Figure 4:** Flow diagram for fault detection using ELM/ KELM.

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## 5 Simulation results

### 5.1 Basic ELM implementation results

Fault detection and classification are performed with training and testing samples using the ELM algorithm in MATLAB tool version 2013a. ELM algorithm has five input parameters. The parameters are training set, testing set, parameter to determine regression or classification, hidden nodes, and activation function. The value 0 is used for regression and 1 is used for classification [21, 22].

A set of 1853 samples from the fault dictionary is used where 1403 samples are used for training and 450 samples are used for testing the network. The samples are given as inputs to ELM for fault classification. The number of hidden nodes is varied and the performance measures like training time, testing time, training accuracy and testing accuracy are noted and these parameters are compared for different hidden node values as in Figure 5. Five different activation functions are used in the algorithm, which are sigmoid, sine, hard limit, triangular basis and radial basis function. The performance measures for the five different functions are compared and are shown in Table2.

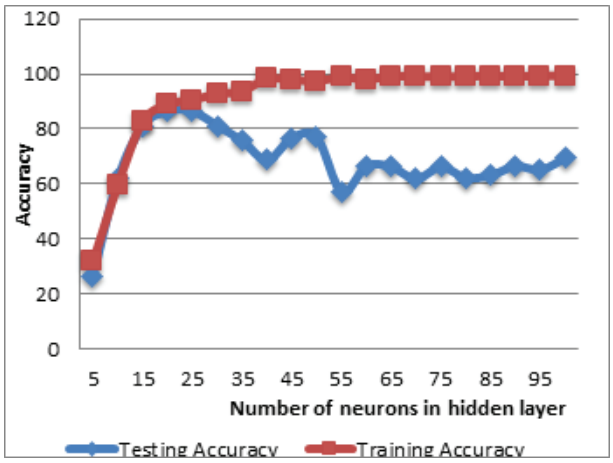


**Figure 5:** Accuracy Performances for Sigmoid Activation Function

Figure 5 shows the training and testing accuracy for different numbers of hidden nodes. The training accuracy increases as the number of node increases and remains stable when the number of nodes is increased beyond 40 and the testing accuracy increases as the number of nodes increases and starts decreasing as the number of nodes is increased beyond 20.

**Table 2:** Performance comparison of ELM with several activation functions

| Activation Function | Training Accuracy % | Training Time Secs | Testing Accuracy % | Testing Time Secs |
|---|---|---|---|---|
| Sine | 87.41 | 0.1250 | 86.67 | 0 |
| Sigmoid | 91.19 | 0.8281 | 82.66 | 0.0313 |
| Hard limit | 70.37 | 0.1094 | 67.04 | 0.0156 |
| Triangular Basis | 89.59 | 0.0781 | 88.15 | 0 |
| Radial Basis | 86.61 | 0.1875 | 82.96 | 0 |

The performance measures of the varied activation functions indicate that the sigmoid activation function produces the optimum performance compared to the

other activation function because it has better misclassification and compressing property.

The performance of ELM algorithm is compared with the BP-NN. BP neural networks are a kind of multilayer feed forward neural network, with a mapping function which has the ability of reverse transmission and error correction. It expresses the system through associative memory and learning input/output parameters of the unknown system. The main function of BP is to repeatedly adjust and train the weights and bias of the network by using the back propagation algorithm to make the output vector and expected vector to become closer. The adjusting and training is not complete until the sum of squares of network output layer error is less than the specified error.

The performances of the algorithms are analyzed by using confusion matrix. The confusion matrix contains information about actual class and predicted class. The matrix describes all the possible outcomes of the result. The possible outcomes of the results are True Positive (TP), True Negative (TN), False Positive (FP) and False Negative (FN). The faults which occurred are correctly identified and are named as TP and faults which do not occur are identified are named as TN. If the faults are identified when the faults actually do not occur, they are named as FP and if the faults are not identified if the faults actually occur they are named as FN. The measures used for analyzing the performance are accuracy, sensitivity, specificity, error, and precision. Accuracy means the proportion of the correctly identified samples to the total number of samples. Specificity is the ability of the methods to identify the normal cases and sensitivity measures the abnormal cases. Error is the measure of the misclassification rate. Precision is the proportion of the positively predicted cases. The above measures are computed using the formulas from the confusion matrix for both the algorithms and the comparison of BP-NN and ELM algorithm is given for testing samples in Table 3.

$$\text{Accuracy} = \frac{TP + TN}{TP + TN + FP + FN} \tag{12}$$

$$\text{Error} = \frac{FP + FN}{TP + TN + FP + FN} \tag{13}$$

$$\text{Sensitivity} = \frac{TP}{TP + FN} \tag{14}$$

$$\text{Specificity} = \frac{TN}{TN + FP} \tag{15}$$

$$\text{Precision} = \frac{TP}{TP + FP} \tag{16}$$

The ELM algorithm with 20 hidden neurons provides training accuracy of the average 97.7% with 0.0781sec training time and testing accuracy of the average 96 % with 0.0625sec testing time. BP-NN takes more training time of 25.656 sec and testing time of 0.0469 sec and provides less testing accuracy of 91% for detecting the faults.

### *5.2 Kernal ELM implementation results*

In the KELM learning algorithm, the learning ability and the generalization performance are influenced mainly by the kernel parameters of different kernel functions. In this paper, the RBF kernel function, linear kernel function, polynomial, and wavelet kernel function are used to construct a different classifier for predicting the faults in state variable filter circuit. ELM with kernels takes no consideration of the feature mapping function h(**x**), input weight **w**, bias b, and the number of hidden layer nodes L. Instead, ELM with kernels concerns only the kernel functions K (**x***i*, **x***j*) and the training samples.

The KELM algorithm has four different types of kernel such as RBF kernel, linear kernel, poly kernel, and wavelet kernel. The algorithm performance for the different

**Table 3:** Performance comparison between ELM and BP-NN.

| Fault index | Accuracy in % | | Error in % | | Precision in % | | Sensitivity in % | | Specificity in % | |
|---|---|---|---|---|---|---|---|---|---|---|
| | BP-NN | ELM | BP-NN | ELM | BP-NN | ELM | BP-NN | ELM | BP-NN | ELM |
| 1 | 91.4 | 95.6 | 8.6 | 4.4 | 89.7 | 81.3 | 52.0 | 78.0 | 98.9 | 97.8 |
| 2 | 91.4 | 98.9 | 8.6 | 1.1 | 69.5 | 95.9 | 82.0 | 94 | 93.1 | 99.5 |
| 3 | 95.6 | 95.3 | 4.4 | 4.7 | 84.9 | 76.4 | 90.0 | 84 | 96.8 | 96.8 |
| 4 | 76.4 | 98.0 | 20.6 | 2.0 | 36.4 | 100 | 64.0 | 82 | 81.9 | 100 |
| 5 | 100 | 95.1 | 0 | 4.9 | 100 | 88.9 | 100 | 64 | 100 | 99 |
| 6 | 82.4 | 93.8 | 17.6 | 6.2 | 17.7 | 65.7 | 60 | 92 | 95.7 | 94 |
| 7 | 89.3 | 96.9 | 10.7 | 3.1 | 75.0 | 78.1 | 48.0 | 100 | 97 | 96.5 |
| 8 | 95.0 | 96.9 | 5.0 | 3.1 | 78.7 | 100 | 96.0 | 72 | 94.8 | 100 |
| 9 | 95.6 | 96.4 | 4.4 | 3.6 | 97.3 | 85.6 | 75.0 | 83.6 | 96.6 | 97.9 |

**Table 4:** Performance of various kernels

| Kernel Type | Kernel Parameter | Training Time(s) | Testing Time(s) | Training Accuracy | Testing Accuracy |
|---|---|---|---|---|---|
| RBF Kernel | 0.01 | 0.1453 | 0.0318 | 100 | 98.77 |
| Linear Kernel | 0.01 | 0.3442 | 0.0221 | 26.09 | 22 |
| Poly Kernel | [0.01 10] | 0.8209 | 0.2172 | 85.74 | 74.44 |
| Wavelet kernel | [0.01 0.01 0.01] | 0.5544 | 0.1321 | 100 | 94.44 |

kernel types are obtained by varying the kernel parameters. The kernel parameter is given in scalar form for RBF and linear kernel. The kernel parameter is given as a vector for polynomial and wavelet kernel. Among the entire kernels, RBF kernel with 0.01 as kernel parameter gives the best result in terms of time and accuracy, and is shown in Table 4. Accuracy performance for various types of kernel is shown in Figure 6.

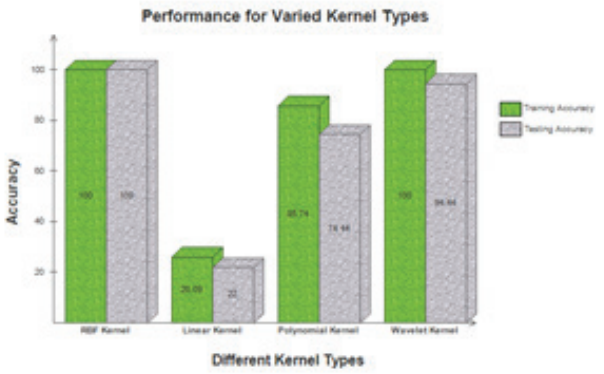


**Figure 6:** Accuracy performance for various kernel types

The testing accuracy and training accuracy for varied RBF kernel parameter is shown in Figure 6a and 6b.

The performance of KELM algorithm with RBF kernel for detecting a single fault in state variable filter is analyzed using confusion matrix and the parameter accuracy, error, precision, sensitivity, and specificity determined are tabulated in Table 5 for testing samples after training is carried out.

**Table 5:** SVF Single Fault -Testing data results

| Fault Index | Accuracy (%) | Error (%) | Precision (%) | Sensitivity (%) | Specificity (%) |
|---|---|---|---|---|---|
| 1 | 98.22 | 1.78 | 93.75 | 90 | 99.25 |
| 2 | 98.67 | 1.33 | 95.83 | 92 | 99.5 |
| 3 | 97.33 | 2.67 | 82.76 | 96 | 97.5 |
| 4 | 98.67 | 1.33 | 92.31 | 96 | 99 |
| 5 | 98.67 | 1.33 | 100 | 88 | 100 |
| 6 | 99.56 | 0.44 | 96.15 | 100 | 99.5 |
| 7 | 99.56 | 0.44 | 100 | 96 | 100 |
| 8 | 99.11 | 0.89 | 94.23 | 98 | 99.25 |
| 9 | 99.11 | 0.89 | 97.92 | 94 | 99.75 |
| Average | 98.77 | 1.23 | 94.77 | 94.44 | 99.31 |

KELM with RBF kernel outperforms that with the other three kernel functions with an accuracy of 98.77%, an error of 1.23%, precision of 94.77%, sensitivity of 94.44%, and specificity of 99.31%.

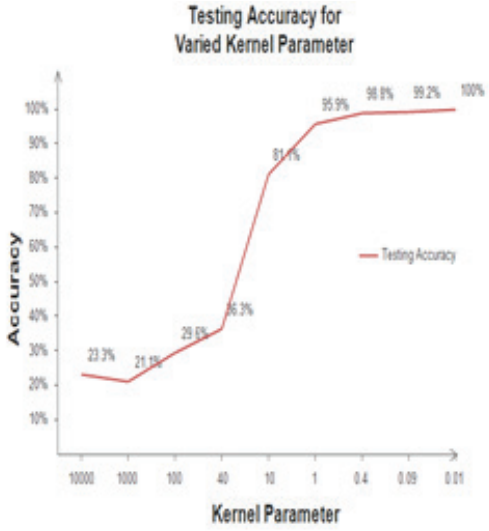


**Figure 6a:** Relationship between the testing classification accuracy and Kernel parameter.

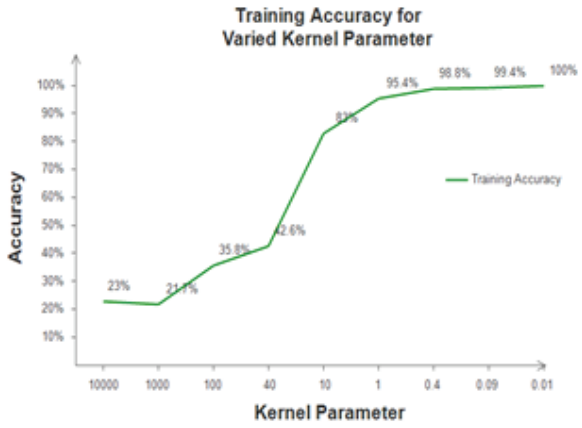


**Figure 6b:** Relationship between the training classification accuracy and Kernel parameter.

## 6 Conclusion

The parametric fault detection is experimented using ELM and KELM algorithms. ELM is a single hidden

layer feed forward neural network (SLFN) and iterative tuning is not needed for the hidden layer. The algorithm randomly chooses the input weight and the bias matrix. The hidden layer output is calculated from the activation function and the randomly generated input matrices. The hidden layer output is used in the computation of the output weight which is used in the calculation of training and testing accuracy. The comparison shows that the sigmoid activation function and twenty hidden neurons of ELM algorithm provides 97.7% training accuracy with 0.0781sec training time and testing accuracy of 96% with a 0.0625 sec testing time. This algorithm saves time efficiently. The result is compared with the BP–NN single layer architecture with the same twenty neurons for the same state variable filter. The training time obtained is 25.656 seconds and the testing time of 0.0469 seconds with testing accuracy of 91%.The results indicate that ELM provides better scalability and generalization performance at faster learning speed. The comparison between ELM and KELM is carried out which shows that KELM provides 100% training accuracy and 98.77% testing accuracy with RBF kernel. The results indicate that KELM achieves higher accuracy performance.

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# MDE-based Rapid DSE of multi-core embedded systems: The H.264 Decoder Case Study

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**Abstract:** The recent advances in Unified Modeling Language (UML) give a valuable milestone for its application to modern embedded systems design space exploration. However, it is essential to remember that UML is unable to solve the difficulty associated with embedded systems analysis, but it only provides standard modeling means. A reliable Design Space Exploration (DSE) process which suits the peculiarities of complex embedded systems design is necessary to complement the use of UML for design space exploration. In this article, we propose a Model Driven Engineering-based (MDE) co-design flow that combines high-level data-intensive application analysis with rapid prototyping. In order to specify the embedded system, our methodology relies on the Modeling and Analysis of Real-Time and Embedded Systems (MARTE) UML profile. Moreover, the present contribution uses the Parameterized and Interfaced Synchronous Dataflow (πSDF) Model-of-Computation (MoC) and a model based on the IP-XACT standard as intermediate levels of abstraction to facilitate the analysis step in the co-design flow. The rapid prototyping process relies on the πSDF graph of the application and a system-level description of the architecture. This paper presents our Hw/Sw co-specification methodology, including its support for gradual refinement of the high-level models towards lower levels of abstraction for design space exploration purposes.

**Keywords:** Co-Design; MP2SoC; MDE; MARTE; πSDF; S-LAM; PREESM; SoC

# Hiter DSE večjedrnih vgrajenih sistemov na osnovi MDE: Primer H.264 dekoderja

**Izvleček:** Najnovejši napredki poenotenega modelirnega jezika (UML) ponujajo pomembne mejnike pri raziskovanju načrtovalskega prostora modernih vgrajenih sistemov. Poudariti pa je potrebno, da ULM ne rešuje problemov analize vgrajenih sistemov temveč določa le standard pri njihovem načrtovanju. Zanesljivo raziskovanje načrtovalskega prostora (DSE), ki ustreza posebnostim kompleksnih vgrajenih sistemov je potrebno za dopolnilno uporabo ULM. V članku predlagamo modelno gnan načrtovalni potek na osnovi inženirskega pristopa, ki združuje analizo podatkovno intenzivne aplikacije na visokem nivoju s hitrim izdelavi prototipov. Določitev vgrajenega sistema temelji na ULM profilu modeliranja in analize vgrajenih sistemov v realnem času. Dodatno, predlagana rešitev vključuje parametiziran in z vmesnikom sinhroniziran (πSDF) model toka podatkov (MoC) in model na osnovi IP-XACT standarda vmesnih nivojev za pospešitev korakov analize v poteku načrtovanja. Hitra izdelava prototipov temelji na πSDF grafih aplikacije in na opisu arhitekture sistemskega nivoja. Članek predstavlja programsko/strojno metodologijo, skupaj s podporo postopne izboljšave od modelov višjih nivojev do nizkih nivojev abstrakcije raziskovanja načrtovalskega prostora.

**Ključne besede:** so-načrtovanje; MP2SoC; MDE; MARTE; πSDF; S-LAM; PREESM; SoC

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## 1 Introduction

At the present time, Massively Parallel Multi-Processors System-on-Chip (MP2SoC) are commonly dedicated to data-intensive processing applications where huge amounts of data are handled in a regular way by means of repetitive computations. As performance presents an important feature of emerging MP2SoCs, the design of such systems should meet strict time-to-market and cost constraints, while holding the guarantee of rising performance through parallelism.

Performance relies on a diverse set of factors (granularity of the application, model of the architecture, partitioning and allocation choices, etc.) and parameters

(number of processing units, memory sizes, etc). Design Space Exploration (DSE) means adjusting these factors and parameters while taking into account a set of metrics (execution time, latency, throughput, energy, etc.) to find the optimal combination between the MP2SoC architecture and the data-intensive processing application at an early phase of the system design. The DSE of complex embedded systems involves three issues which are:

- The modeling effort: which depends on the specification methodology
- The evaluation effort: which depends on the performance estimation techniques and tools
- The results accuracy: which depends on the exploration strategies that reduce the vast design space while reaching accurate performance numbers

Research on the DSE of modern applications running on complex System-on-chip (SoC) is still emerging. Several design frameworks have been suggested enabling high-level system specification. Based on the Model Driven Engineering (MDE) guidelines, the Unified Modeling Language (UML) [1] semantics and the Modeling and Analysis of Real-Time and Embedded Systems (MARTE) [2] profile annotations, these frameworks guarantee a model-based specification methodology that stresses the use of models in the embedded systems development life cycle and argues automation via meta-modeling, model transformation and code generation techniques.

In addition, state-of-the art DSE frameworks rely on different evaluation techniques and exploration strategies. A common practice of embedded systems performance estimation in these approaches [3, 4, 5] is simulation. Although the simulation approach is more accurate, it is often time-consuming to be involved inside the design space exploration loop. Moreover, it requires well-defined rich input models imposing extensive specification efforts. The COMPLEX framework [3], for example, uses MDE foundations for the co-design of embedded systems, but, it directly generates executable files of the system to run a simulation-based DSE process. Providing such an executable model at an early phase of the design process may introduce an unjustified burden when making early design decisions.

On the contrary, analytical design space exploration approaches [6, 7, 8] do not depend on simulators or on running code on real hardware. They rather take high-level specification of the embedded application, combine it with high-level model of the architecture and perform a static analysis to obtain performance measurements for this combination. For this reason, we propose a purely analytical approach based on the high-level analysis of the embedded system. While building a simulation model is computationally costly, analytical estimations can be considered to accelerate the design process.

In this paper, we propose an automatic approach that takes advantage from MDE and MARTE and defines two levels of abstraction that alleviate the analysis and generation of data-intensive processing applications running on multi-processor architectures. The first level is based on a novel extension of the famous Synchronous Data Flow (SDF) [9] Model-of-Computation (MoC), the Parameterized and Interfaced Synchronous Dataflow (πSDF) [10] model. Another level is introduced in our platform-based co-design flow facilitating IP integration, architecture generation and system analysis. This level complies with a model based on the IP-XACT standard [11] named System-Level Architecture Model (S-LAM) [12]. High-level MARTE-based specification of the parallel architecture can be then refined in an MDE-based process to produce S-LAM description of the platform. These two abstraction levels were integrated with the PREESM [13] system-level rapid prototyping tool in an MDE-based co-design flow for complex embedded systems design.

In previous work [14], the UML/MARTE methodology for modeling the data-parallel application and the automatic generation of the πSDF specification have been presented. In [15] the automatic generation from the UML/MARTE specification of the S-LAM description of the architecture was explained. In this paper, a complete overview of the proposed DSE flow is given in Section 2. Moreover, the paper contributes new features not addressed in previous work, specifically the integration of the PREESM rapid prototyping tool inside the DSE framework and the validation of the proposed DSE methodology using a more complex case study (the H.264 decoder) which will be addressed in Section 3.

## 2 The proposed co-design flow

Accurate performance numbers can be reached at the cost of very detailed modeling. On the other hand, a moderate effort for modeling leads to a high-level evaluation task, but the accuracy is lost. In the proposed co-design framework, a balanced tradeoff has been made between design space exploration performance and accuracy allowing for extremely rapid system-level analysis while still yielding reliable estimations. In fact, our framework (Figure 1) is a complete and automatic Computer-Aided Design (CAD) tool for the co-specification, design space exploration and code generation

of MP2SoC systems that totally relies on MDE techniques. Being based on the Eclipse framework, front-end, transformation chains and back-end tools are grouped together in a fully-integrated flow.

### *2.1 UML/MARTE front-end: modeling concepts*

The proposed co-specification methodology supports the description of the architecture, the application, the allocation, and the deployment within a unified UML model. Description of the architecture, the application, and the allocation are declared by means of UML classes (class diagram and composite structure diagram) annotated with MARTE stereotypes (Table 1). Deployment of software and hardware IPs, describing implementation details of application tasks and architecture components, are described using the UML deployment diagram decorated by stereotypes of our proposed deployment profile as shown in Table 1.

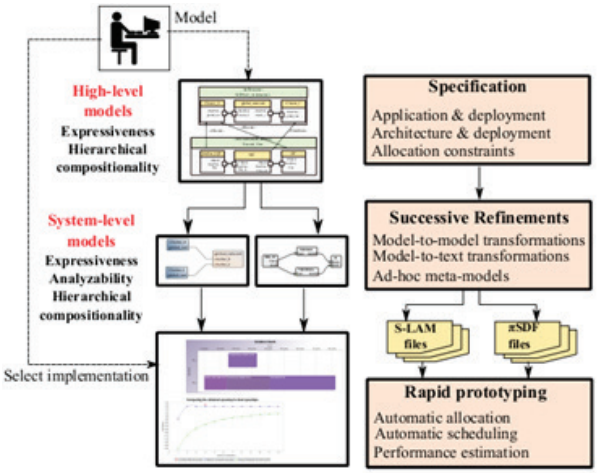


**Figure 1:** Our proposed co-design flow

### *2.2 Refinements and abstraction levels inside the proposed flow*

Two MoCs were introduced in the proposed co-design flow to prune the design-space exploration step: πSDF and S-LAM.

#### 2.2.1 The πSDF MoC

Generally, MoCs can be evaluated based on their expressiveness and analyzability. SDF MoC proved to be a very successful mean providing a good degree of expressiveness while offering a lot of potential analysis [16] [17].

This combination makes this MoC very motivating in the domain of multimedia applications for embedded systems since throughput, storage requirements and latency can be easily estimated using analysis methods. Being able to specify complex hierarchic and parametric dataflow-based applications, the πSDF MoC extends the SDF MoC while preserving expressiveness and analyzability features. This MoC promotes rapid design space exploration and reconfigurable resource allocation of heterogeneous multicore systems. A πSDF graph is a directed graph represented by a tuple G=(A,F,I,π,Δ), where A is a set of actors and F is a set of FIFOs. The hierarchical compositionality mechanism is based on the set of hierarchical interfaces I. Furthermore, dynamism in πSDF relies on π and Δ, which describes respectively the set of parameters and their dependencies.

#### 2.2.2 The S-LAM MoC

To be properly analyzed and prototyped, the hardware architecture part of a given embedded system needs to be described at system-level. The S-LAM MoC, which facilitates such specifications, allows a simple and ex-

**Table 1:** Used MARTE subset for the architecture (HW), the application (Sw), and the allocation models

| Concept | Stereotype | Package | Model |
|---|---|---|---|
| Processing resource | HwProcessor | MARTE:HRM | Hw |
| Storage resource | HwMemory | MARTE:HRM | Hw |
| Communication resource | HwCommunicationResource | MARTE:HRM | Hw |
| Task | SwSchedulableResource | MARTE:SRM | Sw |
| Communication port | FlowPort | MARTE:GCM | Hw, Sw |
| Repetitive component | Shaped | MARTE:RSM | Hw, SW |
| Complex link topology | Tiler | MARTE:RSM | Hw, SW |
| Complex link topology | Reshape | MARTE:RSM | Hw, SW |
| Simple allocation | Allocate | MARTE:Alloc | allocation |
| Repetitive allocation | Distribute | MARTE:Alloc | allocation |
| Hardware component | HwResource | MARTE:HRM | Hw |
| Hardware IP | HwIP | Deployment | deployment |
| Software IP | SwIP | Deployment | deployment |

pressive description while enabling rapid simulations. Being compatible with the IP-XACT model, the S-LAM meta-model does not use the entire IP-XACT meta-model, but it exploits a sub-set of concepts that capture the needed information for the exploration phase [15].

There are two main motivations behind the use of S-LAM as intermediate abstraction level:
Simplicity: S-LAM knows nothing about the implementation details of each component of the hardware architecture while detailing its primary properties
Compositional: S-LAM makes the hierarchical description of the system possible which facilitates the specification of massively parallel architectures complex structure.

### 2.2.3 Refinements using transformation chains

Three transformation chains were defined in our co-design flow. The first transformation generates the πSDF description of the data-parallel application. The second transformation chain generates an S-LAM compliant description of the parallel architecture. And the third chain generates a scenario file, the third design entry of the rapid prototyping tool. The implementation of a transformation flow in the MDE approach relies on the definition of ad-hoc meta-models for each abstraction level. For this reason, three meta-models were proposed: the MARTE and Deployment meta-model, the πSDF meta-model and the S-LAM meta-model. In addition, model-to-model and model-to-text transformations were defined inside the transformation chains as depicted in Figure 2. In our approach, model-to-model transformation rules are defined using the QVTO language [18] and model-to-text transformation rules are described using the Acceleo tool. Following the MDE principles, an automatic transformation was developed to generate a MARTE-compliant model from a UML-based specification. The first model-to-model transformation produces generic models of the application, the architecture and the allocation conform to the MARTE meta-model.

The MARTE to πSDF transformation chain [14] takes as input the generic application model resulting from the first transformation and generates as output a πSDF specification which conforms to the πSDF meta-model. The S-LAM transformation chain [15] generates a model that conforms to the S-LAM meta-model taking as entry point the generic architecture model.
The generated πSDF and S-LAM models should be processed by two model-to-text transformations to produce .pi and .slam files of the application and the architecture. The generation of a scenario file aims at separating the algorithm and architecture constraints from system-level models.

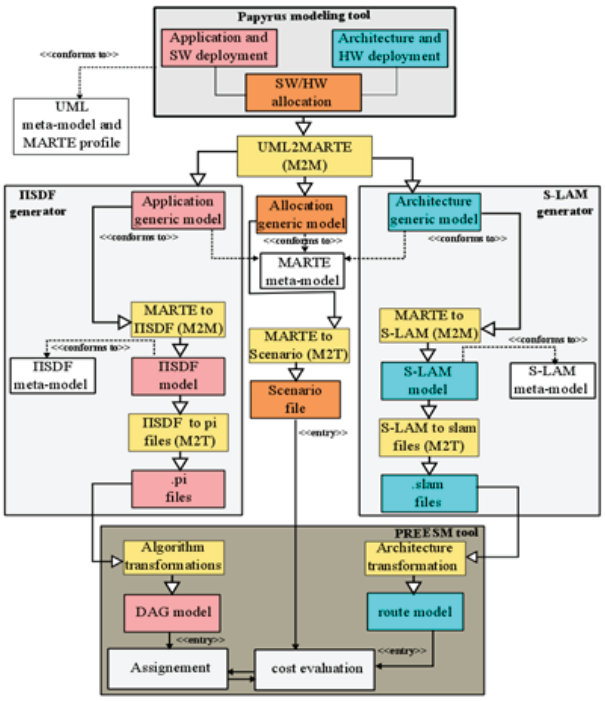


**Figure 2:** Refinements and abstraction levels inside the proposed flow

## *2.3 Rapid prototyping with PREESM*

Based on the previously described steps (co-specification, successive refinements), we described a multi-level design space exploration methodology that relies on high-level models and refinement chains to enhance the rapid analysis of high-performance embedded systems. The final step in the proposed approach is the rapid prototyping of the πSDF/S-LAM combination using PREESM which will be described in this section.

The flexible rapid prototyping process in PREESM consists of exploring the design tradeoffs at system-level while taking into account system constraints and objectives present in the scenario file. The central feature of the rapid prototyping method is the multi-core scheduler. Before starting the scheduling phase, PREESM performs two transformations aiming to expose the parallelism of the application and the architecture. In the one hand, the πSDF graph is transformed into a Hierarchical SDF, then into a Homogeneous SDF and finally into a Directed Acyclic Graph (DAG). The latter will be processed by the scheduler. On the other hand, a route model is generated from the S-LAM model aiming to facilitate the allocation task. The NP-complete scheduling process in PREESM consists of two separate operations:

- Assignment: relies on the DAG model of the application to assign actors to operators

- Cost evaluation: relies on the route model and the scenario to estimate the cost of the proposed solution

Such a scheduling process must satisfy both the data dependencies between tasks of the application and the execution constraints imposed by the execution platform. It also increases predictability, and allows precise performance estimations. At the end of the scheduling process, a Gantt chart of the execution is displayed plotting the optimal schedule. Memory storage requirements and speedup values are also estimated and plotted in different charts.

## 3 Experimental results

Our objective is to illustrate the effectiveness of the proposed co-design framework in terms of rapidity and accuracy of the exploration results. The H.264 decoder application [19], a typical data-intensive signal processing application, is chosen to demonstrate the efficiency of the proposed exploration tools. We mainly focus on a coarse-grain parallelization technique implemented in the literature [20] and try to predict the advantage of running such complex application on massively parallel architectures.

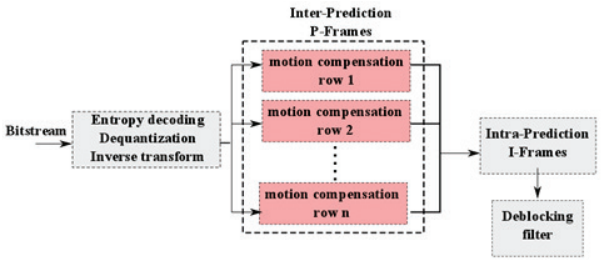


**Figure 3:** Parallel motion compensation application block diagram

### 3.1 The H.264/AVC decoder

Among numerous video compression standards, H.264 seems to be very effective in terms of compression and quality. Providing a compression efficiency gain of 50% compared to previous standards, the H.264 codec proves its effectiveness in high definition systems as well as low resolution devices. The H.264 AVC decoder splits each frame of a given video sequence into macroblocks (blocks of 16 × 16 pixels). These macroblocks are decoded in raser scan order using intra-prediction, inter-prediction and deblocking filter.

With the uncontrollably evolution of video resolutions, the processing time of this decoder keeps increasing. Executing such complex application on parallel cores should solve this problem. However, dependencies, data coherency and synchronization introduced in the intra-prediction, inter-prediction and deblocking filter kernels are challenging characteristics making the parallelization task very hard.

In recent years, coarse-grain and fine-grain parallelization techniques were proposed. Coarse-grain methods allow decoding groups of pictures, frame or slices in parallel. Fine-grain techniques investigate smaller units named macroblocks.

In this case study, we aim to study the motion compensation parallelization technique [20]. This technique divides the frame into rows of independent macroblocks as shown in Figure 3. The motion compensation stage is processed for each row of the frame. The decoder process begins with the entropy decoding. Then, dequantization and inverse transformation are executed on the resulting data. Afterward, every row of macroblocks of a frame is inter-predicted (motion compensation task). At the end, the deblocking filter is applied.

### 3.2 The target model of the architecture

MP2SoC, as presented in Figure 4, is composed of a parametric number of processing elements (PE), grouped into two clusters. The clusters can communicate via a global interconnection network. The first cluster, cluster0, contains one processing element connected to its local memory and can act as a global controller of the architecture. Inside the second cluster, each processing element is connected to its local memory and can communicate to other processors via a local network. The presented architecture [21] is parametric and configurable to satisfy a wide range of systematic signal processing applications. Its design is based on IP assembly approach.

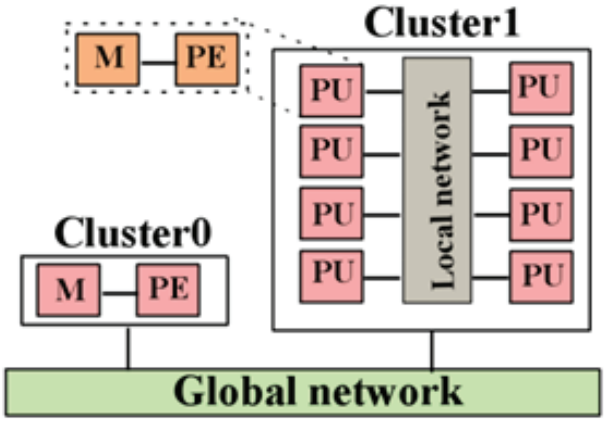


**Figure 4:** MP2SoC architecture

### *3.3 Modeling the H.264 decoder*

In Figure 5, the shaped stereotype associated with the instance of the MC_Row class denotes the data-parallelism of the application. Each repetition of the motion compensation task consumes one input pattern and produces one output pattern. A pattern corresponds to a row of macroblocks.

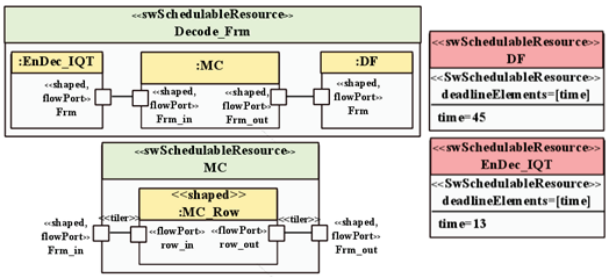


**Figure 5:** Parallel motion compensation in UML

Table 2 summarizes the multiplicities of consumed and produced patterns inside the Decode_Frm and MC classes where X and Y present the number of macroblocks in the horizontal and vertical directions, and nbrow specifies the number of rows processed in parallel. To guarantee accuracy of the exploration results, the deadlineElements attribute of the SwSchedulableResource stereotype is used to specify how much of program execution time each elementary task used as seen in Figure 5.

### *3.4 Modeling the MP2SoC architecture*

Figure 6 shows the UML specification of the MP2SoC architecture. The main component of the architecture, named MP2SoC_Architecture, is composed of two clusters connected via a global network. The Cluster_1 class encloses a parametric number of processing units (PU) specified using the Shaped repetition concept. The Tiler connector (whose attributes are not shown in this figure for the simplicity purpose) between the global_net port of the PU and the global_net port of the Cluster_1 specifies how processing units are regularly connected to the global network.

### *3.5 Partial allocation view of the case study*

Data-parallel splitting of the motion compensation process while leaving parts of the application sequential requires a constrained allocation view that will guide the rapid prototyping process. In Figure 7, the main component of the H.264 decoder and the main component of the hardware architecture are displayed. Since parallel processing is not needed for the EnDec_IQT and DF tasks, they are completely mapped on the processing unit of Cluster_0 via the Allocate links. The data-parallel splitting of the MC_Row task imposes the distribution of the repetitions of this task onto the processing units of Cluster_1 using the Distribute stereotype.

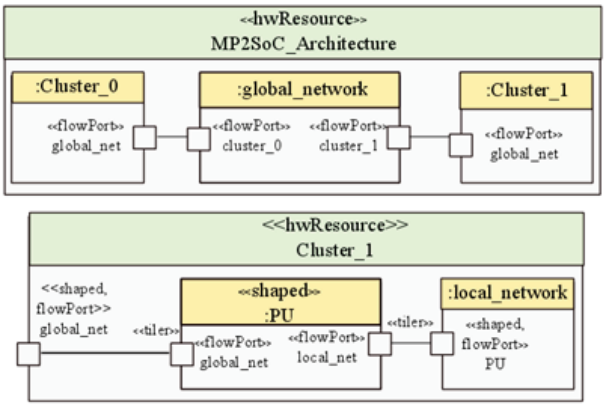


**Figure 6:** MP2SoC UML models

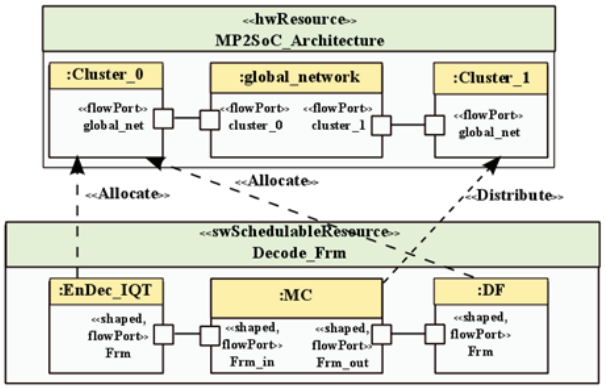


**Figure 7:** Allocation for the motion estimation parallelization

### *3.6 Deployment modeling*

Figure 8 presents the deployment of the PE elementary component onto the PE_IP artifact stereotyped hwIP. This class is deployed on the Nios II processor. The Nios

**Table 2:** Multiplicities inside the parallel motion

| Class | EnDec _IQT | MC | MC | DF | MC_Row | MC_Row |
|---|---|---|---|---|---|---|
| Port | Frm | Frm_in | Frm_out | Frm | row_in | row_out |
| Multiplicity | X × Y | X × Y | X × Y | X × Y | X × (Y ÷ nbrow) | X × (Y ÷ nbrow) |

II processor IP is provided with the hardware library, associated with our framework, which contains processor, memory and communication network IPs. While the filePath attribute facilitates the generation of the MP2SoC source code, the vlnv attribute guides the S-LAM generation process as it gathers required IP properties.

Our framework integrates a source code generator that produces the implementation of a given MP2SoC architecture. Currently, Nios II-based systems can be directly generated from a parameterized specification of the architecture in terms of processor numbers.

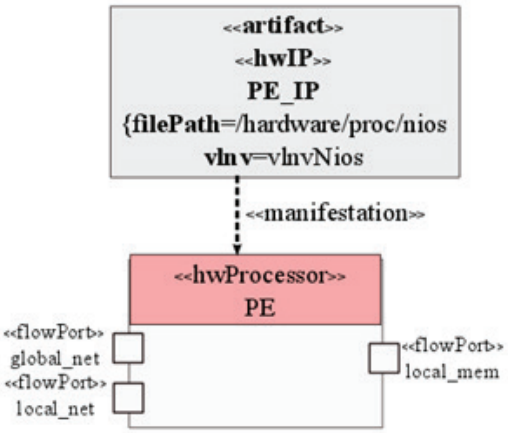


**Figure 8:** Deployment of the PE

### *3.7 Executing transformation chains within the case study*

#### 3.7.1 Generation of πSDF files

Executing the πSDF transformation chain on the parallel motion compensation application generates one πSDF file for each hierarchic class: Decode_Frm.pi (Figure 9(a)) and MC.pi (Figure 9(b)) files. The hierarchic structure of the application is conserved during the transformation phase for the two applications.

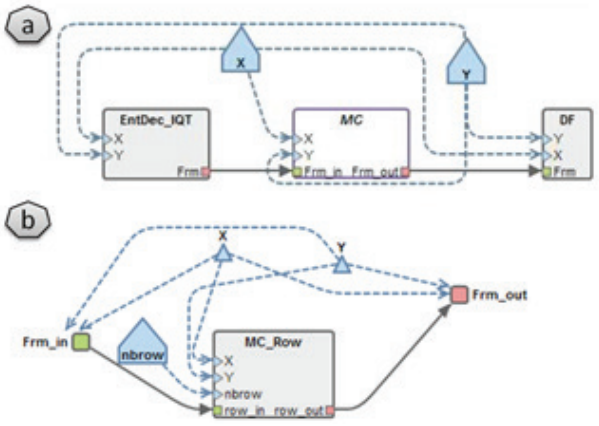


**Figure 9:** .pi files of the parallel motion compensation application

#### 3.7.2 Generation of S-LAM files

Different configurations of MP2SoC were generated varying the number of processing units (by changing the shape value of the PU class). For the rapid prototyping of the parallel motion compensation application, four architectures were produced containing 2, 4, 8 and 16 processing units in the Cluster1. Generating a complete MP2SoC architecture containing 8 processing units is illustrated in Figure 10.

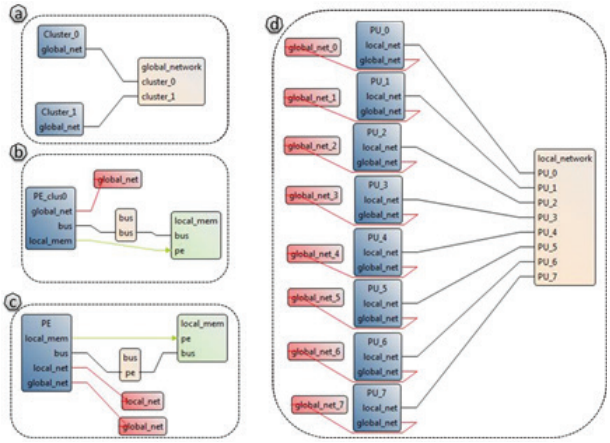

**Figure 10:** S-LAM files of the MP2SoC architecture

### *3.8 Exploration results in the case study*

In the parallel motion compensation approach, the motion compensation task for each row of one P-frame is executed in parallel on different cores. We experiment this parallelization method using the CIF (352 × 288) resolution.

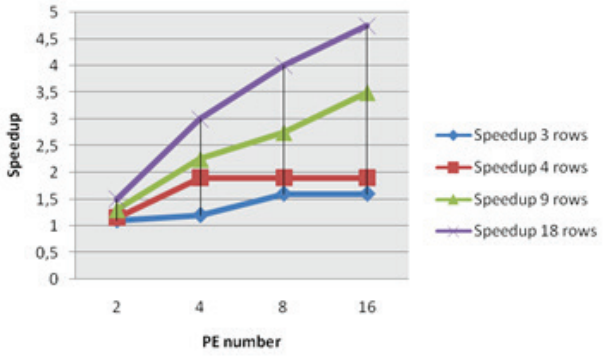


**Figure 11:** Speedup of the parallel motion compensation parallelization method

In CIF resolution, each frame has 22 horizontal macroblocks and 18 vertical macroblocks. Figure 11 shows the average speedup of the motion compensation task for different number of rows. For the CIF resolution, the maximum speedup of 4.75 is reached using 16 processing units and 18 rows. The speedup decreases as the number of rows decreases for the same processing unit

number. In fact, decreasing the row number leads to increasing the number of macroblocks inside each row, the fact that slows down the execution time. In contrary, increasing the row number intensifies the speedup. For example, doubling the row number (from 9 to 18) improves the speedup with 45% in an eight processing units-based architecture. In fact, the scheduler distributes a set of rows of small size on the processing units, once the parallel execution of these rows completes rapidly, it distributes another amount of rows.

The speedup for 18 rows is around 4 when eight processing units are used. Doubling the number of processing units rise the speedup to 4.75 which cannot be considered as efficient as expected since barely a poor improvement of 18% is gained. The main reasons are the extra-time needed for synchronization between processing units and the big amount of data transfer overhead that intensifies the execution time.

## *4 Conclusion*

The starting point of our study is to adapt a methodology for the co-design of complex embedded systems. Previous research works in the co-design domain focus on simulation for system analysis. While some other researches promote elevation of design abstraction levels, they do not benefit from the advantages offered by the MARTE profile and the novel πSDF MoC. The contribution of this paper is the definition of an MDE-based flow that takes as input the UML diagrams specified with the MARTE profile and transforms them into intermediate models corresponding to the πSDF and S-LAM models. These intermediate models add additional semantics and techniques, with the intended goal of analyzing the application, exploring the design space of possible implementations and generating the system implementation.

Component-based approach provides means to decompose a complex system into simpler components. As we have seen in this paper, our framework takes advantage of this approach for the specification of the data-intensive application and the massively parallel architecture. The complex structure of data-intensive applications makes them suitable to compositional or hierarchical design. Compositional design of MP2SoC architectures can be done using hardware components consisting of elementary or composite classes arranged in a hierarchical manner. In Section 3, we described a compositional specification technique that is totally based on the composite structure diagram concepts where a complex application is divided into simpler tasks and a given MP2SoC architecture is specified based on a bottom-up approach that builds the hierarchy of the architecture using elementary components assembling. To benefit from component-based design for MP2SoC systems, the scheduler should be addressed for high performance applications running on clusters.

The static scheduling algorithms implemented within the PREESM scheduler assign tasks to computing resources before applications are executed. At compilation time, task execution time and communication time are supposed to be known and specified as discussed in Section 3. These algorithms, including the list scheduling and the FAST algorithms, are mainly dedicated to scheduling tasks on multi-core systems. Prototyping the H.264 decoder using the scheduling kernel of PREESM brings some limitations including:
Limitations in code generation: the current PREESM code generation supports exclusively static πSDF graphs. A new code generation based on a runtime system name Spider and supporting all πSDF features is currently studied
Lack of energy and area cost estimation: performance is evaluated based on two metrics, throughput and latency. Although the optimization of these constraints is vital when dealing with high-performance applications, power consumption and area occupation remains more important with the ever increasing number of cores inside MP2SoC systems.

Mapping task graph nodes onto clusters means clustering. The task graph clustering approach [22] for scheduling massive parallel tasks on cluster-based architectures seems to be effective for MP2SoC systems. Researches in this field try to combine clustering algorithms with power consumption reduction [23, 24]. These efforts use emerging power reduction techniques, for example, the Dynamic Voltage and Frequency Scaling (DVFS) [25] and try to adapt them for the cluster-based systems. Integrating such technique into the PREESM scheduler seems to be a good direction to support the composition characteristic of the architecture and the application. Another motivating point is that these techniques are based on a DAG description of the application [26], which is the entry point of the PREESM scheduler.

The PREESM scheduler, as seen in Section 2, divides the assignment and cost evaluation tasks into two sub-modules. One advantage of this approach is that additional heuristics, like power and area, can be easily integrated within the cost evaluation kernel. Since the S-LAM model of the application and the scenario file enclosing system constraints are the inputs of the cost evaluation task, additional values needed for the power and area estimation need to be generated from

high-level UML models and encapsulated into these files. These values include the processor frequency, hardware resources occupation area, and power constraints, etc. Attributes associated with stereotypes of the MARTE profile will be used to specify these values.

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# Voltage Mode Electronically Tunable Full-wave Rectifier

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**Abstract:** The paper presents a new realization of bipolar full-wave rectifier of input sinusoidal signals, employing one MO-CCCII (multiple output current controlled current conveyor), a zero-crossing detector (ZCD), and one resistor connected to a fixed potential. The circuit provides the operating frequency up to 10 MHz with increased linearity and precision in processing of low-level input voltage signal, with a very low harmonic distortion. The errors related to the signal processing and errors bound were investigated and provided in the paper. The PSpice simulations are depicted and agree well with the theoretical anticipation. The maximum power consumption of the converter is approximately 2.83 mW, at ±1.2 V supply voltages.

**Keywords:** bipolar transistor circuits; circuit analysis; circuit simulation; error analysis; rectifiers

# Napetostni elektronsko nastavljiv polnovalni usmernik

**Izvleček:** Članek predstavlja novo realizacijo bipolarnega polnovalnega usmernika vhodnih sinusnih signalov z uporabo ene MO-CCCII (večizhodni tokovno krmiljen tokovni ojačevalnik), detektorja ničelnega prehoda (ZCD) in upora vezanih na fiksen potencial. Delovna frekvenca vezja je do 10 MHz z naraščajočo linearnostjo in natančnostjo v procesiranju nizko-nivojhih vhodnih napetostnih signalov z nizkim harmoničnim popačenjem. V članku so raziskane in predstavljene napake pri procesiranju signalov. Teoretična predvidevanja so potrjena s počjo PSPice simulacij. Največja poraba energije ojačevalnika je 2.83 mW pri napajalni napetosti ±1.2 V.

**Ključne besede:** vezja bipolarnega tranzistorja; analiza vezij; simulacije vezij; analiza napak; usmernik

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## 1 Introduction

Rectification is the essential and demanding aspect of signal processing in instrumentation, measurement and control. Rectifiers are widely applied in signal processing, signal–polarity detectors, amplitude modulated signal detectors, AC voltmeters and ampermeters, watt meters, RF demodulators, function fitting error measurements, RMS to DC conversions, sample and hold circuits, peak value detectors, clipper circuits [1-3], etc.. Owing to the threshold voltage of diodes, conventional diode rectifiers are limited and are only used in specific applications, such as DC voltage supplies. However, simple diode rectifiers cannot be used for applications requiring accuracy in the threshold voltage range. This can be overcome by using high precision integrated circuit rectifiers.

Although the use of current-mode (CM) active devices is restricted to current processing, it offers certain advantages such as higher usable gain, more reduced voltage excursion at sensitive nodes, greater linearity, lower power consumption, wider bandwidth, better accuracy and larger dynamic range compared to that of their voltage-mode counterparts. The CCII is a reported active component, especially suitable for the class of analog signal processing. However, the CCII cannot control the parasitic resistance at $x$ ($R_x$) port, therefore – when it is used in some circuits, it inevitably requires external passive components, especially resistors [2]. This makes it inappropriate for IC implementation, as it occupies a greater chip area, high power dissipation and excludes electronic controllability. On the other hand, the recently introduced second-generation current controlled conveyor (CCCII) has the advantage of electronic adjustability over the CCII [4]. Also, the use of dual-output current-conveyors is found to be useful in the derivation of current-mode single input circuits.

In order to improve performance of OA-based circuits the use of the current conveyor was proposed in [5]. The full-wave rectifier [6], with a single three-output CCCII, two MOS transistors and a resistor with large cross-over distortion, was able to perform rectification at lower frequencies, e.g. 5 kHz. The papers [7-8] described full-wave rectifier circuits based on usage of two second-generation current conveyors (CCIIs) and four diodes. The rectifier circuits [9-10] offer a wide dynamic range and show a broadband operation thanks to the use of a CMOS class AB amplifier and current rectifier operation. The rectifier capable of providing output voltages nearly at the level of the input voltage combined with low power consumption is described in [11], which was also achieved through the circuit design proposed here. In [11], CMOS integrated active rectifier concept as an innovative approach for higher efficiencies is used.

A full-wave rectifier proposed in [12] is based on the usage of two plus-type second-generation current conveyors (CCII+s) and three MOSFETs. A voltage-mode (VM) rectifier with high-input impedance using dual-X current conveyors (DXCCII) and three MOSFETs, without passive components, is described in [13]. In [14], the current-mode (CM) rectifier uses two CCII+s and four diodes. The CM rectifier based on one current conveyor and one universal voltage conveyor (UVC) and two diodes is introduced in [15]. The circuits proposed in [16] employ at least two current and/or voltage conveyors as active elements and two diodes, and works in CM. A CM full-wave rectifier circuit with one active element – current differencing transconductance amplifier (CDTA) and four diodes and one resistor is reported in [17]. The circuits proposed in [18-19] are designed based on MOS transistors with fairly simple structure. The rectifier [18] requires a floating input voltage source, while the circuit [19] needs three external bias current sources to be realized separately. The circuits in [20], [21] use CDTA or DXCCII which have more complex internal structures with respect to CCII and DVCC. A CM full-wave rectifier based on a single modified Z-copy current difference transconductance amplifier (MZC-CDTA) and two switches is reported in [22].

This paper presents the principles of operation, and the detailed circuit design of the new bipolar realization of the full-wave rectifier. The features of the proposed circuit are: it employs one MO-CCCII, one zero-crossing detector, and one resistor connected to source voltage, which is suitable for fabrication in a monolithic chip. Unlike the rectifier described in [2-3], which was realized using the CMOS technology, the one described in this paper involves a simpler and more accurate control structure. Besides, the proposed circuit does not require a more precise bias voltages realization and complex transistor pairing, which was typical of the realizations described in [2-3]. The rectifier circuit provides the operating frequency of up to 10 MHz, with increased linearity and precision in processing of low level input voltage signals. The performance of the proposed circuit is illustrated by PSpice simulations, showing a good agreement with the calculation. The circuits proposed in this paper have been compared to similar circuits reported in literature.

## 2 Proposed full-wave rectifier circuits

Fig. 1 presents the proposed circuit of the full-wave rectifier.

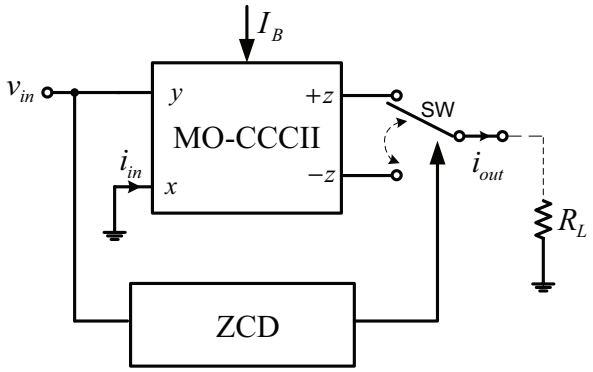



**Figure 1:** The proposed circuit of the full-wave rectifier

Conceptually, the rectifier presented in Fig. 1 is very similar to the one proposed in [6], the former, however, having more precise and new zero-crossing detection (ZCD) circuits, and without shunting of the high output of MO-CCCII. The proposed ZCD circuits demand considerably less resistance in the output stage (50 times) compared to the realization in [6]. This modification ensures greater linearity rectification within a wider frequency range. Additionally, this configuration imposes no limitations in realization of the analog switch, contrary to the circuit described in [6].

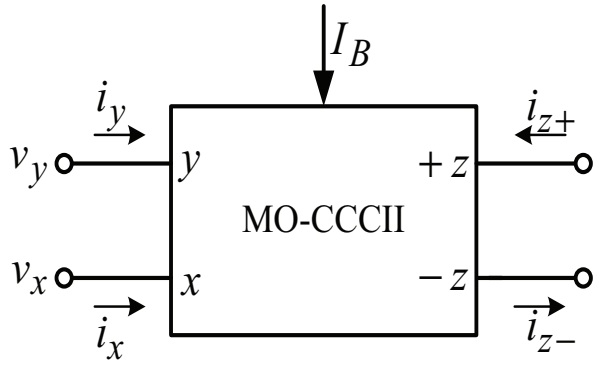



**Figure 2:** Electrical symbol of MO-CCCII

Generally, a MO-CCCII is a multiple-terminal active building block, as shown in Fig. 1. The electrical symbol of the MO-CCCII is shown in Fig. 2.

The port relations of the MO-CCCII can be presented by the following equation:

$$i_y = 0; v_x = v_y + i_x R_x; i_{z+} = +i_x; i_{z-} = -i_x \quad (1)$$

The schematic bipolar realization is shown in Fig. 3 [23]. According to equation (1), the MO-CCCII has a unity voltage gain between terminal *y* and *x* and a unity current gain between terminal *x* and *z*. The $R_x$ is an inner resistance of a translinear mixed loop ($Q_1$ to $Q_4$) with grounded resistor equivalent controlled by bias current $I_B$. In this case, the parasitic resistance $R_x$ at the terminal *x* can be expressed by:

$$R_x = \frac{V_T}{2I_B} \quad (2)$$

where $V_T$=26 mV at 27° C is the usual thermal voltage given by *kT/q*, *k*=Boltzmann's constant=1.38×10-23 J/K, *T*=the absolute temperature (in Kelvin's), and *q*= 1.6×10-19 C and $I_B$ (Fig. 1) is the bias current of the conveyor which remains tunable over several decades.

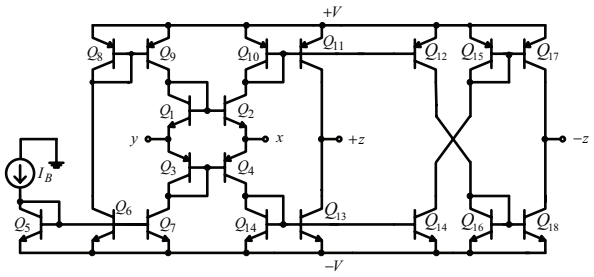



**Figure 3:** Bipolar realization of MO-CCCII

Precision in processing of the input voltage signal is directly dependent on the manner in which ZCD is able to reliably detect the moment when the input signal changes the polarity. This required the construction of new bipolar detector circuits, as shown in Fig. 4. The transistors $Q_{19}$ and $Q_{20}$ will promptly follow the variations in input voltage, thus reducing the total delay time of the comparator. The resistor $R_1$ has one end attached to the source from which it is powered together with the detectors. The resistor can be coupled to the source of a different voltage level, if this should prove necessary due to the demands of analog switches (realized with two complementary MOS transistors).

By the routine analysis of the proposed full-wave circuit shown in Fig. 1 and using the properties of MO-CCCII, for $v_{in}$>0, the *z*+ current ($v_{in}/R_x$) to pass on to the load. For $v_{in}$<0, *z*– current ($-v_{in}/R_x$) passes on to the load, thus inverting the negative cycle of input:

$$i_{out} = i_{z+} = \frac{v_{in}}{R_x}, \quad v_{in}(t) \geq 0 \quad (3)$$

$$i_{out} = i_{z-} = -\frac{v_{in}}{R_x}, \quad v_{in}(t) < 0 \quad (4)$$

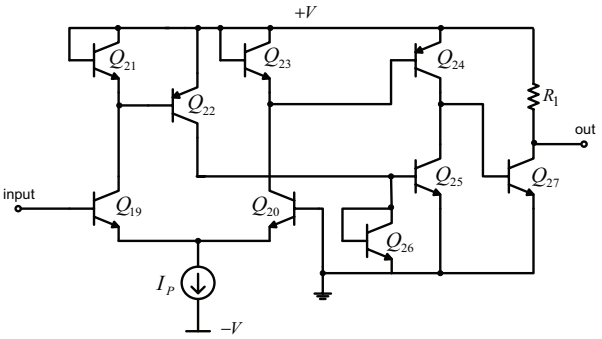



**Figure 4:** Bipolar realization of comparator

Unidirectional current flows through the load in either case, resulting in a full-wave rectified output.

Depending on the detected sign of the input signal (practically by detecting the negative half-period of input processing signal), over the ZCD (Fig. 1), the position of the switch SW (two complementary MOS transistors) can be determined. The control voltage signal, obtained on the output of the ZCD, defines the position of the switch SW and brings the current either from port *z*+, or from port *z*- of the MO-CCCII. Such control enables the current input from the port *z*+ on the load at the interval at which the input voltage signal is positive, i.e. from the port *z*- when the input voltage is negative. The output voltage $v_{out}$ for input $v_{in}$ is as follows:

$$v_{out} = \frac{R_L}{R_{in}} v_{in}; \quad v_{in} \geq 0 \quad (5)$$

$$v_{out} = -\frac{R_L}{R_{in}} v_{in}; v_{in} < 0 \quad (6)$$

where $R_{in}$=$R_x$. The equations (5) and (6) can be presented in form:

$$v_{out} = \frac{R_L}{R_{in}} |v_{in}| \quad (7)$$

Based on (7), it is obvious that the voltage value at the output of the proposed circuit corresponds to the rectified value of the input sinusoid signal with amplification or rectifier with attenuation. In the proposed

circuit, rectification is not performed by diodes, which implies fewer ripples, compared with the known diode rectifier circuits [14-17]. It is also possible to perform low-voltage (below threshold level of the diode) rectification using the proposed circuit.

## 3 Non-ideal Effects

The effects of MO-CCCII and comparator non-idealities on the full-wave rectifier performance are to be considered in this section. By considering the non-ideal MO-CCCII characteristics, equation (1) can be rewritten as:

$$i_y = 0; v_x = \alpha v_y + i_x R_x; i_{z+} = +\beta_p i_x; i_{z-} = -\beta_n i_x \quad (8)$$

where $\alpha$=1-$\varepsilon_v$ and $\varepsilon_v$ ($|\varepsilon_v|$<<1) represents the voltage tracking error from $y$ to $x$ terminal, $\beta_p$=1-$\varepsilon_p$ and $\varepsilon_p$ ($|\varepsilon_p|$<<1) denotes the current tracking error from $x$ to $z$+ terminal, while $\beta_n$=1-$\varepsilon_n$ and $\varepsilon_n$ ($|\varepsilon_n|$<<1) stands for the current tracking error from $x$ to $z$- terminal of the MO-CCCII, respectively. Generally, these tracking factors remain constant and frequency independent within low to medium frequency ranges. Typical values of the non-ideal current transfer gains and the transconductance inaccuracy factor $\alpha$, $\beta_p$ and $\beta_n$ range from 0.9 to 1, with an ideal value of 1. However, at higher frequencies these tracking factors become frequency dependent. Given the non-idealities, currents generated from MO-CCCII can be defined as:

$$i'_{out} = i_{z-} - i_{z+} = (\beta_p - \beta_n)\frac{\alpha v_{in}}{R_{in}} \quad (9)$$

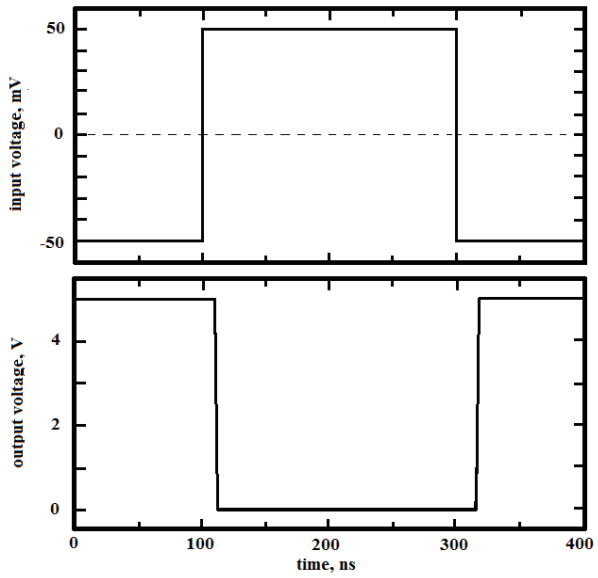
$$i'_{out} = 2\beta_p \frac{\alpha v_{in}}{V_T} I_B = 2\beta_p q \frac{\alpha v_{in}}{kT} I_B, \qquad v_{in}(t) \geq 0 \quad (10)$$

$$i'_{out} = -2\beta_n \frac{\alpha v_{in}}{V_T} I_B = -2\beta_n q \frac{\alpha v_{in}}{kT} I_B, \quad v_{in}(t) < 0 \quad (11)$$

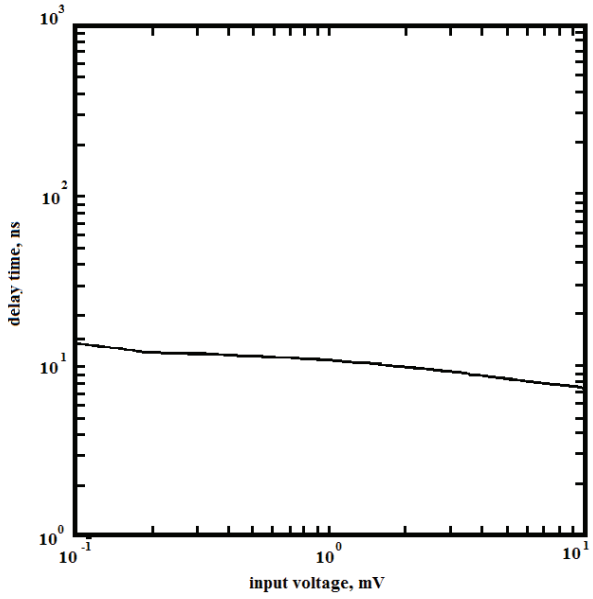
which results in an absolute error as:

$$Error = \left| i_{out} - i'_{out} \right| \quad (12)$$

As for equations (10) and (11), the tracking errors slightly change the output current of the proposed full-wave circuits. However, the above relation does not include error when determining the interval in which the input voltage signal is negative (the ZCD error), which also defines the precision of the proposed rectification process. Fig. 5 a) shows the waveform of the output voltage in response to an input voltage step of ±50mV for the proposed comparator. In Fig. 5 b), the average delay times of the proposed comparator as a function of the input voltage amplitude is reported. As can be seen, at low input voltages, the response time of the proposed circuit is very small. The higher the input voltage, the lower the delay time, as the enhanced output voltage swing (due to the higher voltage values) causes $Q_{19}$ and $Q_{20}$ to completely turn-off. Simulation results confirm the fact that the proposed ZCD circuits are capable of high precision processing of the input signal. It is assumed that the incremental sensitivities of the output current $i_{out}$ at parameters $\alpha$, $\beta_p$, $\beta_n$ and $T$ are: 1; 1; 1 and -1 (all the active and passive sensitivities are of an equal unity in magnitude). Thus, the proposed circuit exhibits a low sensitivity performance.




a)




b)

**Figure 5:** a) Output voltage waveforms for proposed ZCD, b) Average delays time against input voltage

The error (12) is a function of input voltage signals and varies depending on its content. A way to express the error is to consider the values of the observed parameters as random quantities characterized by their PDFs (Probability Density Function). Therefore, the interval having a 2ε width, around the nominal value of the observed parameters needs to be defined and associated with a certain distribution, e.g. uniform distribution.

The Monte Carlo approach [24] gives the lower and upper limits of interval which contains 95% of error samples. The Monte Carlo analysis in PSpice was used for simulations with a given error on different parameters and components (Monte Carlo predicts the behaviour of a circuit statistically when part values are varied within their tolerance range by 5%), Fig. 6. This test is very useful for visualizing how a circuit runs with imperfect parameters as are used in reality. The number of individual simulation was 2000.

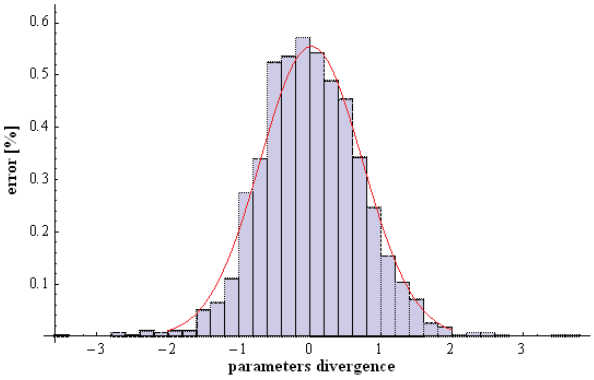



**Figure 6.** The distribution of errors, for the divergence in the value of the parameters, from their nominal values

## 4 Simulation Results

To confirm the given theoretical analysis, the proposed voltage-mode bipolar full-wave circuit in Fig. 1 was simulated using the PSpice program. The MO-CCCII and ZCD were realized by the schematic bipolar implementations given in Figs. 3 and 4, with the transistor model parameters of PR200N (PNP) and NP200N (NPN) of the bipolar arrays ALA400 from AT&T [25], Table 1. The supply voltages and the values of the bias currents were +V=–V=1.2 V and $I_p$=300 μA respectively, whereas the input voltage was within the range of ±100 mV. Parameters of National Semiconductor circuits AH510 [26] were used as analog current switch during simulation.

**Table 1:** PR200N and NP200N transistor parameters

| Transistor type: NP200N |
|---|
| .MODEL NX2 NPN RB = 262.5 IRB = 0 RBM = 12.5 RC = 25 RE = 0.5 IS = 242E - 18 EG = 1.206 XTI = 2 XTB = 1.538 BF = 137.5 IKF = 13.94E - 3 NF = 1.0 VAF = 159.4 ISE = 72E - 16 NE = 1.713 BR = 0.7258 IKR = 4.396E - 3 NR = 1.0 VAR = 10.73 ISC = 0 NC = 2 + TF = 0.425E - 9 TR = 0.425E - 8 CJE = 0.428E - 12 VJE = 0.5 MJE = 0.28 CJC = 1.97E - 13 VJC = 0.5 MJC = 0.3 XCJC = 0.065 CJS = 1.17E - 12 VJS = 0.64 MJS = 0.4 FC = 0.5 |
| **Transistor type: PR200N** |
| .MODEL PX2 PNP RB = 163.5 IRB = 0 RBM = 12.27 RC = 25 RE = 1.5 IS = 147E - 18 EG = 1.206 XTI = 1.7 XTB = 1.866 BF = 110.0 IKF = 4.718E - 3 NF = 1 VAF = 51.8 ISE = 50.2E - 16 NE = 1.65 BR = 0.4745 IKR = 12.96E - 3 NR = 1 VAR = 9.96 ISC = 0 NC = 2 TF = 0.610E - 9 TR = 0.610E - 8 CJE = 0.36E - 12 VJE = 0.5 MJE = 0.28 CJC = 0.328E - 12 VJC = 0.8 MJC = 0.4 XCJC = 0.074 CJS = 1.39E - 12 VJS = 0.55 MJS = 0.35 FC = 0.5 |

Time response of the proposed ZCD circuits is shown in Fig. 7, where the input voltage signal is of 1 MHz frequency and 20 mV peak. Resistor $R_1$=1 kΩ was used in the simulation process. This clearly infers that the proposed solution detectors are able to sense polarity of the input voltage signal with high precision, whereby the error resulting from imprecision in detection is negligible in practical applications.

The DC characteristic of the proposed circuit at a frequency of 1 MHz is shown in Fig. 8. Fig. 8 implies that

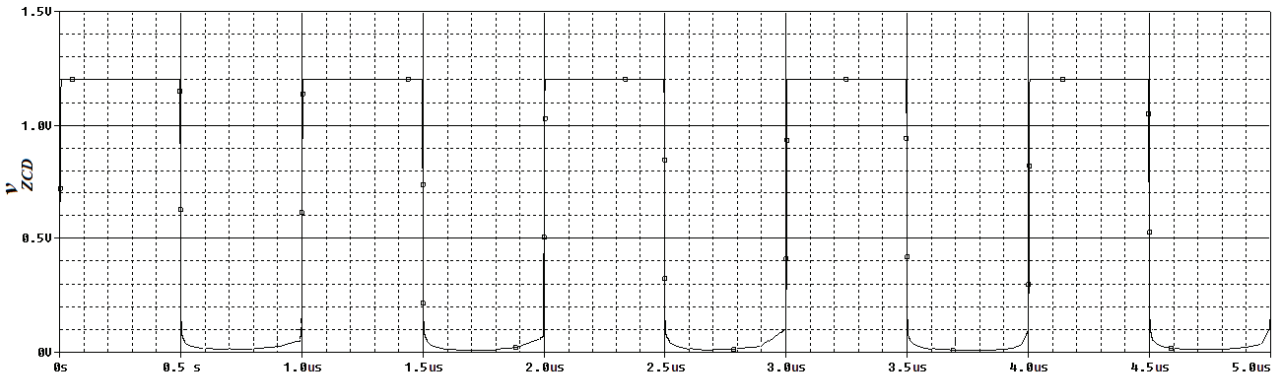



**Figure 7:** Time-domain response of proposed ZCD

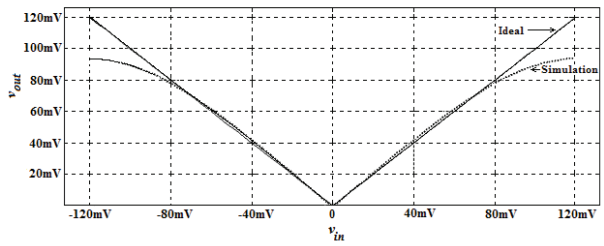
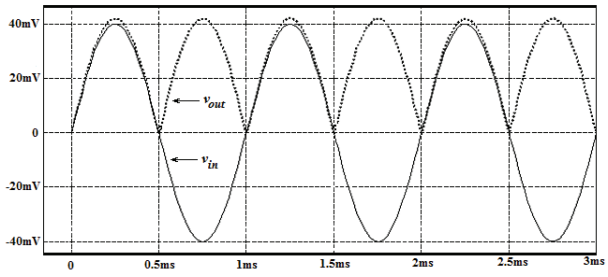



**Figure 8:** DC transfer characteristics for the proposed rectifier circuit

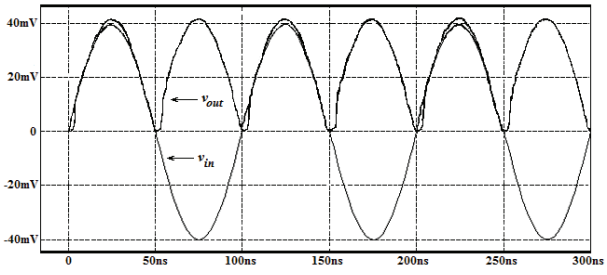
the proposed circuit retains a linear character in a wide voltage range.

Fig. 9 shows the wave form of the signal at the output of the circuit shown in Fig. 1 (voltage $v_{out}$), at different frequencies. For these simulations, the input signal is taken as a sinusoidal voltage signal at 40 mV peak value, the selected frequencies ranging from 1 kHz to 10 MHz. Fig. 9 shows that the output waveform of the proposed rectifier is in a good agreement with the theoretical ones at low and high frequencies. However, the higher the frequency of the processed signal, the greater the deviations.

The total power dissipation was 2.83 mW. Low power consumption of the proposed circuits occurs due to the application of low-voltage current mode and transconductance mode integrated circuits, along with the use of bipolar transistor technique. Applying the current mode signal processing to solve the issues under consideration is a sensible approach to the problem. However, similar and sometimes lower power consumption can be achieved using CMOS technology instead of the bipolar one.




a)




a)

**Figure 9:** Time-domain response of the proposed full-wave rectifier for different frequencies of a) 1 kHz and b) 10 MHz

To test the tunability of the gain of the proposed rectifier circuit, the bias current of the MO-CCCI ($I_B$) is changed and the results are shown in Fig. 10. For these simulations, the input signal is taken as a sinusoidal voltage signal with 100 kHz frequency and 50 mV peak value at a load of $R_L$=100 Ω.

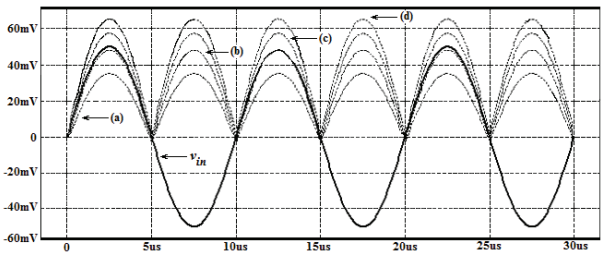



**Figure 10:** Tunability of the gain of the proposed rectifier with changing the bias current $I_B$ a) $I_B$=200 μA; b) $I_B$=130 μA; c) $I_B$=115 μA; d) $I_B$=100 μA

### *4.1 Harmonic distortion*

A further indication of the performance of each of the full-wave rectifiers can be gleaned by examining the distortion already present in a full-wave rectified signal. When a sinusoidal signal of frequency *f* is applied to a full-wave rectifier, the steady-state response at the output ideally consists of harmonic components at 2*f*, 4*f*, 6*f*, etc. [2]. The harmonics in the signal causes the distortion in the output of the circuit. Because of its periodic nature, these harmonic components can be analyzed by the Fourier series (with fast Fourier transform using PSpice).

In the case of a full-wave rectifier, the steady-state response at the output consists of even harmonics. Fig. 11 shows the total harmonic distortion of the output voltage of the proposed circuit, Fig. 1. The THD of the proposed circuit is -15.6 dB at 50 Hz and -20.8 dB at 1

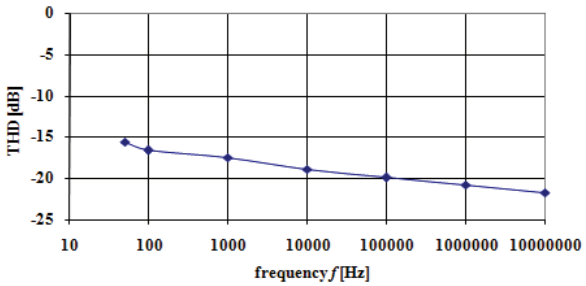



**Figure 11:** Total harmonic distortion (THD) versus frequency at input amplitude voltage of 50mV

MHz with an input signal of 50 mV. The THD is significantly lower than in [2], [27], [28] (the THD of previously reported circuit slowly increases with frequency), because of higher frequency ranges, the diode switching ON and OFF tends to become sluggish due to its higher impendence and more distortions.

### *4.2 Comparison with the Existing Circuits*

To gain a better insight into the technique proposed here, the performance of the proposed circuits was compared to the previous one implementing full-wave rectifiers. Table 2 summarizes this comparison by showing some important parameters of the rectifiers. It should be assumed here that not all of the comparison realizations rely on the concept of a voltage-mode circuit, as is the one proposed in this paper.

The proposed rectifier requires fewer active components than the one described in [2], [22], [27], [31], along with lower THD of the output voltage and lower consumption. Additionally, the circuit described in this paper enables electronic control of the gain of the proposed rectifier circuit (amplitude of the output voltage signal).

## *5 Conclusion*

In this paper, new full-wave rectifier topologies are given. The circuit employs only two active components and one resistor operating in VM, which is advantageous from the integration point of view. The performance of the proposed circuits is demonstrated by PSpice simulations using the bipolar arrays ALA400 from AT&T technology parameters. The effects of the non-idealities of the active elements are also investigated. The proposed circuit has a high precision and linearity, low power consumption and wide bandwidth.

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**Table 2:** Comparison of performance of different rectifiers

| Ref. | Type of active building blocks used | Number of diodes | Number of resistors | Auxiliary bias sources | Maximum frequency | Maximum amplitude | Power consumption |
|---|---|---|---|---|---|---|---|
| [2] | 4 CCCII, 3 MOS | - | - | yes | 20 MHz | ±1 V | 9.43 mW |
| [6] | 1 CCCII, 2 MOS | - | 1 | no | 100 kHz | ±10 mV | - |
| [12] | 2 CCIIs, 3 MOS | - | - | no | 22 MHz | ±50 mV | - |
| [13] | 1 DXCCII, 3MOS | - | - | yes | 10 MHz | ±150 mV | 3.33 mW |
| [14] | 2 CCIIs | 4 | 2 | no | 10 kHz | 3 V | - |
| [15] | 1 CCIIs, 1 UVCs | 2 | - | no | 500 kHz | ±200 mA | 1.19 mW |
| [16] | 1 CCIIs, 1 UVCs | 2 | - | yes | 1 MHz | ±300 mV | - |
| [17] | 1 CDTAs | 4 | 1 | no | 10 MHz | ±1 mA | - |
| [20] | 1 CDTAs | 2 | 1 | no | Variable up to 42 MHz | ±5 mA | - |
| [21] | 1 DXCCIIs | 2 | 1 | no | 1 MHz | ±500 mV | - |
| [22] | 1 MZC-CDTA, 2 MOS | - | - | no | 10 MHz | ±300 mA | 14 mW |
| [27] | 3OA, 3 AD633/AD | 1 | 9 | no | 1 MHz | ±5 V | - |
| [28] | 3 CCCII | - | 5 | yes | 5 MHz | ±500 mV | - |
| [29] | 1 OTA/1 DVCC | 2 | 2/3 | no | 1 MHz | ±200 mA | - |
| [30] | 1 CDTA | 4 | - | yes | 1 GHz | ±210 µA | 6.31 mW |
| [31] | 1 CCII, 1 DXCCII | 2 | 2 | no | 1 MHz | ±350 mV | - |
| [32] | 47 MOS, 9 CS | - | 1 | no | 100 MHz | ±200 mV | 5.2 mW |
| [33] | 2 CCII | 2 | 3 | yes | 10 MHz | ±1 V | - |
| This work | 1 DOCCCIIs, ZCD, 2 MOS | - | 1 | no | 10 MHz | ±100 mV | 2.83 mW |

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# *Advanced gate control system for power MOSFET switching losses reduction with complete switching sequence control*

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**Abstract:** To meet strict EMC requirements for power electronics applications driving an inductive load, it is often necessary to mitigate current and voltage transition slopes. Using the conventional MOSFET control method, the slope mitigation is commonly performed by modifying a series gate resistance, which results in high switching losses, long turn-on and turn-off delays and long final gate charging and discharging durations affecting the overall application efficiency. In order to improve this, a novel MOSFET control method is developed and presented in this paper. It enables a complete control over all intervals of the switching sequences utilizing the gate current shaping principle. Switching losses, delays and final gate charging and discharging durations can be kept as low as possible, as the method allows to mitigate only the critical transition. The design of the system allows its implementation in a broad spectrum of applications regardless of the current or voltage rating and with a minimal impact on the application design. The paper presents the detailed description of the proposed system operation and its realization as an integrated circuit. The efficiency measurements of the conventional and the advanced gate control methods are reported as well, showing significant advantages of the proposed system.

**Keywords:** Power MOSFET switching behavior; advanced gate control; gate current shaping; switching losses reduction; EMC in power electronics

# *Napredno krmiljenje vrat močnostnih MOSFET tranzistorjev za zmanjševanje preklopnih izgub z nadzorom nad celotno preklopno sekvenco*

**Izvleček:** Za doseganje elektromagnetne skladnosti moramo v močnostni elektroniki pri napravah z induktivnim bremenom pogosto zmanjšati naklon toka ali napetosti med preklopi. Pri konvencionalni krmilni metodi to storimo s spreminjanjem serijske upornosti v vratih MOSFET tranzistorja. Slednje se odraža v povečanju preklopnih izgub, podaljševanju zakasnitev vklopa in izklopa ter podaljševanju trajanja končnega polnjenja in praznjenja vrat. Našteto zmanjšuje zmogljivost celotne naprave. Navedene pomanjkljivosti konvencionalne metode ublažimo z uporabo nove napredne krmilne metode, ki je predstavljena v tem članku. Deluje na principu spreminjanja toka, ki teče v vrata MOSFET tranzistorja ter omogoča nadzor nad dogajanjem v vsakem intervalu preklopne sekvence. Ker lahko na tak način omilimo le kritični naklon, sistem omogoča vzdrževanje minimalnih preklopnih izgub, zakasnitev in trajanj končnega polnjenja in praznjenja vrat. Sistem je zasnovan tako, da ga lahko vgradimo v širok spekter naprav, ne glede na napetostno ali tokovno zmogljivost in z minimalnim poseganjem v zasnovo same naprave. V članku je detajlno opisano delovanje predstavljenega sistema ter njegova realizacija v obliki integriranega vezja. Predstavljene so tudi meritve učinkovitosti konvencionalne in napredne kontrole vrat. Rezultati so občutno boljši v primeru uporabe predstavljenega sistema.

**Ključne besede:** Preklopi močnostnega MOSFET tranzistorja; napredno krmiljenje vrat; oblikovanje toka v vrata tranzistorja; zmanjševanje preklopnih izgub; EMC v močnostni elektroniki

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## 1 Introduction

The tradeoff between switching losses and electromagnetic emissions is often of great concern during the design of power electronic applications with an inductive load. Fast transitions of voltage and current at power switch (in this paper we are focusing on power MOSFETs) cause excessive emissions and oscillations, while slow transitions cause significant switching losses. To meet strict EMC requirements, slopes must often be limited, which is obviously done at the expense of increased switching losses.

Power MOSFETs are commonly driven via series gate resistor ($R_g$). Transition slopes are adjusted by changing $R_g$ value but such approach is not the most effective. The problem is that changing $R_g$ resistance influences all intervals of the switching sequence instead of mitigating only the critical transition that is responsible for emissions. This produces excessive switching losses, introduces long turn-on and turn-off delays and extends final gate charging and discharging durations. To improve this process, a different gate control method should be used to allow control over transition in each interval of the switching sequence independently.

Several papers [1–10] report improvements of the conventional control method with a gate resistor or propose entirely new control approaches that differ in functionality, complexity, efficiency and cost.

For example, the methods presented in [1], [2], [4], [7] focus only on the mitigation of turn-off voltage overshoot and the following oscillations, which are often an issue especially among IGBT circuits. Papers [5], [8] introduce the combined control over turn-off voltage and turn-on current transition. The latter is usually of great concern, as the current slope impacts reverse recovery severity, it may induce oscillation and it strongly impacts the emissions rate. The method [9] focuses on the acceleration of turn-on voltage fall and minimization of the turn-off delay. The most comprehensive approaches are reported by Rose [3], Park [6] and Lobsiger [10] demonstrating current and voltage transition control during the turn-on and the turn-off. None of the presented methods, however, addressed control over the whole duration of the switching sequence.

The presented control methods are based on significantly different principles for the operating point detection of the controlled MOSFET (or IGBT), which is an essential part of any advanced control method. Certain methods [2], [6], [7], [10] use capacitor or special differentiator circuit connected to the transistor drain (or collector) terminal. Despite being simple and low-cost, such approach may be susceptible to noise [4] and oscillations that potentially mask the actual voltage transition resulting in an inappropriate control procedure. On the other hand, methods [3], [4], [6], [10] exploit intrinsic inductances from the physical circuit to detect the current transitions. Such system may be found difficult to implement, taking into account diverse layout topologies, current slopes and ratings.

Gate control approach as presented in this paper aims to enable control over transitions in all intervals of the switching sequences and to use such operating point detection principle that allows system implementation in various applications regardless of voltage or current ratings and with a minimal impact on the circuit layout design.

Presented system is also a subject of PCT patent application.

Paper is organized in the following order: section 2 presents the inductive load switching sequence, switching losses and EMC overview and provides an explanation about the conventional gate control drawbacks; section 3 describes the concept of the proposed gate control system; section 4 presents system realization as an integrated circuit; section 5 presents system measurements, results and discussion, while section 6 concludes the paper.

## 2 Switching sequences, switching losses and EMC

A short insight into a well known switching behaviour of a MOSFET with a clamped inductive load is given first in order to present switching losses and electromagnetic emission (EM) generation and to underline the importance of the advanced gate control introduction.

A clamped inductive load circuit, presented in Figure 1, is comprised of MOSFET $M_1$, inductive load ($L_{load}$), freewheeling diode ($D_{fwd}$, which is the intrinsic diode of permanently closed MOSFET $M_2$), driving circuit ($V_{gg}$ and $R_g$), MOSFET $M_1$ intrinsic capacitances ($C_{gs}$ and $C_{gd}$) and supply voltage source $V_{bat}$. The corresponding switching waveforms of $M_1$ turn-on and turn-off sequences are shown in Figure 2 [11]. Just before the $t_0$, the initial conditions in the circuit are as follows: $v_{gg}$=0 and $v_{gs}$=0, so $M_1$ is switched-off ($i_d$=0); due to previous excitations, inductor $L_{load}$ drives current $I_0$ through $D_{fwd}$ ($i_{fwd}$=$I_0$), and since $D_{fwd}$ is forward-biased, $v_{ds}$ equals $V_{bat}$.

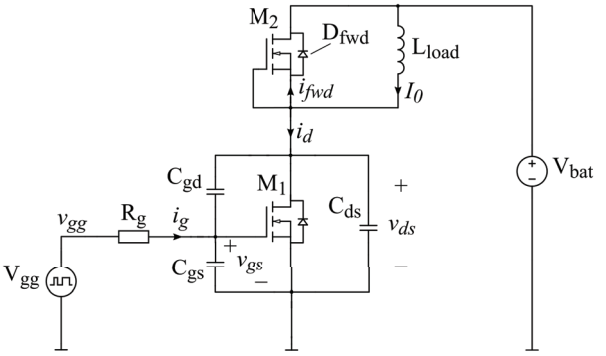


**Figure 1:** Clamped inductive load circuit

The turn-on sequence starts with the interval $T_1$ (turn-on delay) at $t=t_0$, when $V_{gg}$ turns-on ($v_{gg}=V_{gg}$) and starts charging $C_{gs}$ (Figure 2a). As $v_{gs}$ reaches the threshold voltage $V_{th}$ at the beginning of the interval $T_2$, $M_1$ starts conducting (Figure 2b) and taking over the load current $I_0$ from $D_{fwd}$. When $i_d$ rises to $I_0$, $i_{fwd}$ falls to zero, so $D_{fwd}$ can be reverse-biased; the reverse-recovery process takes effect manifesting as $M_1$ drain current overshoot. During the whole interval $T_2$, the forwardly biased $D_{fwd}$ clamps $v_{ds}$ to $V_{bat}$ level. In the interval $T_3$, $v_{ds}$ drops as $C_{gd}$ is discharged (Figure 2c). The total current from $V_{gg}$ is now diverted to $C_{gd}$, causing $v_{gs}$ to remain constant at the Miller plateau ($V_\mu$). After $v_{ds}$ drops to $V_{ds,on}$ (a consequence of M1 channel resistance), $C_{gs}$ starts charging again and $v_{gs}$ is rising again towards $V_{gg}$ in $T_4$. The turn-on is thus accomplished [11] [12].

The turn-off occurs in a similar manner. It begins with $V_{gg}$ going low at $t=t_0'$, followed by a turn-off delay interval $T_4'$, in which $v_{gs}$ falls to Miller plateau, as $C_{gs}$ is discharged (Figure 2e). Beyond $v_{gs}=V_\mu$, further $C_{gs}$ discharging requires drain current reduction, which is impossible at that moment, since $D_{fwd}$ is reverse biased ($V_{bat}>v_{ds}$) and cannot take over load current ($I_0$) yet. Therefore, $v_{ds}$ rises first in $T_3'$ (Figure 2g). When $v_{ds}$ meets $V_{bat}$, $I_0$ can eventually be diverted to $D_{fwd}$, so $M_1$ drain current ($i_d$) falls in $T_2'$ (Figure 2f). At $v_{gs}=V_{th}$, $M_1$ closes ($i_d=0$, $i_{fwd}=I_0$) and only $v_{gs}$ remains to drop to zero in $T_1'$, thus terminating turn-off sequence [11].

The review of the switching sequences shows that the current ($i_d$) transitions in $T_2$ and $T_2'$ occur at the full voltage ($v_{ds}$) on $M_1$. Similarly, voltage ($v_{ds}$) transitions in $T_3$ and $T_3'$ occur at the maximum drain current. This results in high power dissipation, $p_{sw}=i_d \cdot v_{ds}$. The integrals of $p_{sw}$ over $T_2$ and $T_3$ for turn-on (1) and over $T_2'$ and $T_3'$ for turn-off (2) determine the turn-on ($E_{sw,on}$) and turn-off ($E_{sw,off}$) switching losses (Figure 2d and h) [11] [12].

$$E_{sw,on} = \int_{T2,T3} p_{sw}(t)\,\mathrm{dt} = \frac{1}{2} I_0 V_{bat} (T_2 + T_3) \qquad (1)$$

$$E_{sw,off} = \int_{T2',T3'} p_{sw}(t)\,\mathrm{dt} = \frac{1}{2} I_0 V_{bat} (T_2' + T_3') \qquad (2)$$

The dissipated energy, manifested as heat, is the root cause of several engineering challenges. Most importantly, it is necessary to provide adequate heat sinking, which often results in a bulky and expensive design and presents a limit for the application implementation. Moreover, elevated application temperature results in increased degradation rate of assembly components and impact general system reliability. As switching losses may present an important source of heating, their minimization is of great concern [13].

It is also well established that current and voltage transitions in $T_2$, $T_2'$ and $T_3$, $T_3'$ are the main source of electromagnetic emissions in power applications. High *di/dt* and *dv/dt* rates in conjunction with inductive and capacitive coupling cause conducted (and indirectly also radiated) differential (DM) and common mode (CM) emissions. Moreover, *di/dt* and *dv/dt* could excite oscillations and overshoots in resonant circuits (formed by parasitic inductances and capacitances), producing additional emissions and affecting the system reliability. There are several mechanisms available to mitigate emissions and oscillations (to meet EMC standards), each with its own trade-offs. One possibility is obviously to decrease *di/dt* and *dv/dt* rates (i.e. extend intervals $T_2$, $T_3$, $T_2'$ and $T_3'$) and eliminate the emissions origin, but at the expense of additional switching losses. We can furthermore tweak layout or insert additional components, such as snubber circuits or blocking capacitors, which usually involves a lot of prototyping and has only limited effect. Another possibility is the implementation of CM and DM filters, which is an effective but bulky and expensive solution. Most designs require to utilize all of the above, each in the scope of its own trade-offs and affected application characteristics [13][14]. On the other hand, any improvement of the described mechanisms eases the application design and boosts its efficiency.

This paper presents one of such improvements, which deals with the MOSFET control circuit and increases slope adaptation mechanism efficiency. The main drawback of the conventional method employing a series gate resistor $R_g$ is that increasing the gate circuit resistance in order to reduce critical current or voltage slopes prolongs all intervals in corresponding switching sequence. First, it causes excessive switching losses in $T_2$, $T_2'$, $T_3$ or $T_3'$, as it extends both current and voltage transitions. Moreover, an extension of $T_1$ and $T_4'$ has a negative impact on applicability of some control algorithms, as it requires longer dead-times and in turn also produces higher diode $D_{fwd}$ losses [12]. Extension of $T_4$ or $T_1'$ affects the system reliability in terms of the unintentional turn-on / turn-off immunity.

Introduction of the advanced gate control system presented in this paper, which allows setting the duration of each interval of the switching sequence separately, extends the margins where slope adaptation effectively improves the application efficiency.

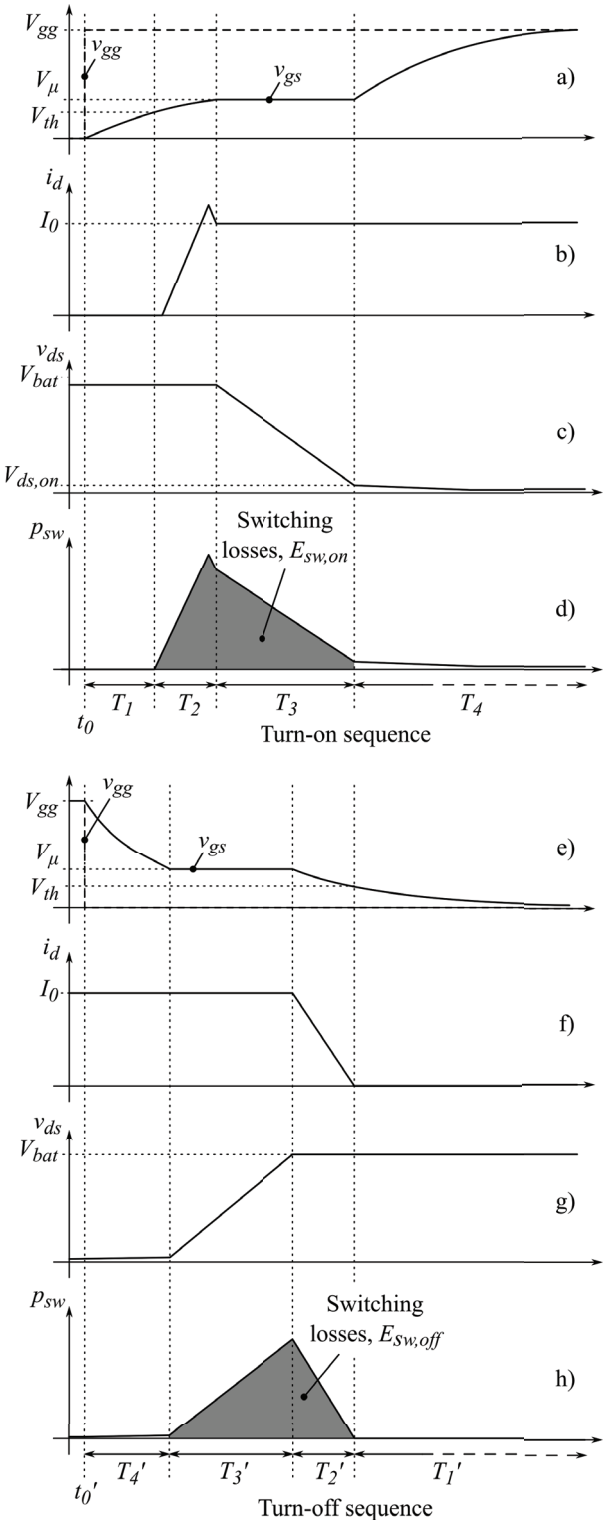


**Figure 2:** Switching sequence waveforms

## 3 Advanced gate control system

Figure 3 depicts the block diagram of the advanced gate control system presented in this paper. The system is constructed of two main units, namely the current sources unit and the control circuit unit. The role of the first is to feed the power MOSFET gate, while the second unit monitors the power MOSFET operating point, detects the ongoing switching sequence interval and produces control signals for the current sources unit. Each unit operation is explained in detail in the following sections.

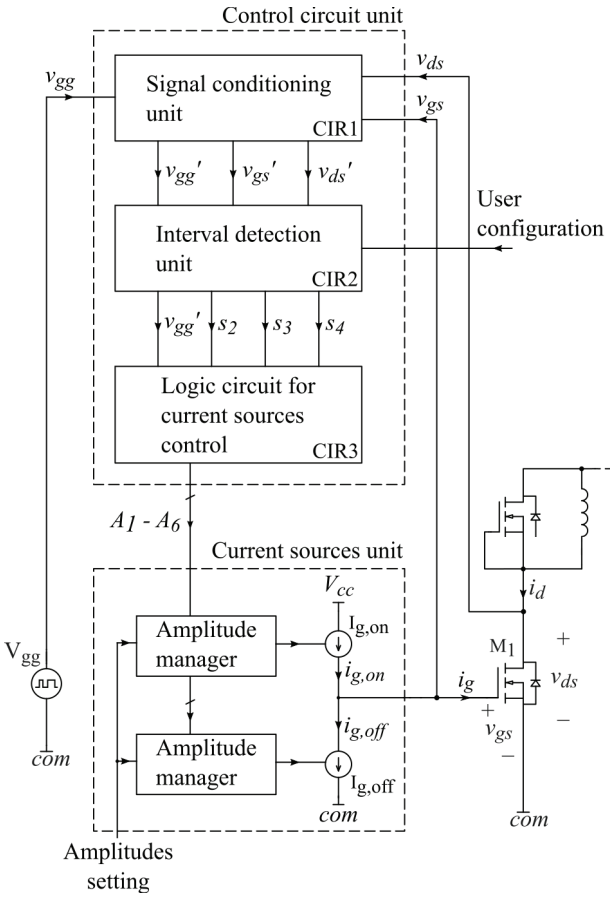


**Figure 3:** Advanced gate control system block diagram

### 3.1 Current sources unit

The advanced gate control system (Figure 3) is based on the power transistor gate current shaping ($i_g$) principle, implemented using two controlled current sources ($I_{g,on}$ and $I_{g,off}$) that charge and discharge the transistor input capacitance during its turn-on and turn-off. Each source amplitude can be individually set in each interval of the switching sequences.

By adjusting the gate current ($i_g$) in each interval, the charge flow rate to the gate is governed and hence the rate of change of each interval transition can be indi-

vidually controlled. We can therefore adjust each current and voltage slope (*di/dt* and *dv/dt*) in intervals $T_2$, $T_3$, $T_2'$ and $T_3'$ and also minimize turn-on and turn-off delays in $T_1$ and $T_4'$ and the duration of the final gate charging and discharging in the intervals $T_4$ and $T_1'$. An example of the advanced gate control operation is shown in Figure 4.

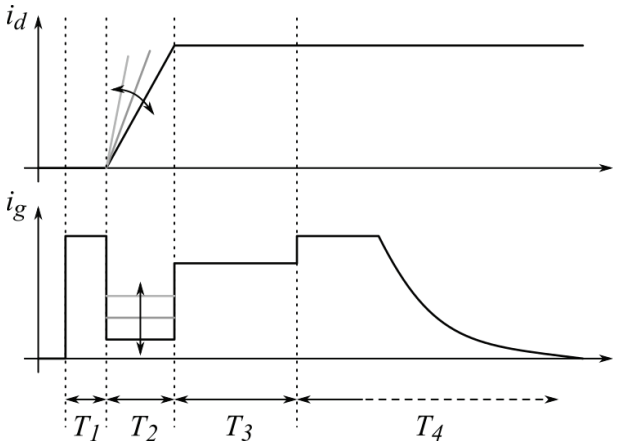


**Figure 4:** By shaping gate current ig drain current slope is being controlled

The presented gate control approach can improve the conventional gate control drawback where all interval transitions are influenced simultaneously with $R_g$ adaptation. Determining the optimal point of the trade-off between switching losses and electromagnetic emissions is thus much more effective. In most situations, less switching losses are produced for the same rate of electromagnetic emissions. Delays and final gate charging and discharging durations can also be minimized.

The $i_g$ amplitude adjustment throughout the switching intervals is performed by the amplitude manager system. It enables the user to set the desired interval amplitude levels and control the $I_{g,on}$ and $I_{g,off}$ current sources. The operation of the amplitude manager is based on the information about the ongoing interval, which is obtained from the control circuit unit. Amplitude managers and current sources are implemented as current mirrors, described in detail in section 4.

The current sources are supplied with voltages ($V_{cc}$) equal to gate-source voltage ($v_{gs}$) required for power transistor full turn-on (typically 12V for common power MOSFETs).

### *3.2 Control circuit unit*

The role of the control circuit unit is to detect borders between the intervals of the switching sequence and to subsequently send information about the ongoing interval to the current sources block. It consists of three subunits, namely the signal conditioning unit (CIR1), interval detection unit (CIR2) and logic circuit for the current sources control (CIR3).

#### 3.2.1 Signal detection and Signal conditioning unit

The signal conditioning unit (CIR1) accepts signals $v_{ds}$ and $v_{gs}$ from the MOSFET and the control signal $v_{gg}$ (usually from a microcontroller). To understand why it is necessary to monitor $v_{ds}$ and $v_{gs}$, we must first take a look at the interval detection principle. The interval borders are associated with specific events, marked with points $N_0$, $N_2$, $N_3$ and $N_4$ for turn-on and $F_0$, $F_4$, $F_3$ and $F_2$ for turn-off in Figure 5 and explained in Table 1. As evident from Figure 5, the points are located on $v_{ds}$, $v_{gs}$ and $v_{gg}$, which means that these signals provide full information about the ongoing interval. It should be emphasized that the points are located exclusively on the voltage signals that are commonly present in each inductive load circuit. This is an important advantage of the presented system, as it enables an implementation in various power applications regardless of voltage or current rating.

**Table 1:** Interval border points explanation

| Point | Start of interval | Associated event |
|---|---|---|
| $N_0$ | $T_1$ | Start of TURN-ON sequence, vgg starts rising |
| $N_2$ | $T_2$ | vgs reaches threshold voltage Vth |
| $N_3$ | $T_3$ | vds starts falling |
| $N_4$ | $T_4$ | vds drops to the final value |
| Power transistor is ON | | |
| $F_0$ | $T_4'$ | Start of TURN-OFF sequence, vgg starts dropping |
| $F_4$ | $T_3'$ | vds starts rising |
| $F_3$ | $T_2'$ | vds rises to the final value |
| $F_2$ | $T_1'$ | vgs drops to the threshold voltage |
| Power transistor is OFF | | |

Before point sensing and interval detection, the input signals $v_{ds}$ and $v_{gs}$ are processed by the signal conditioning unit (Figure 6). Signals must be filtered first to eliminate high-frequency oscillations that commonly occur during the power transistor switching. The filters must be carefully designed to keep their time constant small compared to the switching sequence interval durations. The control signal $v_{gg}$, which is a logic signal, must be voltage-matched to meet the comparator input requirements.

#### 3.2.2 Interval detection unit

After filtering, the signals are passed to the interval detection unit (CIR2) that outputs the signals $s_2$, $s_3$ and $s_4$

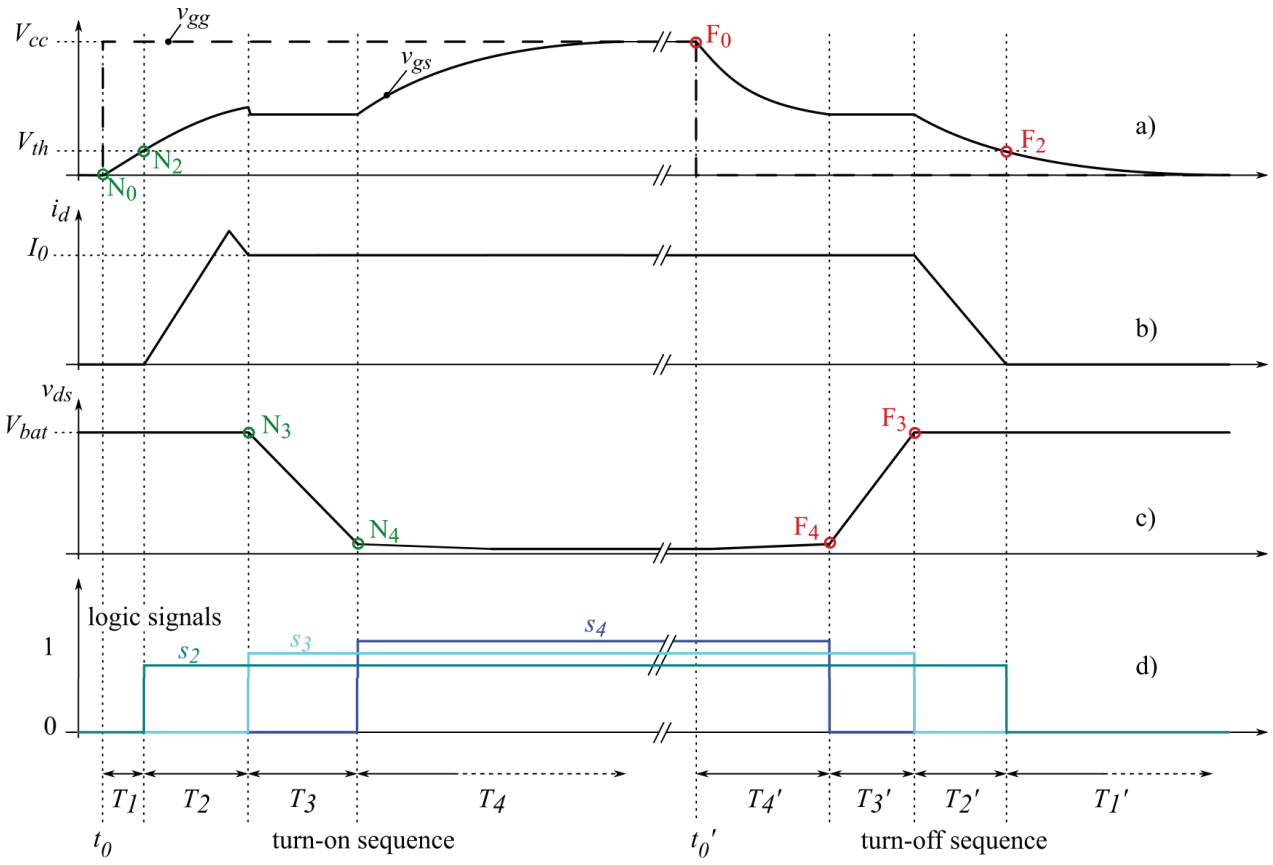


**Figure 5:** Switching sequence with N and F points

(Figure 5 d), which provide full information about the ongoing interval (by forming a unique combination in each interval) in conjunction with $v_{gg}$. Each of the three signals is set high and then low at two points: $s_2$ at $N_2$ and $F_2$, $s_3$ at $N_3$ and $F_3$, and $s_4$ at $N_4$ and $F_4$ respectively (Figure 5). Since each point pair detection and corresponding output signal generation follows the same principle and utilizes an identical circuit (depicted in Figure 7), a common explanation is applicable hereafter, where the input signal stands for $v_{gs}'$ and $v_{ds}'$ and the output signal for $s_2$, $s_3$ and $s_4$. For $s_2$, the input signal is $v_{gs}'$, while for $s_3$ and $s_4$ generation, the input signal is $v_{ds}'$. Since $v_{gg}'$ is a logic signal, the detection of points $N_0$ an $F_0$ does not require utilizing the circuit from Figure 7. The $v_{gg}'$ transition detection is carried out in the logic circuit for current sources control unit (CIR3).

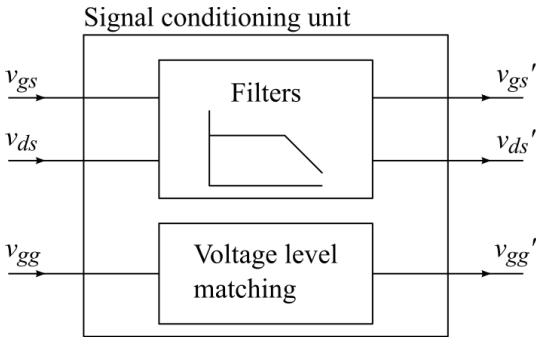


**Figure 6:** Signal conditioning unit (CIR1)

As evident from Figure 7, the input signal $v_{gs}'$ or $v_{ds}'$ crossing a certain level at points $N_i$ or $F_i$ is sensed by the comparator ($U_1$ and $U_2$). The point levels are user-configured by adapting the input voltage dividers ($R_1$-$R_2$) and ($R_3$-$R_4$). In case that a voltage signal at a compara-

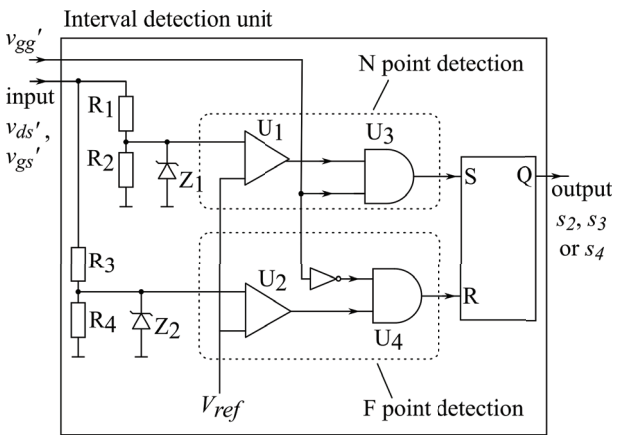


**Figure 7:** Interval detection unit (CIR2) – one out of three identical circuits is depicted.

tor input exceeds its rating, the Zener diodes $Z_1$ and $Z_2$ start clamping to protect the comparator inputs. To ensure that $N_i$ and $F_i$ points are detected exclusively during turn-on and turn-off sequences and to prevent flip-flop mistriggering, the AND gates $U_3$ and $U_4$ with applied $v_{gg}'$ and $\overline{v_{gg}}'$ inputs are inserted to generate a sequence-matching window for passing comparator output signal. When a point crossing is detected, a SR flip-flop input is triggered: *S* input at $N_i$ and *R* input at $F_i$ point detection, which generates a *Q* signal that matches the desired output signal waveforms $s_2$, $s_3$ or $s_4$, Figure 5.

Using flip-flops for the interval detection is also important to ensure the immunity to oscillations, as SR flip-flops react only on the first input triggering. Therefore, comparator input signal oscillation around $V_{ref}$ (which results in comparator output alternating) has no effect on the $s_2$, $s_3$ or $s_4$ waveforms.

**3.2.3 Logic circuit for current sources control**

The signals $s_2$, $s_3$ and $s_4$ are passed to the logic circuit CIR3 (Figure 3) that together with the signal $v_{gg}'$ produces the controlling signals $A_1$ to $A_6$ for the current sources unit. The operation of this unit follows the selected current sources control scheme, which is described in detail in the next section.

# 4 System implementation

The system is implemented as an IC in a 250 nm TSMC technology (Figure 10). The circuit integration is essential for an efficient system embodiment. First, it enables short propagation delay of the controlling circuit, which is crucial to be small in comparison to the interval durations allowing the management of switching transients. To make our system implementable in applications with expected switching transient durations of 100ns, it is considered that signal propagation delay must not exceed 10 ns, which is likely unachievable using discrete components. Furthermore, the integration allows an efficient realization of current sources and amplitude managers in the form of integrated current mirrors. An important integration benefit is also minimization of the system physical dimensions.

The purpose of the system implementation presented in this work is to prove the concept of the described system. In order to simplify the system development and future research, only the crucial parts are integrated. According to Figure 3, these are the current sources unit with the exception of resistors the $R_{ref1}$ to $R_{ref6}$ (Figure 8), logic circuitry for controlling current sources and the interval border detection unit with the exception of input voltage dividers ($R_1$, $R_2$ and $R_3$, $R_4$ in Figure 7). The system is supplied with two voltage levels, 5 V for the controlling circuit and 12 V ($V_{cc}$) for the current sources unit.

## 4.1 Current sources unit realization

Figure 8 presents a realization of the current sources unit with integrated current mirrors. The transistors $M_{h0}$ and $M_{l0}$ present a physical implementation of the current sources $I_{g,on}$ an $I_{g,off}$ (from Figure 3), while the rest of the circuit embodies the corresponding amplitude managers. The unit is divided into a high-side and low-side subcircuit, each consisting of three channels (two of them depicted dimmed) that enable setting different $i_{g,on}$ and $i_{g,off}$ amplitude levels and shape the gate current ($i_g$) during switching sequence intervals.

The amplitude levels are user-defined by adjusting the $R_{ref1}$ to $R_{ref6}$ resistor values (not part of IC) that determine current mirror reference currents for each channel ($i_{r1}$, $i_{r2}$, $i_{r3}$ and $i_{r4}$, $i_{r5}$, $i_{r6}$). The reference currents are mirrored to $i_{h2}$, $i_{h2}'$, $i_{h2}''$ and $i_{l2}$, $i_{l2}'$, $i_{l2}''$. A single mirror is required for the high side subcircuit, while the low side requires two mirroring stages for the $I_{g,on}$ and $I_{g,off}$ source and sink realization. The mirrored currents are then combined into $i_{h1}$ and $i_{l1}$ ($i_{h1}=i_{h2}+i_{h2}'+i_{h2}''$ and $i_{l1}=i_{l2}+i_{l2}'+i_{l2}''$) that present the reference currents for the $M_{h1}$-$M_{h0}$ and $M_{l1}$-$M_{l0}$ current mirrors and in turn determine the $i_{g,on}$ and $i_{g,off}$ waveforms. Each output current therefore consists of three components and can be defined as (3) and (4), where *M* indicates the total current mirror multiplication factor. In this design, *M* equals 1000.

$$i_{g,on}(t) = M \cdot i_{r1}(t) + M \cdot i_{r2}(t) + M \cdot i_{r3}(t) \quad (3)$$

$$i_{g,off}(t) = M \cdot i_{r4}(t) + M \cdot i_{r5}(t) + M \cdot i_{r6}(t) \quad (4)$$

To set the $i_g$ amplitude in each interval separately, the transistors $M_{h3}$, $M_{h3}'$, $M_{h3}'$ and $M_{l3}$, $M_{l3}'$, $M_{l3}''$ are utilized, controlled by the $A_1$ to $A_6$ signals from the logic circuit for current sources control CIR3 (Figure 3). The transistors act as switches and take over the reference currents $i_{r1}$ to $i_{r6}$ from $M_{h2}$, $M_{h2}'$, $M_{h2}''$ and $M_{l2}$, $M_{l2}'$, $M_{l2}''$. This causes zero current mirroring in the corresponding channels and consequently zero $i_{h2}$, $i_{h2}'$, $i_{h2}''$, $i_{l2}$, $i_{l2}'$ or $i_{l2}''$ contribution in the formation of the $i_{h1}$ and $i_{l1}$ currents, which, as presented, impact the $i_{g,on}$ and $i_{g,off}$ amplitudes.

To put it briefly, the gate current $i_g$ shaping is embodied by the switching signals $A_1$ to $A_6$ throughout intervals which define the appropriate current components from the expressions (3) and (4) to form the $i_{g,on}$ and $i_{g,off}$ currents at a given time. The $i_{g,on}$ and $i_{g,off}$ amplitude levels are set by adjusting the reference currents by the external $R_{ref1}$ to $R_{ref6}$ resistors.

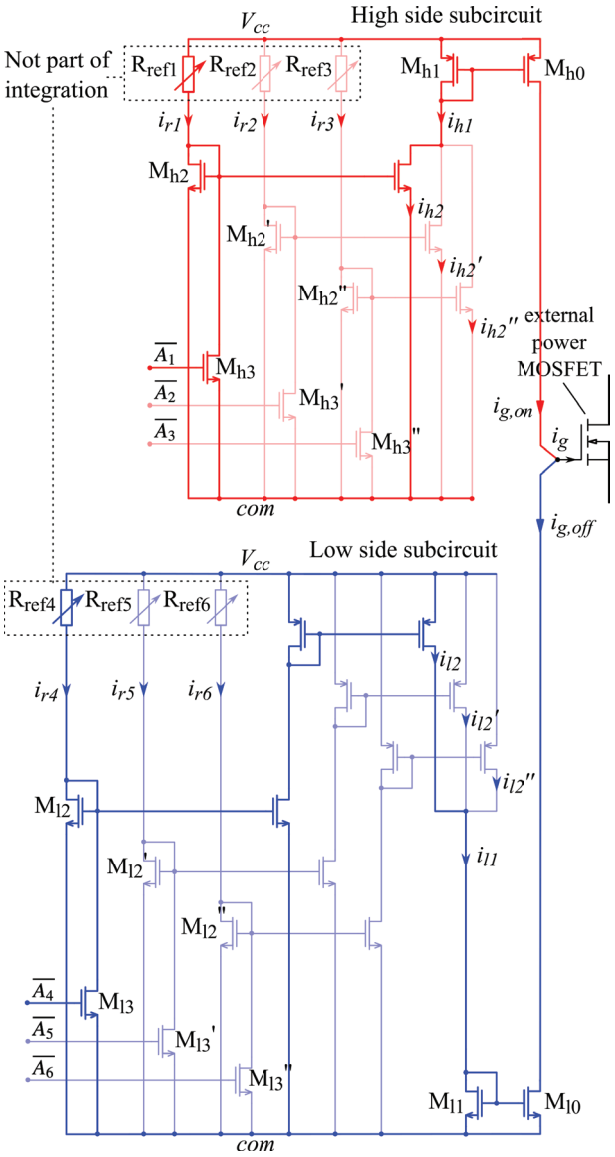


**Figure 8:** Schematic of current sources unit and corresponding amplitude managers (High side subcircuit for $I_{g,on}$ and Low side subcircuit for $I_{g,off}$)

### *4.2 Current sources controlling scheme*

In each interval, a particular $A_1$ to $A_6$ signal combination is provided by logic circuit for current sources control (CIR3) to ensure fast and smooth current shaping. The resulting $i_{g,on}$ and $i_{g,off}$ current composition of multiplied reference currents ($M{\cdot}i_{r1}$ to $M{\cdot}i_{r6}$) is presented in Figure 9.

As evident, the $i_{g,on}$ and $i_{g,off}$ components $M{\cdot}i_{r2}$ and $M{\cdot}i_{r6}$ are present during the whole turn-on and turn-off sequences. Regarding the turn-on, in the intervals $T_1$ and $T_4$ $M{\cdot}i_{r1}$ is added to $M{\cdot}i_{r2}$ to minimize the delay and final gate charging duration. During $T_2$, only $M{\cdot}i_{r2}$ is available – the power transistor current slope is usually the one requiring the strongest mitigation and therefore requires the lowest gate current. The voltage slope in $T_3$ is managed by $M{\cdot}i_{r2}$ and $M{\cdot}i_{r3}$.

A similar operation refers to the turn-off: $M{\cdot}i_{r6}$ and $M{\cdot}i_{r4}$ in $T_4'$ minimize the turn-off delay, and $M{\cdot}i_{r6}$ and $M{\cdot}i_{r5}$ determine the voltage slope in $T_3'$. Only $M{\cdot}i_{r6}$ component is present during the current transition in $T_2'$. Since the duration of the input capacitances discharging in $T_1'$ is already limited by the low power transistor $v_{gs}$ voltage and intrinsic resistances, only the $M{\cdot}i_{r6}$ component is provided.

During the turn-on sequence, $i_{g,off}$ equals zero, and similarly, $i_{g,on}$ equals zero during the turn-off.

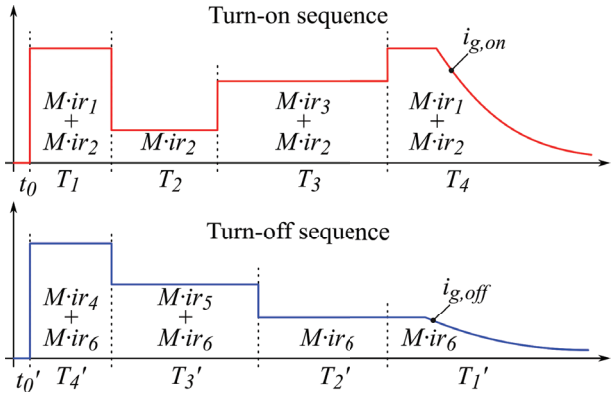


**Figure 9:** composition of $i_{g,on}$ and $i_{g,off}$ currents

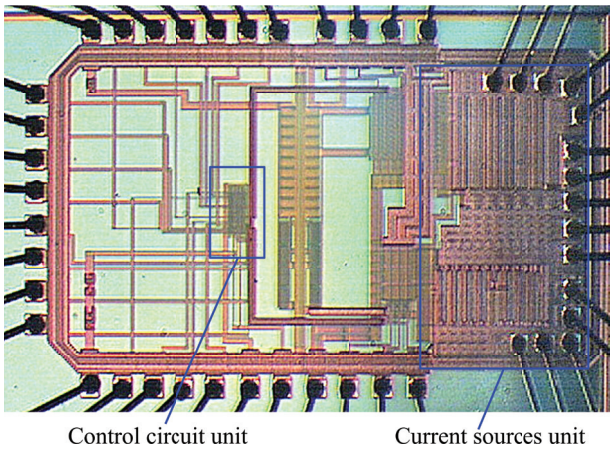


**Figure 10:** A microphotograph of the advanced gate control ASIC. IC dimensions approx. 1502 um x 2430 um

## *5 Testing, results and discussion*

### *5.1 Test setup*

To investigate the efficiency, the advanced gate control system is compared to the conventional control method with the series gate resistance. The test is carried out using a common inductive load circuit, as depicted

in Figure 11 (the circuit basic operation is already described in Section 1). Between the gate and the source terminals of MOSFET $M_1$, a 10 kΩ resistor and a 10 nF capacitor are inserted to emulate realistic conditions. The two components are often inserted in power circuits to improve immunity against unintentional turn-on and to mitigate the Miller effect consequences. MOSFET $M_1$ can be driven with the advanced or conventional control method, while the drain-source voltage ($v_{ds}$), the gate-source voltage ($v_{gs}$) and the drain current ($i_d$) are monitored with the oscilloscope. To measure the $i_d$ current, a Rogowski coil is utilized. The MOSFETs $M_1$ and $M_2$ are both Infineon IPB010N06N.

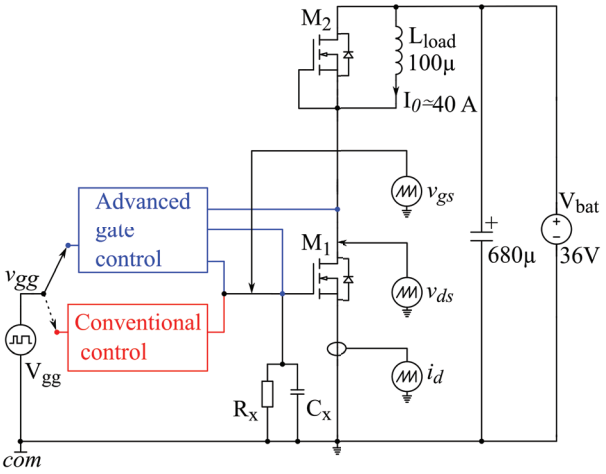


**Figure 11:** The test circuit schematics

The waveform generator $V_{gg}$ (Agilent 33500B) is programed to produce a pulse shown in Figure 12. During the interval $T_{charge}$, $M_1$ is open. In this interval, the current through $L_{load}$ rises up to the desired value $I_0$, in this case 40 A. After that, $M_1$ is switched off and $i_d$ is diverted into $M_2$'s diode, which produces the required initial conditions to observe the turn-on and turn-off switching sequences at the following $v_{gg}$ fronts. The time between the last three changes of $v_{gg}$ is kept low (20 us) to produce only minimal change in $i_d$.

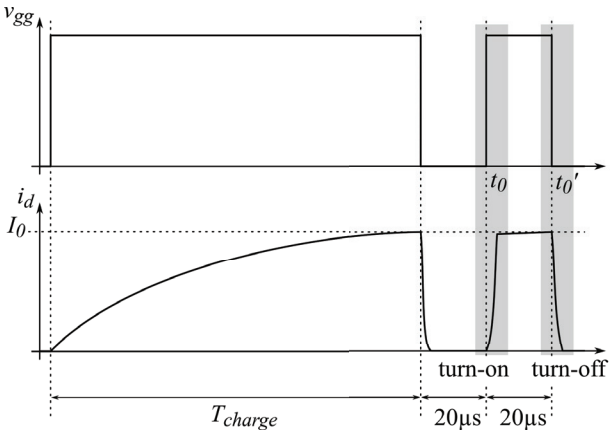


**Figure 12:** $v_{gg}$ and corresponding $i_d$ waveforms

The advanced gate control from Figure 11 as such is described in previous sections. In the signal conditioning unit, first order low-pass filters are employed comprising of 10 kΩ resistor and 1 pF MLCC capacitor. Resistors $R_{ref1}$ to $R_{ref6}$ are trimmer potentiometers with 2 MΩ track resistance. The conventional control is composed of a special driver (IR AUIRS2191S) and the series gate resistor $R_g$.

The efficiency of the two methods is observed by comparing turn-on and turn-off switching losses, delays, and final charging / discharging durations at different values of the drain current rise or fall time. This figure of merit is chosen, as the current transitions are considered the most critical, since they are usually faster than voltage transitions and their mitigation produces greatest amount of surplus switching losses. Moreover, the comparison of current rise and fall times are more accurate, since the current transitions are not affected by parasitic elements in such extent as the voltage transitions.

Definitions of the observed parameters are shown in the Table 2.

**Table 2:** Parameters definitions

| Parameter | Definition |
|---|---|
| Current rise time ($t_{id,rise}$) | $i_d$=10% $I_0$ to $i_d$=90% $I_0$ |
| Current fall time ($i_{d,fall}$) | $i_d$=90% $I_0$ to $i_d$=10% $I_0$ |
| Voltage rise time ($v_{ds,rise}$) | $v_{ds}$=10% $V_{bat}$ to $v_{ds}$=90% $V_{bat}$ |
| Voltage fall time ($v_{ds,fall}$) | $v_{ds}$=90% $V_{bat}$ to $v_{ds}$=10% $V_{bat}$ |
| Turn-on delay | $v_{gs}$=10% $V_{cc}$ to $i_d$=10% $I_0$ |
| Turn-off delay | $v_{gs}$=90% $V_{cc}$ to $v_{ds}$=10% $V_{bat}$ |
| Turn-on final charging | $v_{ds}$=10% $V_{bat}$ to $v_{gs}$=90% $V_{cc}$ |
| Turn-off final discharging | $i_d$=10% $I_0$ to $v_{gs}$=10% $V_{cc}$ |
| Turn-on switching losses ($E_{sw,on}$) | $E_{sw,on} = \int_{t_1}^{t_2} i_d v_{ds} dt$<br>$t_1$ when $i_d$=10% $I_0$<br>$t_2$ when $v_{ds}$=10% $V_{bat}$ |
| Turn-off switching losses ($E_{sw,off}$) | $E_{sw,on} = \int_{t_1}^{t_2} i_d v_{ds} dt$<br>$t_1$ when $v_{ds}$=10% $V_{bat}$<br>$t_2$ when $i_d$=10% $I_0$ |

### *5.2 Measurements and results*

Figure 13 first shows an example of the advanced gate control operation. The graphs present three turn-on switching sequence waveforms ($i_d$, $v_{ds}$ and $v_{gs}$). Each time a different setting for $i_{ref3}$ is applied (by adjusting $R_{ref3}$ trimmer resistor) in order to manipulate $v_{ds}$ fall time. Specifically, the $i_{ref3}$ current is set to 1.7 mA, 706 µA and 63 µA, while the currents $i_{ref1}$ and $i_{ref2}$ are constant in all three cases and set to 370 µA and 39 µA respectively. It should be noted that the voltage drop that occurs during the current transition (while $M{\cdot}i_{r2}$ is active) is a consequence of the voltage induction on parasitic inductances due to the relatively high *di/dt* rate being present and cannot be manipulated with the advanced gate control system. However, the last part of $v_{ds}$ drop that can be influenced clearly underlines the system key advantage. While keeping the drain current rise time constant (at around 200 ns), the voltage drop rate could be boosted (in regards to the emission generation) thus reducing switching losses.

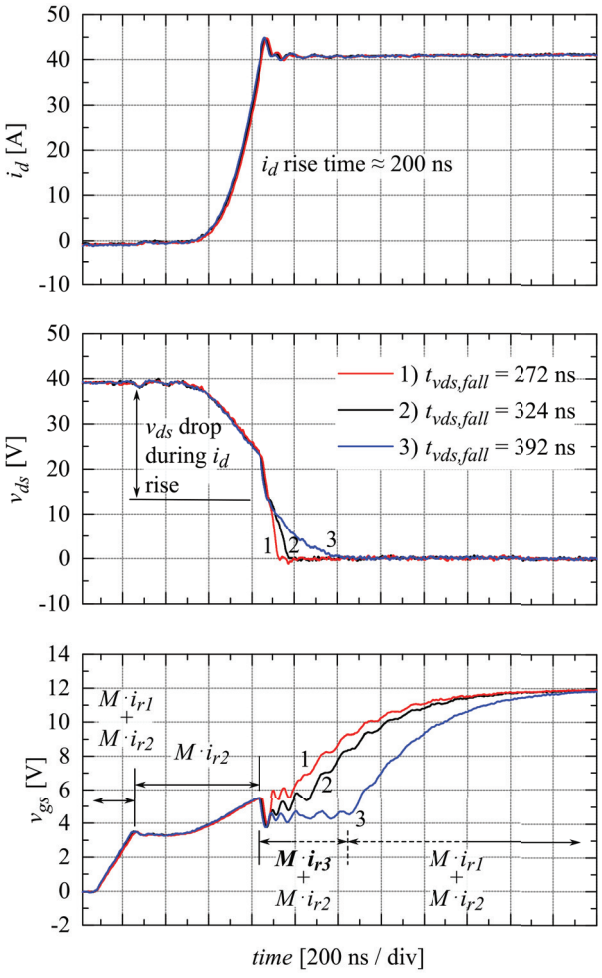


**Figure 13:** Advanced gate control operation, turn-on sequence oscillograms. Different $t_{vds,fall}$ are applied at the same $t_{id,rise}$.

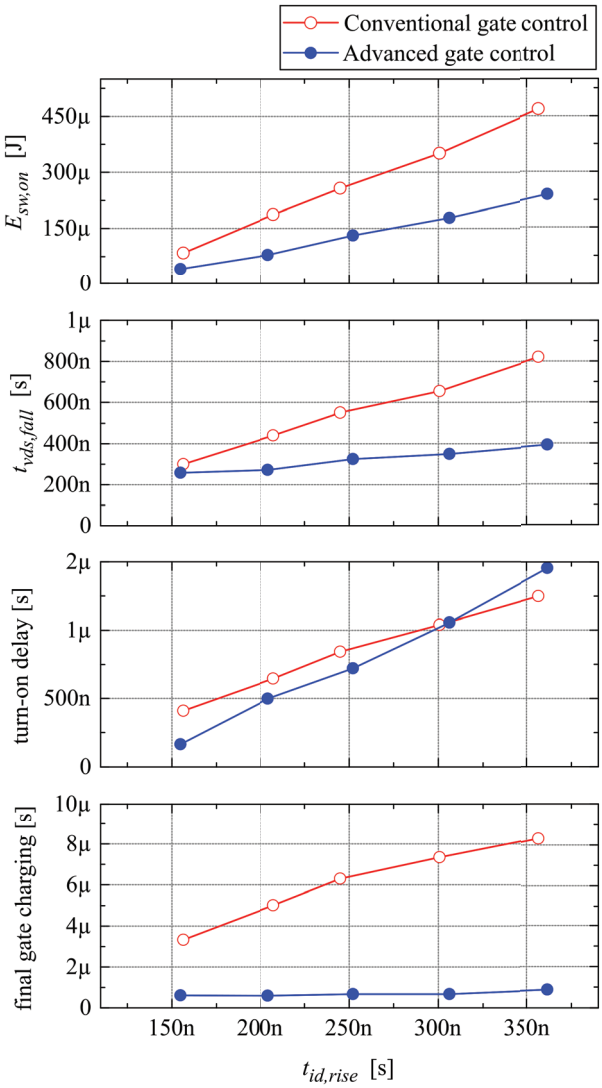


**Figure 14:** Comparison of the conventional and the advanced gate control methods, turn-on

To compare the two methods, the efficiency measurements are performed first with the conventional gate driving method using different gate resistor $R_g$ values. For the turn-on, 39 Ω, 68 Ω, 90 Ω, 120 Ω and 150 Ω are used, which results in the following $i_d$ rise times: 156 ns, 208 ns, 245 ns, 300 ns and 357 ns respectively. Similarly, for the turn-off, 47 Ω, 82 Ω, 100 Ω, 120 Ω and 150 Ω $R_g$ values are applied, producing 141 ns, 201 ns, 246 ns 277 ns and 346 ns $i_d$ fall times. The corresponding turn-on and turn-off parameters from Table 2 are obtained by processing waveforms acquired from the oscilloscope.

Similar measurement is carried out using the advanced gate control system. This time, trimmer resistors $R_{ref1}$ to $R_{ref3}$ for the turn-on and $R_{ref4}$ to $R_{ref6}$ for the turn-off from Figure 8 are adjusted to manipulate switching sequence transitions. Such resistor values are chosen that $v_{ds}$ rise and fall times, delays and final charging and dis-

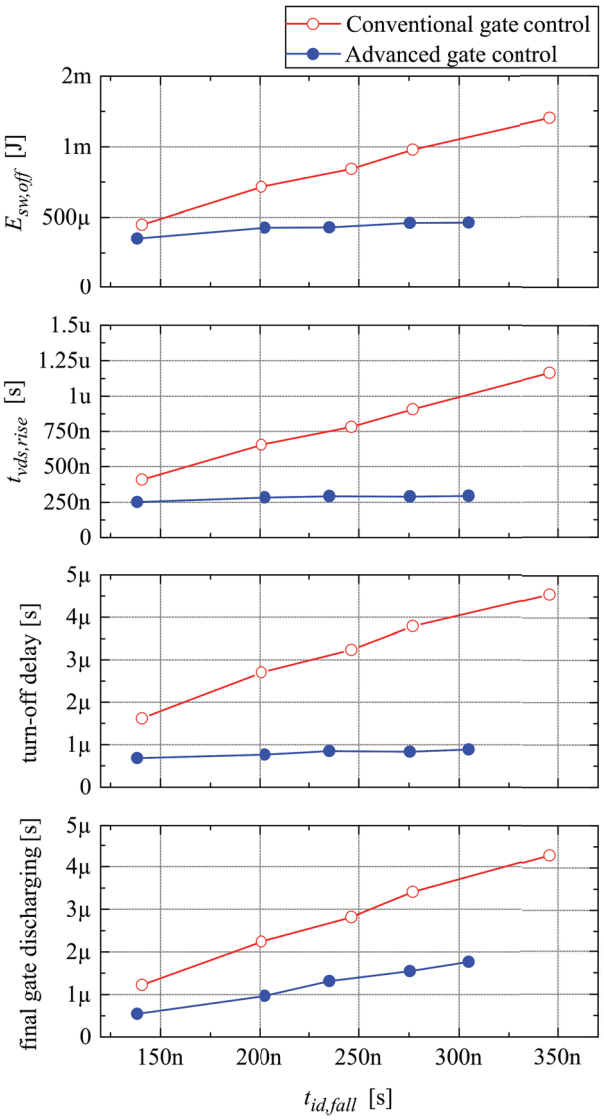


**Figure 15:** Comparison of the conventional and the advanced gate control methods, turn-off

charging durations are kept as low as possible, while $i_d$ rise and fall times are matched to the values obtained using $R_g$ control method. Again, turn-on and turn-off parameters from Table 2 are obtained by processing waveforms acquired from the oscilloscope.

The results of the comparison of the two methods are presented in Figure 14 and Figure 15.

Figure 14 and Figure 15 show that the extending drain current ($i_d$) rise and fall times produce notably less switching losses, shorter turn-off delay and shorter final charging and discharging durations when using the advanced gate control. Switching losses reduction is in this case a consequence of keeping $v_{ds}$ rise and fall time as small as possible.

The only parameter without a significant improvement is the turn-on delay, where the results of both methods are comparable. The reason for the advanced control method to be inefficient in this case is presumably the fact that the low reference current $i_{r2}$ must first charge parasitic capacitances formed by connections on the test PCB and bond pads**.** This delays the establishment of adequate conditions in current mirrors in interval $T_2$ for proper mirroring (in which only $M{\cdot}i_{r2}$ is supposed to form $i_{g,on}$). This causes that the current $i_{g,on}$ to equal zero for a period of time, resulting in $i_d$ current rise delay. The described effect is also evident in Figure 13. Just after $M{\cdot}i_{r1}+M{\cdot}i_{r2}$ are active, there is a period of $v_{gs}$ stagnation, which is a consequence of zero $i_{g,on}$. It is considered that the full integration of the amplitude manager (by using a different method for reference current setting instead of external $R_{ref1}$ to $R_{ref6}$ resistors) would eliminate the described problem.

## 6 Conclusion

The presented advanced gate control method efficiently reduces switching losses, as well as enables the minimization of the turn-off delay and final charging and discharging durations. This conclusion is obtained by comparing the advanced gate control with the conventional method. For illustration, in case of setting MOSFET drain current rise and fall times to 250 ns, the switching losses reduction is approximately 50% for turn-on and turn-off. Furthermore, the delays are reduced for 15% (turn-on) and 240% (turn-off), the turn-off final gate discharging duration is reduced for 50% while the turn-on final gate charging is as much as 10 times shorter. The system effectiveness increases with the current or voltage slope mitigation rate. The novel gate driving approach is thus proven effective.

The described method is applicable in a broad spectrum of applications, since it requires only to monitor the drain-source and gate-source voltages of the controlled MOSFET. The applications which would most significantly benefit from using the presented system are those where the switching losses dominate in the overall system losses, i.e. the applications with high switching frequency and/or high voltage and current ratings.

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# *Multiparametric Oled-Based Biosensor for Rapid Dengue Serotype Recognition With a New Point-Of-Care Serological Test*

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**Abstract:** With more than 40% of the world population potentially affected, the Dengue disease is currently one of the most spread diseases, worldwide. The Dengue disease is caused by a flavi-virus that has four different serotypes. The most dangerous complications (Dengue Hemorrhagic Fever or Dengue Shock Syndrome) may arise in secondary infections, when a patient is infected by two or more different virus serotypes.

In this paper, we present a new multi parametric immuno-fluorescence based test able to discriminate the Dengue serotypes using a serological test. The serological test is based on a disposable multi parametric biosensor able to detect the IgM or the IgG antibodies with good serotype specificity.

The test results are obtained in 30 minutes in a newly developed portable reader where the fluorescent signal of 3 μl of serum sample is detected. This new device is an OLED-based hand-held reader and therefore enabled Point-of-Care operation. Image processing software, integrated with the reader, allows to discriminate the virus serotypes also in presence of serotype cross-reactivity, which is currently one of the most important issues in flavi-virus serological test. Due to the high test sensitivity, a very early Dengue diagnostic has also been demonstrated.

**Keywords:** OLED-based biosensor; Point-of-Care diagnostics; serological test; Dengue disease

# *Multiparametrični oled-biosenzor za hitro določanje serotipa dengue z novim "point-of-care" serološkim testom*

**Izvleček:** Denga je ena od najbolj razširjenih bolezni v svetovnem merilu, saj je z njo potencialno okužene več kot 40% svetovne populacije. Povzroča jo flavi virus, poznani pa so štirje različni serotipi virusa. Najbolj nevarne komplikacije (Denga hemoragična mrzlica ali Denga šok sindrom) se lahko pojavijo kot sekundarna infekcija, kadar je bolnik okužen z dvema ali več različnimi serotipi virusa.

V prispevku opisujemo nov serološki multiparametrični test na osnovi imunofluorescence, ki razlikuje med Denga serotipi. Osnovan je na zamenljivem multiparametričnem biosenzorju, ki detektira protitelesa IgG in IgM z dobro specifičnostjo za serotipe. Z novo razvitim in predstavljenim prenosljivim čitalcem, ki detektira fluorescenčni signal v 3 μl vzorca seruma dobimo rezultate testiranja v 30 minutah. Čitalec na osnovi lastno razvitega OLED vzbujevalnega vira je ročne izvedbe in omogoča t.i. diagnosticiranje na samem mestu odvzema vzorca (angl. Point-of-Care).

Razvita programska oprema, ki je vgrajena v čitalec in obdela dobljeni fluorescenčni signal, omogoča razlikovanje med serotipi virusa tudi v primeru navzkrižne reaktivnosti, kar je eden od najpomembnejših izzivov v seroloških testih za flavi virus. Ker je test zelo občutljiv, ga je možno koristno uporabiti v primerih diagnostike bolezni v zgodnji fazi razvoja.

**Ključne besede:** OLED- biosenzorji; »point-of-care« diagnostika; serološki testi; Denga

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# 1 Introduction

Currently used Dengue diagnostics, as well as diagnostics of other flavi-viruses, are based on various techniques both serological and molecular [1,2]. However, two major problems affect the molecular and serological diagnostics of flaviruses:

1) molecular diagnostics effectiveness is limited to a specific time window as virus in patient sera or urine is present till the fifth/sixth day from the infection. As typically the disease symptoms raise after the second/third day from the infection and the patient may go to the doctor few days later, it is well possible that virus is no more present in the biological samples, thus not allowing to diagnose with this method. Nevertheless, it is worth to mention that this is the most accurate method for early disease diagnostic and Dengue serotype recognition.
2) serological diagnostics focus on the detection of antibodies produced by the immunological system to face the infection. Two different kinds of antibodies are normally detected for diagnostic purposes: immuno-globuline M, IgM (present in the sera starting from the fifth/seventh day from the infection and lasting normally about three-six months) and immuno-globuline G, IgG (start to be present in the sera after eight/fourteen days from the infection but can be detected for years). It appears evident that this diagnostics are not ideally suited for an early diagnosis. Furthermore, in flaviviruses infection there is another important issue to be considered: the cross-reactivity of antibodies raised by the immunological system against viruses of the same flavivirus family. This issue may seriously affects the accuracy of the diagnose, in particular in that regions where several kinds of flaviviruses are present (as it is for Dengue and Zika in Latin America).

To mitigate these issues the scientific community has found a complementary serological approach by looking at the presence of the non structural protein NS1 (glycoprotein) in the patient sera [3,4]. This protein is expressed by the cells at the very first stage of the virus infection (first day) and while its role is still not completely understood, its presence seems to be related with the virus replication [5]. The detection of the NS1 protein allow an early diagnostic with a better accuracy than the methods previously described, where its expression is specifically related to the virus that has generated it. It is currently detected using either sandwich ELISA or lateral flow based diagnostics.

There is also another possible early stage and specific diagnostic, currently not extensively investigated, i.e. the detection of antibodies (IgM and IgG) against the specific NS1 protein [6]. In particular, researchers focused their attention on the Dengue serotype specificity of IgM against the serotype-specific NS1 protein [7,8]. As described in there, while a certain degree of cross-reactivity between the different NS1 serotype specific antibodies still persists, it is possible to observe that the amount of IgM against the specific serotype is higher for the right serotype as compared to the others. It is also important to note that, as described in ref. [9], the anti-NS1 IgM are raised in a very early stage of the patient infection. In the same reference it is also reported that the anti-NS1 IgM may be observed almost simultaneously with NS1 proteins in serological tests.

Therefore, following this idea, we have realized a multi parametric, disposable cartridge by depositing a 1 µl drops of NS1 protein on the cartridge transparent substrate for each of four Dengue serotypes to detect the presence of specific anti-NS1 IgM and IgG. The sera of the Dengue patients, kindly provided by local hospitals, has been diagnosed. The tested sera have been previously characterized by other techniques (Enzyme-Linked Immunosorbent Assay (ELISA) for anti-virus IgM, IgG and protein NS1, and Reverse Transcription Polymerase Chain Reaction (RT-PCR)). Using a secondary labeled (ALEXAFLUOR 430) antibody in an inverse immuno fluorescence method, it was possible to detect the presence of Dengue anti-NS1 antibodies, identifying their serotype. The fluorescence detection has been performed using the hand-held reader developed at OR-EL d.o.o. and based on an Organic Light Emitting Diode (O-LED), which allows to optimally excite the fluorophore emission [10,11,12]. The fluorescence signal was detected using both a high sensitivity scientific CCD camera and a new CMOS sensor fitted to the reader. Specifically developed image processing software has been used to acquire the images, analyze them and perform a quantification of the fluorescence signal.

To present our work the following paper architecture has been adopted: a short description of the methods used in our experiments is given in section 2, the results obtained using the previously characterized patients sera are presented in section 3 and finally, the discussion on the obtained results is presented in the section 4.

# 2 Methods

## 2.1 Disposable cartridge preparation

Our diagnostic point-of-care system adopts a low cost disposable cartridge, developed at OR-EL d.o.o. The car-

tridge is realized using black plastic and a central hole (Fig. 1, top). A highly transparent polystyrene substrate (T > 90%, thickness 180 μm), chemically functionalized to present a hydrophilic surface, is then attached to the bottom of the the hole to obtain a 150 μl reaction chamber. Two different cartridge types have been realized: the first one with a single reaction chamber and a second one with four channels to implement the fluidic circuit to feed the reaction chamber. Four 1μl spots of the four different NS1 Dengue serotype specific glycoprotein solution have been then deposited manually on the transparent substrate by the pipette.

The NS1 protein solutions have been obtained diluting a 0.5 mg/ml NS1solution in carbonate buffer 1mM at a dilution ratioof 1:50. The four spots have then been incubated overnight at room temperature. The positions of the different Dengue NS1 spots on the cartridge transparent substrate is shown in Fig.1, bottom image.

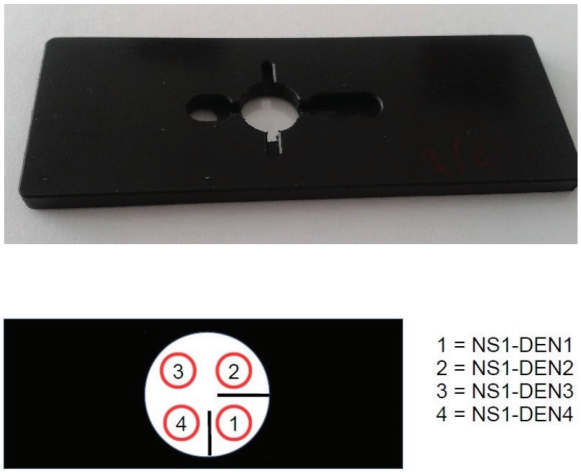


**Figure 1:** Top image: the plastic cartridge with fluidic circuit. Bottom image: geometry of the different serotype specific antigens deposition on the transparent substrate of the reaction chamber.

### *2.2 Diagnostics test procedure*

In order to detect the presence of IgG and IgM anti-NS1 in the patient's sera the following procedure has been adopted.

A volume of 150 μl of diluted serum has been put in the reaction chamber in contact with the NS1 protein spots (serum dilution 1:50 in PBS-T, phosphate saline buffer with 0.05% of Tween 20, total amount of sera 3μl) and incubated at T > 37 °C for 15 minutes. In the case of IgM test a preliminary step for IgG removal from the patient serum has been performed.

After washing with 150 μl of PBS-T, we performed a second incubation by using a 120 μl solution of secondary antibodies (anti-IgG or anti-IgM), conjugated with AlexaFluor 430 in a dilution of 1:40, starting from a concentration of 2 mg/ml. Also this second incubation was performed at T > 37 °C for 15 minutes. After the final wash with 150 μl of PBS-T, the dried slide has been measured to detect the fluorescence of the spots and to identify the Dengue anti-NS1 antibodies presence as well as their reactivity with the serotype specific antigens.

### *2.3 Fluorescence measurement*

The detection of the fluorescence spot has been obtained with two setup approaches. The first one was by using a high sensitivity scientific CCD camera (Hamamatsu C8484-G03) and the second one was by using the prototype reader equipped with the CMOS sensor and the specifically developed software to perform the image processing and automated spot recognition. The results obtained with the two presented setup approaches produced comparable results (article in preparation). In this paper we discuss only the results obtained with the CCD camera. The spot fluorescence was excited with a deep blue OLED ($\lambda_{peak}$ = 436 nm, FWHM= 45 nm), powered with a voltage of 7.0 V and emitting an optical power density of 85 mW/cm$^{2}$. For the complete OLED description see ref. [10,11,12]. The emitted radiation has been filtered with a high-pass filter with cut-off frequency at 500 nm and a transmission of T >90% in the transmission region and T< $10^{-5}$ in the blocking region. The fluorescence signal has been observed using a band-pass filter centered at 540 nm with FWHM=40 nm and with a transmission of T >90% in the transmission region and T< $10^{-5}$ in the blocking region. All images have been acquired with an Integration Time of 30 sec, with the CCD gain set at maximum. To quantify the fluorescence signal the images acquired have been despeckled after the background subtraction. A 12-bit digitizater provided intensity values from 0 to 4095. All acquired images have been processed using the open source software Image J (W.S. Rasband, U.S. National Institute of Health, Bethesda, Maryland, USA.), while the images acquired with the prototype reader, always with 12 bits digitizer, have been processed using the specific software developed at University of Bologna. The fluorescence intensity value has been obtained as the average value of the pixels gray level in the emitting spot area.

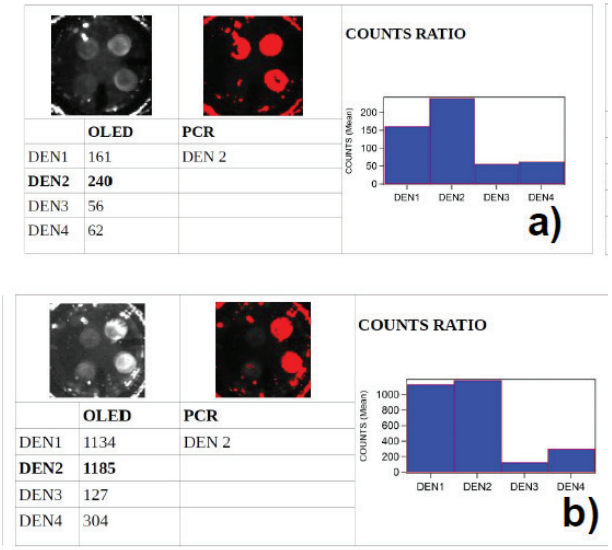


**Figure 2:** Fluorescence image acquired with the CCD camera and the same image with threshold applied, to outline the brightest spots: a) anti-NS1 IgM detection with NS1 spots deposited as shown in Fig. 1, b) anti-NS1 IgG detection with NS1 spots deposited as shown in Fig. 1.

## 3 Results

The fluorescence images acquired after sera sample processing in the disposable cartridge exhibited the presence of multiple spots due to the intrinsic cross-reactivity of the anti-NS1 antibodies. However, for most samples, one spot was clearly brighter than the others allowing the serotype recognition, as reported in ref. [9] and shown in Fig. 2.

As reported also in literature [8,9], the better serotype specificity for the current infection is achieved by considering the results of the anti-NS1 IgM test. Moreover, considering the anti-NS1 IgG test it is possible to observe the presence of previous Dengue infections due to a different Dengue serotype. This allows to recognize secondary infections and to understand the kind of serotype present in the first Dengue episode. In the case depicted in Fig. 2.b it is possible to observe the traces of a previous infection with Dengue serotype 1.

In our experiment, a 32 Dengue patient sera samples, kindly provided by Institute for Tropical Diseases, Hospital Sacro Cuore – Don Calabria, Negrar (VR), Italy, have been analyzed. All sera have been already characterized by the Hospital for the presence of IgG, IgM (against the virus) and NS1 (by different ELISA tests) and with a PCR test to identify the Dengue serotype. It has to be mentioned that there was no indication though on what day from the symptoms onset the samples were collected. Consequently, as explained in the introduction, only 19 from 32 samples have been serotype identified by PCR. The other 13 samples were virus-less, which may be due to the late blood collection (after the seventh/eighth day from infection).

Among the 32 samples, 21 have been found positive to the presence of NS1 (test BioRad and SD), 12 were positive to anti-virus IgM (using two tests,FGM and SD), 8 were with doubt (one test positive while the second negative) and 12 were negative.

The anti-virus IgG tests showed the presence of 7 positive samples, 14 negative samples and 11 with doubt. The OLED anti-NS1 test gave the following results: 28 IgM positive results and 4 IgM negative results, 17 IgG positive results, 12 IgG negative results and 3 IgG with doubt. From these results it was possible to observe that the OLED anti-NS1 test was more sensitive than the standard IgM anti-virus serological test (ELISA), being able to recognize the positive samples also at a stage where the standard ELISA test was not able to recognize them. However for these early stage sera samples, the serotype recognition was not found very precise. Only 50% of the PCR measured samples were correctly identified, due to a weak fluorescence signal. Generally, in the case of incorrectly identified samples, the first fluorescence signal was concentrated in the spot position corresponding to the Dengue serotype 3 and 4 (see Fig.3a). On the other hand, 10 out of 13 samples not identified by PCR (as presumably collected after the seventh day from the symptom onset) presented a very strong and well defined serotype definition, as shown in Fig.3c and Fig.3d. A first statistical characterization of this new test has also been carried out. After the manual production of 20 cartridges and by depositing four spots of the same antigen NS1-DEN3, the serum of the same patient was used on each cartridge. All these new tests have then been re-measured. Using this procedure we calculated the test inter and intra-assay values. Using always the same manual protocol for all the serological OLED tests, we obtained an intra-assay value of 9.4% and an inter-assay value of 12.7%.

In the further work we expect better values by using completely automated procedure, from spot deposition to fluidic sample manipulation.

## 4 Discussion

A serological diagnostic analysis for the simultaneous detection of different Dengue serotypes has been performed on different human sera samples. Herein,

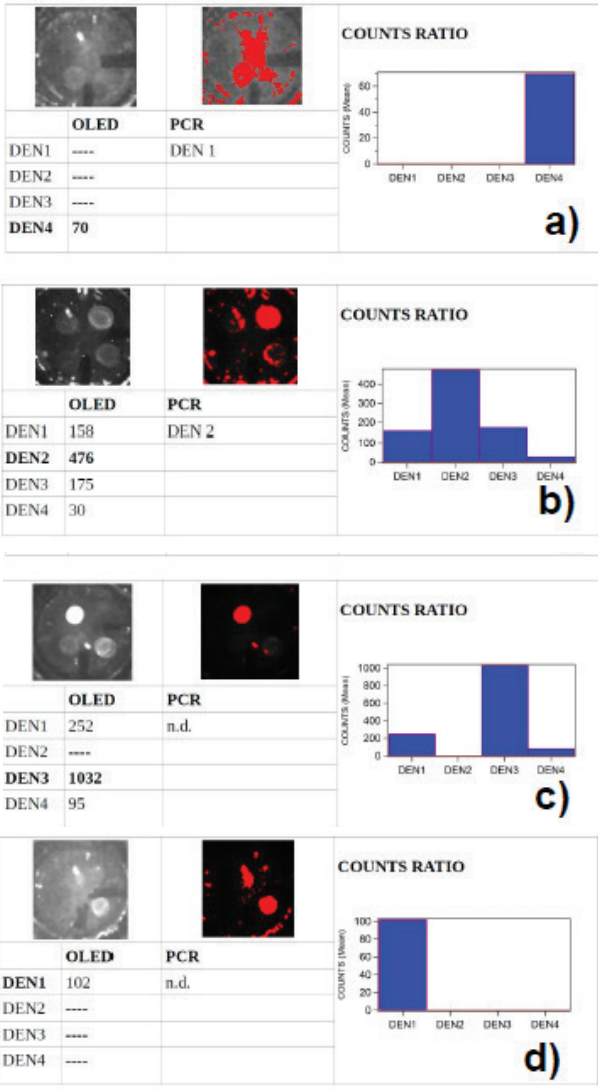


**Figure 3:** a) early Dengue serum sample IgM anti-NS1, b) correct serotype identification of IgM anti-NS1, c) and d) clear serotype identification of IgM anti-NS1 with sera sample not identified with PCR.

an inverse immuno fluorescence procedure in a multi parametric disposable cartridge has been used. For both IgM and IgG anti-NS1 fluorescence detection, a cross-reactivity between different serotype specific antigens has been observed, with a strong variability for different samples. However, the serotype recognition is clearly indicated by looking at the position of the brightest fluorescence signal recorded with a CCD camera, as shown in Fig.2 and 3. The comparison with standard ELISA and PCR tests performed on the same samples lead us to 3 significant observations:

1) The use of the OLED immuno fluorescence test allows an early detection of Dengue infection, comparable with a standard NS1 ELISA test;
2) The serotype recognition seems to be not very precise using early stage disease sera samples. Much more evident serotype recognition is observed in sample collected in a convalescent disease stage. In this case up to 85% of the PCR non-identified samples can be clearly attributed to a defined serotype in a IgM OLED based immuno fluorescence test (see Fig. 3c and d);
3) In the early stage samples, with the evidence of IgM anti-NS1 signal (while weak, around 80 counts per fluorescent spot), the serotype was not correctly identified by the spot position. In this case, the most frequently illuminated spots correspond to the positions of DEN 3 and 4 (see Fig.3a). Further investigations are planned to understand this point.

In order to better understand the relation of the immuno fluorescence Dengue serotype identification with the day of sera collection, we have obtained from another hospital the human sera samples of the same patient, but collected in specific different disease periods.

These new experiments will be presented in a forthcoming paper, which is in preparation. The already obtained results confirm our observation of a very good serotype identification (in IgM anti-NS1 test) in sera samples collected after the seventh/eighth day from the disease symptom onset.

In the case of IgG test, combined with the IgM test, it is also possible to obtain a supplementary information on the current infection. In particular when comparing the IgM and IgG test it is possible to recognize a secondary infection and understand the different serotypes involved in the primary and secondary infection. As shown in Fig. 2, it is clear that the secondary infection is due to the Dengue serotype 2 (result of IgM test). While looking at the result of the IgG test it is possible to understand that probably the primary infection was due to Dengue serotype 1. So this method can become useful also for epidemiological studies in geographical regions where more serotypes are co-circulating and where it is not easy to collect blood sera in the early stage of the disease. To apply this new multi parametric test to Point-of-Care, a portable reader, using the same cartridge, has been developed. This new reader is based on a CMOS sensor and it was tested by using the same samples described in this paper. A picture of the hand-held reader is shown in Fig. 4. The reader is operated from a laptop or a tablet via USB and the acquired image can be directly processed in the laptop using the custom developed software.

Currently we are working on an automatic fluidic circuit to enable a complete serological analysis in 30 minutes, directly at the patient site. We are confident that the

automated system will also improve the inter and intra-assay reproducibility.


**Figure 4:** Hand held reader device, here shown with the case dismounted. A credit card in the forefront, is used for dimensional comparison purpose.

## 5 Conclusions

The OLED-based inverse immuno fluorescence multi-parametric analysis of the four Dengue serotypes has confirmed a very good sensitivity for early detection of Dengue disease (comparable with an ELISA detection of NS1 protein in sera). While the specific serotype recognition is not very accurate in the very early stage of the infection, much more accurate serotype recognition by detection of anti-NS1 IgM has been observed using blood sample collected after the seventh day from the symptoms onset. A second set of measurements (not presented here, paper in preparation) has confirmed a very good serotype specificity using these kind of sera. A Point-of-Care reader has also been developed, allowing to perform these analysis in a very short time and with high sensitivity and specificity due to the software image processing.

## 6 Acknowledgments

The authors wish to thanks Dr. Francesca Perandin, Dr. Fabio Formenti and Dr. Zeno Bisoffi of Center for Tropical Diseases, Hospital Sacro Cuore – Don Calabria, Negrar (VR), Italy for kindly providing the characterized human sera samples. An acknowledgment also to Dr. Maria Giovanna Perrotta for helping in the experiments.

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# Radiation Induced Multiple Bit Upset Prediction and Correction in Memories using Cost Efficient CMC

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**Abstract:** This paper presents a cost efficient technique to correct Multiple Bit Upsets (MBUs) to protect memories against radiation. To protect memories from MBUs, many complex error correction codes (ECCs) were used previously, but the major issue is higher redundant memory overhead. The proposed method called counter matrix code (CMC) utilizes combinational ones counter and parity generator with less redundant memory overhead. CMC based on error predictor predicts the exact number of upsets before the actual error detection and correction process. The proposed technique uses Encode-Compare for minimizing the cost and increase the speed of the decoding process. The results are compared to the well-known codes such as CRC, Hamming and other matrix codes. The obtained results show that the correction coverage per cost (CCC) of the proposed scheme is higher than other traditional techniques. The mean time to repair (MTTR) of the proposed scheme is 3 times reduced than Xilinx cyclic redundancy check (CRC) + Reload technique for 100% correction coverage. At the same time MTTR of the proposed scheme is 0.3 ms, 0.2 ms and 1.8 ms less than I3D, DMC and MC, respectively with improved correction coverage.

**Keywords:** Multiple bit upsets (MBUs); memories; ones counter; parity codes; mean time to repair (MTTR)

# Napoved in korekcija s sevanjem povzročenih večbitnih napak v pomnilnikih z uporabo učinkovitih CMC kod

**Izvleček:** Članek predstavlja učinkovito metodo korekcije večbitih napak (MBU) za zaščito pomilnikov pred sevanjem. V preteklosti so se za zaščito pomnilnikov uporabljale številne kompleksne metode popravljanja napak, ki pa so zahtevale veliko spominskega prostora. Predlagana metoda CMC združuje števec in generator paritete z manjšo zahtevo po redundančnem spominu. CMC napove natančno število napak pred dejansko detekcijo in korekcijo. Rezultati so primerjani z ostalimi metodami kot so: CRC, Hamming in druge. Rezultati izkazujejo učinkovitejšo korekcijo kot konvencionalne metode, pri čemer je povprečen čas korekcije 3 krat krajši kot pri Xilinx CRC tehniki. Istočasno je MTTR 0.3 ms, 0.2 ms in 1.8 ms krajši od I3D, DMC in MC.

**Ključne besede:** večbitne napake (MBUs); pomnilniki; pariteta ; števec; parity codes; povprečni čas korekcije (MTTR)

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## 1 Introduction

Today Electronic Design Automation (EDA) industries aims to make reliability the next level of radiation protection by drawing on advances in fault tolerant techniques to protect CMOS memory chips and promoting the protected memory chips to space and safety critical applications. SRAM memories are mainly utilized by reconfigurable devices like field reprogrammable gate arrays (FPGAs) and recent programmable system on chips (SoCs). Recently the usages of SRAM memories are increased and occupied more than 90% of chip area in modern SoCs [1-3]. These SRAM memories are disturbed by soft errors and distresses system reliability and sustainability [4-5]. Minimum transistor size and increased memory density due to technology scaling are becoming increasingly susceptible to multiple bit up-

sets (MBUs) [6]. The largest MBUs size observed in the neutron induced experiment is 24 bits [7]. For smaller nanometer technologies, this count of MBU size is even more [6]. This status evidently shows the significance of protecting SRAM memories against MBU incidents.

Several proven techniques have been addressed to protect SRAM memories from radiation induced soft errors in FPGA configuration frames. Xilinx design flow consisting single event upset (SEU) mitigation step to cope single bit soft errors [18]. In addition to that Xilinx offers a two adjacent erroneous bits correction using IP block as a soft error alleviation controller based on global cyclic redundancy check (CRC) and error correction coding (ECC) technique [19]. The most common and efficient approach to preserve a good level of reliability for memory words is to use ECCs. The widely used ECC for memory protection is Hamming and odd weight codes against radiation induced soft errors due to their ability to mitigate single bit upsets (SBUs) practically with reduced energy and area overhead [8], [9]. On the other hand, single charged particle can provoke MBUs in the memory words and these MBUs are not corrected by these single bit correctable ECCs. However, there are highly developed ECCs such as Reed–Solomon codes [15], Reed–Muller code [10] and punctured difference set (PDS) codes [16] have been used to mitigate MBUs in memories. But the encoding and decoding steps are more complex to cope with MBUs in these highly developed codes. More over this is achieved at the expense of high area, delay and power consumption.

In matrix code (MC) [11], two errors are corrected based on Hamming and vertical syndrome bits in all cases. Recently DMC proposed by Jing Guo et.al to correct MBU with high reliability, but it uses more redundant bits. For 32 bit memory word, 36 numbers of redundant bits are needed to correct MBU in DMC. This extra bits occupy more area in memory chip [12]. Parallel error correction code has been presented to correct MBU's with huge area overhead [13]. More recently, in [14], 2-D ECCs such as 2-D SHMC (Symbolic Hamming Matrix Code) and 2-D RMC (Reconfigurable Matrix Code) has been proposed to efficiently mitigate MBUs of 32-bit memory word. The advantage of these codes is that the delay is minimized due to the Encode-Compare mechanism instead of Decode-Compare mechanism. In [22], an approach that combines interleaved 3-D parity technique (I3D) with erasure code has been conceived to be applied at architectural level. It uses horizontal, vertical and diagonal parity bits to detect MBUs and erasure codes for MBU correction. The results achieved from this approach shown that additional recovery time needed to correct MBUs over other codes. Based on the combinational ones counter and parity code, preliminary version of algorithm has been proposed for MBU error prediction and error correction in SRAM [17].

In the proposed work, both intra and inter word error detection and correction and error prediction are introduced by combinational counting operation. The redundant bits used for the detection and correction are computed from the outputs of row and column counters. Computing redundant bits from group of words reduces the redundant memory overhead. This work uses Encode-Compare instead of Decode-Compare mechanism in decoder for reducing the delay overhead.

The presentation of this work can be divided into five sections. In section II, the proposed CMC is introduced and its encoder and decoder architectures are given with sample calculations. Section III discusses the correction coverage and overhead analysis of the various MBU mitigation methods. Conclusions and future work ideas are given in Section IV.

## 2 Proposed counter matrix code

In this section, CMC encoding and decoding algorithm is proposed to predict and correct the MBUs and the VLSI architectures for encoder and decoder are presented. The proposed CMC based encoding and decoding algorithm appears to lend itself to detect both

**Table 1:** 128-bit logical organization of CMC

| S.No | Symbol8 | Symbol7 | Symbol6 | Symbol5 | Symbol4 | Symbol3 | Symbol2 | Symbol1 | $H_{CC}$ | $H_{PC}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | $B_0^{(31-28)}$ | $B_0^{(27-24)}$ | $B_0^{(23-20)}$ | $B_0^{(19-16)}$ | $B_0^{(15-12)}$ | $B_0^{(11-8)}$ | $B_0^{(7-4)}$ | $B_0^{(3-0)}$ | $H_0^{(3-0)}$ | $H_{p0}^{(3-0)}$ |
| 1 | $B_1^{(31-28)}$ | $B_1^{(27-24)}$ | $B_1^{(23-20)}$ | $B_1^{(19-16)}$ | $B_1^{(15-12)}$ | $B_1^{(11-8)}$ | $B_1^{(7-4)}$ | $B_1^{(3-0)}$ | $H_1^{(3-0)}$ | $H_{p1}^{(3-0)}$ |
| 2 | $B_2^{(31-28)}$ | $B_2^{(27-24)}$ | $B_2^{(23-20)}$ | $B_2^{(19-16)}$ | $B_2^{(15-12)}$ | $B_2^{(11-8)}$ | $B_2^{(7-4)}$ | $B_2^{(3-0)}$ | $H_2^{(3-0)}$ | $H_{p2}^{(3-0)}$ |
| 3 | $B_3^{(31-28)}$ | $B_3^{(27-24)}$ | $B_3^{(23-20)}$ | $B_3^{(19-16)}$ | $B_3^{(15-12)}$ | $B_3^{(11-8)}$ | $B_3^{(7-4)}$ | $B_3^{(3-0)}$ | $H_3^{(3-0)}$ | $H_{p3}^{(3-0)}$ |
| $\mathbf{V_{CC}}$ | $V_{(31-28)}$ | $V_{(27-24)}$ | $V_{(23-20)}$ | $V_{(19-16)}$ | $V_{(15-12)}$ | $V_{(11-8)}$ | $V_{(7-4)}$ | $V_{(3-0)}$ | | |
| $\mathbf{V_{PC}}$ | $V_{p(31-28)}$ | $V_{p(27-24)}$ | $V_{p(23-20)}$ | $V_{p(19-16)}$ | $V_{p(15-12)}$ | $V_{p(11-8)}$ | $V_{p(7-4)}$ | $V_{p(3-0)}$ | | |

inter-word and intra-word MBUs in memory system. The differentiator of CMC from other coding techniques is soft error prediction, which predicts the exact number of soft errors present in the memories before the correction task.

### *2.1 Proposed CMC encoder and decoder*

The cost of the ECC technique is directly proportional to the required redundant bits [11]. In the proposed CMC, group of words are taken as input to the encoder and decoder instead of single word taken in the existing works, for achieving lower redundant bits. i.e. N-bit words are arranged in M rows each forms a matrix of size M×N. Each word (row) is divided into k symbols of m bits N= k×m. The horizontal counter codes ($H_{CC}$), horizontal prediction codes ($H_{PC}$), vertical counter codes ($V_{CC}$) and vertical parity codes ($V_{PC}$) includes the vertical counter bits $V_{(3\text{-}0)\ldots}V_{(31\text{-}28)}$ and horizontal counter bits $H_0^{(3\text{-}0)}\ldots H_3^{(3\text{-}0)}$ for error prediction and the vertical parity bits $V_{P(3\text{-}0)\ldots}$ $V_{P\,(31\text{-}28),}$ horizontal parity bits $H_{P0}^{(3\text{-}0)}\ldots.$ $H_{P3}^{(3\text{-}0)}$ for error correction respectively. To explain the proposed CMC, 32-bit words are considered as an example, arranged in 4 rows each forms 4×32 matrix as shown in Table I. The required number of parity bits for the group length is given in Table II. It shows that more number of words in a group needs less number of redundant bits. For example the computation of redundant bits for 8 words in a group needs 64 redundant bits and 4 words in a two different group (2×48) is 96 redundant bits. But more number of words in a group will affect the percentage of correction coverage. For this reason this work limits the number of words in a group to 4.

**Table 2:** Required no. of parity bits per group

| No. of words per group | No. Of Redundant bits |
|---|---|
| 1 | 24 |
| 2 | 40 |
| 3 | 44 |
| 4 | 48 |
| 5 | 52 |
| 6 | 56 |
| 7 | 60 |
| 8 | 64 |

The proposed CMC has two steps, first combinational ones counter operation is performed on data bits for predicting and reducing the number of redundant bits for further error detection and correction. For an array of memory words, the horizontal (row) counter code bits can be calculated using Equation 1. For example the horizontal counter code of first row word is shown in (Equation 2) – (Equation 5)

$$H_M m = \sum_{k=0}^{k-1} B_M \,\hat{}\, (4k+m) \tag{1}$$

$$H_0^0 = B_0^0 + B_0^4 + B_0^8 + B_0^{12} + B_0^{16} + B_0^{20} + B_0^{24} + B_0^{28} \tag{2}$$
$$H_0^1 = B_0^1 + B_0^5 + B_0^9 + B_0^{13} + B_0^{17} + B_0^{21} + B_0^{25} + B_0^{29} \tag{3}$$
$$H_0^2 = B_0^2 + B_0^6 + B_0^{10} + B_0^{14} + B_0^{18} + B_0^{22} + B_0^{26} + B_0^{30} \tag{4}$$
$$H_0^3 = B_0^3 + B_0^7 + B_0^{11} + B_0^{15} + B_0^{19} + B_0^{23} + B_0^{27} + B_0^{31} \tag{5}$$

For an array of memory words, the vertical (column) counter code bits are calculated using Equation 6. For example the vertical counter code of first column is shown in (Equation 7)-( Equation 10)

$$V_N = \sum_{m=0}^{m-1} Bm\hat{}\,(N) \tag{6}$$

$$V_0 = B_0^0 + B_1^0 + B_2^0 + B_3^0 \tag{7}$$
$$V_1 = B_0^1 + B_1^1 + B_2^1 + B_3^1 \tag{8}$$
$$V_2 = B_0^2 + B_1^2 + B_2^2 + B_3^2 \tag{9}$$
$$V_3 = B_0^3 + B_1^3 + B_2^3 + B_3^3 \tag{10}$$

where k is the number of symbols in a word; m is the number of bits in a symbol and M is the number of words in the array. In the second step horizontal and vertical parity bits can be calculated from the horizontal and vertical counter codes. Horizontal parity bits are calculated from horizontal counter codes using Equation 11. Similarly, vertical parity bits are calculated from horizontal counter codes using Equation 12. Finally, both the intra and inter word errors will be corrected in decoding step.

$$H_{pM} m = \{\ 0 \ \ for\ \ H_M m = 0,2,\ldots k\ ;\ 1\ \ for\, H_M m = 1,3,\ldots k-1\ ; \tag{11}$$

$$V_{pN} m = \{\ 0 \ \ for\ \ V_N m = 0,2,\ldots k\ ;\ 1\ \ for\, V_N m = 1,3,\ldots k-1\ ; \tag{12}$$

The encoding and decoding algorithms are given below to understand the flow.

Algorithm for Encoding.

ACW - Array of configuration word
$H_{CC}$ – Horizontal (row) counter codes
$V_{CC}$ – Vertical (column) counter codes
$H_{PC}$ – Horizontal (row) parity codes
$V_{CC}$ – Vertical (column) parity codes

Input: *ACW [4 ×32=128 bits]*
Output: $H_{CC}$, $V_{CC}$, $H_{PC}$, $V_{PC}$
1: *ACW to be written*
*2: Split into K symbols per Configuration word*
2: while *symbols* = *true* do
3: for all $H_N m \in H_{CC}$ do *onescount* (*ACW*);
4: for all $H_{pm} m \in H_{PC}$ do *parity*($H_{CC}$);
5: for all $V_N \in V_{CC}$ do *onescount* (*ACW*);
6: for all $V_{pN} m \in V_{PC}$ do *parity*($V_{CC}$);
6: update $H_{CC}$, $V_{CC}$, $H_{PC}$, *and* $V_{PC}$;
7: end while
8: return *ACW*;

Algorithm for *Decoding*.

Input : Errored *ACW[4 ×32=128 bits], Hcc, Vcc, Hpc, Vpc*
Output : error prediction value (epv) , corrected word (cw)
1: Read *errored ACW [ACWm]*
*2: Split into K symbols per Configuration word*
*3: Read Hcc,Vcc,Hpc,Vpc*
4: while *symbols* = *true* do
5: for all $H_N m \in Hccm$ do *onescount* (*ACWm*);
6: for all $H_{pm} m \in Hpc$ do *parity*(*Hcc'*);
7: for all $V_N \in Vccm$ do *onescount* (*ACWm*);
8: for all $V_{pN} m \in Vpc$ do *parity*(*Vcc'*);
9: update *Hcc',Vcc',Hpc',Vpc'*;
10: find hsc= diff(Hcc-Hcc')
11: find hsp= diff(Hpc-Hpc')
12: find vsc= diff(Vcc-Vcc')
13: find vsp= diff(Vpc-Vpc')
14: if((hsp==0)&(vsp==0))
15: begin
16: {Syndrome =0
17: error=0 }
18: end
19: else
20: begin
21: { Syndrome ≠ 0
22: error ≠ 0
23: epv = {hsc,vsc};
24: $B_{intracorrect}$ = ACW $m$ XOR vs
$B_{intercorrect}$ = ACW $m$ XOR Hs } }
25: end
26: end while
22: return *ACW*;

## 2.2 Proposed fault-tolerant memory architecture

The proposed fault-tolerant memory architecture is illustrated in Figure 1. First, for the period of encoding process, original data bits *D* are fed to the encoder, and then $H_{CC}$, $H_{PC}$ and $V_{PC}$ are obtained from the CMC encoder. The obtained CMC codeword consist data and redundancy bits, which are stored in the separate SRAM memories. The MBUs occurred in the memory is being corrected at the decoding process using the CMC Encode-Compare.

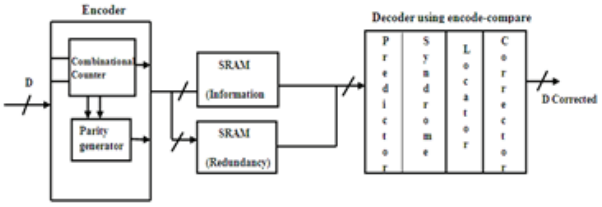



**Figure 1:** Fault-tolerant memory architecture

The detail architecture of CMC encoder is shown in Figure 2. First, the $H_{CC}$ *and* $V_{CC}$ bits are computed by performing 8-bit combinational counting operation of selected sliced bits of symbols per row and 4-bit combinational counting operation of selected sliced bits of symbols per column respectively. Second the 4-bit $H_{PC}$ are computed by performing XOR operations of respective row $H_{CCs}$, totally 16 bit $H_{PCs}$ are computed for 4 rows. The 1-bit $V_{PC}$ is computed by performing XOR operations of respective column VCCs, totally 32 bit VPCs are computed for 32 columns.

The proposed CMC Encoder consists of two combinational ones counter circuits, namely 8-bit combinational ones counter and 4-bit combinational ones counter. The 8-bit combinational ones counter (Row counter) shown in Figure 3(a). The row counter counts the number of one's using 9 half adders (HAs), 2 full adders (FAs) and 2 XOR gates and is given in (Equation 13). Similarly, the 4-bit combinational ones counter (Column counter) shown in Figure 3(b) counts the number of one's using 4 half adders (HAs), and one XOR gate and is given in (Equation 14). The detail architecture of CMC decoder is shown in Figure 4. Decoder consists of predictor, syndrome calculator (detector), locator and corrector. Horizontal and vertical syndrome calculator are used to detect and locate the MBUs in the memories.

$$\left.\begin{aligned} out[0] &= (a\oplus b)\oplus(c\oplus d)\oplus(e\oplus f)\oplus(g\oplus h)\\ out[1] &= (a\oplus b).(c\oplus d)\oplus(a.b)\oplus(c.d)\oplus(e\oplus f)(g\oplus h).(e.f)(g.h)(a\oplus b)\oplus(c\oplus d).(e\oplus f)\oplus(g\oplus h)\\ out[2] &= (a.b.c.d)(e.f.g.h)+[(a.b.c.d)\oplus(e.f.g.h)][(a\oplus b).(c\oplus d)\oplus(a.b)\oplus(c.d).(e\oplus f).(g\oplus h)\oplus(g.h)(e.f)\\ out[3] &= a.b.c.d.e.f.g.h \end{aligned}\right\} \quad (13)$$

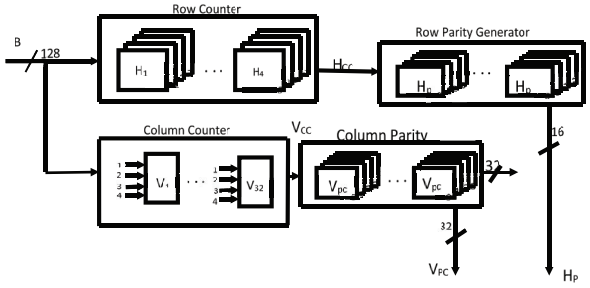
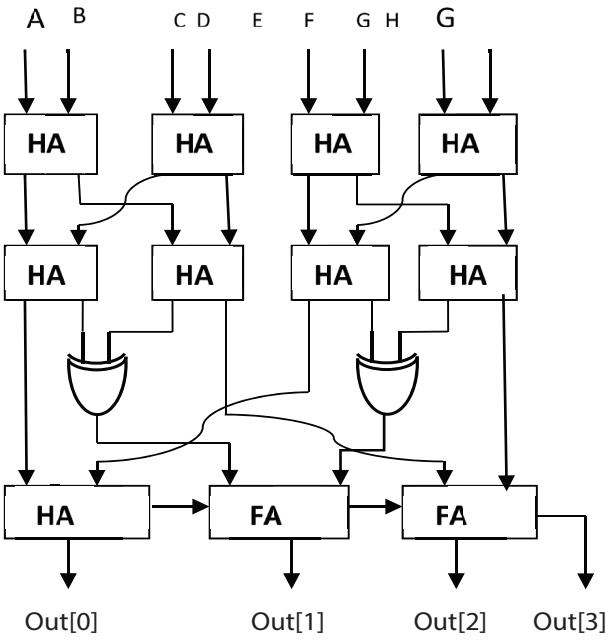
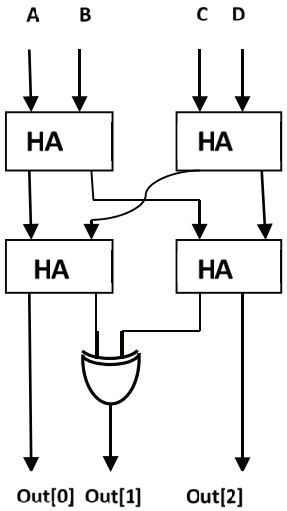



**Figure 2:** Architecture for CMC Encoder.




(a) Row Counter




(b) Column Counter

**Figure 3:** 1's counters (a) Row counter (b) Column Counter.

$$\left.\begin{aligned} out[0] &= a \oplus b \oplus c \oplus d \\ out[1] &= (a \oplus b).(c \oplus d). \oplus (a.b). \oplus (c.d) \\ out[2] &= a.b.c.d \end{aligned}\right\} \quad (14)$$

Finally corrector is used to correct the erroneous bits based on horizontal syndrome, vertical syndrome and erroneous bits.

The following example gives the computation of horizontal, vertical parity bits for MBU detection and correction for a group of words. Let us consider the original information bits (B) as 128 bits. It can be divided into four rows, each containing 32 bits. Each row is divided into 8 symbols, each containing four bits. $H_{CC}$ and $V_{CC}$ are horizontal ones counter (Row counter) and Vertical ones counter (Column counter) for predicting soft errors and reducing the number of redundant bits. An $H_{PC}$ and $V_{PC}$ bit detects and corrects the errors in 128-bits. For example the original 128-bits information is shown in Table III (a), may have intra-word errors as shown in Table III (b), and inter-word errors are shown in Table III (c), for 128-bits information. The horizontal counter codes were calculated using Equation (1)-(5) and vertical counter codes were calculated using Equation (6)-(10). The horizontal and vertical parity bits were calculated using Equation (11) and Equation (12) respectively. Finally, both the intra and inter word MBUs can be corrected by the decoding algorithm.

## *3 Correction coverage and overhead analysis*

In this section, the proposed CMC has been coded in Verilog hardware description language (HDL), simulated using Xilinx-Isim and tested its functionality for various inputs. The correction coverage and overhead analysis have been done. For fair comparisons, Hamming [8] [9], MC [11], DMC [12], SHMC [14], RMC [14], I3D [22], XILINX CRC [19] [20] are used for reference.

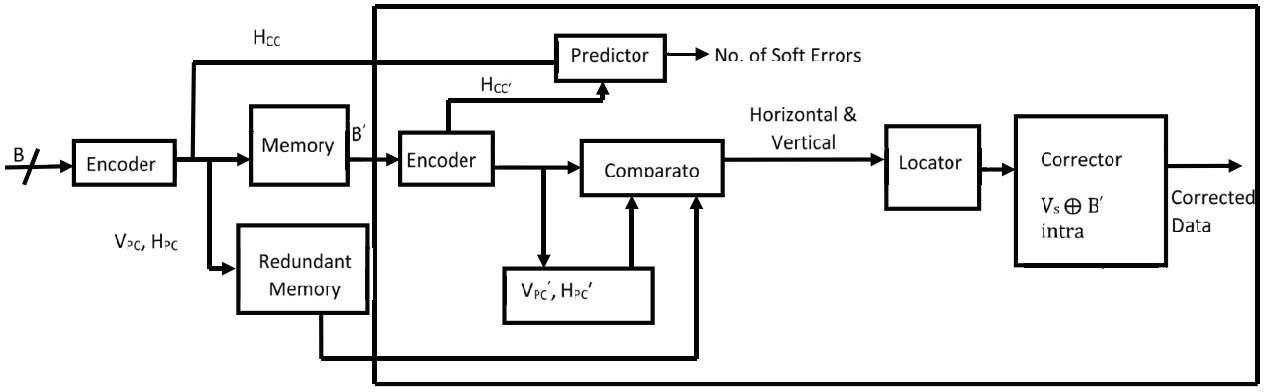



**Figure 4:** Architecture for CMC Decoder.

**Table 3:** (a) 128-bit logical organization of cmc

| S.NO | Symbol8 | Symbol7 | Symbol6 | Symbol5 | Symbol4 | Symbol3 | Symbol2 | Symbol1 | $H_{CC}$ | $H_{PC}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1010 | 1010 | 1010 | 1010 | 1010 | 1010 | 1010 | 1010 | 8080 | 0000 |
| 2 | 0101 | 0101 | 0101 | 0101 | 0101 | 0101 | 0101 | 0101 | 0808 | 0000 |
| 3 | 1001 | 1001 | 1001 | 1001 | 1001 | 1001 | 1001 | 1001 | 8008 | 0000 |
| 4 | 0110 | 0110 | 0110 | 0110 | 0110 | 0110 | 0110 | 0110 | 0880 | 0000 |
| $V_{CC}$ | 2222 | 2222 | 2222 | 2222 | 2222 | 2222 | 2222 | 2222 | | |
| $V_{PC}$ | 0000 | 0000 | 0000 | 0000 | 0000 | 0000 | 0000 | 0000 | | |

(b) Intra word error version

| S.NO | Symbol8 | Symbol7 | Symbol6 | Symbol5 | Symbol4 | Symbol3 | Symbol2 | Symbol1 | $H'_{CC}$ | $H'_{PC}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0101 | 0101 | 0101 | 0101 | 0101 | 0101 | 0101 | 0101 | 0808 | 0000 |
| 2 | 0101 | 0101 | 0101 | 0101 | 0101 | 0101 | 0101 | 0101 | 0808 | 0000 |
| 3 | 1001 | 1001 | 1001 | 1001 | 1001 | 1001 | 1001 | 1001 | 8008 | 0000 |
| 4 | 0110 | 0110 | 0110 | 0110 | 0110 | 0110 | 0110 | 0110 | 0880 | 0000 |
| $V'_{CC}$ | 1313 | 1313 | 1313 | 1313 | 1313 | 1313 | 1313 | 1313 | | |
| $V'_{PC}$ | 1111 | 1111 | 1111 | 1111 | 1111 | 1111 | 1111 | 1111 | | |

(C) Inter word error version

| S.NO | Symbol8 | Symbol7 | Symbol6 | Symbol5 | Symbol4 | Symbol3 | Symbol2 | Symbol1 | $H'_{cc}$ | $H'_{pc}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0101 | 1010 | 1010 | 1010 | 1010 | 1010 | 1010 | 1010 | 7171 | 1111 |
| 2 | 1010 | 0101 | 0101 | 0101 | 0101 | 0101 | 0101 | 0101 | 1717 | 1111 |
| 3 | 0110 | 1001 | 1001 | 1001 | 1001 | 1001 | 1001 | 1001 | 7117 | 1111 |
| 4 | 1001 | 0110 | 0110 | 0110 | 0110 | 0110 | 0110 | 0110 | 1771 | 1111 |
| $V'_{cc}$ | 2222 | 2222 | 2222 | 2222 | 2222 | 2222 | 2222 | 2222 | | |
| $V'_{pc}$ | 0000 | 0000 | 0000 | 0000 | 0000 | 0000 | 0000 | 0000 | | |

### *3.1 MBU Patterns*

In 2009, E. Ibe et .al analyzed the scaling effects on neutron induced soft error in SRAM array down to 22 nm technology node and they observed that nearly 50 % of soft errors are MBU incidents [21]. In order to fairly enumerate the MBU correction coverage of the proposed CMC technique, the detailed information about the possible MBU error patterns of 28nm SRAM array and their individual occurrence probabilities are needed. Figure 5 shows the MBU patterns and their occurrence probabilities [22] –[23].

### *3.2 Comparison for correction coverage*

To facilitate the benefits and drawbacks of the proposed scheme, it is extensively compared with previous techniques. Simulation based MBU injection experiment has been done to extract error correction coverage of the previous techniques. The original 128-bit information and the faulty information can be specified in the text fixture, and fault injection can be implemented in a test-bench. Both single and multiple bit faults were injected, in case of MBU injection around one million combinations were injected. The correction coverage of various MBU mitigation techniques such as CMC, DMC, MC, and Hamming is obtained for various intra-word error test cases and it is shown in Figure 6. It is clear that the DMC performs 100% intra error correction up to 5 bit errors and 11.8% error correction in 16 bit errors. Similarly, MC performs 100% intra error correction up to 2 bits and 0.6% error correction up to 8 bits. But the proposed CMC provides 100% protection that is possible error correction up to 32 bits. In addition to that the correction coverage depicted in Table V compares the proposed technique, proven soft error mitigation techniques and existing research techniques.

The possibility of correction coverage is tested for larger the word widths which results the higher the correction capabilities. The maximum correction capability (MCC) is given in Table IV. In DMC, the correction capability for a 64- bit and 128-bit word is up to 9 bits and 17 bits respectively. In proposed CMC, the correction capability for a 64-bit and 128-bit word is up to 36 bits

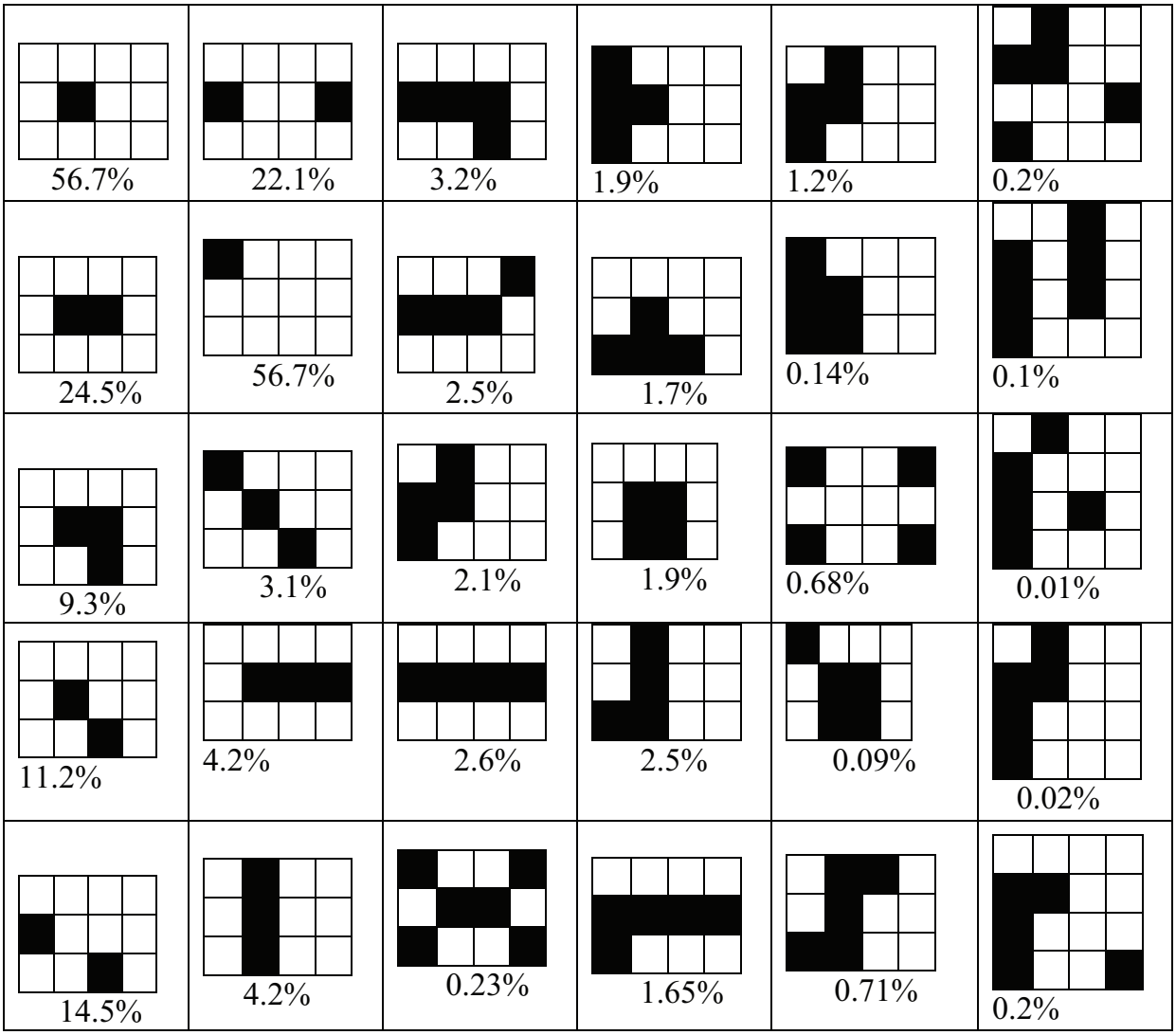



**Figure 5:** MBU patterns of high occurrence probabilities in 28nm SRAM array [22]-[23]

and 44 bits respectively. The results depicted in Table IV show that proposed CMC exceeds the performance of other codes by its efficient error tolerance capability against larger the MBU widths.

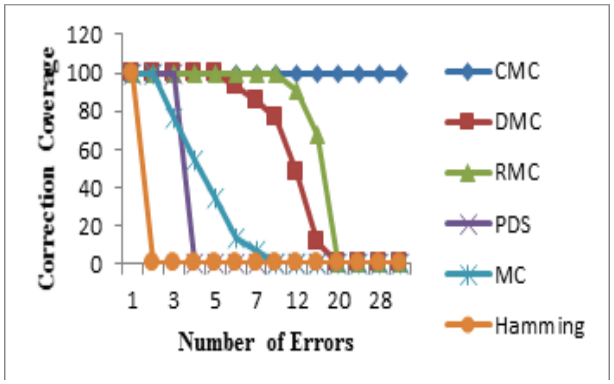



**Figure 6:** Intra word Correction coverage for various ECCs

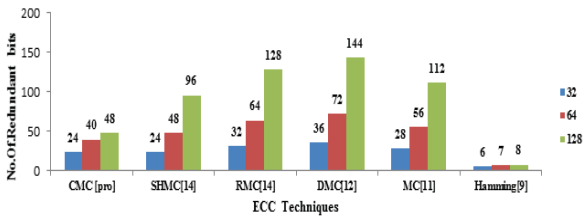



**Figure 7:** Required number of redundant bits for various error correction codes

**Table 4:** Maximum Correction Capability (MCC)

| Technique | MCC (64-bits) | MCC (128-bits) |
|---|---|---|
| CMC | 36 bits | 44 bits |
| RMC | 16 bits | 32 bits |
| DMC | 9 bits | 17 bits |
| MC | 4 bits | 8 bits |

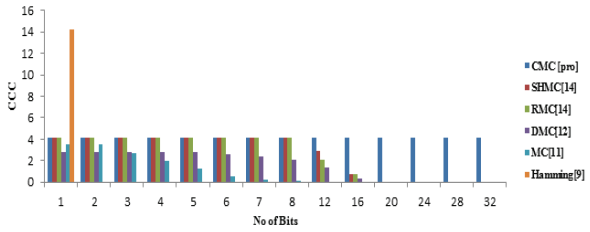



**Figure 8:** Correction coverage per cost for various error correction codes

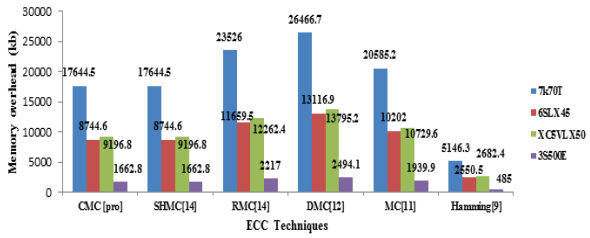



**Figure 9:** Intra word Memory Area overhead analysis of various Xilinx FPGA Devices.

### *3.3 Comparison for overhead analysis*

In order to evaluate the efficiency of error mitigation techniques, the implementation overheads of these protection codes have to be analyzed. This paper analyzes the overheads in terms of cost and correction coverage per cost (CCC). The term cost indicates the number of redundant bits required to implement the error correction codes [11]. The cost for the proposed and typical coding techniques is portrayed for 32, 64 and 128 bits in Figure 7. This implies Hamming code needs very less number of redundant bits, but their correction capability is limited to 1. DMC need more number of redundant bits compared to all other codes. Linear increasing of redundant bits for the higher word lengths of the traditional codes were shown in Figure 7. The proposed CMC needs less number of redundant bits compared to all other codes due to the inter word processing capability. The CCC results of the proposed and typical coding techniques are portrayed up to 32 bits in a word is shown in Figure 8. This implies that coding techniques should have high value of the CCC for higher reliable solution. It should be noticed that when the number of errors is more than one per word, Hamming code cannot correct any errors. The proposed CMC provides consistent performance compared to all typical coding techniques. Thus, based on the analysis given in Figure 7 and Figure 8, the proposed CMC technique is better suited for low cost and safety critical (high- Performance) applications.

The best metric used to select the appropriate coding technique for the practical solutions is mean time to repair (MTTR) which is analyzed for all soft error mitigation techniques and portrayed in Table V. MTTR-R represents the actual MTTR and additional recovery time. The results shown in the Table V implies that proven mitigation techniques [19], Xilinx CRC+ECC [20] needs minimum MTTR value, but the correction coverage for the recent scaled technology (28 nm) is not satisfactory. The technique presented in the Xilinx CRC+Reload [20] gives 100% correction coverage, but they require MTTR as almost 3-times of the other techniques and this MTTR overhead is not acceptable in real time. Next the coding techniques presented in the [14] require minimum MTTR due to Encode-Compare mechanism,

**Table 4:** Comparison of different soft error mitigation techniques

| Soft Error Correction Techniques | MTTR (ms) | MTTR-R (ms) | Correction coverage (%) | Distinguished Note |
|---|---|---|---|---|
| Proven Mitigation Techniques | | | | |
| Xilinx SEU Correction [19] | 9.342 | 0 | 51.72 | Single bit correction |
| Xilinx CRC+ECC [20] | 9.342 | 0 | 61.1 | Global detection & Single bit correction |
| Xilinx CRC +Reload [20] | 9.342 | 18.7 | 100 | External Storage required |
| Existing Research Techniques | | | | |
| Hamming code[8],[9] | 10.7 | 0 | 51.652 | Decode-Compare |
| DMC [12] | 9.6 | 0 | 95.823 | Decode-Compare |
| MC [11] | 11.2 | 0 | 93.81 | Decode-Compare |
| SHMC [14] | 6.57 | 0 | 95.913 | Encode-Compare |
| RMC[14] | 6.68 | 0 | 94.62 | Encode-Compare |
| I3D[22] | 9.343 | 0.351 | 94.2 | Erasure code |
| Proposed Technique | | | | |
| CMC[Pro] | 9.387 | 0 | 100 | Prediction & Encode-Compare |

but the correction coverage is not a maximum. DMC technique requires 9.6 ms for correcting the errors and the respected correction coverage is only about 95.823% [12]. The recent technique I3D requires 9.343 ms for detecting the error and 0.351 ms for recover the particular error word, the total MTTR is 9.694 ms and the respected correction coverage is only about 94.2% [22]. The proposed CMC require only 9.387 ms for correcting all error patterns shown in the Figure 7 and this MTTR value is almost equivalent to the proven techniques .Thus the proposed CMC technique can be used in safety critical applications compared to all typical coding techniques. Finally memory overhead for storing the redundant bits in Xilinx FPGA devices are shown in Figure 9. This implies that Hamming code need minimum memory overhead but the correction capability is limited to 1. The proposed CMC and the SHMC technique presented in [14] are require acceptable level of redundant memory overhead compared to all other codes.

## 4 Conclusion

In this paper, a novel technique CMC is proposed to cope with radiation induced MBUs. The obtained results showed that the proposed scheme has a better protection level against huge MBUs in the intra and inter words of the memory. The proposed CMC utilized Encode-Compare mechanism to predict and correct errors for a group of words, so that the MTTR value is minimum and equivalent to proven mitigation techniques with improved correction coverage. The only drawback of the proposed work is the requirement of more redundant bits to protect memory. In future the research will be conducted for improving reliability and reducing cost of the proposed technique for the below 28 nm FPGAs.

## 5 Acknowledgements

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# Combined optical model for micro-structured organic light-emitting diodes

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**Abstract:** Organic light-emitting diodes (OLEDs) with prospect of low cost, high efficiency and high quality lighting are a promising future light source. One of their limitations is poor light outcoupling, reaching only 20-30 % for conventional flat-plate lighting devices. Optical modelling and simulations are of great importance in optimizing the outcoupling efficiency. Complex structures of OLEDs, in which thin layers with emitting sources are combined with thick texturized substrate layers, require coupled optical modelling approach. We developed a combined optical model, comprising a thin layer stack where light is described as waves and thick texturized layers where light is described as rays. This combination enables simulation of OLEDs as complete devices with micro textures. We present the main considerations of the developed model. Finally, an OLED with laser structured sine textures is used to compare experimental results with simulation results obtained with the developed model.

**Keywords:** OLED; organic light emitting diode; optical modeling; light outcoupling

# Združeni optični model za mikrostrukturirane organske svetleče diode

**Izvleček:** Organske svetleče diode (OLED) predstavljajo obetajoč svetlobni vir, ki ga lahko uporabimo tudi pri razsvetljavi prostorov. Predvidena nizkocenovna proizvodnja visoko učinkovitih OLED omogoča izdelavo svetil z velikimi površinami. Ena izmed glavnih omejitev sodobnih OLED je nizka stopnja učinkovitosti izstopa svetlobe iz tankoplastne strukture elementa. Konvencionalne izvedbe OLED z gladkimi površinami dosegajo le 20-30 % stopnjo učinkovitosti izstopa svetlobe. Pomembno vlogo pri načrtovanju in optični optimizaciji struktur OLED igra optično modeliranje v povezavi z numeričnimi simulacijami. Strukture OLED združujejo tanke organske plasti v kombinaciji z debelejšimi plastmi (substrati), zato pri simulaciji potrebujemo poseben, združen optični model, ki omogoča koherentno in nekoherentno širjenje svetlobe. Razvili smo tridimenzionalni združeni optični model, kjer tanke plasti z optičnimi viri lahko obravnavamo skupaj z debelejšimi plastmi, ki hkrati vsebujejo teksture za izboljšanje učinkovitosti izstopa svetlobe. Ta kombinacija nam tako omogoča simulacije in optično optimizacijo celotnih OLED struktur, ki vsebujejo mikroteksturirane površine. V prispevku so predstavljene glavne lastnosti modela. Rezultate simulacij z razvitim modelom validiramo z izdelanimi vzorci, kjer smo teksture izdelali z laserskim graviranjem steklenega substrata.

**Ključne besede:** OLED; organske svetleče diode; optično modeliranje; ekstrakcija svetlobe

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## 1 Introduction

Over 20 % of the generated electrical power in the developed countries and a considerable amount in the developing countries is used for lighting and the consumption will continue to grow [1]. Therefore, efficient lighting is one of the cornerstones of reducing the carbon footprint for achieving a greener future. One of the emerging lighting technologies called organic light-emitting diodes (OLEDs), offers high possibilities of becoming a future lighting source, since it is a thin film, large area (and not point source like their inorganic equivalents) lightweight device with a potential to provide low cost, highly efficient and high quality general lighting [2–4]. Similar to the limited conversion efficiency of photovoltaic devices or laser power converters [5, 6], OLEDs are also facing theoretical limits. One of the main obstacles for OLEDs to reach their full potential is poor light outcoupling, as for normal

devices only ~20-30 % of the generated light reaches the far field as useful light [7, 8], while the internal conversion efficiency from an injected electron to a generated photon is close to 100 % [9–11]. Intensive research has been done in the last years to reduce the optical losses in OLEDs, see for example [12–14], but a lot of room for improvement still remains. OLEDs are optically relatively complex devices, where even planar devices include combination of thin and thick layers, a microcavity effect, a different orientation of emitting dipoles – anisotropy, coupling of light to surface plasmon polaritons (SPP), an arbitrary angular distribution of emitted light, absorption in layers and others. Therefore, optical modelling and simulations are an essential tool in design and optimization of these devices. In this article, we present an optical model that we developed for a three-dimensional (3D) simulation of OLED structures including micro textures for efficient control of light. The model couples emitting sources (dipoles) in thin organic layers with thin-film optics of surrounding layers, ray tracing in thick incoherent layers and at micro textured surfaces. The physics of the model will be presented, followed by selected examples of validation on realistic OLED structures.

## 2 Optical model

### 2.1 OLED structure and operation

A conventional bottom-emitting p-i-n OLED structure is presented in Figure 1. It consists of a thin layer stack,

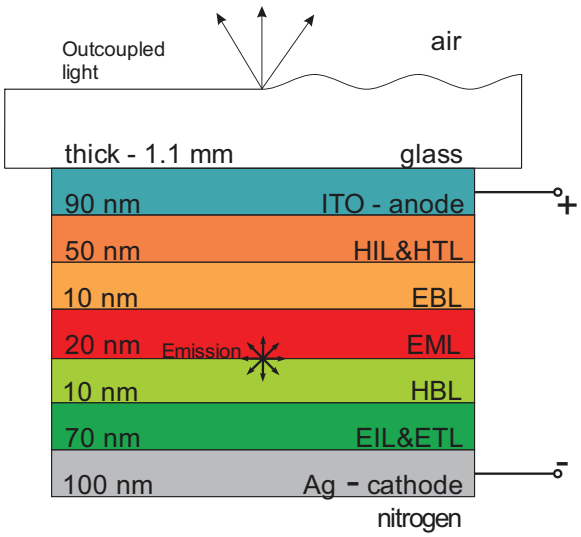


**Figure 1:** Structure of a conventional p-i-n bottom-emitting red OLED deposited on a glass substrate and encapsulated under a nitrogen atmosphere. Texturization of the substrate (on light escaping side) is indicated on the right hand side of the substrate.

containing light emission sources and a thick transparent substrate, e.g. glass or transparent foil that can be non-structured or structured.

Light is generated in thin emission layer (EML) by radiative recombination of electrons and holes. To ensure good supply of both, optional electron- and hole-transport (ETL, HTL), injection (EIL, HIL) and blocking layers (EBL, HBL) are added and contacted with an opaque highly reflective silver cathode and a transparent indium tin oxide (ITO) anode as shown in Figure 1.

The thicknesses of thin layers are in the range of light wavelengths therefore the light has to be treated coherently, in terms of electromagnetic waves. In thicker layers (e.g. the transparent substrate) the light has to be treated incoherently, in terms of rays.

The overall OLED device efficiency, including optical and electrical performance, can be presented by the external quantum efficiency (*EQE*) [15, 16], which is the ratio between the number of photons reaching the far field as useful light to the number of injected charge carriers:

$$EQE = \gamma \int_{\lambda} s_{\mathrm{el}}(\lambda)\, \eta^{*}_{\mathrm{rad,e}}(\lambda)\, \eta_{\mathrm{out}}(\lambda)\, d\lambda \tag{1}$$

$$\eta^{*}_{\mathrm{rad,e}}(\lambda) = \frac{\eta_{\mathrm{rad,e}} F(\lambda)}{1 - \eta_{\mathrm{rad,e}} + \eta_{\mathrm{rad,e}} F(\lambda)} \tag{2}$$

$$\eta_{\mathrm{out}} = \frac{U(\lambda)}{F(\lambda)} \tag{3}$$

Where $s_{\mathrm{el}}$ is a normalized luminescence spectrum of the emitting material ($\int_{\lambda} s_{\mathrm{el}}(\lambda)\, d\lambda = 1$), $\gamma$ is the electrical efficiency and $\eta^{*}_{\mathrm{rad,e}}$ is the effective radiative efficiency of the emitter. Its definition is given in Eq. (2), in which $\eta_{\mathrm{rad,e}}$ is the intrinsic radiative efficiency of the emitter and $F(\lambda)$ is the total radiated power at the emitter location relative to the power radiated in an infinite homogeneous medium (also called the Purcell factor). Finally $\eta_{\mathrm{out}}$ in Eq. (1) is the outcoupling efficiency that is defined in Eq. (3) as the ratio of the total radiated power outcoupled from the OLED structure to the far field (usually air), $U(\lambda)$, to the total Purcell factor, $F(\lambda)$. Looking back to Eqs. (1)-(3), we can see that the optical properties of *EQE* are fully defined by $U(\lambda)$ and $F(\lambda)$ parameters. An optical model should therefore determine these two parameters ($U(\lambda)$ and $F(\lambda)$), while also provide an insight in optical behavior inside and outside the structure.

### *2.2 Concept of the model*

Our model combines two sub-models: a thin-film optical model with light sources and a ray-tracing model - Figure 2. The thin-film model is based on a transfer matrix model (TMM), in which we incorporate internal light sources, in form of dipoles (as commonly used to describe light generation in organic layers) or in any other arbitrary form of light sources. The ray-tracing model is a 3D model utilized in CROWM simulator [17]. The ray-tracing model of the simulator was upgraded with TMM to be able to include thin-layer stacks also outside the OLED device (e.g. on the front side of the device, in general). The TMM approach requires that the thin layers are locally flat and plane parallel. Applied textures with micrometer dimensions (dimensions larger than light wavelengths of interest) still fulfill this condition, thus our model enables us to include micro textures either on the surface or at internal interfaces of OLED structures (see Figure 2). In the following sections, we present the main properties of the developed simulation model with governing equations and main specifics.

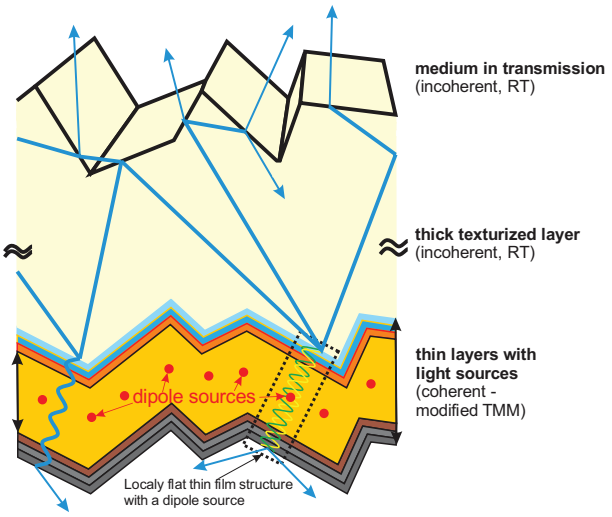


**Figure 2:** Combined OLED model, combining thin film layers containing dipole sources (locally flat TMM model) with thick incoherent layers (CROWM).

### *2.3 TMM with internal light sources*

Organic layers and the thin film contacts in the OLED structure are stacks of locally flat plane parallel coherent layers. To describe the light behavior in these stacks without particular light sources at the first stage, TMM presents an efficient solution for the calculation of the optical properties inside and outside the stack. Most commonly, TMM is used for modelling of thin-film optical devices with an external light source (e.g. an illuminated flat solar cell), while in the OLEDs, the light is generated inside the thin-film structure. Therefore, to incorporate such an internal light source, we modified the TMM formulation to properly describe the light generation and propagation in a thin layer stack. A similar approach has been presented in [18].

Following the TMM formalism from [19], a plane wave propagating obliquely through the thin-film stack under some angle $\vartheta_i$ can first be separated according to its polarization – we differentiate between the transverse-electric (TE) and the transverse-magnetic (TM) polarizations, based on the plane of incidence and the orientation of the electric and magnetic fields. Next, for each of the two polarizations, the waves are further distributed into two components: the transverse plane wave component that is travelling perpendicularly to the flat interfaces through the stack, and the component that is travelling in parallel along the interfaces. TMM formalism treats only the transverse components which interact (interfere) constructively or destructively with each other, while information about the full wave is contained in the propagating angle. The electric field that belongs to the transverse wave component of emission source (incident light or internal source) is calculated separately for the TE and TM polarization for emission as:

$$E_{\mathrm{emi}}^{\mathrm{T,TE}} = E^{\mathrm{TE}} \quad E_{\mathrm{emi}}^{\mathrm{T,TM}} = E^{\mathrm{TM}} \cos\vartheta_{\mathrm{emi}} \tag{4}$$

where $\vartheta_{\mathrm{emi}}$ is the incident angle of the total electric field incident on interfaces. In the following formulation, all the electric fields in the equations are considered to be the electric fields that belong to the transverse wave component, as denoted by the superscript T, and can originate from either the TE or the TM polarization, thus all further presented formulations need to be considered separately for TE and TM polarizations as specified in TMM formulations [19].

A thin-film layer structure, that is described by the layer thicknesses and by the corresponding complex refractive indices of the individual layers, can be defined by a TMM formalism using the product of propagation matrices *P* (propagation through layer) and matching matrices *M* (reflection and transmission at the interface) [19]. The matching matrices (*M*) are obtained by Fresnel's transverse reflection ($r_j^{\mathrm{T}}$) and transverse transmission ($t_j^{\mathrm{T}}$) coefficients (separately for TE and TM) at *j*-th interface as:

$$\begin{bmatrix} E_{\mathrm{j,l}}^{\mathrm{T}+} \\ E_{\mathrm{j,l}}^{\mathrm{T}-} \end{bmatrix} = \frac{1}{t_{\mathrm{j}}^{\mathrm{T}}} \begin{bmatrix} 1 & r_{\mathrm{j}}^{\mathrm{T}} \\ r_{\mathrm{j}}^{\mathrm{T}} & 1 \end{bmatrix} \cdot \begin{bmatrix} E_{\mathrm{j,r}}^{\mathrm{T}+} \\ E_{\mathrm{j,r}}^{\mathrm{T}-} \end{bmatrix} = \left[ M_{\mathrm{j}} \right] \cdot \begin{bmatrix} E_{\mathrm{j,r}}^{\mathrm{T}+} \\ E_{\mathrm{j,r}}^{\mathrm{T}-} \end{bmatrix} \tag{5}$$

where $E_{\mathrm{j,l}}^{\mathrm{T}\pm}$ and $E_{\mathrm{j,r}}^{\mathrm{T}\pm}$ are electric fields on the left and right side of the *j*-th interface, respectively, propagating in the positive (+) or the negative (–) direction.

Propagation matrices (*P*) are obtained by propagating the above fields through the *k*-th layer as:

$$\begin{bmatrix} E_{\mathrm{k,l}}^{\mathrm{T}+} \\ E_{\mathrm{k,l}}^{\mathrm{T}-} \end{bmatrix} = \begin{bmatrix} e^{j\delta_{\mathrm{k}}} & 0 \\ 0 & e^{-j\delta_{\mathrm{k}}} \end{bmatrix} \cdot \begin{bmatrix} E_{\mathrm{k,r}}^{\mathrm{T}+} \\ E_{\mathrm{k,r}}^{\mathrm{T}-} \end{bmatrix} = \left[P_{\mathrm{k}}\right] \cdot \begin{bmatrix} E_{\mathrm{k,r}}^{\mathrm{T}+} \\ E_{\mathrm{k,r}}^{\mathrm{T}-} \end{bmatrix} \tag{6}$$

Where $\delta_{\mathrm{k}}$ contains the information about the phase change and the absorption inside the layer, via the layer thickness and the complex refractive index of the layer material. A more detailed explanation and derivation of *P* and *M* matrices can be found in [19].

In the case of devices with internal sources (e.g. OLEDs), the initial electric field (presenting the emission source) is generated inside the thin film structure, namely inside a specified layer. We assume the sources are located on a plane parallel to the interfaces. More detailed emission source definition for OLED sources (dipoles) is presented in the next subchapter. To incorporate the initial electric field of the source, we put a new virtual interface parallel to the existing interfaces inside the specified layer (*m*) at an arbitrary position. The position of this virtual interface is defined by the spatial position parameter *p* as shown in eq. (7). The interface splits the original (*m*-th) layer into two layers with their thicknesses defined by *p* parameter (0 < *p* < 1) as:

$$d_{\mathrm{v,l}} = d_{\mathrm{m}} * p \; d_{\mathrm{v,r}} = d_{\mathrm{m}} * \left(1 - p\right) \tag{7}$$

Where $d_{\mathrm{v,l}}$ and $d_{\mathrm{v,r}}$ are the thicknesses of the left and the right part of the *m*-th layer after the splitting, respectively.

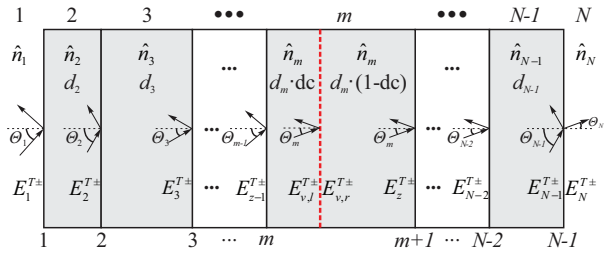


**Figure 3:** Schematic representation of a thin-film multilayer stack with an additional virtual interface incorporating an internal source in arbitrary layer *m*.

New electric fields (equation (4)) are introduced at the new virtual interface "*v*", their values are defined by particular emitting sources. This initial source waves are propagating away of the interface, therefore we have on the left side of the interface a source wave in negative direction ($E_{\mathrm{emi}}^{\mathrm{T}-}$) and on the right side in positive direction ($E_{\mathrm{emi}}^{\mathrm{T}+}$). Considering that the virtual interface is placed within the layer we can write the following relations:

$$E_{\mathrm{v,r}}^{\mathrm{T}+} = E_{\mathrm{v,l}}^{\mathrm{T}+} + E_{\mathrm{emi}}^{\mathrm{T}+} \; E_{\mathrm{v,l}}^{\mathrm{T}-} = E_{\mathrm{v,r}}^{\mathrm{T}-} + E_{\mathrm{emi}}^{\mathrm{T}-} \tag{8}$$

To describe these new conditions at the virtual interface, we split the entire optical system into two parts, the first part describing the thin film environment on the left of the virtual interface, and second on the right. The thin film stack on the left of the virtual interface can thus be described as:

$$\begin{bmatrix} E_1^{\mathrm{T}+} \\ E_1^{\mathrm{T}-} \end{bmatrix} = \begin{bmatrix} 0 \\ E_1^{\mathrm{T}-} \end{bmatrix} = \left[M_1\right] \cdot \left[P_2\right] \left[M_2\right] \cdot \ldots \cdot \left[M_{\mathrm{m-1}}\right] \cdot \left[P_{\mathrm{m}}^{*}\right] \cdot \begin{bmatrix} E_{\mathrm{v,l}}^{\mathrm{T}+} \\ E_{\mathrm{v,l}}^{\mathrm{T}-} \end{bmatrix} = \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix} \cdot \begin{bmatrix} E_{\mathrm{v,r}}^{\mathrm{T}+} \\ E_{\mathrm{v,r}}^{\mathrm{T}-} \end{bmatrix} \tag{9}$$

and on the right of the virtual interface as:

$$\begin{bmatrix} E_{\mathrm{v,r}}^{\mathrm{T}+} \\ E_{\mathrm{v,r}}^{\mathrm{T}-} \end{bmatrix} = \left[P_{\mathrm{m}}^{**}\right] \cdot \left[M_{\mathrm{m}}\right] \left[P_{\mathrm{m+1}}\right] \cdot \ldots \cdot \left[P_{\mathrm{N-1}}\right] \cdot \left[M_{\mathrm{N-1}}\right] \begin{bmatrix} E_{\mathrm{N}}^{\mathrm{T}+} \\ E_{\mathrm{N}}^{\mathrm{T}-} \end{bmatrix} = \begin{bmatrix} F_{11} & F_{12} \\ F_{21} & F_{22} \end{bmatrix} \cdot \begin{bmatrix} E_{\mathrm{N}}^{\mathrm{T}+} \\ 0 \end{bmatrix} \tag{10}$$

where $P_{\mathrm{m}}^{*}$ and $P_{\mathrm{m}}^{**}$ – are modified propagation matrices due to the change of thicknesses due to introducing a new virtual interface. Additionally, as the source is inside the thin film structure and no incident light from the outside is considered, the transversal electric fields representing the incoming light from the outside of the thin film structure ($E_1^{\mathrm{T}+}$ and $E_{\mathrm{N}}^{\mathrm{T}-}$) are set to 0.

Using equations (8), (9) and (10), it is straightforward to calculate the new conditions ($E_{\mathrm{v,l(r)}}^{\mathrm{T}\pm}$) at the virtual interface due to the introduced emission source ($E_{\mathrm{emi}}^{\mathrm{T}\pm}$) in the entire thin film system. Here we present the final results for superimposed fields at the position of the virtual interface only (either for TE or TM polarisation):

$$\begin{aligned} E_{\mathrm{v,r}}^{\mathrm{T}+} &= \frac{F_{11}}{B_{11} \cdot F_{11} + B_{12} \cdot F_{21}} * \left(B_{11} \cdot E_{\mathrm{emi}}^{\mathrm{T}+} - B_{12} \cdot E_{\mathrm{emi}}^{\mathrm{T}-}\right) \\ E_{\mathrm{v,r}}^{\mathrm{T}-} &= \frac{-B_{12} \cdot F_{21}}{B_{11} \cdot F_{11} + B_{12} \cdot F_{21}} * \left(E_{\mathrm{emi}}^{\mathrm{T}-} + E_{\mathrm{emi}}^{\mathrm{T}+}\right) \end{aligned} \tag{11}$$

It is worth noting that due to dipole emission symmetry $E_{\mathrm{emi}}^{\mathrm{T}+} = E_{\mathrm{emi}}^{\mathrm{T}-}$, the presented formulations are nevertheless applicable also to non-symmetric sources.

Once we determine the fields at the virtual interface, that represent source fields $E_{\mathrm{v,l(r)}}^{\mathrm{T}\pm}$, the electric fields at all other interfaces can be easily calculated using the standard TMM formulations [19]. In the final step we calculate the total $E^{\mathrm{T}}$ and $H^{\mathrm{T}}$ fields at each interface as:

$$\begin{bmatrix} E_{\mathrm{i}}^{\mathrm{T}} \\ H_{\mathrm{i}}^{\mathrm{T}} \end{bmatrix} = \begin{bmatrix} E_{\mathrm{i,t}}^{\mathrm{T}+} + E_{\mathrm{i,t}}^{\mathrm{T}-} \\ \frac{1}{\eta_{\mathrm{i}}} \left(E_{\mathrm{i,t}}^{\mathrm{T}+} - E_{\mathrm{i,t}}^{\mathrm{T}-}\right) \end{bmatrix} \tag{12}$$

where $\eta_{\mathrm{i}}$ is the material impedance connecting $E^{\mathrm{T}}$ and $H^{\mathrm{T}}$ field in the specific material. As $E_{\mathrm{v,l(r)}}^{\mathrm{T}\pm}$ are modified by

forward and backward matrices (optical environment), all the results will be relative, to the modified source expressed with the conditions at the virtual layer (not to the original input emission source). Using $E^T$ and $H^T$ fields, we simply calculate the total power densities of the wave entering the *i*-th layer by using the Poynting vector as:

$$P_i = \frac{1}{2} Re\left(E_i^T \times H_i^{T*}\right) / \cos\left(\vartheta_i\right) \quad (13)$$

Here, $\cos(\vartheta_i)$ is added to the classic Poynting vector formulation to obtain the power of the complete wave propagating under an oblique angle $\vartheta_i$ through the *i*-th layer. Finally, due to the modified source, expressed with the conditions at the virtual interface, all power densities must be normalized with respect to the total power density that exist on both sides of the virtual interface and corresponds to the total emission power of the source ($P_{emi,tot}$). By knowing the relative power entering each layer we can simply calculate the relative absorption ($A_i$) in each layer. And finally, the relative power of the light that exits the thin film stack at the left and the right side of the stack correspond to $P_1$ and $P_N$, respectively.

### *2.4 Definition of internal light sources*

In the case of OLEDs, the electroluminescent emission is considered as a dipole transition from an excited molecular state to the ground state [20]. The sizes of the emitting sources in OLEDs do not exceed a few nanometers, being very small with respect to the wavelength, thus they can be approximated by point dipoles [20]. Point dipole emitters are in the model simulated as a classical, continuously oscillating dipole sources with predefined spectrum and angular intensity distribution (AID). The AID of a dipole in infinite medium is presented in Figure 4. The 3D AID and the two cross-sections with the corresponding angular functions are presented for the vertically oriented dipole (see black arrow). From here on the dipole orientation (vertical, horizontal) is referred to with respect to the interface planes of the structure. If the dipole is rotated, its AID rotates accordingly. Once it is put inside a thin-film multilayer structure, interference effects with reflected waves have to be considered (included in TMM).

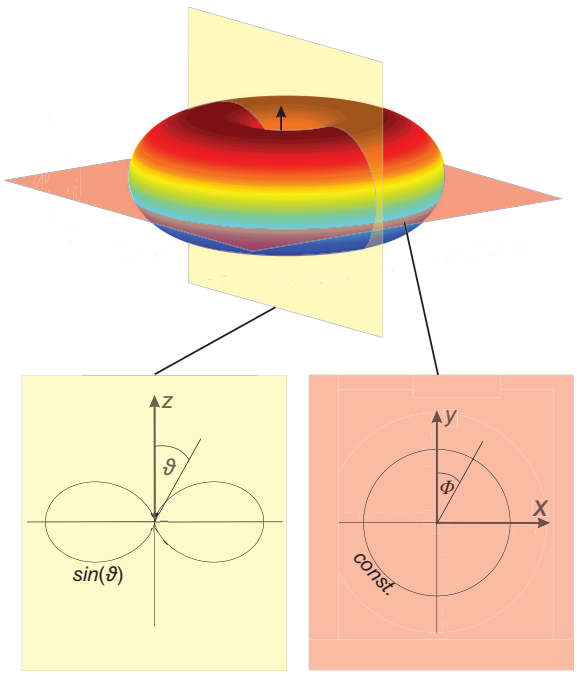


**Figure 4:** Vertically (according to the *xy* plane) oriented dipole in homogeneous space, with cross-sectional projections showing polar ($\theta$) and azimuth ($\Phi$) angles.

As dipoles emit light as spherical waves, which is not very useful in TMM formulations, their emission is converted through Fourier decomposition into plane waves travelling under specified angles. These angles may be real or imaginary valued, according to Fourier decomposition [20]. The imaginary components represent evanescent waves, which are also taken into account in the TMM.

Emitting sources (dipoles) are considered to be isotropically orientated in the plane of the layered system, thus only orientation with respect to the layered system normal has to be considered. Any arbitrary oriented dipole is decomposed into three orthogonal dipoles in the model, two parallel (horizontal) and one perpendicular (vertical) dipole, defined by their orientation to the interfaces of the planar system and the corresponding emission polarization. Special care has to be taken when defining the TE and TM components of the planar waves approaching the interfaces at different incident angles. While the magnetic field is always perpendicular to the dipole orientation, the electric field lies in the plane which is defined by dipole orientation and the direction of wave propagation. Another condition is that magnetic field, electric field and the propagation direction are perpendicular to each other. Based on these rules TE and TM components can be defined in the model.

In the OLED, the emitting layer is combined from multiple randomly oriented dipoles that can in general have some preferential orientation to the layered system normal, this can be a consequence of material properties or deposition methods (e.g. sputtering, spin coating). This preferential orientation of dipoles can be incorporated in anisotropy coefficient *a*, as a ratio between the number of vertical dipoles to the number of all dipoles. In the case of random orientation of dipoles,

$a$ = 1/3, meaning that contributions from all three orthogonal dipoles (two horizontal and one vertical as defined above) are considered equally. Incorporating anisotropy reduces the highly complex problem of describing detailed dipole orientation to a rather simple problem of defining the fraction of parallel and perpendicular dipole moments [20].

For complete optical description of emission source (dipole), TTM approach described in previous subchapter needs to be applied for all discretized Fourier plane waves defining the (dipole) source. The ratio of total emitted power in layered system and total emitted power of the same source in an infinitive medium is the Purcell factor for a given wavelength, $F(\lambda)$, and is our first important optical parameter that can be defined by simulation.

### *2.5 Combining TMM model with the ray tracing simulator CROWM*

A simple flat structure with a single thick layer can be easily simulated using an expanded TMM formulation that also considers incoherent light propagation through the thick flat layer [21]. However, a problem occurs when we introduce more complicated structures, e.g. such as structures with textured surfaces of the thick layer or with additional thin layers on top of the substrate. To overcome this problem, we combined our TMM model with the optical simulator CROWM [17] that enables complete optical simulation of advanced structures including thin and thick layers with or without textures. This way, it is possible to simulate arbitrary complex LED devices with flat or micro-textured substrates as well as with additional thin-film stacks incorporated in the device, such as antireflection layers etc. The simulation initiates by calculating the output of the developed TMM model with internal sources (relative powers $P_1$ and $P_N$, their angles of propagation and TE/TM decomposition), which are then taken as the input into the general CROWM simulation (combination of ray tracing and classical TMM). While the polar angles ($\vartheta$) are defined with TMM formulations, the azimuth angles ($\Phi$) are, due to assumed $z$-axis symmetry and under the assumption of isotropically oriented dipoles in a planar layer, equally distributed over possible discrete values (0-360°). Each discrete part is then considered as a ray (separately for TE and TM) and traced through the rest of the structure until it is either extracted to air or reabsorbed in the structure. Additionally, since sources are considered as point sources in a locally flat structure, a large number of sources distributed across the entire area of the device (see Figure 2) are considered, and the final result is an average of all the contributions, ensuring realistic representation of the real device.

### *2.6 Model limitation and advantages*

The thin-film model with emission sources is considered locally flat and anisotropic in parallel planes, which is true for most OLEDs. The emitting organic layer is considered to be non-absorbing as absorption can suppress spontaneous emission from radiating dipoles [22]. As absorption of emissive layers (at emissive wavelengths) is considerably small it can be neglected without affecting accuracy [15].

Multiple emitting layers (interfaces) with independent anisotropy, independent emission locations, independent emission spectrum and independent distribution in emissive layer(s) can be simulated, this being very suitable for white (multi-color) devices. In many models [18, 23] only transmission to the exit medium (usually air) and total relative emission (Purcell factor) are presented, while in our model absorption of each individual layer can also be extracted. Due to the use of ray tracing in combination with TMM, multiple thick layers with thin-film stacks and various micro textures can be included in the simulations.

Another important advantage of our model is the possibility of simulating with restricted geometry in lateral dimensions. An entire device with independently limited emission and limited texture area can be simulated. This is very useful especially in research, where smaller samples are usually produced with limited emission area and limited texture area, see Figure 5 where only small pixel area is active and emits light while the texture is produced only above this pixel area. This can have immense effect on final results, thus limited area simulations are very beneficial for modeling realistic devices.

## *3 Experimental validation of the combined model*

In this contribution, we present an experimental validation of the combined model on red bottom emitting p-i-n OLEDs (produced at TU Dresden) with flat and sine textured substrate / air interface. OLED structure with layer thicknesses is presented in Figure 1, while final device with visible laser structured sine texture can be seen in Figure 2. Sine textures were produced using laser structuring of the glass substrate – see Figure 5. Final textures are simple 1D sine textures with constant period $P$ = 175 µm and three different heights $h$ (2.5 µm, 6.5 µm and 15 µm). OLED production details can be found in [16, 24].

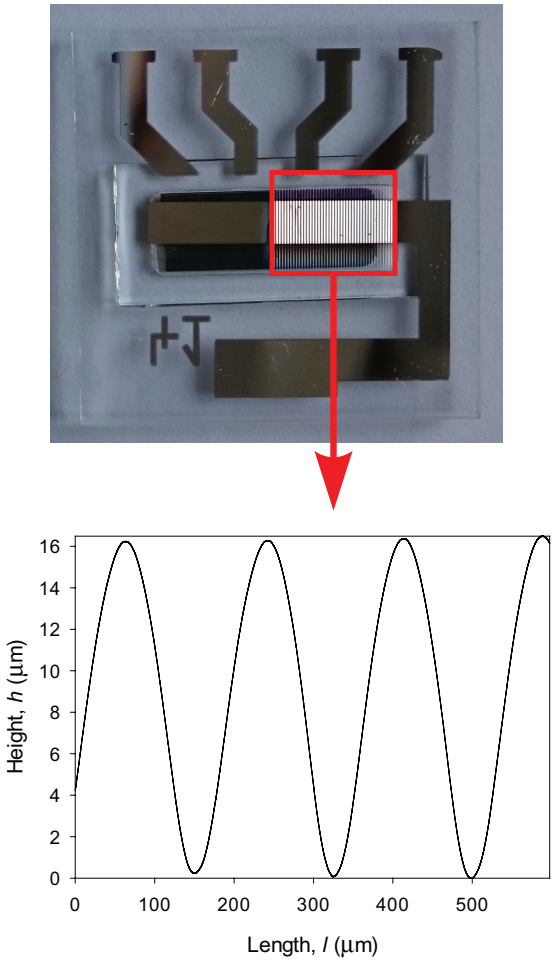


**Figure 5:** A produced bottom-emitting red OLED (four dots as indicated by the contacts) with sine textures on glass / air interface. Red rectangle indicates limited textured area of approx. 7x9 mm$^2$. Additionally, profilometer measurements of the sine textures for selected example is also shown.

Emitter material properties ( $\gamma$= 0.92, $\eta_{rad,e}$ = 0.87, anisotropy $a$ = 0.256, $s_{el}$ – emission spectrum, emission positon) are taken from a previously published data [15] or gained from internal sources and were experimentally confirmed. The emission position was set at a single position in the emission layer with $p$ = 1, the emission is still considered to be in emission layer, but infinitively close to the HBL (see Figure 1). Optical properties, in particular layer thicknesses and material refractive indices were supplied by TU Dresden and are within the anticipated error range.

Here we present comparison between simulations and experimental results for the total radiant intensity, *EQE* and AID which are important performance parameters of OLEDs. Comparison between simulations and experiment for total radiant intensity for flat and textured (sine textures with $P$ = 175 µm and $h$ = 15 µm) devices can be seen in Figure 6. Good matching between simulations and experiment can be observed, especially for the flat device. Some deviations are due to limited texture size in the experimental device (see Figure 5), as in simulations we simulated textured area as infinitive (this is justified for actual lightning applications since the emission and texture area are both large enough, more than 10x10 cm$^2$).

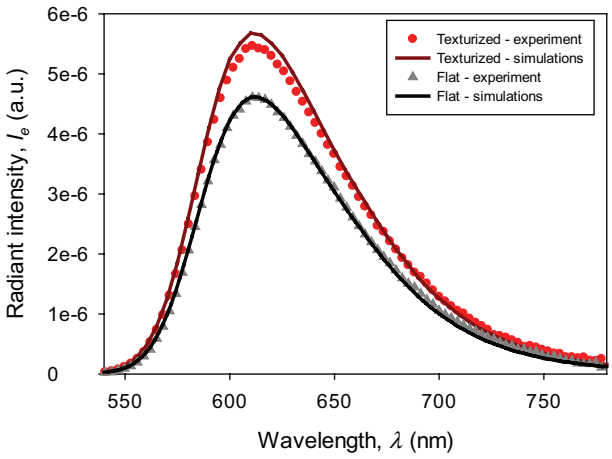


**Figure 6:** Comparison of total radiant intensity of a flat device and textured (sine textures with $P$ = 175 µm and $h$ = 15 µm) device for measurements and simulations.

We also compare measured and simulated *EQE*. The *EQE* was gained from AID measurements assuming rotation symmetry as:

$$EQE\left(I_c\right)=\frac{2\pi e}{I_c hc}\iint_{\vartheta\lambda}\lambda I_e\left(\vartheta,\lambda\right)\sin\vartheta d\vartheta d\lambda \qquad (14)$$

Where $I_e$ is radiand intensity, $I_c$ is applied current, $e$ is elementary charge, $c$ is the speed of light in vacuum, $h$ is Planck constant and $\vartheta$ is a polar angle.

The *EQE* was calculated and simulated for a flat and a texturized OLED. The *EQE* of a flat OLED was taken as a reference and the gain ($G$) when using textures was defined as:

$$G=\frac{EQE_{\text{texturized}}-EQE_{\text{flat}}}{EQE_{\text{flat}}}*100\% \qquad (15)$$

We present here simulation and experimental results for 3 texturized OLED devices, with different sine aspect ratios ($AR$ = $h$/$P$) of the textures. The results are presented in Table 1. Good matching was found again, minor deviations are due to limited texture size in experimental device (see Figure 5).

**Table 1:** Gain (*G*) comparison between experimental and simulation results for different *AR* of the sine textures.

| Aspect ratio – *AR* (*h* (µm) / *P* (µm)) | *G* (%) - experiment | *G* (%) - simulations |
|---|---|---|
| 0 (0 / -) | 0 | **0** |
| 0.0143 (2.5 / 175) | 7.0 | **9.0** |
| 0.0371 (6.5 / 175) | 11.2 | **12.5** |
| 0.0857 (15 / 175) | 19.7 | **20.6** |

Another important parameter in OLEDs is the AID. We compare the simulated AID for flat and textured devices. Results for OLED with flat and texturized device (sine textures $P$ = 175 µm, $h$ = 15 µm) can be seen in Figure 7. Here we present an AID at emission peak wavelength of 610 nm. Comparing normalized simulated and experimental AID data from 0° to 60 °, deviations up to 2 % and up to 3 % can be found at individual angles for the flat and the textured device, respectively. While for angles over 60 ° where limited texture size (as light travelling under high angles in substrate does not fall on the textured surface entirely) starts to influence the measurement results, thus the difference rises up to 7 % and 15 % for flat and textured device, respectively. Only small deviations between simulation and experimental AID is identified and very good matching for flat and textured device can be observed.

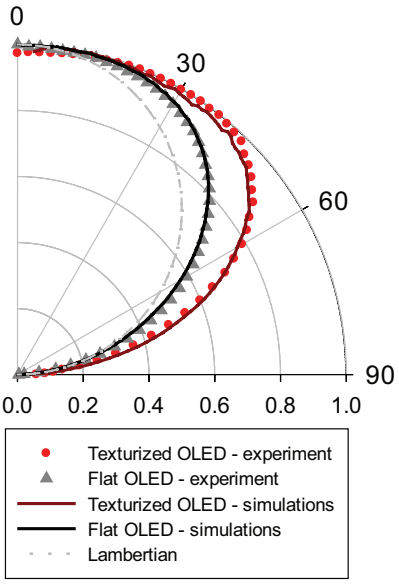


**Figure 7**: Angular intensity distribution (AID) comparison for flat and device with textured interface (sine textures on interface substrate/air with $P$ = 175 µm and $h$ = 15 µm) vs. simulation results for corresponding structures. Additionally, ideal Lambertian distribution is added.

## 4 Conclusions

A new combined optical model, based on TMM and ray-tracing approaches has been developed. Detailed modification of TMM to incorporate internal dipole sources was presented. TMM model with internal sources was combined with ray tracing simulator CROWM, to incorporate simulations of thick texturized layers. Dipoles as emission sources in OLEDs were applied to TMM formulations. OLEDs optical performance parameters - outcoupling efficiency and Purcell factor were gained using developed optical model and used in further calculations where good matching with experimental results was obtained. Additionally, simulated angular intensity distribution showed excellent matching with experimental results. The mismatch for angles up to 60° was under 3 %, for both flat and textured devices. In the final part, validation of the developed model was presented by comparison of simulated results with experimental ones. Good matching was obtained for red bottom-emitting p-i-n OLED devices on glass with flat and micro-textured front surface. Developed optical model accurately predicts optical behavior of flat and textured OLEDs and is appropriate for further simulations of advanced OLED devices. OLEDs with 1D front surface sine textures (textures were made by simple laser structuring of glass) outperform the flat counterpart in all performance parameters.

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# *Najvišja priznanja v slovenski znanosti v letu 2016*

Odbor za nagrade, ki mu predseduje prof. dr. Tamara Lah Turnšek, je 21.11.2016 v Cankarjevem domu v Ljubljani podelil najvišja priznanja za dosežke na znanstveno raziskovalnem področju. Slavnostni govornik na prireditvi je bil predsednik državnega zbora dr. Milan Brglez. Zoisovo nagrado za življenjsko delo sta prejela akad. prof. dr. Uroš Skalerič in akad. prof. dr. Branko Stanovnik, Priznanje ambasador znanosti Republike Slovenije so prejeli prof. dr. Sara Dolničar, prof. dr. Gregor Cevc in prof. dr. Igor Gregorič, Zoisove nagrade za vrhunske dosežke so šle v roke prof. dr. Janku Prunku in prof. dr. Božidarju Šarlerju. Podeljenih je bilo tudi pet Zoisovih priznanj in eno Puhovo priznanje.

Med letošnjimi dobitniki petih Zoisovih priznanj za pomembne dosežke na posameznih področjih je tudi dolgoletni član društva MIDEM **prof. dr. Janez Krč** s Fakultete za elektrotehniko Univerze v Ljubljani, ki je prejel ***Zoisovo priznanje za pomembne dosežke v fotovoltaiki in optoelektroniki***. Pri načrtovanju sodobnih optoelektronskih gradnikov predstavlja numerično modeliranje ključno orodje tako za optimizacijo obstoječih struktur kot tudi za razvoj novih. Prof. dr. Krč je razvil enodimenzionalni optični model za simulacijo tankoplastnih optoelektronskih struktur z nanohrapavimi spoji, kar je omogočilo podrobno analizo in izboljšanje učinkovitosti pretvorbe sončnih celic. Prof. dr. Krč je odigral odločilno vlogo tudi pri razvoju ostalih optičnih modelov in simulatorjev v Laboratoriju za fotovoltaiko in optoelektroniko. Mednje sodi tudi koncept sklopljenega modeliranja, ki omogoča simulacije najsodobnejših optoelektronskih gradnikov z nano- in mikrofotonskimi strukturami. Izbrane pristope modeliranja tankoplastnih fotonapetostnih gradnikov

prof. dr. janez Krč (Arhiv MIZŠ. Foto: STA / Tamino Petelinšek )

je kot prvi avtor objavil v znanstveni monografiji pri mednarodni založbi CRC Press. Licence razvitih simulatorjev uporabljajo v priznanih raziskovalnih organizacijah, med njimi sta Ecole polytechnique federal de Lausanne v Švici in Helmholtz-Zentrum Berlin v Nemčiji, ter v uglednih podjetjih v Evropi, ZDA in Aziji.

Iskrene čestitke vsem prejemnikom nagrad in priznanj, še posebej pa dolgoletnemu članu našega društva prof. dr. Janezu Krču!

Prof. dr. Marko Topič
Predsednik društva MIDEM

Nagrajenci s predsednico Odbora za nagrade, prof. dr. Tamaro Lah Turnšek, ministrico za izobraževanje, znanost in šport, prof. dr. Majo Makovec Brenčič in predsednikom državnega zbora dr. Milanom Brglezom (v sredini). (Arhiv MIZŠ. Foto: STA / Tamino Petelinšek)

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