Expanding the power pulse duration range for electroporation

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Abstract. *A universal power pulse generator in terms of power pulse duration would improve the capability of exploration of the phenomena of electroporation. This paper is focused on finding a method for expanding the range of the pulse duration of the power pulse generators considering the power of the pulse. A power pulse generator with an unlimited maximum pulse duration is designed according to the results of the research and tested. The pulse amplitude can be adjusted from 0 V to 500 V. An 80 ns 500 V pulse with rise and fall times of 6 ns is generated with a SiC power device.*

1 Introduction

Despite the wide and promising area of usage of electroporation in food industry as well as in medicine for cancer treatment the phenomena of electroporation has still not been entirely explored [1]. In order to generate credible and comparable analysis on the permeabilization effect of different electroporation pulse properties on the biological cells a continuously adjustable power pulse forming device is necessary. The pulse range of the power pulse generating devices is limited [2]. Power switch based pulse generators introduce a wide and continuously adjustable pulse duration range but are limited with the switching speed. Lower pulse durations can though be achieved with pulse forming network based pulse generators which are by their operation principle limited to a single pulse length or are sensitive to load resistance [3]. Unique tuning of the pulse forming networks prevents a much needed continuous setting of the pulse properties. Moreover, the number of devices needed for a complete overview of the permeabilization process with respect to the pulse parameters, namely pulse duration, pulse amplitude and pulse current is blocking the research in the field of electroporation. Any step further in increasing the range of the pulse parameters of a single pulse generator is a step forward to understanding the phenomena of the electroporation and further development of electroporation based technologies and treatments [4].

It is obvious that pulse forming networks cannot present a basis for expanding the pulse duration range of an electroporator device, therefore this research is grounded on pulse generators based on power devices. The generation of longer power pulses with the power devices is not exceptionally challenging, therefore this study is focused on the generation of short power pulses.

2 Methods and materials

Despite GaN (gallium nitride) based power devices being the leading semiconductor technology for the fast switching applications the SiC (silicon carbide) based power devices achieve higher voltage carrying capabilities due to their physical structure [5]. The opposing positioning of the source and drain in the SiC power cells with respect to the substrate results in a higher breakdown voltage in comparison to GaN cells which have the drain and source on the same side of the substrate and very close to one another. Currently the maximum drain-source voltage v_{ds} of the GaN based power devices reaches 650 V while the maximum drain-source voltage v_{ds} of SiC based power devices reaches up to 1700 V. A serial connection of power devices *PS* (Power Switch) is quite challenging and is so far limited with the count number of the serially connected power devices PS. Consequently, the SiC devices present the future for the high voltage, high current applications such as electroporation. Accordingly, this study is focused in increasing the switching speed of SiC MOSFETs.

Additionally, it is known that the cells of the power devices have a much better switching performance than being achieved [6]. The driving of the power switches does not extract the optimal performance out of the power cells. As the driving circuit contributes greatly to the power switch performance emphasis is put on the choice of the driving circuit topology and its design.

2.1 Pulse generator topology

An overview of the driving circuit topologies for controlling power switches is performed. The NZID (Near Zero Interlock Delay) driving principle [6, 7, 8] topology (Figure 1) is chosen as the most suitable for a high frequency high power design.

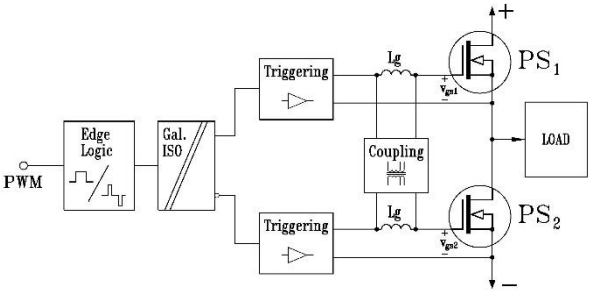

Figure 1. NZID driving circuit topology (Edge logic generates trigger pulses at every PWM change – Synchronized galvanic isolation ensures a synchronic transfer of the trigger pulses to the triggering circuit– Triggering circuit with powering generates triggering voltage ranged between the V_{on} and V_{off} – Inductor in a function of a ramp generating circuit forms the slope of the v_{GS}, enables the return of the excess energy and generates an over-sway) – Coupling transformer ensures the mirroring of both gate source driving signals v_{gs1} and v_{gs2} of the power switches PS_1 and PS_2 respectively.

Aforementioned topology excludes the pre-set dead time t_{DT}. With no pre-set dead time t_{DT} a faster control and a faster responsiveness of the power switches are achievable. The level of freedom of the timing of the actual switch execution is narrowed due to the low propagation delays and low propagation delay differences. As a result of a more precise timing of the actual switch execution the minimum on- or off- time is shorter, wherein the on-time presents the pulse duration.

Additionally, this topology offers a high driving current which helps to overcome the large capacitive currents caused by the combination of the Miller capacitance and fast drain-source voltage v_{ds} transients. Classical driver configurations use a gate resistor, therefore in order to overcome the Miller effect in said topologies the gate source voltage would have had to be overdriven for a short moment at every turn-on and turn-off and then reduced to a normal value to avoid the destruction of the power device. In contrary to the classical driving through a resistor the NZID topology provides an additional acceleration of the gate-source voltage transient due to a quasi-resonant driving through an inductor.

It is the only available topology to ensure simultaneity of the gate-source voltages v_{gs1} and v_{gs2} due to the coupling of the gate-source voltages v_{gs} and low inductivity connections as an additional but obligatory condition for either parallel or serial connection of the power devices PS. In comparison to classical driving the NZID driving offers very low propagation delay and therefore also low propagation delay differences.

The NZID topology enables a continuous operation, maximum pulse duration is limited with the power supply and cooling body.

2.2 The increase of the switching speed

There are quite a few factors that affect the speed of a single switch execution. A high driving current is needed to overcome the large capacitive currents and to speed up the switching process. Accordingly, in function of the trigger switches Q_1 and Q_2 (Figure 2) a complementary pair enhancement mode MOSFET, namely ZXMC3AMCTA by Diodes Incorporated, USA is used. The ZXMC3AMCTA has a very low turn-on delay time, namely 1.7 ns and a very low static drain-source on resistance R_{DSon}, typically 0.1 Ω. Consequently, Q_1 and Q_2 are able to generate a high pulse source current of up to 13 A. The trigger switches Q_1 and Q_2 are only open for the time needed for the gate-source capacitance C_{gs1} or C_{gs2} of the corresponding power device PS_1 or PS_2 to be charged to either a turn-on gate-source voltage level V_{on} or turn-off gate-source voltage level V_{off}, whereas

$$|V_{on} + V_{off}| < \Delta V_{GSmax}. \quad (1)$$

The negative value of the turn-off gate source voltage level V_{off} accelerates the switch-off. The gate-source voltage v_{gs} is additionally increased by the inductance L_g, which is the total inductance between the triggering circuit (Q_1 and Q_2) and the switch cell comprising an added gate inductor, wiring and power device housing. The energy gathered in the L_g during the charging process is released to the input capacitances of the power device, namely C_{gs} and the fluctuating Miller capacitance C_{dg} and is observed as an overshoot of the gate source voltage v_{gs}. The overshoot presents an additional energy to speed up the Miller plateau duration. A damping resistor R_g is used to prevent an uncontrolled behavior of the power device PS. The damping resistor R_g reduces the ringing of the gate-source voltage v_{gs}, which could have caused an uncontrolled switching behavior of the power devices PS.

To prevent the due to the drain-source current changes ΔI_{ds} induced voltages to effect the gate-source voltage v_{gs} a Kelvin source contact of the power device PS is used preferably.

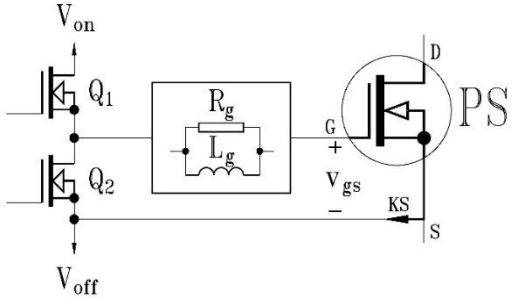

Figure 2. Control of an individual power device

Not just a single switch execution also the repetition frequency of the switch execution is crucial for generation of very short pulses in the range of a few tens of nanoseconds. The shortest PWM pulse is decreased by shortening the interlock delay, as the actual time of the both power devices PS_1 and PS_2 being in the cutoff region. The interlock delay t_{ID} is minimized by eliminating the dead time t_{DT}. Even without any pre-set dead time t_{DT} an actual interlock delay t_{ID} does appear (Figure 3). The transient of the gate-source voltage v_{gs} cannot be instantaneous and additional few nanoseconds are needed for the gate-source voltage v_{gs} to reach the threshold voltage value V_{th}. The value of the interlock delay remains constant and is determined by the turn-on and turn-off voltage values V_{on} and V_{off}. The fine adjustments of the interlock delay t_{ID} are made with the choice of the gate inductor.

Considering equations 1 and 2 the turn-on gate-source voltage level V_{on} is chosen to be 8 V and the turn-off gate-source voltage level V_{off} is - 10 V.

$$V_m = \frac{V_{on}+V_{off}}{2} \quad (2)$$

The SiC devices cannot withstand the constant - 8 V of negative voltage V_{off} needed to prevent the cross conduction. Additional circuit is added to cut the minimal v_{gs} value at maximum negative turn-off voltage V_{offmax} to a safe -4 V for the power device PS being used. Furthermore, to increase the V_{on} to 15 V that are needed to turn the power device on an additional circuit using the energy of the gate-source voltage v_{gs} is implemented into the design.

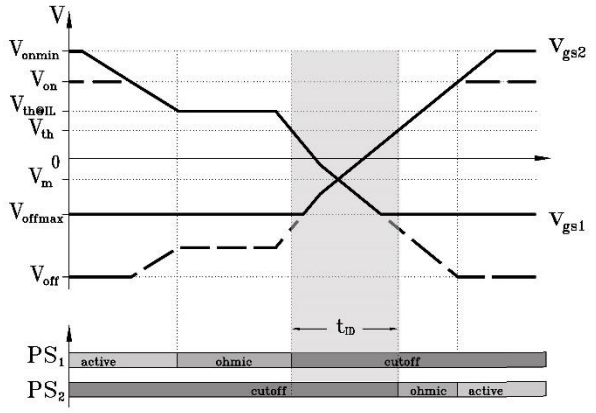

Figure 3. Basic mirrored control voltages marked with a dotted line and actual gate-source voltages including a -4 V clamping and a 5 V increase with a solid line. The stages of the power devices PS and the t_{ID} are marked below.

With such setting of the turn-on and turn-off gate source voltage levels V_{on} and V_{off} the mirroring voltage level V_m is defined to be 3 V below the threshold voltage V_{th}, which is typically 2 V for the power device used. The 3 V difference is enough to compensate the temperature drift of the V_{th}. If an even shorter interlock delay t_{ID} is demanded said temperature drift of the threshold voltage V_{th} is to be detected with a feedback loop. The turn-on and turn-off gate source voltage levels V_{on} and V_{off} are changed within the software accordingly.

An inductance of 15 nH of the gate inductor L_g is used. The interlock delay is set to 5 ns.

Additionally, the power devices PS are limited with a maximum voltage change rate (dv/dt). A serial connection of the power devices PS increases this dv/dt for a factor of the count number of the serially connected power devices PS.

2.3 The increase of the pulse power

Besides to the contribution of decreasing the shortest PWM pulse duration the synchronization of the gate-source voltages v_{gs1} and v_{gs2} presents a basis for increasing the pulse power. Synchronization of the gate source voltages v_{gs} is crucial for either a serial (voltage increase) or parallel (current increase) connection of the power devices or any combination of both. Synchronization is achieved by the choice of the components with a low propagation delay. The propagation delay of the driving circuit is 15 ns. To decrease the already small propagation delay differences a coupling transformer is placed between the gate-source voltages v_{gs}. A high quality coupling is made between gate-source voltage v_{gs1} of the first group of power devices PS_1 and the gate-source voltage v_{gs2} of the second group of the power devices PS_2 with a coupling transformer having a coupling ratio of -1 (Figure 1). The coupling transformer is designed within PCB to have the coupling coefficient near to 1.

The wiring of the coupled v_{gs1} and v_{gs2} needs to have a matching electric properties. The difference in inductance of said wiring would have caused a non-matching propagation delay. Instead of equalizing the length which can still cause a difference in inductance due to different wiring path shape low inductivity connections are used. Minimizing the path inductance results in a lower inductance difference and a lower propagation delay difference. Additionally, the propagation delay is reduced to 1 ns.

The inductivity of the MOSFET housing is summed up to the total inductivity of the entire power loop. Accordingly, besides to the v_{DSmax}, which needs to be as high as possible, the choice of the SiC MOSFET is based on its housing. TOLL housing is used as a housing with the lowest inductivity that is commercially available. Furthermore, the TOLL housing includes a Kelvin source contact. Pre-production samples of 900 V 65mΩ SiC MOSFET, namely C3M0065090J by Wolfspeed USA in TOLL housing are used in the test board. The TOLL housing includes a Kelvin source contact. According to the datasheet [9] this device performs the fastest possible switch in 32 ns ($t_r + t_{d(on)} + t_f + t_{d(off)} = 32\,ns$).

2.4 Test PCB board design

In the high frequency applications parasitic effects of the system become more prominent and have to be considered within the design of the pulse generator (Figure 4).

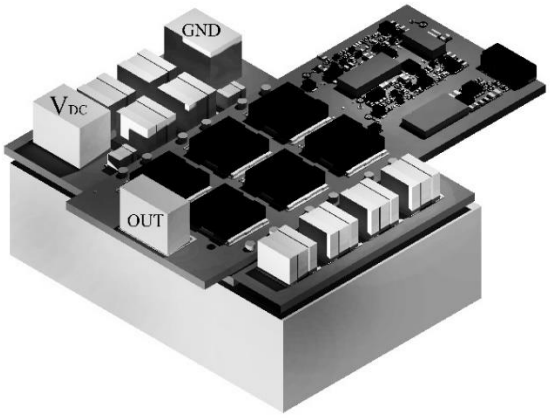

Figure 4. PCB board with marked DC link voltage V_{DC}, GND and output OUT

Therefore, besides to the driver circuit board an additional DC link distribution board (Figure 4) is designed to reduce the alternating magnetic field induced disturbances (Figure 5). To reduce the costs of multilayer board, the DC link distribution board is on a different board. The DC link capacitors mounted are a 500 V 1 µF CeraLink ceramic capacitors by EPCOS, Germany. A cooling body is attached to the board for cooling the power devices in case of longer pulse durations.

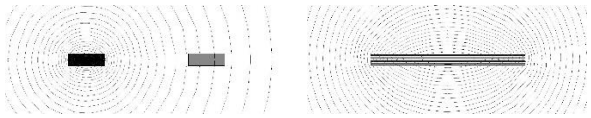

Figure 5. The magnetic field changes due to an alternating current direction induce disturbances of the DC link that are minimized within the improved configuration of the DC link distribution board (right) in comparison to a classical DC link configuration (left). Only one current direction is shown.

3 Results

The pulse generator performance was measured with a calibrated Wavepro 7300A oscilloscope, HVD3206A differential voltage probe and CP031A current probe by LeCroy, USA. The DC link voltage was generated with a Fug HV power supply MCP 350-1250, by Fug, Germany. A resistor of 50 Ω was connected to the output on cables of about 0.5 m length.

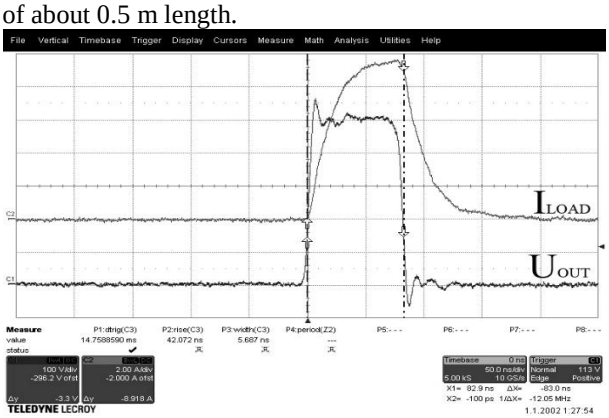

Figure 6. An 80 ns 500 V pulse U_{OUT} generated on the ouput of the test board. Current through a 50 Ω load resistor is demonstrated. (50 ns/div, 100 V/div and 2 A/div)

The PCB board generates an output voltage U_{OUT} pulse of 80 ns duration and 500 V amplitude (Figure 6). Said pulse amplitude is limited by the DC link capacitors to 500 V. The pulse is stable regardless the DC link voltage value. The rise time is 6 ns. A 500 V switch is executed in about 15 ns. A minor overshoot is noticed, which does not reflect on the load current I_{LOAD}. The ringing of the output voltage is dumped with DC link capacitors. The load current I_{LOAD} at 500 V is 10 A. A large inductance of the load loop is noticed on the load current I_{LOAD}. Appearance of this inductance is obvious from the board design. According to the time constant of about 40 ns, this inductance was about 800 nH.

The synchronization of the gate-source voltages v_{gs} of the parallel connected power devices is in the range of 1 ns. No problems with propagation delay of the gate-source voltages v_{gs} were detected. The interlock delay appears stable and is measured to be 5 ns. No cross-conduction through the half bridge is detected.

4 Discussion and Conclusion

Driving the power devices with the NZID (Near Zero Interlock Delay) topology speeds up the switch performance and simultaneously allows a continuous operation. Power device which is declared to perform a switch in 32 ns, is driven to perform a switch in 15 ns. The shape and polarity of the pulses is defined within the microprocessor and is not limited. Despite the NZID driving technology proves to be appropriate for the design of a power pulse generator with wide range of the power pulse properties, the pulse delivery is limited by the inductivity of the load loop, which includes also the cables to the electrodes and the electrodes of the electroporator. Said inductivity limits both the pulse amplitude and the pulse duration on the load and should be minimized in the upcoming designs.

Based on the results of the parallel connected power devices, a serial connection is possible by adding additional windings with coupling ratio 1 to the coupling transformer and should be tested in the future.

5 Acknowledgment

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Literature

[1] J. C. Weaver, K. C. Smith, A. T. Esser, R. S. Son, and T. R. Gowrishankar, “A brief overview of electroporation pulse strength–duration space: A region where additional intracellular effects are expected,” Bioelectrochemistry, vol. 87, pp. 236–243, Oct. 2012

[2] S. Haberl, D. Miklavčič, G. Serša, W. Frey, B. Rubinski: Cell membrane electroporation – Part 2: The applications, IEEE Electr. Insul. M. 29(1): 29-37, 2013

[3] M. Reberšek, M. Kranjc, D. Pavliha, T. Batista Napotnik, D. Vrtačnik, S. Amon, D. Miklavčič: Blumlein configuration for high-repetition-rate pulse generation of variable duration and polarity using synchronized switch control, IEEE T. Biomed. Eng. 56:2642-2648, 2009

[4] D. Miklavčič: Handbook of electroporation; Ljubljana, Slovenia, 2017

[5] A. V. Vertiatchikh, L. F. Eastman, Effect of drain-to-source spacing of AlGaN/GaN transistor on frequency response and breakdown characteristics

[6] A. Zajc, F. Zajc, I. Zajc Zdešar, F. Zajc: NZID (Near Zero Interlock Delay) driving principle, PCIM Europe 2014, 20. - 22. May 2014, Nürnberg, Germany

[7] F. Zajc: A method and apparatus for driving half bridge connected semiconductor power switches with a stable and extremely short interlock delay combined with a switching transition speed increase and a driving power consumption reduction, EP2805418B1, 2014

[8] F. Zajc: Method and apparatus for driving a voltage controlled power switch device, EP2618486B1, 2013

[9] Wolfspeet, Silicon Carbide Power MOSFET, C3M0065090J datasheet, Revised June 2019