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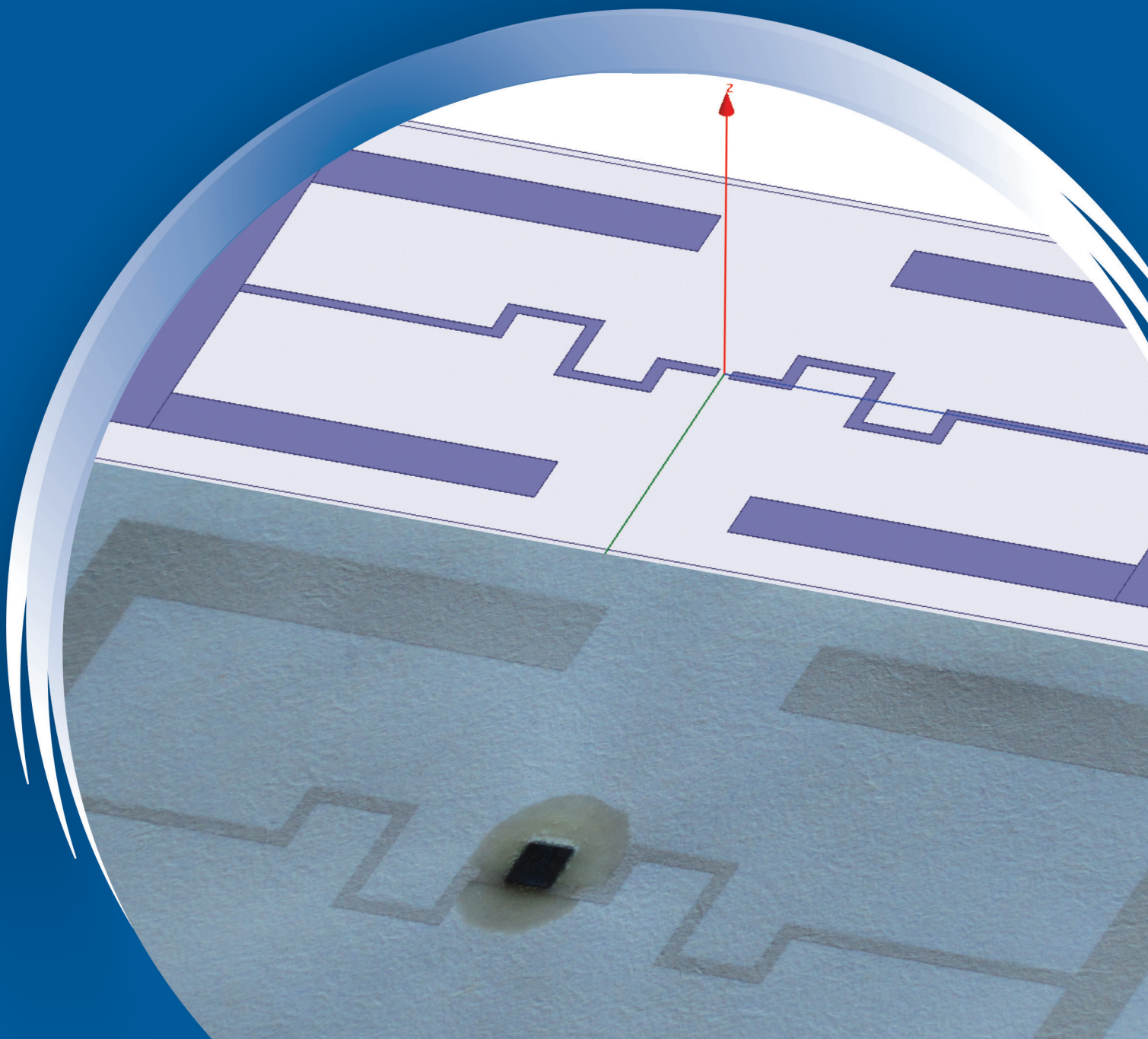

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Original scientific papers | Izvirni članki

Professional papers | Strokovni članki

Editorial | Uvodnik

Dear Reader,

This issue belongs to the second volume of our renewed journal, so it is time to review facts from the previous volume and reveal some statistics. The previous volume (vol. 42) brought some changes and reflects the renewal of the Editorial Board and the journal design. We have internationalized the EB with distinguished researchers across Europe and beyond to cover five areas of research and development:

- **Technologies and Materials** (Associate Editor: Asst. Prof. Dr. Danjela Kuščer Hrovatin)
- **Sensors and Actuators** (Associate Editor: Prof. Dr. Slavko Amon)
- **Electronics** (Associate Editor: Prof. Dr. Andrej Žemva)
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related to Microelectronics, Electronic Devices and Materials. The renewed Editorial Board counts 16 members (above are named five Associate Editors) with devotion to increase high quality standards for all types of papers being published in our journal (order of appearance in each quarterly issue):

- review scientific paper (*pregledni znanstveni članek*)
- original scientific paper (*izvirni znanstveni članek*)
- professional paper (*strokovni članek*)

Since we publish papers only quarterly we see no purpose to publish letter papers or short communication papers.

All submitted manuscripts undergo peer-review process with up to two reviewers and from manuscripts submitted in 2012 has brought the following statistics of submitted manuscripts:

- accepted 47 % (most of them after minor or major revision)
- rejected 26 % (most of them after revised version)
- under review 16 %
- out-of-scope: 7 % (before undergoing peer-review)
- withdrawn: 4 %.

The whole EB strived to shorten the review process and we cordially thank all reviewers, past, present and future, for their dedicated work in 2012. We have not calculated the time between submission and decision of submitted manuscripts yet, but the time spread is big and mainly depends on the willingness of potential reviewers to accept a manuscript for peer-review. In these modern times when nobody has time it is hard to find reviewers, but a broad international network of experts that members of editorial board have makes our peer-review process objective and time efficient. I sincerely thank all members of editorial board for numerous e-mails in search for reviewers.

In the volume 42 with its four issues we have publish 34 original scientific papers and one professional paper.

We still ask for and encourage you to submit review papers solicited to the above areas to be published. Some short news and announcements may appear at the end of each issue as it used to be in the previous volumes.

Marko Topič
Editor-in-Chief

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Original scientific paper

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Optimization of grooved micromixer for microengineering technologies

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Abstract: Due to the absence of turbulent flow and the slow diffusion process, mixing of solutions at micro-scale is a difficult task. This paper describes the optimization route towards the efficient design of a bottom grooved micromixer. Based on thoroughly discussed mixing mechanisms, the optimization was performed using FEM numerical simulations and the starting geometry was a Staggered Herringbone Mixer (SHM) groove design. Optimization procedure consists of two sequences: (I) one SHM groove geometry is optimized based on the magnitude of transversal velocity at the end of the groove and (II) different configurations of six grooves are investigated taking into account capabilities and limitations of microengineering technologies (MET). Newly developed designs were benchmarked against the established SHM design and a better efficiency was achieved. Additionally, a good mixing efficiency was also achieved with a modified Slanted Groove Micromixer (SGM). A SGM prototype was machined by micro electrical discharge milling (EDM) technology. The simulation results were experimentally verified with flow visualization and a good agreement was observed. Due to simple 2.5D geometry and efficient mixing properties the proposed micromixer design is adequate to be used in the Lab-On-A-Chip (LOC) systems.

Keywords: micromixer, microstructures, micromachining, micro electrical discharge milling, microfluidics, design optimization, FEM simulations.

Optimizacija mikromešalnika z utori za izdelavo z mikroinženirskimi tehnologijami

Izvleček: Mešanje dveh tekočin v mikrokanalih je zaradi odsotnosti turbolentnih tokov in počasnega procesa difuzije oteženo. V prispevku je predstavljen pristop k optimizaciji geometrije mikromešalnika z utori. Za izhodiščno geometrijo je bil izbran kljukasti utor (SHM utor). Optimizacija je bila izvedena s pomočjo numeričnega modeliranja z metodo končnih elementov, upoštevajoč temeljne mehanizme delovanja mikromešalnika z utori. Optimizacija je bila izvedena v dveh korakih. Najprej je bila optimizirana geometrija enega SHM utora glede na povprečno velikost komponente hitrosti prečno na mikrokanal takoj za utorom. Nato je bil raziskan vpliv geometrije različnih konfiguracij šestih utorov, kjer so bile upoštevane zmogljivosti in omejitve mikroinženirskih izdelovalnih tehnologij. Nov dizajn izkazuje boljšo učinkovitost mešanja v primerjavi z uveljavljenim dizajnom. Dobro učinkovitost mešanja izkazuje tudi geometrija mikromešalnika s poševnimi utori (SGM geometrija). Za namen verifikacije simulacij je bil izdelan prototip SGM geometrije s tehnologijo mikro elektroerozijskega dolbenja. Rezultati simulacij so bili eksperimentalno verificirani z metodo vizualizacije toka fluida in opaženo je bilo dobro ujemanje. Zaradi preproste 2.5D geometrije mikrostruktur in učinkovitosti mešanja je predlagan dizajn mikromešalnika primeren za uporabo v sistemih laboratorija na čipu (LOC).

Ključne besede: mikromešalnik, mikrostrukture, mikroobdelava, mikro elektroerozijsko dolbenje, mikrofluidika, optimizacija dizajna, metoda končnih elementov, simulacije.

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1. Introduction

Miniaturization is a recent trend in analytical chemistry and life sciences as well as in non-silicon micromachining technologies [1,2]. In the past two decades, miniaturization of fluid handling and fluid analysis has emerged in the interdisciplinary field of microfluidics. A micromixer is a microstructured device and is an important component of a microfluidic system. Rapid mixing is essential in many of microfluidic systems used in biochemistry analysis, drug delivery, sequencing of synthesis of nucleic acids as well as in microreac-

tor systems [3-6]. Its function is to mix the reactants for initiation of the reaction process, and it is an indispensable component in lab-on-a-chip (LOC) platforms for complex chemical reactions. Micromixers can be integrated in a microfluidic system or work as stand-alone devices.

To mix solutions at the micro-scale is a difficult task. Under typical low Reynolds number operating conditions ($Re < 100$) the fluid flow is laminar. The absence of turbulent flow patterns and a slow diffusion process are the main challenges to overcome in order to achieve mixing. The ratio between the mass transport due to advection and that of diffusion is defined by Peclet number $Pe = vL/D$ where v denotes mean fluid velocity, L is a characteristic linear dimension of the channel geometry and D is a mass diffusion coefficient. In microchannels, the Peclet number is typically higher than 100, meaning a very slow diffusion process with respect to advection [7].

In contrast to active micromixers, where an additional source of energy has to be introduced into the microfluidic system (e.g. time-dependant electric or magnetic fields [8,9]), passive micromixers depend solely on pressure driven flow through the system relaying on enhancing mixing through lamination of the solute flow [10,11], injection of solute into a solvent flow [12], forming droplets of the mixed liquids [13] or inducing chaotic advection of the fluid flow by means of placing obstacles within the flow path [14,15], making a complex 2.5D channel geometry (e.g. modified Tesla structure [16]) or pattern the inner channel walls with oblique grooves [6,17-22]. Passive micromixers do not require external actuators. Therefore they are robust, stable in operation and easily integrated into more complex systems.

Bottom grooved micromixers attracted a lot of research interest due to the good mixing efficiency below $Re < 50$, small pressure drop, and established soft lithographic methods for its fabrication [6,17,19,20,22]. The most common geometries of grooved micromixers are the slanted groove micromixer (SGM) and the staggered herringbone micromixer (SHM), both embedded on the floor of the microchannel. The SGM grooves are inclined at an angle with respect to the axial direction, whereas the SHM grooves have the shape of a herringbone pattern (Fig. 1).

The oblique grooves serve to transport fluid from the apex of the groove structure to the downstream edges of the microchannel. Consequently, the fluid in the upper part of the channel starts to rotate in the opposite direction causing a helical flow pattern. The herringbone pattern of the SHM generates two counter-rotating helical flows and when alternating the asymmetry of the SHM grooves a chaotic flow profile is created. The circulating motion stretches and folds the fluids, which exponentially reduces the distance over which different molecules have to diffuse.

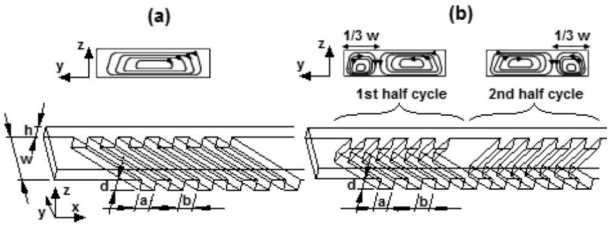

Figure 1: (a) Typical geometry of the slanted groove micromixer (SGM) and the schematic representation of streamlines in the channel cross-section. (b) Geometry of the staggered herringbone micromixer (SHM) and schematic representation of double helical motion caused by the groove geometry. One full cycle is composed of two half-cycles, one half-cycle has grooves oriented the same way.

To date, there have been a number of theoretical, experimental, and numerical studies aimed at the optimization of SGM and SHM geometry [6,17,23-30]. Different approaches were applied when optimizing the mixing efficiency of SGM and SHM geometries by means of numerical simulations. Hassel and Zimmerman [31] investigated convective motion through SHM geometries and used several flow based descriptors. They concluded that the efficiency of the groove in moving fluid cross channel could be reasonably described by the single groove case. Lynn and Dandy [24] defined a measure to quantify the magnitude of helical flow within the SGM by the ratio of non-axial to axial flow, normalized by the groove-ridge width and the channel width. They avoided the criteria of numerically simulated concentration fields due to possible numerical errors. Among the methods to quantify SHM and SGM mixing efficiency such as particle tracking [15,23,32,33], striation thickness [30], flow helicity [31], length of stretching [33,34], entropic measures [27], the relative variance of the concentration profile is most commonly used [14,16,25,26,34].

Experimentally, numerically simulated mixing behavior can be verified through the imaging of the concentration profile on the surface of the see-through micromixers by studying the change of color due to some chemical reaction of the fluid phases [6,15,18,19]. More detailed information at higher cost can be obtained by confocal microscopy [17,20,21]. Recently, Du et al. [6] verified the simulation results through fluorescent quenching experiments thus proving that numerically solved convection-diffusion equations give reliable information about mixing efficiency.

The SGM and SHM realizations reported in the literature have a lot of shallow grooves on the bottom of the mixing channel which suits the characteristics of soft lithographic manufacturing methods [6,17,19,20]. Thus, most of the optimization studies are limited to small deviations around the originally proposed geometry by Stroock et al. [17] which leads to local optimums within confined geometrical dimensions. The related papers provide a general trend about the geometry layout of microstructured grooves and its effects on mixing performance. However, the true optimum design has yet to be discovered for a specific application through numerical simulations [6].

For a successful micromixer design, it is important to consider the fabrication methods. In addition, microengineering technologies (MET) such as laser ablation, micromilling, micro EDM milling, etc. enable the fabrication of long life tools with high aspect ratio microstructures using, for example hardened steel or ceramics [1]. Thus, optimization of efficiency of every single groove is essential to minimize the costs of micromixer fabrication.

In this paper, a detailed insight into the design, optimization, analysis and performance of the grooved micromixer, suitable to be machined with micro EDM milling, is presented. The optimal geometry was benchmarked against established SHM design and the validity of simulations was checked with a flow pattern visualization of the optimized geometry. Special attention is given on the appropriateness of the design to be machined by non-silicon based micromanufacturing technologies and their limitations such as inability to produce sharp inner corners.

2. Materials and methods

2.1. Geometry of the micromixer

Original groove geometry of SHM, proposed by Stroock et al., was used as a starting geometry for mixer design optimization [17]. In Fig. 1(b), a typical structure of the SHM is shown which also denotes the variables used for groove optimization, namely *a* for the lateral groove width, *d* for groove depth and *b* for distance between two successive grooves. Primary flow flows along the *x*-axis, the *y*-axis is in the direction of the channel width and *z*-axis is in the direction of channel height.

The main channel width *w* and height *h* were fixed to $w = 200$ µm and $h = 50$ µm, since the selected channel size is commonly used channel cross section of commercially available microreactor systems [35,36].

The asymmetry of the SHM grooves was set to one third, meaning that the apex position of the groove is positioned at one third of the channel width, since that was found to be the optimal apex position in SHM design in the alternating half-cycle configuration [17,26]. The grooves are patterned at a 45° angle to the *x*-axis [17,26]. The total length of a simulated channel varied from 1.5 mm for simulations of one-groove geometry to 3.5 mm for six groove geometry. Preliminary simulations showed that only few optimized grooves were sufficient to complete the mixing. Thus the number of grooves for multiple groove configurations was fixed to six in order to show the efficiency of optimized one-groove geometry in comparison to established SHM geometry, and to maintain a design layout compatible with micro EDM milling technology. In line with the paradigm of design for manufacturing (DFM) the corners of groove geometries in multiple groove configurations were rounded to a minimum radius of $r_{groove} = 25$ µm which is readily achievable with micro EDM milling. Investigated groove parameters at different mixing regimes are gathered in Table 1.

2.2. Simulation tool

CFD modeling was performed using Comsol Multiphysics 4.1 which implements the finite element method (FEM) for numerical computation of physics governing equations. The numerical simulation was used to solve Navier-Stokes equations for incompressible fluid and convection-diffusion equations at steady state. The governing equations that describe the physical phenomena of mixing are as followed: Navier-Stokes (NS) equations,

$$\rho(\mathbf{v}\cdot\nabla)\mathbf{v} - \nabla\cdot\eta\left(\nabla\mathbf{v} + (\nabla\mathbf{v})^T\right) + \nabla p = 0,$$
$$\nabla\cdot\mathbf{v} = 0, \qquad (1)$$

Table 1: Presentation of parameters varied and configurations used: *a* – groove width, *d* – groove depth, *Re* – Reynolds number, *b* – ridge distance, r_{groove} – corner rounding, *D* – diffusion coefficient.

One-groove geometry			Six groove geometry, Re = 0.5, D = 10^{-9} m^2/s		
a [mm]	d [mm]	Re	b [mm]	r_{groove} [mm]	Configurations
0.05 – 0.30	0.03 – 0.20	0.5 - 20	0.05 – 0.35	0.025, 0.05*	SHM, SGM

* only in configuration of SGM_{rmax}

and convection-diffusion (CD) equations,

$$D\nabla^2 c - \mathbf{v}\cdot\nabla c = 0. \quad (2)$$

In equations 1 and 2 ρ denotes density [kg/m^3], $\boldsymbol{v}$ is the velocity vector [m/s], η denotes viscosity [Pa·s], p equals pressure [Pa], D denotes the diffusion coefficient [m^2/s] and c represents the concentration [mol/m^3].

Meshing of simulated geometries was implemented by the software applying free mesh elements that can easily adapt to the structure of the channel. The tetrahedral free meshing method with meshing parameters similar to that reported in literature was used [6,20]. Briefly, the computation of NS and CD equations was decoupled in order to reduce the computational power needed to run the simulation on a PC workstation (Intel i7 processor, 24 GB RAM). Maximum mesh element size for the main channel of the mixer used when solving NS equations was set to 15 µm, while the mesh in the grooves was set to 5 µm in order to reliably capture the fluid dynamics in the grooves. Maximum element size scaling factor was set to 0.2, element growth rate to 1.3, mesh curvature factor to 0.2 and the resolution of the narrow region to 1. Total number of mesh elements consisted of 2 to 6 x 10^5, depending on the simulated geometry. Mesh settings for solving CD equations were similar while reducing the maximum element size to 10 µm, resulting in 1 to 3 x 10^6 mesh elements. Finer adjustments of the mesh were performed in order to obtain the required convergence at a reasonable time scale while maintaining the required accuracy.

The fluid properties were set to the ones of water at 20˚C; density ρ = 998.2 kg/m^3 and viscosity η = 1.002 mPa·s. The diffusion coefficient of the solute was set to $D = 10^{-9}$ m^2/s since this is a typical value for most ions in aqueous solution. The inlet flows were set as inflows with average linear fluid velocity according to the *Re* regime investigated. The optimization of six groove geometries was conducted only for *Re* = 0.5, corresponding to v = 0.0063 m/s and a Peclet number of 630. The boundary condition for the outflow was set to 0 Pa (pressure, no viscous stress) and flow velocity at the walls to a no-slip condition (v = 0 m/s). Fluid concentration of one half of the channel was set to o 1 mol/m^3 (bright color) and the other half to 0 mol/m^3 (dark color) respectively. The post processing and visualizations of simulated results were obtained using the associated functions in Comsol and Matlab.

2.3. Optimization procedure

Measuring the quantity of the transversal flow is a logical predictor of the mixing efficiency [24,31]. Hassel and Zimmerman [31] also determined that peak values of non–axial velocities correspond to flow leaving the groove and that efficiency of the grooves in moving fluid cross channel could be reasonably described by the single groove case. These findings were utilized in presented optimization approach.

The optimization of the micromixer geometry was performed in two steps. In the first step, one-groove geometry was optimized based on the criterion of the average transversal velocity vector (Eq. 3). The average square root value of the velocity vector in directions perpendicular to primary flow (v_y, v_z) was calculated as

$$v_{AVGyz} = \frac{1}{N}\sum_i \sqrt{v_{y_i}^2 + v_{z_i}^2} \quad (3)$$

in the cut plane at the end of the single SHM groove (Fig. 2(a)), N denotes the number of points in the cut plane.

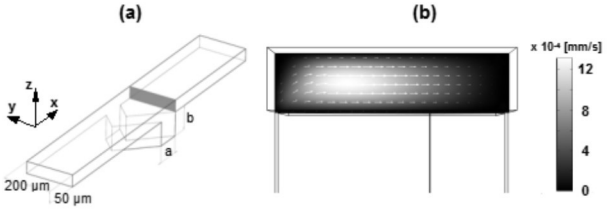

Figure 2: (a) Schematic presentation of single SHM groove geometry and the position of the cut plane where v_{AVGyz} is calculated. (b) Presentation of non-axial velocity field in *yz*-direction. Black and white color-coding denotes the amplitude of v_{AVGyz}.

In the second step an optimal 6 groove configuration, within the channel length of 3 mm, was determined by the criteria of relative variance of the concentration profile S at the distance x along the main channel length defined as,

$$S_x = \frac{\frac{s_x}{A_x}}{\frac{s_{inlet}}{A_{inlet}}}, \quad (4)$$

where s_x corresponds to variance of the concentration profile at particular cut plane,

$$s_x = \int_A (c_{xi} - c_\infty) dA, \quad (5)$$

where A denotes the *yz*-cut plane at coordinate x, c_{xi} denotes the concentration at a point on the cut plane and c_∞ denotes complete mixing, which is 0.5 mol/m^3 in our case. A value of S_x closer to 0 corresponds to better mixing performance.

2.4. Experimental setup

Based upon preceding geometry optimization a micromixer prototype was machined by micro EDM milling technology (Fig. 3(a)) in the tool steel (Fig. 11, configuration SGM_{rmax}—25). The lateral dimensions of the machined geometry were measured with optical microscope CETR, UMT Multi-Specimen Test System at a magnification of 550. Depth of micromixer structures was measured with a laboratory developed laser system with a resolution of 1 µm. The measured dimensions were:

- main channel width: $w = 203 \pm 4$ µm,
- main channel height: $h = 50 \pm 3$ µm,
- groove width: $a = 150 \pm 4$ µm,
- bottom groove depth: $d = 148 \pm 3$ µm.

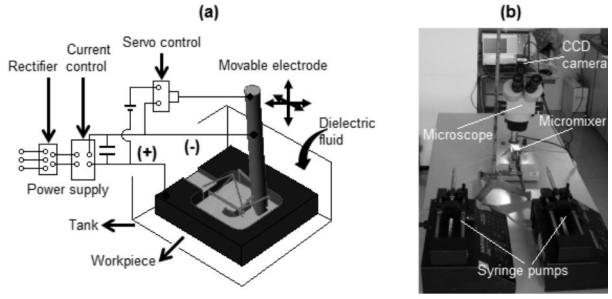

Figure 3: (a) Schematic presentation of micro EDM milling process. (b) Experimental setup.

Experimental setup is shown on Fig. 3(b). To seal the micromixer, a Plexiglas cover was bolted on the steel substrate which was polished to mirror finish before micro EDM milling. Plastic adapters were fitted for two inlets and one outlet. Two syringe pumps (PHD 4400, Harvard apparatus) were used to introduce two colored water phases into the micromixer. One phase was colored blue (Water blue, 5 g/l, dark color on grayscale figures) and the second one red (Congo red, 0.5 g/L, bright color on grayscale figures). These colored aqueous solutions provide a good contrast due to high solubility and large extinction coefficient of the dye. Due to the similar chemical structure of both solvents their diffusion coefficient is approximately the same and the reported value found in the literature corresponds to $D = 3.2 \cdot 10^{-10}$ m²/s [10].

A CCD camera (Image source DFK 22) was attached to the optical microscope with 100 times magnification and resolution of 4 µm per pixel. The inflow for each phase was set to 1.875 µl/min, which corresponds to an average fluid velocity of 6.3 mm/s.

Captured images were processed in MATLAB and RGB values of pixels at investigated cross sections were used to determine the phase borders. The results of simulation were verified via comparison of the course of the interface between both phases obtained by simulation and experiment.

3. Investigation of one-groove geometry

Investigation of one-groove SHM geometry was conducted under various *Re* regimes, namely from 0.5 to 20. The geometry parameters under investigation were lateral groove width *a* and groove depth *d*. Average transverse flow v_{AVGyz} induced by the groove was calculated at a cut plane at the end of the groove, and its dependence on groove geometry and flow regime is presented in Fig. 4. Values of v_{AVGyz} are normalized with the average fluid velocity along the *x*-axis, corresponding to each *Re* regime in order to make the comparison more transparent.

The amount of transversal fluid motion caused by the SHM groove, described by the parameter v_{AVGyz} is strongly dependent on the depth and width of the groove. For a fixed groove depth an optimal groove width exists; wider groove does not contribute to the increase of velocity v_{AVGyz} (Fig. 3). The same conclusion stands for groove depth. Beyond a certain groove depth the transversal motion of the fluid is not enhanced. This is due to the fact, that fluid near the bottom of deeper grooves has less impact on the flow profile (Fig. 5(a)). Therefore, for specific main channel geometry an optimal SHM groove geometry exists.

Optimal groove dimensions were considered at the intersection of the two asymptotes (Fig. 4). The first describes transversal motion of the fluid (v_{AVGyz}) at short groove widths ($a \rightarrow 0$) and the second corresponds to longer groove widths ($a \rightarrow \infty$); optimal groove depth at all simulated *Re* regimes corresponds to d_{opt} = 100 µm. Later observation is in line with findings that optimal groove depth is mainly determined by the channel aspect ratio [6,24]. By this characterization of optimal one-groove geometry, two important mixer efficiency conditions are satisfied: minimization of dead volume of the groove and minimization of volume to be removed by the micro EDM milling process in order to fabricate the geometry while maintaining the optimal mixing efficiency. The choice of d_{opt} = 100 µm is further clarified in Fig. 5(b), where at fixed $Re = 0.5$ and $a = 150$ µm the relative magnitude of v_{AVGyz} at $d = 100$ µm reaches 97.2% of the value of the deepest groove tested, $d = 200$ µm.

Fig. 4 shows the v_{AVGyz} dependence on the flow regime. Up to a *Re* number 10 the optimal groove dimensions are basically the same, i.e. groove width a_{opt} = 150 µm

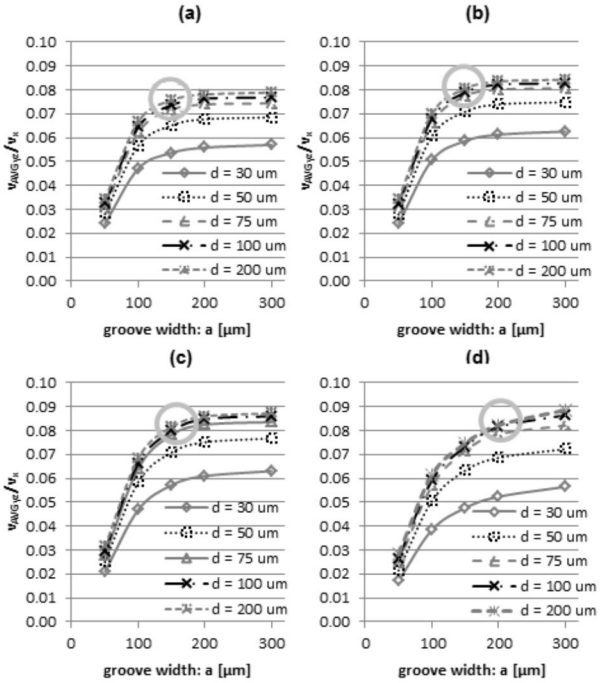

Figure 4: Dependence of relative magnitude of average transversal velocity (v_{AVGyz}/v_x) on SHM groove depth d and groove width a for (a) Re = 0.5, corresponding to average fluid velocity in x-direction of v_x = 6.3 mm/s, (b) Re = 5, v_x = 63 mm/s, (c) Re = 10, v_x = 126 mm/s and (d) Re = 20, v_x = 252 mm/s. Circles denote regions of optimal one-groove geometry dimensions.

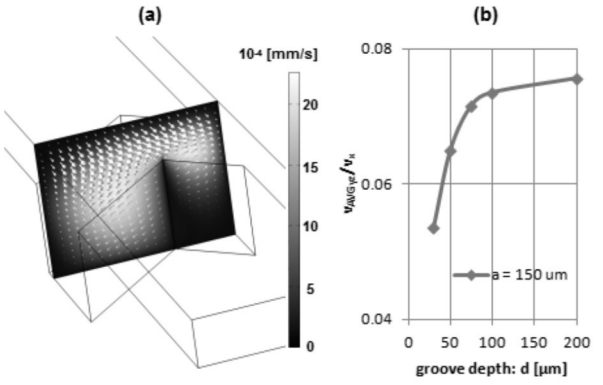

Figure 5: (a) Vector velocity field within the SHM groove, a = 150 μm, d = 100 μm. (b) Dependency of v_{AVGyz}/v_x on groove depth at fixed groove width a = 150 μm and Re = 0.5.

and groove depth d_{opt} = 100 μm. An evident shift towards a wider optimal groove dimension is seen at Re = 20, indicating a different flow behavior which can be explained as follows: greater the inertial forces, less fluid enters the groove. Increased inertia hampers the fluids ability to enter the groove and reduced viscous effects inhibit the ability of the entrained liquid in the groove to transfer momentum trough viscous stresses to the bulk flow. This conclusion is in line with the observations reported in the literature dealing with shallow grooves [20,31].

The efficiency of SHM is in strong connection with creating maximal cross channel fluid transfer. Yang et al. [26] concluded that the flow rate within the grooves of the SHM is substantiated as the most critical parameter of its efficiency which supports our choice of defining one-groove mixing efficiency by v_{AVGyz}. v_{AVGyz} is indirectly correlated with entrained fluid in the groove, namely, fluid cross channel transfer at the end of the groove is a consequence of momentum transfer of entrained fluid dragging the bulk flow due to viscous stresses.

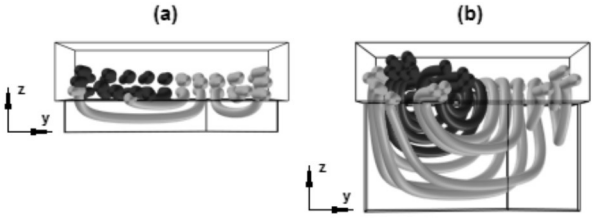

Figure 6: (a) Comparison of streamlines of one SHM groove at Re = 0.5, a = 50 μm, d = 30 μm and (b) a = 150 μm, d = 100 μm. Starting points of bottom row streamlines were set to 5 μm and upper row to 30 μm above channel floor. The amount of rotation of the streamlines after exiting the groove can be directly correlated to v_{AVGyz} parameter.

Another important mixing efficiency factor of one-groove geometry is evident from Fig. 6. As both fluid phases enter the groove the interface surface stretches and significantly increases the area over which diffusion takes place. Stretched interface surface is then folded in the bulk channel, further increasing the interface area by induced cross-channel convective motion resulting in greater mixing efficiency per groove.

4. Investigation of 6 groove configurations

4.1 Investigation of one full-cycle SHM configuration

Grooved micromixers are efficient only in sequences of multiple grooves. For established SHM configurations the grooves are organized into half-cycles, denoting a specific number of consequent grooves with the same apex orientation (Fig. 1(b)). In order to explore the cumulative effect, the influence of ridge distance b between two consecutive grooves on mixer performance, using one whole cycle SHM configuration was investigated. This configuration is denoted as SHM_6_3 meaning that six-grooves are organized in 3 grooves

per half-cycle (represented in Fig. 8, #3). The optimal geometry of a single groove determined in section 3 with a rounding of inner corners to r_{groove} = 25 µm was applied. The course of mixing along the length of the main channel (*x*-axis) for different ridge distances between consecutive grooves *b* is presented in Fig. 7.

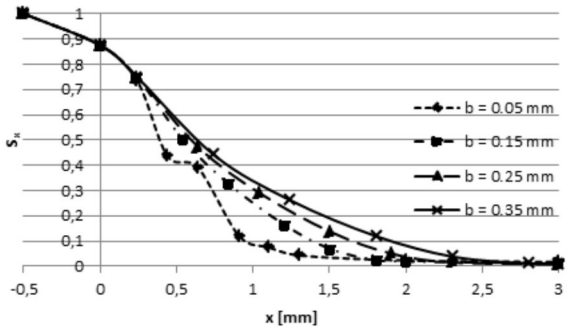

Figure 7: The course of mixing for SHM_6_3 configurations with different ridge distances *b*. First 0.5 mm is a grooveless section. Relative variance of the concentration profiles S_x was determined after every groove and at the exit of the channel (x = 3 mm).

The most efficient SHM_6_3 geometry is the one with the longest ridge distance tested b = 0.35 mm (Table 2). A plausible explanation of this result is as follows: if we presume that a single groove has a similar efficiency regardless of the ridge distance then in SHM_6_3_35 configuration the grooves are evenly distributed along the 3 mm main channel, enhancing the mixing process along the whole channel length, whereas in SHM_6_3_05 only 1.3 mm is effective. In the shortest configuration a reduction in the effectiveness at the cross-over region between half-cycles can be observed (Fig. 7, b = 0.05 mm, at x ≈ 0.5 mm).

In Table 2, an asymmetry around a mean concentration value of 0.5 can be noticed (c_{max}, c_{min}). This is due to the fact that a finite number of grooves are present in the simulated geometries, resulting in a skewed concentration distribution.

Efficiency of mixing can also be expressed with the minimum mixing length where 90% of the mixing is achieved. This value corresponds to the relative concentration variance value of S_x = 0.1 [25,26]. By this criterion the SHM_6_3_05 configuration is vastly superior to others, since 90% of mixing is achieved in the first 0.91 mm. On the other hand, from the production technology point of view, thin ridges could pose difficulties when manufacturing. From the results presented another important finding should be put forward: when dealing with a limited number of grooves the cumulative resonance effect, denoting an increased fluid entrainment due preceding groove(s) [23,24,26], does not outperform the configurations with longer ridge distances where cross channel convective motion decays, thus every groove fully exploits it's mixing potential. Due to the similar mixing performance the optimal ridge distance is between 0.25 and 0.35 mm for the given geometry.

It can also be inferred that in case of dealing with chemical solutions of slower diffusion constants and consequently higher Peclet numbers, the higher number of grooves is needed. If the optimization objective is mixing on the shortest distance possible, then ridge distance should be kept minimal, in this case 0.05 mm.

4.2 Investigation of six groove SHM and SGM geometry

The optimal number of grooves in a half cycle is not known in advance, thus all possible 6 groove SHM configurations were tested. In addition, the ridge distance b between the consecutive grooves was varied on the interval of 0.05 mm < b < 0.35 mm. Mixing efficiencies of simpler SGM groove configurations are also presented. Denotations of particular configurations are explained in Fig. 8. All the configuration tested exhibited the best mixing efficiency with the ridge distance b between 0.25 mm (Fig. 8, configurations #1, #2, #4, #6) and 0.35 mm (Fig. 8, configurations #3, #5, #7) implying that the optimal gap between consecutive grooves in order to fully exploit the potential of each single groove, should be in this range.

Among the tested configurations the most efficient one turned out to be SHM_6_2_25 (#1) based on both

Table 2: Presentation of mixing efficiency of the SHM_6_3 design with respect to ridge distance *b*. S_x – relative variance of concentration profile; c_{max} and c_{min} – maximum and minimum concentration value at x = 3 mm; *90% mix.* – length after 90% of mixing is achieved;

Ridge distance b [mm]	0.05	0.15	0.25	0.35
Configuration den.	SHM_6_3_05	SHM_6_3_15	SHM_6_3_25	SHM_6_3_35
S_x (x = 3 mm)	0.017	0.013	0.010	0.009
c_{max} (x = 3 mm)	0.615	0.610	0.614	0.633
c_{min} (x = 3 mm)	0.425	0.437	0.441	0.444
90% mix., (S_x = 0.1) [mm]	0.91	1.40	1.65	1.9

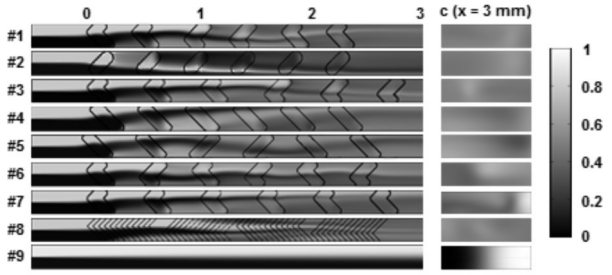

Figure 8: Best six groove SHM and SGM configurations at *Re* = 0.5 ordered from best to worst configuration. Configuration denotations are as followed: SHM_6_2_25 (#1), SGM_{rmax}_6_6_25 (#2), SHM_6_3_35 (#3), SGM_6_6_25 (#4), SGM_6_2_35 (#5), SHM_6_1_25 (#6) and SHM_6_6_35 (#7). Configuration #8 represents the benchmark geometry and #9 presents a grooveless channel. Explanation of specific configuration denotation: SHM or SGM_number of grooves_number of grooves in a half-cycle_ridge distance in tenths of millimeters. On the right part of the figure concentration profiles of the *yz*-cut plane at $x = 3$ mm are presented. The scale shows the color coding for concentrations.

criteria used, namely the lowest relative concentration variance and concentration profile at $x = 3$ mm (Figs. 9 and 10). The results show, that just 2 optimized grooves in a half-cycle by spatial transfer of the fluid efficiently stretch and fold both phases across the channel (Fig. 8, #1), which confirms the hypothesis of Lynn and Dandy [24] stating that only several grooves per half-cycle could be enough. In the first half-cycle the side with longer SHM groove arm is chiefly active. In the second half-cycle the longer arm switches position and exhibits strong mixing in that region. The last half-cycle further enhances mixing.

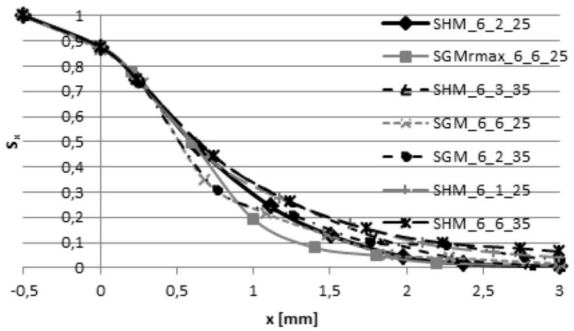

Figure 9: The course of mixing for the best 6 groove configurations optimized for ridge distance *b*. Relative concentration variance S_x is determined after every groove.

Surprisingly, due to the known fact of SHM geometry supremacy [6,17,24], SGM with the largest rounding radius, denoted as SGM_{rmax}_6_6_25 (#2), performed second best ($S_{3mm} = 0.008$) and significantly better than the #4 configuration with smaller corner radius. Due

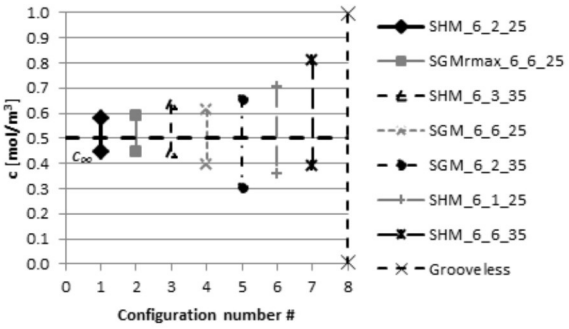

Figure 10: Minimum and maximum values of the concentration profile (c_{min} and c_{max}) for optimal 6 groove configurations at the outlet of the channel ($x = 3$ mm)

to largest corner rounding the configuration exhibited more complex rotation cycles which was also indicated by an increase of v_{AVGyz} by 45% in comparison to results obtained with sharp one-groove SGM geometry. It should be noted, that a significant part of increase of v_{AVGyz} is a consequence of a reference cut plane being closer due to groove rounding and thus direct comparison of the values would not be prudent. The poorly performing SGM_6_2_35 (#5) configuration, which can be viewed as an approximation of the #1 configuration without the shorter groove arms, highlights the important role of SHM's short arm.

Low mixing performance of SHM_6_1_25 (#6) configuration implies that one groove only does not transfer enough fluid across the main channel in order to promote stretching and folding of both fluid phases. The main reason for low efficiency is the effect of oppositely signed grooves, where the changing groove shape causes a reverse in directions of v_y and v_z, which results in dissipation of flow caused by the previous groove similarly observed by Hassell and Zimmerman [31].

The worst configuration of all tested was SHM_6_6_35 (#7). This is due to the obvious reason of the same orientation of grooves throughout the channel, thus the fluid in the shorter arm side remained very poorly mixed. On the other hand, good mixing is achieved in the longer arm section. This observation supports the hypothesis of Lynn and Dandy that the fluid flow within the long arm is the primary mechanism of mixing [24].

To show the adequacy of presented optimization procedure a benchmark simulation was performed applying established SHM design. Benchmark geometry was a slightly modified geometry proposed by Stroock et al. [17] with the main difference in the main channel cross-section which was fixed to ours ($h = 50$ µm, $w = 200$ µm). The benchmark micromixer, denoted as SHB, consisted of four half-cycles of 6 grooves with a groove depth of 35 µm, groove width of 50 µm and groove

ridge distance of 50 µm (Fig. 8 #8). Quantitative indexes show that SHM_6_2_25 design is more efficient compared to SHB design (Table 3). Thus, only six grooves of optimal dimensions compared to 24 grooves of established geometry are sufficient, making the final design compliant with the micro EDM milling technology.

Table 3: Comparison between benchmark SHB design and SHM_6_2_25 design. Values represent S_x – relative variance of concentration profile; c_{max} and c_{min} – maximum and minimum concentration value at x = 3 mm; *90% mix.* – length after 90% of mixing is achieved; p – pressure drop across the whole channel length.

Design	S_x (x = 3 mm)	c_{max} (x = 3 mm)	c_{min} (x = 3 mm)	90% mix., [mm]	p [Pa]
SHB	$6.95 \cdot 10^{-3}$	0.585	0.441	1.70	109.6
SHM_6_2_25	$4.87 \cdot 10^{-3}$	0.579	0.450	1.60	98.9

5. Experimental verification

In order to verify simulation results, a SGM_{rmax}–25 configuration was fabricated in tool steel by micro EDM milling starting with a 1 mm grooveless section before the first groove. Due to using the tool steel, verification methods which require see-through material could not be applied, thus actual mixing efficiency could not be determined. As the corresponding flow patterns are closely related to mixing efficiency [20], an indirect method via verification of the flow patterns was applied. A new simulation of mixing dynamics was performed using the diffusion constants of the experimentally used water coloring agents, namely $D = 3.2 \cdot 10^{-10}$ m^2/s. A good agreement of simulated and experimental flow patterns can be observed in Fig. 11.

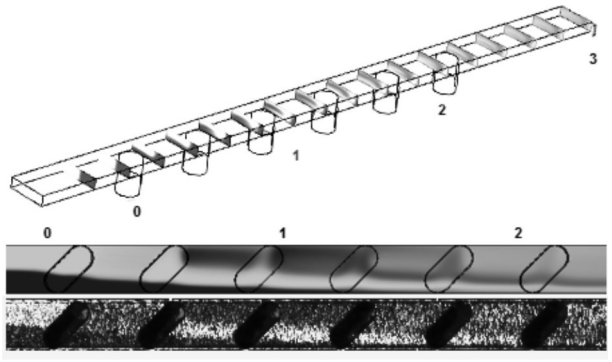

Figure 11: Experimental verification of the simulated flow pattern: on the upper part of the figure the dynamics of the water phases along the channel is presented. The middle picture shows the presence of both phases in the *xy*-plane at z = -25 µm. The bottom photograph of the experiment shows the course of the red phase (bright color) along the *x*-axis which closely resembles the simulated flow pattern.

In the upper part of Fig. 11 the principle of enhanced mixing by the SGM_{rmax} due to stretching and folding of the fluid phases, is presented. As both water phases start rotating in a clockwise direction, the interface layer dramatically increases. The brighter colored band can only be seen when the red phase occupies the whole vertical space from the top to the bottom of the channel, since this is also the direction of the channel observation through the microscope. For this reason a *xy*-plane at the height of z = -25 µm was selected as a cut plane to present results of the simulation and to compare the phase distribution along the *x*-axis with experimental results. The interface borders were detected by digital processing of the acquired pictures and obtained results are presented in Fig. 12. Excellent agreement of the course of the interface along the channel between both water phases is observed, thus it can be concluded that simulations reflect the real environment.

6. Conclusions

In the paper optimization procedure for grooved micromixer design suitable for microengineering technologies is presented. Principles behind grooved micromixer efficiency are thoroughly discussed and analyzed with FEM simulations. Optimization procedure can be easily applied in micromixer design stage.

Firstly, one groove geometry is optimized to maximize transversal fluid movement at the end of the groove. The simulation results revealed that for all Re regimes tested ($0.5 \leq Re \leq 20$), the optimal depth of the groove is 100 µm, but the groove should be wider in the case

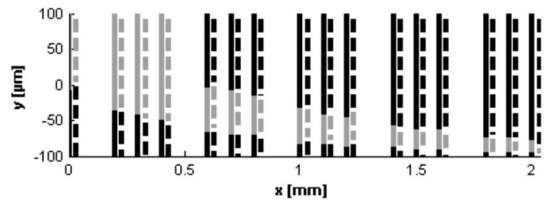

Figure 12: Detected interface border between two water phases with the bright color corresponding to the Congo red phase. A solid line is used for the simulation result at *xy*-plane of z = -25 µm and a dashed line for experimental results. The interface border was determined via computer image processing, in detail the amplitude of the R and B level of the RGB color scale were processed.

of higher Re regimes, thus optimal geometry of the groove is Re dependent.

In the second step, concentration parameters were used to quantify 6 groove configurations. Limitations and capabilities of micro EDM milling technology were considered. The results show that efficiency of mixing depends on configuration layout. The best configuration tested consisted of 2 grooves in a SHM half-cycle, which was benchmarked against an established SHM design with 2 full-cycles of 24 grooves and the new design performed better using only 6 grooves, making the design compliant with MET. The adaptation of the micromixer design to the manufacturing technology resulted in much simpler design with the same mixing capability as the original one.

Compared to the suggestions of the optimal grooved micromixer geometry found in literature our best groove design exhibits deeper and wider grooves. The mixing efficiency is further more enhanced through rounding of the groove corners.

A prototype of the optimized micromixer was produced by micro EDM milling. Experimental results were in good agreement with simulations. Furthermore, the micromixer was successfully applied in ionic liquid synthesis.

In the future work, optimized micromixer design will be used in a realization of a low cost microreactor system, made from polymers. Obtained microstructural geometries are suitable to be implemented with micro injection moulding technology.

Acknowledgments

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Hidden node avoidance mechanism for IEEE 802.15.4 wireless sensor networks

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Abstract: IEEE 802.15.4 is the standard for short range Wireless Personal Area Networks (WPAN). It is targeted for battery powered applications where a long battery life is the main requirement. Most of the device energy is spent for radio communication, where packet collision, caused due to a hidden node problem, is one of the main sources of unnecessary energy waste. IEEE 802.15.4 standard does not originally provide any protection from hidden node collisions. This paper shows influences of hidden node problem on the overall network performances and presents the RTS/CTS handshake mechanism which can be successfully used to prevent hidden node collisions in IEEE 802.15.4 wireless networks.

Key words: Hidden node, Wireless sensor network, IEEE 802.15.4, MAC, RTS/CTS

Mehanizem izogibanja problema skritega vozlišča v IEEE 802.15.4 brezžičnih senzorskih omrežjih

Povzetek: IEEE 802.15.4 standard, za brezžična osebna omrežja (WPAN), je namenjen za aplikacije s baterijskim napajanjem, kjer je pomembna dolga življenjska doba baterije. Tovrstne naprave porabijo večino energije za radijsko komuniciranje. Eden izmed najpomembnejših vzrokov za nepotrebno porabo energije predstavlja problem skritih vozlišč, zaradi katerega prihaja do trkov paketov. Standard IEEE 802.15.4 originalno ne ponuja mehanizmov zaščite pred trki paketov. V tem članku smo prikazali rezultate analize vpliva problema skritih vozlišč na zmogljivost omrežja ter predstavili RTS/CTS mehanizem rokovanja, ki predstavlja eden izmed uspešnih pristopov preprečevanja trkov paketov, ki nastajajo zaradi skritih vozlišč v IEEE 802.15.4 brezžičnih omrežjih.

Ključne besede: Skrito vozlišče, Brezžično senzorsko omrežje, IEEE 802.15.4, MAC, RTS/CTS

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1. Introduction

Wireless sensor networks (WSN) consist of a large number of autonomous battery-powered sensor devices, referred as *nodes*. They are capable to measure an environmental event, process and transmit collected data to a central node in network. One of the main goals in the wireless sensor networks design process is to minimize overall power consumption in order to achieve months or even years of autonomy operation with the use of a single set of batteries. WSN power consumption can be reduced through a careful selection of low power devices and by suitable communication protocols, which permit usage of long periods of inactivity to take full advantage of low power modes of the device; known as sleep mode.

Much of the node's energy is used for radio transmission, which needs to be efficient in order to increase service life of sensor nodes. There are several sources of unnecessary energy waste during radio communication such as: idle listening, overhearing, protocol's overhead, packet loss due to collisions, etc [1]. One of the biggest sources of energy waste is packet collision. Packet collision represents situation when two nodes transmit packets at the same time, which results in partial or complete distortion of packet on the recipient node. Collided packets cannot be received and they need to be discarded and retransmitted again.

1.1 Problem formulation

IEEE 802.15.4 standard [2] uses blind backoff CSMA/CA (Carrier Sense Medium Access with Collision Avoid-

ance) channel access mechanism, where device checks the state of the channel before any transmission. If it ensures that channel is free, it can start the transmission; if not it will retry the entire procedure after some time. This approach works fine only when all nodes hear each other, which is a rare case in WSN. In most cases, network's coverage area is much larger than the coverage area of a single node. A well-defined coverage area does not exist for wireless media because propagation characteristics are dynamic and uncertain. In that case, the node is not capable to discover what is happening beyond its receiver radio range and its transmission can lead to occurrence of hidden node collision. Hidden node collision occurs when two nodes A and C (Figure 1.) are communicating with node B, although they are not aware of each other's existence since they are not in radio range. According to papers [3] and [4], the probability that two randomly distributed nodes, in the radio range of central node, cannot hear each other is as high as 41%.

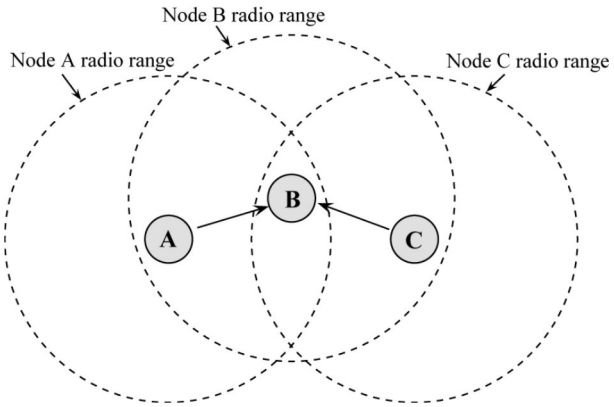

Figure 1: Explanation of hidden node problem

According to CSMA/CA, nodes A and C can start the transmission if they detect an idle channel. Since they cannot hear each other, they can begin the transmission simultaneously, without knowing that they have created packet collision on the node B. In this case, the node B is not able to receive any of the transmitted packets and both packets need to be retransmitted again, which causes unnecessary energy consumption.

IEEE 802.15.4 protocol does not originally provide any protection against the hidden node problem. Since these kinds of networks are designed for the low-rate traffic, occurrence of this phenomenon is rare. Probability of collisions, due to hidden nodes, increases with the increase of network traffic. This kind of scenario is also possible in networks with low-rate traffic, in places that represent traffic bottlenecks, which are usually located near the sink nodes. Occurrence of such events, in some parts of the network, can easily produce a chain reaction, which can affect or even disrupt operation of the entire network.

1.2 Related work

Several solutions to avoid a hidden node problem in WSN have being proposed. Besides the task of elimination of hidden node problem, these solutions need to comply with basic principles of WSN design, hence simplicity and energy efficiency. Solutions for hidden node problem in WSN can be classified into two categories: proactive and reactive approaches. Proactive approaches prevent occurrence of hidden node collision, by use of: busy tone mechanisms [5], carrier sense tuning [6], node groping [7, 8] or RTS/CTS handshake mechanism [9]. First two approaches are not practical since they require additional hardware radio resources which increase power consumption. Node grouping technique forms network groups in which all devices that participate in one group can hear each other. This solution suffers from frequent group reallocation in networks with mobile nodes. RTS/CTS Handshake mechanism employs channel reservation around transmitter and receiver using RTS/CTS frames. Their uses in IEEE 802.15.4 networks have been proposed in [10], although best to our knowledge, measurements of effectiveness of this solution have not been performed yet. Authors of paper [8] have analyzed a possibility to use RTS/CTS mechanism in WSN networks and have concluded that this method is not particularly suitable for WSN networks. Reactive approaches react only when hidden node collisions happened in order to solve collision chain and to prevent its future occurrence [3].

The main idea behind this research is to analyze the possibility of implementation of RTS/CTS handshake mechanism in IEEE 802.15.4 MAC as a hidden node avoidance mechanism. Since its implementation in IEEE 802.15.4 networks has just been suggested, measurements of its effectiveness are not performed. It is shown that the proposed hidden node avoidance mechanism helps to prevent collisions due to hidden nodes. The main disadvantage of this solution is high packet overhead which increases packet delay and limits its channel throughout, which limits its usefulness in IEEE 802.15.4 networks.

2. Influence of hidden node collisions on wireless transmission

In real world communications, modulated signals sent through a channel are received together with some unwanted signals, which are referred to as noise. Noise can be classified into two groups: background noise and interference noise. Background noise is present throughout the whole frequency spectrum. Interference noise represents a noise that is present in limited

parts of the frequency spectrum and which bandwidth overlaps with the bandwidth of the modulated signal. If interfering signal shares the same frequency spectrum, but uses different modulation its influence on the modulated signal can be treated the same as the background noise. If signals, which are interfering, are compliant, signal collision, known as co-channel interference, occurs. When compliant signals interfere, than they cause a collision, and their content may be damaged. If power of interfering signal is lower than the power of the originally received signal, there is a possibility that the original packet is received without any errors. This phenomenon, called capture effect, is in greater detail presented in this paper [11]. The amount of background noise presented in the received signal, is quantitatively represented in a form of Signal-to-Noise Radio (SNR), which represents the ratio between the power of the received signal P_S and the power of the background noise P_N. Signal-to-Interference Radio (SIR) represents the ratio between the power of the received signal P_S and the power of the interfering signal P_I. Signal-to-Noise-Interference Radio (SNIR) represents the ratio between the power of the received signal P_S and the sum of powers of background P_N and interference noise P_I.

Since these two noise sources have a completely different effect on the constellation diagram [12], their real influence on the BER is investigated with the use of MATLAB experiment. Developed simulation model (Figure 2.), consists of the two transmitters and one receiver. Transmitter is composed of the Bernoulli Binary Generator, Symbol-to-Chip mapping block and baseband O-QPSK modulator. Transmitters send a modulated signal, with a normalized power level, through AWGN (Additive White Gaussian Noise) channel, where background noise is added to the modulated signal. Power level of the background noise added to the signal is determined by SNR. Power of the interfering signal is determined by SIR.

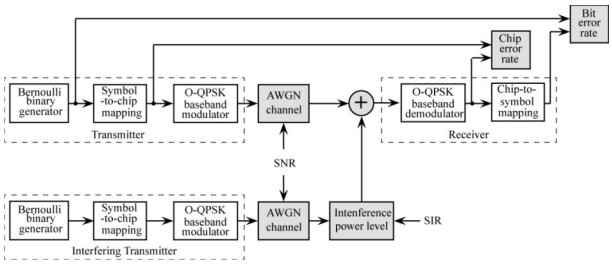

Figure 2: Matlab simulation model

Signals from both transmitters are added at the receiver side, where they are firstly demodulated by the O-QPSK demodulator. Received chip sequence is cross correlated to 16 known chip sequences and the most familiar is chosen as the output binary sequence. The difference between transmitted and received chip and binary sequences are determined by error rate calculation blocks. In preformed simulations, the SNR and SIR values are changed, which results in changes in power levels of the interfering signal and background noise, relative to power of the modulated signal. Received chip and bit sequences are compared to transmitted sequences in order to determine Chip Error Rate (CER) and Bit Error Rate (BER).

The first part of the simulation is performed under the presence of just background noise without an interfering signal, where SNR changes in range of [+10 dB,-10 dB].

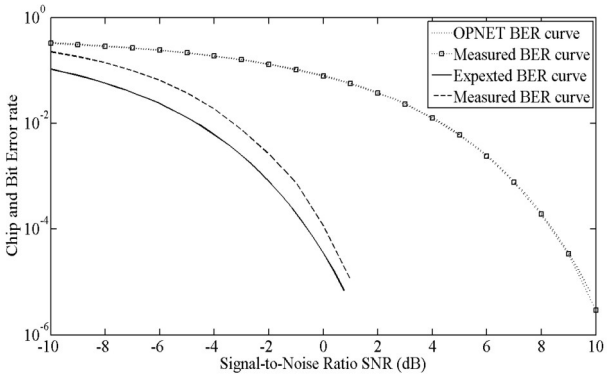

Figure 3: Error probability with just background noise

The results from Figure 3. show that the measured CER is in close match with theoretical results [2]. Results for measured BER curve show due to the use of signal spreading, an existence of the processing gain, although they do not reach the expected theoretical value of 9 dB [2]. This is probably because of use of quasi-orthogonal codes.

In the second part of the simulation collisions are modeled between the modulated and the interfering signal. The power of the interfering signal, relative to the power of the modulated signal is determined through the use of SIR value. Power level of the background noise, relative to the power of the modulated signal is determined by SNR parameter. The received chip and bit sequences are compared to the transmitted sequences in order to determine the Chip Error Rate (CER) and Bit Error Rate (BER). Since CER and BER are functions that depend on two variables, SNR and SIR, several simulations are performed for various fixed values of the SNR while during simulation, the SIR value is changed. These two parameters are transformed into SNIR, which give the ratio between the power of the modulated signal and all noise sources, including background noise and interference noise.

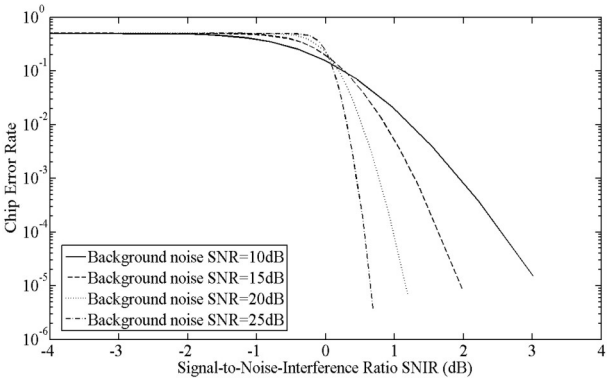

Figure 4: Error probability with both interference and background noise

Results obtained from simulations show significant differences between the effect of the background noise and interfering noise on the CER and BER. This indicates that these two noise sources need to be separated one from another. Based on the MATLAB simulation results, the appropriate model is created, which precisely models effects of these two noise sources on the chip and bit error probability.

3. IEEE 802.15.4 Simulation model

Effects that hidden nodes have on IEEE 802.15.4 WSN are examined by the developed simulation model in OPNET Modeler. The OPNET Modeler represents an environment for modeling, simulation and performance analysis of communication networks, devices and protocols. It is based on discrete event simulation, where simulation is executed as a chronological sequence of events. Each event occurs at an instant in time and marks a change of state in the system. OPNET Modeler provides hierarchical structure to modeling, where each level of the hierarchy describes different aspects of the complete model being simulated. Hierarchical model is composed from three levels: network model, node model and process model.

The starting point for a model presented in this paper is Open-ZB model of IEEE 802.15.4 network, developed by IPP-HURRAY! Group [13]. This model supports only star topology, where communication is established between a single PAN coordinator and arbitrary number of End Devices. Nodes in this model support Beacon Enabled mode with an unlimited radio range of all nodes participating in the network. Original Open-ZB model is modified in order to simulate effects of hidden nodes, and it is an upgraded structure that is presented in Figure 5.

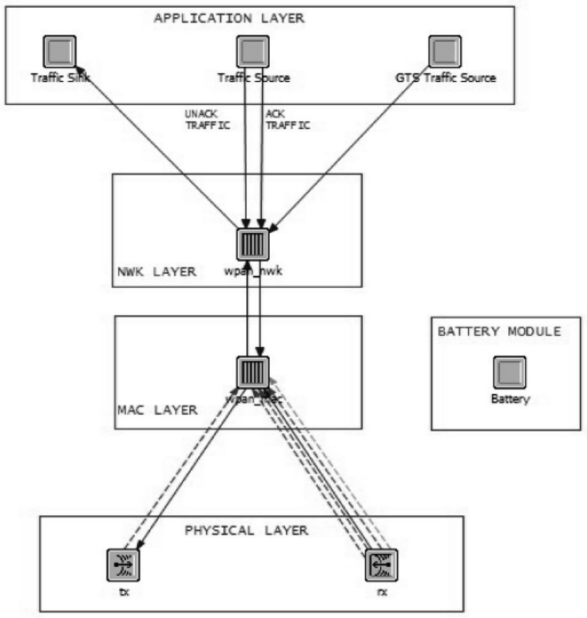

Figure 5: Upgraded OPEN-ZB simulation model

Crucial changes are introduced into the Physical Layer. In order to simulate the hidden node effect, radio range of transceivers needs to be limited. This is enabled through changes introduced in the Link Closure stage of the radio transceiver pipeline. For a given transmit power and path loss between the transmitter and receiver, power of the reception signal is calculated. If the signal power is lower than a receiver's sensitivity threshold, the radio link is not established. Path loss calculation is dependent on the distance between the transmitter and receiver and on terrain model, which is used in simulation. Value of the receiver's sensitivity threshold is chosen to be -85 dBm, according to the IEEE 802.15.4 standard specification. For standard transmit power level of 1mW (0dBm), transceiver radio range, with a free-space propagation model, is around 175m.

Further changes are introduced in Bit Error Rate Stage of the radio transceiver pipeline. Existing BER model used in OPNET network simulation tool is based on the claim that these two noise sources have the same influence on wireless transmission and that they can be treated as one common noise. Previous chapter shows that these noise sources need to be treated independently. If only a background noise is present in the communication channel, the appropriate BER curve from previous chapter is imported in the OPNET in the form of the table of the measured BER values. When both the background noise and the interference noise are present in communication channel, BER stage calculates a value of the bit error rate in accordance to parameters SIR and SNR. Data for such BER curve is imported in the OPNET in the form of a two-dimensional table of

the measured BER values. The obtained results for both cases are feds as output from Bit Error Rate Stage. In the Bit Error Allocation pipeline stage, the number of bit errors in a packet is determined. It is based on the values of the bit error rate end length of the packet in bits. Statistical wires, which connect Physical and Medium access layer, are used to carry values of the received power, SNIR, and bit errors for each packet. These values are used by MAC Layer to distinguish between valid and collided packets.

The MAC Layer is upgraded with Non-Beacon Enabled mode, which is missing in the original model. Now, the MAC layer is capable of operating in two modes, which is determined by the Beacon Order parameter. Implementation of the RTS/CTS Handshake mechanism starts with an introduction of a two new types of frames into the MAC layer. Structure of the MAC header and MAC footer is similar to other MAC frames. RTS and CTS frames are distinguished from other frame types with their use of the 3 bit long Frame Type subfield. If data transfer requires acknowledgement of the successful reception, value of the Ack Request subfield is set to 1, both for RTS and CTS frames, in order to inform all other nodes that Acknowledgment frame transmits right after data transmission. MAC payload is composed from two fields: Data length and Power indication field. Data length field is used to provide information about the length of the data frame, which is further transferred. This information is first sent by RTS frame to the recipient, which returns it with CTS frame in order to inform all the hidden nodes about the following data transmission. Power indication field is optional, and it can be used in a process of adjusting the level of transmitting power during data and acknowledgment frame transmission. When a device wants to initiate a transmission sequence it sends information about the current level of the power transmission with RTS frame. When a destination node receives this frame, it calculates path-loss based on the power level of the transmitted and the received signal. It adjusts its transmit power if a packet needs acknowledgment and sends information with CTS frame about the power level, which is low enough that data frame is successfully received. After the reception of the CTS frame message the source node adjusts its power level and starts data transmission.

Channel access mechanism is modified a bit in comparison to the CSMA/CA use in IEEE 802.15.4. When a node wants to transmit, it firstly turns on its radio and listens for the specified amount of time for eventual RTS or CTS frame. If such frame appears, the node goes to low-power sleep until current data transmission is finished. Then it wakes up and listens for a random backoff time, and if none RTS or CTS frames are received, it sends its own RTS frame to destination node. When a destination receives this frame it immediately replies with CTS frame, after which the data frame is sent by source node. Transmission sequence is finished by sending an optional acknowledgment frame, after which a new contention for medium access can begin.

Additional MAC commands for association are introduced and are used when new nodes join the network. Synchro module, used in the old model, is removed, since its role has been taken by a network layer, which controls the operation of the MAC layer through the use of service primitives. In the newly formed Network Layer, cluster-tree topology is supported. Star topology is implemented as a special case of cluster-tree topology, where network depth is set to the value of one. Mechanism of the network formation is implemented with default distributed address allocation to all nodes, which associate to the newly formed network.

4. Simulation results

Developed model of IEEE 802.15.4 wireless network, is used in simulations to demonstrate the effect of hidden node collisions of network performance. It is also used to analyze benefits of using the proposed RTS/CTS handshake mechanism to avoid hidden node collisions.

4.1 Influence of the hidden nodes on the network performance

Effect that hidden node collisions have on standard IEEE 802.15.4 CSMA/CA is demonstrated through two scenarios, with and without hidden nodes. Simulation scenarios are composed of eight End Devices, equidistant from PAN Coordinator, which create star topology. Medium Access layer operates in the Non-Beacon Enabled mode which uses un-slotted CSMA/CA medium access mechanism. Radio range of each device, under free-space propagation model is set to 175 m. In first simulation scenario, all End Devices that participate in the network can hear each other (distance between maximally separated End Devices is 160 m) and collisions due to the hidden node effect are avoided. In the second scenario, each End Device can hear four of the seven other End devices. This gives 42.9 % probability that each pair of the nodes is hidden from each other, which is close to the theoretical value of 41 % [4]. This scenario represents the near worst-case scenario because radio transmissions of the End Devices are received at PAN coordinator with the same power level, so each collision leads to a complete packet loss.

End Devices generate and transmit the acknowledged data frame whose destination is PAN coordinator. Data

frame has a constant application payload of 400 bits, which are extended with 216 bits of the packet overhead (64 bits added by the network layer, 104 bits added by the medium access layer and 48 bits added by the physical layer) and 88 bits long acknowledgment frame. Frames are generated with inter-arrival time according to Rayleigh probability density function. This distribution is chosen to simulate near-to-equidistant packets inter-arrival time, which simulates behavior of the real wireless sensor network.

In the first experiment, the amount of received application traffic (referred to as goodput) is monitored as a function of the generated application traffic for both simulation scenarios (with and without the hidden nodes). Application traffic represents an amount of application data per time unit (payload of the NWK frame), which is generated or received by a node:

$$AppLoad=M\,\lambda\,L \quad (1)$$

where *M* represents a number of nodes which generate application traffic, λ represents a number of generated packets in a unit of time (inversely proportional to packet inter-arrival time) and *L* represents the length of frame's data payload which is, in this case, equal to 400 bits.

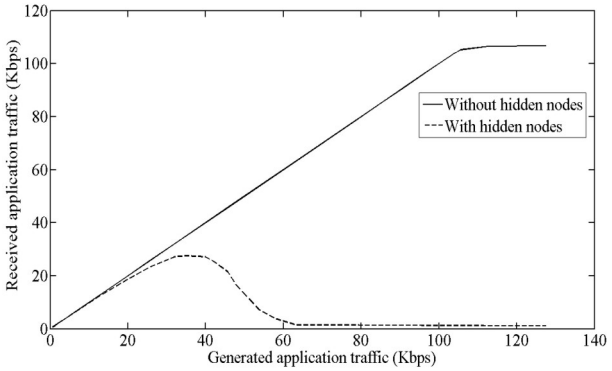

Figure 6: Received goodput as function of the generated application traffic

Presented results show that regular CSMA/CA without a presence of the hidden nodes performs very well, until it reaches its limits because of the channel saturation (Figure 6). In that situation, the amount of generated traffic is larger than what can be physically transmitted trough channel; hence the unsent packet can overflow transmission buffers. When a small amount of application traffic is generated in a presence of the hidden nodes, the hidden node collisions are not that frequent and most of the generated application traffic is received. As application traffic increases, a number of collisions increases too, which leads to severe degradation of the network performance, where network goodput is reduced almost four times when compared with the scenario without hidden nodes. The obtained results are similar to results presented in the paper [14].

One of the consequences of the hidden node problem is the loss of transmitted packets, due to collisions, which destroy their content, so they cannot be received. Ratio of the successful packet delivery is used to express the ratio between a number of the received and number of the generated data frames. Results for the ratio of the successful packet delivery (Figure 7), show that CSMA/CA, without a presence of the hidden stations, has 100\% success probability of the delivered packets. When it reaches its channel capacity limit, the number of generated packets is higher than the number of packets which can be transmitted. Packets, which cannot be transmitted, are dropped. In the presence of the hidden nodes, packets are lost for every hidden node collision and as traffic increases so does the number of collisions, which results in a higher number of lost packets.

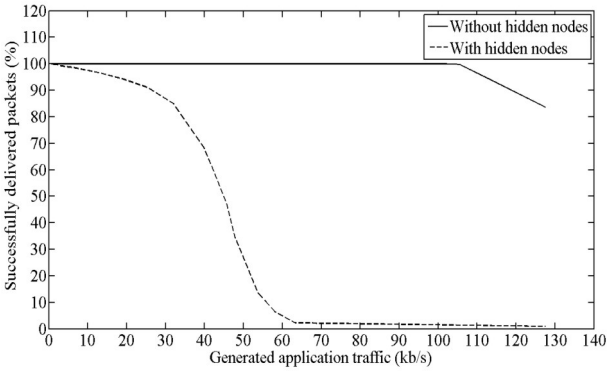

Figure 7: Ratio of the successfully delivered packets

Packet delivery time represents the time, which elapsed form its creation to the time when a packet is successfully received by destination node. This time is often called End-to-End delay. The measured results of the End-to-End Delay, for both scenarios, are presented in the Figure 8.

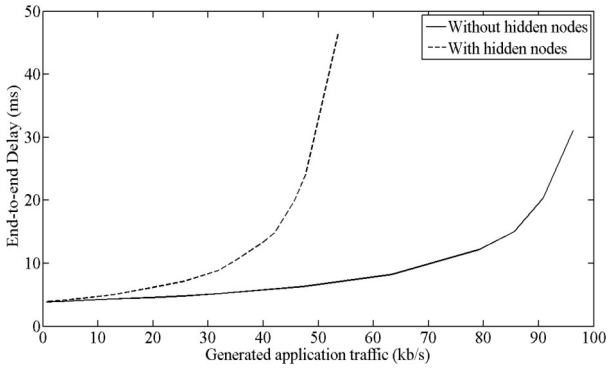

Figure 8: End-to-end delay of the transmitted packets

In regular CSMA/CA without a presence of the hidden stations, Packet delivery time gradually increases, because nodes need to wait until the end of the current transmission, to start their own transmission. As the amount of traffic increases, the average time also increases. In that case the node needs to wait until the channel is free. Packet collisions, caused by the hidden stations, require packet retransmissions, which additionally increases packet delivery time.

In both scenarios, when channel becomes saturated with traffic, packets cannot be transmitted and they are stored in queues or even dropped if the queues are full. This event dramatically increases end-to-end delay.

4.2 Network performances with hidden node avoidance mechanism

Hidden node avoidance mechanism presented in this paper, based on RTS/CTS handshake mechanism, is compared to a standard CSMA/CA medium access in the presence of hidden nodes. RTS/CTS handshake mechanism is added to CSMA/CA MAC, which is originally used in the IEEE 802.15.4. Unit backoff period of the modified medium access mechanism is increased from 20 to 92 symbols (from 80 to 368 bits) in order to accept one complete RTS/CTS sequence. This sequence is composed of one RTS and CTS frame, each 160 bit long, which are separated by a turn-around time, which is 12 symbols (48 bits) long. This modification prevents collisions during a contention phase.

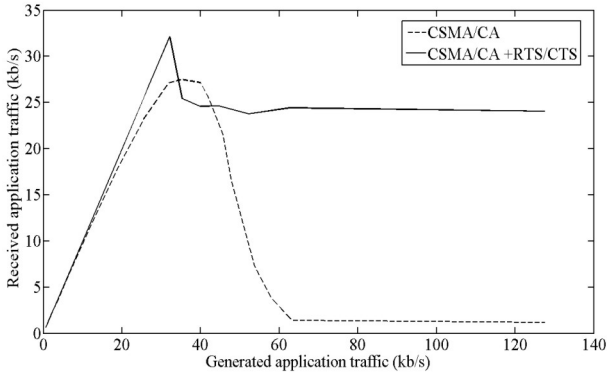

Figure 9: Application goodput with and without RTS/CTS mechanism

In the first experiment, the amount of the received application goodput is monitored, both for regular and CSMA/CA with the hidden node avoidance mechanism. Results presented in Figures 9 and 10 show that the hidden node avoidance mechanism works as expected and that all the hidden node collisions are avoided and that there is not any packet loss. The proposed hidden node problem avoidance mechanism reaches its maximum output, which is three times lower than the standard CSMA/CA, without an influence of the hidden stations. The main reason for this reduced capacity is in high packet overhead, which increases by RTS and CTS frames, when compared to the standard transmission sequence.

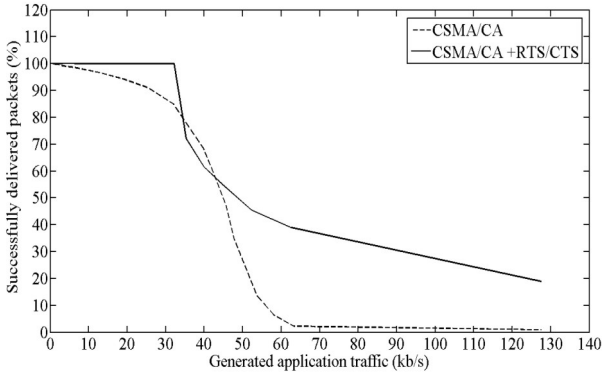

Figure 10: Ratio of the successfully delivered packets with and without RTS/CTS mechanism

In the last experiment, the end-to-end delay of the standard and modified CSMA/CA is compared. The proposed hidden node avoidance mechanism almost has twice the longer end-to-end delay, in comparison to the original CSMA/CA used in the IEEE 802.15.4 (Figure 11). The reason for a longer end-to-end delay is in much longer transmission sequence, which requires transmission of the additional RTS and CTS frames, prior to data transmission. Furthermore, unit of the backoff period increases 4.5 times, which additionally increases the overall packet delay.

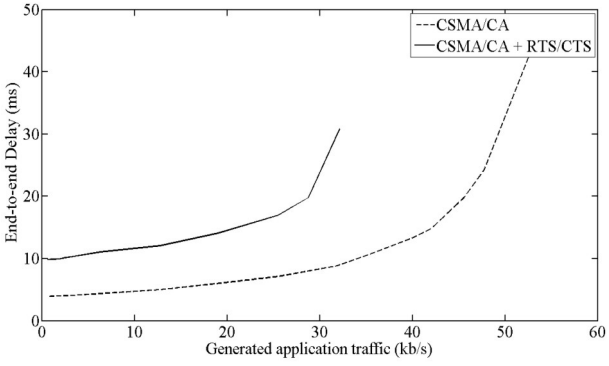

Figure 11: End-to-end delay with and without RTS/CTS mechanism

5. Conclusion

The hidden node problem represents a real threat to any type of wireless communication. This paper presents an effect that hidden node collisions have on IEEE 802.15.4 networks, which originally do not offer any kind of protection against this problem. The results show a severe degradation of the network performance

caused by the hidden node collisions, which drastically reduces useful application's goodput and increases in number of lost packets and packet delivery time.
The proposed RTS/CTS handshake mechanism for IEEE 802.15.4 networks enables avoidance of hidden node collisions. Network goodput is increased when compared to standard CSMA/CA, especially in high traffic conditions. Also, packet loss is much lower with the proposed hidden avoidance mechanism, compared to a standard CSMA/CA medium access in presence of hidden nodes. The main drawback of this mechanism is its high packet overhead, which is caused through addition of RTS and CTS frames to data transmission sequence, which increases end-to-end delay. Based on the results, it can be conclude that RTS/CTS handshake mechanism can be used as the hidden node problem avoidance mechanism in the IEEE 802.15.4 wireless networks.

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Two-Port Piezoelectric Silicon Carbide MEMS Cantilever Resonator

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Abstract: A two-port silicon carbide single-clamped beam (cantilever) microelectromechanical system (MEMS) resonant device actuated piezoelectrically and sensed piezoelectrically has been designed, fabricated and tested. Lead zirconium titanate (PZT) has been used as active material to implement the piezoelectric actuator and sensor. Piezoelectric electrodes have been placed on the top of the single 3C-SiC beam forming a flexural-mode resonator. Operation has been demonstrated with two-port measurements of the transmission frequency response. The 250-µm long device resonates at 371 kHz with Q factor of 385 in atmospheric conditions. The tuning of the resonant frequency has been demonstrated by applying DC bias voltage in the range 0 V – 10 V and frequency tuning range of 1025 ppm has been achieved.

Key words: Silicon carbide, MEMS, resonator, cantilever, piezoelectric actuation, piezoelectric sensing, frequency tuning

Dvovhodni piezoelektrični MEMS resonator na ročico iz silicijevega karbida

Povzetek: Načrtovan, izdelan in testiran je bil, piezoelektrično vzbujan in merjen, dvovhodni mikroelektromehanski (MEMS) resonatorski sistem z ročko. Za aktuator in senzor je bil uporabljen svinčev cirkonijev titanat (PZT). Piezoelektrične elektrode so nameščene na vrh enojne 3C-SiC gredi, ki tvori upogibni resonator. Delovanje je demonstrirano z dvovhodnimi meritvami prenosa odzivne frekvence. pod atmosferskimi pogoji 250-µm dolg element resonira s frekvenco 371 kHz in Q faktorjem 385. Uglaševanje resonančne frekvence je predstavljeno s spreminjanjem DC napetosti od 0 – 10 V, pri čemer je bilo območje uglaševanja frekvence doseglo 1025 ppm.

Ključne besede: silicijev karbid, MEMS, resonator, ročica, piezoelektrično vzbujanje, piezoelektrični senzor, uglaševanje frekvence

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1. Introduction

Microelectromechanical system (MEMS) resonant devices are being increasingly considered for replacing filter [1] components and quartz crystal [2] currently used in communication systems. Relatively small dimensions and low operating voltages enable MEMS resonators to solve power consumption and miniaturisation issues in portable wireless devices [2, 3]. Selection of the material plays a very important role for realization of high efficiency MEMS resonant devices. Silicon carbide (SiC), a wide band-gap semiconductor, possesses outstanding mechanical properties that make SiC the most promising material for MEMS resonator applications [4]. SiC exhibits a large Young's modulus to mass density ratio and the resonant frequency of a SiC resonator can be three times higher than its silicon (Si) equivalent [5]. 3C-SiC has emerged as the dominant polytype for MEMS applications as it can be synthesised on Si wafers, potentially leading to large-scale production. Other polytypes such as 4H-SiC and 6H-SiC form at temperatures above the melting point of Si [4].

Electrical actuation and sensing of resonator mechanical vibration is essential requirement for the practical implementation of MEMS resonators. Electrostatic and piezoelectric transductions have emerged as the leading techniques and both have been widely implemented in Si and SiO_2 resonators [3,6]. However, the complex fabrication process in electrostatic transduction associated with achieving an electrode-to-resonator gap

spacing in the nanometric scale motivates the use of piezoelectric transduction. Recently, 3C-SiC has been integrated with lead-zirconium-titanate (PZT) ports allowing electrical actuation [7] and sensing [8-10] of flexural-mode 3C-SiC resonators.

The overall structural design plays an important role in achieving expected performance of flexural-mode resonators. Even though single-clamped beam (cantilever) resonators exhibit a resonant frequency about 6 times lower than double-clamped beam (bridge) and about 10 times lower than circular membrane (ring) resonators [11], they are characterized by the largest vibration amplitude, which is essential for piezoelectric sensing of the vertical resonant vibration. In this paper, piezoelectric sensing of a 3C-SiC cantilever resonator that is actuated piezoelectrically has been presented. The device has been designed as a two-port single-clamped vertical-mode beam resonator with a top piezoelectric actuator (input-port) and a sensor (output-port) made of platinum (Pt) and PZT (Figure 1). The resonant frequency has been determined by two-port measurements of the resonator's transmission frequency response. In addition, resonant frequency tuning has been demonstrated by applying DC bias voltages.

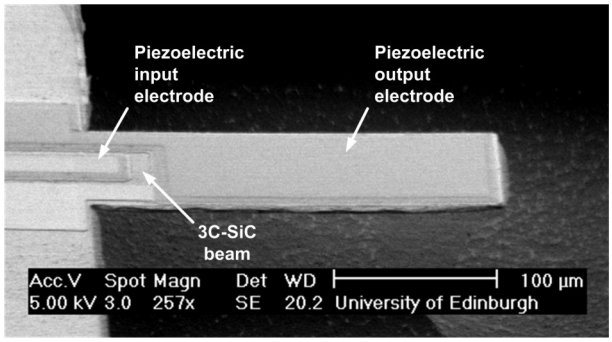

Figure 1: Scanning electron micrograph of the fabricated 3C-SiC single-clamped beam (cantilever) resonant device with input and output piezoelectric electrodes placed on the top of the beam.

2. Piezoelectric transduction and device operation

Piezoelectric effect refers to the property of a material to become electrically polarized when subjected to mechanical stress and conversely, to mechanically deform under application of electric field. Piezoelectricity can be used as a transduction technique for electrically inducing (actuating) or detecting (sensing) a mechanical deformation of a structure. The structure of the presented device consists of two dominant layers, a piezoelectric layer positioned on the top of an elastic 3C-SiC layer. The shape of the 3C-SiC layer is the single-clamped beam (i.e. cantilever). When an electric field is applied to the actuating piezoelectric layer (input electrode) of the device, the induced expansion/compression of the piezoelectric layer results in a shear stress that is transformed in bending moment, and consequently the beam deflects in the vertical direction. If an alternating electric field is applied with a frequency matching the structure's natural frequency, the resonator's active body (beam) is driven into resonance.

Due to the reciprocity of the piezoelectric effect, the beam deflection in the vertical direction can be sensed by detecting the voltage difference as a result of the change in the electric field induced by the mechanical strain. In particular, when the resonator's beam is vibrating, an oscillating voltage with a frequency equal to the frequency of the mechanical oscillations can be detected across the piezoelectric material of the sensing (output) electrode.

3. Experimental details

3.1 Device design

The device has been designed as a two-port single-clamped vertical-mode beam resonator with piezoelectric electrodes placed on the top of the 3C-SiC beam. As the piezoelectric material, lead zirconium titanate (PZT) has been used because of its high piezoelectric coefficient [12]. Platinum (Pt) has been used as top and bottom metal contacts between which PZT has been sandwiched to form the actuating (input) and sensing (output) electrode. The schematic of the designed device together with the beam dimensions is shown in Figure 2. The resonator's beam length is 250 µm and beam width is 100 µm. The input electrode has been designed with a length of 25 µm (1/10 of the beam length) and with a width of 35 µm. The strong electromechanical coupling offered by piezoelectric transduction [6] allows induction of relatively large vibration amplitude by positioning actuation electrode close to the root of the beam, giving the possibility of designing additional sensing electrode on the remaining part of the single beam. In order to maximize the electrical output, the sensing piezoelectric electrode covers most of the surface of the beam.

3.2 Fabrication

The process for the device fabrication starts with a 2 µm thick 3C-SiC epilayer deposition on 4-inch Si wafer [13]. A 100 nm thick silicon dioxide (SiO_2) passivation layer has been grown thermally. On top of the SiO_2, a

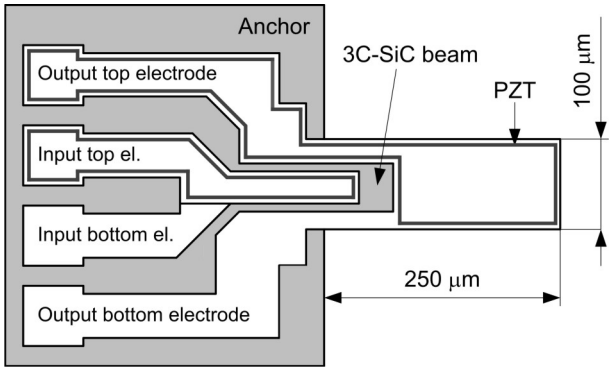

Figure 2: Schematic of the designed device with the beam dimensions.

titanium (Ti) layer (10 nm) has been deposited as an adhesion layer between Pt layer and substrate. The Pt/PZT/Pt stack has been deposited with thicknesses of 100/500/100 nm [14], respectively. Once all layers have been deposited, the electrode stack has been patterned photolithographically. The top Pt and bottom Pt/Ti layers have been dry etched [7] whereas PZT has been wet etched [15]. After depositing a 3 μm thick SiO_2 layer to be used for masking the 3C-SiC layer, the beam shape has been patterned photolithographically and the exposed SiO_2 has been dry etched. The 3C-SiC beam has been plasma etched and released using a SF_6/O_2 gas mixture [16]. Afterwards, the residues of the masking SiO_2 left on the 3C-SiC surface have been removed in a CF_4/H_2 plasma. The detailed fabrication process for the Pt/PZT/Pt/SiC beams has been reported elsewhere [7]. The schematic side view of the fabricated device including the layers thicknesses is shown in Figure 3.

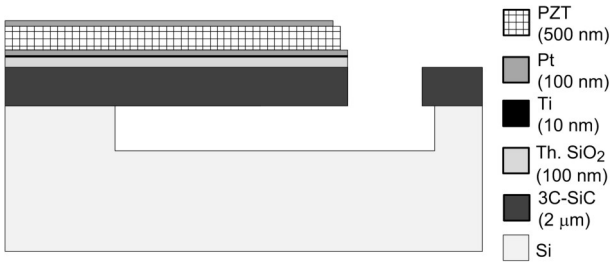

Figure 3: Schematic side view of the fabricated device.

3.3 Measurement setup

Two-port measurements of the fabricated device have been performed with an HP 8753C vector network analyzer. Signal-ground (SG) probes have been used and full two-port calibration (short, open, load, and through - SOLT) has been performed before starting the measurements. The device has been tested without any signal amplification or impedance matching (Figure 4). The bottom electrodes of the device under test have been grounded, while each of the two top electrodes has been used for either piezoelectrical actuation or sensing. In order to perform the tuning of the resonant frequency, the actuating AC signal applied with the network analyzer has been superimposed to a DC signal provided by an external stabilized DC power supply. All measurements have been performed at atmospheric pressure.

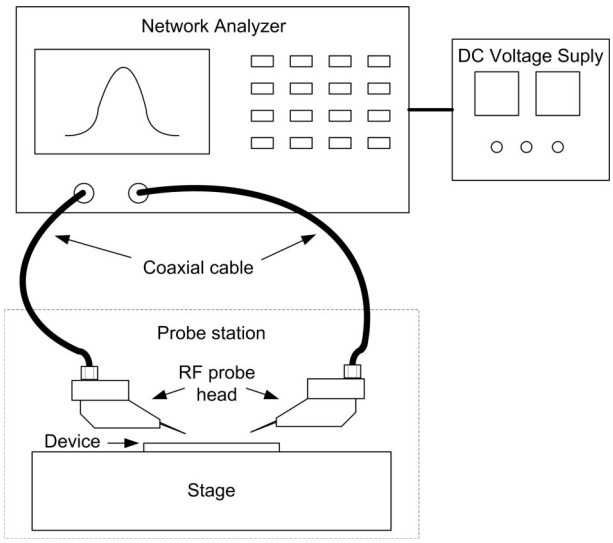

Figure 4: Schematic of the measurement setup.

4. Results and discussion

4.1 Resonant frequency detection

Measured transmission frequency response, both magnitude and phase, of the device is shown in Figure 5. The power of the input signal used has been set at 10 dBm and frequency swept from 367 kHz to 375 kHz. No DC bias voltage has been used for this measurement. The resonant frequency has been measured to be 371.174 kHz. The maximum resolution error of the resonant frequency measurements has been calculated to be 13 ppm. The phase change between output and input signal has been measured to be about 100°. Quality (Q) factor defined as ratio of the resonant frequency and the bandwidth of 3dB transmission magnitude drop has been calculated to be 385. Measurements performed in vacuum should give higher values for the Q factor [17]. Furthermore, the insertion loss should be additionally reduced under appropriate impedance matched conditions between the device input/output and the 50 Ω load impedances of the network analyzer.

4.2 DC voltage tuning

In piezoelectric MEMS resonators such as the device presented in this paper (Figure 1), the piezoelectric effect can be used for driving the structure into reso-

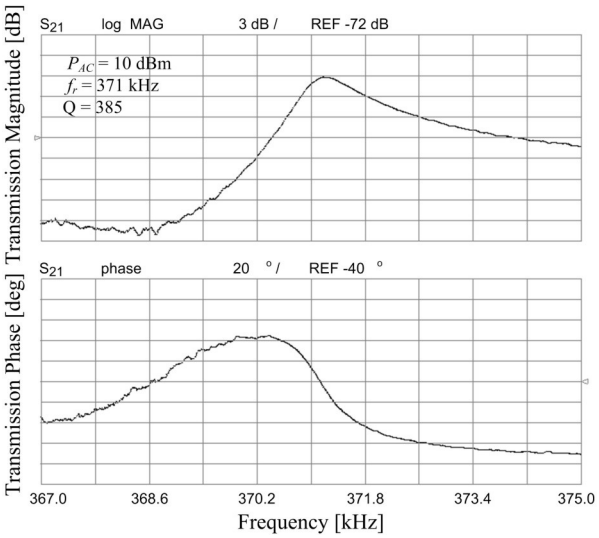

Figure 5: Two-port measurements of the transmission frequency response of the 250 µm-long device.

nance and at the same time for tuning the resonant frequency by applying a superimposed DC bias voltage at the input [18, 10]. Figure 6a shows the transmission magnitude plots for different values of DC bias voltage. A constant input AC signal power of 10 dBm has been applied to the input electrode while the DC bias voltage has been swept in the range 2 V - 8 V with steps of 2 V. The resonant frequency has been shown to increase linearly as the DC bias voltage increases. Figure 6b shows the resonant frequency shift measured at different DC bias voltages with AC input power equal to 10 dBm. As the DC bias increases from 0 V to 10 V, the resonant frequency shift increases by 1025 ppm (i.e. the resonant frequency increases by 380 Hz).

The increase in resonant frequency obtained when increasing the DC bias voltage is attributed to the influence of the electric field on the stress and mass density of the piezoelectric active layer [19, 10]. As the DC bias voltage increases, the stress within the structure induced by the piezoelectric layer increases thus influencing the structure's resonant frequency [10]. Since the resonant frequency is dominated by the 3C-SiC layer and its internal stress, the frequency tuning capability of our device is relatively small comparing to other piezoelectric resonators [18, 20]. Wider frequency tuning can be obtained by increasing the input electrode length [10]. DC bias voltage adjustments can be used to compensate for a frequency shift caused by fabrication processes and operating conditions.

5. Conclusions

The design, fabrication and operation of a novel two-port 3C-SiC cantilever resonant device actuated piezo-

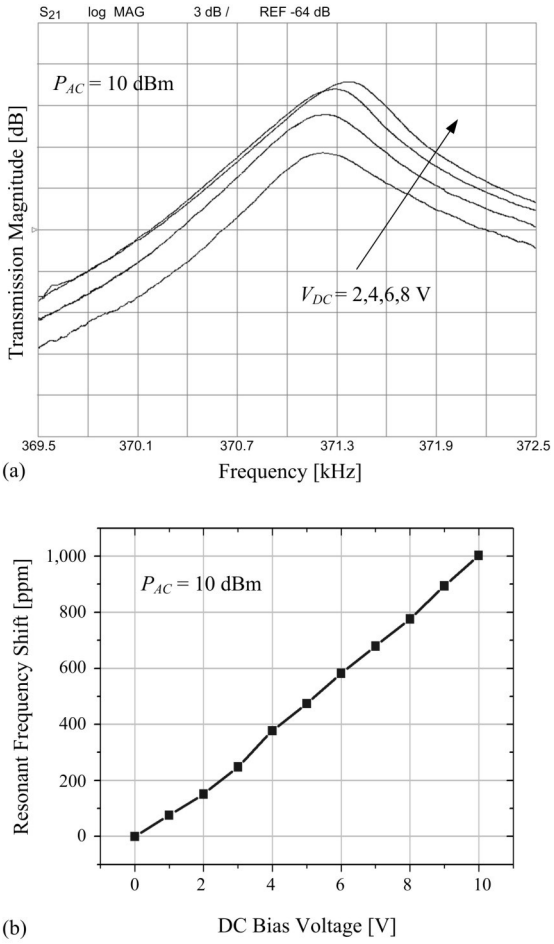

Figure 6: Transmission magnitude plots for different DC voltages (a) and measured resonant frequency shift versus DC bias voltage (b).

electrically and sensed piezoelectrically has been presented. PZT has been used as the piezoelectric material and sandwiched between Pt layers to form transducer electrodes that have been placed on the top of the 3C-SiC beam. From the transmission frequency response measurements, it has been shown that the resonant frequency of the presented device measured at atmospheric pressure is 371 kHz with a Q factor of 385. For the device operation, a DC bias voltage is not required and therefore, the device is suitable for low-power timing and frequency control applications. Resonant frequency tuning range of 1025 ppm is demonstrated by applying DC bias voltages in the range 0 V - 10 V. This tuning method can be used to overcome fabrication tolerances and reliability issues.

Acknowledgments

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Impact of the Excess Base Current and the Emitter Injection Efficiency on Radiation Tolerance of a Vertical PNP Power Transistor in a Voltage Regulator

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Abstract: Examinations of the minimum dropout voltage with a high load current demonstrated proper operation of voltage regulators L4940V5 for gamma radiation doses of up to 500 Gy(SiO2). An increase in the minimum dropout voltage of approximately 0.5 V was measured. Due to the relatively small dissipation, the thermal protection circuit did not significantly affect the operation of the voltage regulator L4940V5. According to the line regulation characteristics, obtained after absorption of a total ionising dose of 300 Gy(SiO2), the voltage reference was negligibly affected by the irradiation. Variations in the line regulation characteristics after irradiation were less than 1% in comparison with initial values. Despite the operation with a load current of 400 mA, the serial PNP transistor emitter injection efficiency remained high after irradiation, with an estimated value greater than 0.93. The interdigitated structure of the serial transistor's base-emitter junction led to an abrupt increase of the surface recombination in a gamma radiation environment, followed by a great rise in the excess base current. This effect was enabled by the feedback circuit reaction and its influence on a driver transistor, affecting the sharp increase of the serial transistor's base current. On the other hand, the antisaturation circuit prevented a rise in the total voltage regulator's quiescent current above the limit of approximately 40 mA.

Key words: vertical PNP transistor, excess base current, collector-emitter dropout voltage, voltage regulator, emitter injection efficiency, ionising radiation.

Vpliv presežnega baznega toka in izkoristek injekcije emitorja na tolerance radiacije vertikalnega PNP močnostnega tranzistorja v napetostnem regulatorju

Povzetek: Raziskave najnižjega padca napetosti pri visokem bremenskem toku so pokazale pravilno delovanje napetostnih regulatorjev L4940V5 za gama radiacijske doze do 500 Gy(SiO2). Izmerjeno je bilo povišanje minimalnega padca napetosti za okoli 0.5 V. Zaradi relativno majhne disipacije temično zaščitno vezje ni imelo pomembnega vpliva na napetostni regulator L4940V5. Glede na regulacijske karakteristike po absorpciji ionizirajočega sevanja v višini 300 Gy(SiO2) je bil vpliv sevanja na referenčna napetost zanemarljiv. Variacije vhodnih regulacijskih karakteristik po obsevanju so bile manjše od 1 %. Pri bremenskem toku 400 mA je izkoristek injekcije emitorja serijskega PNP tranzistorja ostal visok tudi po obsevanju in je po oceni znašal 0.93. Prepletena struktura bazno-emitorskega spoja serijskega tranzistorja je vodila v nenadno povečanje površinskih rekombinacij v okolju gama žarkov, kar je povzročilo hitro in veliko prekoračitev baznega toka. Ta efekt je posledica povratne vezave in njenega vpliva na gonilni tranzistor, kar povzroča strm porast baznega toka serijskega tranzistorja. Po drugi strani antisaturacijsko vezje preprečuje porast toka nad 40 mA.

Ključne besede: vertikalni PNP tranzistor, presežni bazni tok, padec napetosti kolektor - emitor, napetostni regulator, izkoristek injekcije emitorja, ionizacijsko sevanje.

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1. Introduction

Recent advances in aerospace applications, especially in the development of satellite electronic devices, have attracted much attention to the operation of electronic devices in the radiation environment [1, 2]. Most of the efforts in analysing the radiation effects have been dedicated to the MOSFET-based electronic components [3, 4] necessary for the operation of these complex technical systems, such as microprocessors [3, 5], memories [3], switching power supplies [4], logical circuits [1, 6] and discrete transistors [7, 8], including electronic dosimeters [9]. Nevertheless, much attention was also dedicated to the influence of the radiation environment on electronic equipment based on bipolar transistors [2, 6], such as operational amplifiers [10–12], comparators [13, 14], and, finally, linear voltage regulators [15–17]. Research into the radiation effects in linear integrated circuits with bipolar transistors attracted much attention during the last two decades. After the discovery of enhanced-low-dose-rate sensitivity (ELDRS) in bipolar transistors [2, 18], examination of linear bipolar integrated circuits in the radiation environment became a highly interesting topic [19–21].

Beside operational amplifiers and comparators, examinations of the low-dropout voltage regulators became particularly frequent [15–17, 22, 23]. Yet, owing to the very high prices of radiation tolerant integrated circuits (ICs), requirements were imposed for the use of commercial-off-the-shelf (COTS) electronic components in aerospace and nuclear applications [4]. According to these requirements, an effort was made to detect appropriate commercial low-dropout voltage regulators suitable for use in the radiation environment. Moreover, detection of the appropriate radiation tolerant commercial technological processes, as well as definition of their preferable characteristics, was undertaken.

Gain degradation in irradiated bipolar transistors can be a significant problem, particularly in linear integrated circuits. Ionizing radiation causes the base current in bipolar transistors to increase, due to the presence of net positive charge in the oxides covering sensitive device areas and increases in surface recombination velocity [1]. When bipolar integrated circuits are exposed to ionizing radiation in space, there are two primary failure mechanisms: (1) leakage current caused by trapped positive charge in the field oxide or (2) reduction of the current gain of individual transistors [1]. Digital circuits are usually designed to be relatively insensitive to variations in current gain, so total-dose failures in digital ICs are primarily isolation-related. However, for most bipolar technologies that are used in linear integrated circuits, the total-dose failure mechanism is reduction of the current gain [1]. The forward emitter current gain degradation in bipolar transistors is caused by the interactive effects of radiation-induced charge in the oxide and increased surface recombination velocity. The charge in the oxide increases the surface potential, causing the recombination rate near the emitter-base junction of NPN transistors to increase as the electron and hole concentrations become comparable (crossover point) [1]. When the charge in the oxide is sufficient to move the recombination peak beneath the surface of the base region, additional increases in base current with total dose are quite small. Vertical PNP transistors are usually radiation tolerant because the net positive charge in the oxide accumulates the base region. Since the emitter doping in vertical PNP transistors is large compared to the base doping in NPN transistors, the effects of oxide charge on surface recombination are much less. However, lateral PNP transistors can be quite radiation sensitive because of the current-flow path near the surface [1].

A recent article on the characteristics of commercial-off-the-shelf low-dropout voltage regulators "STMicroelectronics"® L4940V5 dealt with the analysis of the complex response of irradiated integrated circuits with a negative feedback loop in the gamma radiation field [24]. Besides gamma radiation, the isolated collector vertical PNP power transistor was also seriously affected by the load current and input voltage [24–26]. The increase in load current had a major effect on the reduction of the serial transistor's current gain. Nevertheless, owing to the device's tests with a moderate load, the impact of the radiation effects in the emitter area on the serial transistor's radiation hardness could not be determined, since the power transistor certainly operated without emitter crowding. Moreover, the magnitude of the emitter injection efficiency and the influence of the particular integrated circuit's functional blocks on negative feedback reaction remained ambiguous [25]. Therefore, tests of minimum dropout voltage with high load current had to be carried out in order to acquire complete data on the examined circuit's radiation response.

Since the voltage regulators L4940V5, primarily designed for automotive applications, long ago showed significant radiation hardness [27], a new series of experiments in the radiation environment were undertaken on these integrated circuits. The primary hypothesis was that the main cause of the L4940V5 voltage regulator's high radiation hardness was the small degradation of the serial vertical PNP transistor's forward emitter current gain (β), which was mainly due to the shift of current flow from the surface towards the substrate [26, 27]. However, recent experiments, relying on examinations of the voltage regulator's quiescent current, together with the maximum output current, highlighted

the increase of the serial transistor's base current and consequently, the significant decrease of its forward emitter current gain [26]. This led to the conclusion that the primary influence on the previously perceived high radiation tolerance of the L4940V5 voltage regulator is the control circuit and not the serial PNP transistor. Nevertheless, as already mentioned, it was not clear what primarily affected the rise of the power vertical PNP transistor's base current; whether it was the control circuit (negative feedback circuit reaction, activation of some protective parts of the integrated circuit) or degradation of the serial power transistor itself. A further difficulty for the necessary analysis was that it was not possible to obtain even the simplest schematic circuit diagrams of the L4940V5 voltage regulator. Therefore, defining an experiment that would enable analysis of both the serial PNP transistor and elementary blocks of the voltage regulator's control circuit, in order to obtain data on the most radiation-sensitive parts of the L4940V5 voltage regulator, without the need to unseal the integrated circuits, was a problem.

In this paper, the results presented relate to the change in the serial transistor's minimum dropout voltage, the excess base current and the forward emitter current gain in the heavily loaded voltage regulators L4940V5, operating in the γ radiation field. Also, the line regulation characteristics have been presented in order to complete the analysis of the voltage regulator's critical mode of operation, with low input voltages and high output currents.

2. Materials and methods

Integrated 5-volt positive voltage regulators L4940V5 were tested in the Vinča Institute of Nuclear Sciences, Belgrade, Serbia, in the Metrology-dosimetric Laboratory. Circuits L4940V5 were from the batch WKOOGO 408, made by "STMicroelectronics"® in China [27, 28].

As a source of γ-radiation, the ^{60}Co was used and it was situated in a device for the realisation of the γ-field, IRPIK-B. The accepted mean energy of γ-photons is E_γ = 1.25 MeV. The exposition doses are measured using a cavity ionising chamber "Dosimentor"® PTW M23361, with a volume of $3 \cdot 10^{-5}$ m^3. With the cavity ionising chamber, the reader DI4 was used [27].

Devices had been irradiated until the predetermined total doses were reached. Devices in the γ-radiation field were exposed to a total dose of 500 Gy, with a dose rate of 4 cGy(SiO_2)/s [26]. All measurements were performed within half an hour after the exposure.

Current and voltage measurements were carried out with laboratory instruments "Fluke"® 8050A and "Hewlett-Packard"® 3466A. All measurements and the irradiation of the components were performed at a room temperature of 20°C.

The main values used for detection of the degradation of the voltage regulator due to the exposure to ionising radiation were the serial transistor's forward emitter current gain and collector-emitter (dropout) voltage. The electrical values measured were the voltage regulator's input and output voltages and quiescent current. During the irradiation, the biased devices examined were supplied with the same input voltage, 8 V, while the load currents had three different values: 1 mA, 100 mA and 500 mA. The fourth group of irradiated devices comprised unbiased voltage regulators, without input supply voltage [24, 26].

Examination of the change in the collector-emitter (dropout) voltage on the serial transistor was performed as follows: the input voltage was increased until the output voltage dropped to 4.9 V, for a constant output current of 400 mA [27]. The difference between the input and output voltages represents the dropout voltage on the serial transistor (QS in Fig. 1) for the corresponding current.

The next step was the measurement of the output voltage and the quiescent current for an unloaded voltage regulator, with input voltage equal to the value measured on the device loaded with 400 mA, as low as necessary to reduce the output voltage to 4.9 V. In voltage regulators with the serial PNP power transistor, a quiescent current (I_q) represents a sum of the control circuit's internal consumption current and the serial transistor's base current [26]. Quiescent current for an unloaded voltage regulator (I_{q0}), with constant input voltage, was assumed to be approximately equal to the value of the loaded voltage regulator's internal consumption. Subtraction of the unloaded circuit's quiescent current from a quiescent current of devices loaded with 400 mA, for the same input voltages, gave the value of the serial transistor's base current [29].

$$I_b = I_q\Big|_{(I_C = I_{load})} - I_{q_0}\Big|_{(I_C = 0)} \quad (1)$$

The values of the quiescent currents for the unloaded voltage regulators (I_{q0}) were obtained during examination of the samples with disconnected load, with the same input voltage as previously recorded on the same devices operating with a load current of 400 mA.

The serial transistor's forward emitter current gain was determined as the quotient of the voltage regulator's output current (that is, the serial transistor's collector

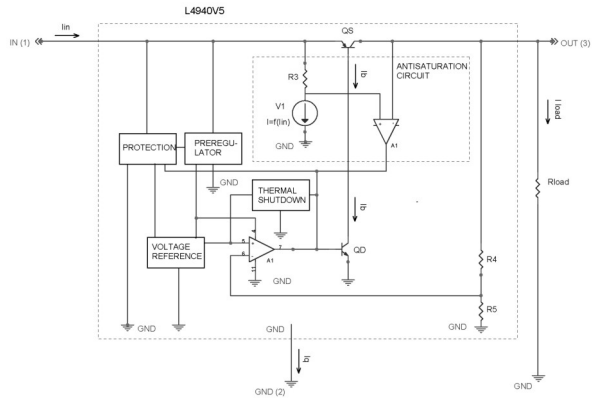

Figure 1: Schematic block diagram of the L4940V5 voltage regulator.

current on the variable resistor) and the calculated value of the base current [26, 29]:

$$\beta = \frac{\partial I_c}{\partial I_b} \approx \frac{I_c}{I_b} \tag{2}$$

During irradiation, heat sinks of the specific thermal resistance of 14 K/W were attached to the tested samples of voltage regulators [29]. When the thermal resistance junction – case (in this case the standard integrated circuit's TO-220 case equals 3 K/W) was included in the calculation, the overall thermal resistance junction – ambient of the voltage regulator L4940V5 would not exceed 17 K/W. The manufacturer declares that the usual dropout voltage is about 0.5 V with a load current of 1.5 A [28], and, also, that the maximum power dissipation is nearly 7.3 W for a heat sink of 14 K/W and ambient temperature equal to 25°C [28] (calculated for the total thermal resistance of 17 K/W and the maximum junction temperature of 150°C).

All the above-mentioned measurements were performed in joint experiments on voltage regulators, focused on maximum output current [26], minimum dropout voltage for moderately loaded devices [24, 25] and, in this paper, dropout voltage for heavily loaded samples. All three kinds of measurements were performed in the same conditions, in the order specified in this paragraph. According to the guidelines found in literature [30, 31] and previously reported uncertainties of measurement [29], the calculated combined uncertainty of measurement for the implemented experimental procedure was approximately 0.6% [25].

Besides the examination of the minimum dropout voltage and related parameters, the results of the examination of the line regulation characteristics in the voltage regulators L4940V5 were also presented. In this experiment, values of the output voltage were measured for constant output current (0A, 100 mA, 300 mA, 500 mA and 700 mA), while the input voltage had values of up to 15 V (specifically 6.5V, 8V, 10V, 12V and 15V) [27]. The resulting diagrams represent the difference between values of the output voltage recorded prior to irradiation and after exposure to the total dose of gamma radiation of 300 Gy(SiO_2). The line regulation characteristics were obtained during the primary examinations of the low-dropout voltage regulators L4940V5, so the ionising radiation dose rate differs slightly, having a value of 5.5 cGy(SiO_2)/s [27]. All the other measurement equipment, sources of radiation, dosimetry and experimental set-up were the same.

The block diagram of voltage regulator L4940V5, according to the data published in the literature [28, 32], is presented in Fig. 1. More details about the experiment, integrated circuits and implemented technological processes are provided in the references [24–29, 32].

3. Results and discussion

Figs. 2–7 present the changes in the serial transistor's dropout voltage and the forward emitter current gain for the voltage regulators L4940V5, for a constant load current of 400 mA and output voltage of 4.9 V. The total dropout voltage rise (*i.e.*, increase of the collector – emitter voltage of the serial transistor QS, Fig. 1) following the gamma radiation absorption of 500 Gy(SiO_2) was approximately 0.5–0.6 V (Fig. 2). Initial values of the measured minimum dropout voltage, obtained using precise laboratory sources and for a load current of 400 mA, were approximately 0.23 V. On the other hand, simultaneously with the moderate rise of the serial transistor's dropout voltage, an abrupt decrease of the serial transistor's forward emitter current gain (β; Fig. 3) was recorded. Some important questions needed answers in the attempted research: is the perceived decrease of the serial transistor's current gain a consequence of the feedback circuit reaction, only affecting the serial transistor's operation point without a real sharp decrease of its forward emitter current gain? Either the main cause of the voltage regulator's reaction may be sudden activation of some of the protective circuits, such as the thermal shutdown or antisaturation circuit. Or the serial transistor itself primarily affected the complete integrated circuit's operation owing to the change of operation mode or sudden decrease of the emitter injection efficiency.

A standard procedure to obtain answers to the questions posed could be to implement a simulation model for the integrated circuit. However, unfortunately, the manufacturer did not provide any detailed schematic

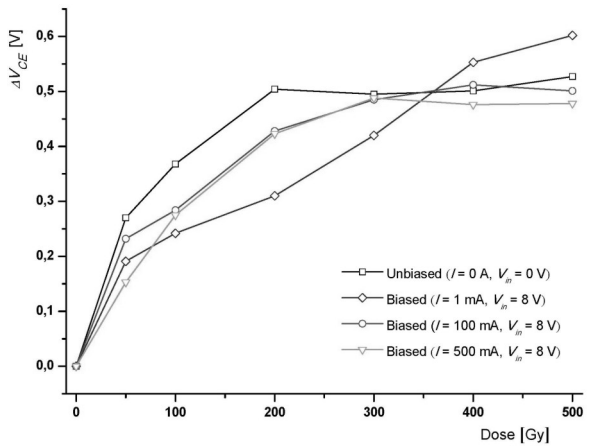

Figure 2: Change in the mean serial transistor's minimum dropout voltage in the voltage regulator L4940V5 under the influence of γ-radiation (V_{out} = 4.9 V, I_{out} = 400 mA).

circuit diagram either in the datasheet [28] or in articles [32] or patents [33] regarding the voltage regulator L4940V5. Beside the simple block diagram [28], presented also in Fig. 1, some details were provided about the antisaturation circuit [32], but this was not nearly enough to create a detailed simulation model. Therefore, analysis of the primary mechanisms of the degradation of the L4940V5 voltage regulator would have to rely on the available experimental data, both as presented here and as previously reported [26, 27, 29].

In the paper related to the analysis of the L4940V5 voltage regulator's maximum output current, it was perceived that, despite the integrated circuit's significant radiation hardness, its vertical serial power transistor was more sensitive than expected [26]. The main cause of the sharp rise in the serial transistor's base current was identified as the interdigitated structure of the isolated collector vertical PNP transistor. This structure affected the great rise in the serial transistor's base current as a consequence of the increased surface recombination processes along the base-emitter junction, due to its high perimeter-to-area ratio [26]. Increase in the injection level leads to decrease of the surface recombination contribution and decreased degradation of the forward emitter current gain. The results obtained for the heavily loaded voltage regulators, shown in Fig. 3, also lead to the conclusion that the dominant influence on the radiation response of the moderately loaded devices has the negative feedback reaction [24].

The previous paper examined the minimum dropout voltage of the L4940V5 voltage regulator with a constant load current of 100 mA [24]. Compared with the previously noticed decline in the forward emitter current gain by 30–80 times [24], now the registered decline of the current gain was no greater than 6–9 times (from 70–105 down to approximately 12; Fig. 3). A nearly sevenfold increase in the base current and its saturation on the level of approximately 35 mA (Fig. 7) also leads to the hypothesis that the primary cause of the seemingly sharp decline of the serial transistor's forward emitter current gain was the very strong influence of the control circuit, primarily by the change in the serial transistor's base current. The interpretation of the observed phenomenon is the same as in the case of moderately loaded devices: a sevenfold decline in the forward emitter current gain of the PNP power transistor (for the same values of the base-emitter voltage) did not occur, but the negative feedback reaction caused a shift in the voltage regulator's operating point on the characteristic $\beta(I_C)$ of the serial transistor.

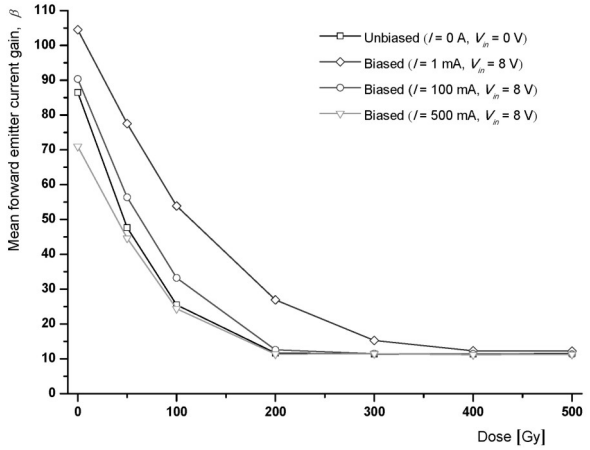

Figure 3: Change in the mean serial transistor's forward emitter current gain in the voltage regulator L4940V5 under the influence of γ-radiation (V_{out} = 4.9 V, I_{out} = 400 mA).

However, the data presented in Figs. 3 and 4 are a clearer illustration of the previously reported comment – the same devices, after the same total ionising doses, operated with a forward emitter current gain of approximately 12 (for I_{load} = 400 mA), compared with the cases of moderately loaded devices (I_{load} = 100 mA), where measured values of the current gain declined down to 2–3 [24]. Yet, it should be mentioned again that the measured values of the serial transistor's forward emitter current gain were not obtained for the same values of the base – emitter voltage (V_{BE}), but rather the quotient of the measured collector and base currents (equation (2)) of the serial device QS (Fig. 1) during the experiment.

Since a simulation model of the L4940V5 voltage regulator could not be created, confirmation of the presented hypothesis on the primary influence of the feedback circuit on measured values of the serial transistor's current gain have to be obtained by eliminating the

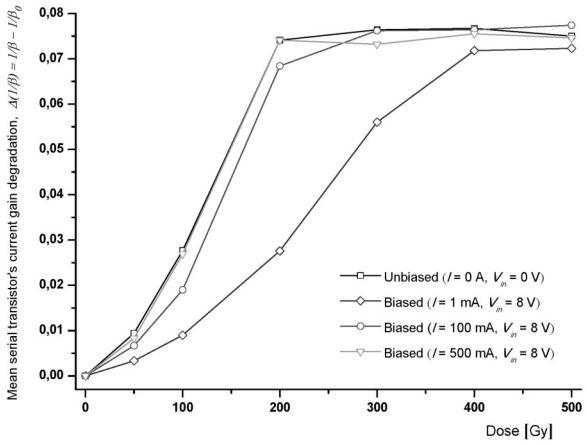

Figure 4: Change in the mean serial transistor's current gain degradation in the voltage regulator L4940V5 under the influence of γ-radiation (V_{out} = 4.9 V, I_{out} = 400 mA).

dominant influence of all the other functional blocks in the voltage regulator. These blocks are, as presented in Fig. 1, the preregulator with protection circuitry (thermal protection, overload protection, shutdown circuit, etc.), the antisaturation circuit, the feedback circuit with operational amplifier and, finally, the serial PNP power transistor. Now the influence of particular functional blocks on the radiation hardness of the L4940V5 voltage regulator will be analysed, with particular attention to the exploitation characteristics of the serial vertical PNP transistor.

The saturation boundary of the serial transistor's base current was approximately 35 mA. This value is nearly the same as the base currents observed during examination of the maximum output current [26]. During the same tests, the values of the serial PNP transistor's forward emitter current gain were measured, being in the range of approximately 20–25. The presented analysis leads to the conclusion that a rise in the output current from 400 mA up to 700–800 mA would have led to characteristics similar to those obtained during examination of the voltage regulator's maximum output current [26], with a slightly lower measured current gain, similar values of the base current and minimum influence of the negative feedback reaction. Values of the base currents presented in Fig. 7 were obtained by subtracting the voltage regulator's quiescent currents without load (Fig. 6) from the total voltage regulator's quiescent currents (Fig. 5).

In the case of a high load current of 400 mA, there was little difference between the curves depending on the bias conditions. Owing to the requirement for the voltage regulator to provide much higher output current than during the previous tests, regardless of the bias conditions, the base currents quickly rose to the saturation value of 35 mA (Fig. 7). However, the rise in the base current for biased devices with negligible load current (V_{in} = 8 V, I = 1 mA) was the slowest.

The obvious limits of the voltage regulator's quiescent current (up to 40 mA; Fig. 5) and the serial PNP transistor's base current (up to 35 mA; Fig. 7) are consequences of the applied antisaturation circuit (Fig. 1). In the voltage regulator L4940V5 a circuit is included which prevents intrinsic saturation of the PNP transistor, eliminating quiescent current peaks [32]. Following the bias of the isolated collector power PNP transistor operating in the saturation mode, a current is observed to flow to the substrate. The reason was the triggering of the parasitic PNP transistor whose collector is the substrate. The forward emitter current gain of this parasitic element is β = 2 - 4, but it can drain a considerably larger current if the power PNP transistor is forced into very deep saturation [32]. This is the case when the regulator is starting with a small load and the driver is supplying the maximum current at the base of the vertical PNP transistor. In these conditions, for a load current of nearly 1 mA, the PNP power transistor's base current may be 100 mA, while the substrate quiescent current could reach 300 mA [32]. To prevent this effect, an antisaturation circuit has been incorporated into the device. This circuit prevents the emitter-collector voltage of the PNP transistor from falling below the predetermined level of the input current due to the limitation of the serial transistor's base current, preventing the saturation of the PNP power transistor [32].

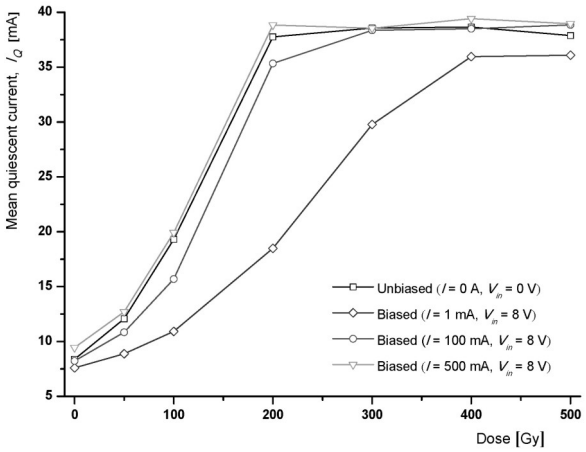

Figure 5: Change in the mean quiescent current in the voltage regulator L4940V5 under the influence of γ-radiation (V_{out} = 4.9 V, I_{out} = 400 mA).

Soon after the start of irradiation, the serial transistor's base current begins to rise, affected by the load current and input voltage. The process is shown in Fig. 7 and is related to amount of the absorbed total ionising dose rather than the time-dependency effects during irradiation. After a total dose of 200 Gy(SiO_2), for most

of the examined samples the base current reached the limit, primarily as a consequence of the antisaturation circuit reaction. The effect of the antisaturation circuit becomes explicitly represented during the operation with a high load current. If the antisaturation circuit did not react, the rise in the serial transistor's excess base current and, consequently, the voltage regulator's quiescent current would be much more marked.

The effect of the negative feedback reaction in a low-dropout voltage regulator is to preserve the stable output voltage, and conserve the minimum possible dropout voltage, quiescent current and chip temperature. Since the heavily loaded samples of voltage regulators L4940V5 operated with output current of 400 mA, which is nearly a quarter of the declared maximum current of examined integrated circuit and approximately half of the measured values of the maximum output current, problems on the circuit's overload were not related to this case. Hence, the voltage regulator's control circuit had to balance the influences of ionising radiation on the quiescent current and the serial transistor's dropout voltage. Although devices L4940V5 are low-dropout voltage regulators, primarily designed for operation with the minimum voltage collector-emitter on the serial transistor, an excessive rise in the quiescent current and, therefore, the serial transistor's base current may lead the power PNP transistor into saturation mode, threatening the correct operation of the voltage regulator as a linear integrated circuit. Therefore, prevention of an excessive increase in the voltage regulator's quiescent current is a priority, even in the low-dropout voltage regulator. This preferential reaction of the antisaturation circuit is clearly noticeable in Figs. 5 and 7, being directly connected with the increase in the serial transistor's dropout voltage after the absorption of the total doses of 200–300 Gy(SiO_2) (Fig. 2).

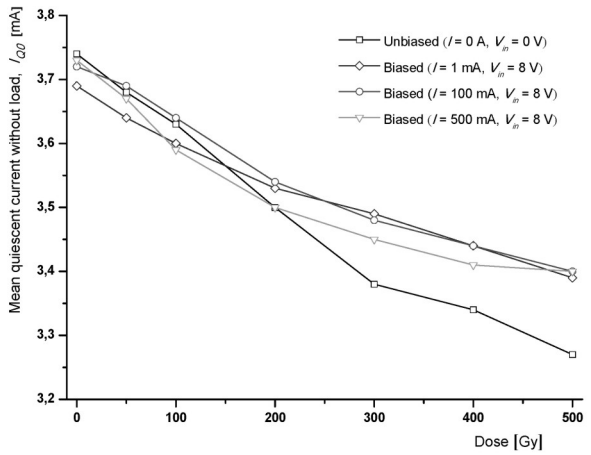

Figure 6: Change in the mean quiescent current in the unloaded voltage regulator L4940V5 under the influence of γ-radiation ($V_{in} = V_{CE(400\,mA)} - 4.9$ V, $I_{out} = 0$ A).

From early examinations of the radiation effects in voltage regulators L4940V5, line regulation characteristics for unbiased and biased samples after the absorption of the total dose of gamma radiation of 3 kGy(SiO_2) were published [27]. A group of five samples was exposed to gamma radiation with a dose rate of 5.5 cGy(SiO_2)/s [27]. Despite the influence of γ radiation, in a wide range of the input voltages and load currents, the output voltage expressed very moderate change, measured only in tens of millivolts [27].

In this paper we presented results of examination of the voltage regulator's line regulation characteristics from the same primary experiment, but after absorption of a ten times lower dose than presented in the previous article [27]. This was nearly on the half of the range of 500 Gy(SiO_2) used in the experiment described in this paper. Samples were analysed after the absorption of the total gamma radiation dose of 300 Gy(SiO_2). Line regulation characteristics obtained without bias during the irradiation were presented in Fig. 8, while Fig. 9 showed the line regulation characteristics of devices that operated with input voltage V_{in} = 7 V and output current I_{load} = 100 mA in a gamma radiation environment. In these cases, changes in the line regulation characteristics were symbolic, being in the range of millivolts. Some greater variations of the output voltage could only be perceived for the operation modes with lower input voltages (6.5 V and 8 V) and higher load currents (from 300 mA up to 700 mA). Nevertheless, the maximum variations of the output voltage after absorption of the total dose of 300 Gy(SiO_2) did not exceed 40 mV, which is less than 1% of the nominal output voltage.

Other useful information obtained from the line regulation data is related to the voltage reference. Since variations of the output voltage for load currents up to 100 mA are only a few millivolts, regardless of the input voltage, they are a good indication that the degradation of the voltage reference is negligible. Slightly higher variations of the output voltage from the nominal value of 5 V were recorded for higher load currents and lower input voltages, yet in all cases within the boundaries of ±1% around the nominal value. These minor variations of the output voltage represent verification of the proper operation of the negative feedback circuit and particularly the operational amplifier A1 (Fig. 1).

As mentioned earlier, the attached heatsinks enabled the voltage regulators to operate with power dissipations exceeding 7 W. In the events presented in the literature [23, 33], the high chip temperature led to early activation of the thermal protection circuit and the reduction of the voltage regulator's output current. On the other hand, examinations of the minimum dropout voltage on the serial transistor, with constant load cur-

rent of 400 mA, were always in operation modes with low dissipation, never exceeding 1 W. Therefore, analysis of the line regulation characteristics enabled both estimation of the thermal shutdown circuit on the voltage regulator's operation, and the integrated circuit's operation with low input voltages and higher load currents.

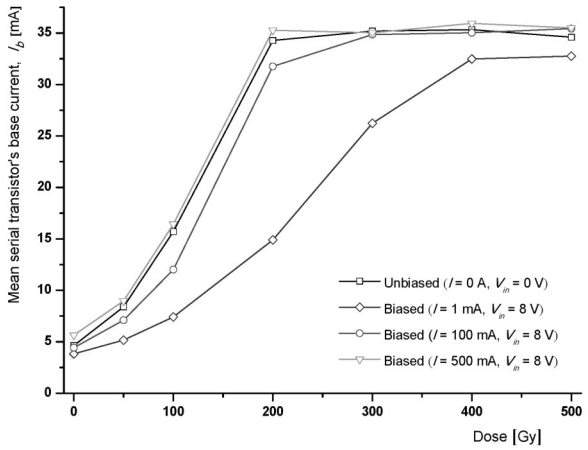

Figure 7: Change in the mean serial transistor's base current in the voltage regulator L4940V5 under the influence of γ-radiation (V_{out} = 4.9 V, I_{out} = 400 mA).

While obtaining the line regulation characteristics, the L4940V5 voltage regulator successfully operated with both low dissipations and power dissipations up to 7 W (for V_{in} = 15 V, I_{load} = 700 mA; Figures 8 and 9). As may be seen from Figures 8 and 9, there were no problems during the voltage regulator's operation that would activate the thermal shutdown circuit, affecting the operation of the serial transistor QS and the entire integrated circuit. Therefore, power dissipations significantly below the threshold of 1 W would certainly not have any effect on the thermal shutdown circuit during examination of the minimum dropout voltage, eliminating its potential influence on the sharp rise in the serial transistor's base current, I_b (Fig. 1).

Examination of the minimum dropout voltage in the heavily loaded voltage regulators L4940V5 was expected to lead to manifestation of the mechanism of the serial PNP transistor's emitter crowding. Very sharp saturation of the base current was evident even for doses of 200 Gy(SiO_2), as may be seen in Fig. 7. The mechanism of emitter crowding may lead to a great decline in the serial transistor's forward emitter current gain, affecting the rise in the base current.

Due to the operation of tested samples with a high load current, the emitter depletion mechanism was expected to have greater influence than in samples operating with less than 10% of the serial transistor's nominal current. Results obtained during the examinations of the moderately loaded samples clearly demonstrated the strong influence of the load current during irradiation on the serial transistor's excess base current [24]. In the case of heavily loaded devices, all types of irradiation are followed by the detection of the minimum dropout voltage with a high load current of 400 mA. Therefore, additional data on the influence of high load current on the radiation tolerance of the vertical PNP power transistor were expected.

Despite the difficulties in estimating the transistor's physical parameters in an integrated circuit, especially due to their significant changes during the radiation exposure, some data, on the technological process and the main characteristics of the vertical PNP power transistor, enabled estimation of the emitter injection efficiency. Consequently, evaluation of the emitter crowding and its influence is possible, also as an estimation of the emitter depletion mechanism on the radiation hardness of the serial transistor in the voltage regulator L4940V5.

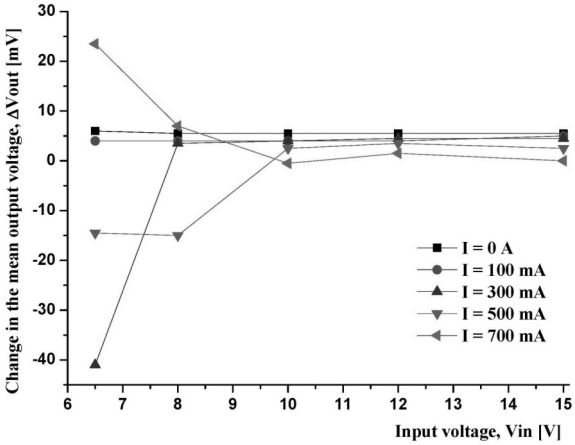

Figure 8: Relative line regulation characteristics of the unbiased voltage regulators L4940V5 after deposition of the total dose of γ-radiation of 300 Gy(SiO_2) (bias conditions: Vin = 0 V, I = 0 A).

Now, the principal characteristics of the isolated collector vertical PNP power transistor in the voltage regulator L4940V5 have to be estimated. Therefore, data on the implemented technological process and construction of the integrated circuit L4940V5 have to be analysed.

The implemented serial element is the isolated collector PNP power transistor (ICV PNP) [29], created from 36 groups of elementary interdigitated PNP transistors made by "$HDS^2/P^{2\prime\prime}$® Multipower 20 V ("High Density Super Signal / Power Process") [27, 34]. The vertical PNP transistor is created with the isolated collector (a graded collector with the p enhancement region) and the nested emitter (a p type, with the phosphorous impurities, $Q_p \approx 5 \cdot 10^{13}$ cm^{-2}). Also, a graded base was

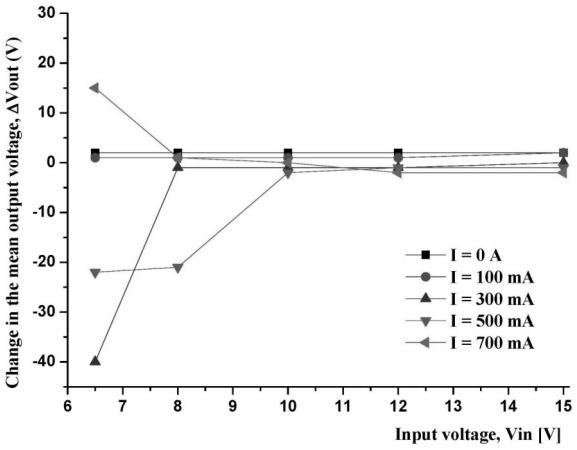

Figure 9: Relative line regulation characteristics of the biased voltage regulators L4940V5 after deposition of the total dose of γ-radiation of 300 Gy(SiO_2) (bias conditions: Vin = 7 V, I = 100 mA).

implemented (n+ area near the base contact, with arsenic impurities, $Q_{As} \approx 5 \cdot 10^{15}$ cm^{-2}, together with the n type volume of the base surrounding the emitter, with boron impurities, $Q_B \approx 2 \cdot 10^{13}$ cm^{-2}) [27, 34]. After synthesis of the semiconductor structure was completed, an insulating layer made of silicon-dioxide was deposited above the wafer, followed by another layer of silicon-dioxide implanted with phosphorous and boron (Phosphorous Boron Silicon Glass, PBSG). Both layers had a thickness of 500 nm [27, 34].

For the exact determination of the doping densities of the emitter and base areas, it would be necessary to obtain exact data on the effective width of their layers. However, such data are not provided by the examined references [32, 34]. Nevertheless, the base width can be estimated from the gain-bandwidth product, f_T (the product of the common emitter current gain β and the frequency of measurement at which the gain-frequency curve begins to descend) [35]. Since the gain-bandwidth product for the ICV PNP transistor is f_T = 80 MHz [32], from the table for the calculation of a base width from the approximate gain-bandwidth product in reference [35], the active base width may be estimated to be approximately 2.25 μm. If the effective emitter length was rated as 1.5 μm, and also according to the known initial values of total quantity of impurities per unit area in the emitter and active base area ($Q_p \approx 5 \cdot 10^{13}$ cm^{-2} and $Q_B \approx 2 \cdot 10^{13}$ cm^{-2}) [34], the rated surface doping densities in the emitter and active base area before irradiation are $N_E = 3.3 \cdot 10^{17}$ cm^{-3} and $N_B = 9 \cdot 10^{16}$ cm^{-3}, respectively.

Therefore, estimated values of the base width (W_B) and the impurity concentrations in the emitter (N_E) and base (N_B) areas, as well as the thermal voltage V_T (equal to 26 mV at room temperature [36]) may be used in the calculation. The equation for the diffusion constant for the holes in the n type base area is [37]:

$$D_B = V_T \mu_p \tag{3}$$

The equation for the diffusion length of the holes in the base area is [37]:

$$L_B = \sqrt{D_B \tau_B} \tag{4}$$

From the relation for the estimation of the holes' lifetime in the n type base area [38]:

$$\tau_B = \frac{5 \cdot 10^{-7}}{1 + 2 \cdot 10^{-17} \cdot N_B} \tag{5}$$

as well as from equations (3) and (4), the holes' diffusion length in the base area on L_B = 12.6 μm may now be defined (mobility of holes in the n type base area obtained from the diagram on the mobility of holes in silicon, at 300 K, as $\mu_p = 340 \ \frac{cm^2}{Vs}$ [38]; therefore, the diffusion constant would be $D_B = 8.84 \ \frac{cm^2}{s}$, while the holes' lifetime in the n type base area would be $\tau_B = 1.8 \cdot 10^{-7}$ s).

The next step is the estimation of the base transport factor for a transistor with a narrow base [36]:

$$\alpha_T \approx 1 - \frac{W_B^2}{2L_B^2} \tag{6}$$

Using the obtained data on the base width (W_B = 2.25 μm) and the holes' diffusion length (L_B = 12.6 μm), from equation (6) the base transport factor prior to irradiation as α_T = 0.984 may be calculated.

From the relations on the common base current gain, α_F is [37]:

$$\alpha_F = \gamma \, \alpha_T \tag{7}$$

where γ is the emitter injection efficiency. Also, from the current ratio that defines the common base current gain, α_F (the collector current is the voltage regulator's L4940V5 output current and the emitter current is the device's input current, i.e. the sum of the collector current and the serial transistor's base current) [37]:

$$\alpha_F = \frac{I_C}{I_E} \tag{8}$$

So, finally, the common base current gain, for the serial PNP power transistor before irradiation as $\alpha_F = 0.99$ may be calculated from equation (8) (evaluated for the samples with input voltage of 8 V and output current 1 mA; in this case, the serial transistor's base current was approximately 4 mA (Fig. 7)).

Nevertheless, a correction now has to be made in the calculation of the base transport factor, α_T, obtained from equation (6). Since the $\alpha_F = 0.99$, according to equation (8), and $\gamma \leq 1$, consequently the base transport factor cannot be $\alpha_T = 0.984$, but at least 0.99. Therefore, the approximation written in equation (6) was in this case slightly inaccurate, as was the second iteration regarding the calculation of some basic parameters. If the holes' diffusion length remained the same at room temperature prior to irradiation ($L_B = 12.6$ μm), then, according to equation (6), for the initial value of the base transport factor before irradiation being $\alpha_T = 0.99$, the active base width would be $W_B = 1.8$ μm. In accordance with the result on the base width, also some other parameters may be recalculated from equations (3)-(6) in the second iteration: the doping density in the active base area before irradiation is $N_B = 8.65 \cdot 10^{16}$ cm^{-3}, the holes' lifetime in the n type base area is $\tau_B = 1.83 \cdot 10^{-7}$ s and the effective emitter length may be rated as 1.45 μm. However, despite the significant difference between the active base width in the first and second iterations (approximately 20%), the other three parameters did not demonstrate notable variations (up to 4%).

The calculated value of the emitter injection efficiency points to very efficient operation of the emitter, close to the ideal situation before exposure to γ radiation.

The worst case for emitter injection efficiency after absorption of the total dose of 500 Gy(SiO_2) would be preservation of the base transport factor, α_T, on its initial value of 0.99. However, in reality, this is not the case, since the mobility and lifetime of holes decline in the radiation environment [37]. Irradiation to 500 Gy(SiO_2) will lead to degradation of α_T and it is certainly not correct to assume it to have a constant value. Yet, for a quick evaluation of emitter injection efficiency this is a good assumption, since the exact value of the emitter injection efficiency may only be greater than estimated. In general, the reduced α_T may not have a huge impact on the radiation response. Accordingly, from Fig. 6 it may be perceived that the base current is nearly 35 mA in the worst case, for the constant collector current of 400 mA. Hence, from the data on the mentioned collector current and the emitter current (435 mA; sum of the serial PNP transistor's base and emitter current), from equation (8) the value of the common base current gain $\alpha_F = 0.92$ may be calculated. From equation (7), as well as from the obtained value of the common base current gain, the minimum emitter injection efficiency of the serial PNP power transistor after irradiation of the voltage regulator L4940V5 as $\gamma = 0.93$ may be estimated.

This is a higher value of the emitter injection efficiency than expected, and seeing the gamma radiation effects on the decrease of the base transport factor, it would be even greater. Therefore, despite the operation of the voltage regulator's serial transistor with a high current density and the abrupt rise in the base current, emitter crowding in the voltage regulators L4940V5 loaded with 400 mA was not a significant manifestation. Accordingly, the mechanism of the emitter depletion had a minor influence on the serial power PNP transistor's radiation tolerance. Nevertheless, neither thermal protection, nor the overload protection or voltage reference circuit exerted any significant influence on the radiation hardness of the serial PNP transistor. On the other hand, the antisaturation circuit had a significant impact on the voltage regulator's operation, reducing the rise in the serial transistor's excess base current. Therefore, by eliminating the influence of the mentioned functional blocks (voltage reference, protection circuits), as well as the emitter crowding of the serial transistors, it may be concluded that the interdigitated structure of the serial transistor's base-emitter junction led to an abrupt increase of the surface recombination in a gamma radiation environment. The spread of the space-charge region along the high perimeter base-emitter contact increased recombination in the base area, affecting the rise of the serial power transistor's base current. A high perimeter-to-area ratio enables the reduction of base spreading resistance and, consequently, emitter crowding, but makes transistors very susceptible to degradation due to exposure to ionising radiation, mainly because of the large area of the base-emitter junction. Regardless of its high value, the emitter injection efficiency is not equal to 1. Therefore, a portion of the reduced collector current might be attributed to recombination in the neutral base. The reduced collector current due to neutral base recombination causes the base current to increase while leaving the emitter current constant [39].

Along with an increase of surface recombination, the great rise in the excess base current was enabled by the feedback circuit reaction and its influence on the driver transistor QD (Fig. 1), affecting the sharp increase of the serial transistor's QS base current, I_b (Fig. 1). On the other hand, the antisaturation circuit prevented the total voltage regulator's quiescent current rising above the limit of approximately 40 mA. Therefore, the measured values of the forward emitter current gain were higher as the load current increased, pointing to a shift in the voltage regulator's operating point on the char-

acteristic $\beta(I_C)$ of the serial transistor, rather than to the multiple decline of the serial transistor's current gain.

After completion of irradiation, a brief isothermal annealing at room temperature was performed. This annealing, lasting half an hour, highlighted the relatively quick recovery, which was particularly manifested through the decrease of the quiescent current during the annealing process. After examination of the irradiated integrated circuits, performed nearly one year later, the characteristics of the irradiated L4940V5 voltage regulators were similar to those prior to irradiation. Therefore, there was more expressed annihilation of defects following the irradiation than the appearance of long-term degradation of the L4940V5 voltage regulators. The effects of ionising radiation are mostly expressed through the charging of irradiated insulators, creating trapped charge that is mostly temporary. Nevertheless, irradiated silicon devices can never completely recover from the influence of gamma radiation, because the ionising radiation will knock electrons off atoms in an insulator in order to create electron–hole pairs. Therefore, during repeated exposure to ionising radiation, the failure threshold of previously irradiated integrated circuits might be much lower.

None of the examined samples of L4940V5 voltage regulators showed the output voltage falling below the threshold of 4.9 V, or of an excessive change of the serial transistor's dropout voltage. However, not all the obtained results were as expected prior to starting the examination. It was expected that the emitter injection efficiency would be significantly less than was measured, after operation with a high load current in a radiation environment. Emitter crowding was not an expected effect in the case of the serial PNP transistor in the L4940V5 voltage regulator. This was clearly a demonstration of the adequacy of the implemented interdigitated structure of the power transistor. However, the mentioned structure of the serial PNP power transistor with high perimeter-to-area ratio, led to the greatest deviations from the specified limits for IC requirements under the tested range of irradiation. The major variation from the specified characteristics of the L4940V5 voltage regulator under the tested range of irradiation was related to the sharp rise of the quiescent current. While the maximum tolerable value for the average L4940V5 device is approximately 5 mA [28], the quiescent current of the irradiated samples reached 40 mA. This significant increase, as mentioned earlier, was a consequence of the interdigitated emitter of the power transistor, leading to the increase of its base current. Nevertheless, this effect did not have a decisive influence on the operational characteristics of the L4940V5 voltage regulator; together with the rise of the dropout voltage of 0.5 V, it led to only a minor increase of the integrated circuit's dissipation. In general, the tested device remained functional after absorption of 500 Gy(SiO_2) of gamma radiation but with potentially reduced autonomy if it was used for powering battery-supplied electronic devices in a radiation environment.

As mentioned in introduction section, the examination of voltage regulators has been performed in several papers [15–17, 22, 23, 33]. The devices with power PNP transistors with round emitters, most often examined, were those such as "Micrel" 29372 [16, 23]. Much effort has been devoted to define satisfactory technological processes for use in radiation environments, in order to replace specifically designed radiation-tolerant electron devices with low-cost commercial components. According to data published in the literature, other authors have not performed radiation tests on the "STMicroelectronics" L4940V5 five-volt low-dropout voltage regulators. However, "STMicroelectronics" have made the L4913 adjustable voltage regulator, specifically designed for operation in radiation environments [40]. Therefore, a comparison could be made between data obtained for the L4940V5 commercial-off-the-shelf (COTS) voltage regulator, designed for the automotive environment and the L4913 radiation-hard voltage regulator.

Both circuits were made by the same manufacturer, "STMicroelectronics". The L4913 is a 14-pin low-dropout, positive adjustable voltage regulator with thermal shut down, overcurrent protection and external shutdown control. This device is fabricated using the "STMicroelectronics" high-speed complementary bipolar process [40]. Irradiation was performed in a ^{60}Co gamma radiation field with high (62 cGy(SiO_2)/s) and low dose rates (0.01 cGy(SiO_2)/s) [40]. Samples of the L4940V5 voltage regulators were also exposed to the ^{60}Co gamma radiation field but with a medium dose rate of 4 cGy/s. During irradiation, the input voltage of the L4913 biased circuits was set at 10 V and the output voltage set at 6 V (adjustable), while the load current was 100 mA (for the L4940V5: V_{in} = 8 V, V_{out} = 5 V (fixed value), while I_{load} had three values: 1, 100 and 500 mA). Some samples of both L4913 and L4940V5 were irradiated without bias voltage and load current. The L4913 devices were exposed to a total ionising dose of 3 kGy(SiO_2) [40], whereas the L4940V5 voltage regulators were exposed to a total dose of 500 Gy(SiO_2) (it must be mentioned that during the primary tests, the L4940V5 devices were also exposed to a total ionising dose of 3 kGy(SiO_2) [27]).

During the tests in the gamma radiation fields, the L4913 circuits proved highly radiation tolerant. The minimum dropout voltage increased by only 15–20 mV (after absorption of 500 Gy(SiO_2), depending on

bias conditions, for the load current of I = 200 mA [40]. This was much less than the 500–600 mV measured on the circuits of the commercial L4940V5. However, the decrease in the maximum output current was approximately 15 mA (also after deposition of 500 Gy(SiO_2)), which is close to the 20–35 mA value measured on the L4940V5 voltage regulators [26]. Another similarity between the radiation responses was observed in the output voltages of the L4913 and L4940V5 devices. In both cases, for negligible load currents (1 mA and 5 mA), variations of the output voltage during irradiation were in the range of a few millivolts [25, 40]. Therefore, the commercial L4940V5 demonstrated a much higher increase in dropout voltage than its radiation-tolerant counterpart, the L4913; however, differences in the maximum output currents and output voltages were minimal. In general, radiation-induced damage in the L4913 voltage regulator, for doses up to 3 kGy(SiO_2), was negligible and was significantly less than that for the case of the commercial L4940V5 device. On the other hand, the L4940V5 automotive voltage regulators remained completely functional in the γ radiation field. If the dropout voltage of 500–600 mV was not critical for consumers, the L4940V5 voltage regulator would be completely suitable for the power supply of electronic devices in a ^{60}Co environment, for total doses up to 500 Gy(SiO_2).

Finally, a complete comparison of the results obtained from these two types of voltage regulators could not be performed because the authors of [40] did not observe the L4913 voltage regulator's quiescent current and accordingly, could not present results on the serial transistor's forward emitter current gain and base current. On the other hand, these detailed examinations, regarding the serial power transistor, were done for the L4940V5 voltage regulators. However, McClure and associates [40] came to the conclusion, similar to that which we arrived at for the L4940V5 device, that the damage mechanism of the L4913 voltage regulator was not the loss of the serial transistor gain but more likely to be radiation-induced error in the current sense circuit [40].

4. Conclusion

New data recorded during tests of voltage regulators L4940V5 with a load current of 400 mA showed a decline in the serial vertical PNP transistor's forward emitter current gain of 6–9 times, decreasing the value of the current gain to approximately 12. The dropout voltage on the serial PNP transistor increased approximately 0.5-0.6 V after absorption of the total gamma radiation dose of 500 Gy(SiO_2).

A significant decline in the measured values of the serial power transistor's forward emitter current gain was affected by the abrupt rise in the PNP transistor's base current. Negative feedback reaction in this case caused a shift in the serial transistor's operating point on the $\beta(I_C)$ characteristic. The main reason for the excess base current was implementation of the high perimeter-to-area ratio of the base-emitter junction in the serial PNP power transistor. The major reason for the limited increase of the serial transistor's base current was reaction of the antisaturation circuit, having the primary function to prevent an excessive rise in the quiescent current and keep the serial transistor's operation in the direct active region, and simultaneously keeping the output voltage on the referent value. The principal method for realisation of the negative feedback reaction in the voltage regulator L4940V5 was the effect of the feedback circuit's operational amplifier on the driver transistor, indirectly affecting the serial PNP transistor's base current. According to the line regulation characteristics, obtained after absorption of the total ionising dose of 300 Gy(SiO_2), also the voltage reference was negligibly affected by the irradiation. Variations in the line regulation characteristics after irradiation were expressed in terms of millivolts, being below 1% in comparison with the initial curves. Correct operation of the irradiated voltage regulators during the acquisition of the line regulation characteristics with a power dissipation of up to 7 W on the serial transistor demonstrated the minor influence of the thermal protection circuit on the results obtained. Examinations of the heavily loaded samples of voltage regulators L4940V5 in a gamma radiation field identified relatively little difference between the recorded curves regarding the serial transistor (minimum dropout voltage, forward emitter current gain, base current) for different load currents during the irradiation.

Measurement of the serial transistor's currents, together with the estimation of the physical parameters of the isolated collector vertical PNP transistor, led to the evaluation of the emitter injection efficiency being greater than 0.93 after the circuit's irradiation with a total ionising dose of 500 Gy(SiO_2). This result led to the conclusion that, even during the operation of the serial transistor with high current density, emitter crowding was not a significant factor, leaving emitter depletion as the mechanism of secondary influence on radiation tolerance of the isolated collector vertical PNP power transistor.

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Design and Analysis of Low Power Master Slave Flip-Flops

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Abstract: In this paper, a comparative analysis of existing architectures for flip-flop along with the proposed design is made. The comparison is done on the basis of power, delay, PDP and transistor count. Due to continuous increase in integration of transistors and growing needs of portable equipments, low power design is of prime importance. All simulations are performed on TSpice using BSIM models in 130 nm process node. The simulation results show that for all supply voltages, all clock frequencies and all data activities proposed flip-flop consumes the lowest power. Proposed flip-flop has the second shortest delay and the second lowest PDP and also occupies low area. So this design is best suited for low power and high performance applications.

Key words: Pass transistor, Short circuit current, Flip-flop, Optimization, clock distribution network

Načrtovanje in analiza master-slave flip-flop vezij nizkih moči

Povzetek: V članku je predstavljena primerjalna analiza obstoječih arhitektur flip-flop vezij in predlagan načrt. Primerjava je bila opravljena na osnovi moči, zakasnitev PDP in števila tranzistorjev. Ob konstantnem naraščanju integracije tranzistorjev in uporabi prenosnih naprav ima načrtovanje vezij nizkih moči zelo pomembno. Simulacije so bile izvedene s pomočjo TSpicea z uporabo BSIM modelov v 130 nm koraku. Simulacije izkazujejo nizko porabo moči pri vseh frekvencah ure in podatkovnih aktivnostih flip flopa. Predlagan flip flop ima drugi najkrajši čas zakasnitev in drugo najnižjo vrednost PDP ter zaseda malo prostora, kar mu omogoča najboljšo uporabo za visoko zmogljive aplikacije z nizko porabo.

Ključne besede: prehodni tranzistor, kratkostično vezje, flip-flop, optimizacija, razporeditvena mreža ure

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1. Introduction

In many digital very large scale integration (VLSI) designs, the clock system that includes clock distribution network and flip-flops is one of the highest power consuming components. It accounts for 30% to 60% of the total system power, out of which 90% is consumed by the flip-flops and the last branches of the clock distribution network that is driving the flip-flop [1]. Scaling of transistor feature sizes has provided a remarkable advancement in silicon industry for last three decades. However, while the performance increases due to scaling, the power density increases substantially every generation due to higher integration density. Furthermore, the demand for power-sensitive design has grown significantly in recent years due to tremendous growth in portable applications. Consequently, the need for power-efficient design techniques has grown considerably [2]. In the present design consideration the power consumption and chip area requirements are small and the operating speed is high compared to conventional discrete I.C. design, so low power design with high performance is becoming increasingly important [3]**.** There are three major sources of power consumption in a digital CMOS circuits. The average power is given by the following equation [4]:

$$P_{avg} = p_t (C_L V \cdot V_{dd} f_{clk}) + I_{sc} V_{dd} + I_{leakage} V_{dd} \quad (1)$$

The first term represents the switching component of power, where C_L is the effective switched loading capacitance, f_{clk} is the clock frequency and p_t is the probability that a power consuming transition occurs (or activity factor). The second term represents the direct path short circuit current I_{sc}, which arises when both the NMOS and PMOS transistor networks are simultaneously active or on, conducting current from the supply V_{dd} to ground. The third term is leakage power. The

leakage current can arise from substrate injection, gate leakage and sub threshold effects. $I_{leakage}$ is primarily determined by the CMOS fabrication process technology and modeled based on its characterization.

A conventional ASIC design mostly uses an edge-triggered flip-flop as a sequencing element due to simplicity of its timing model. Specifically, the amount of time available to a combinational block that lies between two flip-flops is fixed. This constrains timing uncertainties within each combinational block, which is important for design steps at higher abstraction level such as logic synthesis when implementation details are unknown [5]. For big circuits implementing complex functionalities like control units, microprocessors, usually a very large number of flip-flops are used. So these flip-flops heavily affect the performance of the entire system. This paper focuses on the minimization of power dissipation in the edge triggered flip-flops.

Flip-flops appear in several configurations, such as D flip-flops, T flip-flops and J-K flip-flops where the D flip-flop is the most common. To lower the complexity of circuit design, a large portion of the most digital circuits is synchronous in the sense that they operate using a clock. A conventional single edge-triggered (SET) flip-flop typically latch data either on the rising or the falling edge of the clock cycle. The SET flip-flops are usually configured as master-slave flip-flops, i.e. a sequential structure using two latches, called master and slave respectively, in cascade [6].

This paper is organized into six sections. Section 2 compares the existing single edge triggered flip-flop structures. In section 3, new flip-flop structure is proposed. The nominal simulation conditions, along with analysis and optimization performed during simulation, are discussed in Section 4. In section 5 results are presented and performance for new proposed design and conventional designs are compared in terms of power, delay, PDP and transistor count. Section 6 ends the paper with conclusion.

2. Existing single edge triggered flip-flops

2.1 Push Pull Flip-Flop

To improve the performance of a conventional Transmission Gate Flip-Flop (TGFF shown in Figure 1) [7, 8], addition of an inverter and transmission gate between the outputs of master and slave latches to accomplish a push–pull effect at the slave latch, was proposed in [9]. This increased 4 transistors. To compensate this increment of transistor count, two transmission gates are eliminated in the Push Pull Flip-Flop from the feedback paths of conventional TGFF. The static Push Pull Flip-Flop (PPFF) is shown in Figure 2.

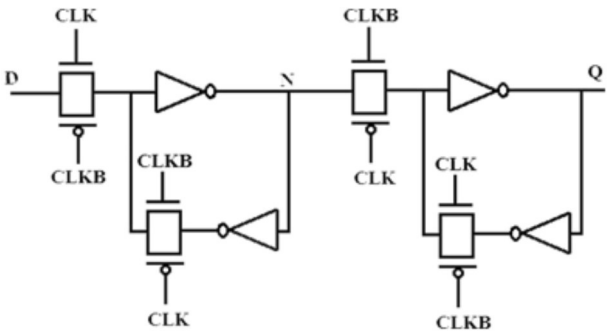

Figure 1: Conventional Transmission Gate Flip-Flop (TGFF)

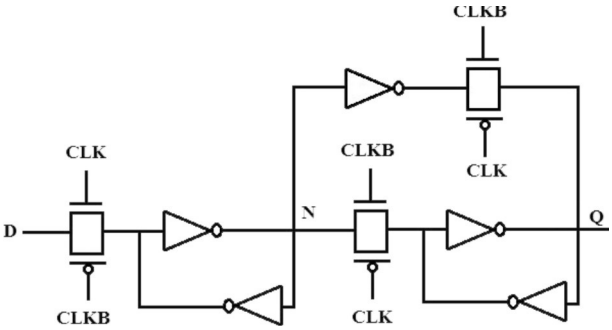

Figure 2: Push Pull Flip-Flop (PPFF)

2.5 Pass Flip-Flop

To save power, the number of transistors of the proposed flip-flop was reduced in [10]. The four transistors in the feedback path of conventional TGFF are replaced by single PMOS transistor. Hence, total 6 transistors are reduced in this flip-flop. This semi-static Pass Flip-Flop (Pass FF) is shown in Figure 3.

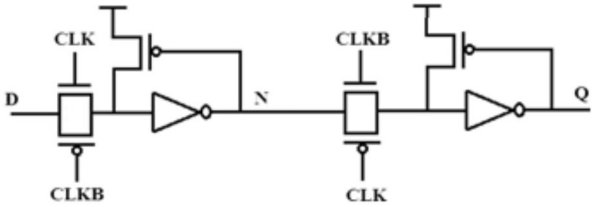

Figure 3: Pass Flip-Flop (Pass FF)

2.6 Pass Isolation Flip-Flop

To activate the feedback path of pass FF only during OFF cycle, a PMOS transistor was added in the feedback in [10]. This semi-static Pass Isolation Flip-Flop (PIFF) is shown in Figure 4. As compare to Pass FF, the number of transistors of this flip-flop is increased by two but this reduces short circuit current during ON cycle. It also improves speed as compare to Pass FF.

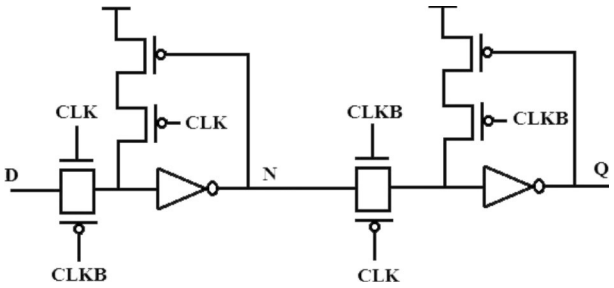

Figure 4: Pass Isolation Flip-Flop (PIFF)

2.2 C²MOS Flip-Flop

Figure 5 shows the static C²MOS Flip- Flop [11]. This flip-flop consists of a C²MOS feedback at the outputs of the master and the slave latches. When clock is at logic 'HIGH', the clocked inverter CLKI1 latches the input D to an intermediate node N. The feedback consisting of clocked inverter CLKI2 and inverter I1 maintains this logic level at node N when clock is at logic level 'HIGH'. Similarly when CLK changes to logic 'LOW', the slave latch gets functional and clocked inverter CLKI3 transfers the logic level from node N to the output Q. The feedback consisting of clocked inverter CLKI4 and inverter I2 maintains this logic level at output node Q when clock is grounded. There are 20 transistors in this circuit, C²MOSFF has largest area but this flip-flop shows the shortest delay and the lowest PDP.

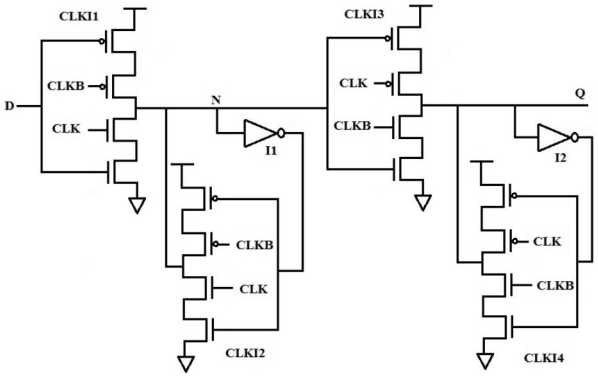

Figure 5: C²MOS Flip-Flop (C²MOS FF)

2.4 High Performance Flip Flop

In High Performance Flip-Flop (HPFF)**,** a feedback is provided from the output node of the slave inverter to a specific internal node in the master-stage as shown in Figure 6. This flip-flop was proposed by [12]. This feedback is provided by only a single transistor. So this has lesser number of transistors as compare to other proposed flip flops discussed in this section. The main advantage of this design is reduced device count and decreased parasitic capacitance at internal nodes of the flip flop which results in improved power-delay product.

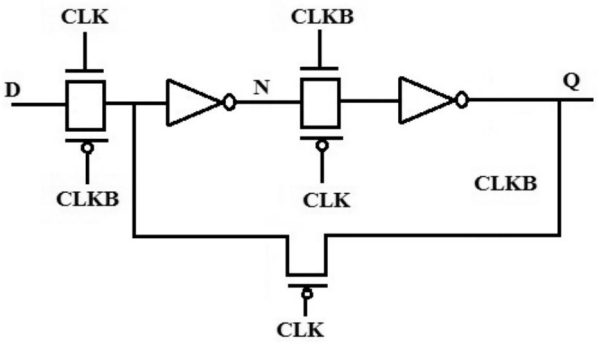

Figure 6: High Performance Flip-Flop (HPFF)

2.3 Area Efficient Flip-Flop

The Area Efficient flip-flop was proposed in [13]. This semi-static flip-flop is illustrated in Figure 7. This flip-flop has lesser transistor count as compared to above discussed flip-flops except HPFF. In this design the feedback circuit of the master section is removed and in slave section, feedback loop consists of a transmission gate. When clock level is 'HIGH', master latch is functional and inverse of the data is stored to an intermediate node N. When clock goes to 'LOW' logic level, the slave latch becomes functional and produces data at the output Q and QB.

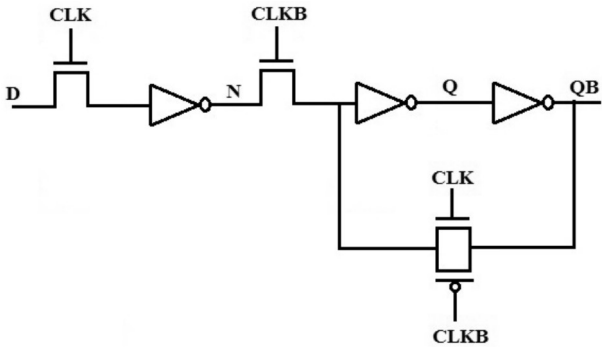

Figure 7: Area Efficient Flip-Flop (Area Efficient FF)

3. Proposed single edge triggered flip-flop

One method to reduce the transistor count is to use an NMOS for latch input. However, since the output of an NMOS can only reach a voltage level of Vdd -Vt when it is at logic 1, it results in increased power dissipation [9]. So in the proposed flip-flop (proposed FF), transmission gates are used in both master and slave latches as shown in Figure 8. This reduces the power dissipation.

The feedback path is improved in the proposed flip-flop. Most of the conventional static designs use two

feedback loops one each in the master as well as the slave stage. This increases the total parasitic capacitance at the internal flip-flop nodes, leading to higher dynamic power dissipation and reduced performance. This also results in total chip area overhead due to increased transistor count [12]. In the proposed flip-flop, the feedback circuit of the master section is removed and there is feedback in slave section to make the flip-flop semi-static in nature. This flip-flop is a modification of the pass flip-flop. The feedback PMOS of Pass flip-flop's master section is removed and in slave section a PMOS transistor with complemented clock signal and an inverter are used to make feedback path functional only during OFF cycle of clock. This reduces short circuit current during ON cycle as compare to pass flip-flop. In the proposed design, device count is reduced and parasitic capacitances at internal nodes of the flip-flop are decreased which results in improved power dissipation. If there is reduction in the number of clocked transistors of design, the clock load capacitance is reduced, leading to low power consumption in the clock distribution network [14]. Thus by reducing the number of clocked transistors, the power dissipation of the proposed design is further reduced.

This flip-flop is negative edge triggered flip-flop. In the proposed FF when clock level is 'HIGH', master latch is activated and inverse of the data is stored to an intermediate node N (output of master latch). When clock goes to 'LOW' logic level, slave latch becomes functional and produces data at the output Q. This is a low area flip- flop and has the smallest power dissipation with the second lowest PDP.

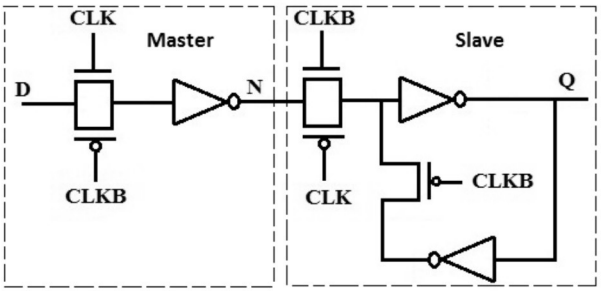

Figure 8: Proposed flip-flop (Proposed FF)

4. Simulation

Simulation parameters used for comparison, are shown in table 1. Under nominal condition, a 16-cycle sequence (1111010110010000) with an activity factor of 18.75% is supplied at the input for average power measurements. Power consumption based on this data sequence of 18.75% was considered as the real parameter for characterizing power dissipation of a flip-flop design. The dynamic power consumption is dependent on switching activities at various nodes of the circuit. It varies with different data rates and circuit topologies. Hence to obtain a fair idea of power dissipation for a circuit topology, different data patterns should be applied with different activity rates [15]. So in simulations, following five different data sequences have been adopted to compare the power consumption of flip-flop structures discussed in this paper:

i) 1111111111111111 (A=0)
ii) 0000000000000000 (A=0)
iii) 1111010110010000 (A=0.18)
iv) 1100110011001100 (A=0.5)
v) 1010101010101010 (A=1)

Where "A" is the data activity. The results are carried out for the period of 16 data sequences. All simulations are performed on TSpice using BSIM 3v3 level 53 models in 130 nm process node. The supply voltage is varied from 1 V to 2 V and the clock frequency is varied from 100 MHz to 1 GHz.

4.1 Analysis

Various parameters of the flip-flops can be compared. In general, a PDP-based comparison is appropriate for low power portable systems in which battery life is the primary index of energy efficiency [16]. In this paper, our main interest is in SETFF usage for low-power applications. Therefore power consumption is selected for comparing different flip-flops. Additionally delay and PDP are also compared of the discussed flip flops.

4.2 Optimization

There is always a tradeoff between power dissipation and propagation delay of a circuit. A flip-flop can be optimized for either high performance or low power,

Table 1: CMOS simulation parameters

S. No.	1	2	3	4	5	6	7	8	9	10
Particulars	CMOS Technology	Min. Gate Width	Max. Gate Width	MOSFET Model	Nominal Supply Voltage	Temperature	Duty Cycle	Nominal Clock Frequency	Sequence Length	Rise and Fall Time of Clock & Data
Value	130 nm	260 nm	0.910 µm	BSIM 3v3 level 53	1.3 V	25° C	50 %	400 MHz	16 Data Cycles	100 ps

but both the parameters are critical. In this work, the designs are simulated to achieve minimum power dissipation. Transistor count is also included to maintain a fair level of comparison. The transistors, that are not located on critical path, are implemented with minimum size to reduce area overhead and to minimize power dissipation.

5. Result and discussion

Figure 9 and Figure 10 indicate the power consumption in microwatts at different supply voltages for 18.75% data activity and 400 MHz clock frequency. These figures show that power increases with increase in supply voltage because all three types of power (i.e. switching power, short circuit power and leakage power) depend on supply voltage and the switching power is proportional to the square of the supply voltage. Approximately 90% power dissipation in CMOS logic is due to the dynamic (switching) power [17]. So power dissipation rapidly reduces with reduction in the supply voltage. Table 2 indicates the power consumption in microwatts at different supply voltages for 18.75% data activity and 400 MHz clock frequency. The simulation results indicate that the proposed FF has the least average power dissipation among all the designs for all supply voltages. For fair comparison, the average of power consumption at all voltages is taken except 1 V, because at 1 V two previously proposed flip-flops failed. This result shows that the proposed FF has 41.25%, 34.91%, 46.51%, 43.65%, 28.02% and 70.22% improvement in average power consumption when compared to the previously proposed flip-flops discussed in section 2 respectively. Proposed FF has up to 70.22% improvement in average power consumption. Among previously proposed flip-flops discussed in section 2, HPFF shows the lowest power consumption for all supply voltages. PPFF and Area efficient FF failed at 1 V. Area efficient FF shows the worst power consumption for all voltages.

Figure 11 shows, all flip-flops consume the largest power at 1 GHz clock frequency and the smallest power at

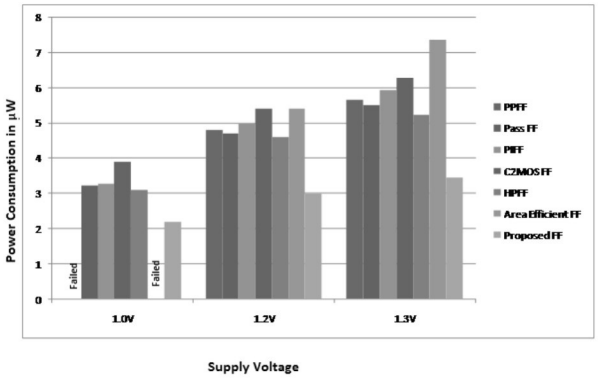

Figure 9: Power consumption as a function of supply voltage for 1.0 V, 1.2 V and 1.3 V

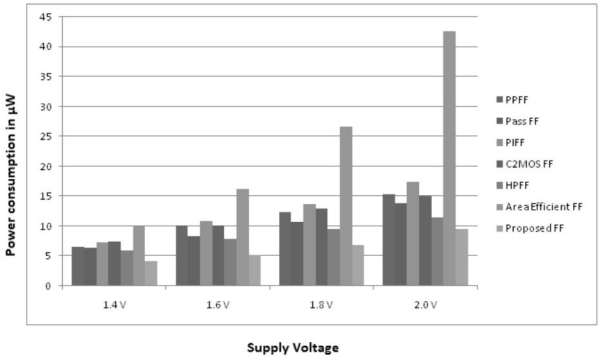

Figure 10: Power consumption as a function of supply voltage for 1.4 V, 1.6 V, 1.8 V and 2.0 V

100 MHz clock frequency. As clock frequency increases, power consumption increases. Table 3 shows power consumption in microwatts as a function of clock frequency. Table shows that for all clock frequencies, the proposed FF has the better power consumption than all the existing flip-flops discussed in section 2. For fair comparison, the average of power consumption at all clock frequencies is taken. This average result shows that the proposed FF has 39.42%, 38.97%, 44.39%, 44.85%, 33.60% and 53.37% improvement in average power consumption when compared to the previously proposed flip-flops discussed in section 2 respectively. Table 3 shows that the proposed FF has up to 53.37% improvement in average power consumption.

Table 2: Power consumption in µW as a function of supply voltage

VDD (V)	PPFF	Pass FF	PIFF	C2MOS FF	HPFF	Area Efficient FF	Proposed FF
1.0	Failed	3.23	3.28	3.9	3.1	Failed	2.2
1.2	4.8	4.7	4.97	5.4	4.6	5.41	3.0
1.3	5.65	5.52	5.94	6.30	5.24	7.38	3.44
1.4	6.5	6.4	7.34	7.4	6.0	10	4.1
1.6	10.1	8.4	10.90	10.1	7.9	16.2	5.2
1.8	12.4	10.7	13.64	12.9	9.5	26.6	6.9
2.0	15.4	13.8	17.42	15.1	11.5	42.6	9.6
Average excluding 1 V	9.14	8.25	10.04	9.53	7.46	18.03	5.37

Table 3: Power consumption in μW as a function of clock frequency

CLOCK (MHz)	PPFF	Pass FF	PIFF	C2MOS FF	HPFF	Area Efficient FF	Proposed FF
100	3.5	3.1	3.63	3.0	2.50	4.7	1.7
200	4.2	4.0	5.01	4.0	3.30	5.5	2.2
250	4.5	4.2	4.25	4.4	3.80	5.9	2.4
400	5.7	5.5	5.94	6.3	5.20	7.4	3.4
10000	9.5	10.4	11.00	12.4	10.20	12.1	6.9
Average	5.48	5.44	5.97	6.02	5.00	7.12	3.32

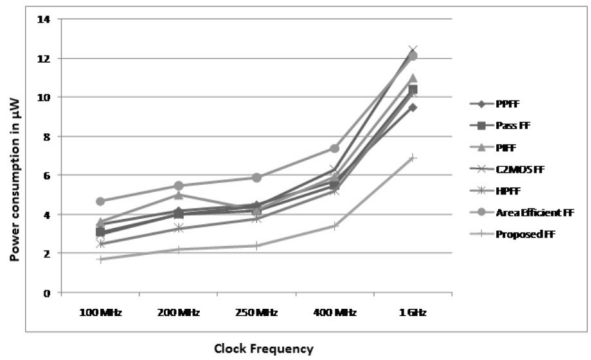

Figure 11: Power consumption as a function of clock frequency

Among previously proposed flip-flops discussed in section 2, HPFF shows better power consumption at all clock frequencies except 1 GHz, at this frequency PPFF shows the better power consumption. Area efficient FF has the highest power consumption for all clock frequencies except 1 GHz. As clock frequency is increased, power consumption of C²MOSFF increases and near 1 GHz clock frequency C²MOSFF consumes the highest power.

Figure 12 shows, 100% data activity exhibits the largest power consumption and 0% data activity exhibits the smallest power consumption. For all switching activities, the proposed flip-flop shows better power dissipation than all the discussed previously proposed flip-flops. Power Consumption in μW as a function of data activity is shown in Table 4. For fair comparison, the average of power consumption at all data activities is taken. This average result shows that the proposed FF has 38.78%, 38.55%, 41.98%, 46.51%, 35.73% and 53.06% improvement in average power consumption when compared to the previously proposed flip-flops discussed in section 2 respectively. Proposed FF has up to 53.06% improvement in average power consumption. Area Efficient FF consumes the highest power for all switching activity except zero switching activity (when all are 0's). For this zero switching activity (when all are 0's), C²MOSFF consumes the highest power. Among previously proposed flip-flops discussed in section 2, HPFF shows better power consumption at all data activities except 0% switching activity(when all are 0's or all are 1's), for 0% switching activity PPFF exhibits better power dissipation.

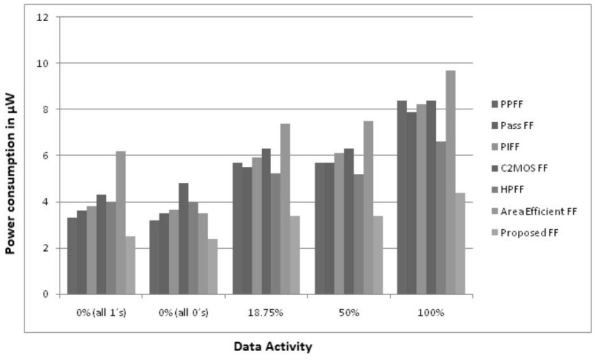

Figure 12: Power consumption dependence on data activity rates

Table 5 shows average clock to output (C_Q) delay in pS at different supply voltages for 18.75% data activ-

Table 4: Power consumption in μW as a function of data activity

Data Activity	PPFF	Pass FF	PIFF	C²MOS FF	HPFF	Area Efficient FF	Proposed FF
0% (all 1's)	3.3	3.6	3.80	4.3	4.00	6.2	2.5
0% (all 0's)	3.2	3.5	3.64	4.8	4.00	3.5	2.4
18.75%	5.7	5.5	5.94	6.3	5.24	7.4	3.4
50%	5.7	5.7	6.13	6.3	5.20	7.5	3.4
100%	8.4	7.9	8.22	8.4	6.60	9.7	4.4
Average	5.26	5.24	5.55	6.02	5.01	6.86	3.22

Table 5: Average clock to Q delay in pS

VDD (V)	PPFF	Pass FF	PIFF	C²MOS FF	HPFF	Area Efficient FF	Proposed FF
1.0	Failed	238.15	166.35	106.9	247.65	Failed	172
1.2	137.85	133.6	126.65	41.35	119.95	593.2	86.6
1.3	99.99	79.77	63.78	25.61	74.31	293.43	39.47
1.4	116.4	103.55	43.52	18.25	56.35	193.65	72.75
1.6	132.4	100.3	9.90	13.35	41.25	98.25	6.65
1.8	111.75	81.3	78.61	11.55	34.05	58.4	46.35
2.0	95.3	66.15	69.54	10.3	30.3	43.75	43.25
Average excluding 1 V	115.62	94.11	65.33	20.07	59.37	213.45	49.18

ity and 400 MHz clock frequency. The simulation results indicate that the proposed FF has the lowest delay among all the designs for 1.6 V supply voltage and the second lowest delay for 1.2 V and 1.3 V. For fair comparison, the average of delay at all voltages is taken. This result shows that the proposed FF has 57.46%, 47.74%, 24.72%, 17.16% and 76.96% improvement in average delay when compared to the previously proposed flip-flops discussed in section 2 respectively except C²MOSFF. The proposed FF has up to 76.96% improvement in average delay and has the second lowest delay.

C²MOSFF shows 59.19% lesser average delay when compared to proposed FF. C²MOSFF shows the lowest delay for all supply voltages except 1.6 V, at this voltage proposed FF shows the lowest delay.

PIFF shows the second lowest delay for 1 V, 1.4 V and 1.6 V. For 1 V HPFF exhibits the longest delay. As supply voltage increases, delay of HPFF decreases as compared to other flip-flops and for 1.8 V, 2 V this flip-flop shows the second lowest delay. For 1.2 V, 1.3 V and 1.4 V Area Efficient FF shows the highest delay but as the supply voltage increases its delay improves. As supply voltage increases, delay of PPFF increases as compared to other flip-flops and for 1.6 V, 1.8 V, 2 V this flip-flop shows the worst delay. Overall Area Efficient FF has the worst delay and C²MOSFF has the smallest delay.

Figure 13 and Figure 14 show the clock to Q PDP for discussed flip-flops as a function of supply voltage. These figures show that for 1 V, 1.3 V, 1.6 V proposed FF shows the lowest PDP while for 1.2 V, 1.4 V, 1.8 V it shows the second lowest PDP. Table 6 shows the clock to Q PDP as a function of supply voltage. For fair comparison, the average of PDP at all voltages is taken except 1 V, because at 1 V two existing flip-flops failed. This average result shows that the proposed FF has 76.30%, 66.41%, 60.65%, 35.73% and 88.12% improvement in PDP when compared to the previously proposed flip-flops discussed in section 2 respectively except C²MOSFF, it has 34.46% better PDP than the proposed FF. The proposed FF has up to 88.12% improvement in PDP. For 1.2 V, 1.4 V, 1.8 V and 2 V C²MOSFF shows the lowest PDP while for 1 V and 1.3 V this flip-flop shows the second lowest PDP. At 1.6 V PIFF shows the second lowest PDP. PPFF and Area Efficient FF failed at 1 V. For 1 V, Pass FF has the worst PDP and for all other voltages Area Efficient FF has the worst PDP. Overall Figure 13 and Figure 14 show that C²MOSFF and proposed FF has the lowest and second lowest PDP respectively while Area efficient FF shows the worst PDP.

Table 7 illustrates the transistor count for the various flip-flop designs discussed in this paper (excluding the inverter to generate the complementary clock signals). The proposed FF has eleven transistors and five clocked transistors. Proposed FF has one more transis-

Table 6: PDP_{C_Q} as a function of supply voltage

VDD (V)	PPFF 10-18J	Pass FF 10-18J	PIFF 10-18J	C2MOS FF 10-18J	HPFF 10-18J	Area Efficient FF	Proposed FF 10-18J
1.0	Failed	769.22	545.63	416.91	767.72	Failed	378.40
1.2	661.68	627.92	629.45	223.30	551.77	3209.21	259.80
1.3	564.94	440.33	378.85	161.34	389.38	2165.51	135.78
1.4	756.60	662.72	319.44	135.10	338.10	1936.50	298.27
1.6	1337.24	842.52	107.91	134.84	325.88	1591.65	34.58
1.8	1385.70	869.91	1072.24	149.00	323.48	1553.44	319.81
2.0	1467.62	912.87	1211.39	155.53	348.45	1863.75	415.20
Average excluding 1V	1028.96	726.05	619.88	159.85	379.51	2053.34	243.91

Table 7: Transistor count of discussed flip-flops

Flip Flop	PPFF	Pass FF	PIFF	C²MOS FF	HPFF	Area Efficient FF	Proposed FF
No of transistor	16	10	12	20	9	10	11
No of clocked transistor	6	4	6	8	5	4	5

tors than Pass FF, Area efficient FF and two more transistors than HPFF but table 2 shows that the proposed FF has 34.91%, 70.22%, 28.02% improvement in average power consumption, table 5 shows that the proposed FF has 47.74%, 76.96%, 17.16% improvement in average delay and table 6 shows that the proposed FF has 66.41%, 88.12%, 35.73% improvement in PDP over these flip-flops respectively. It is further seen that C²MOSFF occupies the largest silicon area but it shows the smallest delay and the smallest PDP. PPFF has the second largest transistor count.

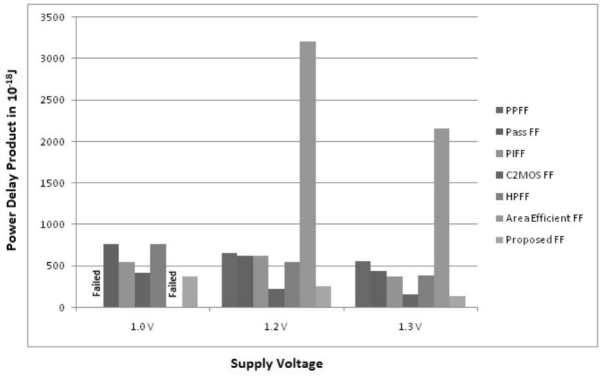

Figure 13: PDP dependence on supply voltage for 1.0 V, 1.2 V and 1.3V

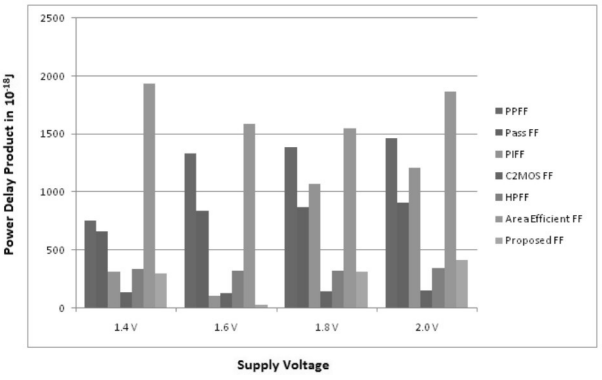

Figure 14: PDP dependence on supply voltage for 1.4 V, 1.6 V, 1.8 V and 2.0 V

6. Conclusion

A comparative analysis of single input single edge triggered flip-flops has been done. Among previously proposed flip-flops discussed in section 2, HPFF shows the lowest power consumption for all supply voltages and for all clock frequencies except 1 GHz, at this frequency PPFF shows the better power consumption. PPFF and Area efficient FF failed at 1 V. Area efficient FF shows the worst power consumption for all voltages and for all clock frequencies except 1 GHz. As clock frequency is increased, power consumption of C²MOSFF increases and near 1 GHz clock frequency C²MOSFF consumes the highest power. Area Efficient FF consumes the highest power for all switching activity except zero switching activity (when all are 0's), for this activity C²MOSFF consumes the highest power. Among previously proposed flip-flops discussed in section 2, HPFF shows better power consumption at all data activities except 0% switching activity(when all are 0's or all are 1's), for this 0% switching activity PPFF exhibits better power dissipation. For low supply voltages Area Efficient FF shows the highest delay but as the supply voltage increases its delay improves, while the delay of PPFF increases with increment of supply voltage as compared to other flip-flops. Area Efficient FF has the worst delay and C²MOSFF has the smallest delay. C²MOSFF has the lowest PDP and this flip-flop has 34.46% better PDP than the proposed FF while Area efficient FF shows the worst PDP. It is further seen that C²MOSFF has largest transistor count but C²MOSFF shows the shortest delay and the lowest PDP. Area efficient FF has only ten transistors but this flip-flop has the highest power consumption, the highest delay and the worst PDP. So the Area efficient FF is not suited for low power or high performance applications.

The new flip-flop structure has been proposed in this paper. The proposed flip-flop structure is compared on the basis of power, delay, PDP and transistor count with the existing flip-flop structures. For all supply voltages, all clock frequencies and all data activities, the proposed FF has better power consumption than all the existing flip-flops discussed in section 2 and proposed FF has up to 70.22% improvement in average power consumption. The simulation results indicate that the proposed FF has the lesser delay than all the existing flip-flop designs discussed in section 2 except C²MOSFF. Proposed FF has up to 76.96% improvement in average delay but C²MOSFF shows 59.19% lesser average delay when compared to the proposed FF. The proposed FF has better PDP than all the existing flip-flop designs discussed in section 2 except C²MOSFF. The proposed FF has up to 88.12% improvement in PDP, C²MOSFF has 34.46% better PDP than the proposed FF. However C²MOSFF uses nine more transistors than the proposed

FF, so proposed FF has lesser area, cost and power as compare to the C²MOSFF.

Among all flip-flops compared, the proposed FF is found to be the best energy efficient having the second lowest PDP and the second shortest delay. The proposed FF has up to 70.22% improvement in average power dissipation, up to 76.96% improvement in delay and up to 88.12% improvement in PDP. So, proposed FF is best suited for low power and high performance applications.

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Printed Electronics on Recycled Paper and Cardboards

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Abstract: RFID antennas can be manufactured in different ways, conventionally by etching, hot stamping or by printing. Printed RFID antennas are becoming increasingly common because of the possibility of producing RFID tags more economically, ecologically and rapidly, using roll-to-roll technology. Different printing technologies enable printing on rigid as well as on flexible materials. In our research the possibility of printing UHF RFID antennas on various low-cost and low-quality materials was analysed. Eighteen different printing materials appropriate for packaging (cardboard) and newspaper (recycled paper) printing were analysed. Firstly, the UHF antenna was designed, and then the antennas were printed using a semi-automatic screen printer. After printing, the optimal drying process was determined and the final resistance was measured. The influence of printing material roughness on line gain, print mottle and abrasion was analysed. Finally, the analysis of simulated and printed antenna was performed and, after chip integration, the final tag operation was checked.

Key words: RFID antenna design, conductive ink, antenna printing, cardboard, recycled paper.

Tiskana elektronika na recikliranem papirju in kartonu

Povzetek: Poznamo različne načine izdelave RFID anten. Lahko so proizvedene konvencionalno z jedkanjem, s folijo z vročim tiskom ali pa so natisnjene s prevodno barvo. Zaradi ekonomskih in ekoloških razlogov se v zadnjem času vse več raziskav dela na področju tiskanih RFID anten, ki so v prednosti tudi zaradi hitrosti, ki jo nudi tehnologija tiska iz zvitka na zvitek. Z različnimi tehnologijami tiska lahko dosežemo različne lastnosti odtisov, tiskamo pa lahko tako na toge kot tudi na fleksibilne materiale. V naši raziskavi smo preučili možnost tiska RFID anten na različne nizkocenovne in nizkokakovostne tiskovne materiale. Analizirali smo osemnajst tiskovnih materialov primernih za tisk embalaže (karton) in časopisov (recikliran papir). Najprej smo načrtovali UHF RFID anteno in jo natisnili s polavtomatskim strojem v tehniki sitotiska. Po tisku smo določili optimalno sušenje za doseganje minimalne upornosti prevodnih linij. Določili smo vpliv hrapavosti tiskovnega materiala na prirast linij, tiskarsko neenakomernost in abrazijo odtisov. Raziskavo smo zaključili z analizami smernega diagrama in impedance natisnjene antene, integrirali čip in preverili delovanje RFID značke.

Ključne besede: načrtovanje RFID antene, prevodna barva, tisk antene, karton, reciklirani papir

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1. Introduction

Even though printing technology has existed for centuries, as in other industries there are new opportunities for development and progress. Products that include electronic components integrated on flexible printed materials, especially different thermoplastic polymers (foils) [1-3], paper-based materials [2-10], Kapton [5, 11, 12], etc., have been developing rapidly, but no studies have analysed the potential of printing RFID antennas on recycled paper and cardboard. An increase of printed electronics is a consequence of searching for new technologies for mass and low-cost production. Both requirements can be achieved by using roll-to-roll technology with different printing techniques [13].

In the literature, the most commonly researched topics in this field are simple passive electronic components, such as RFID antennas, made using screen printing [14-17], inkjet [14, 18-20] and gravure printing [21, 22] and

less commonly with flexo and offset printing technology. Many studies have also been undertaken in regard to the performance of RFID printed antennas [1, 23-27].

RFID technology is an automatic identification technology that consists of RF tags, a reader, an antenna and a deployment environment [28]. The RF tag is composed of an antenna and a chip, and can operate on different operating frequencies [29] (LF: 125–134 kHz, HF: 13.56 MHz, UHF: 860–960 MHz). With these frequencies, UHF RFID tags are mostly used for tracking in logistics; the reading distance is longer in comparison to LF or HF RFID tags.

Since the printing technologies enable printing on rigid as well as on flexible materials, in our research the possibility of printing UHF RFID antennas on different low-cost and low-quality printing materials was analysed. The antennas were printed on different types of recycled paper and cardboard appropriate for packaging (cardboard) and newspaper (recycled paper) printing. Firstly, a UHF antenna the size of a credit card was designed, and then the antennas were printed using a semi-automatic screen printer. After printing, the optimal drying process was determined for obtaining the lowest sheet resistance or maximum electrical conductivity.

The influence of printing material roughness on line gain, print mottle and abrasion was analysed. Then an analysis of simulated and printed antenna was performed. Finally, the chips were integrated with the printed antennas, and the operation of the final tags was checked.

2. Experiment

The experiment began with a selection of 18 printing materials: 9 types of cardboard (C1–C9) and 9 types of recycled paper (P1–P9). The principal characteristics of the printing materials (grammage and thickness) are shown in Table 1.

Table 1: Properties of the used printing materials.

Sample	Grammage [g/m^2] ISO 536	Thickness [µm] ISO 534
C1	245	400
C2	295	505
C3	230	285
C4	270	410
C5	230	280
C6	300	425
C7	300	380
C8	350	525
C9	300	500
P1	59.7	62
P2	80.2	75
P3	58.9	113
P4	71.6	127
P5	79.9	127
P6	60.2	80
P7	97.8	104
P8	96.5	104
P9	53.5	65

For all printing materials, roughness was determined using a TR200 profilometer. The arithmetic mean deviation of profile (arithmetic mean of the absolute values of profile deviation from mean) within the sampling length was measured. The average roughness of 15 measurements for each sample is presented in Figure 4.

The experiment was further divided into six steps (see Figure 1). Firstly, the antenna was designed and printed. Printed samples were dried and afterwards printing materials and conductive print layers were analysed. The final printed antennas were evaluated and finally the chip was integrated. At the end, a final check of the tag's operation was made.

2.1 UHF antenna design

A UHF RFID antenna at an operating frequency of 868 MHz was designed in accordance with chip specifi-

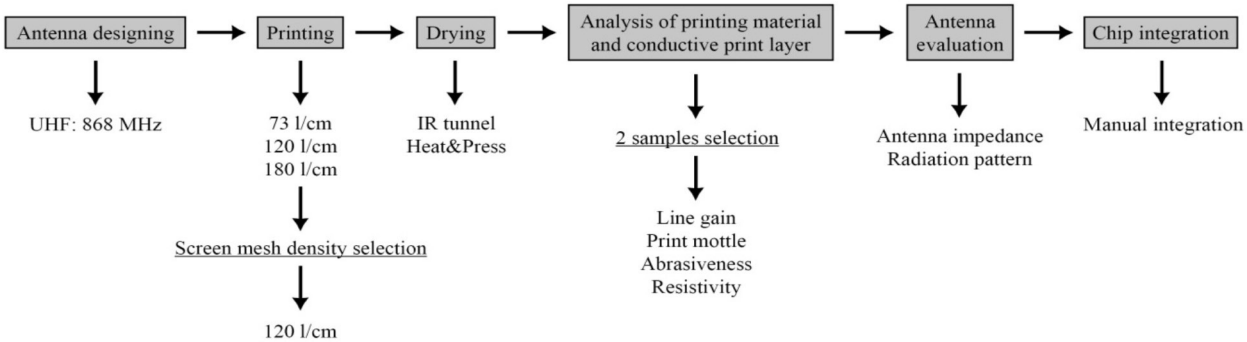

Figure 1: Scheme of experimental.

cation SL900A EPC Class 3 Sensory Tag Chip, the required size, and the printing material (cardboard and recycled paper). The specified chip impedance was Z = 20 – j325 Ω. The type of the antenna was chosen to be the capacitive-loaded (planar) dipole, which fits the standard credit-card size (Figure 2). The impedance and radiation pattern were first simulated using a commercial 3D numerical solver (Ansoft HFSS). The electrical properties of both antenna substrates (cardboard and recycled paper) were the same in the simulation, since a small deviation in the relative permittivity does not change radiation properties much. The electrical properties of both substrates were taken from the published values and were not measured or verified. The modelled antenna comprises a 0.5 mm thick substrate (relative permittivity 3.2, relative permeability 1.0, dielectric loss tangent 0.003, zero surface roughness) simulating the paper and a metallization layer with a 10 μm thickness (1.71*10e6 S/m conductivity as measured from the printed samples, zero surface roughness) simulating the conductive ink. Both surface roughnesses were set to zero in the simulation, since at the design frequency of 868 MHz a major influence on antenna parameters due to the metallization surface roughness is probable. The published relative permittivity of the paper varies from as low as 2.5 to as high as 5, depending on the composition and moisture levels, however chose an intermediate value of 3.2 in our case. The simulated impedance of the antenna model was found to be Z = 20 + j270 Ω with a radiation efficiency of 87% at the specified design frequency.

After the antenna was printed onto several samples it was also evaluated with measurements. We measured the radiation patterns (in the E and H planes) and the impedance using a custom made balun. The comparison between the simulation and measurements is given in the section 3.4 RFID antenna evaluation.

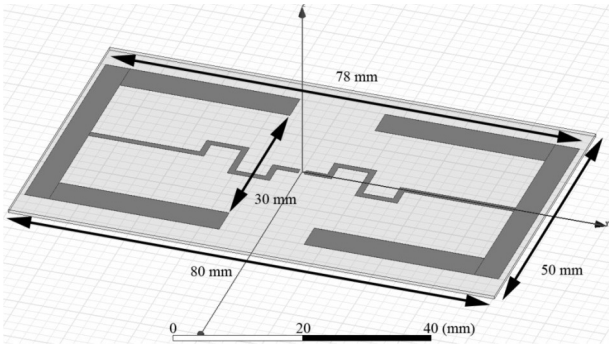

Figure 2: The antenna design.

2.2 Printing

After the antenna was designed, the printing form was prepared (Figure 3). The test elements for measuring line gain, sheet resistance and the newly designed antenna were applied. After that, all various printing materials were printed using SunChemical conductive printing ink (CRSN2442, SunTronic Silver 280, Thermal Drying Silver Conductive Ink). Tree SEFAR® high-modulus monofilament polyester plain weave meshes were applied: 73 l/cm (with theoretical ink volume 26.7 cm^3/m^2), 120 l/cm (with theoretical ink volume 16.3 cm^3/m^2) and 180 l/cm (with theoretical ink volume 9.1 cm^3/m^2) for printing with a semi-automatic screen printer.

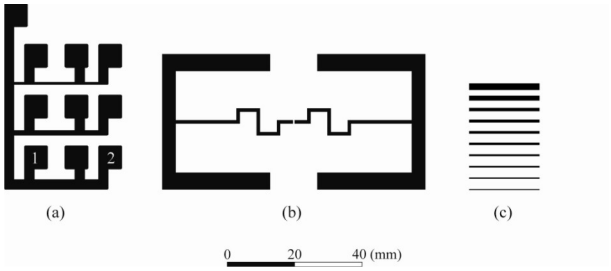

Figure 3: Printing form for printing on recycled paper and cardboard: (a) test element for measuring resistance, (b) antenna design, (c) test element for line gain determination.

2.3 Drying

After printing, the optimal drying process was determined. In accordance with the printing ink specification, drying in an IR tunnel was performed. Firstly, the drying time and temperature were varied for samples printed with all three screen mesh densities (Figure 5). The best results (the lowest sheet resistance) were obtained when samples were heated in the IR tunnel and then additionally dried with a Heat&Press process. When the optimal drying process was determined, the properties of the conductive printed layer were analysed.

2.4 Analysis of conductive print layer

Line gain, print mottle and abrasiveness

Line gain was determined by measuring the area of the ideal line on digital print form (A_{id}) and the area of the same printed line (A_p). The area of lines was determined using ImageJ software and the final ΔL was calculated (Eq. 1).

$$\Delta L = \frac{A_p * 100}{A_{id}} - 100; [\%] \quad (1)$$

Print mottle or print uniformity was determined in accordance with the traditional STFI method [30]. The calculation of the coefficient of variation (*CV*) was made through Eq. 2, where σ is standard deviation of the grey values, *R* is the mean grey value:

$$CV = \frac{\sigma}{R} * 100; [\%] \quad (2)$$

The abrasion resistance of the printed samples was analysed according to standard ASTM D 5264 on a Param RT-01 rub tester instrument. Printed samples were laid on the table and a 0.9 kg test block (mounted with an unprinted receptor of the same material) positioned on the printed sample was rubbing 500 times (cardboard) or 100 times (recycled paper). One stroke is one back-and-forth rub. While paper is rougher than cardboard, the total area coverage on the unprinted receptor comparable to cardboard was reached after only 100 strokes were applied. After rubbing, an analysis of the unprinted specimens was made and the total area coverage (%) with rubbed printing ink was determined using image analysis. The results represent the proportion of area coated with the rubbed ink on the receptor surface.

Sheet resistance

The resistance (*R*) of samples was measured using a digital multimeter DT-890G on test elements, shown on Figure 3 (a), between points 1 and 2. The normal length (*L*) between points 1 and 2 is 22 mm and width (*W*) is 3 mm. The resistance (*R*) was measured after 24 hours conditioning at 50% relative humidity and at 23°C. The nominal number of squares N_{sq} (Eq. 3) and the final sheet resistance R_{sh} (Eq. 4) of the conductive ink layer in mΩ/sq was calculated.

$$N_{sq} = \frac{L}{W} = 10.3 \quad (3)$$

$$R_{sh} = \frac{R}{N_{sq}}; \left[\frac{\Omega}{sq}\right] \quad (4)$$

2.5 RFID antenna evaluation

The printed antenna impedance was measured on a vector network analyser with the help of a balun. The latter was an interface between the symmetrical antenna port and the asymmetrical coaxial cable. The radiation patterns in the E (electric field) and H (magnetic field) planes for the printed antennas on paper and cardboard were measured at the outdoor antenna-measuring polygon.

2.6 Chip integration

After antenna evaluation, the chips were integrated on printed antennas. The manual integration of SL900A chip was applied with isotropic electro-conductive adhesive with silver particles (Bison, Netherlands). While the chip had 18 pads, the pads that are not appropriate for the connection to the antenna were covered with dielectric ink to avoid the connection of the conductive glue with inappropriate pads. The conductive ink was applied with a needle to both appropriate pads and glued to the printed antenna as a flip chip. The glue was heated for 10 min at 100°C. The final check of the RFID tag operation was made using an IDS-R902 reader with a Patch A0025 antenna (Poynting GmbH, Germany) that also measures the strength of the modulated signal backscattered from the tag. The reader supports ISO18000-6C or EPC Gen2 protocol. Its antenna (gain 6.5 dBi) emits circularly polarised UHF radiation with a frequency of *f* = 867 MHz. The reader's output power is +26 dBm (400 mW). It uses amplitude shift keying and has a maximal input sensitivity of −76 dBm.

3. Results and discussion

3.1 Roughness

The roughness of all analysed samples differs from 0.5 µm to almost 6 µm. As expected, coated cardboards have lower roughness than recycled papers, but there are also some exceptions; i.e., cardboard C3 has higher roughness than recycled papers P1 and P2. While one goal of our research was to establish the influence of surface roughness on printability, the comparison and analysis of the most and the least rough material was performed. The lowest roughness was detected on cardboard (C1) and the highest on recycled paper (P3) (Figure 4).

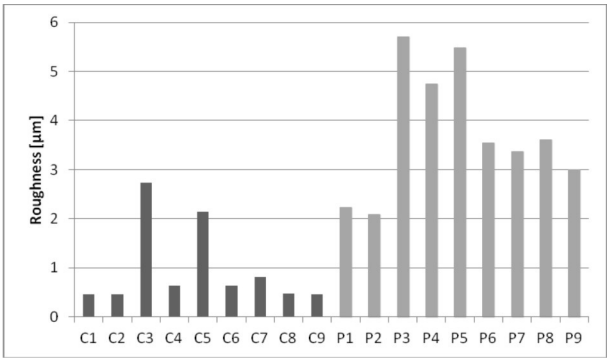

Figure 4: Roughness of all 18 printing materials.

3.2 Drying optimisation

Before drying optimisation, one of the cardboard samples (C1) was printed using all three different screen mesh densities in order to establish the influence of screen mesh density and film thickness on print layer sheet resistance. The optimal screen mesh density was determined after heating for 90 seconds at 115°C (Figure 5).

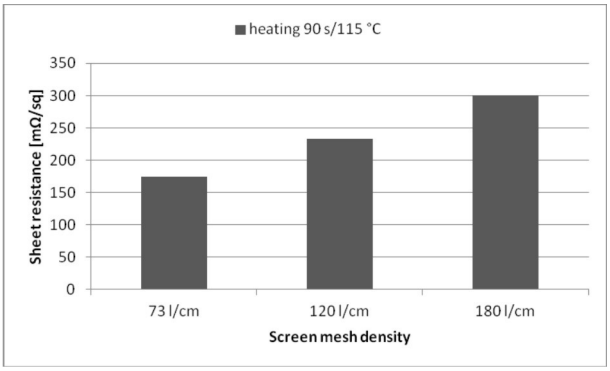

Figure 5: Sheet resistance depending on the screen mesh density and drying time (on cardboard C1).

On the basis of the results presented in Figure 5, one can see that the sheet resistance becomes higher with higher screen mesh density, but the differences are not as high as expected. Because the quantity of ink used influences the sheet resistance of the conductive printed layer, the screen density 120 l/cm was chosen for further investigation, as a compromise between sheet resistance and quantity of printing ink used. While the sheet resistance of the samples was still high after drying in the IR tunnel, additional drying with the pressure (Heat&Press device) at 3 bars was applied. With the aforementioned two-stage drying process the drying was optimised and the sheet resistance of the printed lines on all samples fell below 100 mΩ/sq. Prolonged drying or drying at a higher temperature did not influence the change of sheet resistance. Values remained constant. Final drying conditions are presented in Table 2.

Table 2: Drying conditions.

	Hot zone		Heat&Press	
Printing material	Time [s]	Temperature [°C]	Time [s]	Temperature [°C]
Cardboard	135	115	10	150
Paper	90	115	10	150

3.3 Analysis of conductive print layer

The roughness of printing materials has an impact on the positioning of the flakes of the conductive ink on the material surface [31]. Roughness also affects the quality of the prints (printability), the stability of prints, and, consequently, on abrasiveness, line gain, printing mottle and sheet resistance. In accordance with the results of roughness presented in Figure 4, two printing materials were selected: one with the lowest (C1-coated cardboard) and one with the highest (P3-uncoated recycled paper) surface roughness. This selection was made to determine how surface roughness affects the line gain, print mottle and abrasiveness of the conductive printed layer.

Line gain, print mottle and abrasiveness

The results of the analysed line gain, print mottle and abrasiveness are presented in Figure 6, where it is seen that the higher roughness of the sample P3 causes higher line gain, print mottle and abrasiveness. The difference in line gain is small (2%) - a similar result was obtained with print mottle: the largest difference is in abrasiveness where the cardboard C1 was rubbed 5 times more than recycled paper P3, but the abrasiveness is still much lower than on recycled paper.

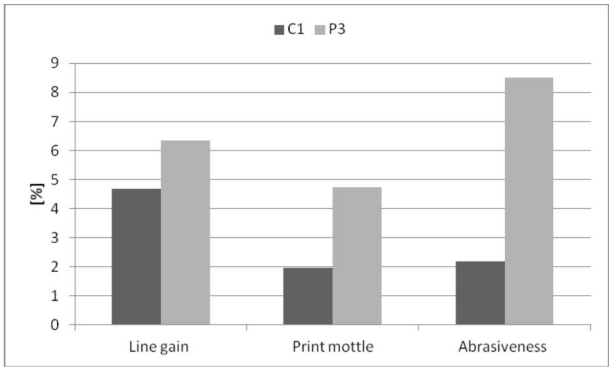

Figure 6: Line gain, print mottle and abrasiveness of selected printing materials.

Sheet resistance

The sheet resistance of printed conductive layers was measured on both selected samples. The values were almost the same: 90 ± 3 mΩ/sq. The result revealed that the printing material (and its surface properties) in our case did not have any influence on the final sheet resistance. The sheet resistance was dependent only on screen mesh density (consequently on conductive layer thickness - see the section 2.2 Printing) and on drying conditions.

3.4 RFID antenna evaluation

The radiation patterns were evaluated with measurements of the antennas printed on the selected coated cardboard C1 and the uncoated recycled paper P3. The results revealed that the patterns are nearly the same for simulated and both printed antennas, regardless of which printing material was used (Figure 7).

In addition to the radiation pattern, the impedance of the antenna was also simulated and measured (Figure 8). The correlation between the measured and the simulated antenna impedances is good. Nevertheless, there is a small deviation between the simulated and measured impedance curves, which is a consequence of the balun used for the measurement. The balun's impedance was subtracted from the measured impedance. We believe that the electromagnetic coupling be-

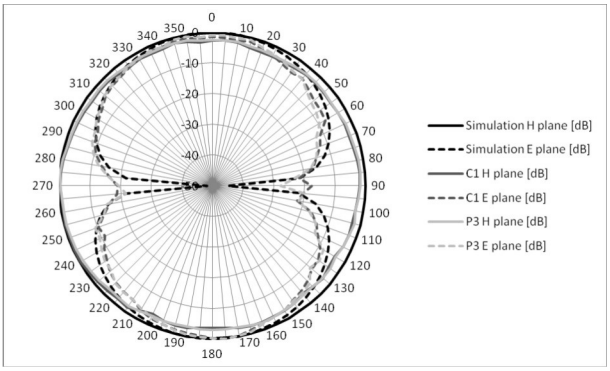

Figure 7: The simulated and measured radiation patterns of the antennas printed on both printing materials.

tween the balun and the antenna structures caused a small effect on the impedance of the printed antenna, making a slight difference between the impedances of the simulated model and the measured antenna.

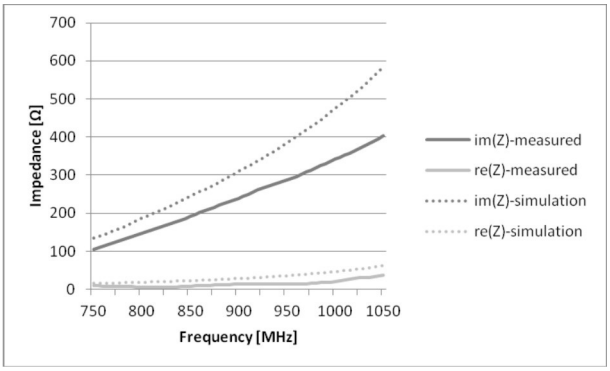

Figure 8: Simulated and measured antenna impedances.

3.5 Chip integration

When the tag was completed (Figure 9), the final operating check was made. It was found that the tags were operational and that momentary temperature could be measured, but only in the near vicinity of the reader antenna. With manual integration, the contact between the antenna and chip is definitely worse and the tag's readability is not optimal. Therefore, much effort towards optimisation remains to be done for better RFID tag operation.

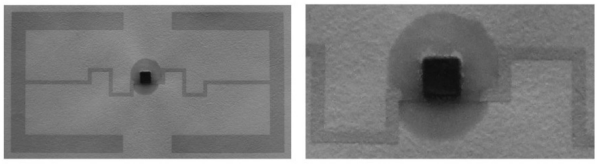

Figure 9: Final RFID tag with printed antenna and integrated chip (left), chip close-up (right).

4. Conclusions

This analysis presented the entire process of manufacturing UHF RFID tags. At the beginning, the UHF antenna was designed in accordance to the chip specification, size limitation, working frequency, and also regarding the printing material. The antenna was printed using three different screen mesh densities for obtaining three different conductive ink thicknesses (see the section 2.2 Printing) and consequently three different levels of resistance. While the resistivity was almost the same, the screen mesh density 120 l/cm was chosen for further analysis. The roughness of all eighteen samples was determined and two samples were selected, one with the highest and one with the lowest roughness. The line gain, print mottle and abrasiveness of both selected samples were analysed. Based on the results, we can conclude that the roughness of printing material has a crucial impact on the quality and the stability of the printed conductive layer. Higher roughness of the recycled paper induces higher line gain, print mottle and abrasiveness. The printed antennas were also evaluated by measuring radiation patterns and impedance. A slight difference in impedance can be observed between the measured and the simulated antennas, but mainly because of the balun used for the connection of the printed sample with the instrument. At the end, the RFID chip was integrated with the antenna and the tag's operation was checked.

We can conclude that the printing material has an impact on the printing properties of the printed antennas, and that it has a small effect on the final sheet resistance and antenna operation. The final tag was detected by the reader and momentary temperature could be measured but some improvements need to be made for better operation and reading at greater distances.

In our further research with the help of the company ams R&D, a chip with a temperature sensor will be modified to allow easier integration in the manner of a strap flip chip.

5. Acknowledgements

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Effects of static and pulsed negative bias temperature stressing on lifetime in p-channel power VDMOSFETs

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Abstract: Threshold voltage shifts associated with negative gate bias temperature instability in p-channel power VDMOSFETs under the static and pulsed stress conditions are analysed in terms of the effects on device lifetime. The pulsed bias stressing is found to cause less significant threshold voltage shifts in comparison with those caused by the static stressing, which is ascribed to the effects of dynamic recovery and shorter actual stress time associated with pulsed bias conditions. Accordingly, pulsed gate bias conditions provide much longer device lifetime than the static ones, which is shown by individual use of the $1/V_G$ and 1/T models for extrapolation to normal operation voltage and temperature, respectively, as well as by combined use of both models for a double extrapolation successively along both voltage and temperature axes. A double extrapolation approach is shown to allow for construction of the surface area representing the lifetime values corresponding to a full range of device operating voltages and temperatures.

Key words: Lifetime estimation, NBTI, VDMOSFET

Vpliv statičnega in pulznega negativnega temperaturnega stresa na življenjske čase v kanalu p močnostnih VDMOSFET-ov

Povzetek: Premik pragovne napetosti zaradi negativne nestabilnosti vrat v kanalu p močnostnih VDMOSFETov v statičnih in pulzno vzbujanih pogojih so analizirani v smislu vplivov na življenjske čase elementa. Izkazalo se je, da pulzno vzbujanje povzroča manjše premike pragovne napetosti glede na razmere pri statičnem vzbujanju, kar lahko pripisujemo vplivom dinamičnega okrevanja in kratkim dejanskim časom pulznega vzbujanja. Pulzno vzbujanje omogoča precej daljše življenjske čase kot pri statičnih pogojih, kar se izkazuje pri individualni uporabi $1/V_G$ in 1/T modelov za ekstrapolacijo do normalnih napetosti in temperatur obratovanja, kakor tudi pri kombinirani uporabi obeh modelov pri ekstrapolaciji po temperaturni in napetostni osi. Dvojna ekstrapolacija omogoča površinski prikaz življenjskih časov preko celotnega temperaturnega in napetostnega območja delovanja elementa.

Ključne besede: Ocena življenjskih časov, NBTI, VDMOSFET

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1. Introduction

With device dimensions in MOS technologies being continuously scaled down, a phenomenon named negative bias temperature instability (NBTI) has been gaining in importance to become widely recognised as one of the most critical mechanisms of device degradation in state-of-the-art CMOS circuits. NBTI refers to the complex physical mechanisms involving generation of oxide-trapped charge and interface traps in MOS structures exposed to stressing by negative gate bias at elevated temperature, and was found to occur mostly in p-channel MOSFETs operated at elevated temperatures (100-250 °C) under negative gate voltages producing gate oxide electric fields in the range 2-6 MV/cm [1-6]. It leads to serious changes in device threshold voltage and may also reduce the transconductance and drain current. Threshold voltage shifts associated with NBTI

are strongly dependent on the stress parameters (gate voltage, temperature, time) and are particularly critical for reliable operation and lifetime of p-channel devices with thin gate oxides [2-4]. However, NBTI could be also critical for reliability of ultra-thick gate oxide devices, such as power MOSFETs. Power MOSFETs, widely used as fast switching devices in home appliances and automotive, industrial and military electronics, are routinely operated at high current and voltage levels, which lead to both self-heating and increased gate oxide fields and thus favour NBTI [7, 8].

In spite of extensive studies over the recent years [1-3, 5, 6], microscopic mechanisms of NBTI are still not well understood, so the technology optimization to minimize NBTI is yet to be achieved. Therefore, accurate models and well established procedures for lifetime estimation are required to make good prediction of device reliable operation. There are several commonly used models for extrapolation along the voltage or electric field axis, such as "V_G", "$1/V_G$" and "power-law" models [9, 10], which enable the use of experimental data obtained under the accelerated stress conditions (increased gate voltage and elevated temperature) to estimate device lifetime for normal operation voltage. These models, however, yield the lifetime only for the temperatures applied during the stressing, so an extrapolation along the temperature axis by "1/T" model, which enables estimation of the lifetime at normal operation temperature, has recently also been proposed [11-13]. A double extrapolation, along both voltage and temperature axes, that lead to lifetime estimates for any reasonable combination of operation voltage and temperature, has been proposed as well [11-13].

It is important to note that gate bias applied during operation of MOS devices in a number of applications switches between the "high" and "low" voltage levels, thus creating the pulsed stress conditions. Some earlier investigations of pulsed NBTI have shown that oxide-trapped charge and interface traps generated during application of the "high" gate voltage level are partially neutralized and/or annealed while the gate is at "low" voltage level [14-17]. So, the lifetime predictions based on static NBT stress conditions [18, 19], where the gate was continuously kept at "high" voltage level, could be wrong, and it is thus necessary to estimate device lifetime under the pulsed NBT stress conditions.

Given the above considerations, in this paper the effects of static and pulsed NBT stressing on threshold voltage in commercial p-channel power VDMOSFETs will be compared in terms of device lifetime. The $1/V_G$ and 1/T models will be applied to appropriate data for NBT stress-induced threshold voltage shift for two separate extrapolations along the voltage and temperature axes in order to get lifetime estimates for the voltages and temperatures expected in device normal operation mode. A double successive extrapolation along the voltage and temperature axes, which extends the validity of the above models to any reasonable set of operation voltages and temperatures, and may provide more realistic lifetime prediction in MOS devices operated under the normal conditions, will be demonstrated as well.

2. Experiment

Devices investigated in this study were commercial p-channel power VDMOSFETs IRF9520, built in standard silicon-gate technology with approximately 100 nm thick gate oxide, which were encapsulated in TO-220 plastic packages. They had the initial threshold voltage $V_{T0} = -3.6$ V and current and voltage ratings of 6.8 A and 100 V, respectively. For the static NBT stress, several sets of devices have been stressed up to 48 hours by applying negative dc voltages in the range 35-45 V to the gate, while drain and source terminals were grounded [18-21]. For the pulsed stress, negative gate voltage pulses (typically 10 kHz, 50 % duty cycle) of the same magnitudes were used. As indicated in Fig. 1, term "stress time" for pulsed stressing in this study refers to the total time, including both the net stress time at V_G (time fraction corresponding to a "high" voltage level of pulsed gate bias) and the time at zero gate bias (time fraction corresponding to the "low" voltage level). Stressing under both static and pulsed conditions was performed at temperatures ranging from 125 to 175 °C.

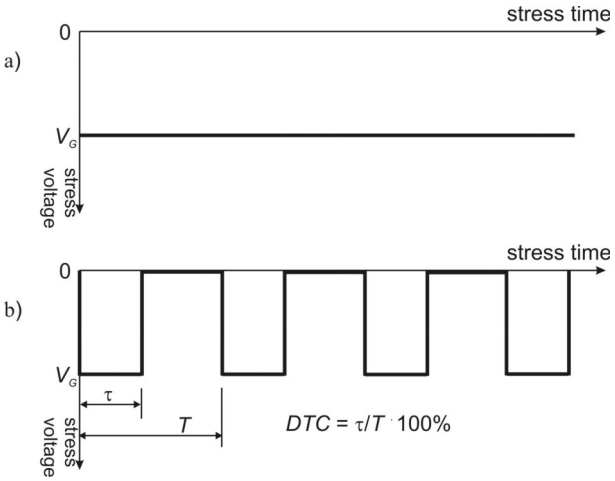

Figure 1: Stress voltage waveforms during the static a) and pulsed b) NBT stress.

Experimental setup for NBT stressing and electrical characterization of stressed devices (measurements of transfer *I-V* characteristics) is illustrated in Fig. 2. As the

accelerated stressing of the above power devices required voltage amplitudes even exceeding 40 V, which were beyond the capabilities of commonly used signal source units [22-24], the inclusion of an external amplifier (booster) between the source unit and the device under test (DUT) was necessary to supply the required stress voltage to DUT. Switches S1 and S2 were used to separate high-voltage stress circuit from the low-voltage measurement circuit (source and drain of DUT were tied to ground during the stress). Gate stress voltage was obtained from the source unit acting either as a dc source or a pulse generator (Tektronix AFG3102), for static and pulsed NBT stress conditions, respectively. Swept gate measurement voltage was provided from the Agilent 6645A source unit, while an Agilent 4156C semiconductor parameter analyzer was used as the source-measure unit for drain biasing and drain current measurements. All the instrumentation, along with the temperature inside the chamber (Heraeus HEP2), have been computer controlled over IEEE-488 GPIB bus.

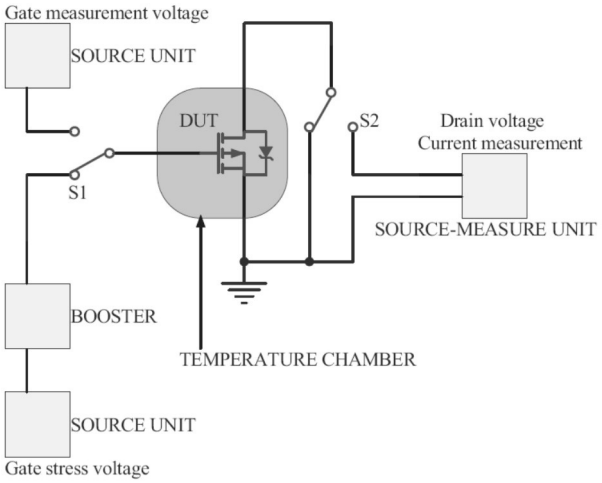

Figure 2: Block diagram for NBT stress and fast measurement on p-channel power VDMOS transistor.

Typical transfer *I-V* characteristics of p-channel power VDMOSFETs measured during the static and pulsed NBT stressing with V_G = – 45 V at 175 °C are shown in Figs. 3 and 4, respectively. It can be seen that, as the stressing progressed, the characteristics were being shifted along the V_{GS} axis towards the higher voltage values, which was the consequence of stress-induced buildup of oxide-trapped charge. The shifts were more significant in the case of static NBT stressing. Also, in both cases the shifts were more pronounced in the early phase of stressing and gradually became smaller in the advanced phase. At the same time, the slope of the transfer characteristics slightly decreased, indicating that interface traps were being generated as well.

Dependencies of stress-induced threshold voltage shifts (ΔV_T) on NBT stress time in devices stressed at several different temperatures with different gate voltages for both static and pulsed stress conditions are shown in Fig. 5. As can be seen, NBT stressing under both static and pulsed gate bias conditions was found to cause significant threshold voltage shifts, which in accordance with observed shifts of transfer characteristics along the voltage axis were more pronounced at higher voltages and/or temperatures. The threshold voltage shifts in the case of pulsed NBT stress appeared with rather significant time delay (30-60 minutes after the start of stressing), which was found to depend on stress temperature and pulse magnitude. In addition, the pulsed stressing caused generally lesser shifts as compared to static stressing performed at the same temperature with the same magnitude of stress voltage. The reason for the observed delay and lesser shifts in the case of pulsed NBT stress can be found in the nature of pulsed stressing itself. As already mentioned, "stress time" in the case of pulsed stress refers to the total time, which includes the time fractions corresponding to both "high" and "low" levels of the pulsed gate voltage applied. Devices are actually stressed only during the time fraction corresponding to a "high" voltage level of pulsed stress voltage, so the actual stress time is significantly shorter than the total time. Also, threshold voltage tends to recover during the time fraction corresponding to a "low" level, and this dynamic recovery of threshold voltage is an additional reason why the resulting shifts appear more slowly and are lower in the case of pulsed NBT stress.

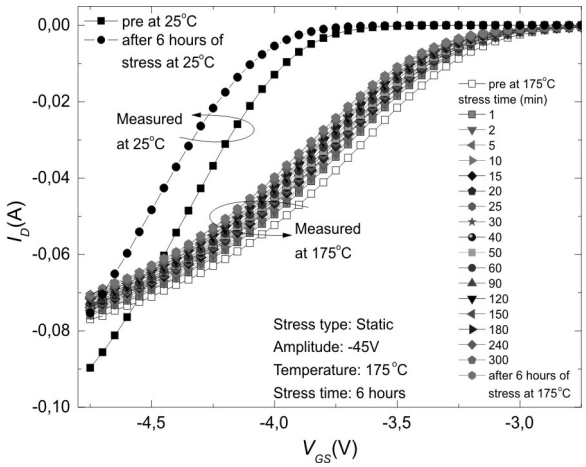

Figure 3: I_D-V_{GS} characteristics of p-channel power VDMOSFETs during the static NBT stressing.

3. NBTI effects on device lifetime

Degradation associated with NBTI can put serious limit to the lifetime of devices operated at elevated temperatures under the increased gate oxide electric field. Our goal in this study was to estimate normal operation lifetime of investigated p-channel power VDMOSFETs

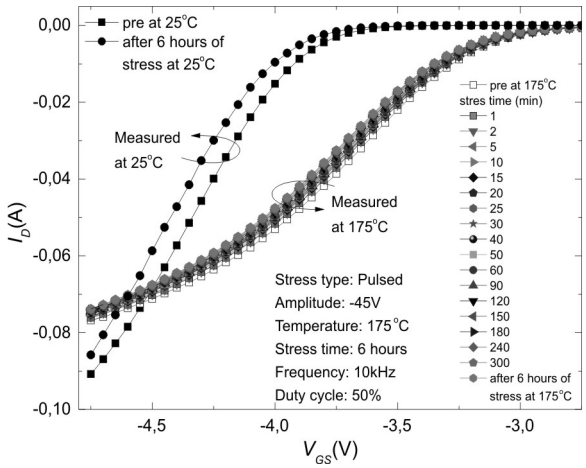

Figure 4: I_D-V_{GS} characteristics of p-channel power VDMOSFETs during the pulsed NBT stressing.

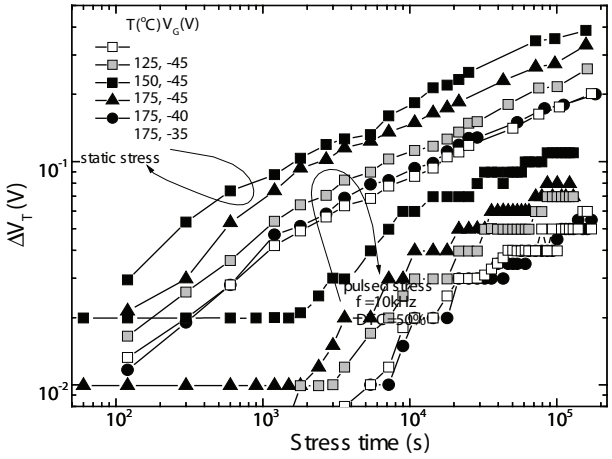

Figure 5: Threshold voltage shifts in p-channel VDMOSFETs during the static and pulsed (f = 10 kHz, DTC=50%) NBT stressing at different voltage magnitudes and temperatures.

by using the experimental data obtained under accelerated NBT stress conditions. Devices under test were the power transistors, so we could assume maximum normal bias V_G = – 20 V and temperature T = 100 °C.

To estimate the device lifetime it is necessary to choose one of device parameters affected by the stress, which would be suitable to monitor the level of stress-induced degradation, as well as to define an appropriate failure criterion (FC) as a maximum allowed change of the chosen parameter that is critical for device and/or circuit reliable operation. Various parameters, such as threshold voltage, transconductance, or drain current, can be used as degradation monitor for the lifetime estimation [25, 26]. Threshold voltage has widely been accepted as a well-suited parameter, so in this study we will use the experimental results for NBT stress-induced threshold voltage shift as degradation monitor to estimate device lifetime in practical operation.

The standard procedure of lifetime estimation requires first to extract the values of lifetime the devices would have if operated under the experimental conditions, and then use these experimental lifetime values for extrapolation to normal operating conditions.

3.1. Extraction of experimental lifetime data

Experimental lifetime is defined as the stress time required for the stress-induced ΔV_T to reach failure criterion, which in our case was set at 50 mV (a proper choice of failure criterion is important, and was discussed in our earlier paper [18]). The extraction of experimental lifetime values from our data, for stressing with different gate voltage magnitudes at T = 150 °C and for stressing with V_G = – 35 V at different temperatures, is illustrated in Figs. 6 and 7, respectively. It can be seen, for example in Fig. 6, that we could not get experimental lifetime for devices pulsed stressed with – 35 V at 150 °C since in this case ΔV_T did not reach 50 mV even after 72 hours of stressing. Thus, duration of the experiment in this case was not sufficient to achieve ΔV_T as high as FC, which means the stress time should have been extended to exceed the device lifetime for a given combination of stress bias and temperature. However, this could require the stressing to be done beyond the reasonable time limit, so in such cases it is convenient to use an adequate fitting model capable to provide reliable prediction of ΔV_T on the bases of available data. There are several well-established fitting models for prediction of ΔV_T, such as regular exponential model, 2-tau exponential model and stretched exponential model [27-30]. The best fit to our experimental results on power VDMOS devices was found to yield the stretched exponential model, which is given by [12, 29, 30]:

$$\Delta V_T(t) = \Delta V_{T\max} \cdot [1 - \exp(-(t/\tau_o)^{\beta})] \quad (1)$$

where ΔV_{Tmax}, τ_o, and β are the fitting parameters. Both experimental and fitting results for threshold voltage shifts during the pulsed NBT stressing of IRF9520 p-channel power devices with – 35 V at 150 °C are shown in Fig. 6. As can be seen, experimental lifetime $\tau 6$ is obtained as the time required that stretched exponential fit for ΔV_T reaches 50 mV. Similarly, stretched exponential fits were used in Fig. 7 to obtain the experimental lifetime values $\theta 5$ and $\theta 6$ for devices pulsed stressed with – 35 V at 150 °C and 125 °C.

3.2. Extrapolation to normal operating voltage

Extrapolation along the voltage or electric field axis by any of the commonly used models, such as V_G, $1/V_G$ and power-law models, which are based on corresponding degradation models for the threshold voltage shifts

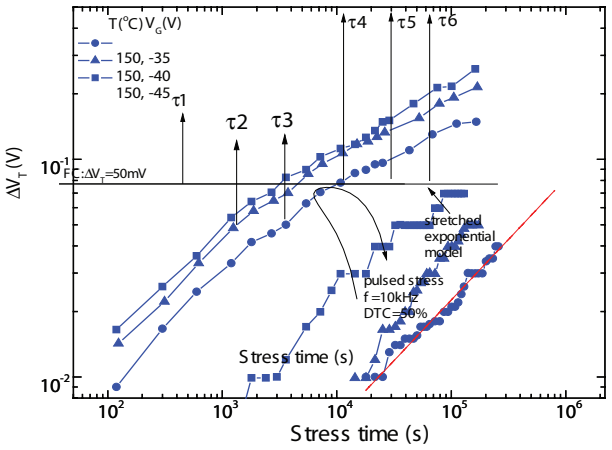

Figure 6: Extraction of experimental lifetime from the threshold voltage shift time dependencies recorded during the NBT stressing with different gate voltage magnitudes at $T = 150$ °C.

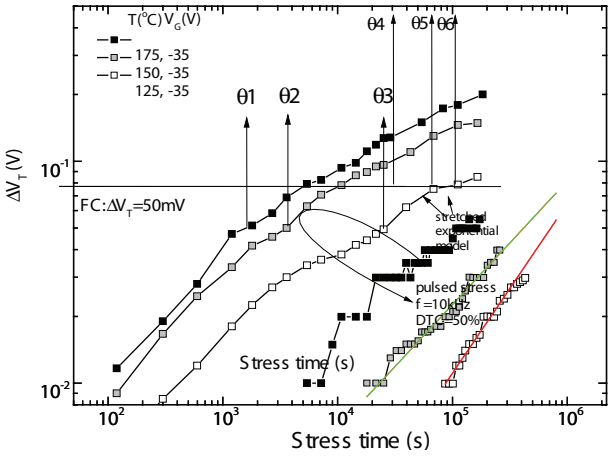

Figure 7: Extraction of experimental lifetime from the threshold voltage shift time dependencies recorded during the NBT stressing with gate voltage $V_G = -35$ V at different temperatures.

[9, 10], requires experimental lifetime values extracted from the data obtained by stressing with different voltages at constant temperature, such as those shown in Fig. 6. Here we use the $1/V_G$ model to estimate lifetime in devices subjected to NBT stress, which is illustrated in Fig. 8 a) for static and b) for pulsed bias conditions. Only extrapolation to $V_G = -20$ V is shown, but the procedure can be used to estimate the lifetime by extrapolation to any other reasonable operation voltage. The procedure additionally allows for estimation of another reliability parameter, so-called "ten year operation voltage", V_{G10Y}, which is defined as maximum gate voltage that allows 10 years of device operation at given temperature so that stress-induced threshold voltage shift remains below the FC. In Fig. 8 only the V_{G10Y} value for devices stressed at 125 °C is indicated, but the values for the other two stress temperatures can be read as well. As can be seen, there are significant differences in lifetime and ten year operation voltage values between devices stressed under the static and pulsed NBT stress conditions. The lifetime values obtained by extrapolation to – 20 V are more than two orders of magnitude higher under the pulsed gate bias conditions (XP1, XP2, XP3) than under the static ones (XS1, XS2, XS3). Also, the ten year operation voltage is 5÷8 V higher under the pulsed voltage regime ($V_{G\ 10Y}^{P}$) than under the static one ($V_{G\ 10Y}^{S}$). These findings indicate that in many real applications of p-channel power MOSFETs, where gate bias switches between the "high" and "low" levels, devices may maintain their proper functionality much longer than if kept constantly under the dc bias.

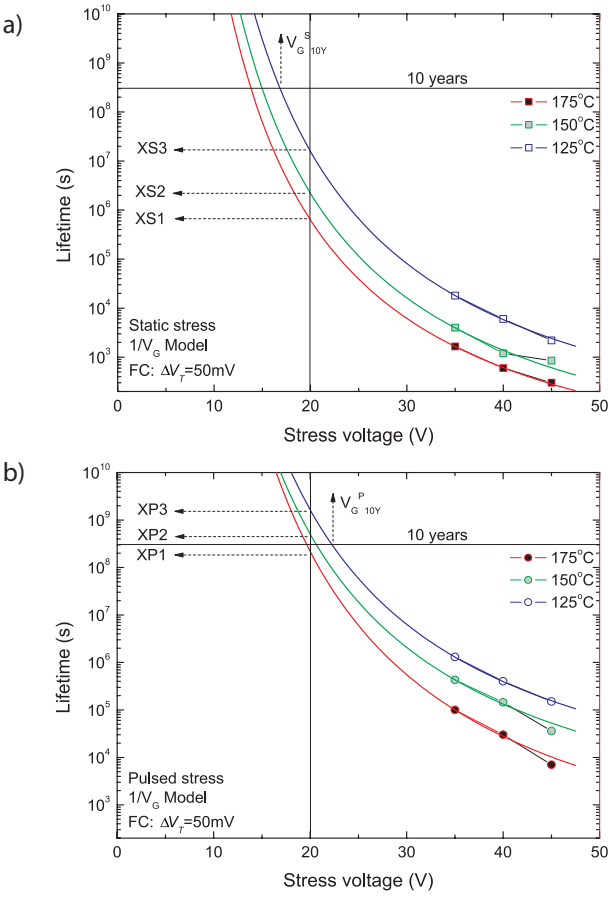

Figure 8: Extrapolation to normal operation gate bias by means of $1/V_G$ model to estimate the lifetime and ten year operation voltage in p-channel power VDMOSFETs subjected to a) static and b) pulsed NBT stressing.

3.3 Extrapolation to normal operating temperature

The $1/V_G$ and other models for extrapolation along the voltage or electric field axis can be used to estimate device reliability parameters (lifetime and ten year operation voltage) for any operating voltage, but only at temperatures applied during accelerated stress experiments, which are generally higher than actual temperatures found in device normal operation mode.

Estimates obtained by these models are very convenient as the worst case expectations, but it could be very useful if possible to estimate the lifetime for normal operation temperatures as well. As a possible solution, we have recently proposed the use of suitable model for extrapolation along the temperature axis [11-13]. The model is easily derived from any of several degradation models for NBT stress-induced threshold voltage shift, which all include the Arrhenius temperature acceleration factor, and can be expressed as:

$$\tau = A \cdot \exp(B / T), \quad (2)$$

where A and B are the fitting parameters taken from the initial degradation model. This model apparently takes the same mathematical form as $1/V_G$ model, and is thus called "1/T" model.

The use of 1/T model requires experimental lifetime values extracted from the data for NBT stressing performed with the same voltage magnitude at several different temperatures, such as those plotted in Fig. 7. The lifetime estimation by means of this model is illustrated in Fig. 9. Only extrapolation to T = 100 °C (which seems rather realistic for operation of power devices) is shown, but the same procedure can be used to estimate device lifetime by extrapolation to any other reasonable operation temperature. Fig. 9 also illustrates that extrapolation procedure by means of the 1/T model, in analogy with the $1/V_G$ model, allows for estimation of an additional reliability parameter, which is accordingly called "ten year operation temperature", T_{10Y}, and is defined as maximum temperature that allows 10 years of device operation under given V_G so that stress-induced ΔV_T remains below FC. As can be seen, 1/T model also yields significant differences between the effects of static and pulsed NBT stress. The lifetime at 100 °C is about two orders of magnitude higher under the pulsed bias conditions (YP1, YP2 and YP3) than under the static ones (YS1, YS2 and YS3). Also, the ten year operation temperature is 8÷18 °C higher under the pulsed regime (T^P_{10Y}) than under the static one (T^S_{10Y}). These observations are completely in line with those obtained by means of $1/V_G$ model.

3.4 Double extrapolation along the voltage and temperature axes

Each of the two extrapolation procedures considered so far disregards one of the stress acceleration factors, either temperature or voltage, so both procedures may underestimate device reliability parameters. The goal of our study was to estimate the lifetime of investigated VDMOSFETs under normal operating conditions (both voltage and temperature) using the results obtained by accelerated NBT stressing. A reasonable solution could be found by combining the two procedures, i.e. by performing two successive extrapolations along the gate voltage (or corresponding electric field) and temperature axes, where the latter extrapolation uses the results of the former one as the input data [11, 12]. This is shown in Fig. 10, which illustrates extrapolation along the temperature axis to 100°C by 1/T model, where the results of previous extrapolation along the voltage axis to – 20 V by $1/V_G$ model from Fig. 8 (XS1, XS2, and XS3 for static stress; XP1, XP2, and XP3 for pulsed stress) have been taken as the input data. As can be seen, the two successive extrapolations yield a single lifetime projection to (– 20 V, 100 °C) for each of the two operating regimes considered (τ_{0S}, for static, and τ_{0P}, for pulsed regime). The order of performing the two extrapolations can be reversed: the YS1, YS2, and YS3 data (for static stress) and YP1, YP2 and YP3 data (for pulsed stress) from Fig. 9, obtained by extrapolation to a normal operation temperature by the 1/T model can be further used for extrapolation to a normal operation voltage by $1/V_G$ model, which is illustrated in Fig. 11. The two τ_{0S} values obtained in Figs. 10 and 11

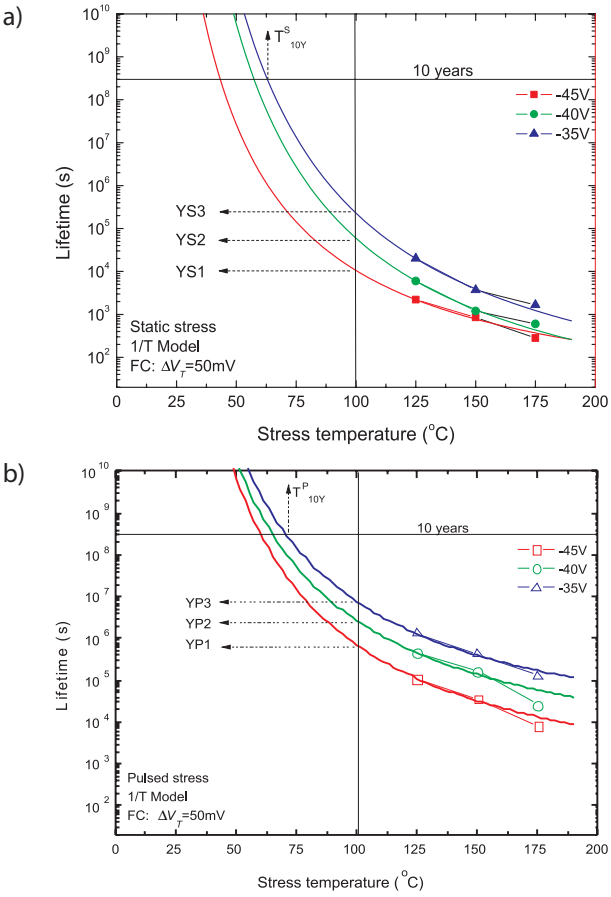

Figure 9: Extrapolation to normal operation temperature by means of 1/T model to estimate the lifetime and ten year operation temperature in p-channel power VDMOSFETs subjected to a) static and b) pulsed NBT stressing.

are close one to the other, and the two τ_{0P} values also are, so the order in performing the two extrapolations does not seem to be of great importance. Also, the results in both figures suggest the device lifetime under the pulsed operation regime could be more than one order of magnitude longer than under the static one. Yet, there are certain differences between the two τ_{0S} values, as well as between the two τ_{0P} values, obtained by the two procedures shown in Figs. 10 and 11. These differences, which are measure for the uncertainties in estimated lifetime values, could be associated with and may depend on variations in stress conditions applied, level of stress-induced degradation taken as the failure criteria, and features of the models used for extrapolation to normal operation conditions [12]. These uncertainties might be lesser if both extrapolation procedures were applied in parallel, so the average of the two estimated lifetime values could be taken as the most probable true lifetime.

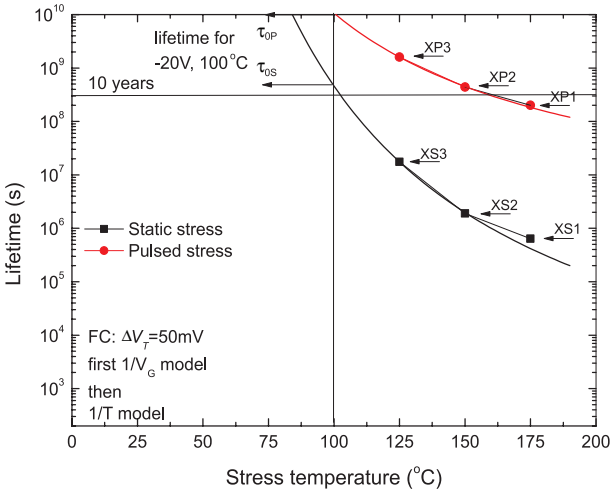

Figure 10: Lifetime extrapolation to normal operating conditions by 1/T model with input data taken from Fig. 8.

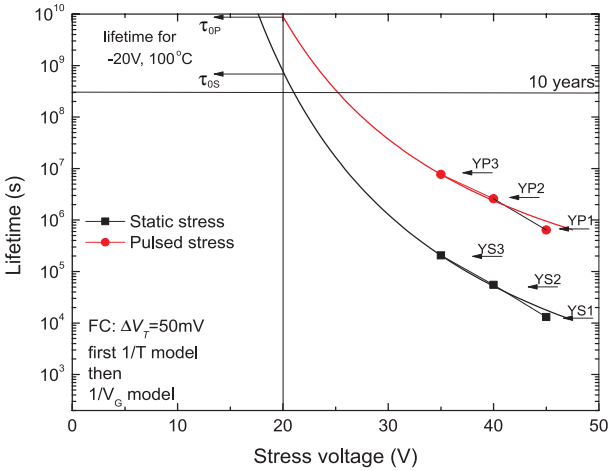

Figure 11: Lifetime extrapolation to normal operating conditions by $1/V_G$ model with input data taken from Fig. 9.

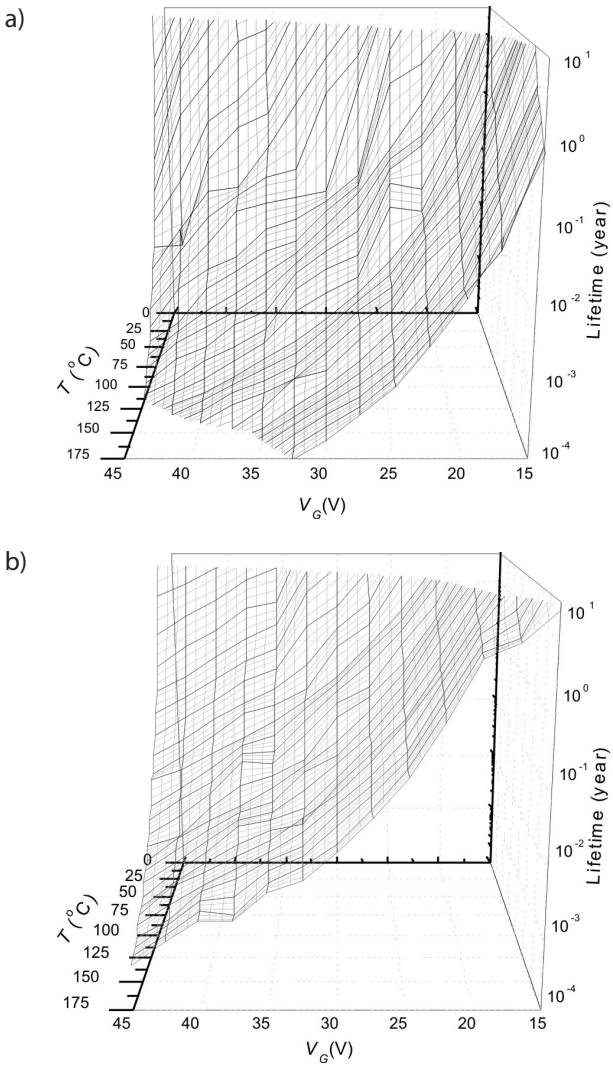

Figure 12: Surface areas representing the lifetime estimates in: a) static and b) pulsed NBT stressed devices for a full range of operating voltages and temperatures with ΔV_T =50 mV taken as a failure criterion.

The 1/T model for extrapolation along the temperature axis may be combined for double extrapolation not only with $1/V_G$ model but also with other models for extrapolation along the voltage axis (V_G model, power law model), where the best choice should be the model that provides the best fit to the data. It is also important to note that double extrapolation approach can be used to estimate device lifetime for any reasonable combination of operating voltages and temperatures, which means the procedure can be re-done for each combination falling within the entire range of operating voltages and temperatures. The set of results obtained in this way can be used to construct the surface area representing the lifetime values corresponding to a full range of device operating conditions. The approach has been applied to our experimental results for static and pulsed NBT stressed p-channel power VD-

MOS devices IRF9520, and Fig. 12 shows such surface areas representing lifetime projections to a full range of operating temperatures and gate voltages for devices operated under the a) static and b) pulsed stress conditions (threshold voltage shift of 50 mV has been taken as the failure criterion in both cases). As can be seen, surface area constructed for the static NBT stress appears to fall below the one for the pulsed stress, which means the lifetime is longer under the pulsed stress conditions than under the static ones independently on the choice of operation voltage magnitude and/or temperature. The appropriate surface areas can be created for different failure criteria, and may help in estimating either the lifetime or maximum allowed voltage and temperature for every single device in the operation environment.

4. Conclusion

NBT stress-induced threshold voltage shifts in p-channel power VDMOSFETs under the static and pulsed stress conditions were compared in terms of the effects on device lifetime. The $1/V_G$ model, for extrapolation along the voltage axis, and 1/T model, for extrapolation along the temperature axis, were used to get lifetime estimates for the voltages and temperatures expected in device normal operation mode. As a consequence of the shorter actual stress time and dynamic recovery effects, threshold voltage shifts were less significant under the pulsed stress conditions. Accordingly, estimated lifetime was much longer under the pulsed stress conditions than under the static ones, as shown by using each of the above two models individually, as well as by combined use of both models for double extrapolation along both voltage and temperature axes. Finally, double extrapolation approach was shown to allow for construction of the surface area representing lifetime values corresponding to a full range of device operating voltages and temperatures.

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A Simplified Approach to Analyze of Active Circuits Containing Operational Amplifiers

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Abstract: In this paper, a systematic and efficient formulation for analysis of active circuits containing operational amplifiers is presented. The modified nodal approach is used in obtaining system equations of active circuits. The model of operational amplifier relating to the used analysis method is given. The model is a matrix-based approach. Therefore, it allows computer-aided analysis of active circuits to be realized efficiently. Application examples are included into the study.

Key words: active circuits, op amp, model, modified nodal analysis

Poenostavljen pristop analize aktivnega vezja z operacijskim ojačevalnikom

Povzetek: V članku je predstavljen sistematična in učinkovita formulacija analize aktivnih vezij z operacijskim ojačevalnikom. Uporabljen je modificiran vozliščni pristop v sistemu enačb aktivnega vezja. Podan je model operacijskega ojačevalnika za uporabljeno metodo analize. Model je na osnovi matrike, kar omogoča učinkovito računalniško podprto analizo aktivnih vezij. Primeri so vključeni v študijo

Ključne besede: aktivna vezja, operacijski ojačevalnik, model, modificirana vozliščna analiza

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1. Introduction

Operational amplifiers (Op amp) are the most important elements of active circuits. They are used in many applications, such as active filters, amplifiers, digital to analog converter and analog to digital converter in circuit analysis and control systems. The ones interested in electrical, electronics and computer engineering generally have difficulties in obtaining system equations of active circuits containing operational amplifiers. It arises from Op amp models used for the formulation.

Singular network elements, nullator and norator, are used for analysis of Op amp circuits in [1]. It is very difficult to understand and realize the analysis with these elements. Wilson proposed a systematic procedure for analysis of Op amp circuits [2]. But, it has some restrictions about dependent sources and some circuit elements. Gottling presented the use of nodal and mesh methods by inspection in the analysis of active circuits [3]. It has a form similar to Wilson's matrix solution. Although it is more general, it involves very intensive mathematical processes and transformations.

In general, it is very suitable to use the modified nodal method for analysis of active circuits. The classical nodal method, before the modified nodal method, is used for both resistive circuit analysis (DC analysis) and dynamic circuit analysis in many introductory electric circuit textbooks [4-7]. The node voltage method using virtual current sources for special cases is realized in [8]. The nodal voltage method is based on a systematic application of Kirchhoff's current law (KCL). In this method, the circuit variables are node voltages. It provides a simple and systematic solution for circuits that contain only independent current sources and resistances/impedances. But, the classical nodal method has some restrictions. Every circuit element cannot be easily included into to the system equations. For analysis with this method, the circuits must not contain de-

pendent sources (excluding voltage-controlled current source) and voltage sources that are not transformable to current sources (independent or dependent). As an extension to the classical nodal voltage method, the modified nodal analysis (MNA) was first introduced by Ho et al [9] to overcome its shortcomings and has been developed more by including many circuit elements (transformer, semiconductor devices, short circuit, etc.) into the system equations so far. In this method, the system equations can be also obtained by inspection. Especially, it is very suitable for computer-aided analysis of active circuits. In this paper, it is shown how to include the terminal equations, the model, of operational amplifier into the MNA system.

The systematic synthesis of operational amplifier circuits is realized by admittance matrix expansion in [10]. Full model and characterization of noise in operational amplifier is given in [11]. Modeling of operational amplifier based on VHDL-AMS is presented in [12]. Several applications, such as filters, amplifiers, relating to Op amps are given in [13-18]. The Op amp is the premier linear active device in present-day analog integrated circuit applications. Therefore, it is very important to model the Op amp for system analysis.

The paper is organized as follows. In Section 2, the modified nodal analysis is explained. Section 3 summarizes the fundamental characteristics of Op amp, before including it into the MNA system. In Section 4, we develop the MNA model of Op amp. Application examples of the approach are given in Section 5. The paper concludes in Section 6.

2. Modified Modal Analysis

The MNA method allows the system equations to be obtained easily and systematically without any limitations. Therefore, it is very understandable analysis method in system analysis. The main advantage is that the system equations can be also obtained by inspection. In this method, there are both voltage variables and current variables. The modified nodal equations in Laplace (s) domain can be written in the following form.

$$[G + sC]X(s) = BU(s) \tag{1}$$

Where, G, C, B are coefficients matrices. All conductance and frequency-independent values arising in the MNA formulation are stored in matrix G, whereas values of capacitors and inductors are stored in matrix C because they are associated with the frequency. Inductors are included in impedance form, capacitors and resistors are included in admittance form into the MNA system. U(s) represents the source vector containing the independent current and voltage sources. X(s) is the unknown vector in s-domain. In this method, in addition to node voltages, currents of inductors, currents of independent and dependent voltage sources are also taken as variables. The idea underlying this formulation is to split the elements into two groups; the first one is formed by elements which have an admittance description and the other by those which do not. Taking into account the types of variables, the unknown vector and coefficient matrices are partitioned as follows.

$$\left\{\begin{bmatrix} G_A & G_{AB} \\ G_{BA} & G_B \end{bmatrix} + s\begin{bmatrix} C_A & 0 \\ 0 & L_A \end{bmatrix}\right\}\begin{bmatrix} X_1(s) \\ X_2(s) \end{bmatrix} = B\begin{bmatrix} E(s) \\ J(s) \end{bmatrix} \tag{2}$$

Where, $X_1(s)$ represents the node voltage variables, $X_2(s)$ represents the current variables. $X_2(s)$ also expresses required additional variables in the formulation of MNA. G_A is conductance matrix. G_{AB} and G_{BA} ($=G_{AB}^T$) are incidence matrices relating to the connection of elements, whose currents are introduced as variables, to the rest of circuit. G_B contains the controlling constants of dependent sources. C_A and L_A are capacitance and inductances matrices, respectively. E(s) and J(s) are independent voltage and current sources. If there are n nodes and m current variables in a circuit, $X_1(s)$ vector contains n−1 nodal voltage variables except reference node (ground) and $X_2(s)$ vector contains m current variables. Thus, the unknown vector X(s) contains n−1+m variables as seen in Eq. (3).

$$X_1(s) = \begin{bmatrix} U_1 \\ U_2 \\ \vdots \\ U_{n-1} \end{bmatrix}, \quad X_2(s) = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_m \end{bmatrix} \Rightarrow X(s) = \begin{bmatrix} X_1(s) \\ \cdots\cdots \\ X_2(s) \end{bmatrix} = \begin{bmatrix} U_1 \\ \vdots \\ U_{n-1} \\ \cdots\cdots \\ I_1 \\ \vdots \\ I_m \end{bmatrix} \tag{3}$$

3. Op-Amp Model

Op amp circuits are fundamental building blocks in a wide range of signal processing applications, especially instrumentation, status monitoring, process control, filtering, digital to analog conversion and analog to digital conversion. Before obtaining the MNA model of Op amp, the fundamental properties of Op amp (Fig. 1) should be summarized. An ideal operational amplifier has the following characteristics: infinite gain for differential input signal, zero gain for common mode input signal, infinite input impedance, zero output impedance and infinite bandwidth. The transfer characteristic of Op amp is shown in Fig. 1. b. It explains the relationships between the input voltages (U_p,U_n) and

the output voltage (U_o). In the linear region, the input-output relation is

$$U_o = A(U_p - U_n) = AU_d \quad (4)$$

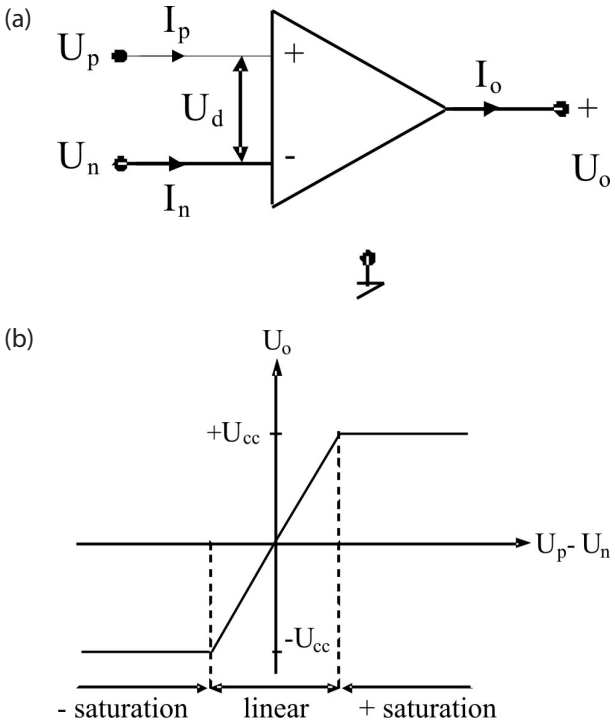

Figure 1: (a) Op amp, (b) Op amp characteristics

In analog integrated circuits, Op amps usually operate in the linear mode. The equivalent circuit model of Op amp operating in its linear range is shown in Fig. 2.a, where R_i is the input resistance, R_o the output resistance. It also contains the voltage controlled voltage source whose gain is A. The ideal Op amp has $R_i=\infty$, $R_o=0$, $A=\infty$ (Fig. 2.b). In the ideal Op amp operating in the linear mode, U_o is limited, the potential difference between input terminals must be zero as A approaches infinity ($A\rightarrow\infty$).

$$U_o = A(U_p - U_n) = AU_d \quad \rightarrow \quad U_d = \frac{U_o}{A} = U_p - U_n = 0 \quad (5.a)$$

$$U_p = U_n \quad (5.b)$$

Since the input resistance of ideal Op amp is infinite, the input currents must be zero.

$$I_p = 0, \quad I_n = 0 \quad (6)$$

According to the Op amp constraints, given in Eq. (5) and Eq. (6), Op amp is a linear and time-invariant device. Because $I_p=I_n=0$ and $U_p=U_n$, the input terminals of Op amp are simultaneously short circuit ($U_p=U_n$) and open circuit ($I_p=I_n=0$). It is an interesting property of the Op amp.

4. MNA model of Op amp

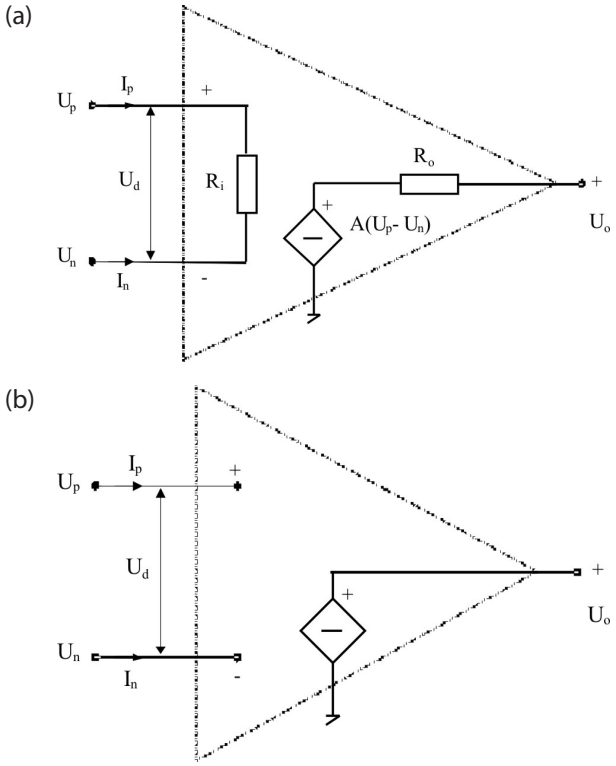

Figure 2: (a) Equivalent circuit of Op Amp, (b) Ideal Op Amp model

The ideal Op amp concept is a good approximation to analyze the Op amp circuits. Therefore, this concept will be used for developing the MNA model of Op amp. For MNA structure, first, the terminal equations of Op amp (Op amp constraints), given in Eq. (5) and Eq. (6), are expressed together as in Eq.(7).

$$\begin{bmatrix} I_p \\ I_n \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} U_p \\ U_n \\ 0 \end{bmatrix} \quad (7)$$

As explained in Section 2, there are m current variables, $X_2(s)$, in the MNA system. I_p, I_n currents of Op amp are located in $X_2(s)$ vector. The short circuit property of input terminals of Op amp is included as an additional equation into the MNA system, as will be explained in the following.

Let an active circuit contain n nodes, including three terminals (nodes) of Op amp. In the MNA system, there

are n–1 nodal voltage variables, $X_1(s)$. In the ideal Op amp model (Fig. 2.b), the output voltage of Op amp is determined by other nodal voltages because of the dependent voltage source connected between the output terminal and ground. Therefore, it is not necessary to write a nodal equation at the output node of Op amp. If there is an Op amp in a circuit, we formulate nodal equations at other n–2 nonreference nodes. Since there are n–1 nodal voltages in the system, we seem to have more unknowns than equations. However, the short circuit property of input terminals of Op amp (U_p–U_n=0) supplies an additional equation into the system. If a circuit contains k Op amps, n–1–k nodal equations are formulated, except output terminals of Op amps, and k additional equations relating to the short circuit property of input terminals are included into the system equations.

In Eq. (8), it is shown how to include the terminal equations of Op amp, input currents and short circuit property in Eq. (7), into the MNA system in Eq. (1). The constraints of Op amp are stored in matrices G and B. Eq.(8) gives the MNA model of Op amp. This model contains both the short circuit property (U_p–U_n=0) and the open circuit property (I_p=I_n=0) of input terminals of Op amp.

$$GX(s) + sCX(s) = BU(s)$$

$$\underbrace{\begin{bmatrix} \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 1 & -1 & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \end{bmatrix}}_{G} \underbrace{\begin{bmatrix} \vdots \\ U_p \\ U_n \\ \vdots \\ \cdots \\ \vdots \\ I_p \\ I_n \\ \vdots \end{bmatrix}}_{X(s)} = \underbrace{\begin{bmatrix} \vdots \\ \cdots \\ \vdots \\ 0 \\ 0 \\ 0 \\ \vdots \end{bmatrix}}_{B} U(s) \quad (8)$$

In the MNA model, given by Eq. (8), the current constraints of the ideal Op Amp concept, I_p=I_n=0, appear to be fairly useless because it draws no currents at its inputs. Therefore, these currents can be ignored when formulating the MNA system in order that the system matrix has min. dimensions, as done in Examples. It is sufficient to take into consideration the short circuit property of input terminals of Op amp. Consequently, the MNA model of Op amp can be also expressed as in Eq. (9). This model can be also included into the system equations by inspection. In the examples of Section 5, for the MNA model of Op amp, Eq. (9) is used in order that the system equations have min. variables.

$$\underbrace{\begin{bmatrix} \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 1 & -1 & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \end{bmatrix}}_{G} \underbrace{\begin{bmatrix} \vdots \\ U_p \\ U_n \\ \vdots \\ \cdots \\ \vdots \\ I_p \\ I_n \\ \vdots \end{bmatrix}}_{X(s)} = \underbrace{\begin{bmatrix} \vdots \\ \cdots \\ \vdots \\ 0 \\ \vdots \end{bmatrix}}_{B} U(s) \quad (9)$$

5. Application Examples

In this section, the analysis of three active circuits containing Op amp are realized by the presented model. The first example is the differential amplifier circuit having two inputs. The second one is the high-pass Butterworth active filter circuit containing energy storage elements (capacitor). The band-pass Butterworth state-variable filter is used to demonstrate the use of Op amps in cascade connection in the last example.

Example 1: Consider the differential amplifier circuit in Fig. 3. It has two input signals.

The circuit has n-1=5 nonreference nodes, including input-output terminals of Op Amp. Thus, in the MNA system, X_1 vector contains 5 nodal voltage variables. Normally, it requires to be obtained an equation for every node. But, it is not necessary to write a nodal equation for output node (node e) because of the features of ideal Op amp, as explained in Section 4. The voltage and current constraints of Op Amp are included into the system equations, as shown in the MNA model of Op Amp in Eq. (8) or Eq. (9). There is no need to put the input terminal currents of the Op amp into the MNA system according to Eq. (9). Therefore, the current variables in X_2 vector are only source currents. They are relating to additional equations.

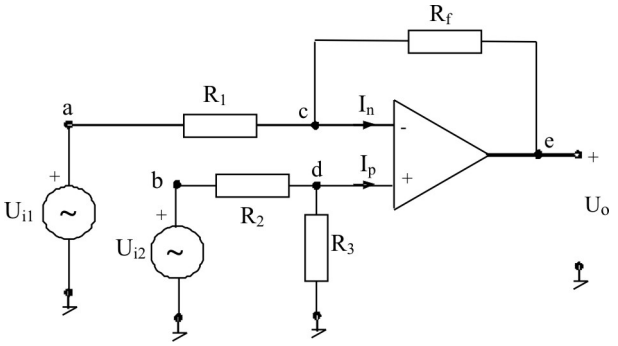

Figure 3: Differential amplifier

The nodal (main) equations of the differential amplifier:

$$a \rightarrow \; G_1(U_a - U_c) + I_{Ui1} = 0$$
$$b \rightarrow \; G_2(U_b - U_d) + I_{Ui2} = 0$$
$$c \rightarrow \; G_f(U_c - U_e) - G_1(U_a - U_c) + I_n = 0$$
$$d \rightarrow \; G_3 U_d - G_2(U_b - U_d) + I_p = 0$$

Additional equations: $U_c - U_d = 0 \rightarrow$ Op Amp constraint, $I_p = 0, \; I_n = 0$

$$U_a = U_{i1}$$
$$U_b = U_{i2}$$

The overall equations constitute the MNA system (Eq. 10). They are represented in matrix form, as in Eq. (1) or Eq. (2). Since the circuit has no storage elements, Matrix C is not available. The MNA model of Op Amp, given by Eq. (9), can be also seen from system equations in Eq. (10).

$$GX(s) = BU(s) \rightarrow \begin{bmatrix} G_A & \vdots & G_{AB} \\ \cdots\cdots & \cdots & \cdots\cdots \\ G_{BA} & \vdots & G_B \end{bmatrix} \begin{bmatrix} X_1(s) \\ \cdots\cdots \\ X_2(s) \end{bmatrix} = BU(s)$$

$$\begin{bmatrix} G_1 & 0 & -G_1 & 0 & 0 & \vdots & 1 & 0 \\ 0 & G_2 & 0 & -G_2 & 0 & \vdots & 0 & 1 \\ -G_1 & 0 & G_1+G_f & 0 & -G_f & \vdots & 0 & 0 \\ 0 & -G_2 & 0 & G_2+G_3 & 0 & \vdots & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & \vdots & 0 & 0 \\ \cdots & \cdots & \cdots\cdots & \cdots\cdots & \cdots & \cdots & \cdots & \cdots \\ 1 & 0 & 0 & 0 & 0 & \vdots & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & \vdots & 0 & 0 \end{bmatrix} \begin{bmatrix} U_a \\ U_b \\ U_c \\ U_d \\ U_e \\ \cdots \\ I_{Ui1} \\ I_{Ui2} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ \cdots & \cdots \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} U_{i1}(s) \\ U_{i2}(s) \end{bmatrix}$$

Additional equations

(10)

The output voltage, $U_o = U_e$, is obtained by solving the system equations as follows;

$$U_o(s) = -\frac{R_f}{R_1} U_{i1}(s) + \left(\frac{R_3(R_f + R_1)}{R_1(R_2 + R_3)} \right) U_{i2}(s)$$

Example 2: Consider the high-pass Butterworth filter circuit in Fig. 4. It has two energy storage elements.

The circuit has n−1=5 nonreference nodes, including input-output terminals of Op Amp. Therefore, X_1 vector contains 5 nodal voltage variables. It is not necessary to write a nodal equation for output node (node e) and to put the input terminal currents of the Op amp into the MNA system according to Eq. (9).

The nodal (main) equations of high-pass Butterworth filter circuit**:**

$$a \rightarrow \; sC_1(U_a - U_b) + I_{Ui} = 0$$
$$b \rightarrow \; sC_2(U_b - U_c) - sC_1(U_a - U_b) + G_1(U_b - U_e) = 0$$
$$c \rightarrow \; G_2 U_c - sC_2(U_b - U_c) + I_p = 0$$
$$d \rightarrow \; G_b U_d - G_a(U_e - U_d) + I_n = 0$$

Additional equations : $U_c - U_d = 0 \rightarrow$ Op Amp constraint, $I_p = 0, \; I_n = 0$

$$U_a = U_i$$

The overall equations constitute the MNA system (Eq.11). They are represented in matrix form, as in Eq.(1).

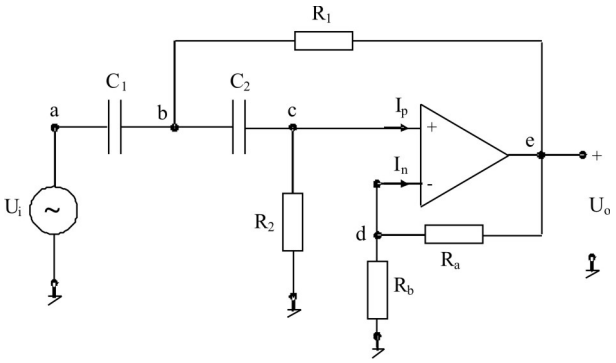

Figure 4: High-pass Butterworth active filter circuit

$$[G + sC]X(s) = BU(s)$$

$$\begin{bmatrix} sC_1 & -sC_1 & 0 & 0 & 0 & \vdots & 1 \\ -sC_1 & G_1+sC_1+sC_2 & -sC_2 & 0 & -G_1 & \vdots & 0 \\ 0 & -sC_2 & G_2+sC_2 & 0 & 0 & \vdots & 0 \\ 0 & 0 & 0 & G_a+G_b & -G_a & \vdots & 0 \\ 0 & 0 & 1 & -1 & 0 & \vdots & 0 \\ \cdots & \cdots\cdots & \cdots & \cdots\cdots & \cdots & \cdots & \cdots \\ 1 & 0 & 0 & 0 & 0 & \vdots & 0 \end{bmatrix} \begin{bmatrix} U_a \\ U_b \\ U_c \\ U_d \\ U_e \\ \cdots \\ I_{Ui} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \cdots \\ 1 \end{bmatrix} U_i(s)$$

Additional equations

(11)

The output voltage, $U_o = U_e$, is obtained by solving the system equations as follows;

$$U_o(s) = \frac{s^2 R_1 R_2 C_1 C_2 (R_a + R_b)}{s^2 R_1 R_2 R_b C_1 C_2 + s(R_1 R_b C_1 + R_1 R_b C_2 - R_a R_2 C_2) + R_b} U_i(s)$$

Example 3: Consider the band-pass Butterworth state-variable filter circuit in Fig. 5. Here, the use of Op amps in cascade connection is shown. It will be seen how much the model simplify the solution of complex Op amp circuits by dint of its efficient formulation. The state-variable filter uses three Op amps, two integrators and one summing amplifier. The main advantageous of the state variable filter is that it has low-pass (LP), high-pass (HP) and band-pass outputs (BP). In Fig. 5, these outputs are shown as U_{LP}, U_{HP} and U_{BP}, respectively.

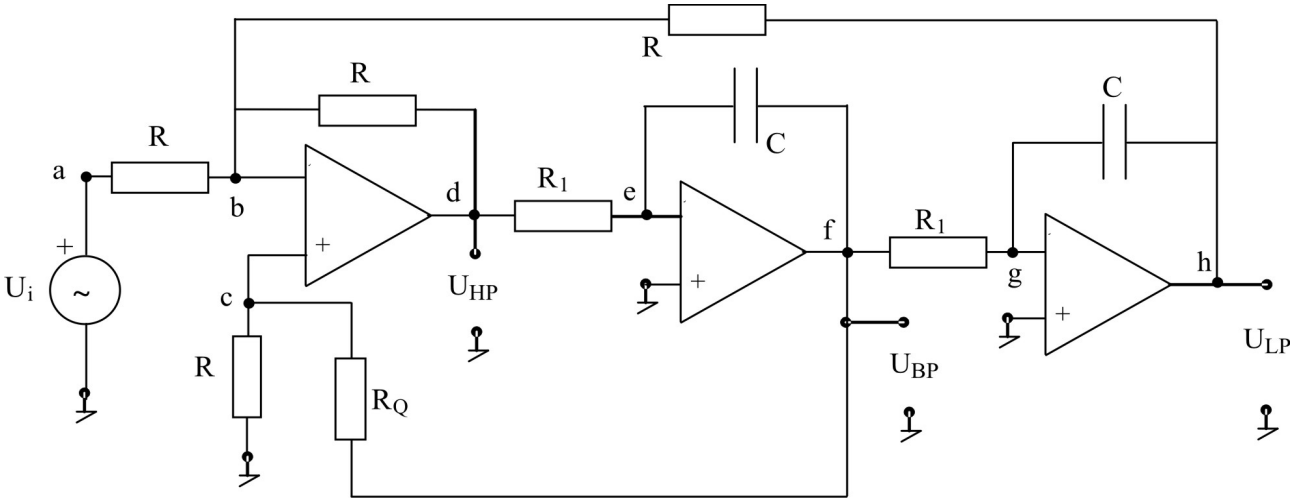

Figure 5: Band-pass Butterworth state-variable filter circuit

The circuit has n-1=8 nonreference nodes, including input-output terminals of Op Amps. Therefore, X_1 vector contains 8 nodal voltage variables. It is not necessary to write nodal equations for output nodes (node d, f, h) and to put the input terminal currents of the Op amps into the MNA system according to Eq. (9). In the system equations and Fig. 5, these currents are not shown.

The nodal (main) equations of the circuit**:**

$$a \rightarrow \quad G(U_a - U_b) + I_{Ui} = 0$$

$$b \rightarrow \quad G(U_b - U_d) - G(U_a - U_b) + G(U_b - U_h) = 0$$

$$c \rightarrow \quad GU_c + G_Q(U_c - U_f) = 0$$

$$e \rightarrow \quad G_1(U_e - U_d) + sC(U_e - U_f) = 0$$

$$g \rightarrow \quad G_1(U_g - U_f) + sC(U_g - U_h) = 0$$

Additional equations: $U_b - U_c = 0 \quad , U_e = 0, \quad U_g = 0$

$$U_a = U_i$$

The overall equations constitute the MNA system (Eq.12).

$$\begin{bmatrix} G & -G & 0 & 0 & 0 & 0 & 0 & 0 & \vdots & 1 \\ -G & 3G & 0 & -G & 0 & 0 & 0 & -G & \vdots & 0 \\ 0 & 0 & G+G_Q & 0 & 0 & -G_Q & 0 & 0 & \vdots & 0 \\ 0 & 0 & 0 & -G_1 & G_1+sC & -sC & 0 & 0 & \vdots & 0 \\ 0 & 0 & 0 & 0 & 0 & -G_1 & G_1+sC & -sC & \vdots & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & \vdots & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & \vdots & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & \vdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \vdots & 0 \end{bmatrix} \begin{bmatrix} U_a \\ U_b \\ U_c \\ U_d \\ U_e \\ U_f \\ U_g \\ U_h \\ \cdots \\ I_{Ui} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \cdots \\ 1 \end{bmatrix} U_i(s)$$

(Additional equations)

(12)

The filter outputs, $U_{LP}=U_l$, $U_{HP}=U_d$, $U_{BP}=U_g$ are obtained by solving the system equations as below.

$$U_{LP}(s) = U_h(s) = \frac{-(R_Q + R)}{s^2 R_1^{\,2} C^2 (R_Q + R) + 3sRR_1C + R_Q + R} U_i(s)$$

$$U_{HP}(s) = U_d(s) = \frac{-s^2 R_1^{\,2} C^2 (R_Q + R)}{s^2 R_1^{\,2} C^2 (R_Q + R) + 3sRR_1C + R_Q + R} U_i(s)$$

$$U_{BP}(s) = U_f(s) = \frac{sR_1C(R_Q + R)}{s^2 R_1^{\,2} C^2 (R_Q + R) + 3sRR_1C + R_Q + R} U_i(s)$$

6. Conclusion

The main difficulty in obtaining the system equations of active circuits containing Op Amps in system analysis arises from Op Amp models used for the formulation. In this paper, an efficient and systematic approach for analysis of active circuits containing Op Amps has been presented. The modified nodal approach, very understandable analysis method, is used in obtaining the system equations. The fundamental characteristics of Op amp have been summarized and the MNA model of Op amp has been developed. As a result, a matrix-based framework for computer-aided analysis of active circuits has been formulated. The model is general, systematic and can be applied to all possible active circuit structures. Examples are included to show the efficiency of the analysis method and the MNA model of Op amp. Using the presented model, it can be easily obtained system equations of Op Amp circuits by inspection and also, can be written a computer program about analysis of active circuits.

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Investigation of a Compact Dual-band Handheld RFID Reader Antenna

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Abstract: The design of a dual band operational compact antenna is investigated in this paper for RFID handheld reader application. The dual frequency operation of the antenna is achieved by using a U-shaped slot on the patch and a L-shaped slot in the ground plane. The shorted wall connecting the patch and the ground plane plays a vital role to make it compact. The overall dimension of the patch is 20×36 mm2 which is very compact with respect to the operating frequencies. Moreover, the air gap between the patch and the ground plane provides the circuitry to be embedded within the antenna. The antenna achieves a -10 dB impedance bandwidth of 12 and 10.4% respectively covering all sub-bands of universal UHF and ISM 2.4GHz bands. The antenna is seen to operate with linear polarization with stable omni-directional radiation characteristics in both E- and H-planes.

Key words: Dual band, RFID, shorted wall, compact antenna, handheld.

Raziskava kompaktne dvopasovne ročne DFID bralne antene

Povzetek: V članku je predstavljen načrt dvopasovne kompaktne antene za uporabo v ročnih RFID bralnikih. Delovanje antene pri dveh frekvencah je omogočeno s pomočjo U reže na krpici in L reže na ravnini mase. Kratka stena, ki povezuje krpico z ravnino mase igra pomembno vlogo pri kompaktnosti naprave. Celotne dimenzije krpice so 20×36 mm2, kar je zelo majhno glede na frekvenco delovanja. Dodatno zračna reža med krpico in ravnino mase vzpostavlja vgrajeno zanko z anteno. Antena dosega -10 dB impedančno pasovno širino 12 in 10.4 % pri pokrivanju vseh pod pasov pri UHF in ISM 2.4 GHz. Predvideno je, da antena deluje z linearno polarizacijo in stabilno vsesmerno radiacijsko karakteristiko v E in H ravnini.

Ključne besede: Dva pasa, RFID, skrajšana stena, kompaktna antena, ročna naprava.

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1. Introduction

Radio frequency identification (RFID) systems have been widely used recently in supply chain management by retailers and manufacturers to identify and track goods efficiently [1]. RFID system provides a wireless detection of the goods which usually consists of reader/writer and tag. Typically, the reader transmits RF power to the tag, which then sends a unique coded signal back to the reader, while the writer can change the information contained within the tag. Therefore, in the reader side the antenna needs to be carefully designed to ensure good performance of the RFID system. The system can be operated in different frequency bands in accordance to the standard regulation. Several frequency bands have been assigned to the RFID applications, such as 125 kHz, 13.56 MHz, around 900 MHz, 2.45 and 5.8 GHz [2].

There is not a single, universal RFID frequency that is capable of working in all applications. Different RFID technologies will be complementing each other, each used in applications that most suit its characteristics. For example, UHF is best used in logistics, baggage tagging and case pallet tracking, where longer read range is needed, whereas HF is best used in item-level tagging and in areas where liquid and metals are involved but HF may fail in the read range category and speed. The challenge for this technology is to increase the read range and its flexibility to environmental factors for different applications [3, 4].

Recently, UHF and ISM bands are becoming more attractive because of their suitability and cost effectiveness for various applications. UHF RFID tags dominate the market due to their salient features of long distance and high speed reading, more data storage capability and being more immune to environmental factors such as liquids and human presence [5, 6]. However, there is not a specific UHF range accepted worldwide for the RFID applications. Spectral allocation for UHF RFID applications by governments varies from one country to another [7].

902 – 928-MHz band in North and South of America
(840 - 955 MHz) in Asia-Pacific region:
840.5 – 844.5 and 920.5 – 924.5 MHz in China
865 – 868 MHz, 920 – 925 MHz in Hong Kong
919 – 923 MHz in Malaysia
866–869 and 920–925 MHz in Singapore
952–955 MHz in Japan
865 – 867 MHz in India
920 – 928 MHz in Taiwan
908.5 – 910 MHz, 910 – 914 MHz in Korea
920 – 926 MHz in Australia and so on
866 – 869 MHz in Europe

On the other hand, the advantage of using ISM bands like 2.4GHz (2.40-2.483GHz) is a higher range with high data transfer rate, but the drawback is that a clear line of sight from the antenna to the tag should be assured [8]. However, as the operating frequency of RFID systems rises to the microwave region, the reader antenna design becomes more acute and critical. In this circumstance, microstrip antennas are very attractive choice because of their well-known advantages of low profile, light weight, conformal to carrier and easy production [9-14].

Nevertheless, a dual band antenna is capable of replacing two single band antennas. For that reason, more designs of multi-band antennas for RFID readers were presented to fulfill the requirement of the RFID industry. However, in order to fulfill the requirements of the handheld RFID application, the antennas of the devices must be compact and compatible to the circuitry. These antennas are either too big to be incorporated in the handheld RFID reader [15-20] or needs an extra space on the PCB board of the device that might not be covered by the circuitry [21].

In this paper, a compact dual-band handheld RFID reader antenna has been proposed in which the radiating patch is at the top portion of the handheld device and can be very suitable to be adjusted with the circuitry of the reader. A combination of shorted wall patch technique [22] with a U-shaped slot on the patch and an L-shaped slot in the ground is used to achieve the compactness and dual-frequency operation. The proposed antenna is able to operate in almost all the frequencies of universal UHF and ISM 2.4GHz frequency bands.

2. Design of the antenna

The configurations of the proposed antenna are illustrated in Figures 1, 2 and 3. The antenna primarily consists of four components: the printed ground plane, the air substrate, the printed patch with a Superstrate and the shorted wall. The ground plane is assumed to be the common ground for the circuitry and other internal components of the handheld RFID device. The area of the Ground plane is selected to be 40×100 mm^2, which is capable to be embedded in any handheld RFID device. The ground plane is fabricated on a glass-reinforced epoxy resin material namely FR4 with dielectric constant of 4.6 and loss tangent of 0.02. The thickness of FR4 material is 1.6mm which is chosen due to its availability. An L-shaped slot is etched from the ground. This slot provides the required impedance matching to achieve both the frequency bands accurately.

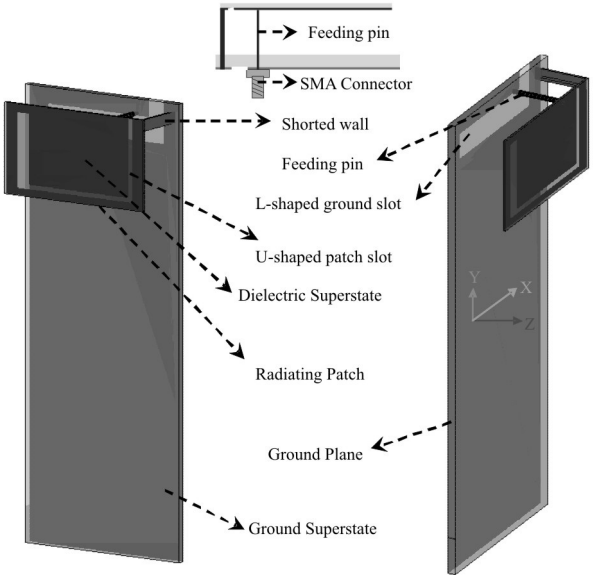

Figure 1: Perspective and side view of the proposed antenna

Air is used as the substrate of the proposed antennas because the free space between the ground plane and patch will be useful to the circuitry of the device. The thickness of air used in this antenna is of 10 mm. A Rogers RO4003 Substrate with dielectric constant of 3.38 and loss tangent of 0.0027 is used as a superstrate to design the patch of the antenna. It is worth mentioning that this 0.508 mm thick Rogers superstrate acts like a protecting cover for the antenna patch section which might prevent it from the abnormal weather condition

and environmental hazards. The antenna is fed with as 50Ω SMA connector. The middle pin of the SMA connector is connected to the top patch and the surrounding ground connection is connected to the ground plane of the antenna.

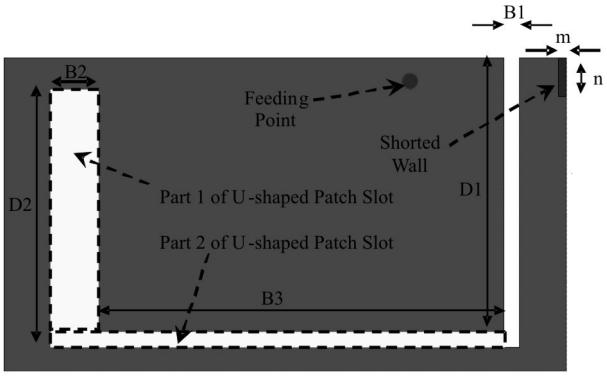

Figure 2: Top view of the patch section

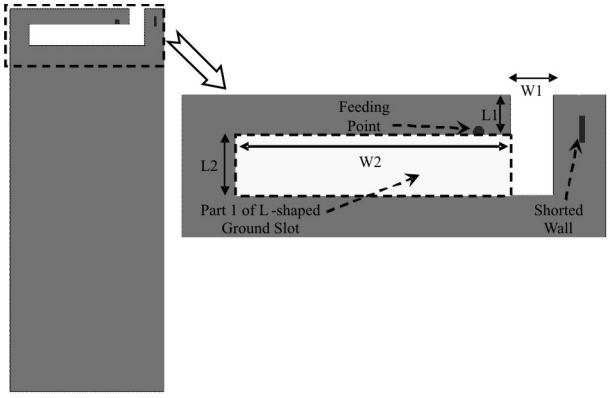

Figure 3: Top view of the ground plane and an enlarged view in the inset

A U-shaped slot is cut on the patch structure. This U-shaped slot is vitally important to achieve the UHF band operation. The overall dimension of the patch is 20×36 mm^2 which is very compact with respect to the operating frequencies. The shorting wall is assumed to be a copper strip with length of 11.6 mm and width of 2.5 mm. The thickness of the strip is 0.5 mm which is soldered at the top corner of the patch and connects it with the ground plane. The shorted wall is mainly responsible for the compactness of the antenna and to be compatible for the handheld application [22]. The optimized values of the antenna parameters are given in Table 1.

3. Parametric analysis

Parametric analysis has been performed to facilitate an elaboration of the design and optimization processes for readers. Various parameters are investigated to examine the effects of the antenna parameters on return loss as well as the impedance bandwidth of the antenna. This study covers the influences of varying lengths of the U- and L- shaped slots and dimensions the shorting wall. For better convenience of the effect on the performance of the antenna upon changing the parameters, only one parameter is changed at a time, while keeping others unchanged [17] Method-of-moment (MoM) based full wave commercially available electromagnetic software IE3D is used in for this analysis.

Table 1: Optimized values of the antenna geometry

Name of the parts	Parameters	Values (mm)
Ground Plane	L1	4
	L2	5.5
	W1	4
	W2	26
Patch	D1	17.5
	D2	16.5
	B1	1
	B2	3
Shorted Wall	m	0.5
	n	2.5
Air Thickness	t	10

The dependencies of the resonating frequencies and bandwidth on L- and U- shaped slots are described in Figure 4. It is observed that these slots have the most vital influence on the resonance. When the part 1 of the L-shaped slot is erased, the antenna achieves only one resonance and that falls down between the middle of our desired frequencies. The removal of whole L-shaped ground slot reveals that the impedance matching of the antenna is primarily dependent on it.

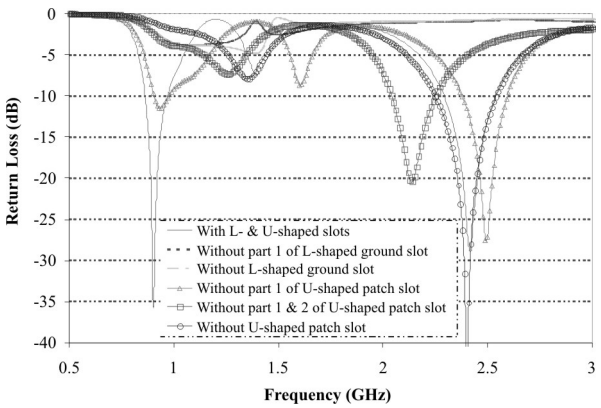

Figure 4: Return losses for the L-, U- shaped slots and various parts of these slots

The antenna can operate in the ISM 2.4 GHz band even the U-shaped slot is not etched on the patch. But the

U-shaped slot and various parts of are very influential on the UHF frequency band and the dimension of the U-shaped slot defines the lowest operating frequency.

In Figure 5 and 6, the effect of various dimensions of L-shaped ground slot is shown. Increasing the value of L1 increases the first resonating frequency point and decreases the resonating point from ISM band; while in both cases the return loss tends to decrease. However, the increments of the value of W1 slightly change the bandwidth of UHF band, but drastically change the ISM band of operation. Therefore, it is important to have a close eye on these two parameters at the time of optimization.

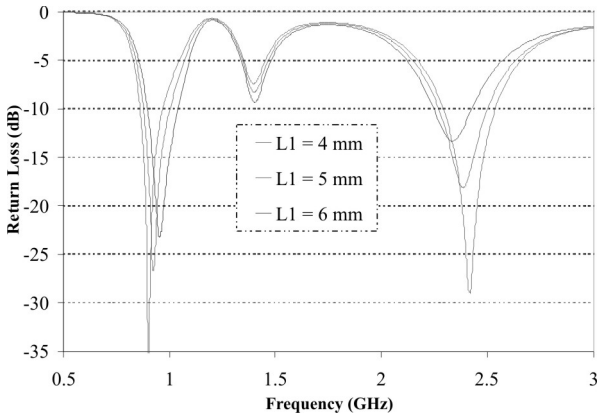

Figure 5: Return losses for different values of *L1*

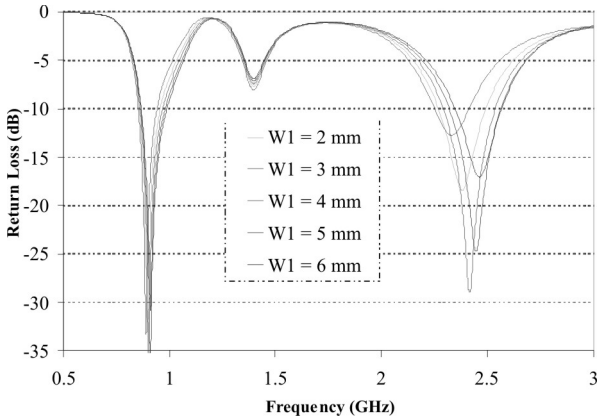

Figure 6: Return losses for different values of *W1*

From Figures 7 and 8, it is evident that the dimensions of L2 and W2 affect the resonating frequencies very much. When the valued of L2 and W2 are increased from the optimized ones, both the resonating frequencies for UHF and ISM bands decreases to some lower frequencies. This might be because of the increment of current paths with the increase of L2 and W2 values.

The lengths D1 and D2 of the U-shaped patch slot are very important mostly to tune the ISM band of 2.4GHz. From Figure 9, it is seen that, when the value of D1 is

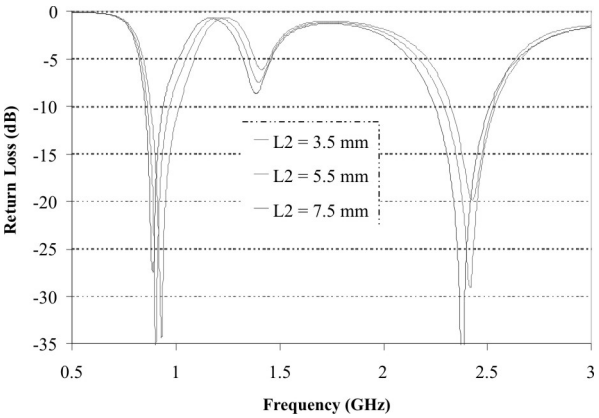

Figure 7: Return losses for different values of *L2*

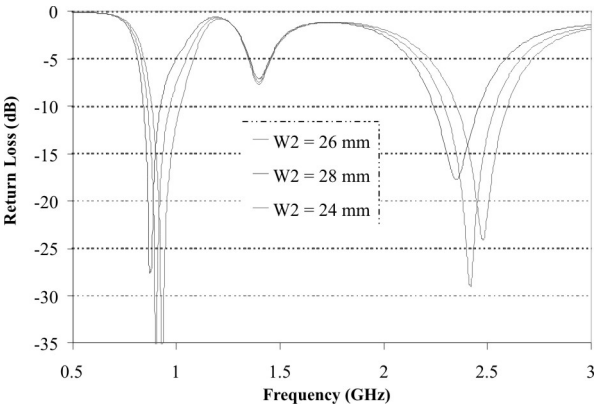

Figure 8: Return losses for different values of *W2*

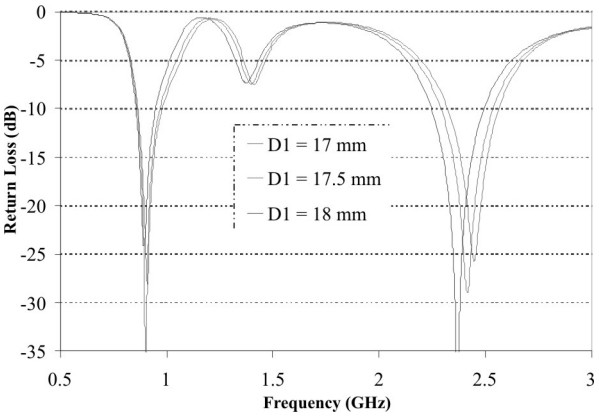

Figure 9: Return losses for different values of *D1*

increased from the optimized value, it provides higher impedance matching. As a result, the antenna attains lower frequencies for ISM band and vice versa. However, the increment of D2 produces some degenerative matching for the antenna, shown in Figure 10. So in this case, the resonating frequency point for ISM band decreases, even though the current path increases. This proofs that the antenna optimization of this antenna is a matter of observation on the impedance matching rather than merely calculating the length of resonating

current path. Figure 11 exhibits the dependencies of the return loss on the value of B1. It is vivid that slot width B1 has only influence on the UHF frequency band. The bandwidth and resonating frequency tends to increase with the increment of the value of B1, while the ISM band remains almost unchanged. However, the value of B2 does not have vital effect of the return loss characteristics of the antenna and so it is not mentioned here.

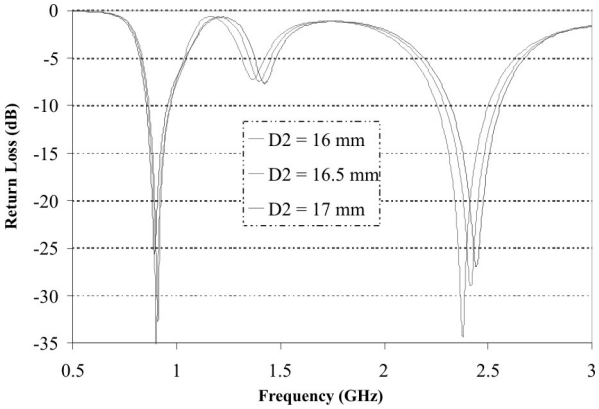

Figure 10: Return losses for different values of *D2*

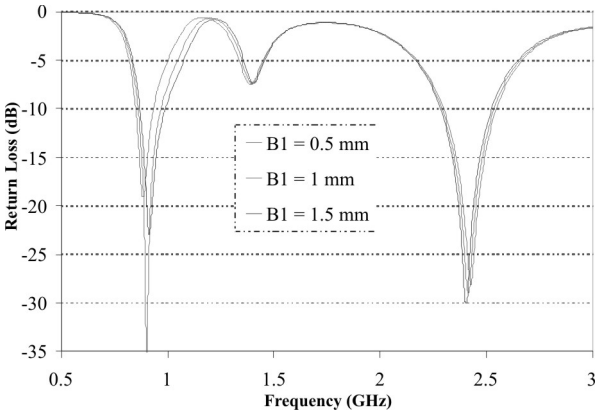

Figure 11: Return losses for different values of *B1*

Lastly, the influence of the shorted wall has been observed. Figure 12 demonstrates that the width, *n* of the shorting wall is very influential for the impedance matching of the ISM band. With the increase of the width, *n* the resonating frequency tends to increase and vice versa. However, the thickness, *m* of the shorting wall does not involve draining much current from the patch to ground. No change of return loss is observed when varied from the optimized value of 0.5 mm and so is not mentioned here.

4. Antenna performances

Figure 13 illustrates the return loss of the proposed antenna. It is observed that the antenna is capable to operate in UHF and ISM 2.4GHz RFID bands. In the lower band, the antenna operates from 860 to 970 MHz (110 MHz) which is equivalently 12% with respect to the center frequency, 915MHz of the operating band. This resonance covers almost all the frequencies of the universal RFID operation. The readings of the return loss are taken in reference to -10dB level. Moreover, the antenna achieves a bandwidth of 250MHz (from 2.29 GHz to 2.54 GHz). This ISM band has an impedance bandwidth of 10.4%, which entirely covers the required band of RFID application.

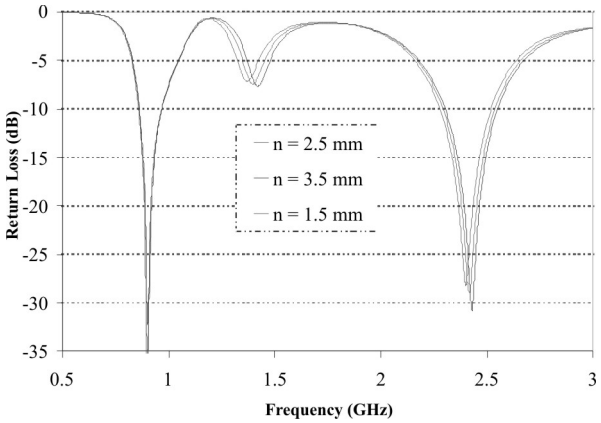

Figure 12: Return losses for different values of *n*

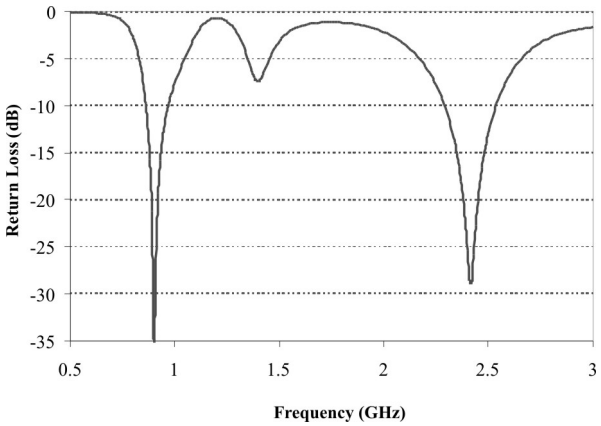

Figure 13: Return loss of the proposed antenna

The maximum gain obtained from the antenna is shown in Figure 14. The antenna is capable to provide a maximum gain of 1.9dBi in the UHF band. In case of the ISM band the antenna attains a peak gain of 2.5dBi at approximately 2.5GHz. The values of the gains are literally enough for short-range handheld operation. The radiation efficiency of the antenna roams around 80% and 75 % respectively at UHF and 2.4 GHz ISM bands. Thus the antenna can communicate efficiently with the surrounding RFID tags.

The E- (XZ) and H- (YZ) plane radiation patterns of the proposed antenna for 900MHz and 2.4GHz is depicted in Figure 15. In the higher ISM band the radiation pat-

terns are a bit distorted, when compared with those the lower UHF band. This can be imputed to the higher harmonics generated by the antenna in the higher frequencies. However, from the polar plots it is evident that the antenna is able to direct the maximum radiation to the boreside (angle = 0 degree) in both the functional bands.

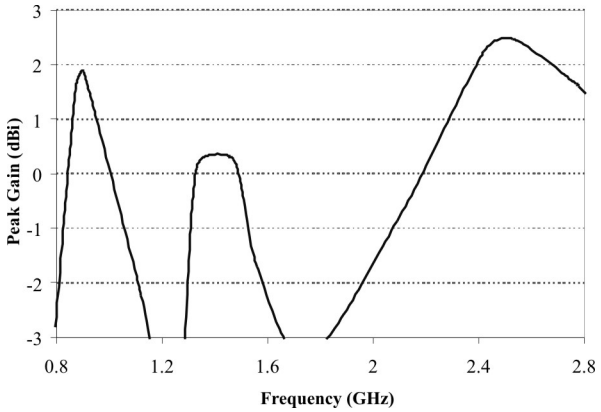

Figure 14: Maximum gain of the proposed antenna

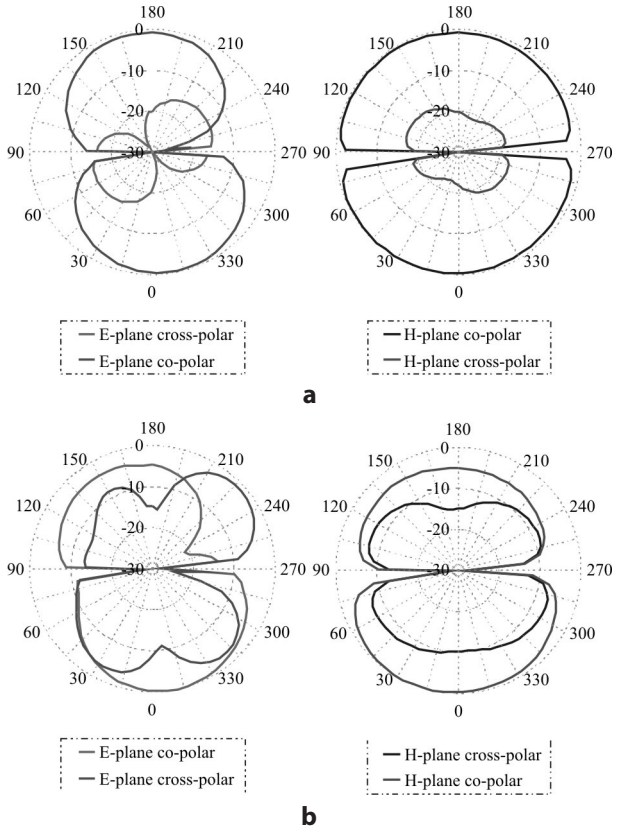

Figure 15: E- (XZ) & H- (YZ) plane radiation patterns of the proposed antenna (in dB unit) at (a) 900MHz and (b) 2.4GHz

Conclusion

A compact RFID antenna for handheld application is presented in this paper. The antenna is able to operate in both UHF and ISM 2.4 GHZ bands. The dual frequency operation of the antenna is achieved by using a U-shaped slot on the patch and a L-shaped slot in the ground plane. The shorted wall connecting the patch and the ground plane plays a vital role to make it compact. The overall dimension of the patch is 20×36 mm^2 which is very compact with respect to the operating frequencies. Moreover, the air gap between the patch and the ground plane provides the circuitry to be embedded within the antenna. The suggested antenna shows good performances in terms of return loss with a -10-dB impedance bandwidth of 110 MHz (860–970MHz) in UHF band and 250 MHz (2.29–2.54 GHz) in ISM band. The functional bands are quite capable of operating in almost all the frequencies used for universal UHF and ISM bands. Moreover the antenna provides good radiation characteristics, which makes the antenna a suitable candidate for the handheld short-range applications.

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