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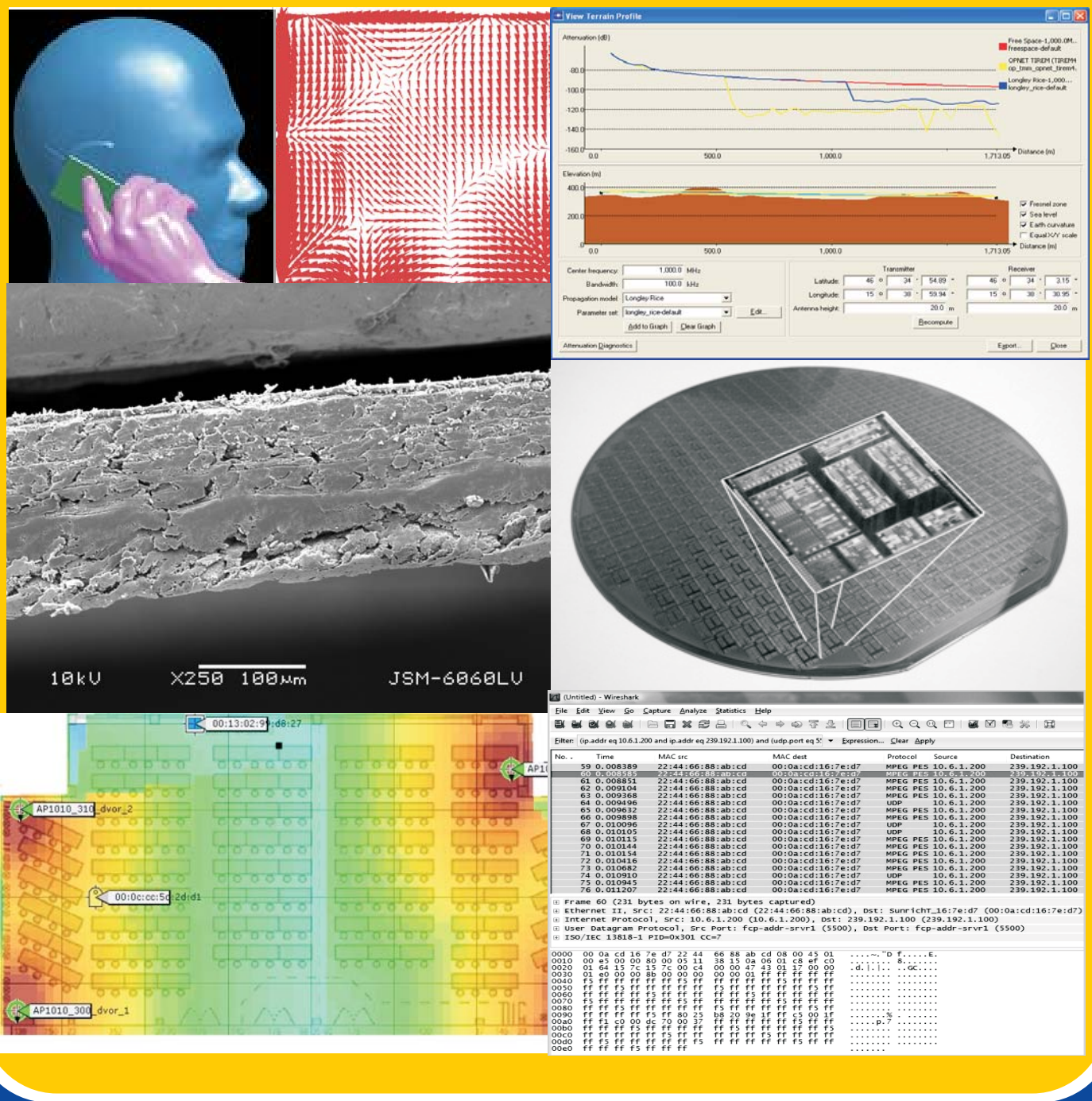

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INFLUENCE OF MOSFET MODEL FORM ON CHARACTERISTICS OF THE BOOST CONVERTER

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Department of Marine Electronics, Gdynia Maritime University, Poland

Key words: MOS transistors, BOOST converters, modelling

Abstract: In the paper boost converter characteristics at the steady state obtained from SPICE analysis with the use of selected kinds of MOSFET models of various complexity and accuracy are compared. The dependencies of the converter output voltage, the watt-hour efficiency and the MOSFET inner temperature on the frequency and the duty cycle of the MOSFET control signal as well as the converter load resistance are considered. The correctness of the calculation results was verified experimentally. The duration time of the analyses corresponding to all the considered models of the MOS transistor are compared, too.

Vpliv modela MOSFET tranzistorja na karakteristike ojačitvenega pretvornika

Kjučne besede: V čLanku primerjamo statične karakteristike pretvornika pridobljene s SPICE simulacijo z uporabo izbranih MOSFET modelov različnih kompleksnosti in natančnosti. Opišemo odvisnost izhodnih napetosti, učinkovitost ter MOSFET temperaturo od frekvence kontrolnega signala in bremenske upornost. Pravilnost dobljenih rezultatov smo preverili tudi eksperimentalno. Primerjali smo tudi čase simulacije v odvisnosti od uporabljenih modelov.

Izvleček: MOS tranzistorji, pretvorniki, modeliranje

1. Introduction

Dc-dc converters are commonly used in power supply systems /1/. The boost converter is the most popular in the class of step-up converters of the output power up to 1 kW. The network representation of the boost converter with the MOS power transistor operating as the switch is shown in Fig.1.

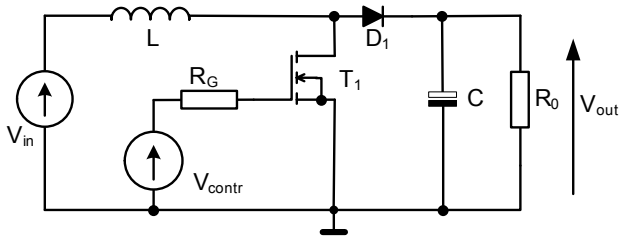

Fig. 1. The diagram of a boost converter

The analysis and design of electronic circuits e.g. dc-dc converters requires the use a proper computer tool (algorithms). To this end SPICE is the appropriate tool /2, 3/. The accuracy and duration time of calculations depend among others on the form of models of semiconductor devices and elements existing in the considered circuit.

The characteristics describing dc-dc converters at the steady state have a fundamental significance for the engineer-designer of such a class of circuits. Two groups of methods of the analysis of dc-dc converters at the steady state can be distinguished. The first method is based on the dc analysis with average models of the analysed circuit taken into account /4-8/, whereas in the other method based on the transient analysis, the large-signal dynamic models of devices operating in the circuit are used /2, 4, 7, 9/. As it was shown in /10/, the second method allows obtaining much better consistency between the calculation and measuring results, but the analysis duration time can be much longer than in the first method.

There are models of different accuracy, among of both kinds of models mentioned before. For example, in the paper /11/ the results of the analysis of the isolated dc-dc converter obtained by nonlinear inertial models of the Schottky diode and the MOS transistor are presented. In turn, the paper /12/ presents the results of a small-signal analysis of the buck-boost converter obtained with the use of devices models of the form of ideal switches. In the paper /13/ the results of the analysis of the dc-dc converter obtained by the SPICE built-in models of the diode and the MOS transistor were used as the reference results to verifie the correctness of the new method of calculations of converter characteristics. The description of the behavioral dc-dc converter models of different accuracy dedicated to the system level analysis can be found in /14/. The similar meaning is to be found in the models presented in the paper /15/, whose parameters values can be estimated with the use of the catalogue data of converter devices. The paper /16/ describes the method of estimation of the electrothermal characteristics of dc-dc converters with the

use of the method of the separated iteration with the use of nonlinear semiconductor devices models. The nonlinear models of semiconductor devices were also used in the analysis of a dc-dc converter in the small-signal /17/ and large-signal /18/ case, respectively. The average models of dc-dc converters with nonlinearities of semiconductor devices taken into account are described in /19, 20/.

The aim of this paper, being of the extended version of the paper /21/, is to estimate the influence of the form of the MOS transistor model on the boost converter characteristics at the steady state obtained by the transient analysis. The analyses were performed by SPICE with the use of SPICE built-in linear models of: the inductor L, the capacitor C, the resistors R_0, R_G, the voltage sources V_{in}, V_{contr} and the model of the diode D1 described in /22/. Five various models of MOS transistor were tested. Namely: the model of the ideal switch, the Dang's model built-in in SPICE, the two-value resistor model, the electrothermal model of the two-value resistor /23/ and the electrothermal hybrid model of the considered device /24/. The results of the analysis of the form of the proper characteristics of the boost converter and the duration time of the analyses performed with the use of the above mentioned MOS transistor models are presented and compared. The calculations were performed in the wide range of variations of the duty cycle D and the frequency f of the control signal as well as the load resistance R0. Some results of the analyses were compared with the results of measurements.

2. MOSFET models used in analyses

The simplest model of the MOS transistor, among the considered models, is the ideal switch model, whose switch-on and switch-off resistances are equal to zero and infinity, respectively. The main drawback of this model is discontinuity of their characteristics, which can result in the problem of the lack of calculations convergence. Such a model cannot be directly implemented in SPICE. On the other hand, the SPICE built-in model of the voltage controlled switch (VSWITCH) with switch-on and switch-off resistances of the values, which tend to be zero and infinity respectively, can be used.

The second in turn considered model is the two-value resistor model, which possesses non-zero value resistance in the on-state (R_{ON}) and the finite value of the resistance in the off-state (R_{OFF}). In this model the values of the resistances RON and R_{OFF} are independent of temperature.

These models are formulated in SPICE with the use of the model of the voltage controlled switch, the characteristics of which are described by the four parameters: the resistances R_{ON}, R_{OFF} and the voltages V_{ON}, V_{OFF} – representing the device gate-source voltage at the device on-state and off-state, respectively.

The third model of the MOS transistor is the electrothermal model of the switch /24/. This model is an improved version of the two-value resistor model, in which the influence of the ambient temperature and the selfheating phenomenon on the resistance R_{ON} are included. This model, the network representation of which is shown in Fig.2, is composed of two elements connected in series: the SPICE built-in model of the voltage controlled switch S1 (the two-values resistor) and the voltage controlled source E_{RON} described by the formula

$$E_{RON} = V_{S1} \cdot \alpha_{RON} \cdot \left(R_{th} \cdot I \cdot V_S - T_0 + T_a\right) \qquad (1)$$

where V_S denotes the voltage on the two-values resistor, V_{S1} – the voltage on the switch S_1, T_a – ambient temperature, R_{th} – the thermal resistance of the transistor, I – the current of the two-value resistor, α_{RON} – the temperature coefficient of variations of the on resistance of the two-values resistor. The resistance of the switched-on switch S_1 is equal to the resistance R_{ONO} corresponding to the on-resistance of the two-values resistor at the reference temperature T_0.

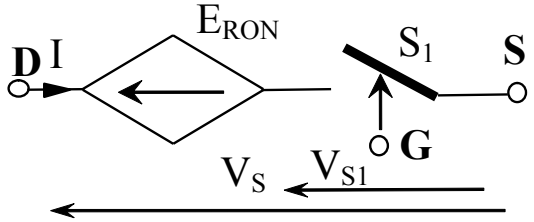

Fig.2. The network representation of the two-values resistor model

Both the electrical inertia and nonlinearity of the device current-voltage characteristics are not included in the presented models.

The next is the Dang's isothermal model of the MOS transistor built-in in SPICE, described e.g. in /22/. This model takes into account the nonlinear d.c. characteristics and the inertia of the considered device, whereas the selfheating phenomenon is not taken into account in this model. There are 28 parameters describing the Dang's model /22/. These parameters are: model index (LEVEL), default channel length (L), default channel width (W), drain ohmic resistance (RD), source ohmic resistance (RS), gate ohmic resistance (RG), bulk/substrate ohmic resistance (RB), zero-bias bulk-drain junction capacitance (CBD), zero-bias bulk-source junction capacitance (CBS), bulk junction saturation current (IS), Bulk junction saturation current per sq-meter of junction area (JS), Bulk junction saturation current per length of sidewall area (JSSW), bulk junction emission coefficient (N), bulk junction potential (PB), bulk junction sidewall potential (PBSW), gate-source overlap capacitance per meter channel width (CGSO), gate-drain overlap capacitance per meter channel width (CGDO), gate-bulk overlap capacitance per meter channel length (CGBO), drain and source diffusion sheet resistance (RSH), Zero-bias bulk junction bottom capacitance per square meter of junction area (CJ), zero-bias bulk junction sidewall capacitance per length of sidewall (CJSW),

bulk junction bottom grading coefficient (MJ), zero-bias bulk junction sidewall capacitance per meter of junction perimeter (CJSW), bulk junction sidewall grading coefficient (MJSW), bulk junction transit time (TT), flicker noise coefficient (KF), flicker noise exponent (AF), coefficient for forward-bias depletion capacitance formula (FC), zero-bias threshold voltage (VTO), transconductance parametr (KP), bulk threshold parameter (GAMMA), surface potential (PHI), oxide thickness (TOX), substrate doping (NSUB), surface state density (NSS), fast surface state density (NFS), type of gate material (TPG), metallurgical junction depta (XJ), lateral diffusion (LD), lateral diffusion width (WD), surface mobility (UO), critical field for mobility degradation (UCRIT), critical field exponent in mobility degradation (UEXP), transverse field coefficient (UTRA), maximum drift velocity of carriers (VMAX), total channel charge coefficient (NEFF), thin-oxide capacitance model flag and a fraction of channel charge attributed to drain (XQC), width effect on threshold voltage (DELTA), mobility modulation (THETA), static feedback (ETA) and saturation field factor (KAPP).

The last one is the electrothermal hybrid model of the MOS transistor proposed by the authors in /24/, the network representation of which is shown in Fig.3. This model consists of the Dang's model (SBM) and two controlled voltage sources E_G and E_{RD} modelling the influence of selfheating on the device threshold voltage and its drain resistance, respectively. The voltages on these sources are expressed by

$$E_{RD} = i_D \cdot R_D \cdot \alpha_{RD}\left(T_j - T_0\right) \tag{2}$$

$$E_G = \alpha_U \left(T_j - T_0\right) \tag{3}$$

In the analytical description of these sources (Eqs (2-3)) the temperature coefficients of variations of both the threshold voltage α_U and the drain series resistance α_{RD}, appear. The internal temperature T_j of the transistor is given by

$$T_j = T_a + R_{th} \cdot v_{DS} \cdot i_D \tag{4}$$

where i_D denotes the drain current and v_{DS} is the drain-source voltage.

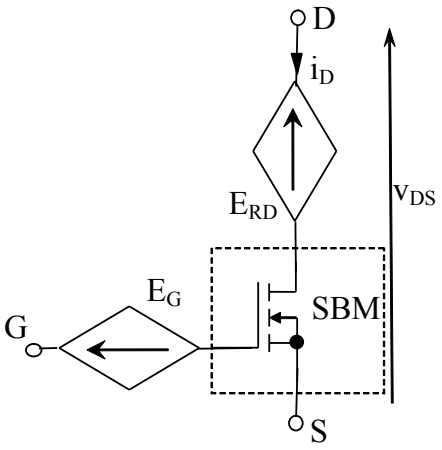

Fig.3. The circuit representation of the electrothermal hybrid model of the MOSFET transistor

The boost converter (Fig.1) with transistor IRF840, the diode BY229, the inductor of inductance 650 µH, and the capacitor of capacitance 47 µF was investigated.

In the considered MOS transistors models the values of the parameters collected in Table 1 were used.

Table 1. The values of parameters of the considered MOS transistor IRF840 models

Dang's model (curve b)							
parameter	LEVEL	KAPPA	TOX	UO	PHI	RS	KP
value	3	0.2	100 nm	600 $cm^2V^{-1}s^{-1}$	0.6 V	6.382 mΩ	20.85 $\mu A/V^2$
parameter	W	L	VTO	RD	TT	RDS	CBD
value	0.68 m	2 µm	3.879 V	0.6703 Ω	710 ns	2.222 MΩ	1.415 nF
parameter	PB	MJ	IS	CGSO	CGDO	RG	
value	0.8 V	0.5	56 pA	1.625 nF/m	133.4 pF/m	0.6038 Ω	
Additional parameters of the electrothermal hybrid model (curve a)							
parameter	α_U	α_{RD}					
value	-3 mV/K	10^{-2} K^{-1}					
Twovalue-resistor model (curve d)							
parameter	R_{ON}	R_{OFF}	V_{ON}	V_{OFF}			
value	0.67 Ω	1 MΩ	14 V	1V			
ideal switch model (curve c)							
parameter	R_{ON}	R_{OFF}	V_{ON}	V_{OFF}			
value	1 µΩ	1 MΩ	14 V	1V			
Electrothermal model of a two-values resistor (curve e)							
parameter	R_{ONO}	R_{OFF}	V_{ON}	V_{OFF}	α_{RON}		
value	0.67 Ω	1 MΩ	14 V	1V	10^{-2} K^{-1}		

To estimate the correctness of the considered models, in Fig.4 the calculated and measured output characteristics $i_D(v_{DS})$ of the transistor IRF840 at v_{GS} = 15 V are presented. In this figure (and in the further ones) the points denote the measuring results, whereas the lines – the results of the analysis. In Fig.4 the following notations are used: a – the electrothermal hybrid model of the considered transistor, b – the isothermal built-in in SPICE Dang's model, c – the ideal switch model, d – the isothermal model of the two-

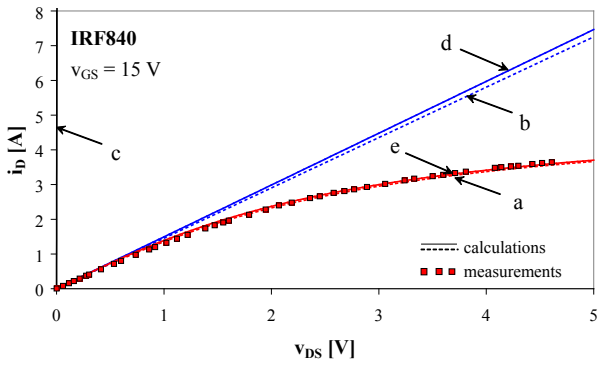

Fig. 4. Calculated and measured dc output characteristics of the transistor IRF840

value resistor, e – electrothermal model of the two-value resistor.

As seen from Fig.4, the characteristic corresponding to the ideal switch (the characteristic c covers the vertical axis of ordinates) differ essentially from the remaining characteristics (curves a, b, d, e). In turn, the characteristics calculated with the device isothermal model (curve b) and with the model of two-value resistor (curve d) are practically identical and linear in the considered range of variations of the drain current. The characteristics corresponding to the models including selfheating (the curves a and e) are nonlinear and practically overlap. The characteristics a and e show that selfheating evidently results in an increase of the device resistance R_{ON}.

3. Results

Using the considered models of the MOS transistor (Section II) the transient analysis of the boost converter (Fig.1) up to the steady state for various values of the load resistance R_0, the duty cycle D and the frequency f of the device control signal, was performed. The influence of these parameters (R_0, D, f) on the output voltage and the watt-hour efficiency of the converter as well as the MOS transistor case temperature was investigated. During the measurements the MOS transistor and the diode were situated on the heat-sinks. The value of the thermal resistance of the MOS transistor measured with the use of the measuring method from /25/ and the measuring set described in /26/ is equal to 5.5 K/W. The mesurements of characteristics were carried out by typical multimeters at the thermal steady-state, whereas the device case temperature was measured by the pyrometer ST-3. In the analysis the SPICE built-in isothermal model of the p-n diode with the following parameter values (corresponding to the diode BY229): Is = 53.4 pA, N = 1.185, RS = 0.12 Ω, trs1 = $3 \cdot 10^{-3}$ K^{-1}, Ikf = 3.5 mA, Cjo = 325 pF, M = 0.3333, Vj = 0,75 V, Fc = 0.5, Isr = 100 pA, Nr = 2, TT = 145 ns was used. In the analysis the inductor series resistance of the value equal to 0.1 Ω was taken into account.

The transient analyses of the considered circuit until the steady-state were performed with the use of all the models described in Chapter III. The calculated values of the converter output voltage V_{out}, the watt-hour efficiency η, and the case temperature T_C are shown in Figs. 5 -7.

In Fig.5 the results of the calculated and measured dependences of the output voltage and the watt-hour efficiency of the considered converter and the MOS transistor case temperature on the duty cycle D of the gate control signal at the frequency f = 108.7 kHz and the load resistance R_0 = 20 Ω are presented.

As seen from Fig.5, the results of analysis with the use of the electrothermal hybrid model of the MOS transistor (curve a) and the electrothermal model of the two-values resistor (curve e) fit well to the measuring results. Neglecting the

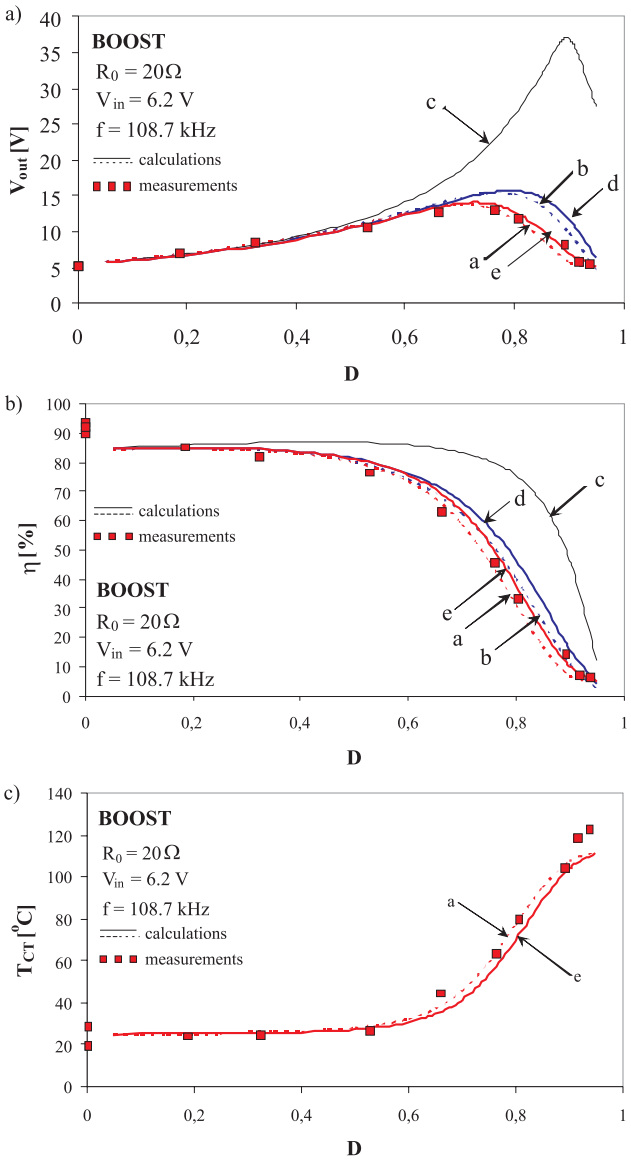

Fig. 5. The calculated and measured dependences of the output voltage (a), the watt-hour efficiency (b) of the converter and the transistor case temperature (c) on the duty-factor of the control signal

selfheating phenomenon in the MOS transistor (curves b and d) results in too high values of the converter output voltage and shifts of the maximum on the characteristic $V_{out}(D)$ towards the higher values of the coefficient D. In turn, neglecting conducting losses in the transistor (curve c) results in a considerable increase of the converter output voltage. It is worth mentioning that the differences between the values of the voltage V_{out} obtained with the use of all the considered models are hardly visible at small values of the coefficient D (D < 0.4). Moreover, these differences increase with an increase of D.

As seen from Fig.5b the dependence η (D) is a decreasing function. The best agreement between the analysis and measuring results is assured by the MOS transistor models with a electrical inertia and selfheating taken into account

(curves a, b, d, e). Disregarding conducting losses in the MOS transistor results in a considerable increase of the watt-hour efficiency of the converter.

It results from Fig.5c that the case temperature T_{CT} of the MOS transistor is an increasing function of the coefficient D and the values of T_{CT} obtained with the use of the both electrothermal models (curves a and e) fit well to the measurements.

In Fig.6 the calculated and measured values of the converter output voltage (Fig.4a) and the watt-hour efficiency (Fig.4b) as well as the MOS transistor case temperature (Fig.4c) on the converter load resistance at D = 0.5 and f = 100 kHz are presented.

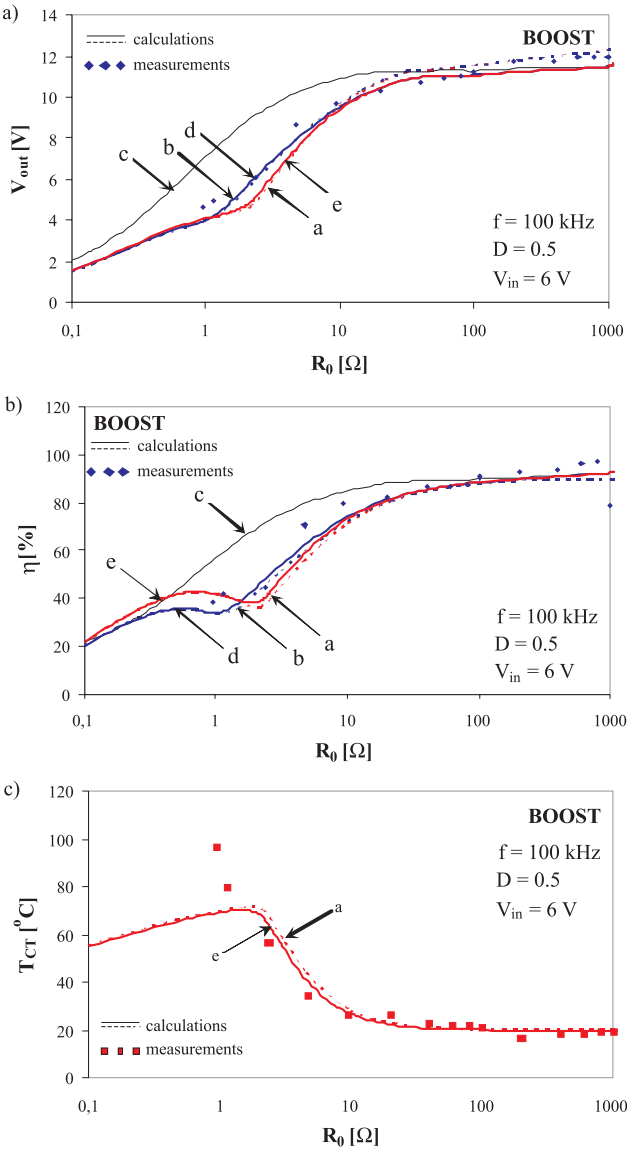

Fig. 6. The calculated and measured dependences of the converter output voltage (a) and the watt-hour efficiency (b), as well as the transistor case temperature (c) on the load resistance.

Fig. 6a shows that the converter output voltage is an increasing function of the resistance R_0. In the range of small values of the load resistance (R_0 < 2 Ω) the considered converter operates incorrectly, that means that $V_{out} < V_{in}$.

It results from Fig.6b that a decrease of the resistance R_0 leads to a decrease of the converter watt-hour efficiency. It is worth mentioning that the dependences η (R_0) obtained with the use of the models taking into account the MOS transistor conducting losses (curves a, b, d, e) have local minimums and local maximums (peaks) at the load resistance values in the range from 0.5 Ω to 2 Ω Neglecting the conducting losses in the MOS transistor results in an increase of both the output voltage and the watt-hour efficiency of the converter even more than 50%.

Fig.6c shows that the measured values of the case temperatures of the MOS transistor fit well to the calculated values at R_0 < 1.5 Ω only. The measured characteristic TCT(R0) is a monotonically decreasing function, whereas the same characteristic obtained from the calculations has the peak at R_0 = 1.5 Ω.

In Fig.7 the influence of the frequency f of the signal controlling the MOS transistor on the converter output voltage (Fig.7a) and the watt-hour efficiency (Fig.7b) as well as the case temperature of the MOS transistor (Fig.5c) is presented. The calculations and measurements were performed at D = 0.75 and R_0 = 20 Ω.

It results from Fig.7a that the voltage V_{out} is a decreasing function of the frequency f. This dependence is described correctly by the electrothermal hybrid model of the MOS transistor (curve a) only. The values of the voltage V_{out} obtained from the remaining models are inflated. For the signal frequency f > 1 MHz the investigated converter does not operate correctly due to too high values of the MOS transistor inner capacitances, which make the proper switching of the MOS transistor impossible. The values of the voltage V_{out} corresponding to this range of the signal frequency are equal to the difference of the converter input voltage and the voltage drop on the forward biased diode D. As seen, the model of the two-value resistor ensures the correct values of the voltage V_{out} if the signal frequency is less than 150 kHz only.

It results from Fig.7b that increasing of the signal frequency f causes increasing of the converter watt-hour efficiency up to a few percentage only in the range of the frequency f > 1 MHz. This phenomenon is observed from the calculation results obtained with the use of all the considered models, because in all the analyses the diode inertia is taken into account.

Fig.7c shows that the electrical power dissipated while switching the MOS transistor influences substantially the device case temperature T_{CT} in the range of higher values of the frequency of the MOS transistor controlling signal. The values of the temperature T_{CT} obtained with the use of both the considered electrothermal models differ from each other even more than 30%. The temperature T_{CT} doubles when the signal frequency f increases from 100 kHz to 5 MHz.

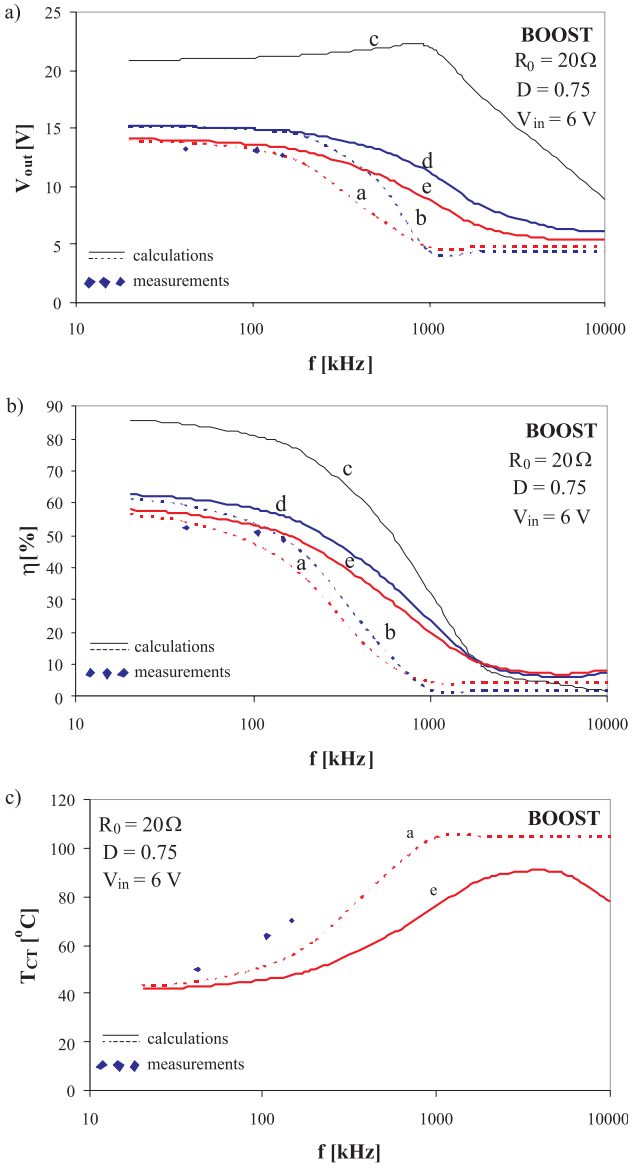

Fig. 7. The calculated and measured dependences of the converter output voltage (a) and the watt-hour efficiency (b) as well as the transistor case temperature (c) on the frequency of the control signal

Apart from the model accuracy, the time of the converter analysis with the use of these models gives also very important information about the usefulness of the models. Table 2 compares the times (in seconds) of the analysis of the boost converter with the use of the considered MOS transistor models.

As seen from Table 2, in the range of small values of the frequency of the control signal, the isothermal model of the two-value resistor ensures the shortest time of the analysis – more than twice shorter than the analysis time with the use of the hybrid electrothermal model. In turn, in all the considered range of variations of the frequency f, the isothermal built-in model of the MOS transistor is the best from the point of view of the analysis rate. In this case the time indispensable for the analysis is twice lower than in the case, when the models of the ideal switch or two-values resistance are used. It is worth mentioning that the model of the worst accuracy (the model of the ideal switch) does not ensure the shortest time of the analysis. This results from the fact, that during switching of the non-inertia switch, very fast changing of the currents and voltages are observed. In a consequence, the time derivatives of currents and voltages of the high values appear, what results in shortening of the calculating step. Finally, the time of analysis have to be increased.

4. Conclusions

In the paper the influence of the model form of the MOS transistor on the characteristics of the boost converter is investigated. As results from the investigations performed by the authors, using the device electrothermal hybrid model ensures a good agreement between the calculated and measured characteristics of the considered dc-dc converter in the wide range of variations of the load resistance, the duty-factor and the frequency of the control signal of the MOS transistor.

If the control signal frequency is less than 150 kHz, then the electrothermal model of the two-value resistor ensures a good agreement between the calculation and measurement results and moreover the analysis time is twice shorter than in the case of the use of the electrothermal hybrid model of the MOS transistor.

For the low values of the MOS transistor control signal frequency and small values of the converter load resistance, selfheating has to be included in the model, whereas it is indispensable for the high values of the control signal frequency to take to account the MOS transistor electrical inertia.

The presented results of the boost converter investigations show that for the control signal frequency less than 150 kHz the inertia can be omitted in the devices models, whereas the static losses in these devices at the on-state

Table 2. Times of the boost convereter analysis with the use of the considered MOS transistor models

Characteristic	Hybrid electro-thermal model	Isothermal built-in model	Ideal switch	Two-value resistor	Electrothermal two-value resistor
$V_{out}(D)$	161.77 s	125.83 s	70.28 s	67.11 s	87.17 s
$V_{out}(R_0)$	366.05 s	289.55 s	148.10 s	126.06 s	165.24 s
$V_{out}(f)$	281.08 s	232.69 s	513.84 s	418.22 s	504.78 s

play the essential role. Therefore a very important challenge would be working out an electrothermal large-signal model of the transistor switch with the inertia phenomena taken into account.

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FLEXIBLE LOW COST ASIC DESIGN VERIFICATION TOOL WITH GUIDELINES FOR GENERATION OF STDF FOR MULTI PROJECT WAFER SORT

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Key words: Wafer sort, ASIC, ATDF, STDF, DAQ Card

Abstract: This article describes practical, low cost approach for sensitive, analog or mixed signal application specific integrated circuit (ASIC) design verification. Step by step is described how to solve the problems about wafer sort on multi-project wafers, how to select appropriate low cost test hardware and suitable operating system platform. All these actions are performed with one main goal in mind to speed up the measurements. It is also described in detail how to achieve test data compatibility with several commercial automatic statistical analysis tools. Entire critical parameter verification process was also practically implemented on very high sensitive ASIC for industrial application and complies with strict automotive standards.

Hitro prilagodljiv in cenovno ugoden testni system za analizo ustreznosti vezij ASIC s priporočili za generiranje STDF datotek na več projektnih silicijevih rezinah

Kjučne besede: Testiranje silicijevih rezin, Vezja po naročilu, ATDF, STDF, DAQ kartica

Izvleček: Članek opisuje praktičen, nizko cenovni pristop za merjenje občutljivih, analognih oziroma analogno-digitalnih sklopov na integriranih vezjih po naročilu. Korak za korakom so opisane tudi rešitve problema testiranja več projektnih silicijevih rezin, kako izbrati primerne testne naprave z ustreznimi operacijskimi sistemi za pospešitev hitrosti zajemanja meritev. Podrobno je opisan tudi način, kako generirati testne podatke, ki so kompatibilni z večino orodij za avtomatsko statistično analizo izmerjenih parametrov. Celoten proces raziskave kritičnih parametrov visoko občutljivega integriranega vezja po naročilu za industrijsko aplikacijo je bil praktično preizkušen in ustreza strogim standardom, ki so predpisani za avtomobilsko industrijo.

1. Introduction

A proper operation of sensitive, analog or mixed signal application specific integrated circuits for microelectronic systems is often influenced by so many parameters that sometimes can't be predicted only by expertise and simulation tools. In such cases, it is a good practice to utilize low cost multi-project wafer production service, which is offered by major semiconductor houses. Schedules for nowadays microelectronics projects are by default very tight. Quick response is critical, when such multi-project wafer is received for design specification evaluation. Usually several ten thousand parts must be evaluated, before new design corrections may be justified and determined. Evaluation time for each part should be well below one second and total control of measurement process is required. It is quite common that several thousand measurements are necessary just for one part characterization in less than one second time frame. The most time efficient way to accomplish this goal is to do measurements directly on silicon wafer /1//2/, to eliminate the device packaging delay. Of course sometimes also package effect must be considered. This even further confirms the described approach, because results on the wafer sort can be later easily compared to the packaged parts measurement results.

There are certainly several software packages for test and automated measurements available on the market. The problem is that in general they are too universal and therefore too bulky. The outcome is relatively slow data acquisition. Sometimes only preparation for one measurement task takes approximately 100 times more time than it is requested for both - preparation and measurement. In this article our approach will be described for low cost and fast wafer sort measurements on multi-project wafers. At the end we will also introduce how to achieve test data compatibility with commercial automatic statistical analysis tools.

2. Adopting wafer sort to multi-project wafers

The most obvious visible characteristic of the multi-project wafer (MPW) is that all devices for different projects are disposed within one small square area on the silicon wafer. The areas are then distributed over the wafer. Example of such different die images on a multi-project reticle is presented in figure1. There may be one or even more than ten identical devices on the same die image.

In general, fully automatic wafer probers are not adapted to the unique layout of multi-project wafers. There are actually two solutions to solve this problem. We may load and run one wafer as many times as there are identical parts to test

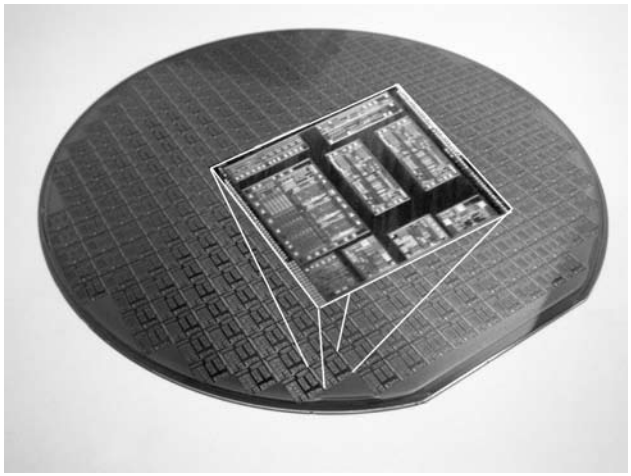

Fig. 1: Multi-Project wafer with emphasized die image.

on one die image. This is not an optimal solution, because it spends quite some time on wafer handling. Better solution is to write a special control software code for the wafer prober. Usually an ordinary personal computer with the suitable interface for wafer prober will do the job. Here we should take care about software compatibility. In case that the same computer is used to control wafer prober and our measurement acquisition system, it is always a good practice to check for the eventual driver and software library compatibility issues.

To teach the wafer prober to march upon the multi-project reticle, we need to adjust device X and Y dimensions to the dimensions of the die image in the multi-project reticle. After that we can use automatic wafer prober features like auto alignment, initial test square area recognition and automatic wafer map generation. Basically, all we need to do to test all devices on one die image is to use relative coordinate control commands of the wafer prober. This enables us to create required wafer prober chuck movements to all identical parts within the same die image that are relating to one project. When all parts on one die image are tested, relative coordinates for return back to the initial position on currently tested die image must be calculated. Than a simple "jump to next die" command can be used to continue with measurements on the next die image.

For marking bad or good parts on multi-project wafers inking is preferred to the wafer map. On the other hand, similar algorithms may also be used to convert original wafer map data from the wafer prober to the packaging company wafer map format.

3. How to select proper measurement equipment

The most crucial point in test program development is to select the right gear to do it. The selection is huge, but from the low cost point of view, it is a very good idea to use multifunction data acquisition cards (DAQ). They do have several limitations, but with proper design of the load board, most of them can be easily removed. As a matter of fact, load board can be connected directly on the DAQ card and everything together can be placed almost on the top of the probe card. This means very low signal degradation and improves signal measurement accuracy. Figure 2 represents such combination of DAQ card and load board that can be simply attached (with connectors) to DAQ card. Figure 3 shows assembled load board and DAQ card with very short wires to probe card on the wafer prober.

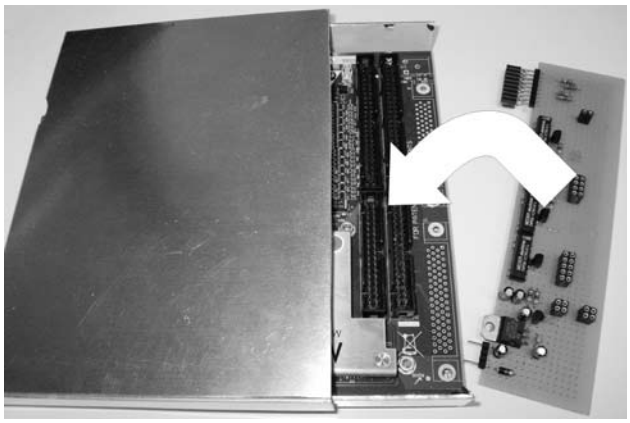

Fig. 2: DAQ card with load board.

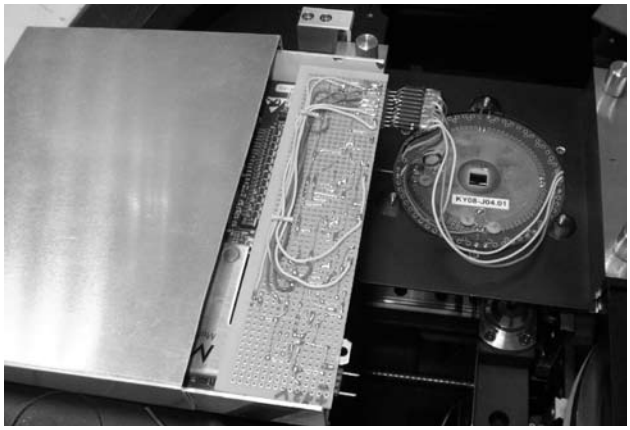

Fig. 3: Assembled DAQ card and load board connected to the probe card on wafer prober.

It is quite common to have a DAQ card with 32 or even more analog inputs (several of them may be also differential), 32 digital inputs/outputs, 4 analog outputs and two or three counters. So each pin of the ASIC that needs to be measured or triggered can be connected directly to its dedicated pin. If the number of pins is insufficient, we may simply add some extra cards to the USB (Universal Serial Bus) port. This method eliminates the need for expensive and time consuming switching matrix. It is well known that in general the switching matrix suffers from poor reliability when huge number of commutations is in question and they also degrade the signals due to longer switching paths.

To achieve high speed, control and flexibility of the DAQ cards we should go to the lowest possible level of program-

ming, which is usually limited by the driver and software library availability. Most of the DAQ cards still support writing subroutines in some kind of programming language like C or C++. A modern DAQ card actually enables us to utilize its own memory and processing power to run data acquisition independently from the control computer. Only trigger, sweep frequency setup and measured data must be transferred between the DAQ card and control computer. On the other hand, the latency may be the problem. Our tests show, that with such configuration the latency across the USB is approximately 20 miliseconds. Consecutive output set and measure time afterwards may be even faster than 1 micro second per repetition. In the case that we need a lot of configuration settings, the latency may be avoided by switching from windows platform to DOS or Windows 98 platform. There are still several DAQ cards available on the market, which are still supported in DOS mode. They also come in CardBus PC card shape and can be easily used with a laptop computer. In this case our test showed almost no latency and output set and measure time took approximately 5 micro seconds. In general, Linux is not widely supported by the DAQ card manufacturers, but the situation is improving.

This brief survey shows us, what kind of compromises must be made. Data acquisition may become even faster, if raw digital data are used for analog output configuration or voltage measurement wherever possible. In this case for unipolar operation the following formula should be used:

$$binaryValue = \frac{Voltage}{referenceVoltage} * \max\ BinaryValue \qquad (1)$$

Where max BinaryValue for 16 bit card is 65536 and referenceVoltage corresponds to the previously selected voltage range. On some cards with gain settings also gain should be considered. Therefore we have for unipolar operation:

$$binary\ Value = Voltage * \left(gain * \left(\frac{\max Binary\ Value}{reference\ Voltage} \right) \right) \qquad (2)$$

4. Generation of STDF file

After we have selected a suitable test platform and created a stable ASIC wafer sort test environment, we would like to do a fast measurement data evaluation. In the beginning of the test program development, acquired test results are usually nicely organized in plain ASCII data files. It is always possible to load such data files into various software tools and do some basic statistical analysis, plot charts and similar.

The problem arises with the growing amount of test data and tested wafers. Suddenly, such approach becomes quite time consuming and the lack of suitable, professional analysis tool is evident. There are several available on the market. In general, they will not accept our specific ASCII data file, but they will definitely accept STDF (Standard Test Data Format)/3/. STDF is a proprietary file format for semiconductor test information, originally developed by Teradyne, as a test result output of all of Teradyne UNIX operating system based testers. Teradyne derives no direct commercial benefit from propagating this standard. Now it is widely used throughout the semiconductor industry, since it is a commonly employed format. It is also produced by automatic test equipment platforms from all leading companies. STDF is a binary format, and specifications are available on the internet. It can be converted either to ASCII format known as ATDF (ASCII Test Data Format) or to a tab delimited test file. Working with STDF variable length binary field data format is not trivial, since it involves a detailed comprehension of over 100 pages long specification document.

Fortunately, conversion from STDF to ATDF does not lose any information and tools are available to do the conversion in both directions - from STDF to ATDF and vice versa. Such tool is called "STDFUtilTools" and it is also available on the internet as well as detailed ATDF specification /4/. ATDF is actually much easier to implement than STDF, so it shouldn't be a big problem for any test programmer using whichever programming language to do it. So we can conclude that STDF test data files may be produced from ATDF data files to conform to one single standard.

Anyway, ATDF specification is also quite extensive and it takes quite some time to determine the required sequence of the necessary record types. So let us give some additional information about sequence of the ATDF record types:

1. First record type should be "FAR" (File Attributes Record). It determines ATDF and STDF format versions and scaling flag.
2. "ATR" (Audit Trail Record) is second record type and it is used to record all operations essential to contents of the file.
3. "MIR" (Master Information Record) record is needed for all global information of the file.
4. "SDR" (Site Description Record) describes information about presence of test sites and test heads.
5. Then we may have several "PMR" (Pin Map Record) type records.
6. "PGR" (Pin Group Record) is used to associate a pin name with a group of pins.
7. "WIR" (Wafer Information Record) is used to mark the beginning of wafer test.
8. "PIR" (Part Information Record) acts as a marker to indicate where testing of a particular DUT (Device under Test) started. It is followed by "BPS" (Begin Program Section Record) type record. Then we can have several "PTR" (Parametric Type Record), "FTR" (Functional Type Record) and other similar record types to store measurement data. After all measurement data for one DUT is stored, we insert "EPS" (End Program Section Record) record type. The last record type is "PRR" (Part Result Record) that contains the results information relating to each part tested by the

test program. Point 8 is then repeated for all parts that were tested.

9. Then we have all necessary "TSR" (Test Synopsis Record) type records. They contain statistics for one parametric or functional test.
10. After "TSR" type record we may have several "HBR" (Hardware Bin Record) type records. They store a count of parts placed in a particular bin after testing. Here we may have "pass", "fail" or similar bins.
11. "PCR" (Part Count Record) type record includes part count totals for one or all test sites.
12. "WRR" (Wafer Results Record) type record includes results for each wafer tested by the test program.
13. "MRR" (Master Results Record) is the last type record in the ATDF file and is a logical extension of the "MIR" type record.

Above 13 points actually describe the ATDF file structure. Further details about all ATDF type records used here are shown in ATDF file specifications /4/. Figure 4 represents a small cut off from the beginning of the ATDF file. Unfortunately some lines are too long and they will not fit on one page to represent them completely.

```
FAR:A|4|2
ATR:14:13:43 23-Mar-2010|created with mx330textfile2ATDF_Ver_6.0
MIR:cxc231-1|mx330_117|mx330_117_S02010001|DAQ1|L-D630|10:30:00 8
SDR:1|0|0|TSK-APM90A|2|TIPS|1|MXldb12|1|Universal|0|0
PMR:1|2|GND|VSS|1|0
PMR:2|3|AICH1|L2|1|0
PMR:3|3|AICH0|L2|1|0
PMR:4|2|VDD|VDD|1|0
PMR:5|3|AICH5|L3|1|0
PMR:6|3|AICH7|REXT|1|0
PMR:7|3|AICH4|OUTA|1|0
PMR:8|4|AICH0|PROG|1|0
PMR:9|5|PC5|COIL|1|0
PGR:0||0
PGR:0||0
WIR:1|18:43:23 08-Nov-2009|0|1
PIR:1|0
BPS:mx_330_wafer_sort
PTR:10|1|0|0.0092|P||CUR|||A|0.0070|0.0110|%f|%f|%f|||3|3|3
PTR:11|1|0|0.8228|P||OUTA8M50|||V|0.5400|1.2700|%f|%f|%f|||3|3|3
PTR:12|1|0|0.3887|P||OUTA8P50|||V|0.1200|0.8000|%f|%f|%f|||3|3|3
PTR:13|1|0|0.4341|P||OUTA50DIF|||V|0.3000|0.6000|%f|%f|%f|||3|3|3
```

Fig. 4: Small cut off from ATDF file.

After ATDF file is generated we may use previously mentioned "STDFUtilTools" tool to create a valid STDF file. This file can be used for an automatic statistical analysis for entire population of tested devices. Usually one STDF file per silicon wafer is required, but we may also join results from several wafers into one STDF file.

5. Conclusions

In this article the most critical parts of the low cost and high precision fully automatic test system development for multi-project wafers evaluation is described. The most important features of such system are respectful test speed and accuracy to low cost ratio, easy adaptation to new ASIC versions and STDF test data compatibility. All aspects of this approach were practically implemented and tested on several wafers.

High precision magnetic micro system that was recently designed and developed in our laboratory was also successfully characterized with such system. Test demands were about 2300 accurate voltage measurements, 18 precise frequency measurements and selective trimming, setting or reading of 250 OTP (one-time programmable) fuses per part at two different temperatures. Unique serial number was also written via OTP fuses to each part. This enables later measurement comparison of packed parts and identification of wafer sort measurement data from the STDF file. Average test time per part was approximately 850 miliseconds and could be even faster, if no DUT settling delays were necessary. Wafer prober moving time is half a second per part, so wafer sort time was a little bit less than 1.5 second. For the time being about one quarter of a million parts were successfully tested.

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DEVELOPMENT OF IMAGE ANALYSIS PROCEDURES FOR EVALUATION OF PRINTED ELECTRONICS QUALITY

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Key words: printed electronics, image analysis, RFID, ImageJ, printed UHF antenna.

Abstract: The procedures described in this work show the feasibility of the first stage of standardized methods for evaluation of printability of printed electronics.

Printed electronics are electronically functional devices printed onto media like paper, plastic, flexible materials, textiles etc. One of the main goals of printed electronics is simply that electronic components could be printed with mass printing technologies, enabling fast production speed and cheaper products. A new area of applied research is focusing on providing several methods for quality evaluation of printed components to perform fast on-line characterisation.

Within present research we study the potential to develop a system for detection of printing defects and imperfections such as substrate non-uniformity and poor surface ink coverage during in-line (in-situ) production of printed electronics. The possibilities for fast and relevant in-line control of printed electronic devices are introduced and applied on printed antenna samples applied for RFID (Radio Frequency Identification) tags.

For evaluation and the prospects of development of procedures for in-line control, image analysis is used with applying ImageJ software. Each separate layer (surface of printing material and conductive printed ink) was captured by CCD camera, stereo microscope and scanning electron microscope. Further, it was evaluated by ImageJ software. For automatic and relevant evaluation different routines were used, developed, modified or upgraded; 1) macro for printing surface coating non-uniformity, 2) macro for evaluation of percentage of coverage of conductive ink on the printed substrate and 3) procedure including 3D visualization plug-in to evaluate ink layer thickness in all three (x, y, z) dimensions.

The first routine presented here gives the information about the homogeneity or potential defects of printing material surface (with or without pre-coating). The non-uniformity of surface coatings and functional layers is an important property of printed electronics as it is directly related to the electrical properties and therefore to the performance of printed electronic. Other two routines give relevant information about percentage of coverage and thickness of printed functional ink layer. That tells us whether printed electronic element is OK or destruct. This way a reliable procedure was obtained for quick on-line (in situ) testing of printed electronics.

These results present the first stage of our research, which is focused on to set up the steps and possibilities for using presented in-line control methods for evaluation of printed electronic devices. The presented procedures could in future be applied for in-line control at printing speeds.

Razvoj metod slikovne analize za oceno tiskovne prehodnosti tiskane elektronike

Kjučne besede: tiskana elektronika, slikovna analiza, RFID, ImageJ, tiskana UHF antena.

Izvleček: Pokazana je možnost hitre in učinkovite kontrole kvalitete struktur tiskane elektronike, ki se izvede med procesom oz. med posameznimi fazami tiska. Pokazan je primer uporabe na tiskani anteni za pasivni RFID. Uporabljena je slikovna analiza mikroskopskih posnetkov s pomočjo ImageJ programa. Površine tiskovne podlage v vsaki fazi tiska se posnamejo s CCD kamero, optičnim mikroskopom in/ali elektronskim mikroskopom, dobljeno sliko pa se digitalno analizira. Za potrebe te analize so bili prilagojeni, razviti ali uporabljeni različni numerični pristopi: 1) makro za analizo enakomernosti površine, 2) makro za vrednotenje deleža površine, ki je pokrita s funkcionalno prevodno plastjo in 3) makro za 3D vrednotenje debeline in oblike plasti v (x,y,z) smereh. Prikazani rezultati so del raziskav v smeri iskanja učinkovitih in hitrih metod za nadzor tiskovne prehodnosti sistemov tiskane elektronike. Za integracijo predlaganih postopkov v tiskarske sisteme bi bilo potrebno vanje vgraditi zgolj vhodne naprave, kot so, npr. CCD kamere..

1. Introduction

Electronically functional devices printed onto media like paper, plastic, flexible materials, textiles etc. are today represented as printed electronics. The majority of applied materials are organic, therefore also the term "organic electronics" is applied – this distinguishes it from classic electronics which base on inorganic materials.

However, in practice organic materials are not applied only by some printing technique, therefore the terms printed electronics and organic electronics may designate products of different technologies.

One of the main goals of printed electronics is simply that it could be printed with mass printing technologies, enabling fast production speed and cheaper products.

Printable electronics technology has the potential to drastically reduce ecological footprint and energy consumption in manufacturing process. For example, digital fabrication using inkjet technology, by patterning high-purity electronically functional materials without the original patterning masks, can reduce costs and turnaround time /1/.

Print techniques used in production of printed electronic structures are screen-printing, offset, gravure printing as

well as flexography, inkjet printing and laser-based printing. The first demonstration was performed on screen printing, which is also used for defining source-drain electrodes (channel length 200 mm, thickness 10 mm) /2/. Offset, the most commercial printing technique, is also very attractive for electronic manufacturing when the right compromise between ink viscosity, surface tension and evaporation rate is established /3/. Gravure printing is less used, but conductive carbon-based ink for interconnections and gate-electronics can be printed with this technique /4/. Flexography is also much less used because the flexible printing plate causes stamp distortions on the prints, resulting in problems with prints accuracy /5/. Plastic transistors created with ink-jet printer present a new low-cost electronics option.

Xerox has reported in 2005 that they have come up with air stable versions of printable electronic elements (conductors and insulators) needed to make long lasting circuits easier /6/.

Another advantage of organic electronic is capability to bend without losing its functionality. The creation of stretchable electronics originates from metal electrodes on rubber substrates, showing good mechanical but poor electronic properties. Nevertheless, active matrix sheet was reported that can be stretched by 70 % without mechanical or electrical damage /7/.

For such applications electrically functional printing inks are needed. Simplified structures of electronic components can be prepared by very small number of them /8/. This is in principle in agreement with industrial printing machines where typically 4 to 12 printing inks or the same number of printing processes are available in series. A number of research studies are focused on modification of different polymer materials to get various electronically-functional properties which are suitable for printing with conventional high-speed printing technologies /9-12/. The potential to adapt graphic art printing techniques to the manufacture of functional devices is today the focus of many research groups. They put the emphasis on the structures for integration of advanced functionality, other than only graphic information on different substrates. It is inspired by the need to reduce the manufacturing cost of existing electronic devices like radiofrequency identification (RFID) tags. Low cost printing can also enable the use of electronic devices in modes, applications and environments, which are currently not accessible by conventional electronics.

A functional ink which is printed in a given shape must form more-or-less continuous layer to assure its proper (acceptable) functionality. Most printing techniques give dot-shaped off-prints rather than uniform coverage of printed shapes. The print quality of normal graphic art applications regards visually accepted quality which, most likely, will not fulfil demands of electronic functionality. In this area more continuous coverage is desired and should be evaluated accordingly. Therefore new and precise methods to evaluate coverage are desired.

Those would also reveal whether some parts of the functional layer were damaged. In this case the coverage of substrate is considerably smaller what may cause inappropriate operation of printed layer or not operation at all. By precise evaluations those faults could be eliminated on time.

Suitable methods that control printability of printed electronic devices are based on structure - property relations. The microscopy methods, like AFM (Atomic Force Microscopy) or SEM (Scanning Electron Microscopy) are used to see the surface. X-ray diffraction data are used to understand the relationship between nucleation, growth, crystallinity and device performance /13/.

By using AFM a wide variety of growth morphologies were observed in organic thin films, revealing the complexity of the building blacks /14/. Other methods used to evaluate the printability are layer thickness determination, optical density and surface resistance.

A new area of applied research is focusing on providing several methods for quality evaluation of printed components to perform fast on-line characterisation.

Image analysis is one of them and is fast and suitable for in-line control of printing process even thought images are captured by digital still cameras. It was already shown that digitally captured images are comparable when compared to newly developed coloured films, though films still show better 3D structure, better details, higher sensitivity and wider dynamic range /15/.

Optical images of printed polymers at magnification rates showing the whole array or just small regions are used to estimate the quality of print. At that stage, the print errors can be determined while still in the production line (in-line control) /16/. Analysis and measurements need to be carried out to pre-process the images and minimize the deformations. In the paper from 2006 the authors have defined five steps for image analysis and processing; 1) the threshold to isolate the area of interest on the image, 2) isolation of pixels in the background, 3) simple calibration of pre-set dimensions in X and Y dimensions, 4) particle filtering analysis to remove particles according to their morphological properties, and 5) the edge-enhancement analysis to enhance the edge, separating it from the background /17/. Following these steps the line patterns in a circuit image can be enhanced so the centre and width of the circuit can be analyzed.

In the field of printed electronic the base surface uniformity of printed material (i.e. a substrate) is also very important. The completely uniform surface without any cracks or any other surface defects has to be achieved, especially when several layers are overprinted to get the final functionality. The polymer foils which are frequently used as printing substrate, usually have adequately uniform surface. In applications in which the paper or board are used as substrates, more surface defects are usually observed. In such cases, the printed conductive ink layer may not

enable desired conductivity and destruction of electronic component may not be an exception. This is the reason why hydrophobic pre-coatings are applied on absorptive materials like papers and boards.

It is essential to recognize problems concerning non-uniformity of the surface as early as possible, best during the printing process. This way the quality of printed electronics could be detected practically on-line during successive printing steps.

2. Materials and methods

For the purpose of present research the professional example of printed UHF (Ultra High Frequency) RFID antenna from a commercial design (COPACO) from the LOPE-C exhibition brochure (Organic Electronics, OE-A) /18/ was investigated. It is presented on Figure 1, reproduced by diverse image capture methods. Antenna was printed with conductive silver ink directly onto cardboard, frequently used for printing electronics in packaging, which was at the same time evaluated by the means of surface coating non-uniformity.

Images of selected sample (antenna and printing surface) were captured using stereo microscope Leica EZ4D with integrated digital image capture device, digital camera NIKON D300 with Nikkor AP-S micro 105mm, 1:2,8G-ED lens and SEM - scanning electron microscope JSM6060LV by JEOL. For SEM observation the sample was coated by C+Au/Pd mixture in vacuum evaporator by JEOL, Japan.

The images were saved in either .jpg and .tiff file format and analyzed with ImageJ /19/. It is freeware software for image processing and analysis in Java, inspired by NIH Image for Macintosh. For automatic and relevant evaluation different routines were used, developed, modified or upgraded; 1) macro for printing surface coating non-uniformity, 2) macro for evaluation of percentage of coverage of conductive ink on the printed substrate and 3) procedure including 3D visualization plug-in to evaluate ink layer thickness in all three (x, y, z) dimensions.

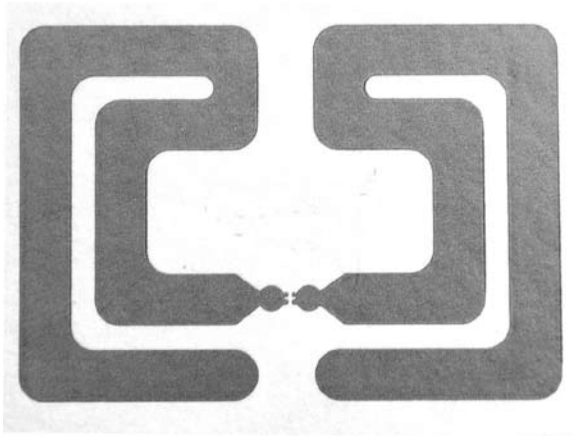
3. Results and discussion

3.1 Diverse image capture methods

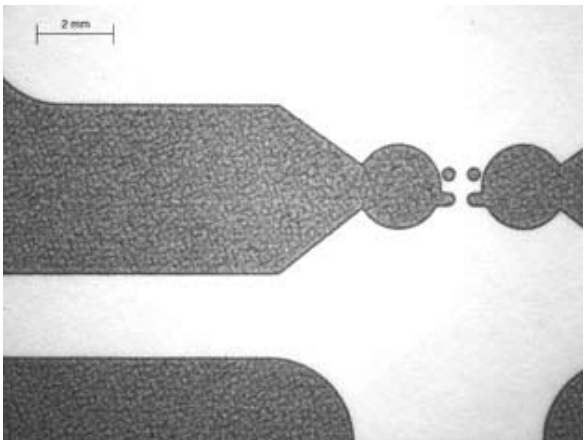
RFID antenna, reproduced by diverse image capture methods is presented on Figure 1.

Different image capture devices results in different surface texture details of the sample presented. Digital camera images and images obtained by stereomicroscope can be used both for research, as well as for in-line control, though magnification conditions have to be experimentally determined. SEM images were later used for 3D calibration of 2D images taken by other two capturing methods to determine the thickness of printed layer and were.

a)



b)



c)

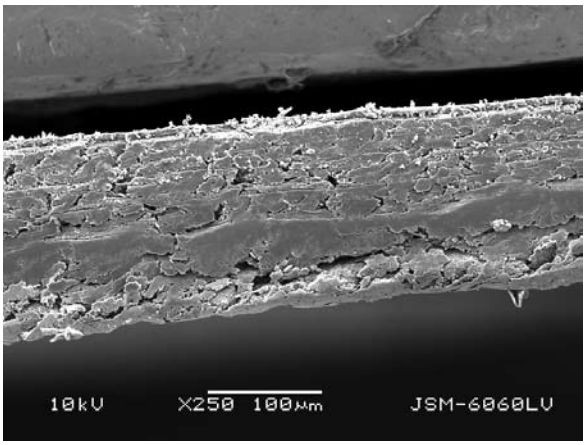


Fig.1: RFID antenna captured with digital camera (a), stereomicroscope (b) and SEM (c) respectively.

3.2 Surface coating non-uniformity

To evaluate the non-uniformity of the printing substrate surface coating as an important property of printed electronics, a special macro was developed. The amount of non-uniformity is calculated on the basis of the image's histogram which represents the number of pixels as a function of their intensity (gray value). The amount of the non uniformity is expressed as the Non-uniformity index (NU):

$$NU = U_x - L_x \quad (1)$$

where U_x and L_x are the average gray values of pixels above and below median grey value, respectively. U_x is calculated as the mean of the intensities between median and maximum gray values of the histogram, whereas L_x is calculated as the mean of the intensities between minimum and median gray values of the histogram. The larger is NU, the greater is the surface non-uniformity. It reveals the relevant measure of the usefulness of the surface texture for application of a functional layer with desired properties. NU value measures whether its surface is uniformed enough.

The designed macro includes sequence steps:

```
saveSettings();
setBatchMode(true);
run("8-bit");
run("Set Measurements...", "mean min median limit
redirect=None
decimal=2");
Dialog.create("Select Area Dimensions to Evaluate");
Dialog.addNumber("Width (px):", 200);
Dialog.addNumber("Height (px):", 200);
Dialog.show();
w = Dialog.getNumber();
q = Dialog.getNumber();
makeRectangle(0, 0, q, w);
ID1 = getImageID();
setTool(0);
beep();
print("Wait For User", "Select Area to Analyze");
if (selectionType () !=0)
exit("Please select rectangle!");
selectImage(ID1);
run("Measure");
median = getResult("Median");
getMinAndMax(min, max);
selectImage(ID1);
//run("Threshold...");
setThreshold(min, median);
run("Measure");
mean = getResult("Mean");
Lx = mean;
resetThreshold;
selectImage(ID1);
//run("Threshold...");
setThreshold(median, max);
run("Measure");
mean = getResult("Mean");
Ux = mean;
resetThreshold;
selectImage(ID1);
NU = (Ux-Lx);
showMessage("Histogram Mottle: ", "Non-uniformity number (NU) is:
"+NU);
title = getTitle();
print(title+" NU is: "+NU);
restoreSettings();
```

The evaluation of surface non-uniformity is shown on Figure 2. The example shows the printed antenna's substrate – a commercial base material, frequently used for printing electronics (coating barriers paper). The NU of the sample is 9,99. If the value would be higher (more uneven base) the functionality of ink layer printed over such a base could be unacceptable. The limit NU level must be defined for each applied substrate individually.

In each case the range of acceptable values have to be determined with some separate experiment.

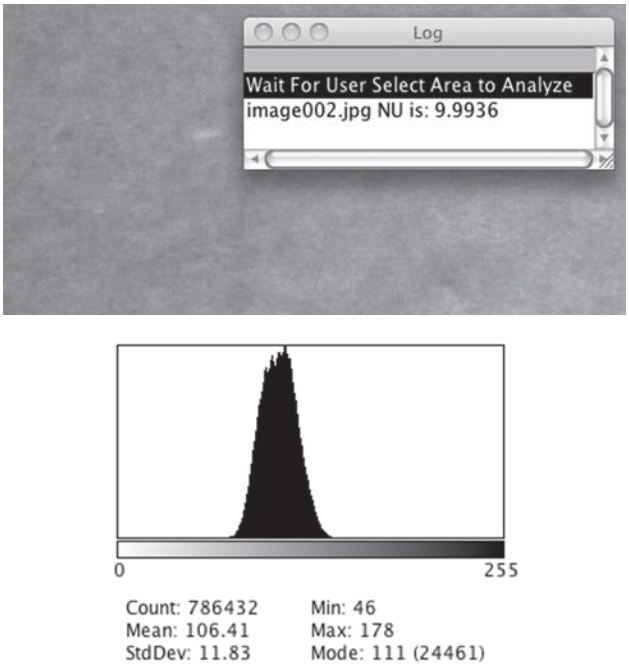


Fig. 2: An example of evaluating of surface coating non-uniformity. The coating barrier paper was captured by stereo microscope Leica EZ4D at 35 x magnification in reflection mode. The histogram of gray values on this picture was obtained by its analysis with ImageJ software.

3.3 Percentage of coverage of functional ink on the printed substrate

To evaluate the print quality of the ink layer, the macro for evaluating the percentage of coverage was upgraded and modified. It measures the coverage of the printing substrate with the printing ink. The adequate percentage of ink coverage is limited by minimal and maximal area covered. These values must be given in advance experimentally.

The procedure was tested on test RFID antenna sample, shown on figure 3.

The example (Figure 3) shows a UHF-antenna designed by COPACO and printed with conductive silver ink directly on cardboard. The applied macro gives relevant information about the print quality in terms of adequate ink coverage

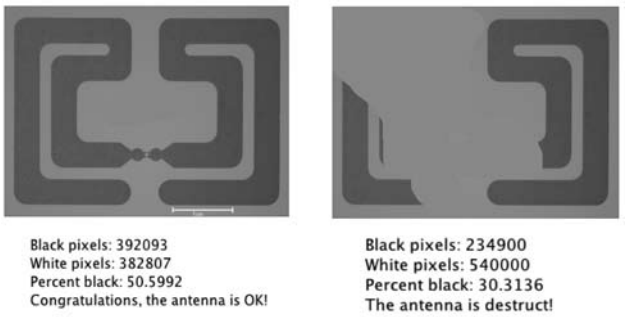


Fig. 3: RFID antenna with application of the macro for evaluation of percentage of coverage of conductive ink on the printed substrate. Left image: good antenna with adequate ink coverage and good ink printability; right image: completely destroyed antenna – ink coverage is not sufficient.

of the passive antenna. If the area of ink layer is not adequate, the macro gives the information that the antenna is destruct. In the presented example the sufficient ink area was determined according to area of CCD captured image on the good-working antenna. For a good on-line evaluation process the limit for covering has to be defined in advance.

The macro steps were as follows:

```
run("8-bit");
run("Make Binary");
if (bitDepth!=8)
exit("This macro requires an 8-bit image");
black = 255;
white = 0;
getHistogram(0, hist, 256);
total = 0;
for (i=0; i<256; i++)
total += hist[i];
print("");
print("Black pixels: " + hist[black]);
print("White pixels: " + hist[white]);
print("Percent black: " +100*hist[black]/total);
P=100*hist[black]/total;
if (P<=30)
print("The antenna is destruct!");
else
print("Congratulations, the antenna is OK!");
```

3.4 Ink layer thickness evaluation in three dimensions

The thickness of conductive ink layer of passive RFID antenna is very important. Among others, it determines the conductivity level and thus, the quality factor of the antenna. With the use of 3D visualization plug-in and custom developed routine, the quick and relevant method for analysis of ink thickness in z-direction from 2D sample image captured by CCD camera can be performed. First, the ink thickness was evaluated by cross cutting of the sample and capturing it by SEM (Figure 4). The thickness of the ink layer was determined by image analyzing tool included in SEM software. The printed passive RFID antenna was then captured by CCD camera. The image was transformed into 8-bit image and Set-scale tool was used to calibrate x and y dimensions in millimetres. After that, the 8 bit image was calibrated in z-direction, by determining and calibrating the ink thickness to grey value. For the final evaluation of ink layer thickness in three dimensions, the image was transformed into 32-bit image type and the plug-in 3D interactive surface plot /20/ was used (Figure 5).

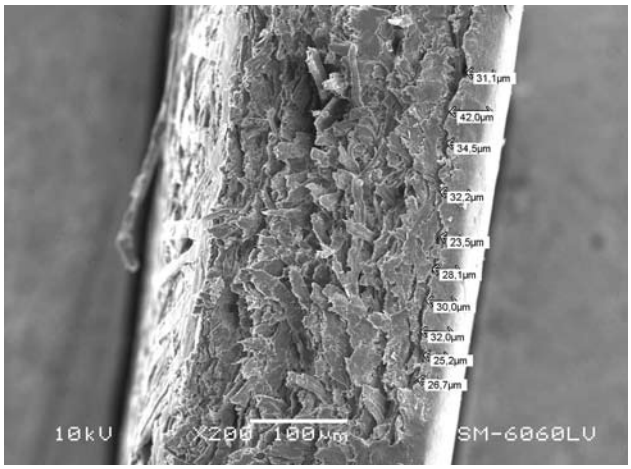


Fig. 4: SEM micrograph of UHF-antenna sample from Fig. 3. Cross cut shows the conductive ink layer on the right side and its determination of the thickness.

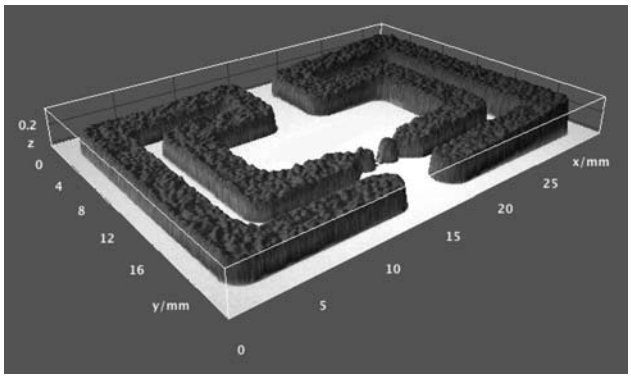


Fig. 5: The example of using macro/plug-in for evaluating the ink layer thickness in three dimensions. In image the UHF-antenna sample from Figure 3 is presented.

Figure 5 shows that captured 2D image, by applying 3D interactive plug-in, can be used to visualize and obtain precise information about ink layer of passive printed antenna in all three directions, acting as a fast analyzing tool for the evaluation of final printed antennas.

4. Conclusions

The procedures described in this work show the feasibility of the first stage of standardized methods for evaluation of

printability of printed electronics. We study the potential to develop a system for detection of printing defects and imperfections such as substrate non-uniformity and poor surface coverage with ink during in-line production of printed electronics.

For automatic and relevant evaluation of printability of printed electronics different routines were used, developed, modified or upgraded utilizing image analyzing software Image J; 1) macro for surface coating non-uniformity, 2) macro for evaluation of percentage of coverage of conductive ink on the printed substrate and 3) procedure including 3D visualization plug-in to evaluate ink layer thickness in all three (x, y, z) dimensions.

The first routine presented here gives the information about the homogeneity or potential defects of printing material surface (with or without pre-coating). Other two routines give relevant information about percentage of coverage and thickness of printed functional ink layer, which is an indicator whether printed electronic element is OK or destruct. This way a reliable procedure was obtained for quick on-line (in situ) testing of printed electronics.

The presented procedures could in future be applied for in-line control at printing speeds. For performing described analysis, in existing printing equipment only the input devices like CCD cameras in the line of printing units should be incorporated.

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ABSORPTION OF MICROWAVE POWER IN NITROGEN PLASMA AT MODERATELY LOW PRESSURE

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Key words: plasma; reflected power; matching; power transfer; energy absorption; electron motion

Abstract: The efficiency of microwave absorption by nitrogen plasma has been studied. Plasma was created within a quartz glass tube mounted perpendicular to a microwave cavity. The cavity was powered by a microwave generator operating at a standard frequency of 2.45 GHz and adjustable nominal power up to 1200 W. Plasma was created at low pressure. The quartz tube was pumped with a two stage rotary pump with a nominal pumping speed of 33 m^3/h. A valve was mounted between the tube and the pump in order to adjust the effective pumping speed. The pressure of nitrogen in the quartz tube was thus varied between 100 Pa and 2500 Pa. The experiments were performed at the gas flow of 20 l/h. The nominal and adsorbed powers were measured with appropriate power meters. At low nominal power the reflected power was rather low but it kept increasing with increasing nominal power. The reflected power also depended on the pressure. The reflected power decreased monotonously with increasing pressure. At the highest pressure the reflected power was about 5 times lower than at the lowest pressure. The results were explained by energy accumulation of electrons at elastic collisions during oscillation in EM field.

Absorpcija mikrovalovne moči v dušikovi plazmi pri nizkih tlakih

Kjučne besede: plazma, odbita moč, uskladitev, prenos moči, absorpcija energije, gibanje elektronov

Izvleček: Preučevali smo učinkovitost absorpcije mikrovalov v plazmi dušika pri nizkih tlakih. Plasma je bila ustvarjena v cevi iz kvarčnega stekla, ki je bila nameščena pravokotno na mikrovalovni resonator. Resonator je bil napajan z mikrovalovnim generatorjem, ki deluje na standardni frekvenci 2,45 GHz in ima nastavljivo nazivno moč do 1200 W. Razelektritveno cev smo črpali z dvostopenjsko rotacijsko črpalko z nazivno črpalno hitrostjo 33 m^3/h. Med cevjo in črpalko je bil nameščen ventil, s katerim smo uravnavali efektivno črpalno hitrost. Tlak dušika v razelektritveni cevi je tako bil med 100 Pa in 2500 Pa. Eksperimenti so bili izvedeni pri pretoku plina 20 l/h. Nominalno in adsorbirano oz. odbito moč smo merili z ustreznimi merilniki moči. Pri nizki nominalni moči je bila odbita moč sicer majhna, vendar je z naraščajočo nominalno močjo naraščala. Odbita moč je bila odvisna tudi od tlaka. Odbita moč je monotono padala z naraščajočim tlakom. Pri največjem tlaku je bila odbita moč približno 5-krat nižja kot pri najnižjem tlaku. Rezultate smo pojasnili s kopičenjem energije elektronov pri elastičnih trkih med nihanjem v EM polju.

1. Introduction

Low pressure gaseous plasma is nowadays widely used for treatment of different materials /1-9/. Depending on specific needs plasma is created by various electrical discharges. Basically we can distinguish between two types of discharges: those where charged particles are accelerated in sheet region next to the electrodes, and those where charged particles are accelerated in electrical field presented in the volume. Examples of the first type of discharges include a simple DC glow discharge /10,11/, capacitively coupled RF discharge /12,13/ and hot-cathode as well as hollow cathode discharges /14/. The second type of discharges includes a variety of resonance discharges such as the popular electron cyclotron resonance (ECR) discharges /15,16/, inductively coupled RF discharges /6,9,17/ and MW discharges /18-22/. The absorption of energy supplied by an appropriate power supply is usually very high at surface discharges, but in volume discharges they may or may not be that high. If conditions for resonant acceleration of charged particles in electromagnetic fields are met, the power absorption is usually pretty high. On the other hand, the absorbed power could be very low and many authors use expressions like unmatched or unbalanced plasma. The problem of insufficient power absorption is particularly severe in devices for modification of the properties of solid materials since the optimal conditions for power absorption can not be made due to particular requirements regarding the samples that are treated. In such cases a compromise between the requirements and the power absorption should be made. A pretty good example is plasma created in a microwave cavity. In this paper we present results on systematic measurements of the reflected power in order to show the right conditions for plasma generation.

2. Experimental

Experiments were performed at solar facilities of PROMES-CNRS laboratories for treatment of materials in Font Romeu through the FP7 program SFERA. The experimental reactor MESOX is used for characterization of high-temperature materials properties after exposure to gaseous plasma at extreme conditions. Samples are heated by concentrated light at maximum power of 5 kW concentrated on a spot area of about 1 cm2 and simultaneously heated by gaseous

plasma. A schematic of the experimental system is shown in Fig. 1. Plasma is created in the discharge chamber which is 50 cm long quartz glass tube with the diameter of 5 cm. The tube is pumped with the two stage rotary pump with the nominal pumping speed of 33 m^3/h. There is a variable valve between the pump and the discharge chamber. The valve serves for adjusting the effective pumping speed at the exhaust of the discharge chamber. Depending on the valve adjustment the pumping speed can be decreased down to about 1 m^3/h. Gas is leaked into the discharge chamber on the other side through flow controller. The maximum throughput of the controller is 20 l/h. Pressure is measured between the discharge chamber and the variable valve as shown in Fig. 1. The pressure in the discharge chamber depends on the position of the leak valve as well as the variable valve. At current experiments we created plasma in pure nitrogen.

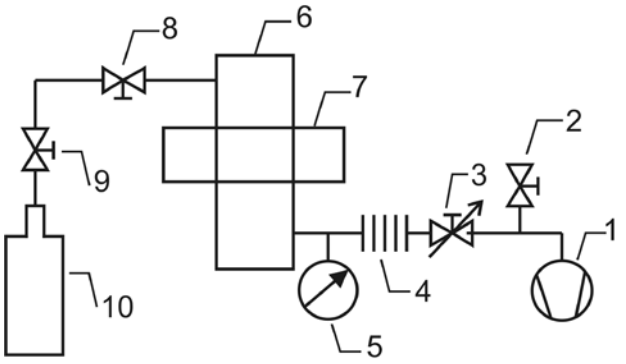

Fig. 1: Schematic of the experimental vacuum system: (1) rotary pump, (2) venting valve, (3) adjustable valve, (4) bellows, (5) absolute vacuum gauge, (6) discharge chamber, (7) MW cavity, (8) leak valve with flow meter, (9) high pressure valve, (10) nitrogen flask.

Plasma was created by a microwave (MW) generator. A detail about plasma system is shown in Fig. 2. The discharge chamber is placed perpendicularly to the microwave cavity which is made from copper and has standard dimensions of 9×4×15 cm^3. The cavity is powered with the MW generator operating at the standard industrial frequency of 2.45 GHz and at adjustable power up to 1200 W. On the other side of the microwave cavity there is manually operating matching unit. At our experiments the matching unit was optimized at the maximal effective pumping speed (practically equal to the nominal pumping speed of the vacuum pump) and was kept at that position during all experiments. The MW generator is equipped with a MW power meter, while the wave-guide between the MW generator and the cavity is equipped with a meter of the reflected power, as shown in Fig. 2.

Experiments were performed at different pressures in the microwave cavity corresponding to different effective pumping speeds. Pressure was measured with an absolute vacuum gauge. Depending on the opening of the variable valve the pressure in the discharge chamber was between

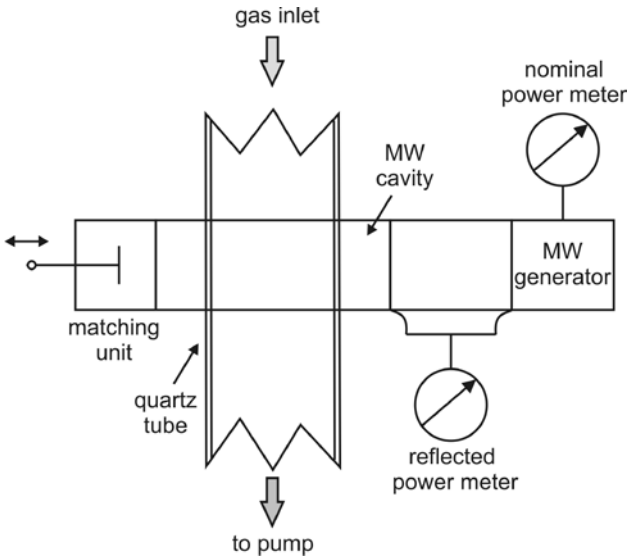

Fig. 2: Detail of the discharge chamber with MW apparatus.

100 Pa and 2500 Pa. At each pressure we performed measurement of the reflected power versus the nominal power of the microwave generator. At high pressure it was possible to perform measurements up to the nominal power of 800 W, but at lower pressure measurement up to lower power were realized because of the automatic switch-off function of the MW generator. Results of systematic measurements are summarized in Fig. 3.

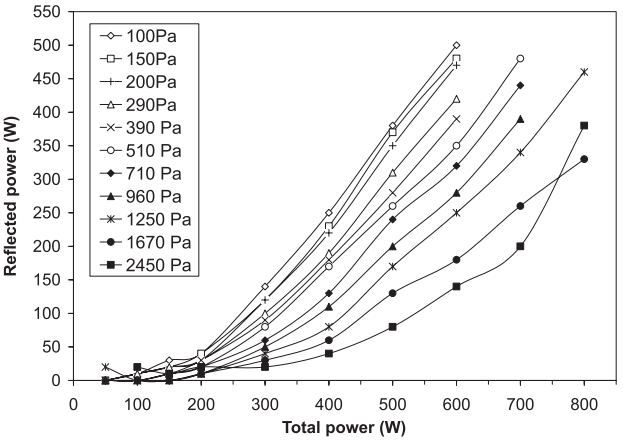

Fig. 3: Reflected power versus the nominal power of the MW generator. The parameter is the nitrogen pressure in the discharge chamber.

3. Discussion

The results of the measurements of the reflective power shown in Fig. 3 reveal some interesting features. As a general rule the reflected power increases with increasing the nominal power. At low power up to about 200 W the reflected power is much lower than the nominal power indicating rather good matching of the microwave generator. As the total power is increased, the reflected power is increased too. The increase of the reflected power

depends enormously on the pressure. At low pressures the increase of the reflected power is pretty steep while at higher pressures a pretty good matching is observed at the total power of say 500 W. Such a huge discrepancy in matching between different pressures is explained by transfer of energy between the electromagnetic field and free electrons in nitrogen plasma.

Charged particles are accelerated in electric field. The energy gained from the field does not depend on the type of charged particle (electrons or ions) in the DC field. Namely, the energy gained is just $e \cdot U$, where e is the charge of the charged particle and U is the voltage, $U = E \cdot x$. Here, E is the electric field and x is the path. This also holds for AC electrical field as long as the frequency is low. As the frequency of the electrical field increases, the charged particles may not rich the walls of the chamber but they start oscillating in the electrical field. The oscillation of a charged particle with mass m in high-frequency electrical field is described by the basic equation /23//23/:

$$m\ddot{x} = eE_0 \cos\omega t \qquad (1)$$

The kinetic energy of charged particles depends on the frequency (ω) and the mass of the charged particle (m) and is determined as:

$$W_k = \frac{1}{2} m\dot{x}^2 \qquad (2)$$

where $\dot{x}$ is the velocity, i.e.

$$\dot{x} = \frac{eE_0}{m\omega} \sin\omega t \qquad (3)$$

The oscillation amplitude is determined by integration of the Eq. (1) and is:

$$x = -\frac{eE}{m\omega^2} \cos\omega t \qquad (4)$$

The Eqs. (1-4) reveal important fact about oscillations of charged particles in high-frequency electrical field. First, the oscillation amplitude and the energy gained depend on the mass of the charged particle. Massive particles gain much less energy than particles with a low mass. The mass of nitrogen molecules is about 30.000-times larger than the electron mass. From Eqs. (1-4) it is clear that charged nitrogen molecules can not follow the oscillations of the electromagnetic field when the frequency is moderately high. In practical cases this often happens at the frequency of about 1 MHz. The frequency of the electrical field in our MW discharge is over 1.000-times larger at 2.45 GHz. Massive ions practically do not feel such high frequency electrical field so they gain practically no energy. On the other hand electrons are much lighter so they are still capable of oscillating with a reasonably large amplitude and kinetic energy. Electrons oscillating in vacuum cannot accumulate energy from the electrical field. Namely, when they reach maximal kinetic energy the electric field is transversed so they are slowing down instead of accelerating. An electron can only accumulate the kinetic energy if suffering an elastic collision with a heavy particle at the time when it has the maximum kinetic energy obtained from the electric field. Namely, at elastic collision the kinetic energy of the electron is preserved, but the direction of the velocity becomes opposite. The electron is thus capable to take advantage of further accelerating in the electric field. If such collisions happen each time when the electric field is changed, the electron can accumulate a lot of energy. In the ideal case, the path between the two collisions should be equal to the oscillation amplitude. In such a case the electron would be able to keep accumulating its kinetic energy so it could gain energy much larger than the maximum energy according to Eq. (2).

The path between two collisions depends on several parameters, but the major one is the pressure. The mean free path decreases linearly with increasing pressure. At the pressure of 100 Pa the mean free path is roughly 10^{-4} m. This is at least of order of magnitude larger than the oscillation amplitude of electrons at 2.45 GHz and power of the order of 100 W. At low pressure obviously the electrons cannot gain much energy from the oscillating electromagnetic field. As the pressure increases the mean free path decreases so the accumulation of kinetic energy by electrons become more and more efficient. The electrons can thus accumulate energy at higher pressure and this accumulation is illustrated as better matching between microwave field and nitrogen plasma. The decrease of the reflected power with increasing pressure is demonstrated in Fig. 3. is therefore explained by better accumulation of the electron kinetic energy.

The upper consideration explains a huge difference in the reflected power versus pressure at high nominal power. Let us now discuss a rather good absorption of MW power at low discharge power. At the nominal power of about 100 W the absorbed power is almost perfect. As mentioned above the matching unit was adjusted just to have best matching at such conditions. The pretty good absorption of MW power at low powers cannot be explained by accumulation of electron kinetic energy at collisions but other effects should be taken into account. As mentioned earlier the heavy particles are not accelerated in the microwave field so their velocity is orders of magnitude smaller than the electron velocity. The consequence of such huge difference between positive ions and electron velocities is depletion of plasma since electrons escape on the walls leaving positive ions in the gas phase. Plasma becomes positively charged against the walls of the discharge chamber. The potential difference between the gas phase and the surface obviously depends on the ratio between electron and ion velocities, but is typically of the order of 10 V. This voltage prevents further depletion of the electrons and causes acceleration of ions towards the surface of the discharge chamber. The typical thickness of the sheath between the wall and unperturbed plasma is of the order of the Debye length /24/. This holds for chamber walls far from any electrode. In practice however there are always electrodes present and the voltage between plasma and the wall backed by an electrode can be as high as several

100 V. Such voltage is high enough to cause acceleration of positive ions onto the wall surface where they may emit a free electron. Electron enters the sheath and is accelerated to an energy which is large enough for sustaining the discharge. A rather good matching at low powers is therefore explained by such surface effects rather than by acceleration of charged particles in the volume.

Here, it is worth mentioning that formation of sheath is only possible when we already have charged particles in the gas phase. Charged particles can be only obtained by multiplication at ionization collisions which is possible only if electrons accumulate their energy. The discharge at low voltage therefore cannot be ignited. This is sound with experiments performed in any lab with MW plasma: the ignition of the discharge is only possible at high power. As mentioned earlier our experiments were performed in such a way that a discharge was ignited at maximum power and once plasma was established, the power was decreased. Opposite procedure would never be possible.

4. Conclusions

The absorption of MW power by nitrogen plasma was studied versus the pressure. While the absorption was pretty good and it did not depend much on pressure at low power, huge differences were observed at large power. The power absorption at low pressure and large power was only about 20% of the available power. At larger pressure, the absorption of MW power became reasonably good also at larger nominal powers. The huge differences in the absorption ability were explained by oscillations of electrons in the electromagnetic field and accumulation of kinetic energy at elastic collision with gaseous particles. At low power, on the other hand the energy accumulation was rather poor so pretty good power absorption was explained by effects in the sheath between the unperturbed plasma and the surface of the discharge tube. The results clearly indicate that high pressure is more suitable for plasma generation by MW discharge. If there is a need for nitrogen plasma generation at lower power one is recommended to use discharge at a lower frequency, such as inductively coupled RF discharge.

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A NEW TEMPERATURE COMPENSATED CURRENT CONTROLLED CONVEYOR

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Key words: Conveyor, Temperature Compensation, Circuit, SPice Simulation

Abstract: A simple and effective temperature compensation scheme which generates approximately temperature-independent output current for a current controlled conveyor and its application to a current-mode oscillator is designed and introduced. The temperature sensitivity of the current controlled conveyor's parasitic resistance is reduced by this new design. This proposed circuit includes two current conveyors and a translinear circuit. The circuits' theoretical analysis was carried out, and the performance of the block circuit was confirmed through PSpice simulation results. From the simulation results for applications of proposed circuit, we found that the circuit's temperature-dependence was reduced.

Novo temperaturno kompenzirano vezje CCCII

Kjučne besede: CCCII, temperaturna kompenzacija, vezje, SPice simulacija

Izvleček: V članku opišemo enostaven in učinkovit pristop k izvedbi tokovno krmiljenega in temperaturno kompenziranega vezja CCCII, kakor tudi njegovo uporabo pri izvedbi tokovno krmiljenega oscilatorja. Z novim pristopom znižamo temperaturno občutljivost parazitnih uporov CCCII. Opravili smo teoretično analizo vezja in potrdili funkcionalnost posameznih blokov s pomočjo PSpive simulacije. Iz rezultatov sklepamo, da smo vezju za to uporabo močno zmanjšali temperaturno odvisnost.

1. Introduction

Until recently, a current-mode circuit has been used as the main building block in circuit design. The fact that the gain-bandwidth product is fixed in voltage mode circuits and the slew rate is bounded are disadvantages in many electronic circuit applications. Because current-mode circuits have a number of positive characteristics, such as large bandwidth, high slew rate, wide dynamic range, low power consumption, basic circuit structure and wide linearity, they are used widely in electronic circuit design, especially for oscillator and filter circuits /1-4/.

Current conveyors and related current-mode circuits have begun to emerge as an important class of circuits with properties that enable them to surpass their voltage-mode counterparts in a wide range of applications. A current-mode approach is not just restricted to current processing, but it offers important advantages when interfaced to voltage-mode circuits. The Current Controlled Conveyor (CCCII) which is electronically controllable by a biasing current has been employed in many applications /5,6/. CCCII has been used as a part of filters, oscillators, multipliers and many current-mode applications that require temperature compensation /6-8/. Parasitic resistance is essentially a disadvantage in electronic circuits. But it is used to advantage in current controlled conveyor circuits because it can be easily controlled by biasing current. Output current is negatively affected by the temperature dependence of this resistance /9/. This resistance is directly proportional to thermal voltage for bipolar technology /10/ and surface mobility (μ) for CMOS technology /11/. This means that the characteristics of the current controlled current conveyor-based circuits will depend strongly on the absolute temperature. Also the MOS transconductance parameter is affected by a strong dependence on temperature /12/. Therefore, a technique for temperature compensation is required. In a previous study /16/, a temperature compensated scheme for a translinear current conveyor-based circuit was investigated. This scheme had a disadvantage because it includes a resistor as a passive component. Also the temperature coefficient of the resistor was neglected in that work /16/. Until now, it is not shown that temperature compensated CCCII is used some where else.

In this study, a new circuit building block which consists of two CCCIIs and a translinear circuit block was designed for temperature compensation. The new building block, called the temperature compensated current controlled conveyor (TC-CCCII) has no passive component. Parasitic resistance's temperature dependence is eliminated, so that temperature compensation can be provided for the output current of the current conveyor. To demonstrate the proposed circuit's easy applicability it was used in a CCCII-based oscillator. The circuits' theoretical analysis was carried out, and the simulation process was realized using a PSpice electronic circuit simulation program. Simulation results verify the theoretical considerations.

2. Current controlled conveyor

A conventional current controlled conveyor is given in Fig. 1. Port characteristics of the current controlled conveyor are given in (1) /14/.

$$\begin{pmatrix} I_y \\ V_y \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & 1 & 0 \end{pmatrix} \cdot \begin{pmatrix} V_x \\ I_x \\ V_z \end{pmatrix} \quad (1)$$

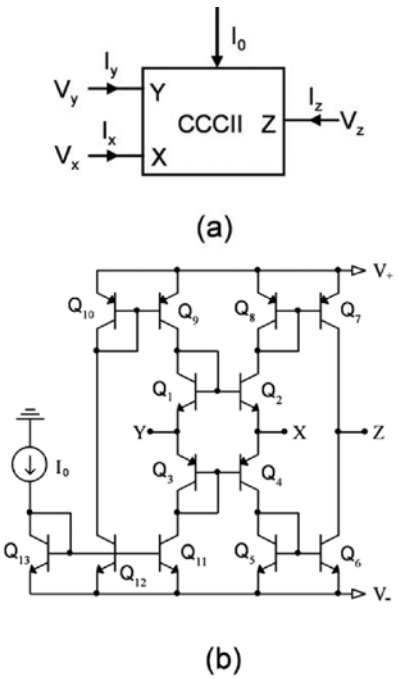

Fig. 1. Conventional CCCII; (a) Symbol, (b) Circuit diagram

When port *Y* of the CCCII is grounded and port *X* constitutes the input of the circuit (Fig. 1), the input current is then given by

$$I_X = 2I_0.\sinh(V_x/V_T) \quad (2)$$

In CCCII based circuits, realization methods take advantage of the parasitic resistance R_x that appears at port X of the conveyor. Hence, the resistance R_x, which can be varied by means of an external bias current. From (2), if $V_x << V_T$ is assumed, then the function sinh (V_x/V_T) is approximately equal to V_x/V_T. The expression for this equivalent resistance is

$$R_x = \frac{V_x}{I_x} = \frac{V_T}{2I_0} \quad (3)$$

where V_T is the thermal voltage given by kT/q and I_0 is an external bias current /9/. This means that the characteristic of the current conveyor based circuits will depend strongly on temperature. Therefore, some form of temperature compensation is required. The relation between ports *X* and *Y* can be modeled as shown in Fig. 2.

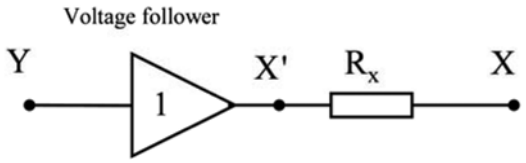

Fig. 2. Equivalent circuit between ports Y and X

3. Proposed circuit topology

Fig. 3 shows symbol and schematic diagram for the proposed temperature compensated current controlled conveyor (TC-CCCII).

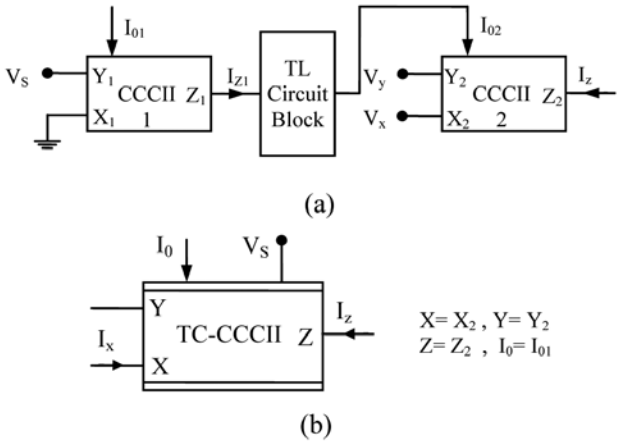

Fig. 3. Proposed TC-CCCII; (a) Schematic diagram, (b) Symbol

The temperature compensated current controlled conveyor was designed using two current conveyors and a translinear (TL) circuit block based on translinear principle.

Currents I_{01}, and I_{02} denote bias currents for the first and second current conveyors, respectively, and V_S is an external voltage. Fig. 4 shows the circuit structure of the TC-CCCII.

When port *X* of the first CCCII (X_1) is grounded and port *Y* of the first current conveyor (Y_1) constitutes the input of the proposed circuit, the output current of the first current conveyor (I_{Z1}), which is equal to current that exists at port *X* of the first current conveyor, can be expressed as

$$I_{Z1} = 2I_{01}\frac{V_S}{V_T} \quad (4)$$

It is shown that output current I_{Z1} of the first current conveyor depends on the voltage V_S applied to port Y_1 and the bias current of the first current conveyor (I_{01}) in (4).

A translinear circuit is used as a current divider circuit to generate bias current for CCCII. This circuit is almost temperature-independent. This circuit is presented in Fig. 5.

The relations among the currents in this circuit are given in (5).

$$I_{02} = \frac{I_1 I_2}{I_{Z1}} \tag{5}$$

where I_{02} is the bias current of the second current conveyor aiming at providing temperature compensation. As shown in Fig. 4, I_1 and I_2 are the collector currents of the Q_B and Q_C transistors respectively. The current of the second current conveyor's port *X* can be expressed as

$$I_x = 2I_{02}\frac{V_x}{V_T} \tag{6}$$

In this case, the current of the second current conveyor's port *X* will be

$$I_x = \frac{I_1 I_2 V_x}{I_{01} V_S} \tag{7}$$

Current mirrors which are obtained by Q_{10}, Q_{12} and Q_B, Q_C transistors allow the biasing current (I_{01}) to flow through the Q_{13} transistor at the collector of the Q_B and Q_C transistors. So I_1 and I_2 currents are equal to current I_{01}. From (7), we can see that the parasitic resistance of the second current conveyor can be expressed as,

$$R_x = \frac{V_S}{I_{01}} \tag{8}$$

The parasitic resistance R_x input current I_x and output current I_z of the whole circuit can be independent from V_T by adjusting the suitable configuration of the circuit blocks.

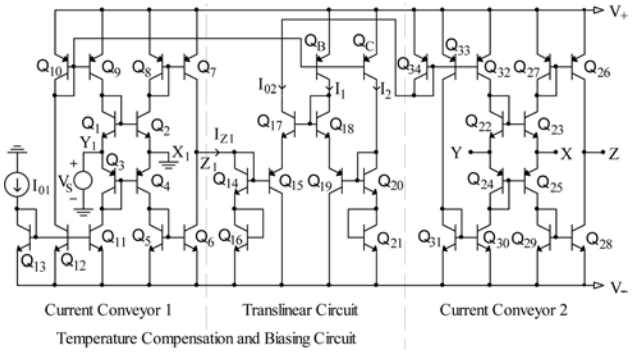

Fig. 4. Realization of the TC-CCCII circuit

4. Simulation results

To verify the validity of the theory, the circuits in Fig. 1 and Fig. 4 were simulated using models for the transistors of type NR100N and PR100N whose parameters are detailed in /15/. The biasing current I_0 = 85 μA , that is, R_x=150 Ω was used for the conventional current conveyor. The circuit parameters were chosen as I_{01}=100 μA and V_S = 15 mV for the temperature compensated current conveyor, and the power supply was ± 2.5 V.

First, a simulation of the conventional current conveyor shown in Fig.1 was realized using a PSpice simulation program. Port Y of the CCCII is grounded and port X constituted the input of the circuit. The I-V characteristic at port X for different temperature values are shown in Fig. 6.

From (1), I_Z is equal to I_X. Thus, from Fig. 6 it is concluded that I_Z is affected by temperature change.

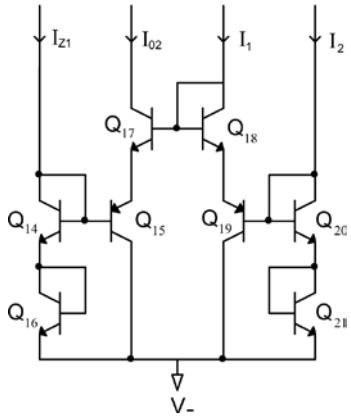

Fig. 5. Translinear circuit

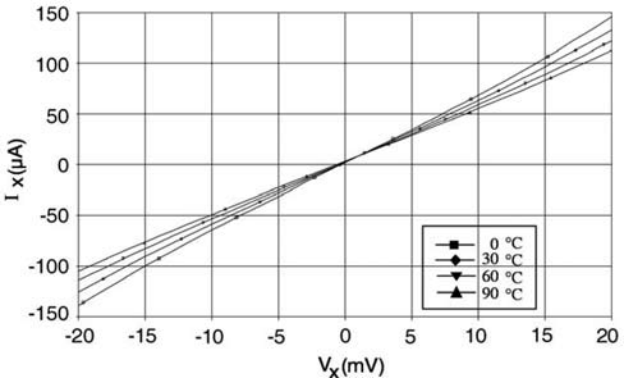

Fig. 6. Current-voltage characteristics of the CCCII without temperature compensation

Next, a simulation of the temperature compensated current conveyor was realized using a PSpice simulation program. Port Y of the second CCCII was grounded and port X of the second CCCII constituted the input of the circuit. The I-V characteristic at port X for different temperature values are shown in Fig. 7.

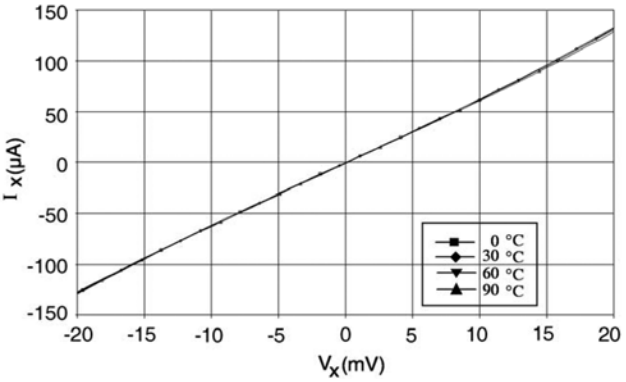

Fig. 7. Current-voltage characteristics of the TC-CCCII

In Fig. 7, it is clear that the output current for different temperature values changes in regard to nanoampers. These values are almost negligible. In addition, when Fig. 7 is taken into consideration, it does not show a characteristic deviation in the origin, on the contrary in Fig. 6. Characteristic deviation in the origin is caused by a mismatch

between the transistors. This situation clearly denotes that the proposed circuit is more stable.

Fig. 8 depicts changing output current versus temperature for both the conventional and the temperature compensated CCCII's output current.

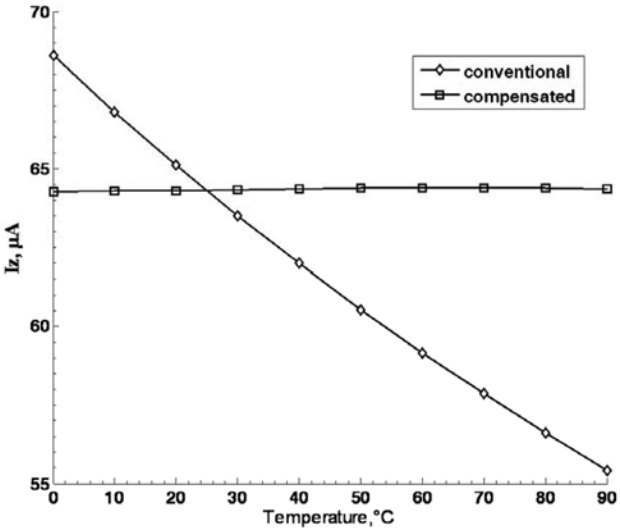

Fig. 8. Variation of the output currents versus temperature for CCCIIs

When the current curve of the conventional CCCII in Fig. 8 is considered, it can be seen that the characteristic is not exactly linear. This result is an obvious consequence of the hyperbolic function in (2). In previous studies /14/, this hyperbolic function was approximately linearized. Thus, the characteristic of CCCII output was obtained in linear form.

5. Current controlled oscillator based on cccii

The oscillator was designed using a current amplifier (current mirror) and two TC-CCCIIs as shown in Fig. 9.

The current loop gain or the return ratio *T(s)* of the circuit at port *X* is characterised by

$$T(s) = \frac{\alpha R_x C_1 S}{1 + 2R_x C_2 S + 2R_x C_1 C_2 S^2} \quad (9)$$

CCCII has a finite input resistance R_X at the X terminal, which is controllable by the bias current I_0 /16/. R_x is considerably affected by temperature. Sinusoidal oscillation frequency is shown in the following equation

$$f_0 = \frac{1}{2\pi R_x \sqrt{C_1 C_2}} \quad (10)$$

where the oscillation condition is α = 2 /16/. Oscillation frequency can be tuned by varying the R_x. The current mirror in Fig. 9 is independent from temperature, so oscillation frequency is not affected under this condition. Table 1 depicts a theoretical changing R_X and oscillation frequency versus temperature for the conventional CCCII.

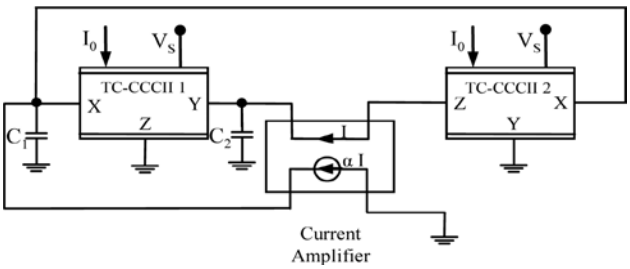

Fig. 9. Proposed current controlled oscillator schematic diagram

In Table 1, it is clear that R_x and oscillation frequency for different temperature values change. Biasing currents were chosen as I_0 = 250 µA for conventional CCCIIs.

Table 1. Theoretical changing R_X and oscillation frequency versus temperature for the conventional CCCII.

Temperature (°C)	R_X (Ω)	Frequency (KHz)
0	46.94	335.06
30	52.12	305.38
60	57.28	277.87
90	62.44	254.91

To demonstrate the applicability of the new temperature compensated CCCII, it was used in place of a conventional CCCII to realize temperature compensation in the current controlled oscillator.

To evaluate the performance of the circuit in Fig. 9, several PSpice simulations have been performed using the typical parameters of the bipolar transistor NR100N and PR100N whose parameters are detailed in /15/. A biasing current I_0 = 250 µA, that is, R_x = 50 Ω was used for the conventional current conveyor.

Circuit parameters were chosen as I_{01} = 75 µA and V_S = 15 mV for the temperature compensated current conveyor in Fig.4 and the power supply was ± 2.5 V. C_1 and C_2 were 0.01 µF for all simulations.

Simulation results are shown in Fig. 10, which displays current amplitude against frequency for a number of temperatures for the current controlled oscillator based on a conventional CCCII. This graph was obtained from an oscillator circuit using conventional CCCII.

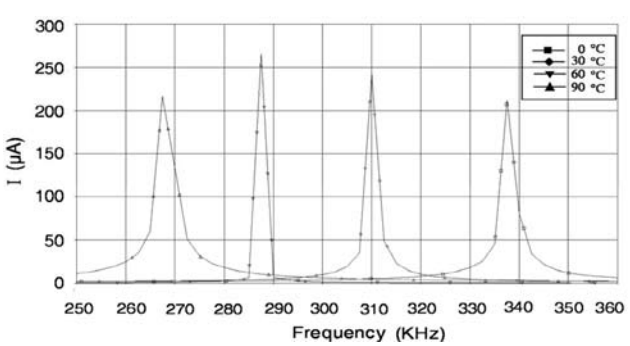

Fig. 10. Unstable oscillation frequency at different temperatures for oscillator based on conventional CCCII.

In Fig. 10, it is clear that, the oscillator's oscillation frequency is strongly affected by temperature change. The oscillation frequency of the circuit changes between 265 KHz – 340 KHz.

Fig. 11 shows stable oscillator frequency at different temperature values for the current controlled oscillator based on the temperature compensated CCCII. This graph was obtained from an oscillator circuit using the TC-CCCII.

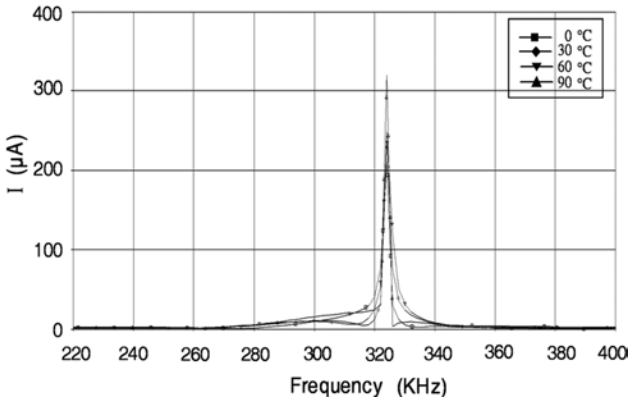

Fig. 11. Stable oscillation frequency at different temperatures for oscillator based on TC-CCCII.

It is clear that the temperature performance of the compensation circuit is much better than that of the conventional circuit. In addition, it can also be seen that the compensated circuit results in a much lower temperature sensitivity.

6. Conclusion

In this study, a temperature compensated circuit for conventional CCCIIs was designed, and its application to a current-mode oscillator was tested. The temperature sensitivity of the current controlled conveyor's parasitic resistance was reduced in this new design. The proposed circuit was simulated using a PSpice simulation program, and its simulation results were compared with the simulation results of a conventional CCCII. The compensated circuit was less temperature sensitive than conventional circuits. However, the proposed circuit was found to be suitable for implementing in integrated circuits due to its having no passive element. To demonstrate the applicability of the new temperature compensated CCCII, it was used in place of a conventional CCCII to realize temperature compensation in a current controlled oscillator. Finally, the proposed circuit which is controllable by biasing current was used as a part of many sensitive current-mode applications that especially require temperature compensation.

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SIMULATION OF TACTICAL NETWORKS USING SYSTEM-OF-THE-LOOP

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Key words: tactical network, simulation, system-in-the-loop, C2IS, real-time

Abstract: The successes of military missions strongly depend on quality planning. The need for near-real time simulation tools has become apparent, which allows the realistic network planning and training of command personnel on real Command and Control Information Systems (C2IS). Real hardware and C2IS software are, in these cases, connected to the simulator via a Local Area Network, where the tactical radio communication infrastructure is simulated on a virtual terrain. Such simulation of the network runs real-time with the simulated use of the C2IS. Operators of C2IS systems can simultaneously evaluate the qualities of tactical networks from the points of view of network throughput, end-to-end delays, radio visibility, etc., for each individual tactical unit. This paper presents some simple examples of using this new simulation methodology, which can be easy adapted to more complex C2IS scenarios.

Simulacija taktičnih omrežij z realnim sistemom v simulacijski zanki

Kjučne besede: taktična omrežja, simulacija, sistem v simulacijski zanki, C2IS, realni čas

Izvleček: Uspeh vojaških akcij je v veliki meri odvisen od kakovostnega planiranja le teh. V zadnjem času se je pojavila potreba po simulacijah taktičnih omrežij v realnem času, ki omogočajo realistično načrtovanje operacij in trening povelniškega osebja na realnem informacijskem sisemu poveljevanja in kontrole (C2IS). Za te namene se je razvil nov tip simulacij, ki omogoča povezavo realne strojne in programske opreme s simulacijskim orodjem. Simulacijsko orodje je namenjeno simulaciji virtualnega terena na katerega postavimo omrežje ter simulacijo povezav ali omrežij, preko katerih poteka komunikacija med realnimi napravami, ki jih priključimo na simulator. V članku predstavljamo simulacijo taktičnih omrežij z realnim sistemom v simulacijski zanki, ki je bila namensko razvita za Slovensko vojsko. V takšnem sistemu smo povezali realni informacijski sistem poveljevanja in kontrole (C2IS) s simuliranim taktičnim radijskim omrežjem na virtualnem terenu. V nadaljevanju smo predstavili različne ekperimente in simulacijske rezultate, kot je prenos digitalnega videa preko simulirane radijske povezave, ter rezultate simulacij v katere smo vključili realne naprave s programsko opremo informacijskega sistema poveljevanje in kontrole (C2IS) Slovenske vojske. S pomočjo takšnih simulacij lahko načrtovalci operacij ovrednotijo kakovost preiskušenih taktičnih omrežij na osnovi prepustnosti, radijske vidljivosti, zakasnitev, itd.

1. Introduction

Since joining NATO, Slovenia has had to face new challenges in terms of modernization and connectivity with other members. In 2001, the Multilateral Interoperability Programme (MIP) was established to advocate successful and harmonized operational functions for international peace-keeping forces /1/. Interoperability is achieved by C2IS (Command and Control Information Systems) at all military levels. C2IS is designed to control the operational, logistical and communication information stored in the C2IEDM (Command and Control Information Exchange Data Model) data bases. The success of this command and control system is highly correlated with the capacities of the data information carriers.

Most of the developed tools for tactical network simulations are "off-line" simulation tools, where we can analyze a tactical network after a simulation run. The most prominent problems in tactical networks are limited bandwidth, big round-trip delays, and the influence of terrain and nodes' mobility under radio link conditions /2/. Simulation of tactical networks is an important task in the process of military mission planning. Such methodologies assure a higher probability of success for critical tactical operations in military arenas. One of the early papers about tactical radio systems' simulation presented a solution /3/, where a specialized FORTRAN program was developed to simulate radio propagation effects, interference, SNR etc. The most often used simulation tool is the OPNET Modeler /4/ which is also used as a basic tool in our work. The results of tactical network simulations can be used when evaluating the performances of tactical communication networks /5/. Two-well known tools have been developed specifically for military tactical network simulations based on OPNET. The first tool is NETWARS /6, 7, 8/, which enables simulation of different tactical simulation scenarios by using diverse combinations of tactical network devices and military concepts. The second tool is INCOT, which represents an intelligent specialized tool for the optimization of communication networks /9-11/. In our case we have developed new simulation methodologies and tools for "off-line" analysis that enable C2 (Command and Control) communication systems' optimization /6-18/. We have de-

veloped the helper application TPGEN (Slovenian acronym for Tactical Information Traffic Generator), which enables user-friendly entering and editing of tactical network parameters to an OPNET simulation data model /15/. We have also developed an expert system application, which enables automatic analysis of OPNET simulation results /17/, and a tactical player visualization tool which combines MAK 3DNV (3D network visualization) simulation records with the results of expert system application /18/.

Over recent years the new concept of »on-line« tactical network simulation has also appeared where simulation is executed in "near-real" time. One of the earlier near- real-time simulators with a military application is the Battlespace communication network planner and simulator /19, 20/. This simulator is based on the OPNET simulation tool, where special communication hardware and software interfaces were developed that allow interconnection with actual command and control (C2) systems. In contrast to what we have described, we have also developed our real time simulator using OPNET with its System-in-the-loop (SITL) module which allows connections between real devices and the simulation. In this case, special communication devices are no longer needed. The SITL module provides packet translation between real and simulated packets /21/, where we show the basic concept of SITL simulations for simple voice application.

This paper presents a simple near real-time simulations example of tactical networks, where the real C2IS equipment of tactical units is connected through the simulator. The developed simulation system enables the testing and training of different tactical missions in a lab-environment, where the radio part of a wireless tactical network is simulated by an OPNET Modeler simulation tool. Within the simulated tactical communication infrastructure we can define radio parameters, position, trajectories of movement, etc., according to real radio equipment, and the mission plan. Radio wave propagation models based on virtual terrain modeling are used in simulation. During the simulation run, tactical planners and operators can analyze situations when a long delay appears, units have lost radio visibility, or lost the connection or data. Such a simulator enables early predictions of any possible problems that may appear during a real mission. In such a way, simulation tool can improve the probability of mission success, depending also on C2IS being dramatically improved. This new simulation methodology, presented in this paper, can be easy adapted to more complex C2IS scenarios, which is schematically shown in Figure 1. This figure shows schematic of connections between real tactical units, equipped with C2IS, and a simulator. External units are connected to the hub, which is connected to the physical interface (NIC) of the computer, where the simulator is installed. In the simulator the external connected units are represented as tactical wireless radio devices. On these modeled wireless stations, planners can set different parameters, such as channel frequency, bandwidth, antenna pattern, etc.

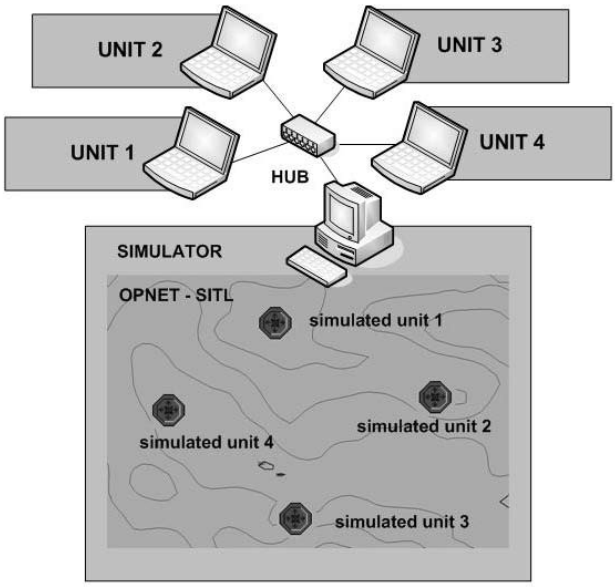

Fig. 1: LAN connections between real tactical units and the simulator, where the tactical radios of tactical units are modeled on virtual terrain.

This paper is organized as follows. The second section briefly describes the command and control information system (C2IS) used by the Slovenian Army. The third section describes advanced methods of OPNET Modeler for near-rear-time simulations. Two examples of near real-time simulations are presented in the fourth section. The first example presents the transmission of a video stream over the simulated wireless link. The second example presents the simulation, using real C2IS software. This section also presents the simulation results for both cases. This paper concludes with some guidelines for future work.

2. Command and control communication system in the slovenian army

Command and Control Information System (C2IS) (TISPINK is the Slovenian acronym) is designed to control the operational, logistical and communication information stored in the operation data bases (C2IEDM/JC3IEDM). The C2IS system provides information about operational developments, the state of your own, other friendly, and hostile units. This information is very important for modern international military operations and for the successes of many international operations. Figure 2 shows the main structure of the TISPINK unit. The core of the TISPINK system represents two main programs developed by a Danish company Systematic Software Engineering A/S /22/, in accordance with MIP recommendations. These programs are IRIS replication mechanism (IRM) and Sitaware. The IRM program /23/ is responsible for data exchange (replications) between the C2IS data bases of military subjects in accordance with so-called agreements. Agreements, which are set between the subjects, are comprised of the

addressee of the military unit, the collection of data to be shared, and of used communication protocol (peer-to-peer or broadcast). This replication mechanism enables flexible control and supervision over information exchange in tactical networks.

The Sitaware program packet /24/ is a graphic interface of the command and control system. It is used for the planning, checking and analyzing of tactical units' activities on the battlefield. It enables the operators or planners of the operations to ascertain information about the situations of individual units in the field, and share this information with other military units. Sitaware is distinguished by a powerful graphical interface which is supported by GIS (Geographical Information System). GIS in turn, supports various geographical map formats and has different user layers thus enabling the entering of different information about tactical conditions on the battlefield.

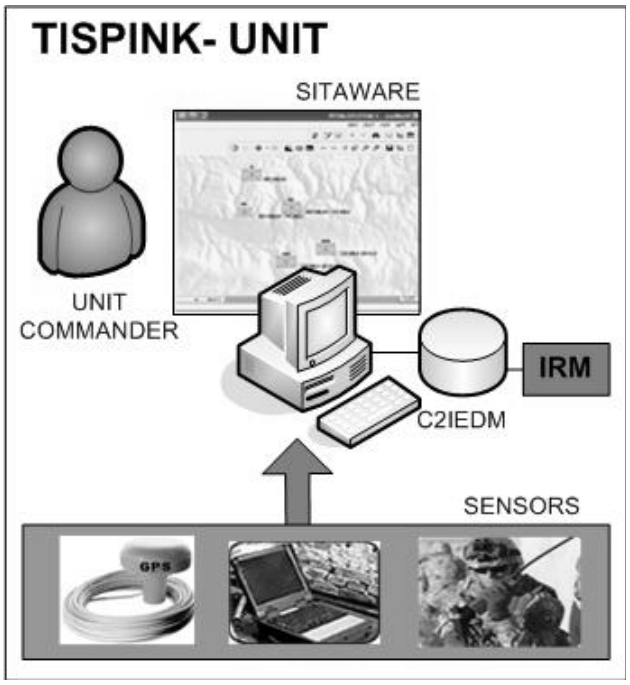

Fig. 2: TISPINK army unit

Figure 2 shows C2IS typical tactical unit. Each unit has its own C2IEDM data base, IRM replication mechanism and Sitaware. Various sensors can be connected to the tactical units, such as GPS. TISPINK units compose the hierarchical tactical network, as shown in Figure 3, where units can communicate by inferior and superior units based on defined IRM contracts, which are described in more details in /14/.

3. Advanced modules for tactical simulator in real time

3.1 OPNET Modeler

The developed tactical network simulation system for near real-time simulations is based on OPNET simulation tool /4, 6, 7, 8, 14/. We used the OPNET Modeler Wireless Suite for Defence, which supports high-fidelity protocols and equipment models with a scalable simulations environment capable of simulating wireless and also wired networks. It supports wireless simulations incorporating terrain influences in path-loss calculations with different propagations models, mobility, and 3D visualization.

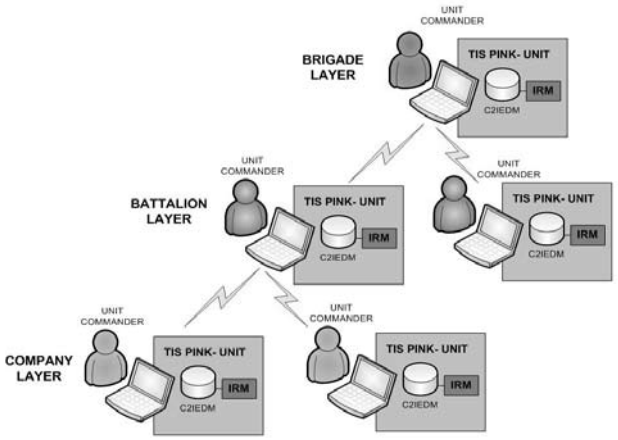

Fig. 3: Hierarchical structure of tactical network

OPNET Modeler is an object-oriented event driven communication simulation tool, with a hierarchical modeling environment, which uses graphic user interfaces (editors) – Network, Node and Processes editors. The *Network editor* enables a graphical description of network topology, while a *Node Editor* is used for describing communication device protocols and connections between them using layers of the ISO/OSI model. The *Process editor* is an upgrade of language C and uses a powerful finite state machine (FSM) approach to represent different communication algorithms and protocols. The OPNET Modeler is used for the modeling and simulation of communication networks and, at the same time, enables construction and study of communication infrastructure, individual devices, protocols, and applications.

3.2 System-in-the-loop module

System-in-the-loop (SITL) /4, 21, 33/ is an OPNET Modeler program module, which provides an interface between physical and simulated networks. It provides packet exchanges between real and simulated communication devices. SITL gateway represents an external device by which the simulation exchanges the packets, where the WinPcap /35/ library is used to route those packets selected by user defined filter, from an Ethernet network adaptor to the simulation process. In such a simulation manner, physical hardware and simulation can interact as a unified system. There are three main simulation topologies for using the SITL module /33/:

- real-to-real (communication between real devices over simulated network)
- sim-to-sim (communication between simulated devices over real network)

- sim-to-real (communication between real and simulated devices)

SITL module is used for near real-time simulations and can be used for many different purposes, such as: testing the effect of a simulated network on a real application, simulating the impact of network traffic amount to real network generating in simulation using a traffic generator, testing new prototypes of newly-developed devices and protocols, testing the performances of new protocols being developed by driving real network traffic over simulated traffic, etc. Simulated models running in the OPNET Modeler affect real applications and devices, providing various network effects, such as packet loss, delay, jitter, duplicate delivery, etc.

Using the module SITL we achieved packet exchanges using discrete event simulation via mapped interfaces. It also allows for multiple interfaces for mapping different network addresses in the simulated network. The SITL module directly routes packets from the network adapter to the simulation, and translates the entire packets, but the IP datagram stays unchanged in the regard to the rest of the simulation. Figure 4 shows the real-sim-real case of SITL simulation.

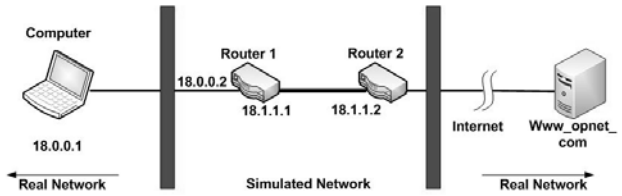

Fig. 4: Example of real-to-real type of SITL simulation, where real devices (client and server) communicate through a simulated network consists from routers.

In the OPNET Modeler 14.0 together with the SITL module support the following protocols /33/:

Ethernet

- IPv4 and IPv6 (except for fragmentation)
- Higher layer protocol conversion (real-sim-real, sim-real)
  - ICMP, ICMPv6
  - OSPFv2
  - RIPv1 and RIPv2
  - TCP, UDP
  - Limited FTP standard model application support
- Users can add support for their own protocols

When developing our own protocols, we wrote our own translation function (SITL translation function) to convert simulation packets to real packets, and vice versa. In the case of real-sim-real simulation, virtually all application-layer protocols are supported because, in this case, the simulation network is only used as a transit network for IPv4 or IPv6 packets.

3.3 3DNV

A 3D Network Visualizer (3DNV) /18, 21, 34/ is an additional OPNET Modeler module, which enables 3D animation simulated network topology, network devices, and link status. It can be used for visually demonstrating how terrain features, such as hills and mountains interfere with the wireless communication devices of mobile networks. Visual presentation can also be enhanced by network statistics, such as received packets, transmission quality, throughput, delay, message status information, etc. The communication devices used in the OPNET Modeler can be visualized in 3DNV by many different 3D objects, which are stored in a library of 3D models (cars, planes, ships, tanks, etc.). Figure 5 shows an example of communication unit visualization in 3DNV. 3DNV allows viewing animation of the whole network or just one or a few units, from any perspective. It also allows viewing animation of unit movement by predefined trajectories from different viewing angles at different altitudes. A set of 3D animation configuration objects used in animations are also included, as are lines between nodes which represent packets transmission, spheres to represent the transmitter's range, and numbers which represent the simulation results.

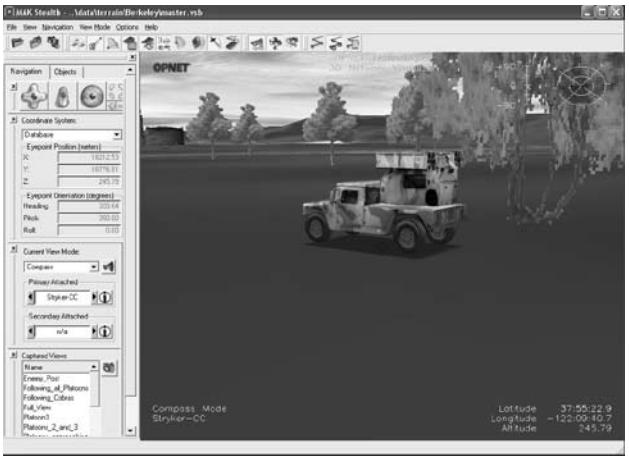

Fig. 5: An example of communication unit visualization by 3D Network Visualizer (3DNV)

3.4 Wireless package

The OPNET Modeler Wireless package is flexible and a scalable environment for the modeling and simulation of wireless networks /25, 26/. All the characteristics of wireless networks are integrated into lower layer protocols, which enables the modeling of all viewing points regarding wireless transmission, such as the spreading of RF electromagnetic waves /27/ by considering ground impact to the diffraction, fading, interferences, characteristics of the receiver and transmitter, nodes mobility, etc. OPNET allows efficient development of various wireless communication technologies such as MANET, 802.11, 3G/4G, Ultra Wide Band, WiMAX, Bluetooth, Satellite links /25, 26, 28/. In OPNET, wireless package wireless links between transmitter and receiver are simulated by using an open-concept called a transceiver pipeline. The transceiver pipeline

enables delay computations during the spreading of radio waves, closing radio links, consideration of an aerial's emissive diagram, background noise, modulation effects, interference, bit-error rate, forward error corrections, etc.

3.5 Terrain modeling module (TMM)

The Terrain Modeling Module (TMM) is a special OPNET module which enables improvement in the accuracy of the wireless network simulations, by taking into account signal loss due to terrain effects. They include the impact of natural barriers on simulations (mountains and the earth's curvature) and the physical characteristics of the environment (conduction, permeability, surface refractivity) spreading of radio waves. TMM supports various propagation models:

A free space propagation model /29/ using the theory of spreading electromagnetic waves in an ideal vacuum. This model does not use terrain effects or any other physical limitations.

Longley-Rice model /30, 31/, also known as Irregular Terrain Model (ITM), is a more accurate propagation model of radio waves spread, as a model of optical visibility (LOS). It is used within frequencies ranging between 20 MHz and 20 GHz. It was originally developed for television transmission in 1960's.

The TIREM model /32/ is the most detailed, with the fewest limitations. It is used within a frequency range between 1 MHz and 40 GHz. It also includes effects such as multiple diffraction on edges and barriers, reflections from the troposphere, absorption in atmosphere, surface guiding of waves because of ground conductance, troposphere dispersing, long-term fading etc. It is one of the best choices for use in models of non urban terrain.

Virtual terrain is modeled by using DTED (Digital Terrain Elevation Data) and USGS (U.S. Geological Survey) DEM (Digital Elevation Model) maps. Figure 6 shows a terrain profile between the transmitter and receiver, and an estimation of the received power for different propagation models.

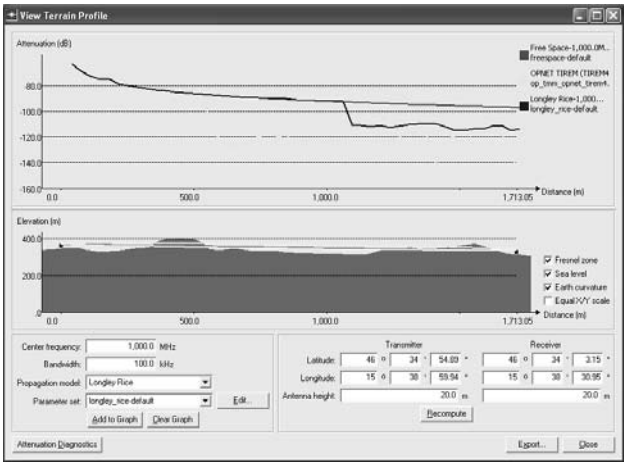

Fig. 6: Terrain profile with calculation of radio signal power between transmitter and receiver by using different propagation models.

4. Tispink system simulation in real time

We used the real-sim-real type of SITL simulation, where real C2IS equipment communicates through a simulated wireless environment. Figure 1 shows the basic connections between tactical units and the simulator. This is more detailed in Figure 7 which shows configuration of our test simulation scenario. Here, two real TISPINK tactical units are connected to the hub. On each of these TISPINK units we define IP addresses, gateway, disabled firewall, etc. The hub is also connected to the physical interface (NIC) of the computer, where OPNET simulation tool is installed. On this computer we must also set IP addresses, gateways, disabled firewall, etc. It is important that each of tactical the unit is from a different subnet. In other cases they will communicate directly across the hub and not to over the OPNET simulator.

In the simulation environment we modeled the tactical radio equipment on virtual terrain, as shown in Figure 7, where tactical radios are labeled as simulated units (Unit 1 and Unit 2). Externally connected real tactical equipment serve as traffic sources and sinks. Modified real packets of TISPINK application run through simulation, where the SITL gateway translates real packets to simulation packets, and vice versa.

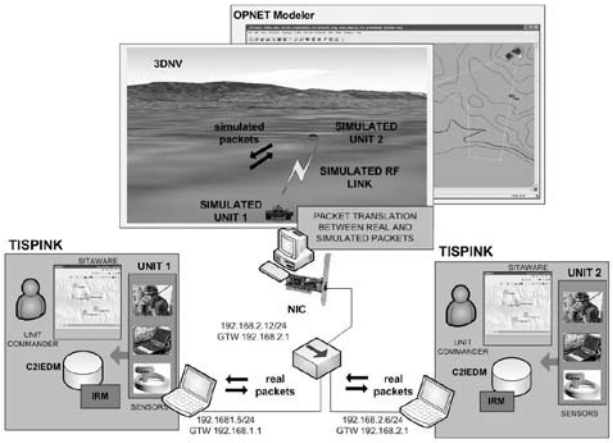

Fig. 7: Topology of test network for data transmission between real Unit 1 and Unit 2 over simulated wireless link.

In the OPNET Modeler, we created a model of tactical radio for the purpose of simulations in near real-time, as shown in Figure 8. It consists of three devices: SITL gateway (node_2), SITL link, and wireless router as tactical radio model (node_1). SITL gateway translates packets between simulated and real communication equipment. Using its attributes, it can configure a filter that defines which packets from which network interface card will be imported or exported via the SITL gateway. Using the wireless router we can define the tactical radio's attributes such as the transmitter's power, receiver's sensitivity, channel frequency, types of modulations, types of antenna, etc.

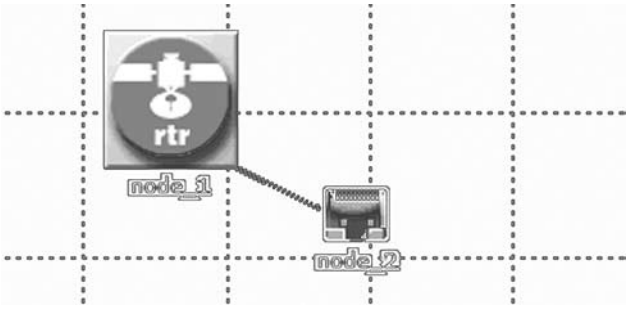

Fig. 8: Model of tactical radio device for SITL simulations: connection between SITL gateway and wireless router with SITL link

4.1 Video over simulated wireless link

In this example, of near real-time simulation, we show the transmission of video stream over the simulated wireless link. Figure 7 illustrates the topology we used in our experiments with the exception that we did not use any special C2IS on the tactical unit stations. The simulation scenario on the OPNET Modeler's side is shown in Figure 9, where the radio equipment of Units 1 and 2 are located at certain positions on the virtual terrain. Unit 1 (video stream receiver) represents the fixed node. Unit 2 (video stream transmitter) is the mobile unit, which moves by a predefined trajectory, as shown in Figure 9.

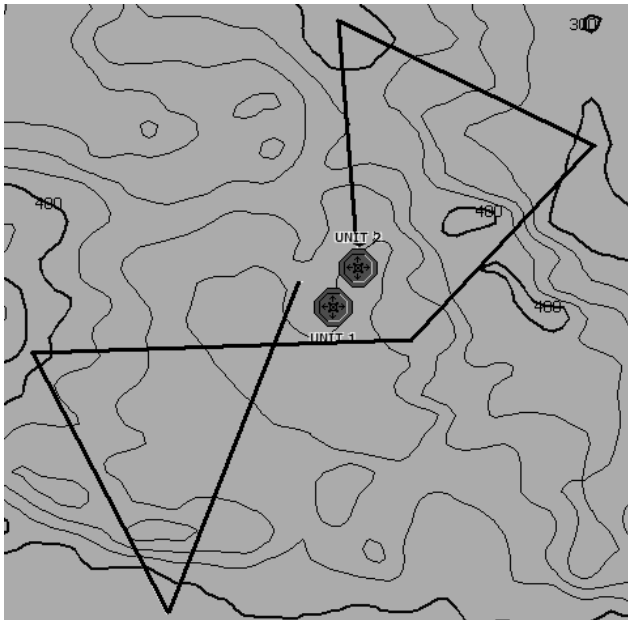

Fig. 9: Simulation scenario in OPNET Modeler, where tactical units are located at certain position on the virtual terrain. Unit 1 presents the fixed tactical unit, Unit 2 presents the mobile tactical units, which moves during the simulation run along a predefined trajectory.

The speed of unit movement is 60km/h. The radio equipment of both units act as wireless 802.11g devices with channel capacity of 54Mbps. Virtual terrain is defined by using a DTED Level 2 elevation map with 30m resolution. For a propagation model we chose TIREM. With these requirements we can ensure the best possible realistic transmission of live video stream over simulated wireless link. We used the well known VLC media player - the cross-platform media player and streaming server as video streaming equipment. It can be used for unicast or multicast streaming in IPv4 or IPv6 high-bandwidth networks for various audio and video formats (MPEG-1, MPEG-2, MPEG-4, DivX, mp3, etc.). Both tactical computer workstations are connected to the Ethernet network interface card (NIC) of simulation computer over hub (Figure 7). Such a kind of connection is possible in the case, where the external computers (Unit1 and Unit 2) have network IP addresses from different subnets; otherwise, communication between them would go directly over the hub and not over the simulation process. Multiple network interface cards are needed (one NIC for each external computer) to support such configurations, where both external computers have IP addresses from the same subnet.

During a near real-time simulation run, we can observe video signal on the real transmitter and receiver. For video source at the transmitter side, we chose the AVI movie. Real packets of a test movie video stream were transmitted through the simulated wireless link, which is affected by simulated conditions such as distances, radio visibility, etc. During simulation runs we could see that, over some time intervals, we lost some packets and errors appeared in received video signal. Sometimes the receiver lost the video signal for several seconds or for even longer periods up to 60 seconds. In these cases there was no radio visibility between receiver and transmitter. Figure 10 shows the examples of the captured video frames from transmitter (left) and receiver side (right) under various link conditions.

Fig. 10: Captured video stream on the transmitter (left side) and receiver (right side) for two cases. In the first case (upper figures) without packets lost and in the second case (lower figures) distortions appears on receiver caused by lost packets.

The graphs in Figure 11 represent the traffic of the transmitted video stream from Unit 2 (first graph) and received video

stream from Unit 1 (second graph). On the second graph parts without received traffic and some additional peaks are noticeable some, which represent packets' repetitions in the conditions of the transmission errors on radio's visibility borders. Figure 12 shows the received power (first graph) and bit-error rate - BER (second graph) for the receiver (Unit 1). In those cases, where the receiver power is lower than the threshold (sensitivity), the receiver is unable to detect incoming traffic. On the radio visibility boundary, the S/N ratio increases what is visible through increasing BER. In those intervals, where radio visibility between receiver and transmitter is established, BER is almost equal to 0. In the intervals where radio visibility was almost lost, BER strongly increased. At these intervals the packet-rate of the received traffic is also increased, caused by packet repetitions, as can be seen on the second graph in Figure 11. BER was not calculated for intervals without radio visibility

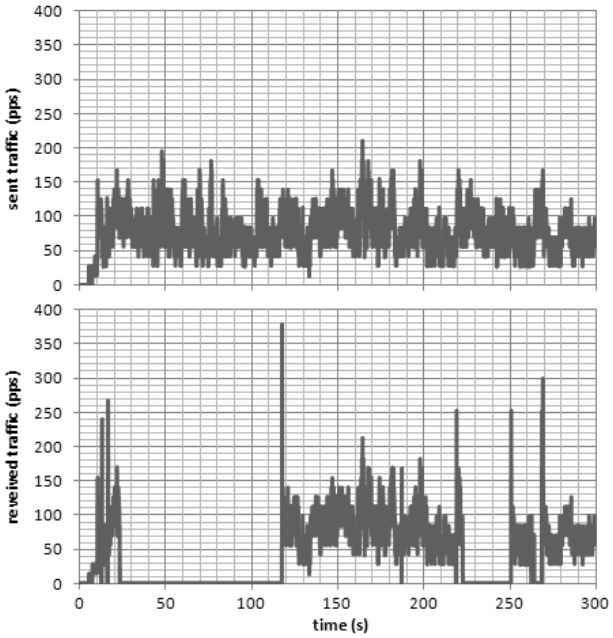

Fig. 11: Comparison between sent traffic from Unit 2 (video transmitter) and received traffic by Unit 1 (video receiver).

4.2 Tispink system simulation in near real-time

In the second example, we used TISPINK applications (Sitaware and IRM replication mechanism) installed for tactical units Unit 1 and Unit 2, instead of video streaming application. Unit 1 is the role of the Battalion and Unit 2 represents the Brigade. Using the IRM user interface shown in Figure 13, we defined ''peer-to-peer'' contract between units Unit1 and Unit 2. Traffic between these units was caused manually by sending and requesting management or the operational bulks of the IRM replication mechanism. In this simulation case we used the same topology (shown in Figure 8), as in the first example. We also used the same virtual terrain, the same predefined trajectory from Figure 9, and the same tactical radio parameters.

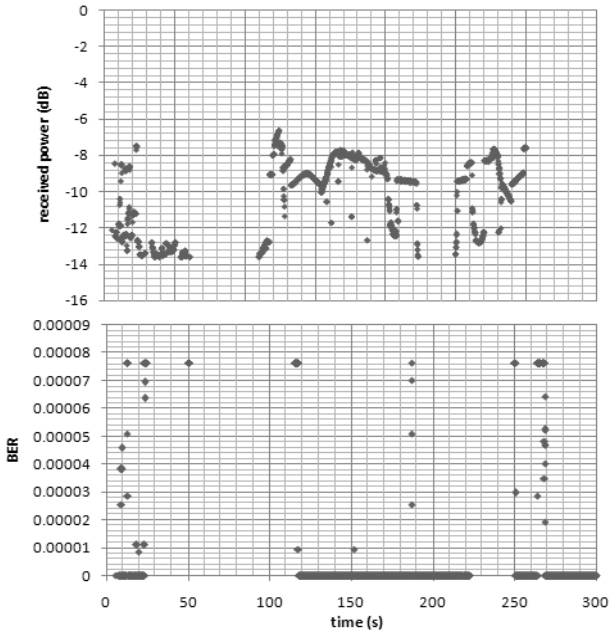

Fig. 12: First graph represents received power and bit-error rate (BER) on receiver side (Unit 1).

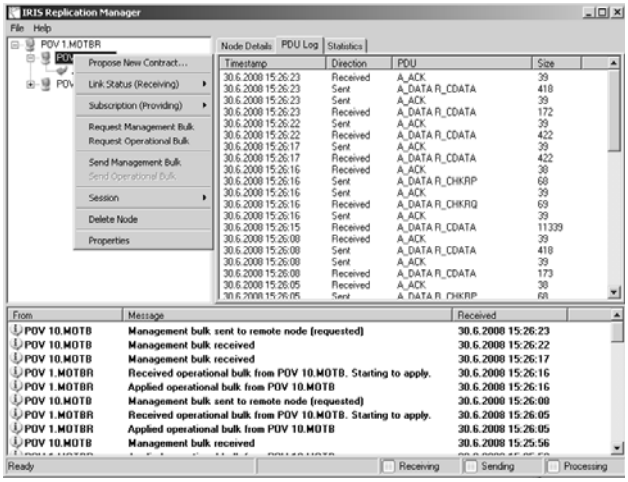

Fig. 13: IRM application user interface at Battalion unit, where we sent and requested operational and management bulk during near-real time simulation.

We created two different scenarios for the OPNET simulation tool. In the first scenario the Battalion and Brigade units (Unit1 and Unit2) are stationary and between them is all the time-assured radio visibility. In the second scenario, Unit 1 is mobile along a defined trajectory and Unit 2 is stationary (Figure 9). In both scenarios, the network traffic is generated by sending and requesting operational and management bulks. In the first scenario, where radio visibility is assured, there are no communication problems during the replication process. From the simulation results (in Figure 14), we can see, that radio visibility between units in the first scenario is possible during all simulation runs. The receiver power at the Brigade tactical unit is almost the same (with some exceptions) during all simulation, and is above the receiver's threshold.

In the second scenario, we repeated simulation when the Brigade was moving along a predefined trajectory (as in Figure 9). For the Battalion we sent and requested operational and management bulk, but at some intervals there are no response from the Brigade unit when connection was lost. In these cases, we cannot successful send management or operational bulks. At the moment when connection has been reestablished, replications of all data changes were accomplish during lost connection. In these cases a large amount of replication traffic appears. This is visible in Figure 15, which shows the sent traffic from the Battalion unit and received traffic of the Brigade unit, where there are some intervals within the range between 50 and 150 seconds, where radio visibility between units is unavailable.

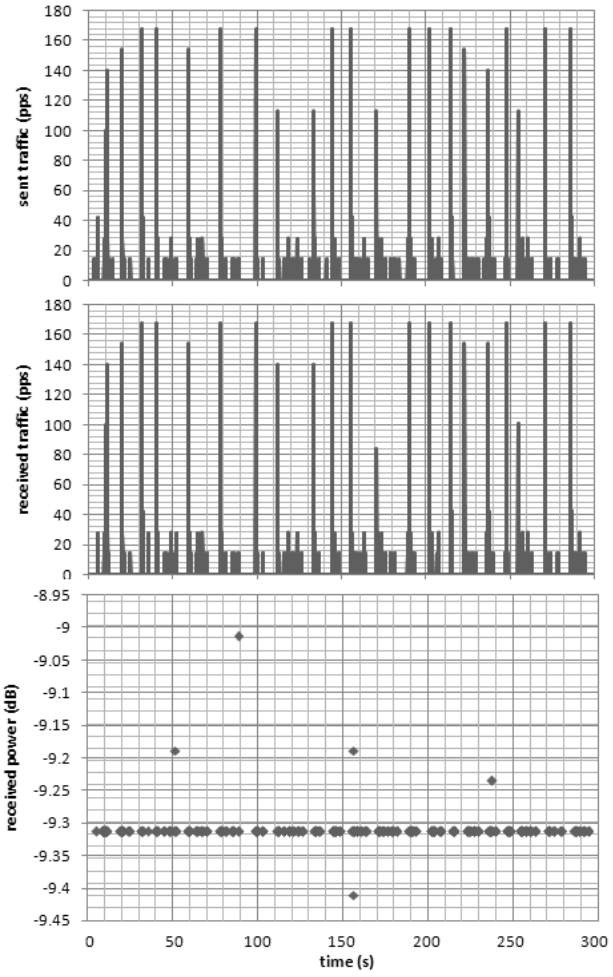

Fig. 14: The first graph shows sent traffic of the Battalion tactical unit, the second graph shows received network traffic by the Brigade tactical unit and the third graph shows the received power of the Brigade unit. The threshold of the receiver is -12.5dB.

Graphs in Figure 16 shows the estimated values for received power and signal-to-noise ratio (SNR) of the Brigade unit, which can only be estimated in cases where connections between units are established. Figure 17 illustrates an example of the 3D Network Visualizer (3DNV) representation of the tactical network.

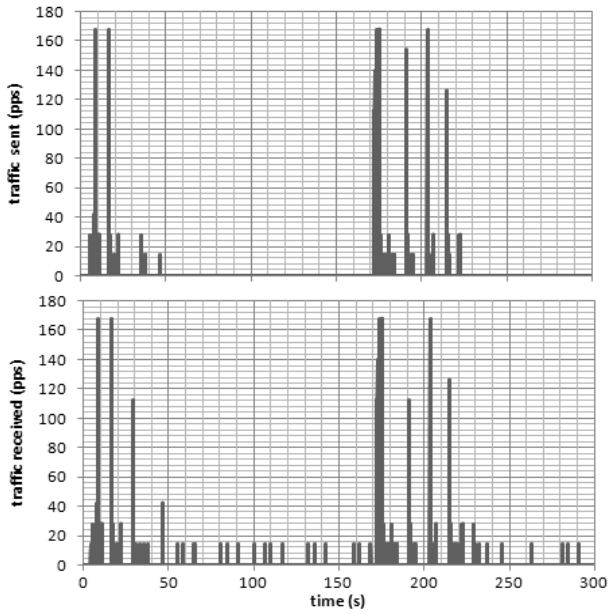

Fig. 15: The first and second graphs show the sent and received network traffic between tactical Unit 1 and Unit 2 for the second scenario.

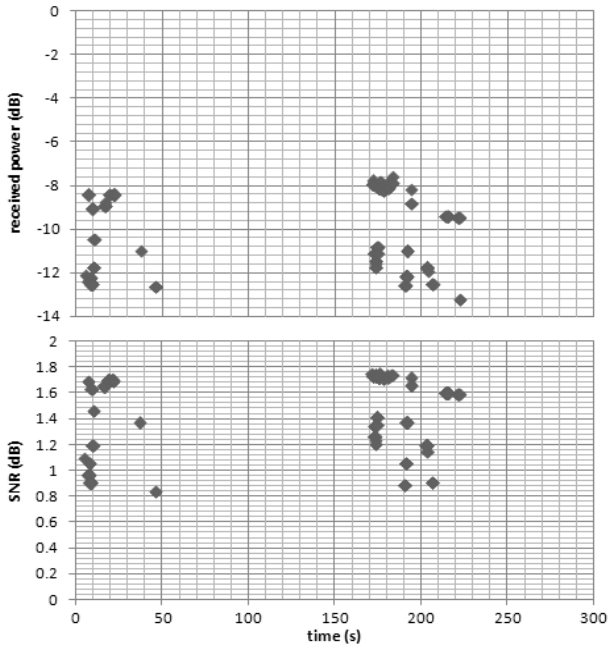

Fig. 16: Received power and signal-to-noise (SNR) parameter for the Brigade.

Conclusions

This paper presents the development of near-real time simulation methodology, where real tactical units can communicate with each other over simulated wireless links. This methodology enables training and planning for tactical missions in laboratory environments. Such a simulator allows the testing of different action scenarios on virtual terrain and to evaluate tactical networks in the sense of network delay, congestion, data lost, etc. We show two different examples of real-time simulations. In the first scenario

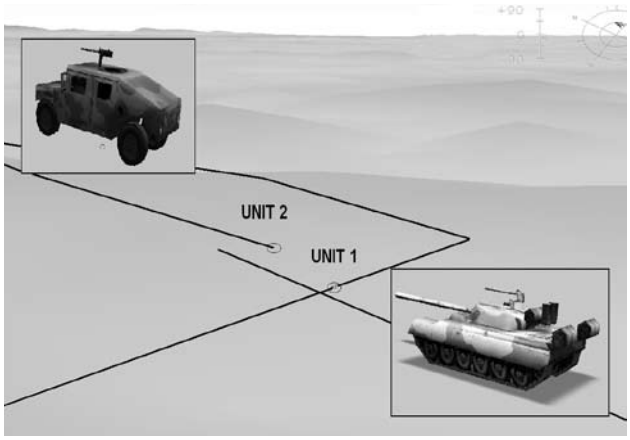

Fig. 17: Tactical network in 3DNV, where Unit 1 (Battalion) is represented as a tactical vehicle, Unit 2 (Brigade) with predefined trajectory on virtual terrain is presented as a combat tank.

we simulate the transmission of real video streams over a simulated wireless link. This is a typical broadcast application. In the second scenario we did simulation, where army units with C2IS applications were connected to the near-real time simulator.

A near-real time simulation of tactical networks is a novelty in the area of tactical network simulations. Such simulations help to predict how tactical networks will act on real terrain in real tactical situations. We can see, what happens if tactical units move on virtual terrain and lose radio contact. For such cases we can observe real application responses on real devices in the sense of traffic delay, losing connections, utilization, etc. Such kinds of results offer substantial help to the tactical mission planners and operators when evaluating tactical networks in real circumstances. This also allows operators and planners to optimally plan tactical missions in such a way, that as much as possible consider simulation results. It is also used for testing the effectiveness of different network topologies and protocol type's, such as peer-to-peer or broadcast. It can also be used for optimizing the amount of traffic between units defined by IRM contracts. Such kinds of simulations are also very important and suitable for the evaluation of new radio equipment before real purchase. It is also possible to evaluate communication parameters such as the necessary bandwidth of radio devices, power levels, antenna gains, etc. We can also carry-out tests with new C2IS software without the need for real tactical radio communication infrastructure. We also show, using two different application examples (video streaming and C2IS), that the presented simulation methodology does not depend upon the application type.

In future research, we would try to fully support this near-real time simulator for the Slovenian Army's needs. One very big problem appeared for the case when tactical units communicate with each other in a broadcasting manner, because the current version of SITL does not support wireless bridge to bridge communication functionality, which is needed in this case. Another important goal is also the reading of certain information (units' positions for example) from units' C2IEDM database and importing that information to the simulator in the real time. For all the presented reasons, we can expect a wider use of such simulators and applications in the near future, which will help in the optimization of networks and in the development of devices and protocols in all fields of communications.

Acknowledgment

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COMPACT UWB PLANAR ANTENNA FOR BROADBAND APPLICATIONS

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Key words: Broadband, Planar antenna, ultrawideband (UWB) antenna, partial ground plane.

Abstract: In this paper, a planar antenna for broadband applications has been proposed. The antenna consists of a rectangular patch, a partial ground plane and a slot on the ground plane. The proposed antenna is easy to be integrated with microwave circuitry for low manufacturing cost. The flat type antenna has a compact structure and the total size is 14.75 ×14.5mm^2. The result shows that the impedance bandwidth (VSWR ≤ 2) of the proposed antenna is 12.87 GHz (3.02 to 15.89 GHz), which is equivalent to 136.12%. Details of the proposed compact planar UWB antenna design is presented and discussed.

Kompaktna UWB planarna antena za širokopasovne aplikacije

Kjučne besede: Širokopasoven, planarna antena, ultra široko pasovna (UWB)antena, delna ozemljitvena ploskev

Izvleček: V članku predstavimo planarno anteno za širokopasovne aplikacije. Antena je sestavljena iz pravokotne zaplate, ozemljitvene ploskve in reže v ozemljitveni ploskvi. Antena z lahkoto integriramo v mikrovalovna vezja, s čimer dosežemo nizke proizvodne stroške. Ploskovna antena ima kompaktno strukturo in je velika 14.75 ×14.5mm^2. Rezultati nam pokažejo, da je impedančna pasovna širina (VSWR ≤ 2) antene 12.87 GHz (3.02 do 15.89 GHz), kar je enako 136.12 %. V članku predstavimo podrobnosti izvedbe kompaktne UWB antene in rezultate.

1. Introduction

Ultra-wideband (UWB) communication systems draw great attention in the wireless world because of their advantages, like high speed data rate, extremely low spectral power density, precision, high precision ranging, low complexity and low cost since the Federal Communications Commission(FCC) allowed 3.1 to 10.6 GHz unlicensed band for UWB communication/1/. UWB also have wide applications in short range and high speed wireless systems, such as ground penetrating radars, medical imaging system, high data rate wireless local area networks (WLAN), communication systems for military and short pulse radars for automotive even or robotics. The antenna is one of the crucial components which determine the performance of UWB system. The UWB antennas proposed in the open literature mainly focus on the slot and monopole antenna /2-5/. Printed wide slot antennas have an attractive property of providing a wide operating bandwidth, especially for those having a modified tuning stub, such as the fork-like stub /6/–/8/, the rectangular stub /9/, and the circular stub /10/ inside the wide slot. Broadband planar monopole antennas have received considerable attention owing to their attractive merits, such as ultrawide frequency band, good radiation properties, simple structure and ease of fabrication. The typical shapes of these antennas are half-disc /11/, circle, ellipse /12/, and rectangle /13/.

One of the popular UWB antenna types requires a perpendicular ground plane, which resulted in increased antenna size and difficult to integration with microwave-integrated circuits. Compared with the three dimensional type of antenna, flat type UWB antenna printed onto a piece of printed circuit board (PCB) is a good option for many applications because it can be easily embedded into wireless devices or integrated with other microwave-integrated circuits. However, the antenna design for broadband applications faces many challenges.

A low profile and embeddable unidirectional antenna is required for certain UWB communication, imaging, localization, and radar applications. The lower and upper UWB spectrums are 3.1–4.8 GHz (43%) and 6.0–10.6 GHz (55%), respectively. The existing broadband directional antennas, such as the Vivaldi, log-periodic, cavity-backed, waveguide, horn, and dish antennas, cover the entire 3.1–10.6 GHz band (109%). However, they are electrically large, and have a high profile in the direction of wave propagation. Omni- and bi-directional antennas, such as

the planar monopoles /14/, /15/, disc cone /16/, and slot antennas /17/, have a low gain and back radiation pattern, therefore they are not suitable for sectorial or unidirectional communication. Also, it is a challenge to maintain a stable radiation pattern across the whole frequency band, since the radiation aperture is frequency dependent.

In this paper, a microstrip-fed antenna for the broadband applications that achieves a physically compact planar profile, sufficient impedance bandwidth and highly stable bi-directional radiation pattern is proposed. The planar antenna consists of a rectangular shaped radiating patch and partial ground plane with a rectangular slot on the upper edge to cause a broad bandwidth from 3 to 16.0 GHz frequency. The antenna structure is flat, and its design is simple and straightforward.

2. Antenna Geometry and Design

Antenna is the key element in UWB systems. The motivation of UWB antenna design is to design a small and simple antenna that introduces low distortions with large bandwidth. Fig. 1 illustrated the configuration of the proposed antenna, which consist of a squarer patch, a partial ground plane and a single rectangular slot on the ground plane. The antenna, which has a compact dimension of 14.75×14.5mm^2, is printed in the front of a FR4 PCB substrate of thickness 1.6 mm and relative permittivity 4.6. The dimension of partial ground plane which is printed in the back side of the substrate is chosen to be 30×7.5mm^2 in this study. The dimension of the slot is 6.0×0.9mm^2 and 3.5mm away from the left edge of the ground plane. The bottom of the patch is connected by a microstrip line, which is fed by a 50 Ω coaxial probe from the side of the antenna. The microstrip line was etched on the same side of the substrate as the radiator. The antenna has the following parameters: L_{sub} = 22mm, W_{sub} = 30mm, L_P =14.75mm, W_P = 14.5mm, L_G = 7.5mm, l_f = 7.25mm, W_f = 4mm, W_e = 3.5mm, w_s = 6.0mm and l_s = 0.9mm.

Three techniques: the use of (i) square radiating patch, (ii) a partial ground plane and (iii) a single slot on the ground plane applied to the proposed design, lead to a good impedance matching. The geometric parameters of this structure can be adjusted to tune the return loss and bandwidth over wide range of frequency.

3. Results

The performance of the proposed antenna has been analyzed and optimized by using commercially available method of moments based full-wave electromagnetic simulator IE3D/18/. The simulated return loss of the proposed antenna is depicted in fig.2.

The plot of the return loss shows that the impedance bandwidth of the proposed antenna is 12.87 GHz (from 3.02 GHz to 15.89 GHz) which is equivalent

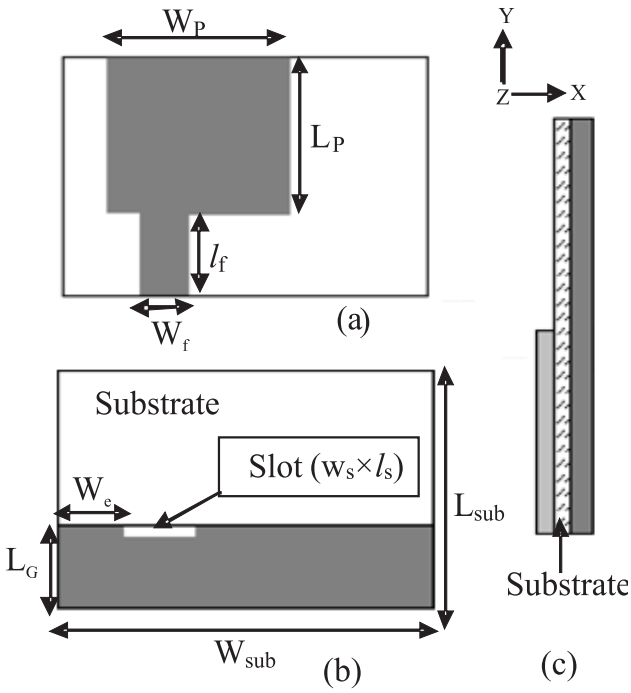

Fig. 1. Geometry of the proposed UWB antenna (a) front view (b) back view(c) side view.

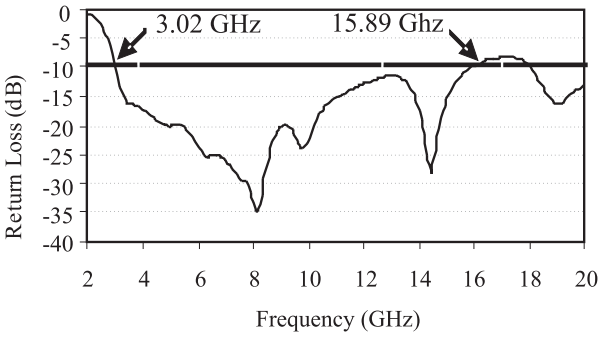

Fig.2. Return loss of the proposed antenna

to 136.12 %. Its covers the entire UWB frequencies mentioned earlier.

Fig. 3 shows the antenna gain in a frequency range of 3-10 GHz. The maximum gain is 1.60 dBi with an average of 0.52dBi, which can meet the usual requirement of -4 dBi for broadband applications. The gain is affected by the size of the ground plane.

The radiation efficiency of the antenna in the frequency range of 2-10 GHz is shown in fig. 4. The antenna has a maximum of 65.34% radiation efficiency at 3 GHz. The use of a substrate with high dielectric constant and a direct microstrip feeder may be the cause for deterioration in the radiation efficiency.

Fig. 5 shows the radiation patterns of the proposed antenna at 4.4, 6.2 and 8.1 GHz. It is seen that proposed antenna has a main beam in the broadside direction (0^0, 180^0) over all operating frequency. At 8.1 GHz although,

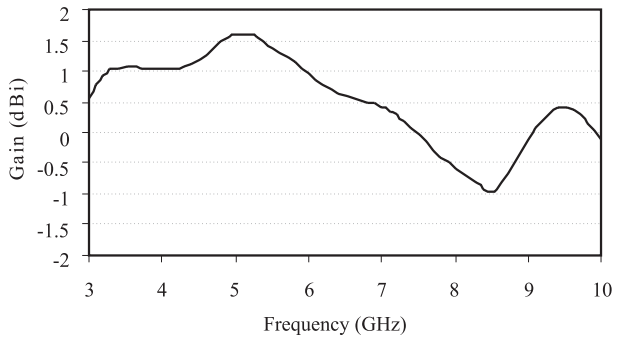

Fig.3. Gain of the proposed antenna in 3-10 GHz

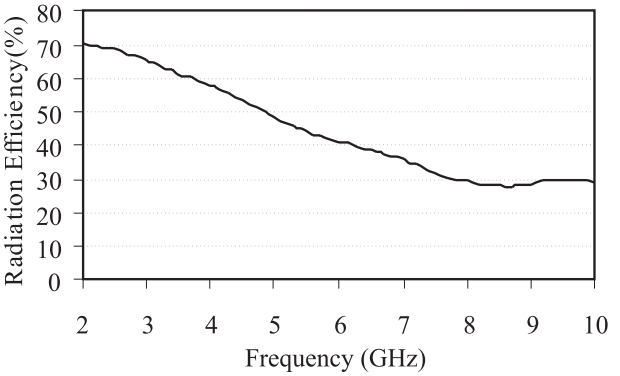

Fig.4. Radiation efficiency of the proposed antenna

the third harmonic radiation pattern (in cross-polarization) is observed, the antenna has a good stable radiation in the broadside direction without gain degradation unlike the existing UWB monopole antennas. At 8.1 GHz the difference of radiation level between copolarization ($\theta = 0^0$) and cross-polarization ($\theta = 90^0$) is approximately 6.69 dBi. The radiation pattern at 4.8 GHz shows that the difference in radiation level is relatively low compared to other frequency data. The differences of polarized radiation levels against the frequencies provide the advantage of minimizing fading effects by multicurrent paths in wireless communications /19/. In the E- plane, the 3 dB beam width is 78^0 at 4.8 GHz, 68.5^0 at 6.2 GHz and 87.9^0 at 8.1 GHz and the radiation patterns are almost symmetric. In the H- plane, the 3 dB beamwidth is 81.3^0 at 4.8 GHz, 78.7^0 at 6.2 GHz and 60.8^0 at 8.1 GHz.

Fig. 6 illustrates the current distributions of the proposed antenna at different frequencies. Through a numerical study of the vector current distributions on the antenna, three characteristics current modes are found to exist over the bandwidth from 3.0 to 16.0 GHz. Using fig. 2 as a reference, each current mode is dominant at each resonance, 8.1, 9.7 and 14.4 GHz respectively. It is seen that, the strongest currents are concentrated on the edges of the patch, which can be easily from fig.6. At 8.1 GHz the polarity of the current on the left portion of the patch is upward (along vertical direction), while at the right portion it is downward as shown in fig.6 (a). At 9.7 GHz the polarity

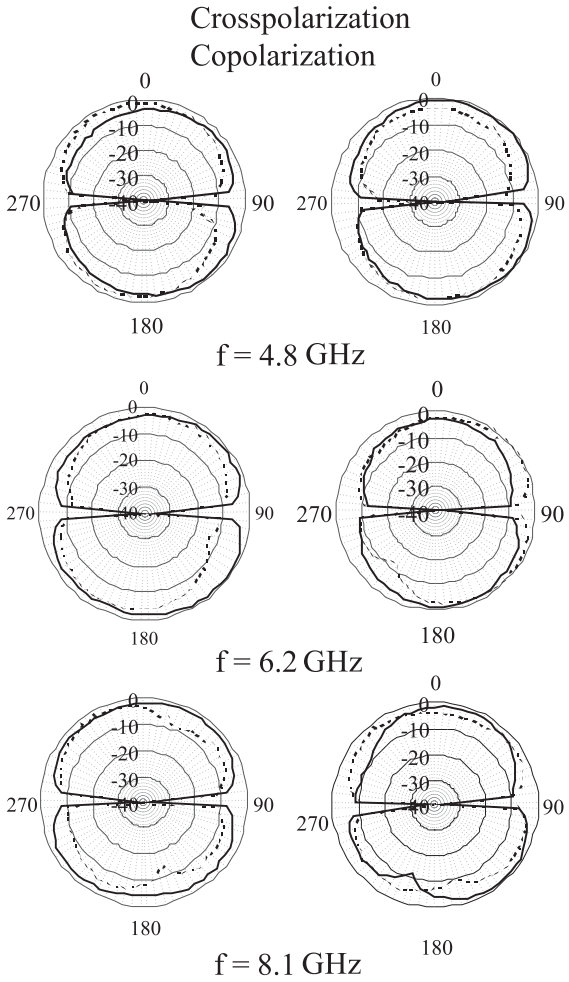

Fig.5. Radiation pattern of the proposed antenna (a) E-plane and (b) H-plane

on the upper portion of the patch (along vertical direction) is opposite to that of lower portion and very little amount of current is found on the centre of the patch as shown in fig.6 (b), while at 14.4 GHz the polarity of current on patch is downward in the upper portion and almost upward in the lower portion as shown in fig.6 (c). However, the current is uniformly distributed elsewhere.

4. Conclusions

A low cost, compact microstrip-fed planar UWB antenna has been proposed and implemented. The antenna size is 14.75×14.5 mm^2. The use of rectangular slot on the upper side of the partial ground plane improves not only the impedance matching in high frequency band but also the radiation characteristics at high frequencies. The antenna structure is flat, and its design is simple and straightforward, so it is easy to fabricate. The proposed antenna achieved a bandwidth of 136.12% (3.02 -15.89 GHz) at -10 dB. The relatively constant bidirectional radiation patterns and rather flat gain throughout the whole bandwidth makes the proposed antenna suitable for broadband applications.

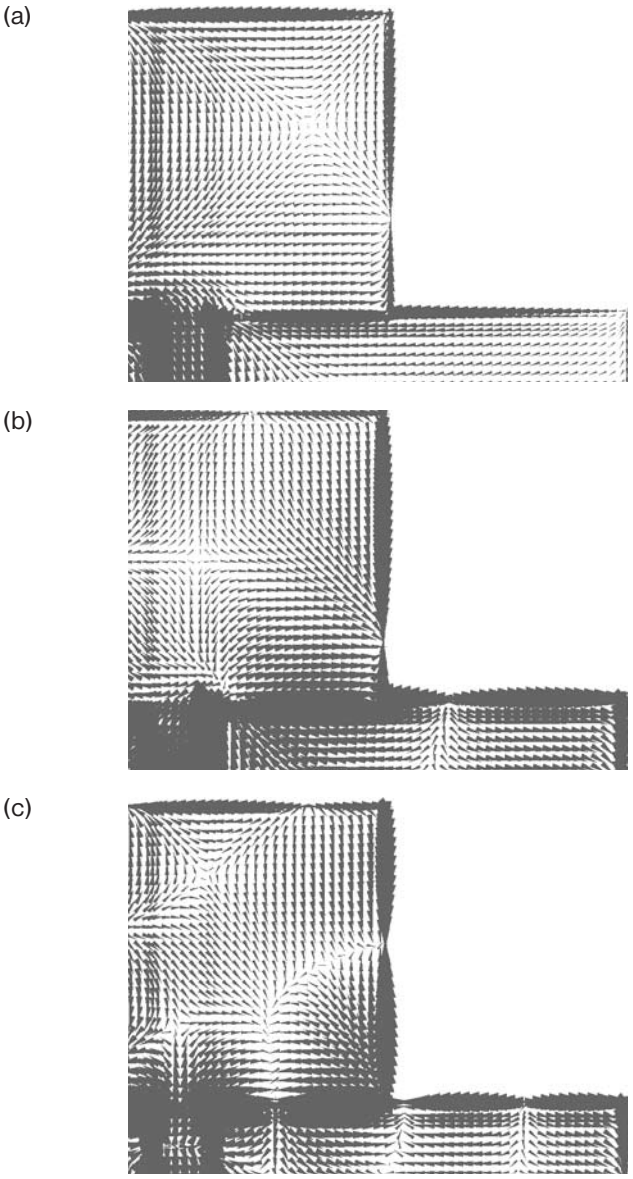

Fig. 6. Current distributions on the antenna at (a) 8.1 GHz, (b) 9.7 GHz and (c) 14.4 GHz.

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SIMULATION OF DIFFERENT ROUTER BUFFER SIZES WHICH INFLUENCES ON VOIP JITTER DELAY WITHIN THE ROUTED NETWORK

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Key words: Jitter, VoIP, delay, queuing discipline, buffer, QoS, voice quality

Abstract: This paper is continuation of /1/ where we tested different queuing methods and their influence on VoIP Jitter delay. Because we combine different queuing disciplines /1/ has also waiting queues be combined, in many cases even doubled. Such method has circumstances in case of VoIP round trip delay and also in case of packet delay variation where they rapidly increase. Such manner is not acceptable in VoIP case where we require small delays in all aspects. This is the reason why we in this paper presented aspects, how to reduce before mentioned delays. One approach is connected with reducing buffer length but anyway it mustn't be too short. The proper solution will also be presented in continuation.

Simulacija vpliva različnih velikosti pomnilnika usmerjevalnikov na zakasnitev VoIP prometa znotraj usmerjanega omrežja

Kjučne besede: Jitter, VoIP, zakasnitev, mehanizmi uvrščanja, pomnilnik, kvaliteta storitev

Izvleček: Članek predstavlja nadaljevanje raiskav, ki smo jih objavili v /1/, kjer smo preizkušali različne metode uvrščanja ter njihov vpliv na VoIP zakasnitev ter vpliv na Jitter. Ker smo v /1/ kombinirali različne mehanizme uvrščanja, so bile s tem kobinirane tudi čakalne vrste, v nekaterih primerih pa so bile celo podvojene. Pristop združevanja mehanizmov uvrščanja in s tem tud čakalnih vrst ima lahko predvsem vpliv na čas obhoda VoIP paketa in na variacijo zakasnitev, kjer se le te lahko opazno povečajo. Takšni scenariji v omrežjih s časovno občutljivimi aplikacijami niso dobrodošli, še posebej ne v primeru VoIP prometa, kjer težimo k čim manjšim zakasnitvam v vseh pogledih. To je pa hkrati tudi glavni razlog, zakaj smo se v tem delu odločili prikazati pristop, kako zmanjšati tovrstne zakasnitve pri kombiniranju mehanizmov uvrščanja. Eden izmed takšnih pristopov je zmanjšanje velikosti pomnilnika uporabljenega pri čakalnih vrstah. Pri zmanjševanju pomnilnika je potrebno paziti tudi na minimalno dolžino, saj se lahko zaradi premajhnega pomnilnika zavrže večje število paketov, kar pa je v nasprotju z našimi zahtevami in željami. Primerno rešitev predstavljamo v nadaljevanju tega prispevka.

1. Introduction

DEMAND upon VoIP quality speech has been expressed from VoIP vendors long time ago. Since then have been presented many solutions, some of them concerned improved voice encoder schemes, other are connected with queuing schemes and third one are connected with buffer length. The last mentioned also represents essential element of this research where we try to prove how buffer length influence on VoIP delay within the network. Definition says that delay is caused when packets of data (voice) take more time than expected to reach their destination. This causes some disruption in the voice quality. However, if it is dealt with properly, its effects can be minimized. When packets are sent over a network towards a destination machine/phone, some of them might be delayed. Reliability features in the voice quality mechanism sees to it that a conversation is not deadlocked waiting for a packet that went to have a walk somewhere in the green. In fact, there are many factors affecting the journey of packets from source to destination, and one of them is the underlying network. The delayed packet may come late or may not come at all, in last case it is lost. QoS (Quality of Service) considerations for voice are relatively tolerant towards packet loss, as compared to text. If you lose a word or a zero in your balance, your text might mean something completely different! If you lost a "hu" or a "ha" in a speech, it does not make a really big impact, except some hitch in voice quality. Besides, voice smoothing mechanism regulates it, so that you don't feel the bump. When a packet is delayed, you will hear the voice later than you should. If the delay is not big and is constant, your conversation can be acceptable. Unfortunately, the delay is not always constant, and varies depending on some technical factors. This variation in delay is called jitter, which causes damage to voice quality. That could such damage be minimal we make simulations where results proves how buffer length influences to VoIP jitter.

Used queuing scheme in simulation is described in the second section, meanwhile the third section presents VoIP jitter and his causes. Fourth section presents used G. 729 voice encoder scheme, fifth section presents the OPNET

Modeler simulation tool, which is used for proving our assumptions and decisions. In sixth section is presented simulated wired network structure, meanwhile obtained simulation results are presented in seventh section. Finally section concludes the paper.

2. Used queuing discipline introduction

Weighted fair queuing (WFQ): In situations where we want to provide constant response time and keep delays within range, without assigning an excessive bandwidth, we require optimal solution, so called weighted fair queuing. WFQ is an algorithm/mechanism which introduces bit-wise fairness and allows each queue to be served fairly (Figure 1). Fairness is provided by a mechanism which counts bytes. For the simplest example, we can observe two queues of the same length. The first contains 100 packets and the second only 50. In this case WFQ will work in the following manner; firstly it will take two packets from the first queue then one packet from the second queue and keep repeating this until fairness is achieved.

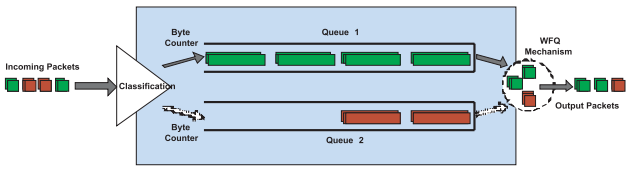

Fig. 1: Weighted fair queuing (WFQ) discipline

Such an algorithm creates service fairness for each participating queue. Low level priority traffic cannot then disturb travel through the network, which is a good compromise for each participating traffic flow within the network. WFQ also has other benefits such is configuring cost minimization, because it is capable of automatically accommodating dynamic network changes. Because of its good qualities, it is used on the majority of serial interfaces configured for E1 operation speeds (2048 Mbps). Weight is also, in this case, defined using the IP priority amount defined in the ToS field of the IP packet. For IP priorities, settings within the range from 0 (best effort) to 5 (IP quality speech) are in use, whilst meanwhile settings 6 and 7 are reserved. The algorithm then uses these data to calculate, how many additional services need to be provided for predicting each individual queue. It can use each available bandwidth that could a interfere with low-priority traffic flows, in an order that does not present high-priority traffic flow. In the basis is this principle, an opposite comparison with time-division multiplexing (TDM) which reserves all available bandwidths and leaves it unused if the traffic flow is not presented. WFQ is suitable for operating with IP priority settings, as is resource reservation protocol (RSVP), and is also capable of managing round-trip delay problem. Such queuing clearly improves an algorithms' SNA, logical link control (LCC) and transmission control protocol (TCP) and is, at the same time, capable of accelerating slow features and removing congestion within the network. Results become more predictable over the whole routing path, meanwhile delays can be multiplied reduced/decreased in comparison with other queuing disciplines (CQ, PQ, FIFO) /2, 3/.

3. VoIP Jitter and his causes introduction

Jitter is a variation in packet transit delay caused by queuing, contention and serialization effects on the path through the network. In general, higher levels of jitter are more likely to occur on either slow or heavily congested links. It is expected that the increasing use of "QoS" control mechanisms such as class based queuing, bandwidth reservation and of higher speed links such as 100 Mbit Ethernet, E3/T3 and SDH will reduce the incidence of jitter related problems at some stage in the future, however jitter will remain a problem for some time to come. In continuation we will introduce the main causes of jitter /4/. In particular, three types of jitter are well-known where belongs 'Constant Jitter (CJ)' marked as group 'A', and which is in correlation with packet to packed delay variation. The second type of jitter marked as group 'B' is 'Transient Jitter (TJ)' which is in connection with substantial incremental delay which could be incurred by a single packet. The last one, marked as group 'C' is short term delay variation which is usually commonly associated with congestions and route changes. Into group 'A' belongs the following causes; load sharing among multiple access links or IP service providers, load sharing within an IP service, and internal load sharing within routers. Into group 'B' belongs such causes which influences on 'TJ' jitter, and those are: sending system packet scheduling, LAN congestions, router firewall, routing table updates, route flapping and timing drift. Into last group belong access link congestion and router firewall conditionally. What is more important in our investigation is Jitter Buffer, respectively buffer length influence on such jitter.

A jitter buffer is designed to remove the effects of jitter from the decoded voice stream, buffering each arriving packet for a short interval before playing it out. This substitutes additional delay and packet loss (discarded late packets) for jitter. A fixed jitter buffer maintains a constant size whereas an adaptive jitter buffer has the capability of adjusting its size dynamically in order to optimize the delay/discard tradeoff. Both fixed and adaptive jitter buffers are capable of automatically adjusting to changes in delay. For example if a step change in delay of 20 milliseconds occurs then there may be some short term packet discards resulting from the change however the jitter buffer would be quickly realigned. In many cases the jitter buffer can be considered as a time window with one side (the early side) aligned with the recent minimum delay and the other side (the late side) representing the maximum permissible delay before a packet would be discarded. Another approach could be used with modeling the jitter buffer, named jitter buffer emulation. In this case we directly determine how many packets would be discarded as a result of jitter. This

has the advantage of being able to directly observe the time distribution of discard events and eliminates the step of trying to relate a jitter metric to a discard rate. If used as a jitter metric this would require a standardized jitter buffer to be used as proposed in /4, 7, 8, 9, and 10/.

4. G. 729 voice encoder scheme

The G.729 speech coder is an 8 kbps Conjugate-Structure Algebraic-Code-Excited Linear Prediction (CS-ACELP) speech compression algorithm approved by ITU-T. G.729. It offers high quality, robust speech performance at the price of higher complexity. It requires 10 ms input frames and generates frames of 80 bits in length. Within the G.729 coder the processing signals are 10 ms frames with additional 5 ms look-ahead. The total delay introduced by algorithm is 15 ms. Since G.729 is based on the Code-Excited Linear Prediction (CELP) model, each produced 80 bit frame, contains linear prediction coefficients, excitation code book indices, and gain parameters that are used by the decoder in order to reproduce speech. The input/output of this algorithm is 16 bit / 8 kbps linear PCM audio stream that is converted from/to a compressed data stream /5/.

5. Opnet modeler

OPNET Modeler's cutting-edge technology provides an environment for designing protocols and technologies as well as testing and demonstrating designs in realistic scenarios prior to production. OPNET Modeler is used by the world's largest network equipment manufacturers to enhance the design of network devices, technologies such as VoIP, TCP, OSPFv3, MPLS, IPv6, etc. Modeler represents a leading simulation tool used for modeling, and simulating communication networks, and their applications. At the same time it offers study analyze of telecommunication infrastructures, individual apparatus, protocols, and applications. This is a graphically-oriented simulation tool, which uses project, node and process editors for building communication models. The project editor offers graphic topological description, whilst the node editor is used for describing protocols. The process editor is an upgrade of C language, which uses a finite-state machine for algorithm and protocol descriptions. OPNET includes many standard communication models for constructing wired, radio, and optical and satellite communication structures. This tool also offers 2D and 3D animation for accompanying changes within the network's structure /6/.

6. Simulation structure

Network topology used in our simulation scenarios is shown in Figure 2. It represents only a test board structure for proving our assumptions about buffer length influence on jitter delay. Our main goal in these simulations is oriented towards improving the network's performances, regarding to the VoIP jitter.

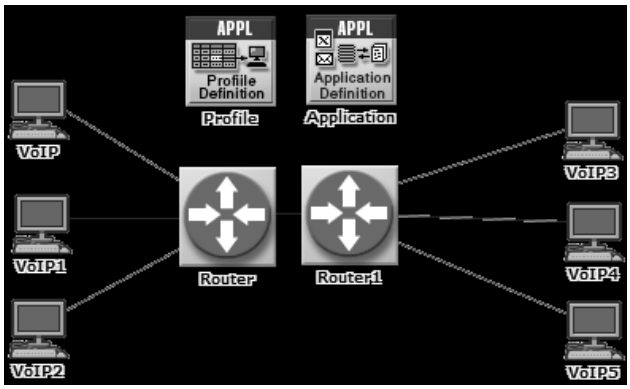

Fig. 2: Network simulation structure

The network structure consists of two sixteen port routers mutual connected where are on each router connected three VoIP users, commonly six, with generated 56 full meshed VoIP traffic flows. All clients are connected over 10BaseT link on routers, where are also routers mutual connected with the same connection type. VoIP application is defined using the 'Application' node shown on the top-right side in Figure 2. With 'Profile' node (beside applications node) are defined a client profiles, respectively what should User Equipment (UE) do, or better say, which application is such UE capable to use.

Table 1: Number of users

Application	Users	Class	Bandwidth
VoIP	6	1	10 Mbit/s

Simulation stricter is very simple because we only want to show how important part plays proper buffer length on voice quality in sense of jitter etc. For that case we prepare two different scenarios. In first is buffer length set to 256 MB (Mbytes). Such buffer represents the memory used to store packets awaiting processing or currently processed by the forwarding CPU. In a centralized scheme, processed packets remain in that memory until sent out on an appropriate interface. In the distributed scheme, processed packets are then forwarded to the appropriate slot memory. In second scenario is such buffer reduced on only 16 MB which contribute better results presented in continuation.

7. Simulation results

As we mentioned above, we use two different scenarios with the same network structure and different buffer lengths. We also try to figure out which length is the proper one, respectively which gives better delay results.

The minimal value which can be chosen in simulation tool is 8MB. For tested behavior of such value we again created new scenario which has been after successfully executed simulation compared with other two scenarios. The analysis shows that decreasing buffer length less than 16MB does not effect on delay parameters within the network, and at

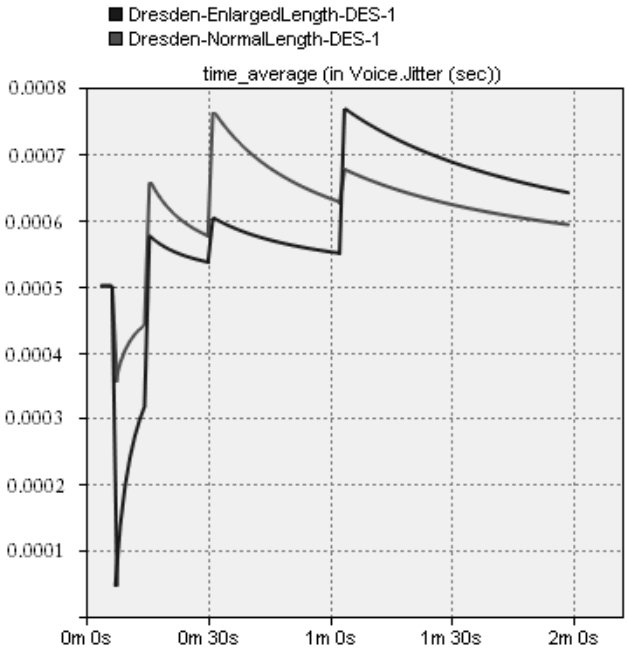

Fig. 3: Voice Jitter of VoIP application transmitted through two different buffer sizes (16MB buffer length –red, and 256MB buffer length - blue) in time average statistic

the same time, results in case of use 8MB buffer are quite similar to results when 16MB buffer is used. Comparison between 8MB and 16MB buffer length and their effect to Voice jitter is shown in figure 3. As we expected, large buffer increase voice jitter in second half of simulated period. Within first half of period largest buffer gives better results compare smaller buffer, because we have in first half of period smaller traffic compare with second half of simulation period. Since buffer is full, voice jitter rapidly increases as is shown in Figure 3 and then such approach fails, because VoIP traffic requires minimal delay within the network. Such jitter for both cases is fully acceptable, because highest value didn't reach 0.8ms, but is clearly to se affect of buffer length.

The end-to-end delay for both scenarios is presented in Figure 4. The end-to-end delay is thus the sum of the delays experienced at each hop on the way to the destination. Each such delay in turn consists of two components, a fixed component which includes the transmission delay at a node and the propagation delay on the link to the next node, and a variable component which includes the processing and queuing delays at the node.

In our case is such delay minimal, but situation can be changed using different simultaneous applications within the same network where can congestions appear and so on. Our simulated network has enough available bandwidth to transmit all VoIP traffic between communicating nodes, and this is the main reason why is end-to-end, respectively packet delay so small. It takes maximal value around 60,53ms for large buffer and around 60,22ms for small buffer.

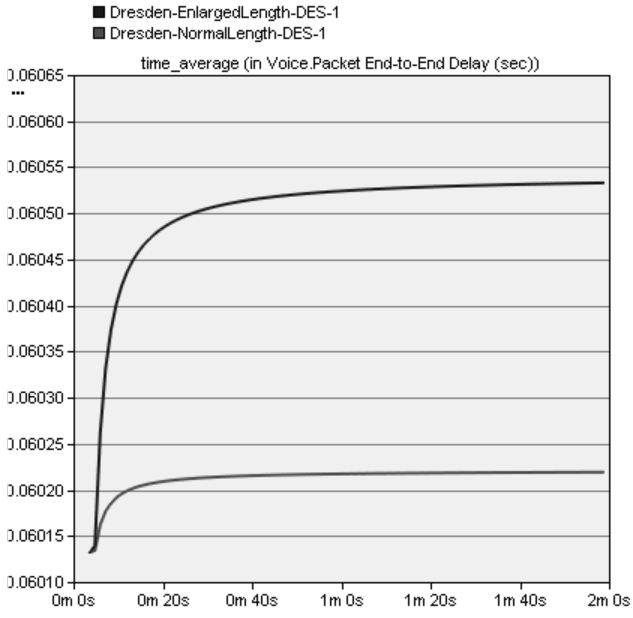

Fig. 4: Voice Packet End-to-End delay for two different buffer sizes (16MB buffer length – red, and 256MB buffer length - blue) in time average statistic

Packet Delay Variation (PDV) is defined by RFC 3393 as the difference in end-to-end delay between selected packets in a flow with any lost packets being ignored. The means of selection is not specified in RFC 3393, but e.g. could be the packets which gave the biggest variation in delay in a selected time period. The delay is specified from the start of the packet being transmitted at the source to the end of the packet being received at the destination. A component of the delay which does not vary from packet to packet can be ignored, hence if the packet lengths are the same and packets always take the same time to be re-assembled at the destination then the packet arrival time at the destination

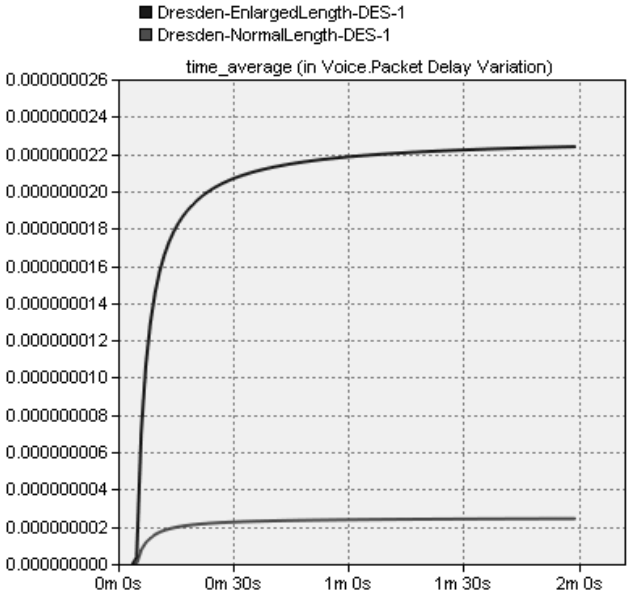

Fig. 5: Voice packet delay variation for two different buffer sizes (16MB buffer length – red, and 256MB buffer length - blue) in time average statistic

could be used instead of the time the end of the packet is received. From obtained results presented on Figure 5 we can assume that is before mention difference for PDV on minimal level, because maximal value don't reach more than 2,3 nano-seconds.

From above Figure we can assume that has been enough bandwidth present within the network for VoIP application transmission and because of that is data loss on minimal level.

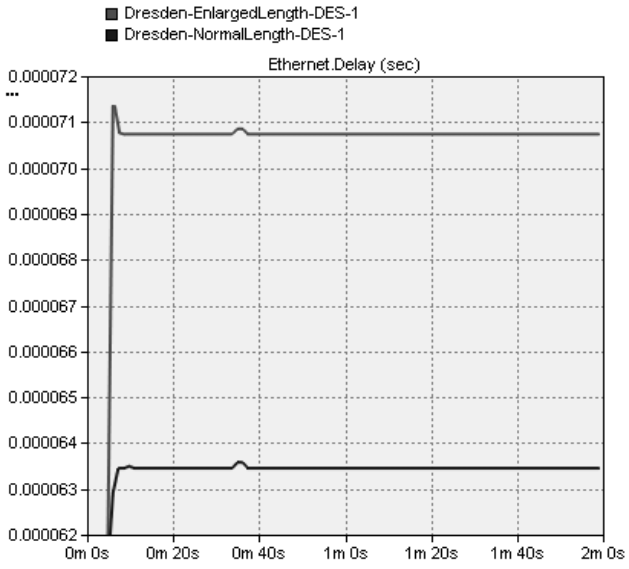

Fig. 6: Ethernet delay for two different buffer sizes (16MB buffer length – red, and 256MB buffer length - blue) in time average statistic

Also in case of Ethernet delay are differences between large and small buffer noticeable but they are on 71us level. Such delay is in practice imperceptible.

8. Conclusion

During this paper we show the reader how one of few possibilities affect on jitter in VoIP case, and how such solution affect on other parameters within the network, such as end-to-end delay and packet delay variation. From simulation results is clearly to see buffer length influence on VoIP traffic delay. As we mentioned in second section, such jitter can be additionally reduced with use of jitter buffer emulation, fixed jitter buffer and adaptive jitter buffers. This is also the issue for further research analysis on this area.

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INFLUENCE OF MATERIAL ATTACHMENT FOR EM ABSORPTION

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Key words: antenna, human head model, lossy-Drude model, materials, SAR.

Abstract: In this paper, reducing electromagnetic absorption (EM) with materials attachment is investigated. The finite-difference time-domain method with lossy-Drude model is adopted in this study. The methodology of SAR reduction is addressed and the effects of attaching location, distance, and size of ferrite sheet material on the SAR reduction are investigated. Materials have achieved a 47.68% reduction of the initial SAR value for the case of 1 gm SAR. These results suggest a guideline to choose various types of materials with the maximum SAR reducing effect for a phone model.

Vpliv feritnega dodatka na EM absorpcijo

Kjučne besede: antena, človeški model glave, model lossy-Drude, materiali, SAR

Izvleček: v članku raziskujemo vpliv dodatnih pritrjenih materialov na EM absorpcijo. Pri simulaciji smo uporabili dva modela. S pomočjo metodologije SAR zasledujemo vpliv položaja, razdalje in velikosti ploskih feritnih materialov na zmanjševanje SAR. Dodani materiali zmanjšajo za 47.68 % začetno SAR vrednost v primeru 1g SAR. S pomočjo teh rezultatov pridemo do smernic pri izbiri materialov za doseganje največjega SAR zmanjšanja za model telefona.

1. Introduction

Sources of radio frequency/microwave (RF/MW) radiation, particularly cellular phones are ever present. RF/MW sources are part of daily life, but they also reason for concern regarding the possible biological effects of microwaves. It is important that the biological effects of RF/MW fields are minimal, at least at the level of their clinical significance, so that health risk can be assessed. Because the potential shock of RF/MW fields on human health has not yet been well characterized, the basic knowledge from laboratory studies based on cellular and animal test systems are invaluable. The interaction of handset antennas with the human body is a great consideration in cellular communications. The user's body, especially the head and hand, influence the antenna voltage standing wave ratio (VSWR), gain, and radiation patterns. Furthermore, thermal effects, when tissues are exposed to unlimited electromagnetic energy, can be a serious health hazard. Therefore standards organizations have set exposure limits in terms of SAR /1, 2/. SAR is a measure of the rate at which radio frequency (RF) energy is absorbed by the body when exposed to a radio-frequency electro-magnetic field. SAR is used to measure exposure to fields between 100 kHz and 10 GHz /3-5/. It is commonly used to measure power absorbed from mobile phones and during MRI scans. The value will depend on the geometry of the part of the body that is exposed to the RF energy, and on the exact location and geometry of the RF source.

Cellular phone protection and the enforcement of pertinent exposure standards are issues in the current media, and regulatory agencies are motivated to assure that compliance testing is acceptable. IEEE Standard 1528 /1/ and IEC 62209-1 specify protocols and process for the measurement of the peak spatial-average SAR induced inside a simplified model of the head of users of hand held radio transceivers (cellular phones). For example, the SAR limit specified in IEEE C95.1: 1999 is 1.6 W/kg in a SAR 1 gm averaging mass while that specified in IEEE C95.1: 2005 has been updated to 2 W/kg in a 10 gm averaging mass /2/. This new SAR limit specified in IEEE C95.1: 2005 is comparable to the limit specified in the International Commission on Non-Ionizing Radiation Protection (ICNIRP) guidelines.

The exposure limits are defined commonly in terms of the spatial peak SAR averaged either over any one gram or ten grams of tissue. Since 1997, the U.S. Federal Communication Commission (FCC) requires the routine SAR evaluation of a phone model prior to device authorization or use. So there is a need to reduce the spatial peak SAR in the design stage of a phone model because the possibility of a spatial peak SAR exceeding the recommended exposure limit cannot be completely ruled out /2/, /3-5/. The interaction of the cellular handset with the human head has been investigated by many published papers considering; first, the effect of the human head on the handset antenna performance including the feed-point impedance, gain, and

efficiency /6-10/, and second, the impact of the antenna EM radiation on the user's head due to the absorbed power, which is measured by predicting the induced SAR in the head tissue /9-13/.

The most used method to solve the electromagnetic problem in this area is the finite-difference time-domain (FDTD) technique /12-13/. Although, in principle, the solution for general geometries does not require any additional effort with respect to the standard method, the technique requires the definition of a discretized space by assigning to each cell its own electromagnetic properties, which is not an easy process /14-16/. Specifically, the problems to be solved in SAR reduction need a correct representation of the cellular phone, anatomical representation of the head, alignment of the phone and the head, and suitable design of materials or metamaterials.

Human exposure to electromagnetic (EM) radiation, as well as the pertinent health effects, constitutes a matter of raised public concern, and this issue has undergoing continuous scientific investigation. Various studies on this subject exist /14–17/, most of which mainly investigate into the consequences of mobile-phone usage. Yet, devices and communication terminals operating in other frequency bands have also gained substantial interest in the last 15 years. In /8/, a ferrite sheet was adopted as protection between the antenna and the human head. A reduction of over 13% for the spatial peak SAR over 1 gm averaging was achieved. A study on the effects of attaching a ferrite sheet for SAR reduction was presented in /15/, and it was concluded that the position of shielding plays an important role in the reduction effectiveness.

In /17/, for the SAR in the human head, an effective approach is the use of a planar antenna integrated onto the back side (away from the head) of a phone model, but it brings additional design difficulties especially in achieving the required frequency bandwidth and radiation efficiency. Another approach is the use of a directional or reflecting antenna /15-16/. Such an antenna structure sacrifices the availability of signals received from all directions to the phone model. The mechanism of SAR reduction by ferrite sheet attachment was due to the suppression of surface currents on the front side of phone model /18/. However, the relationship between the maximum SAR reducing effect and the parameters such as attaching location, size and material properties of ferrite sheet remains unknown.

In /11/,/18/ a perfect electric conductor (PEC) reflector was placed between a human head and the driver of a folded loop antenna. The result showed that the radiation efficiency can be enhanced and the peak SAR value can be reduced. In /14/, a study on the effects of attaching conductive materials to cellular phone for SAR reduction has been presented. It is shown that the position of the shielding material is an important factor for SAR reduction effectiveness. There is a necessity to make an effort for reducing the spatial peak SAR in the design stage of ferrite sheet because the possibility of a spatial peak SAR exceeding the recommended exposure limit cannot be completely ruled out.

This paper is structured as follows. Section II describes the numerical analysis of the handset together with the SAM phantom head. The FDTD method is used with positive meshing techniques for quick and correct analysis. The modeling and analyzing technique will be described in Section III. Simulation and comparing results of materials will be summarized in Section IV and Section V concludes the paper.

2. Simulation model and numerical techniques

A. Model Description

The simulation model which includes the handset with PIFA type of antenna and the SAM phantom head provided by CST Microwave Studio® (CST MWS) is shown in Fig. 1. A complete handset model composed of the circuit board, LCD display, keypad, battery, and housing was used for simulation. The relative permittivity and conductivity of individual components were set to comply with industrial standards. In addition, definitions in /3-4/, /17/ were adopted for material parameters involved in the SAM phantom head. In order to accurately characterize the performance over a broad frequency range, dispersive models for all the dielectrics were adopted during the simulation /3/. Fig. 2 shows the dispersive permittivity of the liquid in the SAM phantom head for simulation. In Fig. 2, Eps' and Eps'' represents dielectric dispersion fit Debye 1st order and 2nd order respectively. The electrical properties of materials used for simulation are listed in Table 1. A PIFA type antenna constructed in a helical sense operating at 900 MHz for GSM application was used in the simulation model. In order to obtain a high-quality geometry approximation for such a helical structure, a predictable meshing scheme used in the FDTD method usually requires large number of hexahedrons which in turn makes it extremely challenging to get convergent results within reasonable simulation time.

Fig. 1: Complete model used for simulation including handset and SAM phantom head.

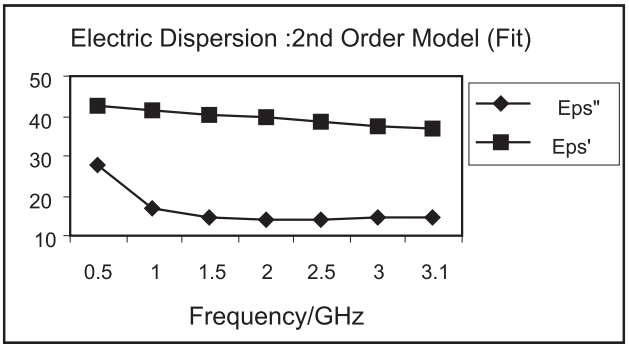

Fig. 2: Dispersive permittivity of the liquid in the SAM phantom head used for simulation.

Table 1: Electrical properties of materials used for simulation

Phone Materials	ε_r	σ (S/m)
Circuit Board	4.4	0.05
Housing Plastic	2.5	0.005
LCD Display	3.0	0.02
Rubber	2.5	0.005
SAM Phantom Head		
Shell	3.7	0.0016
Liquid @ 900MHz	40	1.42

B. Numerical Technique

CST MWS, based on the finite integral time-domain technique (FITD), was used as the main simulation instrument. A non-uniform meshing scheme was adopted so that the major computation endeavor was dedicated to regions along the inhomogeneous boundaries for fast and perfect analysis. Fig. 3 shows the mesh for two cut planes of the complete model indicating the area with denser meshing along the inhomogeneous boundaries. The minimum and maximum mesh sizes were 0.3 mm and 1.0 mm, respectively. A total of 2,097,152 mesh cells were generated for the complete model, and the simulation time was 1163 seconds (including mesh generation) for each run on an Intel Core™ 2 Duo E 8400 3.0 GHz CPU with 4 GB RAM system.

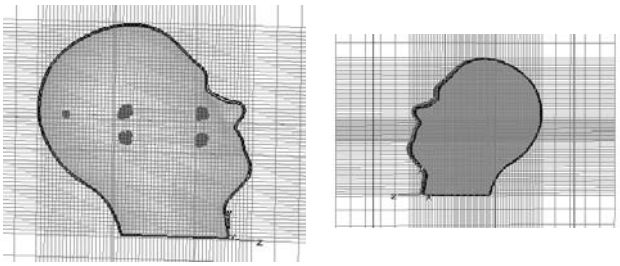

Fig. 3: Mesh view for two cut planes of the complete model showing the non-uniform meshing scheme adopted for simulation.

The analysis workflow started from the design of the antenna with complete handset model in free space. The antenna was designed such that the *S*11 response was less than -10 dB over the frequency band of interest. The SAM phantom head was then included for SAR calculation using the standard definition as /5/

$$SAR = \frac{\sigma}{2\rho} E^2$$

where *E* is the induced electric field (V/m), ρ is the density of the tissue (kg/m^3), and σ is the conductivity of the tissue (S/m). The resultant SAR values averaged over 1 gm and 10 gm of tissue in the head were denoted as SAR 1 gm and SAR 10 gm, respectively. These values were used as a benchmark to appraise the effectiveness in peak SAR reduction.

3. Sar reduction with lossy drude model

A. Lossy-Drude Model

The SA reduction effectiveness and antenna performance with different positions, sizes, and material properties of materials and metamaterials will be analyzed. The head models used in this study were obtained from a MRI-based head model through the whole brain Atlas website. Six types of tissues, i.e., bone, brain, muscle, eye ball, fat, and skin were involved in this model /17-19/. Table II shows their dielectric properties. Fig. 4 shows a horizontal cross-section through the eyes of this head model. The electrical properties of tissues were taken from /13/. Numerical simulation of SAR value was performed by the FDTD method. The parameters for FDTD computation were as follows. In our Lossy-Drude simulation model, the domain was 128 x 128 x 128 cells in the FDTD method. The cell sizes were set as $\Delta x = \Delta y = \Delta z$ = 1.0 mm. The computational domain was terminated with 8 cells perfectly matched layer (PML). A PIFA antenna was modeled for this paper by the thin-wire approximation. Simulations of materials and metamaterials are performed by the FDTD method with the lossy-Drude model /19/. The method is utilized to understand the wave propagation characteristics of materials and metamaterial.

Table 2: Dielectric tissue properties at 900 MHz

Material	Density, ρ (Kg-m^{-3})	Conductivity, σ (S-m^{-1})	Relative permittivity ε_r
Fat, bone	1130	0.12	4.83
Muscle, skin	1020	1.5	50.5
Brain	1050	1.11	41.7
Eye ball	1000	2.03	68.6

B. Analysis Method

Fig. 5 shows a portable telephone model at 900 MHz for the present study. It was considered to be a quarter wavelength PIFA antenna mounted on a rectangular conducting box. The conducting box was 10 cm tall, 4 cm wide, and 3

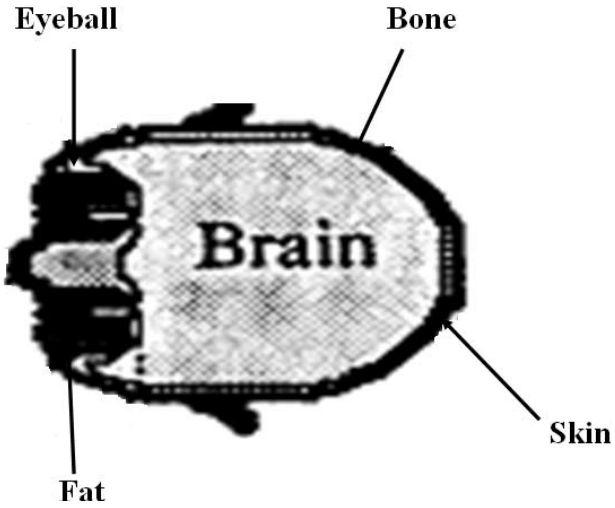

Fig. 4: Human head model for FDTD computation.

cm thick. The PIFA antenna was located at the top surface of the conducting box. A ferrite sheet with a height of 90 mm, a width of 40 mm, and a thickness of 3.5 mm was attached to the conducting box as shown in Fig. 5.

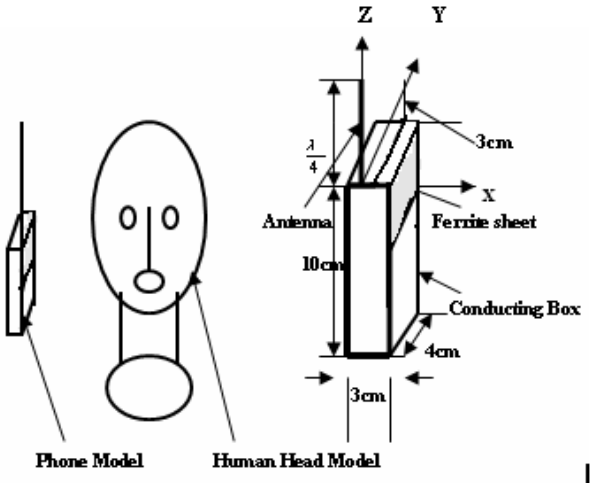

Fig. 5: odels of the head and portable telephone with an attached ferrite sheet.

The SAM head model was considered for this research where it consists about 2,097,152 cubical cells with a resolution of 1 mm. The FDTD method was employed in the numerical analysis. Its discretized formulations were derived from the following Maxwell's time-domain equations:

$$\frac{\delta H}{\delta t} = -\frac{1}{\mu_0 \mu_r'}(\nabla \times E) - \frac{\sigma^*}{\mu_0 \mu_r'} H. \quad (1)$$

$$\frac{\delta E}{\delta t} = -\frac{1}{\varepsilon_0 \varepsilon_r'}(\nabla \times H) - \frac{\sigma^*}{\varepsilon_0 \varepsilon_r'} E. \quad (2)$$

where $\sigma^* = \omega \mu_0 \mu_r''$ and $\sigma = \omega \varepsilon_0 \varepsilon_r''$. A space domain enclosing the human head and the phone model is also shown in Fig. 5. The time step was set to $\frac{\delta}{\sqrt{3}c}$, where *c* is the speed of light, to guarantee the numerical stability. The time-stepping was performed for about eight sinusoidal cycles in order to reach a steady state. To absorb outgoing scattered waves, the second order Mur absorbing boundaries acting on electric fields were used. An antenna excitation was introduced by specifying a sinusoidal voltage across the one-cell gap between the helix and the top surface of the conducting box.

The antenna output power is defined as

$$P_{out} = P_{abs} + P_{ferr} + P_{rad}$$
$$\frac{1}{2}\int_{Vh} \sigma |E|^2 \, dv + \frac{1}{2}\int_{Vf} (\sigma |E|^2 + \sigma^* |H|^2) \, dv + \frac{1}{2} \mathrm{Re} \left(\int_s E \times H^* . \vec{n} . ds \right) \quad (3)$$

where P_{abs} is the power absorbed in the head with a volume of V_h, P_{ferr} is the power dissipated in the ferrite sheet with a volume of V_f, and $P_{rad.}$ is the power radiated to the far-field, which can be calculated by integrating the normal component of the Pointing vector E x H^* over a surface S completely surrounding the head/phone model configuration.

4. Impact on sar of ferrite sheet attachment

In this section, a ferrite sheet is placed between the antenna and a human head thus reducing the SAR value. In order to study SAR reduction of an antenna operated at the GSM 900 band, different positions, sizes, and ferrite sheet materials for SAR reduction effectiveness are also analyzed by using the FDTD method in conjunction with a detailed human head model.

Fig. 6 shows the simulation model which includes the handset with monopole type PIFA antenna and the SAM phantom head provided by CST MWS.

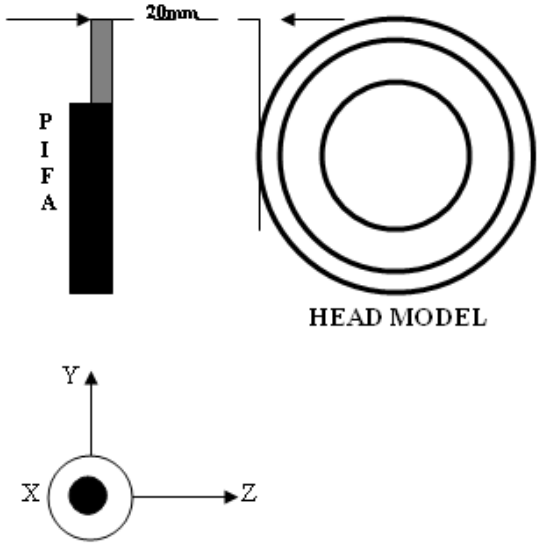

Fig. 6: The head and antenna model for SAR calculation.

The dispersive models for all the dielectrics were adopted during the simulation in order to accurately characterize the ferrite sheet. The antenna was arranged in parallel to the head axis, the distance is varied from 5 mm to 20 mm, and finally 20 mm was chosen for comparison with the ferrite sheet. Besides that, the output power of the mobile phone model needs to be set before SAR is simulated. In this paper, the output power of the cellular phone is 500 mW at the operating frequency of 900 MHz In the real case, the output power of the mobile phone will not exceed 250 mW for normal use, while the maximum output power can reach to 1 W or 2 W when the base station is far away from the mobile station (cellular phone). Without ferrite sheet, the SAR simulation is compared with the results in /6, 17 / for validation, as shown in Table III also with ferrite sheet, the SAR simulation is compared with the result of /8/ for validation, as shown in Table IV. The calculated peak SAR 1 gm value is 2.002 W/kg, and SAR 10 gm value is 1.293 W/kg when the phone model is placed 20 mm away from the human head model without a ferrite sheet. This SAR value is better compared with the result reported in /13/, which is 2.43 W/kg for SAR 1 gm. The ferrite sheet material is utilized in between the phone and head models, and it is found that the simulated value of SAR 1 gm and SAR 10 gm are 1.043 W/kg and 0.676 W/kg respectively. The reduction about of 47.68% was observed in this study when a ferrite sheet is attached between the phone and human head models for SAR 1 gm. This SAR reduction is better than the result reported in /8/, which is 13% for SAR 1 gm. This is achieved using different radiating powers and impedance factors and it is because the electromagnetic source is being moved away from the head. Figs. 7-11 show the SAR value compared with the distance between phone and head models, width of ferrite sheet between 20-40 mm, thickness of ferrite sheet between 2-3.5 mm, and height between 40-90 mm respectively.

Table 3: Comparisons of peak sar at 900 mhz without ferrite sheet

Tissue	SAR value (W/kg)
SAR value for [6]	2.17
SAR value for [17]	2.28
SAR value this work for 1 gm	2.002

Table 4: Comparisons of peak sar at 900 mhz with ferrite sheet

Tissue	SAR value (W/kg)
SAR value for [8]	1.392
SAR value this work for 1 gm	1.043

The reduction efficiency of the SAR depends on its width and height. In order to definitely confirm this, 1 gm and 10 gm average SAR versus distance, width, thickness, and height are plotted in the Figs. 7-11. In Fig. 7, it is shown that if the distance between phone and human head models is varied then the SAR value decreases. This is because the dielectric constant, conductivity, density and magnetic tangent losses are also varied. In Fig. 8, it can be observed that the SAR value reduces with the increase of the width of the ferrite sheet. As shown in Fig. 9, the SAR value decreases until a thickness of 3 mm, and then a different tendency i.e., it started to increase after 3 mm. The height is varied up to 90 mm in Fig. 10. From this figure it can be shown that if the height of the ferrite sheet increases, then the SAR value also decreases up to a height of 80 mm, and it started to increase after 80 mm. Fig. 11 shows the SAR value with ferrite sheet attachment for 1 gm and 10 gm average SAR. It can be observed that with ferrite sheet attachment the SAR value has been decreased for the case of 1 gm and 10 gm average SAR. The results implies that only suppressing the maximum current on the front side of the conducting box contributes significantly to the reduction of spatial peak SAR. This is because the decreased quantity of the power absorbed in the head is considerably larger than that dissipated in the ferrite sheet and it is because the electromagnetic source is being moved away from the head.

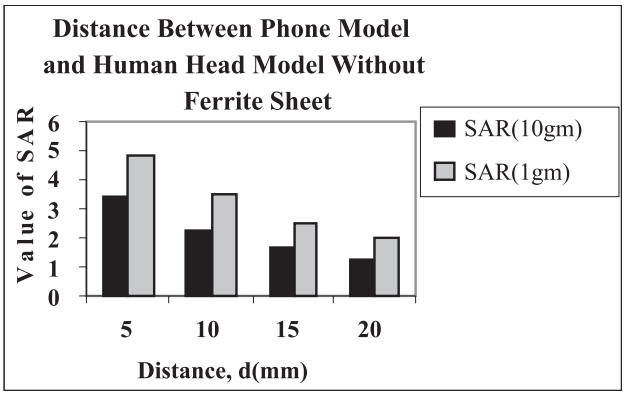

Fig. 7: SAR value compared with the distance between phone model and human head model without ferrite sheet.

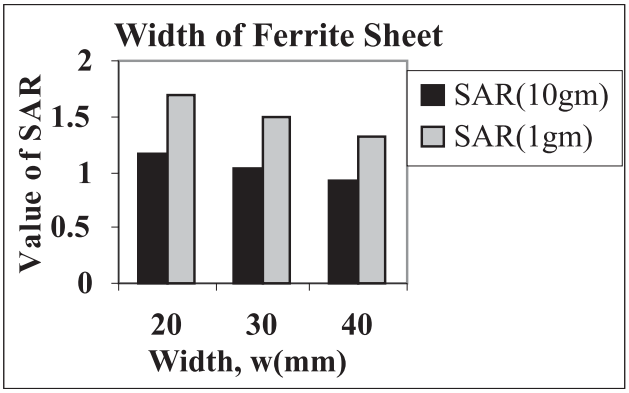

Fig. 8: SAR value compared with the width of the ferrite sheet.

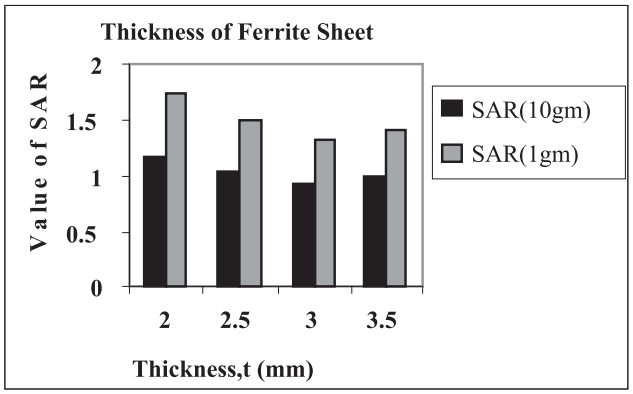

Fig. 9: SAR value compared with the thickness of the ferrite sheet.

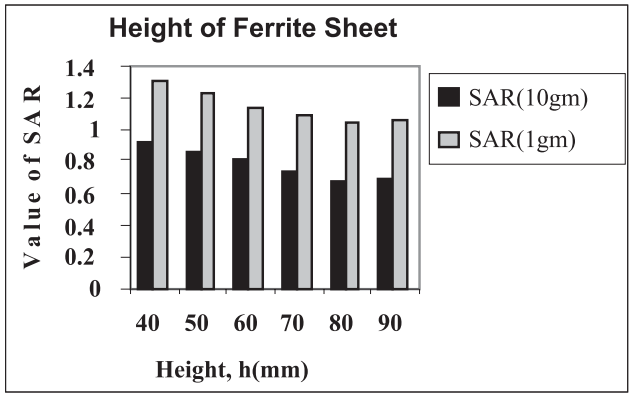

Fig. 10: SAR value compared with the height of the ferrite sheet.

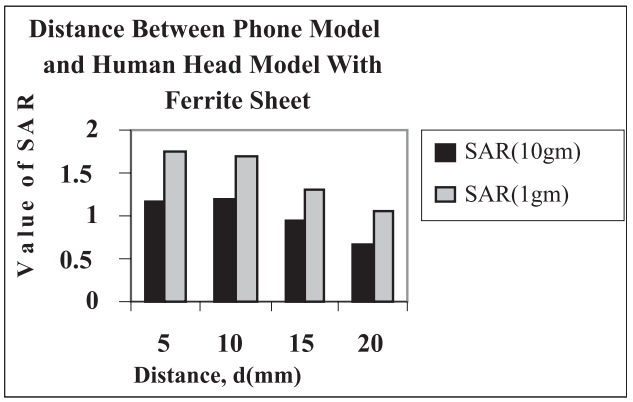

Fig. 11: SAR value compared with the distance between phone model and human head model with ferrite sheet.

5. Conclusion

The EM interaction between an antenna and the human head with ferrite sheet material has been discussed in this paper. Utilizing material in the phone model a SAR value is achieved of about 0.676 W/kg for SAR 10 gm and 1.043 W/kg for SAR 1 gm. Based on the 3-D FDTD method with lossy-Drude model, it is found that for the both cases peak SAR 1 gm and SAR 10 gm of the head can be reduced by placing materials between the antenna and the human head. Numerical results can provide useful information in designing communication equipment for safety compliance.

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MPEG-2 TS MULTIPLEXER IN FPGA TECHNOLOGY

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Key words: Moving Picture Experts Group 2 Transport Stream (MPEG-2 TS), data multiplexer, Field Programmable Gate Array (FPGA), video, Ethernet.

Abstract: This paper discusses design and testing of a Moving Picture Experts Group 2 (MPEG-2) Transport Stream (TS) multiplexer in Field Programmable Gate Array (FPGA) technology that would transmit multiplexed packets via Ethernet. Multiplexer is designed in accordance with standard ISO/IEC 13818-1, thus it is fully compatible with standard players. The digital design is very flexible since adding additional payload sources is effortless. Use of a microprocessor has been dropped since it often provokes non-deterministic situations, hence the design is very robust yet fully programmable.

Podatkovni multiplekser MPEG-2 TS v vezju FPGA

Kjučne besede: Moving Picture Experts Group 2 (MPEG-2) transportni pretok, podatkovni multiplekser, Field Programmable Gate Array (FPGA), video, Ethernet.

Izvleček: V članku je predstavljen razvoj in preizkušanje podatkovnega multiplekserja za transportni pretok Moving Picture Experts Group 2 (MPEG-2 TS) v tehnologiji Field Programmable Gate Array (FPGA), ki oddaja multipleksirane podatkovne pakete prek omrežja Ethernet. Multiplekser je izdelan v skladu s standardom ISO/IEC 13818-1, zaradi česar je popolnoma kompatibilen s standardnimi predvajalniki. Digitalno vezje je zelo fleksibilno, saj je vključevanje dodatnih podatkovnih virov enostavno. Uporaba mikroprocesorja je bila opuščena, saj ta pogosto izzove nedeterministične situacije. Vezje je torej zelo robustno, vendar še vedno popolnoma programabilno.

1. Introduction

As result of rapid evolution of consumer electronics having been faced recently we can notice an immense increase of data transfers worldwide. Predictions have been made about global Internet Protocol (IP) traffic quintupling from 2008 to 2013 /1/. Extensive bandwidth requirements are consequence of technological convergence which is an operators' concept of bundling together various structure-independent services the user can then access /2/, which can be seen from the engineer's point of view as merging of technologies and processes from multiple industries. It is only in the last decade when convergence has taken places in our everyday, joining mobile and stationery communications with broadband internet, terminal applications, digital television and other technologies.

When discussing digital television the data-transferring aspect of such an application should be considered. Nearly real-time transmission of moving picture (i.e. streaming) is very pretentious about required bandwidth, especially when transmitting high-definition (HD) content. Required transmission bitrates for Standard-Definition Television (SDTV) and for High-Definition Television (HDTV) are normally up to 7 Mbps and 30 Mbps, respectively /3/. Because of these bandwidth demands one should reflect on optimizing the data path not only by the means of improving payload compression, but mainly by using a proper information coding system providing an optimal transmission of transferred content. Today it is already very common to have network connections up to 100 Mbps over copper /4/ or 1000 Mbps over fiber; nevertheless an optimal coding system is required because transmission of video is a time-critical application.

If we take a look at a common digital television (DTV) program we can notice it consists of several elements. First, there is the video signal that describes the moving picture, together with one or more audio signals and probably equipped with some other data, such as Electronic Program Guide (EPG). Therefore we need to establish the best possible way of coding data before transmitting it, especially because we want to transmit multiple streams via a single communications channel. Such coding system is described in standard ISO/IEC 13818-1 /5/, known as Moving Picture Experts Group 2 (MPEG-2) Transport Stream (TS). It defines delivery of multiple elementary streams using services of multiplexing, timing, buffer management and control data transmission /6/.

Since recent hardware development tends toward solutions that are not only highly compact but also complex enough to perform sophisticated functions, we developed a solution that embeds an MPEG-2 TS Multiplexer carried out within a Field Programmable Gate Array (FPGA) circuit using digital logic elements only. Therefore the use of an embedded microprocessor has been dropped, which was possible mainly because a multiplexer is actually a fundamental unit of FPGA designs. Therefore a complex multiplexer like MPEG-2 TS can be carried out using basic smaller multiplexers with some additional complex control logic. Nevertheless such a system needs to be flexible enough to embed all the mechanisms that are required by standard ISO/IEC 13818-1 which fully determines MPEG-2 TS /5/.

2. Methods

An ordinary digital television (DTV) program consists of a video signal, an audio signal and auxiliary data (e.g. Electronic Program Guide – EPG). Those fundamentals can be interpreted as elementary streams of that program. Because we want them transferred over a common communications channel we need to packetize the elementary streams and conduct them through the process of multiplexing. An example data multiplexer is presented in Fig.1.

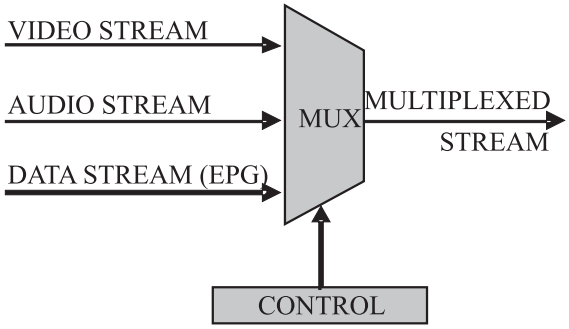

Fig. 1: Example data multiplexer.

The three elementary streams we can see in Fig.1 are coupled into a single multiplexed data stream that embeds both video and audio, together with some additional data (e.g. EPG). Such a stream represents a single DTV program. Nevertheless, if hardware is powerful enough we can perform multiplexing of more than just one DTV program to join them into a single stream that can be transferred via a communications channel. An example of multiplexing three programs into a single stream is shown in Fig.2.

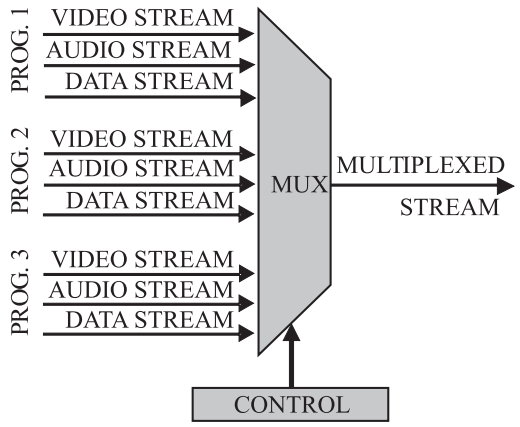

Fig. 2: Example multiprogram data multiplexer.

In order to achieve a configuration capable of multiplexing several digital television (DTV) programs into a single data stream, one should consider a proper hardware configuration that would allow construction of a compact yet powerful device. The solution we developed is based on a Field Programmable Gate Array (FPGA) integrated circuit, together with some additional communication periphery.

2.1 Digital design

Schematics of Field Programmable Gate Array (FPGA) circuit contents are shown in Fig.3. The Moving Picture Experts Group 2 Transport Stream (MPEG-2 TS) multiplexer shown in Fig.3 is basically a complex digital switch, made of several small multiplexers. Due to the FPGA technology being carried out mainly with look-up tables (LUT) and flip-flops (FF), a multiplexer is actually a "natural" unit of an FPGA digital design.

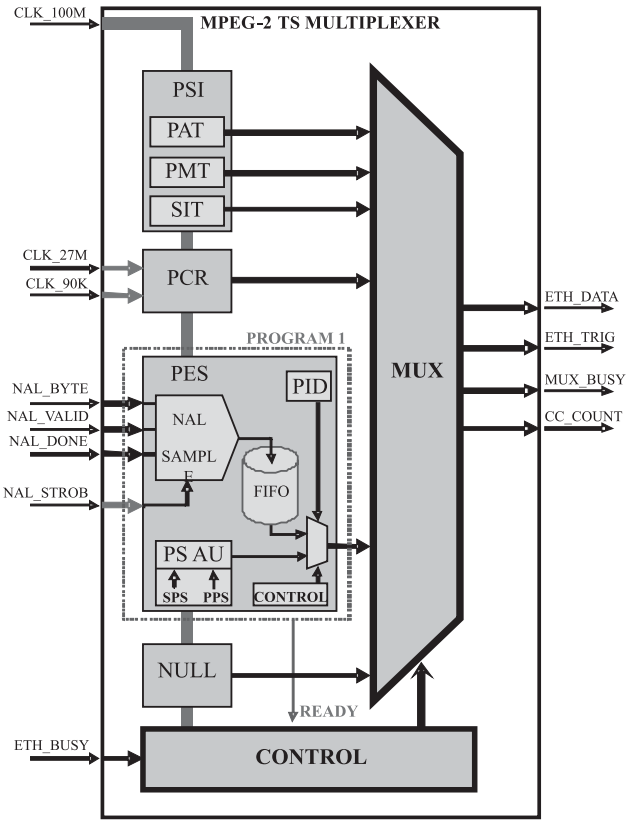

Fig. 3: Contents of FPGA circuit.

The main multiplexer in the MPEG-2 TS digital design (*MUX* in Fig.3) switches between various sources and it is based on 100 MHz clock that is captured directly from an external oscillator, hence jitter is negligible.

Program Specific Information (PSI) Table generation unit produces tables that are needed in MPEG-2 TS to specify what elements are contained within the Transport Stream. These tables are Program Association Table (PAT), Program Map Table (PMT) and Selection Information Table (SIT), and carry information about elementary streams that are then packetized and multiplexed together with other payload data into single Transport Stream.

Program Clock Reference (PCR) section handles two counters that are sampled separately but joined together into a single data packet. The packet contains samples of 27 MHz and 90 kHz clocks and is needed for the decoder to synchronize and properly present the decompressed content at correct time. Since the 27 MHz counter actually represents System Time Clock (STC) it has to have a clean

source, hence it is driven directly from a 27 MHz oscillator so that jitter is insignificant. Clock with frequency 90 kHz is, however, produced using a Digital Clock Manager (DCM) unit and therefore additional jitter is present.

Program Block, marked as "Program 1" on Fig.3, contains logic to handle, temporary store and multiplex a single video signal, represented in the form of a Network Abstraction Layer (NAL) bit stream. Such a representation of video signal is typical of standard Motion Picture Experts Group 4 – Advanced Video Coding (MPEG-4/AVC), more known as H.264 /7/. A stream like this can be handled by our MPEG-2 TS multiplexer quite effortlessly. Program Block incorporates logic to sample NAL bit stream (input NAL_BYTE) regarding appropriate flags (inputs NAL_VALID, NAL_DONE and NAL_STROB) and stores it into a First-In-First-Out (FIFO) buffer, generated as data vector with a pointer that act together as a circular buffer. When first half of buffer is full the Program Block adds the proper Packet Identifier (PID) and sends the NAL bit stream to the main multiplexer as a Packetized Elementary Stream (PES), while still continuing to store the incoming NAL bit stream into the second half of FIFO. Whether the incoming NAL stream does not include Presentation Set Access Units (PS AU), the Program Block can add both Stream Parameter Set (SPS) and Picture Parameter Set (PPS).

Since main benefit of multiplexing video or audio signals is the possibility of packing more such signals into a single transport stream, the Program Block (PES in Fig.3) can be multiplied into several blocks, each handling its own NAL bit stream. Adding parallel blocks is not an issue in FPGA circuits, however the number of available logic blocks and speed of the outgoing Ethernet connection represent the limitation.

Additionally, so called NULL packets can be added to the transport stream. NULL packets are packets that are identified with a Packet Identifier (PID) of 0x1FFF and contain only 0xFF values as their payload. Their purpose is to maintain a constant bit rate of the output transport stream by inserting them when no other packet is scheduled to be multiplexed. However, an upper limitation of inserting these packets has to be implemented in the multiplexer control logic. If not, the Ethernet connection can be flooded and the receiver could not handle proper packet reception anymore.

Output of the multiplexer is a 188-bytes-long data vector (ETH_DATA in Fig.3) sent directly to the LocalLink interface /8/ of the Xilinx Tri-Mode Ethernet Media Access Controller (TEMAC) core, together with trigger (ETH_TRIG) and busy (MUX_BUSY) signals. The output represents a single MPEG-2 TS packet; therefore an Ethernet frame can contain only one MPEG-2 TS packet with a single higher-level packet (PSI, PES or NULL). This is actually a quite strict limitation, which was imposed in order to minimize the time of designing the multiplexer core. Nevertheless, performance is not affected significantly because use of Gigabit Ethernet is applied.

Because MPEG-2 TS packets are normally sent through User Datagram Protocol (UDP) over Internet Protocol (IP) and there is no feedback about success of transmission, /5/ defines a special section that is contained in the header of TS named Continuity Counter which is a 4-bit value that increases every new transmission of a packet with the same PID number. Since there is the restriction of a single packet within one Ethernet frame, we can implement the Continuity Counter outside the MPEG-2 TS multiplexer. In our case the Continuity Counter resides in the LocalLink interface module. Consequently we need to send out of the core a flag vector to signalize the PID of the packet being currently transmitted (CC_COUNT in Fig.3) so that the Continuity Counter can increase properly regarding the PID of the packet being sent.

Digital design described in this chapter was realized with FPGA circuit XC5VFX70T-1FFG1136 /9/ that resides on evaluation platform ML507 /10/.

2.2 Hardware configuration

ML507 Evaluation Platform /10/ is a general-purpose development board, based on XC5VFX70T-1FFG1136 that is an FPGA circuit from Virtex-5 FXT Family /9/. The FPGA itself incorporates 12 Digital Clock Managers (DCMs) that can be used to generate various clock signals. 5,328 kilobits of Block Random Access Memory (BRAM) is available and a maximum of 640 single-ended (or 320 differential-pair) input-output (I/O) pins can be utilized. The designer can also bring into use four Gigabit Ethernet Media Access Controller (GEMAC) blocks and 16 High-Speed *Rocket I/O GTX* transceivers.

ML507 board was mainly selected because of the need for rapid prototyping having been faced. The board embeds both clocking components (27 MHz and 100 MHz oscillators) and connectivity periphery; integrated circuit Marvel 88E1111 is connected to GEMAC using Serial Gigabit Media-Independent Interface (SGMII) and acts as the Physical layer of Ethernet IEEE 802.3 connection /11/ together with Halo RJ-45 connector with magnetics. Hardware configuration that has been used is shown in Fig.4.

As seen in Fig.4 all the Network Abstraction Layer (NAL) signals (NAL_BYTE, NAL_VALID, NAL_DONE and NAL_STROB) are brought into circuit from outside (as input pins) while clock signals (CLK_100M and CLK_27M) are captured from on-board oscillators.

When implemented the MPEG-2 TS design takes 23% of Flip-Flops (FF) and 40% of all available slices in XC5VFX70T. Amongst those, 24% are used as Look-Up Tables (LUT) only, 44% as Flip-Flops (FF) only and the rest (32%) utilizing both LUT and FF. Beside logic elements, 3 units of 18k Block Random Access Memory (RAM) are used. Implementation results are shown in Fig.5.

2.3 Operational process

The whole digital design is synchronized to run at 100 MHz main clock (CLK_100M in Fig.3 and Fig.4). Frequency of multiplexing can be modified through an internal signal, however it is intended to leave the setting at its default value in order to achieve timings that are prescribed by /5/.

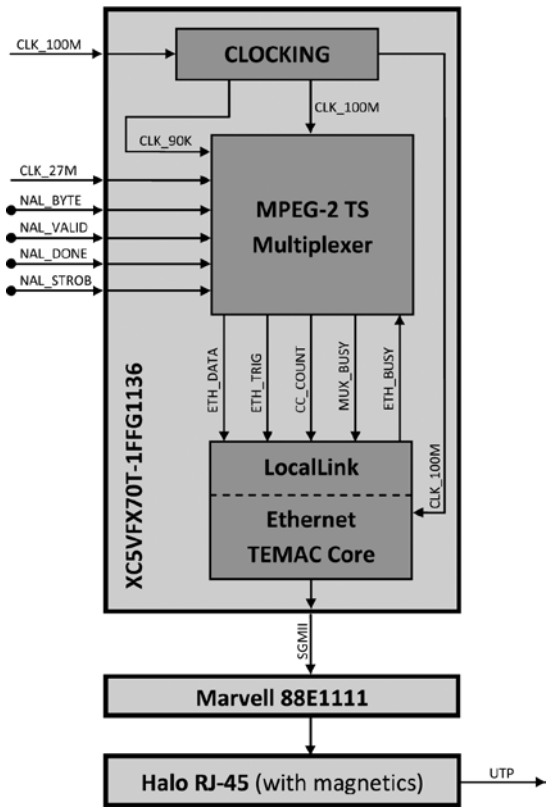

Fig. 4: Hardware configuration.

The Network Abstraction Layer (NAL in Fig.3) handling logic located in Program Block (*Program 1* in Fig.3) is designed to produce a READY internal flag that signalizes a whole Packetized Elementary Stream (PES) packet is waiting in First-In-First-Out (FIFO) buffer to be sent.

Main multiplexer (*MUX* in Fig.3) is designed as a priority switch. If the READY internal flag is detected, PES packet is sent to Ethernet LocalLink interface; else an appropriate table (PAT, PMT, SIT) or counter (PCR) is generated accordingly to timing specifications of /5/ and transmitted to LocalLink interface in the form of a 188-byte vector. If none of the payload-transmitting conditions are met, a NULL packet may be sent instead. Nevertheless, since transmission of NULL packets should be limited in order not to flood the Ethernet connection, not sending anything at all is frequently more appropriate.

The output data vector is then sent to the LocalLink interface of the Xilinx Tri-Mode Ethernet Media Access Controller (TEMAC) core together with flags, where the Continuity Counter (CC) is added and data is encapsulated into the User Datagram Protocol over Internet Protocol (UDP/IP) and sent as an Ethernet frame.

3. Results

Circuit design has been developed using Xilinx ISE Foundation v10.1 K31 (Xilinx, San Jose, USA, 2008) in Very High Speed Integrated Circuit Hardware Description Language (VHSIC HDL – VHDL). Reception of generated multiplexed

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	10,444	44,800	23%
Number used as Flip Flops	10,444		
Number of Slice LUTs	7,720	44,800	17%
Number used as logic	7,708	44,800	17%
Number using O6 output only	7,407		
Number using O5 output only	213		
Number using O5 and O6	88		
Number used as exclusive route-thru	12		
Number of route-thrus	230	89,600	1%
Number using O6 output only	225		
Number using O5 output only	5		
Slice Logic Distribution			
Number of occupied Slices	4,524	11,200	40%
Number of LUT Flip Flop pairs used	13,816		
Number with an unused Flip Flop	3,372	13,816	24%
Number with an unused LUT	6,096	13,816	44%
Number of fully used LUT-FF pairs	4,348	13,816	31%
Number of unique control sets	1,107		
IO Utilization			
Number of bonded IOBs	62	640	9%
Number of bonded IPADs	6		
Specific Feature Utilization			
Number of BlockRAM/FIFO	2	148	1%
Number using BlockRAM only	2		
Total primitives used			
Number of 18k BlockRAM used	3		
Total Memory used (KB)	54	5,328	1%
Number of BUFG/BUFGCTRLs	7	32	21%
Number used as BUFGs	7		
Number of BUFDSs	1	8	12%
Number of BUFRs	1	32	3%
Number of DCM_ADVs	1	12	8%
Number of GTX_DUALs	1	8	12%
Number of TEMACs	1	2	50%

Fig. 5: Implementation results.

test stream was performed on a workstation based on the AMD Athlon64 3000+ Processor (2.0 GHz) with 1.5 GB of DDR SDRAM, equipped with Gigabit Ethernet Network Interface Controller (NIC) Realtek RTL8111B.

To verify the correct reception of User Datagram Protocol (UDP) over Internet Protocol (IP) *Wireshark* software /12/ was used as it performs network protocol analysis. Results from *Wireshark* are shown in Fig.6 where it is noticeable that UDP/IP packets are sent via Ethernet to Media Access Controller (MAC) of the workstation and are properly received. Each received packet consists of 231 bytes of data which is the sum of 188 bytes representing MPEG-2 TS payload data and 43 bytes of MAC/IP/UDP headers. Packets are marked as part of the multicast group with IP address 239.192.1.100 on port 5500.

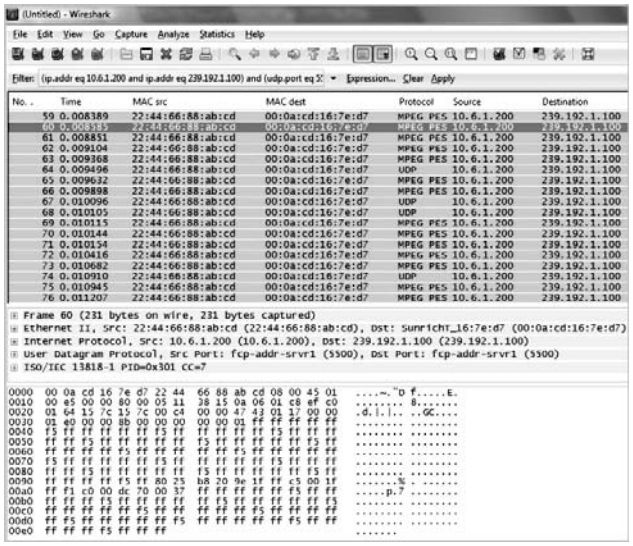

Fig. 6: Network Protocol Analysis results from Wireshark.

Received MPEG-2 TS stream is then isolated using *Wireshark* to include only payload without MAC/IP/UDP headers and after that analyzed using *MPEG-2 Transport Stream Analyzer Enhanced* software by Manzanita Systems, Ltd /13/. Structure of the analyzed stream that has been produced using our MPEG-2 Multiplexer is shown in Fig.7.

PAT Version 0 PID 0x0000	NIT_PID 0x001F			
	Program 1 PID 0x0100	PMT Version 0	Descriptor 0x88 registration_descriptor	
			0x1011 MPEG-4 / AVC / H.264 Video	avc_video_descriptor
			0x1001 PCR	

Fig. 7: Structure of analyzed MPEG-2 Transport Stream that includes sample H.264 video payload.

Ratio of individual elements is also analyzed using *MPEG-2 Transport Stream Analyzer Enhanced* software and is shown in Fig.8 where it can be seen that main part of the stream is taken by video payload. All the other elements occupy less than 2% each. Since table timing limitations prescribed in /5/ are met, such ratio is expected and correct.

To confirm that produced stream is compliant with standard /5/ we performed another analysis. The second tool used is *Stream Analyzer* by *Elecard* /14/. Results of analysis are illustrated in Fig.9.

Stream structure in Fig.9 is the same as in Fig.7; it consists of a single program containing one H.264 video stream. Packet analysis shown in the lower part of Fig.9 also confirms that Presentation Set Access Units (PS AU) of Sequence Parameter Set (SPS) and Picture Parameter Set (PPS) are properly generated, since their decoding is successful.

As mentioned in (2.1.) Program Block (PES in Fig.3) can be multiplied into several blocks in order to multiplex various NAL bit streams into a single MPEG-2 TS. A com-

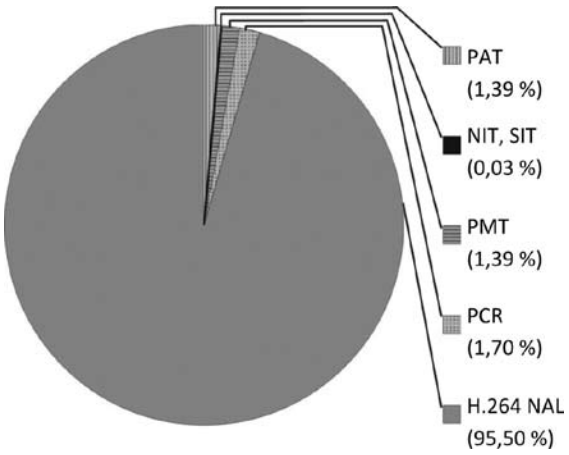

Fig. 8: Ratio of individual elements in the analyzed MPEG-2 Transport Stream.

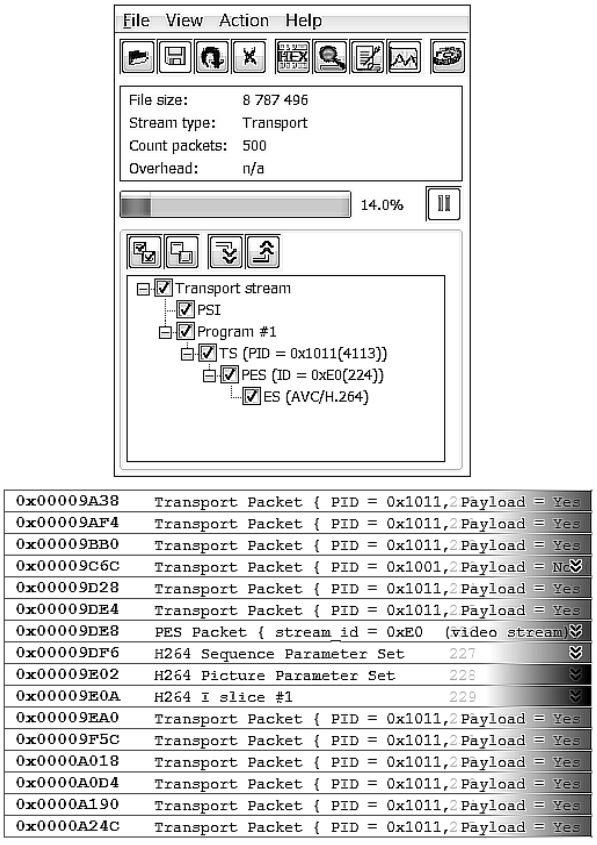

Fig. 9: Analysis of MPEG-2 TS using Stream Analyzer.

parison is shown in Fig.10 where utilization of FPGA circuit XC5VFX70T-1FFG1136 can be seen when only one program block is used (a) or another one is added (b).

As seen in Fig.10, when adding a second program stream, the number of used slices with only Look-Up Table (LUT) basically does not increase; however, increase of Flip-Flop (FF) and combined (LUT with FF) slices is obvious.

Since MPEG-2 TS multiplexer is a time-critical application, timing performance is significant. Timing report that has been generated by the tools /15/ claims all timing con-

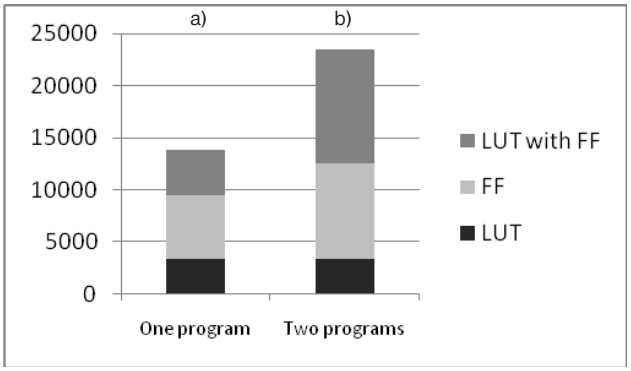

Fig. 10: *LUT and FF utilization comparison.*

straints have been met. There have been 4179 paths and 1003 endpoints analyzed without any errors. Minimum period is 7.609 ns, which represents a maximum frequency of 131.42 MHz.

4. Discussion

This paper discusses design of a Moving Picture Experts Group 2 (MPEG-2) Transport Stream (TS) multiplexer in Field Programmable Gate Array (FPGA) integrated circuit. FPGA allows creating digital designs that are fully programmable while lacking the use of a microprocessor.

The latter is frequently a source of problems, since multiple error-prone situations can occur; first, software can contain bugs that are harder to identify in comparison with a digital design, described in VHDL code. Besides, non-deterministic situations can be provoked as consequence of several microprocessor-related mechanisms (stack, interrupt controllers, exception handlers). All those facts speak in favor of developing a MPEG-2 TS multiplexer using FPGA rather than a microprocessor.

The MPEG-2 TS multiplexer we designed performs in accordance with standard /5/, hence it is fully compatible with hard and/or soft players available on both consumer electronics and professional equipment market.

Upgrade to supporting multiple H.264 streams is possible and effortless. If other content than Network Abstraction Layer (NAL) bit stream shall be multiplexed, only minor modifications in the sampling logic before storage in First-In-First-Out (FIFO) have to be made. The limitations represent the chosen FPGA and the outgoing communication interface, in our case Gigabit Ethernet.

As benefit of this FPGA-based design, use in Application-Specific Integrated Circuit (ASIC) technology could be applied. To make that possible, some improvements should be implemented. Since all stream data (program tables, stream parameters) is stored in FPGA an external interface to an Electrically Erasable Programmable Read-Only Memory (EEPROM) should be considered. The data could, then, be externally programmed, which could lead to a far more flexible system and after all, reduce costs in large quantities of the application.

Acknowledgments

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A PILOT SCENARIO OF SECURE LOCATION-BASED SERVICES IMPLEMENTATION IN A UNIFIED WIFI NETWORK

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Key words: RFID, Location-Based Services, IEEE 802.11 infrastructure, Wi-Fi.

Abstract: In this paper a pilot scenario of secure location-based services implementation in a unified Wi-Fi network based on Cisco networking devices and location aware appliances will be presented. Third party active RFID tags from AeroScout have been used for the location aware tracking of users. We will present an indoor scenario of RF location tracking system implementation based entirely on a unified wireless network IEEE 802.11 infrastructure. In an environment sparse with obstacles a precision accuracy of criteria 1m/50% was achieved.

Pilotni scenarij implementacije varovanih lokalizacijskih storitev v združenem WiFi omrežju

Kjučne besede: RFID, lokacijske storitve, infrastruktura IEEE 802.11, Wi-Fi

Izvleček: V tem članku bomo predstavili pilotski scenarij implementacije varovanih lokalizacijskih storitev v združenem Wi-Fi omrežju zasnovanem na Cisco omrežnih napravah in lokalizacijskih orodjih. Za sledenje položaja uporabnikov so bile uporabljene aktivne značke z radijsko identifikacijo (RFID) podjetja AeroScout. Predstavili bomo scenarij notranje postavitve sistema za sledenje z radijsko identifikacijo, ki temelji izključno na brezžični infrastrukturi IEEE 802.11. V okolju z razmeroma malo ovirami je bila dosežena zanesljivost lokalizacije po kriteriju 1m/50%.

1. Introduction

The term location-based services (LBS) are a recent concept that denotes applications integrating geographic location with the general notion of services /1/. 3GPP strictly distinguishes between location-based services and location services. The latter exclusively deals with the localization of target persons and objects and with making the resulting location data externally available. A location service does not imply the processing of location data in the sense of filtering or selecting location-dependent information or performing other high-level actions as in LBS; it is only responsible for the generation and delivery of location data /2/. Despite the strict definition we will use the term LBS as it appears in most of the literature including location-services based on IEEE 802.11 wireless technology.

The rapid increase in the adoption rate of Wi-Fi coupled with the availability of high quality infrastructure at reasonable cost are key factors behind the outbreak of commercial and academic activity regarding Wi-Fi location-based services. Research and development progress in Wi-Fi location prediction techniques based entirely on IEEE 802.11 infrastructure have facilitated the emergence of indoor RF location tracking systems /3/. With integrated location tracking, enterprise wireless LANs become much more valuable as a corporate business asset.

Maintaining accurate information about the location of individuals or valuable equipment is a complex and ongoing requirement for any large enterprise. To streamline asset tracking and improve workflows for equipment procurement and logistics, new technologies such as radio frequency identification (RFID) are the promising solution on the market /4/.

Offering end-to-end object visibility, the RFID technology seems to revolutionize the supply-chain industry, significantly reducing costs and helping to enable differentiation. With support from such major industry figures as IBM, Wal-Mart, and Procter & Gamble, the momentum is clearly behind this technology. Most deployments are in the pilot phase now, with companies learning about and preparing to use this technology and planning to face the funding issues and business process changes that it will bring.

RFID technology offers the following significant advantages over traditional barcode data collection, although RFID will probably never replace barcodes completely:

- As opposed to barcodes RFID tags identify each item separately
- While barcodes have to be properly oriented Line-of-sight for RFID tags is not necessary.
- Resistant to harsh environments—Barcode life is limited by how long the printed symbols remain readable.
- Can be reprogrammed and reused—New data cannot be written to barcodes.

- Can be read in groups—Barcodes must be read individually, whereas an RFID reader can scan multiple items simultaneously.
- Secures data—Tag memory can be programmed, optionally permanently locked, and can also be erased to protect privacy.

RFID already has numerous commercial applications, such as automobile theft prevention, collecting drive-through tolls, managing traffic, gaining entrance to buildings, automating parking, dispensing goods and books tracking in libraries. As RFID technology solutions mature, companies everywhere will also experience unprecedented supply-chain visibility and information exchange. Currently, EPCglobal, Inc., based on a joint venture between the Uniform Code Council and EAN International, is responsible for developing a single industry standard worldwide to further enable adoption of RFID based on the Electronic Product Code (EPC). The EPC is the favored specification of both Wal-Mart and the U.S. Department of Defense (DoD). This positions EPC as the leader for large supply-chain implementations /5/.

2. RFID Tag Technology

RFID is a means of identifying a person or an object using radio transmissions. This is accomplished by using two primary components: the transponder – an RFID tag located on the object to be identified, which contains a microchip and miniature antenna; and the reader – also known as a detector or interrogator, which communicates with the tag and passes its information on to a controlling system or middleware host /5/.

The majority of RFID tags produced today are passive RFID tags, comprised basically of a microcircuit and an antenna. They are referred to as passive tags because the only time in which they are actively communicating is when they are within the RF field of a passive RFID tag reader.

Another type of common RFID tag is known as the active RFID tag, which usually includes a battery that directly powers RF communication. This onboard power source allows an active RFID tag to transmit information about itself at great range, either by constantly beaconing this information to a RFID tag reader or by transmitting only when it is prompted. Active tags are usually larger in size and can contain substantially more information (because of higher amounts of memory) than do pure passive tag designs /3/.

The combination of both technologies is combined into semi-passive tags which differ from passive tags in that they use an onboard battery to provide power to communication and ancillary support circuits such as temperature and shock monitoring. Although they employ an onboard power source, semi-passive RFID tags do not use it to directly generate RF electromagnetic energy as active RFID's do. Rather, these tags typically make use of backscatter modulation and reflect electromagnetic energy from the RFID reader to generate a tag response similar to that of standard passive tags.

2.1. Active RFID Tags

Active tags are typically used in real-time tracking of high-value assets in closed-loop systems (that is, systems in which the tags are not intended to physically leave the control premises of the tag owner or originator). The relatively higher cost of assets tracked with active RFID tags (as compared to those typically tracked with passive RFID) usually justifies the higher cost of the active tag itself and presents strong motivation for tag re-use. Medical equipment, electronic test gear, computer equipment, reusable containers, and assembly line material-in-process are all excellent examples of applications for active tag technology. Active RFID tags can provide tracking in terms of presence (positive/negative indication of whether an asset is there/missing in a particular area) or real-time location. Active RFID tags are physically larger and typically more costly than passive RFID tags. Most Real Time Location Systems (RTLS) are based on the use of active RFID tag technology.

Active RFID tags can be sub-categorized into those that operate as transponders and those that operate as beacons. Of special interest are the active RFID tags that operate in the unlicensed ISM bands and abide by IEEE 802.11 protocols. These special active RFID tags are known as 802.11 (Wi-Fi) active RFID tags – this type was used for our pilot study.

Beaconing active RFID tags are used in many RTLS systems and are of primary use when the precise location of an asset needs to be tracked anywhere and anytime without the need for pre-positioned interrogators or tag exciters to trigger tag transmission. With a beaconing active RFID tag, a short message payload known as a "beacon" is emitted at pre-programmed intervals with the unique identifier of the RFID tag. This interval is programmed into the tag by the tag owner/user and can be set depending on the degree of criticality associated with tag location updates.

Any 802.11 Wi-Fi active RFID tag that is capable of successfully authenticating and associating with the underlying WLAN infrastructure (and issues probe requests regularly on all channels) should be recognizable by the Cisco LBS solution as a WLAN client (in WCS as a rectangular blue icon, Figure 2).

2.2. Implemented 802.11 Active RFID Tags

802.11 active RFID tags are designed to operate in the unlicensed ISM bands of 2.4 to 2.4835 GHz or 5.8 to 5.825 GHz. Currently manufactured 802.11 Wi-Fi active RFID tags available at publication are limited to 2.4 GHz.

These tags exhibit the characteristics of active RFID tags, but also comply with applicable IEEE 802.11 standards and protocols. Wi-Fi RFID tags can readily communicate directly

with standard Wi-Fi infrastructure without any special hardware or firmware modifications and can co-exist alongside Wi-Fi clients such as laptops, VoWLAN phones, and so on. When powered on, assets equipped with 802.11 Wi-Fi client radios can be tracked natively without the need to have an asset tag attached. Other assets lacking an internal 802.11 Wi-Fi client radio can be tracked via a physically attached 802.11 active RFID tag. A physically attached 802.11 active RFID tag also makes it possible to use the location-aware Cisco UWN to track assets with integrated Wi-Fi client radios when those radios are powered off.

AeroScout T2 Tags were used for the presented scenario of secure LBS. The AeroScout T2 Tag is one of the, if not the leading Wi-Fi tag. The T2 Tag has proven usability, dependability, scalability and flexibility for a wide variety of industries and applications. The T2 messages can be received and processed by standard Cisco Systems wireless access points, keeping infrastructure costs low with a straightforward installation. The T2 is characterized by its long battery life, convenient small size, built-in choke point capabilities and telemetry functionality. T2 Tags enable separate transmission intervals when they are stationary or in motion, which additionally reduces unnecessary network traffic /8/.

3. Location Tracking Approaches

Location tracking and positioning systems can be classified by the measurement techniques they employ to determine mobile device location – localization. These approaches differ in terms of the specific technique used to sense and measure the position of the mobile device in the target environment under observation. Typically, RTLS can be grouped into four basic categories of systems that sense and measure position on the basis of the following:

- Cell of origin (nearest cell)
- Distance (lateration)
- Angle (angulation)
- Location patterning (pattern recognition)

An RTLS designer can choose to implement one or more of these techniques. This may be clearly seen in some approaches attempting to optimize performance in two or more environments with very different propagation characteristics. An example of this is an RTLS system attempting to yield optimal performance for both indoor and outdoor applications by using two different techniques. It is not unusual to hear arguments supporting the case that a fifth category should exist to include those RTLS systems that sense and measure position using a combination of at least two of the four techniques mentioned above. Regardless of the underlying positioning technology, the "real-time" nature of an RTLS is only as real-time as the most current timestamps, signal strengths, or angle-of-incidence measurements. The timing of probe responses, beaconing rates, and location server polling intervals can influence discrepancies seen between actual and reported device position from reporting interval to reporting interval /3/.

4. Accuracy and Precision of the Location Based Services Solution

With proper deployment according to the best practices /3/ the accuracy and precision of the tested LBS solution in indoor deployments is represented as follows:

- Accuracy of less than or equal to 10 meters, with 90 % precision
- Accuracy of less than or equal to 5 meters, with 50 % precision

In other words, given proper design and deployment of the system, the error distance between the reported device location and the actual location should, in 90 % of all reporting instances, be 10 meters or less. In the remaining 10 % of all reporting instances, the error distance may be expected to exceed 10 meters. Note that these specifications apply only to solutions using RF Fingerprinting; namely, the use of a WCS licensed for location usage (with or without a location appliance).

For applications that require better performance than an accuracy of 10 meters with 90 % precision, the Cisco LBS solution can deliver accuracy of 5 meters or less but with 50 % precision. Stated another way, in 50 % of all reporting instances, it can be reasonably expected that the error distance between the reported and the actual location exceeds 5 meters. The location inspection tool can display various levels of accuracy and precision from 2 m to 100 m along with which areas of the inspected environment can meet these accuracy levels.

5. The unified wireless network setup and configuration

The network infrastructure was build from scratch. No appropriate RFID capable or compatible equipment was previously available. The network environment was setup at the annual Cisco EXPO conference (2007). The proof of concept for wireless appliances was targeted for a small to medium enterprise (50-100 employees).

The WAN connection was firewalled with a software based IOS firewall on a Cisco 1800 Series Integrated Services Router. The integrated services routing architecture of the Cisco 1800 Series offers features that provide the complete functionality and flexibility to deliver secure Internet and intranet access. It is ideal for small to medium-sized businesses and small enterprise branch offices enable businesses to reduce costs by deploying a single, resilient system for fast, secure, delivery of multiple mission-critical business services. As aggregation switch a Cisco Series 3560 switch was implemented. The Cisco Catalyst 3560 Series are next-generation energy-efficient Layer 3 Fast

Ethernet switches. For the access switching nodes basic models L2 Cisco Catalyst Express 500 Series of switches were used. Cisco Catalyst Express 500 Series switches meet the needs of growing businesses with up to 250 employees. This family of Layer 2-managed Fast Ethernet and Gigabit Ethernet switches offers non-blocking, wire-speed performance and provides a secure network foundation optimized for data, wireless, and IP Communications (Figure 1,Table 1).

Table 1: Used equipment

Cisco1812	Router Series 1800	1
WS-C3560G	L3 switch with 24 10/100/1000 ports and 2GE SFP ports	1
WS-CE500	L2 switch with 24 ports and 24 PoE	2
AP1010	Lightweight Access Point	6
LOC2710	Location Appliance	1
WLC4402	Wireless Location Controller (12 AP)	1
WCS	Wireless Control System	1

Lightweight access points Cisco 1000 Series were implemented. The Aironet 1000 Series lightweight access points are specifically designed for operation with Cisco Wireless LAN Controllers and the Wireless Control System management tool. They provide dual band support for both 802.11a, 802.11b and 802.11g, simultaneous air monitoring for dynamic, real time RF management. In addition, the Lightweight Access Points handle time-sensitive functions, such as L2 encryption, that securely support voice, video, and data applications in wireless LANs.

The Cisco 4400 Series Wireless Controller for AP management was installed. The Wireless LAN Controllers is designed for medium-to-large enterprise facilities. The Cisco 4402 with two Gigabit Ethernet ports comes in configurations that support up to 12, 25, and 50 lightweight access points. It provides one expansion slot that can be used to add enhanced functionality, such as VPN termination and other future capabilities.

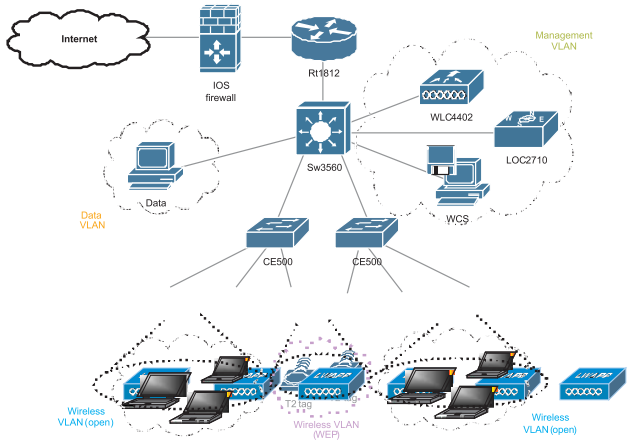

Fig. 1: The implemented location-aware unified wireless network architecture.

Next the Cisco Wireless Location Appliance was integrated. The 2710 Wireless Location Appliance simultaneously tracks thousands of 802.11 wireless devices from directly within a WLAN infrastructure, increasing asset visibility and control of the RF environment. Additionally, the appliance provides location-based alerts for business policy enforcement and records rich historical location information that can be used for location trending, rapid problem resolution, and RF capacity management.

Finally the Wireless Control System was installed on a Windows 2003 server. The Cisco Wireless Control System (WCS) is a Cisco Unified Wireless Network Solution management tool that adds to the capabilities of the web user interface and command line interface (CLI), moving from individual controllers to a network of controllers. WCS includes the same configuration, performance monitoring, security, fault management, and accounting options used at the controller level and adds a graphical view of multiple controllers and managed access points.

Light-Weight Access points forward information to WLAN controller (WLC) regarding the detected signal strength of any WLAN clients (Wireless VLAN) and asset tags (Wireless WEP VLAN). At least three access points detect the asset tag's transmission. It is forwarded to the WLC to which the detecting access points are registered. In normal operation, access points focus their collection activities for this information on their primary channel of operation, going off-channel and scanning the other channels in their regulatory channel set periodically. The collected signal strength information is forwarded to the WLC to which the access point is currently registered, which aggregates the information such as battery status and tag or asset telemetry. The location appliance (LOC) uses SNMP to poll the controller (or controllers if there are many) for the latest signal strength information for each tracked category of device /6/.

All implemented hardware was appropriately configured using /9/, /10/, /11/, /12/, /13/, /14/.

6. Inspecting Location Quality and Precision

A new capability introduced with the latest Wireless Control System (Cisco WCS) and using the location appliance is Location Inspection.

Location inspection is the ability to directly validate the performance of the created path loss models via the calibration process. Unlike the location planner or location readiness tools, which are purely predictive in nature, when location quality is inspected, predicted locations to actual physical locations are directly compared and graphically expressed using the accuracy of the path loss model. With the use of the calibration model and the *location inspection tool*, it can be quantified whether achieving the 10 m/90 % performance metric in the environment and if so, whether it has been uniformly achieved throughout the area. Location inspection allows a topography preview of areas where the location performance may be below the performance

expectations as well as those where it is clearly exceeding them (Figure 2).

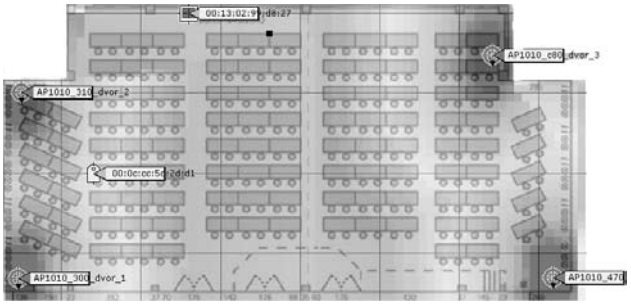

Fig. 2: On-Demand WLAN Client Localization using WCS (clients are depicted with blue whereas RFID tags with yellow).

Location inspection uses the signal strength information recorded during data collection and the path loss model to compute estimated location. It does this for each data collection point that was recorded. These estimated locations are then compared against the actual location coordinates (also recorded during data collection). The results of the comparison are displayed in a graphical format indicating the level of precision available throughout the environment for various selected accuracy levels.

The performance metric often used having the most familiarity and significance is accuracy. Accuracy typically refers to the value of the received information. Location accuracy refers particularly to the quantifiable error distance between the estimated location and the actual location of the mobile device.

In most real-world applications, however, a statement of location accuracy has little value without the ability of the solution to repeatedly and reliably perform at this level. Precision is a direct measure reflecting on the reproducibility of the stated location accuracy. Any indication of location accuracy should therefore include an indication of the confidence interval or percentage of successful location detection as well, otherwise known as the location precision /7/.

Measurements have been performed to estimate the deviation of reported and actual position of targets compared to measurement accuracy as regarding the 10 m/90 % performance metric criteria in the environment under observation and whether it has been uniformly achieved throughout the area.

For the precision estimation of measurements a straightforward arithmetic mean with mean absolute error (MAE) estimation was used. Additionally all measurements in column 2 (Table 2) were rounded up, thus the actual error is even lesser.

$$\overline{x} = \frac{1}{n}\sum_{1}^{n} x_i \qquad \varepsilon_i = \left|\overline{x} - x_i\right| \tag{1}$$

where x_i is the actual measurement and ε_i the absolute error.

Table 2: Accuracy measurements of objects reported by the LBS System compared to a reference grid.

Measurement Nr.	Distance (m)	Error (m)
1	2	-0,79
2	3	0,21
3	4,5	1,71
4	2	-0,79
5	2	-0,79
6	0,5	-2,29
7	4	1,21
8	2,5	-0,29
9	3	0,21
10	3,5	0,71
11	2,5	-0,29
12	4	1,21
13	3	0,21
14	1,5	-1,29
15	2,5	-0,29
16	3	0,21
17	4	1,21
MAE (m)	2,79	

It is evident that all predicted measurements in the environment under inspection were clearly within the guaranteed 10m/90% criteria. In our case with an area including very little obstacles even the 1m/50% criteria could be met. Also measurements have been performed repeatedly to estimate the confidence interval (Figure 3).

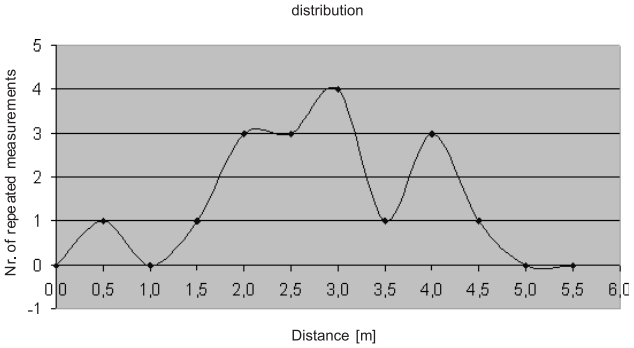

Fig. 3: The confidence interval estimation.

In addition measurements not fulfilling the triangle AP criteria were checked. As expected the measured position of the targets and their actual position were nondeterministic using implemented distance based or TDoA (Time Difference of Arrival) lateration techniques. Nevertheless rude estimation with RSS (Received Signal Strength) with appropriate path loss model is still possible /3/.

7. Conclusion

A Pilot Scenario of Secure Location-Based Services Implementation in a Unified WiFi Network was presented. State of-the-art hardware with the unified wireless Cisco network architecture with IEEE 802.11 infrastructure was used. The benefits of such an implementation are in using the existent

wireless environment extending it with additional hardware for implementation of new services for localization. Localization of targets well beyond the guaranteed 10m/90% criteria was achieved.

Pilot scenarios as the one presented or simple deployments can perform well with standard IP networks without complete upgrades. Localization results even much below the criteria 10m/90% can be achieved in environments sparse with obstacles. An accuracy of 1m/50% was demonstrated. However, network features can be used to optimize RFID deployments. Functionality such as network availability and scalability, simplified network provisioning, network security, and network quality of service are enhancements that advanced deployments will require. Choosing the correct network infrastructure in the beginning of the design will help to ensure the investment protection of RFID networks.

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A NOVEL CMOS DEFUZZIFICATION CIRCUIT EMPLOYING CURRENT DIFFERENCING BUFFERED AMPLIFIER BASED CURRENT-MODE MULTIPLIERS

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Key words: Current Differencing Buffered Amplifier (CDBA), Defuzzification circuit, current-mode multiplier

Abstract: In this paper, design and analysis of a novel current-mode defuzzification circuit is presented. The proposed defuzzification circuit is based on current-mode four-quadrant multipliers that have been constructed with simple current squarer and current differencing buffered amplifier (CDBA). This circuit has capable of high linearity, simple structure, and wide input current range. The defuzzification circuit has been simulated and verified by PSPICE with MIETEC 1.2 μm parameters. The circuit is suitable for using Centre Of Gravity (COG) method in current-mode fuzzy logic controllers. The purpose of this paper is to present an alternative approach for current-mode defuzzification circuit design.

Novo FLC CMOS vezje

Kjučne besede: CDBA vezje, mehčalno vezje, ojačevalniki toka

Izvleček: V prispevku predstavimo načrtovanje in analizo inovativnega vezja FLC (Fuzzy Logic Circuit). Mehčalno vezje (defuzzification circuit) je linearno in ima enostavno strukturo in vhodni tok v širokem intervalu. Vezje smo simulirali s programom PSPICE s parametri MIETEC 1,2um. Namen prispevka je prikazati drugačen pristop k načrtovanju vezij FLC.

1. Introduction

The defuzzification circuit or defuzzifier is one of the most important units in the fuzzy logic controllers (FLC). There are two ways to implement a defuzzifier: the analogue approach and the digital approach. The analogue approach presents several advantages in front of digital ones, especially regarding speed of processing, power dissipation and functional density. Moreover, the analogue circuit based fuzzy blocks perform continuous-time processing and they have the particularly to be well compatible with sensors, actuators and all other analogue signals /1-3/. On the other hand, digital circuits are superior to analogue counterpart in accuracy, extendibility, and easy of design automation /4-5/.

The centre of gravity (COG) is the most popular defuzzification method in FLC. Various defuzzification circuits using COG method are described in literature /6-9/. A high-speed digital defuzzification circuit based on BiCMOS technology has been proposed in /7/ but the fabrication cost is high. The other defuzzification circuit design with current-mode analogue circuits was proposed in /8/. However, both frequency range and speed of these circuits are low. Another defuzzification circuit using resonant tunnelling diodes is proposed by Tang and Lin /9/. Their design reduces circuit complexity compared with conventional digital and analogue signal processing circuits.

Recently, a new five-terminal active current-mode element, called a current differencing buffered amplifier (CDBA), has received much attention in the electronics community /10-12/. It can be operated in both current-mode and voltage-mode in a wide frequency range and can also be implemented with CMOS technology. Differential nature of this element at the input makes it especially suitable for various analogue signal-processing applications demanding high speed, high bandwidth and simple implementation.

In this paper, a new defuzzification circuit employing CDBA based current-mode multipliers is presented. The proposed circuit is built using current-mode four-quadrant multiplier includes simple current squarer and CDBA, and current-mode reverse function circuit as divider unit.

The outline of this paper is as follows. Section II briefly defines a block diagram of proposed defuzzification circuit, then the current squarer and Current Differencing Buffered Amplifier (CDBA) that composed of current-mode four-quadrant multiplier are theoretically described in detailed. Also, the current-mode reverse function circuit is described as the division unit of defuzzification circuit. Section III evaluates a proposed four-quadrant multiplier, reverse function circuit and defuzzification circuit with PSPICE simulation experiments. In Section IV, the overall conclusions are given.

2. Circuit Description

The COG method in current-mode is expressed as

$$I_{out(COG)} = \frac{\sum_{i=1}^{n} I_{\mu i}.I_{ci}}{\sum_{i=1}^{n} I_{\mu i}} \quad (1)$$

where n represents the number of fuzzy sets on the universe of discourse, $I\mu_i$ and Ic_i represent the *membership function output* and *support* value of the *i* th fuzzy set, respectively. Eq. (1) can be arranged with current values of input/output variables as follows.

$$I_{out} = \frac{I_{\mu 1}.I_{c1}}{I_{\Sigma}} + \frac{I_{\mu 2}.I_{c2}}{I_{\Sigma}} + ... + \frac{I_{\mu n}.I_{cn}}{I_{\Sigma}} \quad (2)$$

where I_{Σ} is equal to $\sum_{i=1}^{n} I_{\mu i}$

The input and the output characteristics of each term in equation (2) can be defined by using current-mode four-quadrant multiplier blocks. Each block in Eq. (2) is computed as follows:

$$I_{out} = \frac{I_x I_y}{I_w} \quad (3)$$

where I_x, I_y, I_w, and I_{out} variables are corresponded with $I\mu_i$, Ic_i, I , and I_{oi} , respectively. The block diagram of defuzzification circuit processing unit in Eq. (3) is implemented with two multipliers and one current-mode reverse function block as shown in Fig.1.

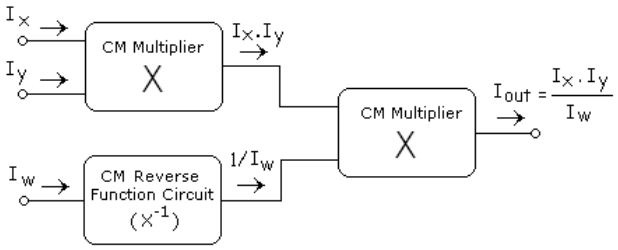


Fig. 1: The block diagram of defuzzification circuit processing unit

The building blocks of current-mode multiplier circuit are shown in Fig. 2. This multiplier circuit is consists of two cascode current mirrors, one modified current differencing amplifier (CDBA), and three current squarer units.

The modified circuit structure of the CDBA in /10/ and circuit symbol is shown in Fig. 3 (a) and (b), respectively. The characteristic equation of this element can be given as

$$V_p = V_n = 0, \quad I_z = I_p - I_n, \quad V_w = V_z \quad (4)$$

Here, current through z-terminal follows the difference of the current through p-terminal and n-terminal. Input terminals, p and n, are internally grounded. A possible CMOS realization of CDBA consisting of a differential current

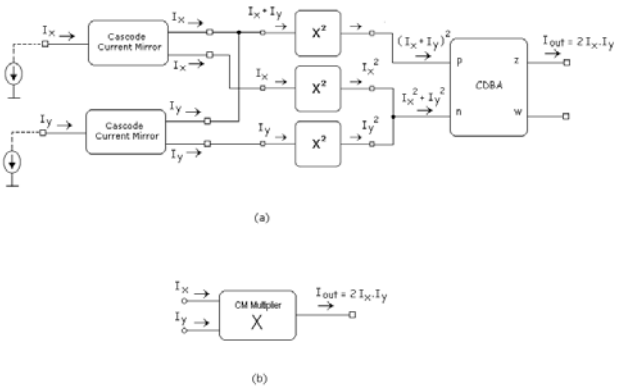


Fig. 2: (a) The building blocks of current-mode multiplier circuit (b) its symbol

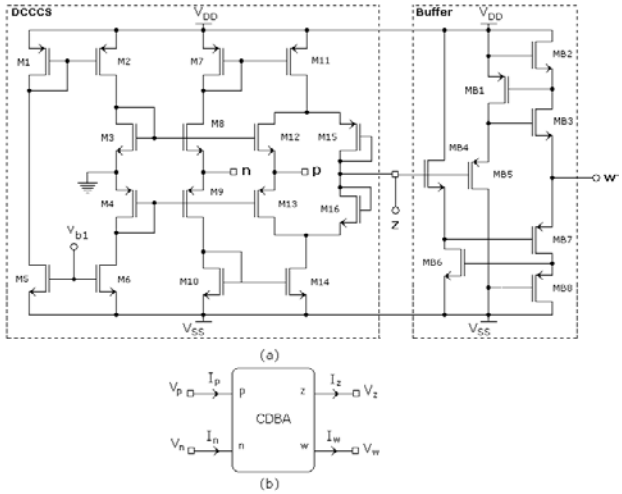


Fig. 3: (a) Simplified CMOS implementation of modified CDBA and (b) its symbol (V_{DD}= -V_{SS}= 2.5 V and V_{b1}= -1.45 V)

controlled current source (DCCCS) followed by a voltage buffer is shown in Fig. 3 (a).

2.1. Current Squarer

The current squarer circuit into four-quadrant multiplier is shown in Fig. 4.The MOSFETs, M1, M2, and M3, are the identical transistors, working in saturation region. In condition that $V_{GS}>V_T$ and $V_{DS}>V_{GS}-V_T$, the expression of drain current for the simple MOS transistor operating in saturation region is

$$I_{ds} = \mu C_{ox} (\frac{W}{L})(V_{GS} - V_T)^2 \quad (5)$$

$$I_{ds} = K(V_{GS} - V_T)^2 \quad (6)$$

Where **K** is trans-conductance parameter, and μ, $C_{ox,}$ W, and L stand for carrier effective mobility, gate oxide capacitance per unit area, width, and length of the channel, respectively /13/.

In Fig. 4, V_B and I_{in} are the dc bias voltage and input current, respectively. If all MOS transistors operate in saturation

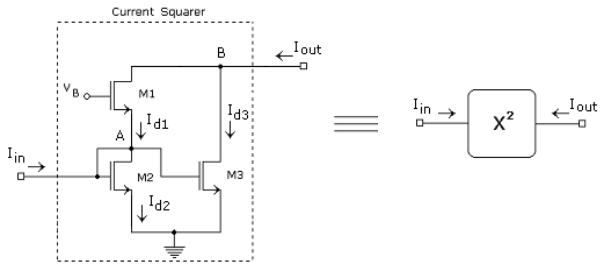


Fig. 4: The current squarer circuit and its symbol

region and trans-conductance parameters of all transistors are identical, i.e., $K_1=K_2=K_3=K$, then bias voltage V_B is given by

$$V_B = V_{gs1} + V_{gs2} \tag{7}$$

If KCL is applied to A and B nodes, output current I_{out} can be obtained as follows:

$$I_{d2} = I_{d3} = I_{in} + I_{d1} \tag{8}$$

$$I_{out} = I_{d1} + I_{d3} \tag{9}$$

Using equations (4)- (5), I_{out} can be derived as follows

$$I_{out} = 2I_{d1} + I_{in} \tag{10}$$

The voltage of node A, V_A, is equal to V_{gs2} and the drain current of M_1 transistor can be obtained by using equation (1) and (2).

$$V_A = V_{gs2} = \sqrt{\frac{(I_{in} + I_{d1})}{K}} + V_t \tag{11}$$

$$I_{d1} = K\left[(V_B - V_{gs2}) - V_t\right]^2 \tag{12}$$

Using equation (7) into (8), the drain current of M_1 transistor, I_{d1}, can be obtained as follows:

$$I_{d1} = \frac{I_{in}^{\,2}}{4K(V_B - 2V_t)^2} + \frac{K}{4}(V_B - 2V_t)^2 - \frac{I_{in}}{2} \tag{13}$$

If equation (9) is placed into equation (6), the output current I_{out} is given by

$$I_{out} = \frac{I_{in}^{\,2}}{2K(V_B - 2V_t)^2} + \frac{K}{2}(V_B - 2V_t)^2 \tag{14}$$

Where K transconductance parameter, bias voltage, V_B, and threshold voltage, V_t, are constant values and are chosen by designers.

Here, $\frac{K}{2}(V_B - 2V_t)^2$ expression in equation (10) is similar to drain-to-source current of MOSFET transistor in saturation region. Therefore, this current can be supplied from a current mirror structure. If this expression is equal to constant bias current as I_B via current mirror, then output current, I_{out}, can be obtained as follows:

$$I_{out} = \frac{1}{4I_B} I_{in}^{\,2} + I_B \tag{15}$$

From (11), the circuit operates as squarer circuit with the dc output offset current of I_B. The offset current is cancelled by adding the current source to the output terminal.

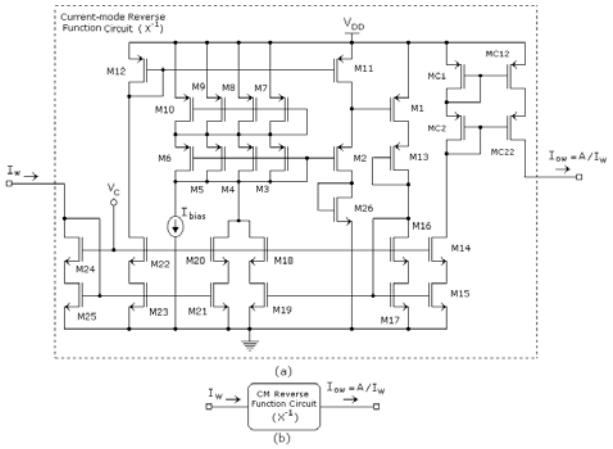


Fig. 5: (a) Current-mode reverse function circuit and (b) its block representation

Figure 5 shows current-mode reverse function (1/x or x^{-1}) circuit as divider operator in proposed defuzzification unit. This circuit is basically current squarer/divider circuit. The reverse function circuit output current I_{out} is obviously given by

$$I_{out} = \frac{I_{bias}^{\,2}}{4I_w} \tag{16}$$

$$I_{out} = \frac{A}{I_w} \quad \text{for} \quad A = \frac{I_{bias}^{\,2}}{4} \tag{17}$$

Here, I_{bias} is corresponded to squaring current and it has been fixed value as dividing coefficient, i.e. $A = I_{bias}^{\,2}/4$. Thus, the circuit can be converted to divider operator by fixing squaring current I_{bias}. In this circuit, the voltage-translinear loops are formed by transistors M1–M10; note that the bulk terminals of these transistors are connected to their sources, thus avoiding the body effect. M13 and M26 are diode-connected transistors included for decreasing the channel-length modulation effect in M1 and M2, respectively. Transistors M11–M12 form a current mirror and M14–M25 constitute high-swing cascode current copiers employed for injecting the required combinations of currents into the voltage-translinear loop. The circuit is designed for VDD = 2.5 V and V_C = 1.3 V /14/.

3. Simulation Results

The behaviour of the implemented CDBA and simple current squarer based defuzzification circuit was confirmed with 1.2 µm MIETEC CMOS process parameters by PSPICE simulations. The all device dimensions of the squarer circuit in Fig. 4 are identical and W/L= 120 µm/2 µm. The transient analysis results of current-mode reverse function circuit are shown in Fig. 6. Here, I_{bias} current is corresponded to

I_z current in current squarer/divider circuit is presented by /14/. This current is fixed value (50 µA) in our proposed defuzzification circuit for using as divider operator.

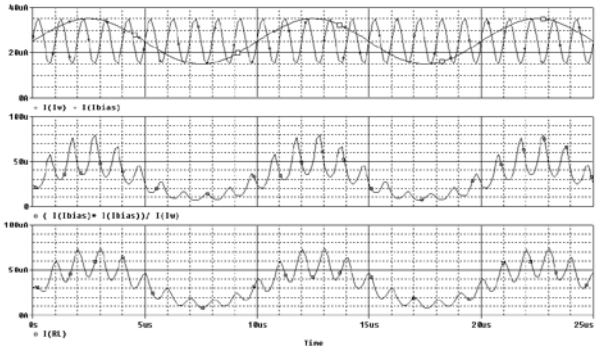
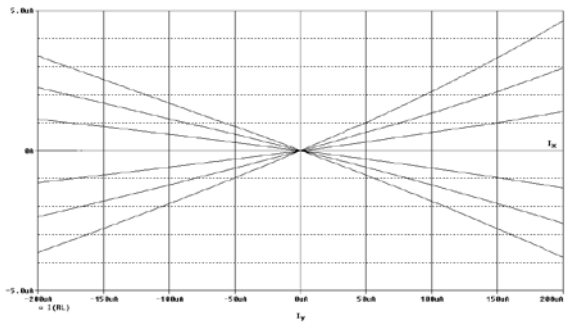


Fig. 6: The transient analysis result of current-mode reverse function circuit. Input signals (top), the calculated result of current-mode reverse function (middle), the circuit output (bottom) /14/.

The PSPICE-DC and transient analysis results of multiplier circuit (Fig.2 (a)) are shown in Fig. 7 (a) and (b), where I_y(i.e. I_{ci} support value) is [-200 µA; +200 µA] in amplitude, I_x (i.e. $I_{\mu i}$ membership value) is varied DC signal forms between [-15 µA; +15 µA] in 5 µA steps. In Fig. 7 (b), the frequencies of input currents, I_x and I_y, are selected 3 and 5 MHz, respectively. The error change of between calculation result and circuit output is about %1. So, this result is shown both wide

a)



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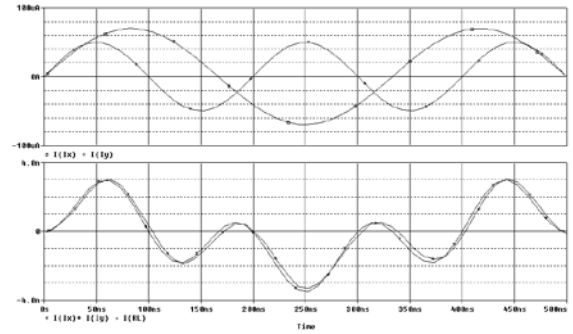

Fig. 7: (a) DC waveform of CDBA and current squarer based current-mode four-quadrant multiplier (b) Transient response of four-quadrant multiplier. Input current signal (top) and together calculated graph and circuit output (bottom) (frequencies of I_x and I_y are 3 and 5 MHz, respectively.)

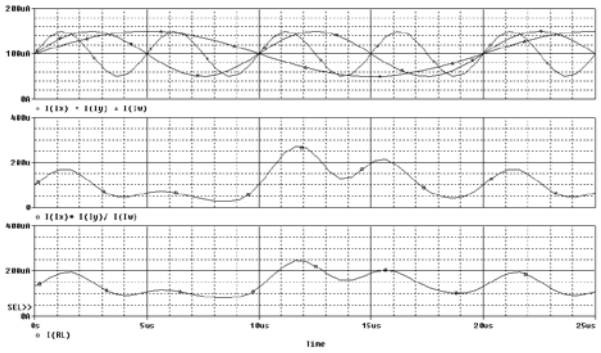

Fig. 8: The simulation results of current squarer and CDBA based defuzzification circuit. Input current signals (top), the calculation result of defuzzification process (middle), and the output waveform of proposed defuzzification circuit (bottom).

input current range and high frequency features of proposed circuit because of using CDBA structure in current-mode four-quadrant multipliers. In the simulations of proposed defuzzification circuit, the circuit parameter values are determined as follows: V_{DD}= -V_{SS}= 2.5 V, -200 µA ≤ I_y (I_{in}) ≤ +200 µA, -15 µA ≤ I_x ($I_{\mu i}$) ≤ 15 µA, V_{b1}= -1.45 V, R_L=1 KΩ.

The mathematical and simulation results of defuzzification processing unit are shown with together in Fig. 8. Three input sinusoidal signals (I_x, I_y, and I_w) are applied defuzzification processing unit. The simulation result of defuzzification circuit is verified to calculation result as shown in Fig. 8.

4. Conclusions

A novel current-mode defuzzification circuit using Centre of Gravity (COG) method has been designed and analyzed. Its behaviour was confirmed by PSPICE simulation experiments with MIETEC 1.2 µm CMOS process. The implemented defuzzification circuit is based on current-mode four-quadrant multipliers and modified current squarer/divider circuits as divider operator in defuzzification processing unit. The proposed current-mode defuzzification circuit has capable of high linearity, simple structure, and wide input current range. The features are verified with PSPICE simulation experiments. The defuzzification circuit is suitable for CMOS fuzzy logic controllers with Centre Of Gravity (COG) method.

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2.8 GHZ – 5.7 GHZ VERY FAST UWB CCO USING DISCRETE-PACKAGED SIGE RF TRANSISTORS

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Key words: current-controlled oscillator, phase noise, modulation bandwidth, discrete-packaged SiGe transistors

Abstract: A simple and successful design for ultra-wideband current-controlled oscillator (UWB CCO) is presented. The circuit uses discrete-packaged transistors and lumped elements. The tuning range of the CCO exceeds one octave in the lower microwave frequency range with reasonable phase-noise performance. Further it achieves a very high tuning speed: its 3 dB FM bandwidth exceeds 400 MHz.

2,8 GHz – 5,7 GHz zelo hiter ultra širokopasoven tokovno krmiljen oscilator z diskretnimi SiGe RF tranzistorji

Kjučne besede: tokovno krmiljen oscillator, fazni šum, modulacijska pasovna širina, diskretni SiGe tranzistorji

Izvleček: V prispevku je predstavljena preprosta in učinkovita izvedba ultra širokopasovnega tokovno krmiljenega oscilatorja (ang. UWB CCO) izdelanega z diskretnimi elektronskimi elementi. Frekvenčni razpon oscilatorja, ob sprejemljivih vrednostih faznega šuma, presega eno oktavo v spodnjem mikrovalovnem frekvenčnem področju. Njegova zasnova omogoča izredno hitro modulacijo; 3 dB frekvenčna modulacijska pasovna širina presega 400 MHz. Osnovna aplikacija predstavljenega oscilatorja je bila simulacija uklenitve kompleksne elektro-optične fazno sklenjene zanke (ang. OPLL), v kateri je oscilator nadomeščal laser. Oscilator je sicer mogoče uporabiti tudi v hitrih mikrovalovnih vezjih (sklopi s fazno sklenjeno zanko) in drugih aplikacijah širokega frekvenčnega spektra.

1 Introduction

UWB voltage or current-controlled oscillators /1-3/ found place in many applications of transmitting data over a wide spectrum with high data rates and in some other special applications. In this paper, we propose a current-controlled oscillator (CCO) using discrete-packaged SiGe:C transistors, capable of very fast tuning over a wide frequency range. Our particular application of the described CCO was the simulation of a complicated electro-optical system in a very fast electro-optical phase-locked loop (OPLLs) /4/, where the CCO simulated an yet-to-be-developed laser.

2 Circuit design

The core of proposed CCO consists of a cross-coupled NPN transistor pair T1 and T2 (see Fig. 1), forming a negative-impedance circuit (NIC) and providing positive feedback to produce oscillation. The NIC is loaded by an external lumped inductor to determine the frequency of the oscillation. DC bias current is fed through the center tap of the inductor on the positive side and through the 56 Ω resistor to the common-emitter node on the negative side. In this CCO circuit no varactor diodes are employed.

The external inductor includes two pieces of thin copper foil soldered to an unetched part of a FR4 printed-circuit board as shown on Fig. 2. This inductor also performs as a transistor holder. The two packaged transistors are first soldered together and then held at a specified height above the FR4 board by the inductor. The inductance value is selected by the height of both transistors above the FR4 board. A recommended height for stable and continuous oscillation was found about 2.5 mm above the ground plane.

Lowering the transistors reduces the inductance and increases the operating frequency. Unfortunately this also narrows the tuning range of the CCO and may produce unstable operation, mainly due to the parasitic inductances of the bonding wires inside the transistor packages.

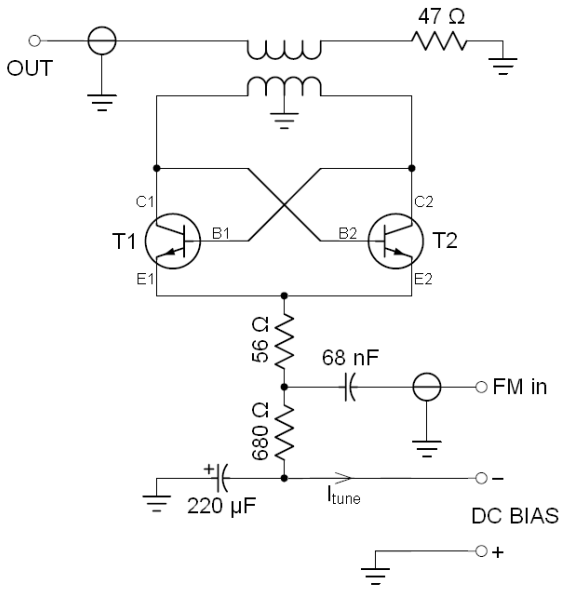

Fig. 1 Ultra-wideband current-controlled oscillator (UWB CCO) circuit design

The CCO is tuned by changing the bias current I_{tune} through 680 Ω and 56 Ω resistors. A 56 Ω resistor is also used for good impedance matching on the FM input. The CCO output is inductively coupled. This coupling is intentionally made very loose to avoid affecting the CCO tuning performance. The output power can be restored by an additional buffer amplifier if required. A practical solution for the output coupling is a 47 Ω resistor installed above the transistors where the resistor leads act as a coupling loop.

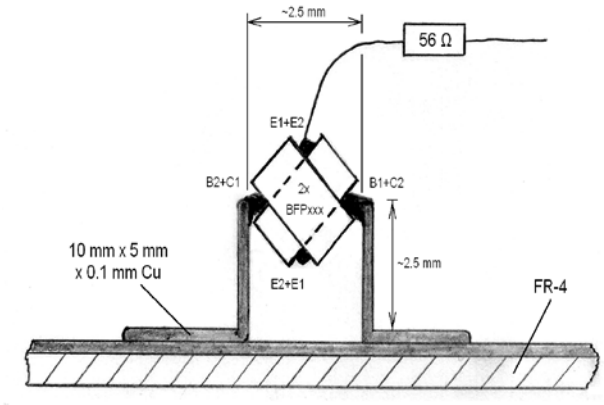

Fig. 2 Transistor mounting in U-shaped Cu holder on FR-4 laminate; the inductance value is selected by the height of both transistors above the FR4 board

3 Measurement results

Practical experiments were made with several different silicon, SiGe and SiGe:C transistors from the BFP series manufactured by Infineon in common-emitter packages SOT-343 and TSFP-4. All CCOs were built on 1-mm thick FR-4 laminate and shielded in a metal box. Microwave-absorber foam was placed above the circuit inside the box to suppress parasitic resonances. Lead-acid batteries were used as noise-free power sources for phase-noise measurements. Transistor types BFP405, 420, 520, 620 and 740 were tested. The best results were achieved with the SiGe:C transistor BFP740 as shown on the following figures.

The CCO tuning curve and output power are shown on Fig. 3. The frequency of the CCO changes from 5.72 GHz to 2.85 GHz when tuning current changes from 1.4 mA to 48 mA. The output frequency is inversely proportional to the operating current resulting in a hyperbolic tuning curve. The tuning slope therefore changes from 100 MHz/mA at the upper frequency limit down to 47 MHz/mA at the lower frequency limit.

The output power stays around –22 dBm in the frequency range from 2.85 GHz to 4.0 GHz and decreases down to –40 dBm at the upper frequency limit.

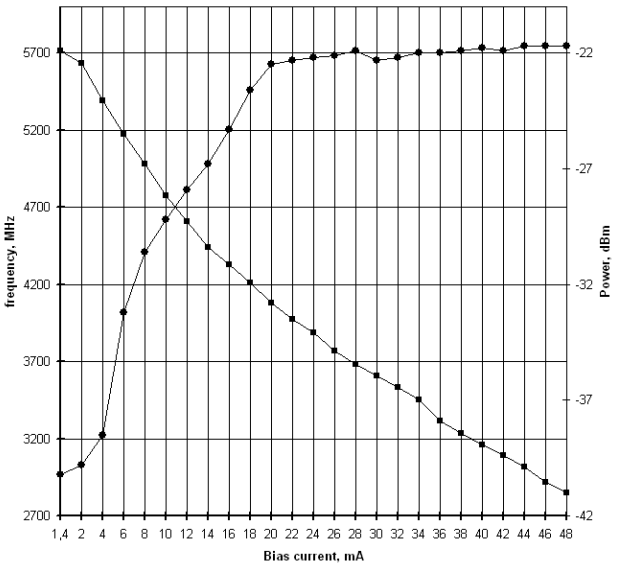

Fig. 3 Frequency and output power against tuning current I_{tune}
■ – frequency
● – power

The CCO phase noise was measured with a HP8565 Spectrum Analyser and is shown on Fig.4. The phase noise increases towards the upper frequency limit where the operating current is very low and the CCO shows a tendency to turn off and/or jump into another oscillation mode due to transistor-package parasitics.

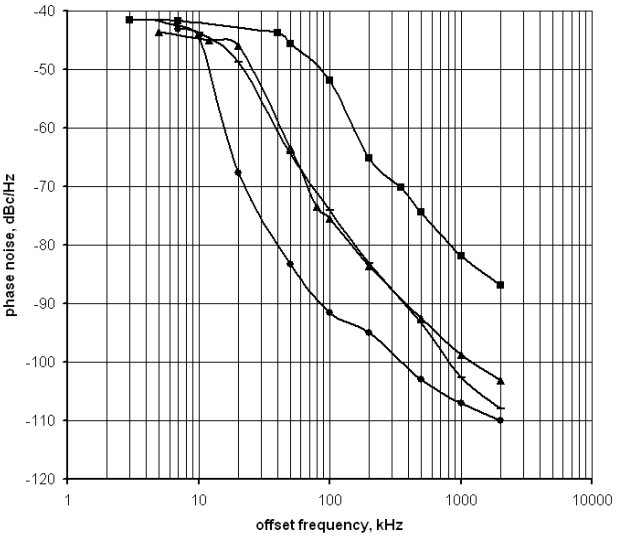

Fig. 4 Measured phase noise at different oscillation frequencies
■ – oscillation frequency @ 5.7 GHz
▲ – oscillation frequency @ 5.0 GHz
▬ – oscillation frequency @ 4.0 GHz
● – oscillation frequency @ 3.0 GHz

The tuning speed of the presented CCO was measured as the frequency-modulation bandwidth that is commonly referred to in the industry /5/. An Agilent E4438C Signal

Generator was connected to the FM input while the CCO output was monitored on a HP8565 Spectrum Analyser. The measured 3 dB modulation bandwidth of the proposed CCO exceeded 400 MHz. In other words, the presented CCO is more than 10-times faster than commercially available varactor-tuned VCOs.

4 Conclusion

A novel, discrete-component design of a CCO achieves a wide tuning range and fast modulation capability using standard, low-cost electronic components. Its phase noise is sufficiently low to allow several different wide-tuning-range applications. The CCO tuning speed is much faster than that of varactor-tuned oscillators, allowing very fast electronic and electro-optical PLLs.

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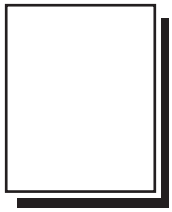

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