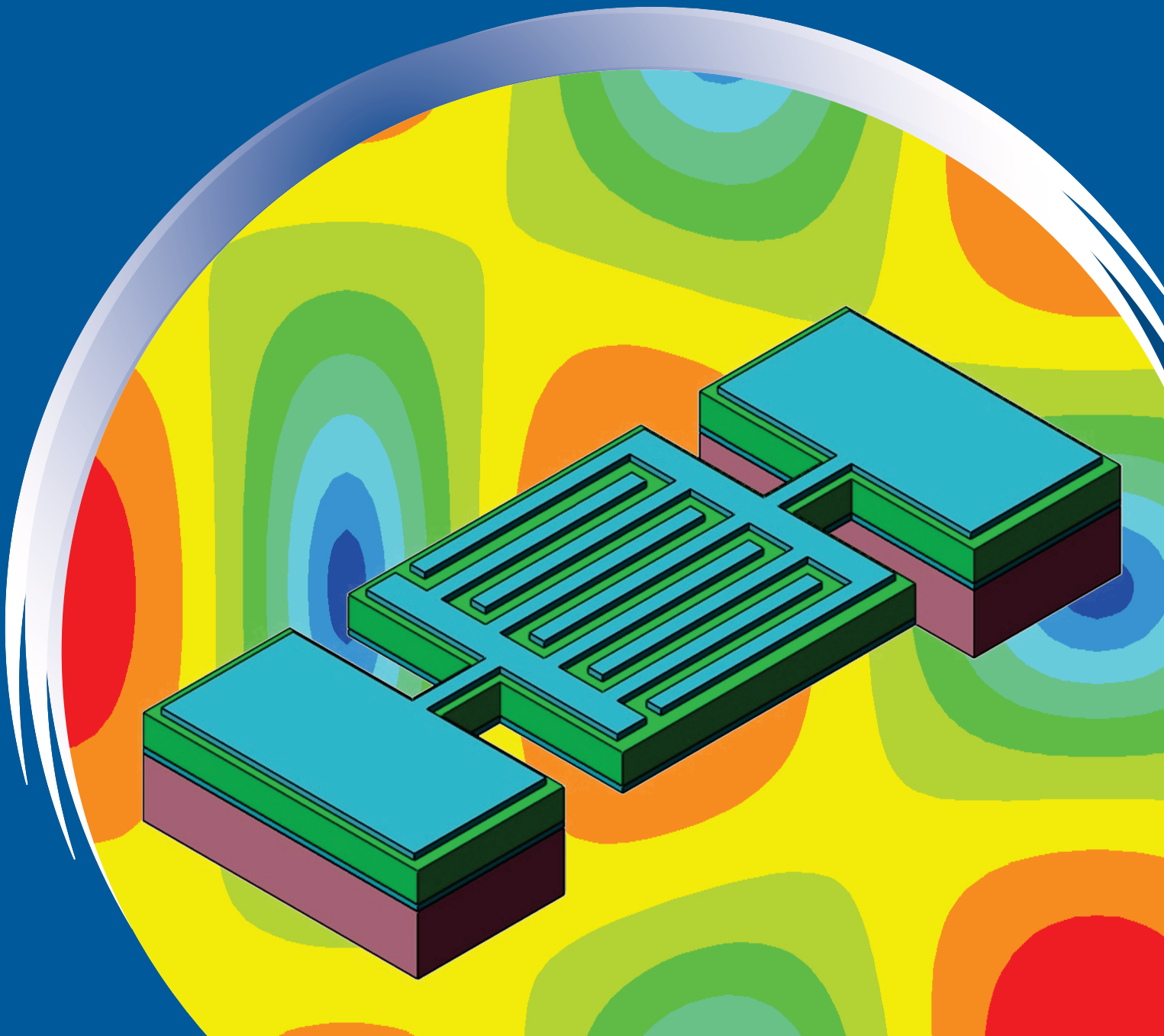
ISSN 0352-9045

# Informacije MIDEM

*Journal of Microelectronics, Electronic Components and Materials*
***Vol. 50, No. 3(2020), September 2020***

*Revija za mikroelektroniko, elektronske sestavne dele in materiale*
***letnik 50, številka 3(2020), September 2020***



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

# *Informacije* MIDEM *3-2020*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 50, NO. 3(175), LJUBLJANA, SEPTEMBER 2020 | LETNIK 50, NO. 3(175), LJUBLJANA, SEPTEMBER 2020

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.




**Headquarters | Naslov uredništva**
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Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 50, No. 3(2020)

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https://doi.org/10.33180/InfMIDEM2020.301

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# A Computationally Efficient 11 Band Non-Uniform Filter Bank for Hearing Aids Targeting Moderately Sloping Sensorineural Hearing Loss

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**Abstract:** A computationally efficient 11 band non-uniform filter bank addressing low or moderately sloping sensorineural hearing loss - the most common type of hearing problem- is proposed. This structure is suitable for low cost, small area implementations of hearing aids. The computational efficiency is achieved by adopting the Frequency Response Masking technique, which uses only two prototype filters with a total of 19 multipliers at 80 dB stopband attenuation for the design of entire non-uniform filter bank. The computational complexity analysis shows that the proposed method provides about a 70-90% reduction in computational resources compared to non-FRM methods and about a 40-80% reduction in computational resources compared to the other FRM methods. The audiogram matching performance analysis shows that the matching error of the proposed filter bank is negligible even without optimization. The delay performance of the filter bank is acceptable for both Closed Canal Fittings and Open Canal Fittings.

**Keywords:** filter bank; frequency response masking; interpolated FIR filter; hearing aid

# Računsko učinkovit 11 pasoven neenoten filter za slušno pomoč pri zmerni senzorno-nevralni izgubi sluha

**Izvleček:** Predlagan je računsko učinkovit 11 pasoven neenoten filter za slušno pomoč pri zmerni senzorno-nevralni izgubi sluha. Uporaben je pri ceneni in majhni implementaciji v slušne pripomočke. Računska učinkovitost je dosežena s tehniko maskiranja frekvenčnega odziva, ki uporablja le dva prototipna filtra z 19 množilniki pri 80 dB atenuaciji. Analiza je pokazala, d apredlagana metoda dosega 70 – 90% zmanjšanje računskih operacij v primerjavi z ne-FRM metodami in 40-80% izboljšanje v primerjavi z ostalimi FRM metodami. Analiza učinkovitosti avdiograma kaže zanemarljive napake tudi brez optimizacije. Zakasnitev filtra je sprejemljiva tako za ujemanje zaprtega kot odprtega kanala.

**Ključne besede:** filter; maskiranje frekvenčnega odziva; interpoliran FIR filter, slušna pomoč

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## 1 Introduction

The pioneering work by eminent researchers in multirate Digital Signal Processing (DSP), as summarized in [1,2], had a tremendous impact on different fields of digital signal processing applications like Hearing Aids (HA). Digital HA, as an assistive listening device, has numerous advantages over its analog counterpart. Flexibility in frequency-dependent speech amplification, programmability, reconfigurability, noise suppression, feedback cancellation, and stability of the system against ageing are some of the critical advantages of digital HA. The significant concerns of HA design are group delay, power consumption, size of the device, and design complexity.

Sensorineural Hearing Loss (SNHL) is the most common type of hearing loss that account for nearly 90% of the reported hearing loss. SNHL is an irrecoverable condition, and HAs are the most common type of treatment suggested for SNHL. Among the SNHL patients, most of the patients are reported with mild or moderate sloping audiograms representing the hearing loss towards higher frequencies. An example audiogram of a patient suffering from moderate sloping SNHL is shown in Figure 1. An audiogram is a graph used by HA experts to measure the softest sound a person can hear at different frequencies. The audiogram is recorded for both the ears. In figure 1, the 'X' marks represent the left ear, and 'O' marks represent the right ear.

The fundamental block diagram of a digital HA is shown in Figure 2. One of the critical parts of a digital HA is a Filter Bank (FB), which consumes almost half of the chip area and power compared to the other parts. The cost of implementing the filter bank with FIR filters that has a sharp transition width increases linearly with an increase in the order of the filter. Thus the fundamental philosophy of digital filter bank realization for audio application is to exploit the properties of FIR filters that result in efficient implementation. The reduction in computational resources of an HA has significant impacts on the overall size of the HAs. The size of HA is a crucial factor in In the Canal (ITC) and Completely in the Canal (CIC) HAs. The reduced computational requirement has multifold advantages like low power consumption, which is essential for battery operated low power HAs, and low-cost implementation.

An attempt to reduce the arithmetic operations in FIR filters, compared to direct form and linear phase implementation, by exploiting the redundancy of the filter coefficients, has resulted in a new class of filter implementation known as Interpolated FIR (IFIR) filter [3]. The main idea is to cascade an upsampler with an interpolator to create a sharp cut off filter using lower-order prototype filters. Another technique based on the IFIR to create sharp transition FIR filters known as Frequency Response Masking (FRM) is introduced in [4]. It is shown in [4] that proper 'masking and recombining' of the interpolated filter output, and its complementary output, can effectively reduce the cost of implementation of sharp filters at the expense of a specific delay added to the system. The same authors extended the work for audio equalization with a tree structure of Filters [5] to obtain reduced arithmetic operations for the realization of sub-filters. The advantage of FRM is that it will create filters with sparse coefficient values, which reduces the cost of implementation of the digital filter bank.

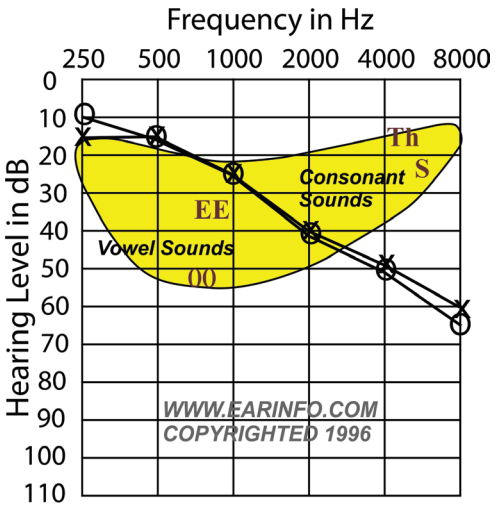



**Figure 1:** Sample Audiogram for Moderately sloping SNHL

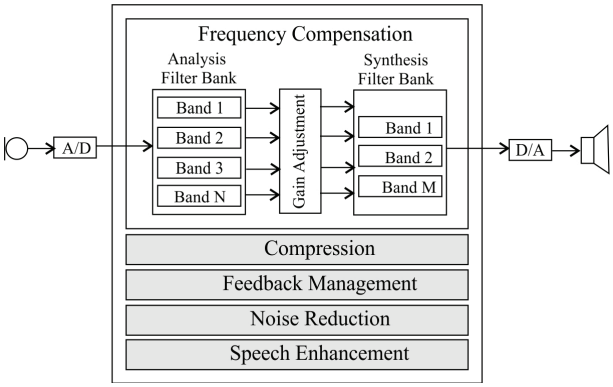



**Figure 2:** Block Diagram of a Digital Hearing Aid

Based on the above-discussed works, an eight-band an eight band IFIR filter bank for HAs has been proposed in [6]. The required frequency bands are created using half band complementary interpolated linear phase FIR filters. The frequency bands generated out of the structure was uniform in nature. One disadvantage of this method is that the delay of various frequency bands will vary, and it is required to use proper delay adjustments for a suitable group delay.

The idea of non-uniform filter banks is introduced in the papers [7-8] to match the non-uniform frequency characteristics of the human auditory system. They are based on FRM, half-band, and Complementary IFIR filter techniques. The above filter banks use only 2 Prototype Filters to realize the non-uniform filter bank. Improved version of the same idea using a different number of prototype filters for increased number of frequency bands are available in [9]. These implementations address the problems of hearing loss at high frequencies by allocating more bands at higher frequencies. A multi-branch FRM scheme, which is an improved version of [9],

is introduced in [10]. It has two or more than two Prototype filters, and an interpolated version of the same frequency masking filter is used to generate the required 16 bands NUFB. In this work, multiple prototype filters and multiplier sharing scheme is utilized to reduce the delay and complexity. However, uniform symmetric filter banks are used at the lower frequency and higher frequency region, which do not follow the octave band splitting scheme. The allocation of more bands at the higher frequency does not provide any added advantage but increases the complexity of the overall filter bank structure. Also, the multi prototype approach increases computational resources and the number of multipliers required to implement the design.

Reconfigurable FRM approaches to design NUFB are introduced in [11-13]. Combining different sub-band distribution schemes, these filter banks can provide a variety of band splitting choices at the expense of increased computational resources and delay. Various innovative ideas are presented in [12-13] to reduce the complexity of the design, which in turn resulted in increased group delay of the Filter Bank Structure. FRM approaches that can shape the frequency gain according to the NAL-NL1 prescription formula, at 1/3 octave frequencies provided by the ANSI S1.11 standards are introduced in [14-17]. The stringent constraints by the above specifications make the design of the filter bank very complicated. Realizations based on relaxed specifications of the above prescription formula can reduce the delay as explained in [15-16].

Other classes of Filter banks are Modulated filter banks and Farrow Structure filter banks [18-20]. They use various approaches of multirate signal processing and optimization techniques to obtain improved delay performance and matching error at the expense of complicated filter bank structure and computational resources. The reported results show that these designs require a vast number of multipliers and adders, which makes the filter bank structure power-hungry among all the other hardware components of the HAs.

The major contributions of this paper can be summarized as follows (i) Evolution of Interpolated Filter Bank for Implementation in HA is thoroughly reviewed (ii) Major design constraints for a filter bank in HA are deeply evaluated (iii) A computationally efficient filter bank structure for mild and moderately sloping SNHL audiograms is proposed (iv) Detailed design considerations of the proposed filter bank is explored and the same is explained with a design example (v) Experimental results of the proposed filter bank with other state-of-the-art filter bank architectures available in the literature are compared. The rest of the paper is organized as follows. In section 2, significant design constraints for digital HA is briefly explained. These constraints are set by different results and conclusions from recent research in the field of Audiology. The structure and design of the proposed filter bank are detailed in Section 3. Experimental results are presented and thoroughly analyzed in section 4. The results are compared with other works on filter bank design for HA reported in the literature and are discussed. The conclusion is drawn in section 5.

## 2 Design constraints of filter bank implementation in HAs

This section briefly explains the design constraints to be considered for a Filter bank used in a digital HA. The parameters described in this section need to be carefully analyzed by signal processing engineers and VLSI engineers for the efficient implementation of filter banks.

### 2.1 Effect of group delay in HAs

The usability of an HA is much dependent on the processing delay or group delay of the device. The two types of HA fittings usually employed in hearing-impaired patients are Open Hearing Aid Fitting (OHAF) and Closed Hearing Aid Fitting (CHAF). Examples of OHAF are Behind the Ear (BTE), and examples of CHAF are ITC and CIC type HAs. Research [21] shows that the delay difference of more than 5-10 ms can cause the 'Comb-Filtering effect' for the HA user. This effect is due to the superimposition of direct sound and amplified sound. The study conducted in [22-24] shows that a delay difference up to 30 ms is acceptable in the case of CHAF. The demand for CHAF has diminished in the past decade due to the 'Occlusion effect' usually found in such devices. Audiologists found that [25] occlusion effect is prominent if the delay is more than 10ms. Thus the delay difference of 10 ms between the actual sound and processed sound remained as an unofficial standard among HA engineers and audiologists. Active occlusion algorithms [26] can improve the situation in CHAF and increase the limit of tolerable delay in CHAF. A recent study in this area [27] shows that hearing-impaired users have significantly higher delay tolerance than ordinary people. Thus up to 20 ms delay is acceptable for hearing-impaired subjects in the case of CHAF. However, an increase in a processing delay of more than 30 ms can cause disruptions in audio-visual integration [28] and question the usability of the HA.

### 2.2 Effect of number of frequency bands

Increasing the number of bands for proper frequency compensation have a direct relationship with the processing complexity and delay of an HA. It is evident

from the findings in [29] that for a moderate slope audiogram, four bands are adequate to provide flexible frequency shaping. However, audiograms with steep slope require more number of bands, and the frequency shaping accuracy increased significantly for seven bands. An extensive study conducted on 957 audiograms in [30] shows that the ideal number of bands required for HAs varies for an audiogram. However, a nine-band HA can accommodate the frequency shaping problem of most of the audiograms. According to the findings in [31], the number of bands required for steep audiograms lies between 9 to18. It is also shown in some studies [32] that the frequency shaping performance remains constant after eight bands for moderately sloping audiograms.

The filter bank in HA imitates the logarithmic perception of the basilar membrane in the ear and has narrow frequency resolution at lower frequencies compared to higher frequencies. Thus more number of bands need to be allocated at the lower frequencies. Increasing the number of bands at high frequencies does not have any proven advantage; instead, it increases the processing complexity and delay. These findings are explored in this work to design the proposed filter bank.

### *2.3 Effect of Matching error*

In HA, hearing loss is compensated by adjusting the gain of the filter bank. The mismatch between prescribed gain and actual ear gain can cause discomfort to the HA user. The error mainly depends on the number of frequency bands and the flexibility of gain adjustment. The term 'matching error' is used to quantify the difference between the prescribed gain and gain adjustment curve provided by the filter bank. This is a measure used to analyze the performance of filter banks in HA. According to work reported in [33], the maximum matching error permitted for a filter bank is ±5dB. Since there are chances of human error during HA fitting, it is always safe to limit the maximum permissible matching error as ±3dB. The filter bank research articles explored in the introduction section [7-8, 12-13, 15-16, 19-20] targets to limit the matching error of the HA between ±3 dB and ±5 dB.

### *2.4 Computational constraints*

A significant factor affecting the customer satisfaction of HA is battery life. A study conducted in [34] shows that DSP processing hardware is responsible for about 70% of the energy consumption in a digital HA. Thus the critical component responsible for the power consumption among other DSP structures in HA is Filter Bank. Many of the work discussed earlier in this section [10, 12-16] have explored low power implementation strategies suitable for filter banks. Research shows that [35] HAs are more likely to be accepted if their benefit per unit of cost to the user is more.

Based on the analysis performed on the past research on VLSI signal processing [3-20] and audiology [21-37], the parameters that need to be considered for Filter Bank Design in Digital HA are summarized in Table 1.

## *3 Proposed filter bank*

The proposed 11 bands filter bank is derived from a basic version of 12 bands filter bank which meticulously follows the 1/3 octave frequency splitting. The 11 band filter bank has a significant delay advantage over 12 bands basic version. In this section, the fundamental design of the 12 bands filter bank is presented and the design of the 11 band improved version is discussed. As shown in Figure 3, the proposed 12 bands filter bank is designed using a Double Prototype FRM scheme. This scheme is an advanced version of the IFIR scheme discussed in [3] and [4]. It has advantages over a multi prototype scheme [10] in saving the additional computations to design more number of sharp transition FIR filters.

So far, in the literature, we can see various filter bank schemes ranging from 8-17 bands. However, our proposed design can optimize the computational resources and keep the other parameters like delay and matching error within acceptable limits, making it suitable for low-cost implementations of HAs. Even the

**Table 1:** Summary of design constraints for filter bank design in HAs.

| Parameter | Requirement |
|---|---|
| Audiogram Matching | Capability to adjust the Magnitude Response |
| Frequency Response Characteristics | Non-uniform suitable for the human ear |
| Number of frequency bands | 4-8 for moderately sloping Audiogram<br>9-18 for steeply sloping Audiogram |
| Computational Cost | Less Number of Multipliers |
| Group Delay | Less than 20 ms for closed fittings and Less than 10ms for open fittings |
| Power | Suitable for Battery operated working |
| Area | Suitable for ITC and CTC hearing aid size |
| Matching Error | Less than ±5dB |

| | |
|---|---|
| Stop Band Attenuation | Greater than 60 dB |
| Phase Response | Linear Phase |
| Bandwidth | 8 kHz for Normal HA<br>10-12 kHz for Advanced high Fidelity HA |
| Aliasing | Inbuilt Cancellation |

16 band filter bank designed in [10] can also be designed in this approach. However, our analysis shows that the additional bands realized in the high-frequency region do not have much effect on the audiogram matching; instead, it introduces compuataional overhead in the overall filter bank structure.

The selection of the sub-bands is made by keeping three objectives in mind. (i) To match the non-uniform characteristics of the human ear by providing 1/3 octave splitting for the frequency region for satisfactory audiogram matching (ii) Reduce the unnecessary computations in the filter bank, especially in the high-frequencies and (iii) Keep the overall delay of the filter bank within the acceptable limit. The primary 12 band structure proposed is suitable for CHAF fittings in which up to 20ms delay is acceptable. To make the structure ideal for OHAF, we have proposed the second structure, which reduces the delay by removing a higher-order interpolation filter branch at the low-frequency region of the basic 12 band NUFB.

### *3.1 Structure of the Proposed filter bank*

The structure of the Proposed filter bank is given in Figure 3 is motivated from 1/3 octave splitting of frequencies. The cut-off frequencies of the proposed structure are determined based on different considerations like minimum matching error and computational resources. From the structure, it can be seen that only two Prototype Filters $H_1(z)$, $H_2(z)$, and their interpolated versions are utilized to obtain the required 12 bands. In this scheme, prototype filters have two roles (i) Band edge frequency shaping and (ii) Frequency masking. Hence this approach can be called a double prototype FRM scheme. In order to achieve high resolution at low frequencies, a sharp transition filter is required, and that leads to the use of a maximum interpolation factor of 12 in the proposed 12 band filter bank. The transfer functions and cut off frequencies of the 12 sub-filters used in the proposed structure is given in Table 2.

An exciting finding from the analysis of low or moderately sloping audiograms is that the slope of the audiogram is less at low frequencies, and removal of the first band which uses an interpolation factor of 12 does not affect the matching error in a more significant manner. Thus we have also found that removing the first band from the structure will result in an 11 band structure, which can significantly improve the delay performance while keeping the matching error satisfactory in the low-frequency region (250Hz-500Hz). The 12 band structure can be used for audiograms with larger slope at 250Hz region, and the 11 band structure can be used for zero slope audiograms at the 250Hz region, respectively.

Generally, a single filter can be used to compensate for the frequency in the region from 4000Hz to 8000Hz. However, this can lead to a significantly large matching error in the high-frequency region. Traditionally IFIR and FRM schemes adopt a symmetric structure in both low pass and high pass regions. The symmetric nature of the frequency bands is because the frequency bands required for high frequency regions are derived from the complementary filter approach [7]. However, we have found that providing four bands with a bandwidth of 1000Hz in the region from 4000-8000Hz is sufficient to provide adequate matching performance in the high-frequency region. The removal of unnecessary symmetrical branches at high frequencies reduced the number of adders in our implementation contrary to other implementations. The reduction of the total number of adders in the filter bank has a slight advantage of reduced computational complexity and significant advantage of reducing the adder dependent critical path delay in the output stage of the filter bank.

The graphical representations of the low pass filter responses ($A_1$-$A_8$) and its corresponding complementary responses of the selected branches ($B_1$-$B_4$) are shown in Figure 4. From the figure, it can be seen that the high-frequency regions require only four complementary filters with reduced interpolation factor of maximum 4. By performing suitable subtraction of the branches, we can obtain the sub-bands ($C_1$-$C_8$ and $D_1$ – $D_4$), as illustrated in Figure 4 (b). The 11 band filter bank will have the first low pass cut off frequency at 500 Hz instead of 250 Hz in 12 band filter bank, as shown in Figure 4 (c). Figure 4 (d) represents the formation of Sub bands in 11 band filter bank by suitable addition and subtraction of the filter responses. The cut-off frequencies of the Prototype filters $H_1(z)$ and $H_2(z)$ in both the structures are 4kHz and 3 kHz, respectively. These prototype filters can produce interpolated versions of the filter response with cut off frequencies 2kHz, 1.5kHz, 1kHz, 750Hz, 500Hz, and 250 Hz.

### *3.2 Design of the Proposed filter bank*

The implementation of the proposed filter bank is based on eight low pass filters denoted as $A_i(z)$ where i=1….8 and four high pass filters denoted as $B_j(z)$ where j=1...4. The 12 sub bands are generated by the subtrac-

tion of the high pass and low pass filters as shown in equation (1) and (2).

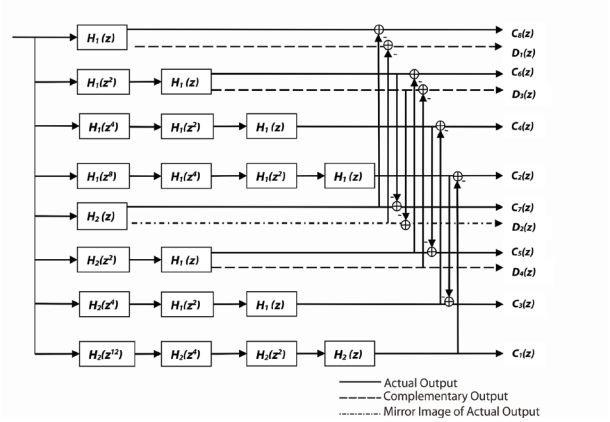



**Figure 3:** Structure of the proposed Filter Bank

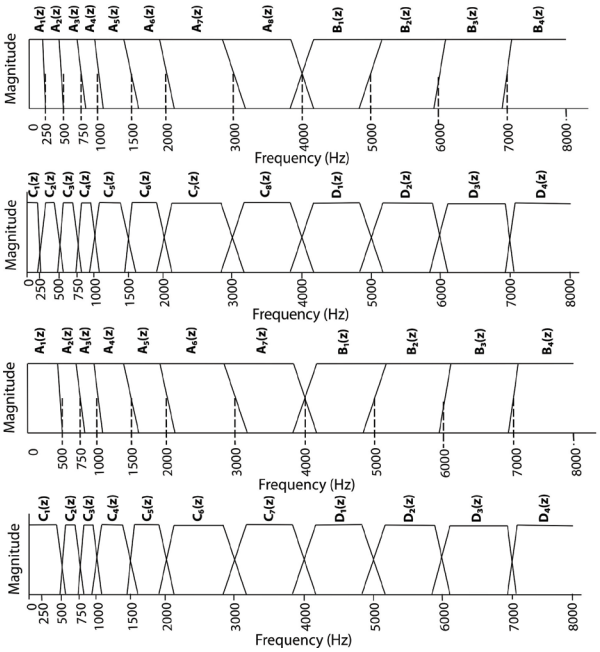



**Figure 4:** Magnitude response of LPFs and HPFs and Sub bands in Filter Bank (a) & (b) 12 band (c) & (d) 11 band

$$C_i(z)=\begin{cases} A_i(z), & i=1 \\ A_i(z)-A_{i-1}(z), & i=2,\ldots,8 \end{cases} \quad (1)$$

$$D_j(z)=\begin{cases} B_j(z)-B_{j+1}(z), & j=1,..,3 \\ B_j(z), & j=4 \end{cases} \quad (2)$$

Where $C_i(z)$ represents the sub bands in the frequency range 0Hz- 4KHz and $D_i(z)$ represents the sub bands in the frequency range 4KHz-8KHz. $A_i(z)$ and $B_i(z)$ represents the low pass and high pass filter responses derived from the prototype filters $H_i(z)$ and $H_2(z)$.

Similarly, the general expressions to derive the bands in the 11 sub bands in the optimized filter bank is given by equation (3) and (4).

$$C_i(z)=\begin{cases} A_{i+1}(z), & i=1 \\ A_{i+1}(z)-A_i(z), & i=2,\ldots,7 \end{cases} \quad (3)$$

$$D_j(z)=\begin{cases} B_j(z)-B_{j+1}(z), & j=1,..,3 \\ B_j(z), & j=4 \end{cases} \quad (4)$$

The filter responses $H_{1c}(z)$ and $H_{2h}(z)$ required to generate the high pass filter bands as shown in Table 2 is derived from the equation given in (5) and (6).

$$H_{1c}(z)=z^{\frac{N-1}{2}}-H_1(z) \quad (5)$$

$$H_{2h}(z)=H_2(-z) \quad (6)$$

It can be seen from the analysis that the delay performance of the filter bank directly depends on the sampling frequency of the input signals. Suppose we want to design a 12 band non-uniform filter bank whose frequency range is from 0Hz to 8kHz. The sampling frequency should be greater than or equal to 16kHz ($2f_m$) in order to satisfy the Nyquist sampling criteria. However, modern HAs are using other sampling rates like 20kHz and 24 kHz also for the high fidelity listening experience.

The design parameters that need to be determined for the required audiogram matching include gains for each sub-band, transition bandwidth for each prototype filters, and the group delay of the overall filter bank. The gain of each sub-band depends on the type of audiogram to be matched. The proposed filter bank is designed by keeping low or moderately sloping SNHL audiograms as targetted audiograms. In order to achieve high resolution in the low-frequency region, sharp transition width filters are required and which significantly increases the order of the filter bank. In our approach, the interpolation and frequency masking is used to overcome this limitation and to produce sharp filters. It is a known fact that interpolation factor M of a filter introduces M replicas of the prototype filter with sharp transition bandwidth [1-2,5]. It is required to mask the unwanted replicas due to interpolation, and that is the reason for using Prototype filter for both frequnecy band creation and masking.

**Table 2:** Cut off frequencies and Transfer functions of sub bands in the filter bank

| Band | Frequency Range (Hz) | Transfer Function |
|---|---|---|
| A1 | 0-250 | $H_2(z^{12})H_2(z^4)H_2(z^2)H_2(z)$ |
| A2 | 0-500 | $H_1(z^8)H_1(z^4)H_1(z^2)H_1(z)$ |
| A3 | 0-750 | $H_2(z^4)H_1(z^2)\ H_1(z)$ |
| A4 | 0-1000 | $H_1(z^4)H_1(z^2)\ H_1(z)$ |
| A5 | 0-1500 | $H_2(z^2)\ H_1(z)$ |
| A6 | 0-2000 | $H_1(z^2)\ H_1(z)$ |
| A7 | 0-3000 | $H_2(z)$ |
| A8 | 0-4000 | $H_1(z)$ |
| B1 | 4000-8000 | $H_{1c}(z)$ |
| B2 | 5000-8000 | $H_{2h}(z)$ |
| B3 | 6000-8000 | $H_1(z^2)H_1c(z)$ |
| B4 | 7000-8000 | $H_1(z^4)H_1(z^2)\ H_1c(z)$ |

A. Gain Adjustment of Sub bands and Calculation of Matching Error

The gain adjustments for different filters in the filter bank are performed as given below.
Let

$$P=\left[p_1,p_2,p_3,\ldots,p_N\right]^T \tag{7}$$

$$M=\left[C_1,C_2,\ \ldots,C_8,D_1,\ldots,D_4\right] \tag{8}$$

Here, P is the sampled audiogram with N data points. The value of $i_{th}$ sample of P is $p_i$. Similary $C_k$ is the sampled magnitude response of the filters in the frequency region between 0Hz and 4KHz and $D_k$ is the sampled magnitude response of the filters in the frequency region between 4KHz and 8KHz.

Assume that the gain of each band is given as $g_i$ (i = 1,2, …, 12) and $C_k$ is the magnitude response of the kth sub band (k = 1,2, …, 8) in logarithmic scale. $D_k$ is the magnitude response of the 8 + $k_{th}$ sub band (k = 1,2, …, 4) in logarithmic scale as showin in equation (9) and (10)

$$G=\left[g_1,g_2,\ g_3,\ldots,g_{12}\right]^T \tag{9}$$

$$C_k=[c_{k,1},c_{k,2},c_{k,3},\ldots,c_{k,N}],\ k=1,2,...,8 \tag{10}$$

$$D_k=[d_{k,1},d_{k,2},\ d_{k,3},\ldots,d_{k,N}],\ k=1,2,...,4 \tag{11}$$

The matching curve can be obtained by summing the magnitude response of all the filters in the filter bank after performing the required gain adjustment suitable for the audiogram. The matching curve, S is given by,

$$S=\sum_{i=1}^{8}C_ig_i+\sum_{i=1}^{4}D_ig_{8+i} \tag{12}$$

The matching error is obtained by finding the difference between the audiogram and the matching curve. The matching error, E is given by,

$$E=P-S \tag{13}$$

The maximum absolute error in dB is given by

$$E_{max}=\max\left|P-S\right| \tag{14}$$

Different optimization schemes can further optimize the matching error. In [10] minimax optimization scheme applied and in [8] minimum least square error scheme is applied to optimize the matching error. Since our matching error results fall under an accepted matching error limit, we have presented our results without optimization. In all the works reported, on average, the optimization can reduce the matching error by about 40-50%. Hence it is evident that optimization can achieve better matching in the proposed design also, which makes it suitable for computationally efficient low-cost implementation with a better matching result.

B. Calculation of Transition Bandwidth of the Filter Responses

In order to obtain proper passband for each subband, the stopband edge of $A_{i-1}$ must be smaller than the passband edge of $A_i$ (i.e the value of x should be less than the value of y as shown in the below Figure 5). To satisfy the above condition, the transition bandwidth of both the prototype filters is selected to be equal. To determine the required transition width for the proposed filter bank structure, the filterbank is designed for different transition bandwidths varying from 0.3kHz to 1.5kHz and corresponding matching errors are noted. A table showing the effect of Transition width on the Maximum Matching Error (MME) of the Audiogram is given in Table 3. The Transition width and the maximum matching error without optimization is presented.

From Table 3, it is observed that the minimum matching error is obtained when the transition bandwidth is 1 kHz. The second minimum matching error occurs at 1.2 kHz. Also, it is observed that the matching error decreases with the increase in the transition bandwidth up to 1 kHz. Further increase in transition bandwidth worsens the matching error due to overlap among different bands, especially in the low frequency where the sub-bands are narrow. From the analysis, 1KHz is

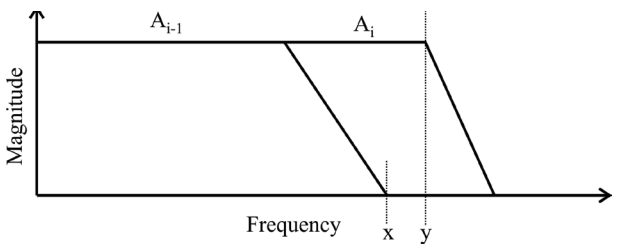



**Figure 5:** Method of generating the Sub bands

selected as the best suitable transition width for minimum matching error. However, it can be shown that the computational resources can be reduced if we select the transition bandwidth as 1.2 kHz. This is because, from Table 3, it can be seen that the number of non-zero coefficients required to implement the two prototype filters is 19 for transition width 1kHz, and that is 14 for transition width 1.2kHz.

These 19 non zero coefficients are responsible for the multiplications in the filter bank, and it also affects the group delay of the filter bank. However, the transition width of 0.8kHz increases the computational requirements by 50%, and the transition width of 1.2kHz decreases the computational requirement by 25%.

C. Delay Analysis of the Filter Bank

The delay of the proposed filter bank $T_d$ can be calculated using the following equation.

$$T_d = T_b + T_m \tag{15}$$

Where $T_b$ is the delay of generating multiple bands by interpolation and $T_m$ is the delay of masking filters, which is used to separate the required low pass or high pass version from the multiple bands.

For a linear phase interpolated filter H (zM), its group delay is given by

$$t = \left[\frac{L-1}{2}\right]\frac{M}{f_s} \tag{16}$$

Where, L is the length of the prototype filter, M is the interpolation factor and fs is the sampling frequency.

In the proposed 12 band filter bank structure, the maximum delay is found at the lowermost branch, which is used for generating the narrow band filter $C_1(z)$. Since the entire branch is derived from a single prototype filter, the total delay is given as

$$t_{tot} = \left[\frac{L-1}{2}\right]\frac{(M_1+M_2+M_3+M_4)}{f_s} \tag{17}$$

Where $M_1$, $M_2$, $M_3$ and $M_4$ are the interpolation factors of $H_2(z12)$, $H_2(z4)$, $H_2(z2)$, and $H_2(z)$, respectively, L is the length of the prototype filter $H_2(z)$. By substituting the values for $M_1$, $M_2$, $M_3$ and $M_4$ we get

For 12 Band filter bank,

$$t_{tot} = \left[\frac{L-1}{2}\right]\frac{(12+4+2+1)}{f_s} = \left[\frac{L-1}{2}\right]\frac{19}{f_s} \tag{18}$$

For 11 Band filter bank,

$$t_{tot} = \left[\frac{L-1}{2}\right]\frac{(8+4+2+1)}{f_s} = \left[\frac{L-1}{2}\right]\frac{15}{f_s} \tag{19}$$

Therefore, the delay of the filter bank for 1kHz transition bandwidth (L=27) is $\frac{195}{f_s}$ and the delay of the filter bank for 1.2 kHz transition bandwidth (L=21) is $\frac{150}{f_s}$.

Table 4 summarizing the delay of the proposed 12 band and 11 band filter banks for different sampling frequencies and transition widths.

D. Design Example

In our proposed design, we are using only two prototype filters. The design of an FRM filter bank with more number of prototype filters can reduce the processing delay at the cost of increased computational resources. A single prototype filter may add a limitation to the design as it is required to provide frequency band shaping and masking. Hence it is required to select the cut off frequencies of the filters in such a way that it can be used as both band shaping filter and masking filter.

**Table 3:** Effect of Transition width on Maximum Matching Error (MME)

| Transition Bandwidth | Order of Prototype Filter | Unique Coefficients | | | Maximum Matching Error |
|---|---|---|---|---|---|
| | | $H_1(z)$ | $H_2(z)$ | Total | |
| 0.3 kHz | 80 | 20 | 38 | 58 | 2.0362 |
| 0.5 kHz | 52 | 14 | 24 | 38 | 1.7346 |
| 0.8 kHz | 38 | 10 | 18 | 28 | 1.3527 |
| 1 kHz | 26 | 7 | 12 | 19 | 1.1107 |
| 1.2 kHz | 20 | 5 | 9 | 14 | 1.3756 |
| 1.5 kHz | 13 | 4 | 6 | 10 | 1.5274 |

**Table 4:** Delay of Proposed Filter Banks for different sampling frequencies.

| Sampling Frequency | Delay of 12 Band Filter Bank (ms) | | Delay of 11 Band Filter Bank (ms) | |
|---|---|---|---|---|
| | Transition widths | | | |
| | 1 kHz | 1.2 kHz | 1 kHz | 1.2 kHz |
| 16 kHz | 15.4 | 11.9 | 12.9 | 9.4 |
| 20 kHz | 12.35 | 9.5 | 9.75 | 7.5 |
| 24 kHz | 10.3 | 7.9 | 8.12 | 6.25 |

Now, different low pass filter bands are designed using interpolation of prototype filters. High pass filters are derived from the complementary approach and half band approach are used to reduce the coefficients. Appropriate filter bands are used to mask the filter responses. The audiogram matching is performed with different transition widths. A base transition width is selected which reduces the matching error. Different optimization techniques can be used to obtain better

matching results. Commonly used optimization methods are min-max optimization [10] and minimum least-square optimization [8]. The optimization process needs to be incorporated into the HA fitting software, which makes the overall HA fitting process complex and costlier. Hence we have presented our results without optimization and are comparable with the results obtained through various optimization schemes.

Delay of the filter bank is depending on the order of the prototype filter and the maximum interpolation factor used in a particular path. Decreasing the order of the filter can improve the delay, but that worsens the matching performance of the filter bank. The tradeoff between matching error and delay is analyzed, and the order of the Prototype filter is fixed. Once the bands of the filter banks are obtained, it is required to individually adjust the gain for each band based on the audiogram.

## 4 Experimental results and discussion

### 4.1 Selection of audiograms

In order to verify the effectiveness of the proposed design, we have examined the performance of the proposed filter bank against four standard audiograms of SNHL patients as given in Figure 6. These Audiograms are taken from Independent Hearing Aid Information, a public service by Hearing alliance of America [38]. All the works compared in this work have used the same audiograms to compare the efficiency of their design. Out of the eight different audiograms available, four are considered for evaluation. These four audiograms are selected based on the criteria of the proposed design, that is, the proposed filter bank design is for mild or moderate sloping Audiograms. Out of the four, two audiograms representing mild sloping and the other two represent moderate sloping audiograms. Since the remaining four audiograms available in the database are notched audiograms with substantial variation in middle frequencies representing rare cases of hearing loss, they are not considered for evaluation in this work. A brief description of the audiograms considered for evaluation is given below.

The audiogram represented as Type 1 is the most common type of audiogram found in aged people. This audiogram represents typical SNHL Hearing loss. In this hearing loss, the HA should leave the low-frequency region untouched and provide mild and moderate amplifications to the sound at middle and high frequencies. The audiogram represented as Type 2 is another common audiogram but represents mild to moderate hearing loss in the low-frequency region. We can see that the hearing loss in the high-frequency region is minimal. The effect of such a hearing loss is the loss of loudness, and the patient may be unaware of some natural sounds or sounds in various conversations. Type 3 audiogram is commonly found in people working in noisy environments. Like in Type 1, in the low-frequency region, it is required to perform only very low amplification. Type 4 audiogram represents total hearing loss at high frequencies. People with this class audiograms have moderate hearing loss at low frequency and high hearing loss at middle frequency. Since there is a total loss at high frequency, the hearing range of the patient will be minimal.

### 4.2 Simulation results

The simulation of the proposed filter bank and matching of the audiograms are performed in the Matlab R2017b environment. The Low pass and high pass versions of the sub-band filters are designed, as explained in the previous section. The individual sub-bands are separated using masking, and the corresponding 12 band and 11 band filter banks are generated. The transition bands of the filters are adjusted in such a way that minimum matching error will be obtained for Type 1 Audiogram. Once the Filter banks are designed, Gain matching is performed for each Audiograms from Type 1 to Type 4.

The Low Pass and High pass versions of the Filters for 12 bands and 11 band filter banks are given in Figure 7(a) and 7(b). These subfilters are subtracted in the proper order to generate the required filter bank structure as shown in Figure 7(c) and 7(d)The matching curve is plotted against the audiograms after the gain adjustment to calculate the matching error. From the matching Curve, Matching error is plotted to calculate the Maximum Matching Error (MME) for each audiogram. The Matching Curve and Matching error corresponding to each audiogram are given in Figure 8. It can be seen from the simulation that the matching performance of the proposed filter bank is reasonable for all the audiograms. The audiogram matching is performed and presented without optimization. From the matching curves, it can be seen that both the 11 band and 12 band filter banks follow the same matching curve except at the beginning of the audiogram. We have also evaluated the performance of 10 band filter bank, that can be achieved by removing one more low-frequency band in the region 500Hz – 750 Hz. However, it does not have any computational or delay improvement; rather, it increases the matching error. Thus we have obtained the optimum number of bands that can give better results in this approach as 11 bands.

It can be seen from the matching curve that this approach flexibly following the audiogram of the hearing impaired person of Type 1 and Type 2 audiogram, which is the most common type of hearing loss, ac-

counts for a major portion of hearing loss in the world. However, the matching error slightly increased for Type 3 and Type 4 audiograms due to the increased slope in the lower and middle frequencies. The MME is largely contributed by the low-frequency region and middle-frequency region, and the high-frequency region frequency region has less impact on the MME. The best matching is achieved for Type 2 audiogram followed by Type 1, Type 3, and Type 4.

All the matching error falls under the acceptable limit of ±5dB, which indicates that the proposed filter bank structure is suitable for sloping audiograms. However, the proposed scheme is not susceptible to large slope variation in the middle-frequency region. This is due to the fact that FRM scheme uses larger bands in the middle frequency region compared to the lower and higher frequencies. The matching performance can be further improved by allocating more number of bands in the middle frequency region, but it will eventually result in an increased number of multipliers and increased group delay of the HA.

### *4.3 Performance comparison and discussion*

A detailed comparison of the proposed filter banks with existing filter banks is given in Table 5. The comparison is made with both FRM based and non-FRM based techniques. From Table 5, it is evident that the proposed filter banks use less computational resources compared to the other techniques. The MME of the proposed filter bank is also superior to the other techniques except [15]. However, comparing the computational resources, the implementation of [15] requires more number of multipliers and the delay is also comparatively high. It is to be noted that the MME of [8] and [10] given in the table are optimized results. Optimization of the proposed filter bank also can provide comparable results with [8] and [10]. However, it is not included in the table as it is not a usual practice in HA fitting process. All the reported works except [8] provide acceptable matching performance for all the audiograms. However, the matching performance of [8] for Type 3 and Type 4 audiograms is not acceptable for real time implementations of HAs.

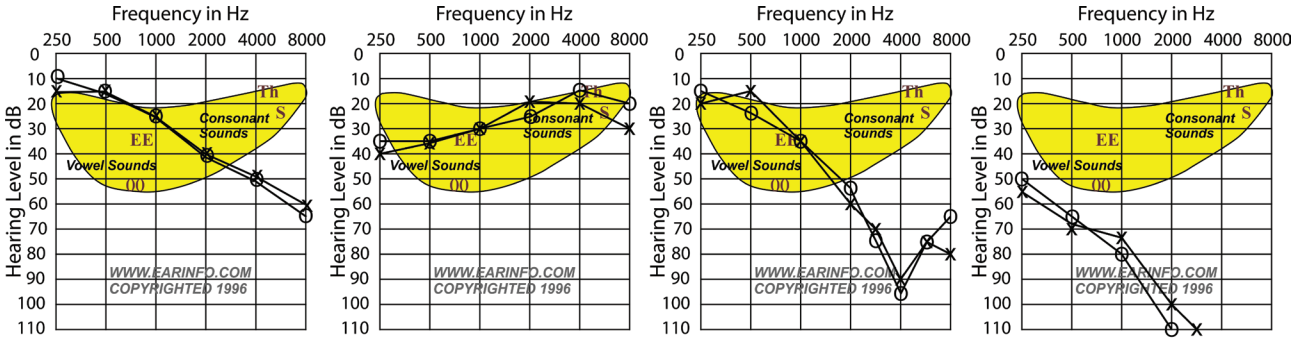
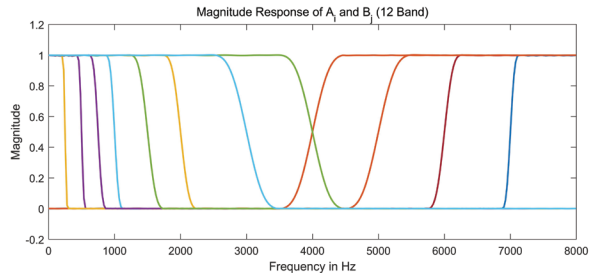


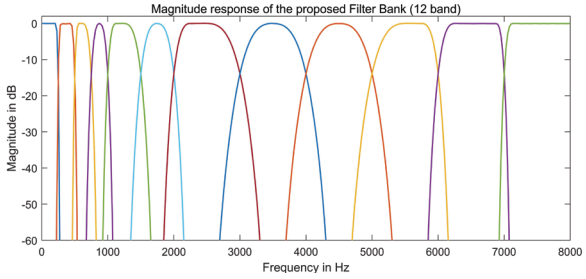

**Figure 6:** (a) Type 1 (b) Type 2 (c) Type 3 (d) Type 4 Audiograms

**Table 5:** The Comparison of non-uniform Filter Banks designed for Hearing Aids

| Filter bank | FRM Based | Maximum Matching Error (MME) for Different Audiograms (in dB) | | | | Computational Resource Requirement | | Delay (ms) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Type 1 | Type 2 | Type 3 | Type 4 | #Multipliers | #Adders | $f_s$=16kHz | $f_s$=20kHz | $f_s$=24kHz |
| Cosine Modulated [18] | N | 2.49 | 2.19 | - | - | 192 | 384 | - | - | - |
| Reconfig. 1 [12] | Y | - | - | - | - | 90 | 190 | 29 | 23.2 | 19.33 |
| Reconfig. 2 [13] | Y | - | - | - | - | 76 | 170 | 12.1 | 9.68 | 8.07 |
| Farrow 1 [19] | N | 2.45 | 1.67 | - | - | 216 | 432 | 1.1 | 0.88 | 0.73 |
| Farrow 2 [20] | N | 2.60 | 1.51 | 2.96 | - | 138 | 276 | 1.3 | 1.04 | 0.87 |
| QANSI [15] | N | - | 0.1 | 0.6 | - | 226 | 452 | 15 | 12 | 10 |
| QANSI 1 [16] | N | 4.28 | - | - | - | 64 | 128 | 16.88 | 13.5 | 11.25 |
| QANSI 2 [16] | N | 1.18 | - | - | - | 72 | 144 | 18.81 | 15.07 | 12.56 |
| FRM 8 band [8] (Optimized) | Y | 0.83 | 2.11 | 14.13 | 9.64 | 18 | 36 | 12.8 | 10.24 | 8.533 |
| FRM 16 band [10] (Optimized) | Y | 0.42 | 0.27 | 4.33 | 1.63 | 33 | 64 | 6 | 4.8 | 4 |
| Proposed 12 band | Y | 1.11 | 0.74 | 3.26 | 2.98 | 19 | 38 | 15.4 | 12.35 | 10.3 |
| Proposed 11 band | Y | 1.11 | 0.74 | 3.26 | 3.23 | 19 | 38 | 12.9 | 9.75 | 8.12 |




(a)

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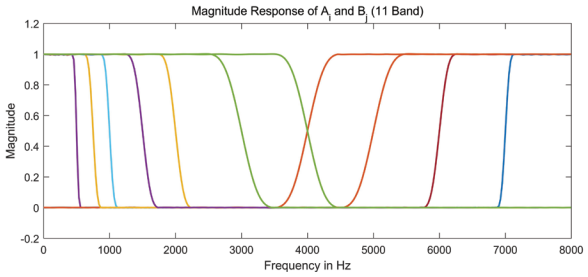


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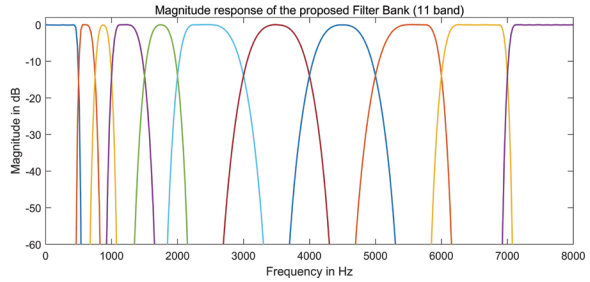


(d)

**Figure 7:** Simulation results of LPFs and HPFs in Filter banks & Sub bands in Filter banks (a) & (b) 12 Band (c) & (d) 11 band

The delay performance of the proposed filter bank is within the acceptable limit for both OHAF and CHAF. The delay performance of [10] is superior to the proposed method as it is implemented using 3 Prototype filters. Implementation of 3 prototype filters requires more number of multipliers compared to our approach. The results shown in [10] claims that the matching performance is achieved using only 33 multipliers, but our estimation shows that this number is very less for the reported matching result.

From the comparison table, it is clear that the FRM based methods [8, 10] have the advantage of reduced computational complexity but has a higher delay. Among the various work reported, Cosine Modulated Filter Bank (CMFB) approach [18] provides the lowest delay filter bank. This is because CMFB filter banks do not use the concepts of interpolation and masking approach.

However, the large number of multipliers and adders makes it significant in the chip area and consumes huger battery power. Reconfigurable filter banks [12-14] offer flexibility in a different type of audiogram matching, especially audiograms with notching in the middle frequency region. However, in this kind of filter banks, the computational complexity is enormous.

Among the filter banks considered for comparison, QANSI filter provides the best audiogram matching performance. Even though the QANSI approaches [15-17] follow the standard prescription formula, the significant computational resources, increased delay, and tedious design process makes it inferior to FRM methods. Among the FRM methods, the proposed structure has more computational efficiency with better matching performance. The delay is kept within the acceptable limits, and the performance of the 11 band filter bank is promising to be used in low-cost implementations of HAs used in OHAF and CHAF. The MME of Type 1 audiogram for the proposed filter bank structure is the lowest among all the reported works. The MME of Type 2 is superior to all the other works reported except [15], Type 3 and Type 4 audiograms also provide comparable results with other filter banks.

The main attraction of the proposed filter bank structure is the lowest computational complexity among all the other works reported. It can be seen from the table that the proposed method requires only 19 multipliers to implement 12 bands and 11 bands structures. If we consider the 11 band filter bank for actual implementation this is about an average 70-90% reduction in the number of multipliers and adders required for the filter bank implementation compared to the non FRM methods. Among the FRM methods, it can be seen that using only one extra multiplier, the proposed filter bank generates three additional frequency bands in the low-frequency region compared to [8]. These extra bands have apparent advantages of matching performance, as seen from the table. The number of multipliers required per band for [8] is 2.25, and that of the proposed method is 1.72. Also, the multipliers re-

quired per band for [10] are 2.06. The results show that the proposed method achieves comparable matching performance with [10] using the reduced number of bands. The adders are also reduced significantly compared to the other FRM methods. This can reduce the adder dependent delay in the actual implementation. The delay of the proposed 12 band filter bank is acceptable but larger compared to the FRM methods. However, the delay performance of the proposed 11 band filter bank is satisfactory compared to all the reported approaches.

The efficiency of the proposed method lies in the following aspects

(i) Design of the 11 bands in the filter bank is carried out using only 2 Prototype Filters, which is a reasonably low multiplier per band among the FRM methods re-

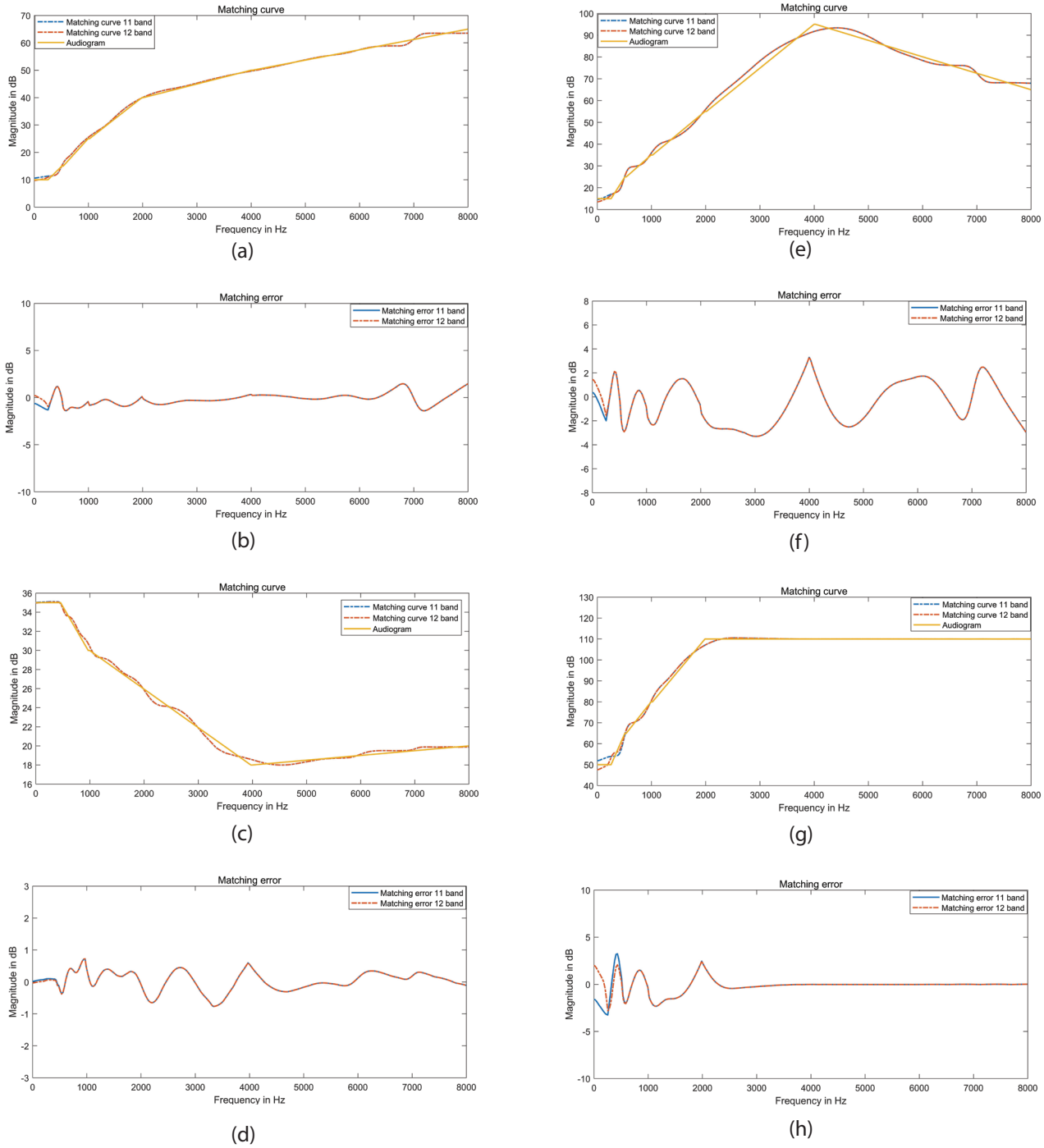


**Figure 8:** Matching Curves and Matching error of different Audiograms (a) & (b) Type 1 (c) & (d) Type 2 (e) & (f) Type 3 (g) & (h) Type 4

ported in the literature. (ii) Only 19 multipliers and 38 adders are required to implement the 11 bands, which makes the proposed structure the computationally efficient than other approaches. (iii) Reasonably better audiogram matching performance especially for Type 1 and Type 2 Audiograms without optimization is achieved. (iv) Acceptable delay performance in all the sampling frequencies, making it suitable for both OHAF and CHAF.

Further study on the proposed work may focus on

(i) Reducing the transition width of filter responses using suitable methods so that sharp prototype filters can be realized at lower order and the number of multipliers can be further reduced (ii) Efficient implementation of the FIR filter structure which uses multiplier less design approaches, coefficient sharing techniques, and other suitable delay reduction techniques (iii) Low power and area efficient VLSI design strategies catering to the need of filter bank implementations suitable for HAs. (iv) Analysis of easy optimization strategies that can be introduced into the software accompanying the HAs for better audiogram matching.

## 5 Conclusion

A computationally efficient 11 band non-uniform filter bank structure suitable for the design of low or moderately sloping SNHL audiograms is proposed. The use of only two prototype filters to implement the 11 subbands makes it suitable for low-cost implementations of filter banks. The FRM method is adopted for the design of the filter bank. In this method, sharp sub-bands are realized using interpolation and masking strategies, makes it suitable for real-time implementations. This technique has a negligible matching error and acceptable group delay. The frequency band splitting is carried out by considering the non-uniform characteristics of the human ear, which has high resolution at lower frequencies. The total number of multipliers required to implement the entire filter bank is 19. This is around 70-90% multiplier saving compared to non FRM methods and around 40-80% multiplier saving compared to FRM methods. Since the filter bank is implemented using a smaller number of multipliers, it can lead to an area and power-efficient implementation of the HAs.

## 6 Conflict of Interest

We have no conflict of interest to declare.

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Arrived: 21. 02. 2020
Accepted: 26. 08. 2020

Original scientific paper
https://doi.org/10.33180/InfMIDEM2020.302

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 50, No. 3(2020), 169 – 177

# Superior Performance of a Negative-capacitance Double-gate Junctionless Field-effect Transistor with Additional Source-drain Doping

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**Abstract:** In this work, we propose a negative-capacitance double-gate junctionless field-effect transistor (NC-JLFET) with additional source-drain doping. Superior performance of the NC-JLFET due to source and drain doping concentration is explained in detail. Additionally, the effects of the drain induced barrier lowering (DIBL) and negative differential resistance (NDR) are precisely analyzed in the NC-JLFET. Sentaurus TCAD simulation demonstrates that the additional source-drain-doped NC-JLFET exhibits a higher on/off current ratio (ION/IOFF) and steeper subthreshold swing (SS < 60 mV/dec) compared to a traditional JLFET. Besides, the negative capacitance effect causes the internal voltage of the gate to be amplified, resulting in negative DIBL and NDR phenomena. Finally, the performance of NC-JLFET can also be optimized by choosing suitable ferroelectric material parameters, such as ferroelectric thickness, coercive field, and remnant polarization. Our simulation study provides theoretical and experimental support for further performance improvement of low-power NCFETs by local structure adjustment.

**Keywords:** Negative-capacitance double-gate junctionless field-effect transistor; additional source-drain doping; on/off current ratio; subthreshold swing; drain induced barrier lowering

# Odlična učinkovitost dvovratnega brezspojnega poljskega tranzistorja z negativno kapacitivnostjo z dodatnim dopiranjem izvor-ponor

**Izvleček:** V članku je predlagan dvovratni brezspojni poljski tranzistor z negativno kapacitivnostjo z dodatnim dopiranjem izvor-ponor (NC_JLFET). Natančno je predstavljena odlična učinkovitost NC_JLFET zaradi dodatnega dopiranja izvora in ponora. Analizirano je znižanje bariere (DIBL) zaradi ponora in negativna diferencialna rezistivnost (NDR). Sentaurus TCAD simulacije kažejo, da dodatno dopiranje izvora in ponora vodi v višjo tokovno razmerje (ION/IOFF) in strmejši podpragovni nihaj (SS< 60 mV/dec). Negativna kapacitivnost povzroča ojačenje notranje napetosti vrat, ki se izkazuje v negativni DIBL in NDR efektu. Učinkovitost NC-JLFET je lahko optimiziran s pravilnimi parametri feroelektričnega materiala, kot je debelina, prisilno polje in preostale polarizacije. Simulacije ponujajo teoretično in eksperimentalno pomoč pri optimizaciji NCFET tranzistorja nizkih moči.

**Ključne besede:** dvovratni brezspojen poljski tranzistor z negativno kapacitivnostjo; dopiranje izvor-ponor; on/off tokovno razmerje; podpragovni nihaj; znižanje bariere

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## 1 Introduction

With the continuous development of integrated circuits (ICs), device sizes have been gradually shrinking. The performance of traditional metal-oxide–semiconductor field-effect transistors is approaching its limit. The off-state leakage current is increasing exponentially caused by the short-channel effect (SCE), resulting in unacceptable static power [1]. At the same time,

it has become difficult for inversion-mode field effect transistors (FETs) (IMFETs) to achieve ultra-deep doping concentration gradients at the device junctions, inducing increasing thermal budget [2]. To overcome these obstacles, some novel device structures have been proposed, including junctionless FETs (JLFETs) and ferroelectric negative-capacitance FETs (NCFETs) [3]-[5].

Compared with traditional inversion-mode transistors, JLFETs have stronger immunity to the SCE [6]. In the actual manufacturing process, there is no super-steep junction, and no additional dopants must be injected into the source and drain regions because the source and drain have the same doping polarity and concentration as the channel. Thus, JLFETs have a simpler manufacturing process and a lower thermal budget than IMFETs [7]. In JLFETs, the majority carriers are conducted in the center of the channel instead of the surface, and the majority carriers in the channel are completely depleted by the gate bias to shut down the device. Moreover, the multigate structure can effectively improve the gate-to-channel control capability, so JLFET devices usually use a double gate to achieve complete channel depletion [8]. It has been verified that the gate metal of JLFETs must have a work function greater than 5.0 eV to completely deplete the Si body to reach the off state [2]. However, it is difficult for a gate metal with a relatively large work function to meet the thermal stability requirement and achieve good adhesion to the gate dielectric [7]-[9]. Therefore, a novel mechanism or structure must be found to overcome this problem.

Since the NCFET was first proposed [4], there have been many reports on both IM and JL structures. A new transistor concept is proposed that combines ultra-thin body and NCFET in [10], It has been proved that performance improvement with low-power NCFETs is realized by amplifying the internal gate voltage caused by the negative-capacitance effect. Hu et al. studied the effects of the variation of ferroelectric material properties (thickness, polarization, and coercivity) on the performance of negative capacitance FETs (NCFETs) in [11]. In our previous studies, we discussed the capacitance matching problem caused by the change of ferroelectric parameters in IM devices, and the performance of NCFET in RF applications [12,13]. Yejoo Choi studied the electrical characteristics of NC-JL-NWFET based on HfO2 through TCAD and MATLAB simulations [14].

In addition, some studies have shown that additional source-drain doping ($N_{S/D}$) of a JLFET can increase the on-state current, but it also causes the higher subthreshold swing (*SS*) and the drain induced barrier lowering (DIBL) effect to become more prominent [15,16]. NCFETs can achieve steep *SS* and improve the DIBL effect, while greatly reducing operating voltage and power consumption [17]-[18]. Therefore, by combining the above two points, the advantages of NCFET can offset the negative effects brought by the additional source-drain doping of JLFET, which can make NC-JLFET have more excellent performance. However, the effect of structure adjustment, such as additional source-drain doping, on the performance of an NC-JLFET has not yet been understood. So, in this work, we construct an NC-JLFET by stacking ferroelectric layers on the gate of the baseline JLFET and investigate the influence of additional source-drain doping on its electrical characteristics. Using Sentaurus TCAD simulation, it is demonstrated that additional source-drain doped NC-JLFETs have improved performance over traditional JLFETs, such as higher $I_{ON}/I_{OFF}$, steeper SS, and negative DIBL.

## 2 Device Structure and Simulation

Figure 1a shows a two-dimensional diagram of an NC-JLFET using a metal-ferroelectric–metal-oxide–semiconductor (MFMIS) structure. The material of the insulating layer is $SiO_2$; the channel, source, and drain are all N-type doped; source, drain, and channel. The channel is uniformly doped and the concentration remains fixed at $1 \times 10^{19}$ cm$^{-3}$. The source and drain are additionally doped with a concentration range of $1 \times 10^{19} - 5 \times 10^{19}$ cm$^{-3}$.

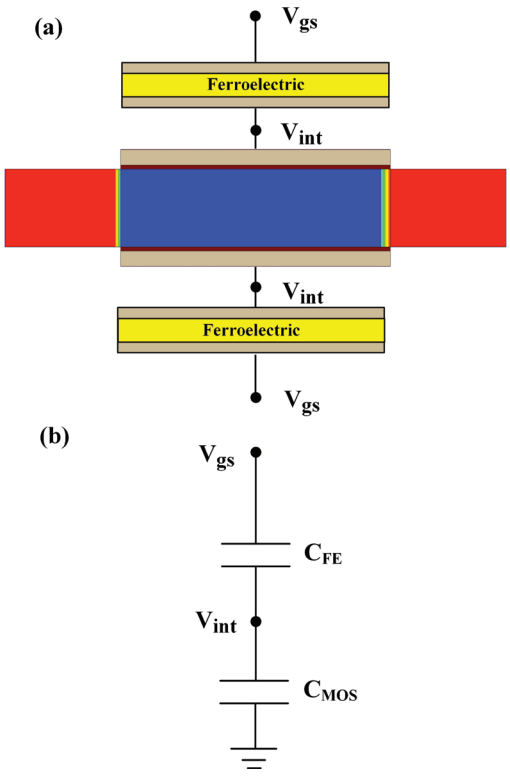


**Figure. 1:** Schematic of (a) NC-JLFET and (b) capacitance equivalent model.

Table I lists other specific device parameters for the proposed NC-JLFET. Among them, the parameters of the baseline transistor JLFET are the gate length *Lg*=28nm, the silicon channel thickness *W*=10nm[14], and the metal work function *WK* is 5.0eV[2], these values of *Pr* and *Ec* are in the same range as those of ferroelectrics such as Hf- and Zr-based binary oxide ferroelectrics[11]. It is assumed that the inner and outer metals have the same work function and that the work function variation is not considered. Figure 1b is a schematic of the equivalent capacitance of the NC-JLFET, where $C_{FE}$ is the ferroelectric layer capacitance and $C_{MOS}$ is the gate equivalent capacitance of the baseline JLFET, including the insulation layer capacitance ($C_{ox}$) and channel depletion capacitance ($C_{dm}$). $V_{gs}$ and $V_{int}$ are the external gate voltage and internal node voltage, respectively. The baseline JLFET is connected in series with the ferroelectric capacitor to form the NC-JLFET. The Landau–Khalatnikov (LK) equation with Gibbs free energy is the standard model of the ferroelectric capacitor, specifically described as the electric field in a ferroelectric as a function of polarization [19]:

$$E_{FE} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho\frac{dP}{dt} \quad (1)$$

where *α*, β, and *γ* are material-dependent parameters of the ferroelectric, α=-3√3/4 x $E_c/P_r$, β=-3√3/8 x $E_c/P_r^3$, and γ = 0 [20], the values of which fit the parameter range in $HfO_2$-based ferroelectrics [21]. The voltage across the ferroelectric capacitor can be obtained from:

$$V_{FE} = \left(2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho\frac{dP}{dt}\right) \times T_{FE} \quad (2)$$

**Table 1:** NC-JLFET device parameters

| Parameter | Physical Meaning | Value |
|---|---|---|
| $L_g$ | Gate length | 28 nm |
| W | Thickness of channel | 10 nm |
| $T_{ox}$ | Oxide thickness | 0.5 nm |
| $T_{FE}$ | Ferroelectric thickness | 1-5 nm |
| WK | Metal work function | 5.0 eV |
| $E_c$ | Coercive field | 1-1.2 MV/cm |
| $P_r$ | Remnant polarization | 3-5 μC/cm² |

Poisson's equation and the continuity equation are solved self-consistently with the LK equation at the same time using Sentaurus TCAD. In simulation, we used some physical models, including doping de-

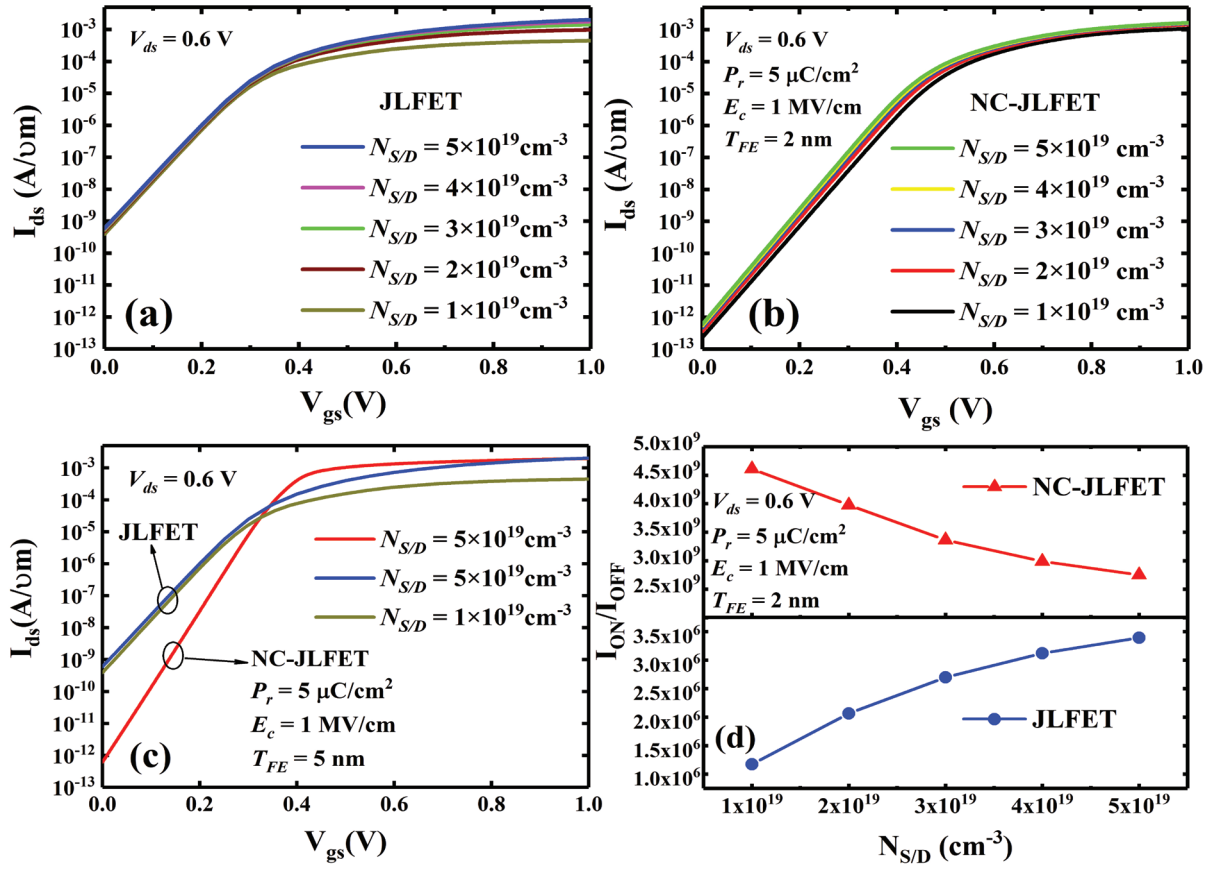


**Figure. 2:** (a) Transfer characteristics of JLFET for different source and drain doping concentrations of source and drain ($N_{S/D}$). (b) Transfer characteristics of NC-JLFET for different source and drain doping concentrations ($N_{S/D}$). (c) Transfer characteristics of NC-JLFET and JLFET. (d) $I_{ON}/I_{OFF}$ with source and drain doping concentrations ($N_{S/D}$).

pendence, high-field saturation (velocity saturation) and considering the silicon bandgap narrowing, the old Slotboom model of band gap narrowing and the Shockley-Read-Hall model for recombination generation are also considered. In view of the highly doped source-drain regions, Fermi (also called Fermi–Dirac) statistics is necessary to make it more physically accurate. In addition, because the device dimension is very small, some quantum modification terms (eQuantum-Potential) are added for the simulation results to be closer to the real condition.

## 3 Results and Discussion

Discussed herein are details of the effects of different source and drain doping concentrations ($N_{S/D}$), ferroelectric thickness ($T_{FE}$), and $E_c$ and $P_r$ values on the on/off current ratio ($I_{ON}/I_{OFF}$), *SS*, DIBL, and output characteristics ($I_{ds}$–$V_{ds}$).

Figures 2a and b show the $I_{ds}$–$V_{gs}$ transfer characteristics of JLFETs and NC-JLFETs with different $N_{S/D}$ values, respectively. It is clear that, as $N_{S/D}$ increases, the on current ($I_{ON}$) increases more and the off current ($I_{OFF}$) is almost constant in JLFETs, but $I_{ON}$ and $I_{OFF}$ both increase slightly in NCJLFETs. Figure 2c is a comparison of the transfer characteristics of NC-JLFET and JLFETs. It is obvious that $I_{OFF}$ is significantly reduced for NC-JLFETs, which leads to the result that the switching characteristic becomes steeper because of the voltage amplifi-

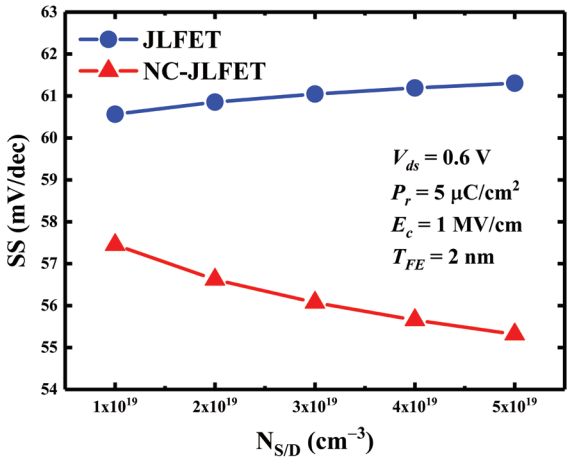


**Figure. 3:** Subthreshold swing (*SS*) of JLFET and NC-JLFET varying with source and drain doping concentration ($N_{S/D}$).

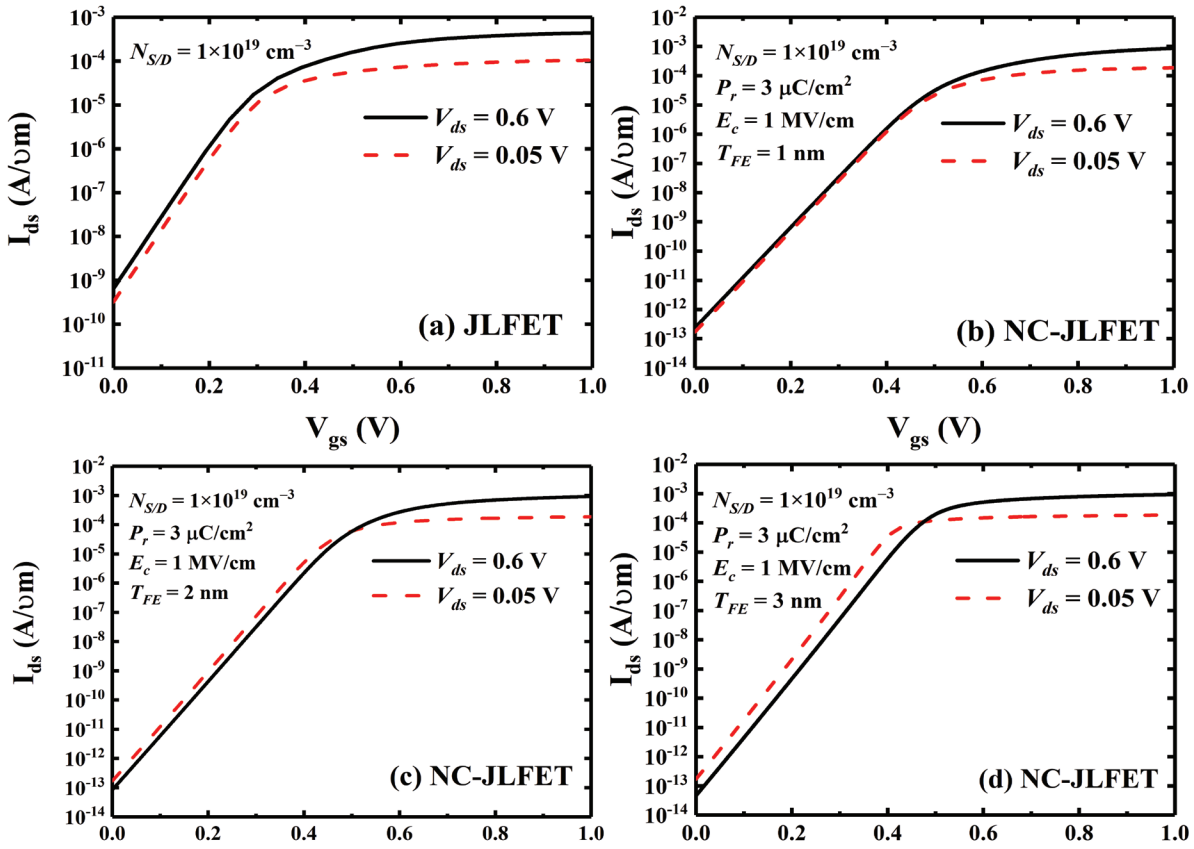


**Figure. 4:** DIBL characteristics of (a) JLFET and NC-JLFET with different ferroelectric thicknesses $T_{FE}$ of (b) 1, (c) 2, and (d) 3 nm.

cation contributed by the ferroelectric layer. As shown in Fig. 2d, the on/off current ratio ($I_{ON}/I_{OFF}$) of JLFETs increases with increasing $N_{S/D}$ because increased $N_{S/D}$ reduces the resistance of the source and drain, which increases the drive current. This trend is also in line with the conclusions obtained in [16,22]. However, for NC-JLFETs, the $I_{ON}/I_{OFF}$ decreases as $N_{S/D}$ increases. This is because increased $N_{S/D}$ values induce doping-dependent electron mobility degradation [14]. Moreover, as the source and drain doping concentrations increase but the channel concentration remains constant, the $I_{ON}/I_{OFF}$ values do not change much. When $N_{S/D} = 5 \times 10^{19}$ cm$^{-3}$, the $I_{ON}/I_{OFF}$ value of the NC-JLFET is still larger than in the JLFET by a factor of nearly $10^3$.

Figure 3 gives the *SS* values of the JLFET and NC-JLFET for different $N_{S/D}$ values. The *SS* in JLFET increases slowly with increasing $N_{S/D}$, but, in the NC-JLFET, *SS* shows a downward trend and all are below 60 mV/dec. These two phenomena can be explained by the following two equations:

$$SS = ln10\frac{kT}{q}\left(1+\frac{C_{dm}}{C_{ox}}\right) \approx 60\times\left(1+\frac{C_{dm}}{C_{ox}}\right) \quad (3)$$

$$SS = 60\times\left(1+\frac{C_{dm}}{C_{ox}}-\frac{C_{dm}}{|C_{FE}|}\right) \quad (4)$$

where $C_{ox}$ is the gate oxide capacitance and $C_{dm}$ is the depletion capacitance. As is well known, in JLFETs, the higher the doping concentration, the larger the $C_{dm}$, and therefore the larger the *SS*. In contrast, in NC-JLFETs, the larger the $C_{dm}$, the greater the increase of $C_{dm}/|C_{FE}|$ compared with the increase of $C_{dm}/C_{ox}$, so the smaller the *SS* will be, that is, less than 60 mV/dec. This is the same as the change trend of *SS* caused by different doping concentrations of NC-JLGAAFET in [14].

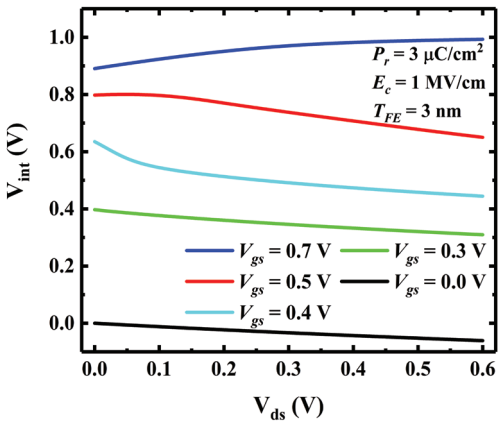


**Figure. 5:** Gate internal voltage ($V_{int}$) versus drain voltage ($V_{ds}$) for NC-JLFET with $T_{FE}$ = 3 nm.

For conventional JLFETs, when the drain voltage ($V_{ds}$) increases, the source-drain depletion layer width is close to the channel length, which reduces the source barrier height. The decrease of the barrier height allows the source electrons to easily cross the barrier to reach the drain, and the channel charge controlled by the gate voltage is reduced, which leads to increased leakage current and lowered threshold voltage. This mechanism is known as the DIBL effect. For traditional JLFETs, increasing $V_{ds}$ will tend to increase current ($I_{ds}$), as can be seen in Fig. 4a. However, for NC-JLFETs, the relationship between the $V_{gs}$ and $V_{int}$ is:

$$V_{int} = V_{gs} - V_{FE} = V_{gs} + |V_{FE}| \quad (5)$$

where $V_{FE}$ is the voltage across the ferroelectric. Owing to drain and channel coupling, when $V_{ds}$ increases, the gate charge decreases, which results in a decrease in $V_{FE}$. In addition, the $V_{int}$ will also decrease, as shown in Fig. 5, which will definitely reduce the channel current intensity. Figures 4b, c, and d show the DIBL characteristics of the NC-JLFET with different $T_{FE}$ values, and it

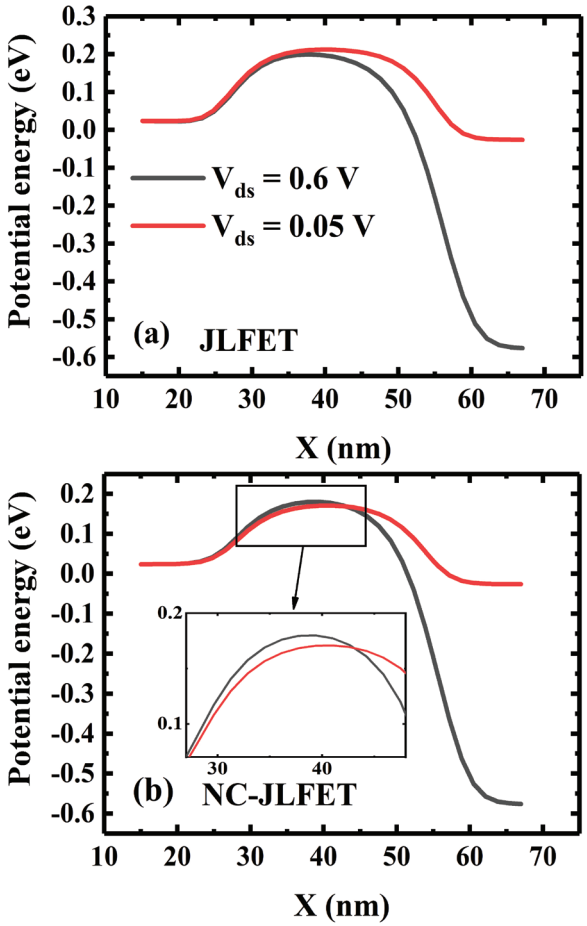


**Figure. 6:** Potential profile at high and low drain voltages ($V_{ds}$). Applied voltage of $V_{gs}$ = 0.3 V. (a) JLFET and (b) NC-JLFET at $T_{FE}$ = 3 nm.

can be clearly seen that negative DIBL characteristics appear when $T_{FE}$ = 2nm and 3 nm.

At the same time, negative DIBL can also be proved by comparing the potential distribution in the channel region of JLFETs and NC-JLFETs as shown in Fig. 6. For a traditional JLFET, the potential barrier height will decrease with increasing $V_{ds}$. For an NC-JLFET, the opposite trend is shown in Fig. 6b. That is, with increasing $V_{ds}$, the height of the barrier near the source will increase causing the negative DIBL phenomenon.

Figure 7 shows the $I_{ds}$-$V_{ds}$ output characteristic of NC-JLFET for different $T_{FE}$ values at $V_{gs}$ = 0.5–0.7 V. As mentioned earlier, when $V_{ds}$ increases, $V_{int}$ decreases, which reduces the drain current. This exhibits a negative differential-resistance (NDR) characteristic as depicted in Fig. 7a. When $V_{gs}$ = 0.5 V, $I_{ds}$ and $V_{ds}$ have a positive correlation in the linear region. As $V_{ds}$ continues to increase, $I_{ds}$ decreases. This NDR effect can also be seen

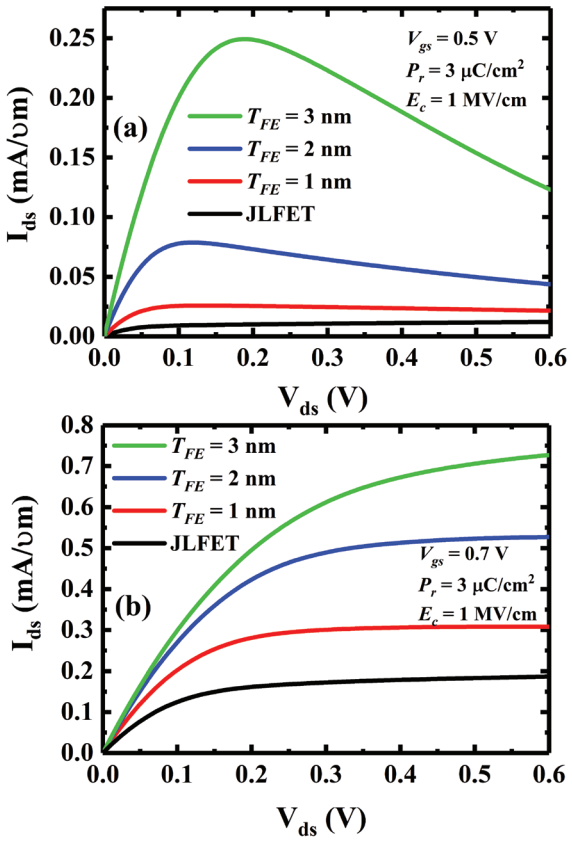


**Figure. 7:** Output characteristics of NC-JLFET for different values of $T_{FE}$ at (a) $V_{gs}$=0.5 V showing NDR and (b) $V_{gs}$ = 0.7 V showing saturation in the ON current.

in the relationship between $V_{int}$ and $V_{ds}$ shown in Fig. 5. However, when $V_{gs}$ = 0.7 V, only a positive correlation exists between $V_{int}$ and $V_{ds}$, so the NDR effect will not appear [see Fig. 7b]. In addition, as the negative DIBL is related to $C_{FE}$, the NDR can be controlled by changing $T_{FE}$. Despite the NDR, an NC-JLFET still provides a larger current than a traditional JLFET. It is worth mentioning that the simulation results of negative DIBL and NDR in our research are consistent with the results of [18].

Figure 8 shows the DIBL values of a JLFET and NC-JLFET for different $N_{S/D}$. It can be clearly seen that as $N_{S/D}$ increases the DIBL effect becomes more serious for the JLFET. This can also be seen in the potential profile diagram. It can be observed from Fig. 9a that the barrier height is significantly reduced when $N_{S/D} = 5\times10^{19}$ cm$^{-3}$, resulting in a more serious DIBL effect. However, for the NC-JLFET, increasing $N_{S/D}$ has little impact on its DIBL, which can also be observed in the potential profile diagram. Figure 9b also shows that $N_{S/D}$ increased from 1 × $10^{19}$ to 5 × $10^{19}$ cm$^{-3}$ and the barrier height shows a downward trend. Due to the negative capacitance effect, the negative DIBL phenomenon still occurs.

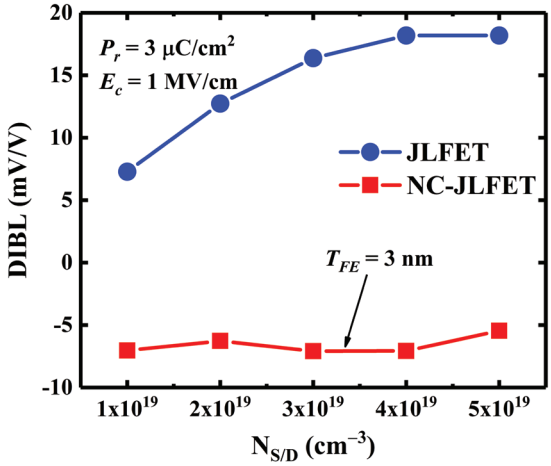


**Figure. 8:** DIBL of JLFET and NC-JLFET varying with source and drain doping concentration ($N_{S/D}$).

Figure 10 exhibits the effect of ferroelectric thickness ($T_{FE}$) on *SS* for different ferroelectric material parameters ($E_c$ and $P_r$). It can be clearly seen that *SS* decreases with increasing $T_{FE}$. This is mainly because as $T_{FE}$ increases, $C_{FE}$ will decrease, which will make $C_{MOS}$ more closely match $C_{FE}$:

$$C_{FE} = \frac{dQ}{dV_{FE}} \approx \frac{1}{2\alpha T_{FE}} = \frac{2}{3\sqrt{3}} \frac{P_r}{E_c T_{FE}} \tag{6}$$

$$A_G = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \tag{7}$$

$$SS = 60 \times (1 + \frac{C_{dm}}{C_{ox}}) \times \frac{1}{A_G} \tag{8}$$

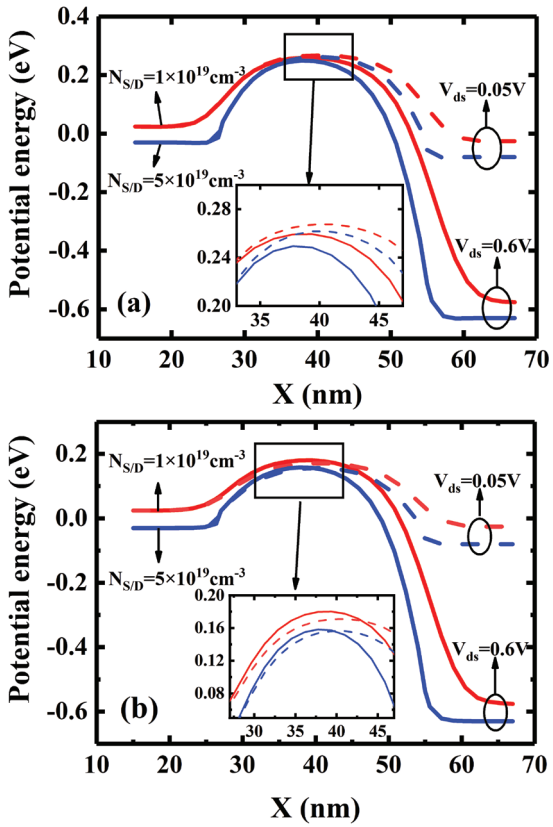


**Figure. 9:** Potential profile for different $N_{S/D}$. Applied voltage of $V_{gs}$ = 0.3V. (a) JLFET and (b) NC-JLFET at $T_{FE}$ = 3 nm.

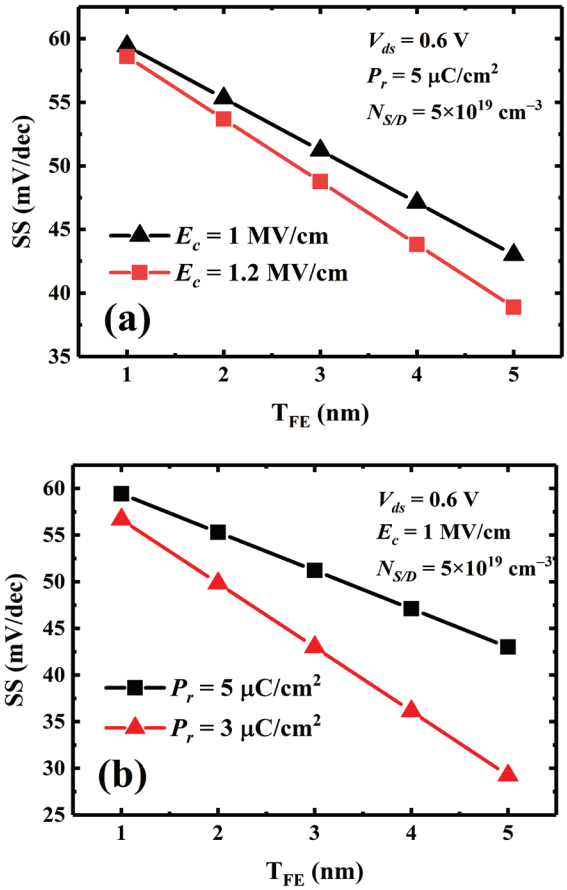


**Figure. 10:** *SS* for NC-JLFET with different (a) $E_c$ and (b) $P_r$ values for different ferroelectric thicknesses ($T_{FE}$).

According to Eq. 7 [23], the voltage amplification factor ($A_G$) increases due to the improved matching between the $C_{MOS}$ and $C_{FE}$ ($|C_{FE}| - C_{MOS} > 0$). The relationship between $A_G$ and *SS* is obtained by Eq. 8 [24], $A_G$ and *SS* have a negative correlation, so *SS* decreases with increasing $T_{FE}$. The relationship between the ferroelectric capacitance ($C_{FE}$) and the ferroelectric material parameters ($E_c$ and $P_r$) is shown in Eq. 6 [11]. When $P_r$ ($E_c$) and $T_{FE}$ remain unchanged, $C_{FE}$ decreases as $E_c$ increases ($P_r$ decreases), and results in lower *SS*. The results obtained in the simulation also conform to this rule, as shown in Fig. 10a and b.

## 4 Conclusions

The electrical performance of a negative-capacitance double-gate junctionless transistor with additional source-drain doping determined by simulation analyses is presented in this paper. It was observed that the negative-capacitance effect and additional source-drain doping can increase the gate voltage and depletion capacitance, respectively, which makes the proposed NC-JLFET have higher $I_{ON}/I_{OFF}$ and lower *SS* values. Then, the NDR and negative DIBL phenomenon are explained through the relationship between internal voltage and gate voltage. In addition, the influence of ferroelectric parameters on the NC-JLFET with additional source-drain doping is explored and shown to have better performance when the proper coercive field, remnant polarization, and ferroelectric thickness are chosen. The additional source-drain doped NC-JLFET studied can achieve superior performance and meet the requirements of low-power IC applications in the future.

## 5 Acknowledgments

This work is supported by Zhejiang Provincial Natural Science Foundation of China (Grant No. LY18F040005), and National Natural Science Foundation of China (Grant No. 61571171, 62071160).

## 6 Conflict of Interest

The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in

the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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Arrived: 04. 06. 2020
Accepted: 28. 08. 2020

Original scientific paper
https://doi.org/10.33180/InfMIDEM2020.303

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 50, No. 3(2020), 179 – 187

# On the Finite-Element Analysis of Resonance MEMS Structures based on Acoustic Lamb Waves

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**Abstract:** This paper considers issues of modeling ultra-high frequency MEMS resonators based on acoustic Lamb waves. In addition, the analysis of factors that determine whether it is possible to increase resonators working frequency and electromechanical coupling factor is carried out. Influence of resonator excitation scheme and acoustic waveguide thickness for a range of piezoelectric materials (i.e. AlN, ZnO, GaN) on phase velocity for acoustic Lamb wave zero modes is investigated. As a result, we've got estimations determining dependence of resonators electromechanical coupling coefficient on their geometry.

**Keywords:** acoustic waves; finite element method; microelectromechanical systems (MEMS); piezoelectric films; microwave resonators

# Analiza končnih elementov resonance MEMS struktur za akustične Lamb valove

**Izvleček:** Članek opisuje problem modeliranja ultra visokih frekvenc MEMS resonatorjev za akustične Lamb valove. Dodatno je bila opravljena analiza faktorjev, ki določajo možnost povečanja delovne frekvence resonatorja in faktor elektromehaničnega sklopljenja. Raziskan je vpliv vzbujalne sheme resonatorja in debeline akustičnega vodnika za različne piezoelektrične materiale (npr. AlN, ZnO, GaN) na fazno hitrost akustičnih Lamb valov v ničelnem modu. Kot rezultat podajamo oceno odvisnosti elektromehanične sklopljenosti resonatorja od njegove geometrije.

**Ključne besede:** akustični valovi; metoda končnih elementov; mikro elektromehanični element (MEMS); piezoelektrične plasti; mikrovalovni resonator

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## 1 Introduction

The growing demand for developing modern space telecommunication devices and constructing new prospective ones, radar and radio navigation systems condition the necessity of substantial working frequency increase of frequency-selective devices. Due to the mentioned above reasons, in recent years most researches have been focused on developing microelectromechanical (MEMS) resonators that have a rather small size, high quality factor values, active device integration function, good resistance to impact and vibration loads and possess many other advantages over the rest of the devices with similar functions [1, 2].

Increase of MEMS resonators working frequencies based on the widely used constructive options involves significant challenges. For instance, resonators based on elements with flexural oscillations reach their scaling limits at frequencies of hundreds of megahertz. It happens because the size needed for higher frequencies is difficult to implement. Moreover, with size decrease the dynamic impedance of such resonators increases, which impedes interfacing with high-frequency devices.

The most prominent way to overcome these limits are resonance structures with contour modes [3-8] that allow implementing micro-resonators with high natural frequencies while dynamic resistance is relatively low, which facilitates the process of matching with RF front-end.

In this resonator type Lamb waves are used as a working acoustic wave. They propagate in thin mechanically isolated piezoelectric film (the thickness does not exceed acoustic wave length) of anisotropic crystals with hexagonal wurtzite-like structure. In particular, these include films of aluminum nitride (AlN), zinc oxide (ZnO) and gallium nitride (GaN) that have piezoelectric response along polar axis C, i.e. perpendicular to the substrate surface (in 0001 direction). Use of piezoeffect provides opportunity to adjust frequency with constant voltage, while single crystal structure and high rigidity provide potentially high quality factor.

One of the main problems in development of MEMS resonators based on Lamb waves in frequency range of gigahertz units is provision of acceptable efficiency of acoustical transformation with working frequency increase.

The aim of this work is to analyze factors that determine possibility of working frequency increase in UHF MEMS resonators based on Lamb waves and to acquire estimations determining dependence of resonators electromechanical coupling coefficient on their geometry.

## 2 Structural and technological implementation of resonators with contour modes

Development of resonators with contour modes involves use of structures with suspended piezoelectric acoustic waveguide. On its surface metal electrodes are formed and constitute interdigital transducers – IDT. You may find an example of micro-resonator structure at Fig. 1.

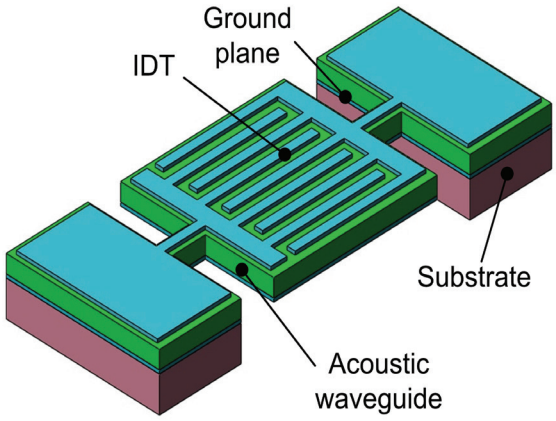


**Figure 1:** Structure of MEMS resonator with contour oscillations.

Use of a suspended structure with free upper and lower boundaries provides an opportunity to excite Lamb waves within an acoustic waveguide featured by vibrational particle displacement in both wave propagation direction (along the acoustic waveguide) and perpendicular to a plate plane.

Change in length, width and position of the electrodes on acoustic waveguide surface allows to set the necessary frequency resonator's properties. Based on electrodes position we can distinguish a range of basic electrode structures implied in single-input (two-pole) resonators with contour modes (Fig. 2) that implement

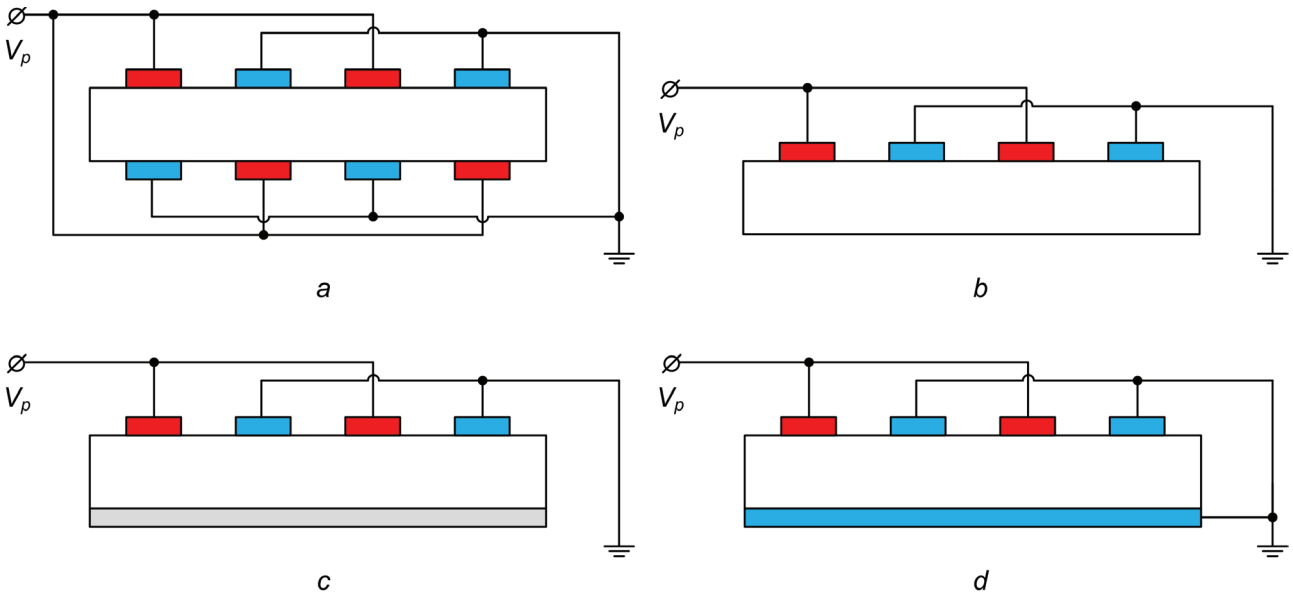


**Figure 2:** Options of electrodes position in single-input resonators: *a* – double IDT, *b* – single IDT, *c* – IDT with floating bottom electrode, *d* – IDT with grounded bottom electrode.

thickness field excitation (TFE) and lateral field excitation (LFE) (Fig. 2, *a* and Fig.2, *b–d* accordingly).

In order to carry out a comparative assessment of micro-resonators we applied a product of working frequency *f* and quality factor *Q*, i.e. an accessory parameter *f·Q* [9]. Fig. 3 shows current results achieved for this parameter. You might notice that working frequencies of MEMS resonators with contour modes may reach the value of 10 GHz. Feasibility of further working frequency increase is limited by the resolution of photolithographic process.

In practice, resonators with contour modes have internal quality characteristic values that do not exceed hundreds of gigahertz. With frequency increase, quality factor usually decreases. The fundamental limit of quality factor increases results in viscous losses in materials, side leakage of acoustic energy and dissipation at microroughness [9–11]. Despite these facts, there is still a way to develop MEMS resonators based on Lamb waves with quality factor of ~5000, applying a special design. To reach this goal a piezoactive layer equipped with IDT should be placed on the acoustic transmission line made of high-quality materials: sapphire [12], silicon carbide SiC [13]. Resonators constructed with the help of this technology are called composite acoustic resonators LOBAR (Lateral Overtone Bulk Acoustic Resonators). Use of a mixed capacitive-piezoelectric conversion mechanism allows implementing resonators with quality factor value over $10^4$ [14].

## *3 Model of wave processes in MEMS resonators based on Lamb waves*

Forming a resonator model implies accepting a list of assumptions. Firstly, it is useful to consider only the coupled elasticity theory and piezoelectricity problem, leaving aside electromagnetic field's properties, regarding it in quasi-static approximation (in comparison to electromagnetic wavelength the structure's size is rather small). Secondly, it is assumed that oscillation amplitude is small and processes in active layer and electrodes materials are described by linear theories of piezoelectricity and elasticity. Finally, bulk forces that affect resonator and internal loss should be omitted; oscillations occur in vacuum.

We will handle this problem in two-dimensional setting, supposing that resonator has an unlimited work field perpendicular to the considered structure section. To analyze acoustic processes let's look at resonator's part of length $L = \lambda$, that contains two exciting electrodes (Fig. 4). Within each one we will acquire solution for coupled electroelasticity problem with relevant boundary conditions.

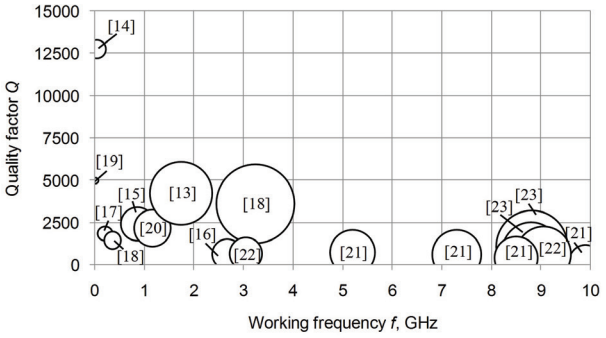


**Figure 3:** Values *f* and *Q* calculated for resonators with contour modes (according to results from [13–23]. Size of „bubbles" reflects resonator's level of quality *f·Q*.

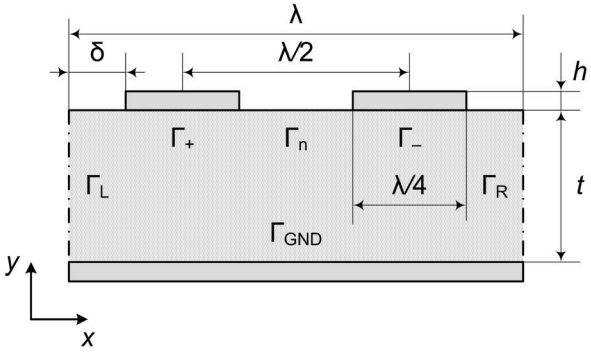


**Figure 4:** Model of Lamb wave micro-resonator's unit cell corresponding to Fig. 2, *c* and Fig. 2, *d*.

System of governing equations for piezoelectric materials that couple mechanical stress **T** and strain **S** to electric field intensity **E** and electric displacement **D** is as follows [24, 25]:

$$\begin{aligned} \mathbf{T} &= \mathbf{c}_E\mathbf{S} - \mathbf{e}\mathbf{E} \\ \mathbf{D} &= \boldsymbol{\varepsilon}_S\mathbf{E} + \mathbf{e}^T\mathbf{S}, \end{aligned} \tag{0}$$

where $\mathbf{c}_E$ is tensor of elasticity coefficients at constant electric field, **e** is tensor of piezoelectric constants, $\varepsilon_S$ is tensor of dielectric constants measured in presence of constant strains, *T* denotes matrix transposition.

Boundary conditions on exciting electrodes surfaces (see Fig.4) constitute Dirichlet condition for electric potential φ:

- $\varphi = \varphi_p$ for the sector of the boundary $\Gamma_+$, $\varphi = -\varphi_p$ for the sector of the boundary $\Gamma_-$,
- $\varphi = 0$ at grounded bottom metallization $\Gamma_{GND}$ (Fig. 2, *c*),
- $\varphi$ = const at bottom metallization with floating potential $\Gamma_{FP}$ (Fig. 2, *c*).

Boundary conditions that constitute continuity of normal components of electric displacement vector are set at left and right unit cell boundaries ($\Gamma_L$, $\Gamma_R$ sectors at Fig. 4):

$$\mathbf{n}\cdot\mathbf{D}_{x=0} = \mathbf{n}\cdot\mathbf{D}_{x=L}, \quad (1)$$

continuity of electric field tangential components:.

$$V_{x=0} = V_{x=L}, \quad (2)$$

continuity of normal mechanical stresses:

$$\mathbf{n}\cdot\mathbf{T}_{x=0} = \mathbf{n}\cdot\mathbf{T}_{x=L}, \quad (3)$$

and continuity of mechanical displacements:

$$u_{x=0} = u_{x=L}, \quad (4)$$

For metallization-free sectors of piezoelectric surface, we set Von Neumann boundary conditions that describe lack of currents flowing across the boundary:

$$\mathbf{n}\cdot\mathbf{D} = 0, \forall N\{x,y\} \in \Gamma_{\mathrm{n}}, \quad (5)$$

and Von Neumann condition for normal surface voltage level:

$$\mathbf{n}\cdot\mathbf{D} = 0, \forall N\{x,y\} \in \Gamma_{+}, \Gamma_{-}, \Gamma_{\mathrm{GND}}, \Gamma_{\mathrm{n}}, \quad (6)$$

where **n** is a vector of unit external normal to the surface.

Analysis of the wave pattern determining resonance structure processes was carried out to identify types of excited waves and to assess correspondence of model and physical processes flowing in micro-resonators. Determination of micro-resonators natural frequencies and oscillation modes was carried out for structures based on AlN, ZnO and GaN. Parameters of the materials used for calculations are presented in Table 1. Behavior of hexagonal crystals AlN, ZnO, GaN is characterized by five independent elastic constants – $C_{11}$, $C_{12}$, $C_{13}$, $C_{33}$, $C_{44}$, three independent piezoelectric constants – $e_{15}$, $e_{31}$, $e_{33}$ and two independent dielectric constants – $\varepsilon_{11}$, $\varepsilon_{33}$. Three independent elastic constants that are needed to describe cubic crystals Al are $C_{11}$, $C_{12}$, $C_{44}$

Calculations were carried out using finite element method (FEM) of ANSYS software package [24,25]. FEM procedures were performed in ANSYS APDL language with the help of two-dimensional finite element PLANE223 with degrees of freedom UX, UY, VOLT. Finite element description acquired in parametric form allows varying model's geometric parameters and materials physical properties, calculating resonators structures with different electrodes position options (see Fig. 2, *a–d*). As a result of modal analysis, we obtained resonators natural frequencies and corresponding oscillation modes representing the relative amplitudes of displacements at finite-element mesh nodes.

If you look at Fig. 5, you may see first four oscillation modes of resonance structure based on aluminum nitride (the structure with single IDT and a grounded bottom electrode – Fig. 2, *d*, the working wavelength $\lambda \approx 4$ μm, thickness of top and bottom Al-electrodes is 0.1 μm). The figure shows characteristic features of Lamb waves: wave pattern is featured by two components of vibrational displacement, one of which is parallel and the other is perpendicular to the acoustic transmission line surface. Modes, that differ in motion of resonator's top and bottom surfaces in the same and opposite directions, belong to symmetric and asymmetric Lamb modes respectively.

The problem of micro-resonator electrode system topology choice is closely connected to the problem of determination of acoustic waves phase speed in thin piezoelectric's plate at frequencies corresponding to the natural modes.

**Table 1:** Parameters of the materials used for calculations [15, 26, 27].

| Parameter | | AlN | ZnO | GaN | Al |
|---|---|---|---|---|---|
| Density, kg/m$^3$ | | 3260 | 5700 | 6150 | 2700 |
| Poisson ratio | | 0.287 | 0.36 | 0.352 | 0.3 |
| Elastic constants, GPa | $C_{11}$ | 345 | 210 | 390 | 112 |
| | $C_{12}$ | 125 | 121 | 145 | 60 |
| | $C_{13}$ | 120 | 105 | 106 | – |
| | $C_{33}$ | 395 | 211 | 398 | – |
| | $C_{44}$ | 118 | 43 | 105 | 44 |
| | $C_{66}$ | 110 | 44.5 | 122.5 | – |
| Piezoelectric constants, C/m$^2$ | $e_{15}$ | –0.48 | –0.48 | –0.3 | – |
| | $e_{31}$ | –0.58 | –0.57 | –0.33 | – |
| | $e_{33}$ | 1.55 | 1.32 | 0.65 | – |
| Relative dielectric permitivity | $\varepsilon_{11}$ | 9.04 | 8.6 | 9.5 | – |
| | $\varepsilon_{33}$ | 11.2 | 10 | 10.4 | – |

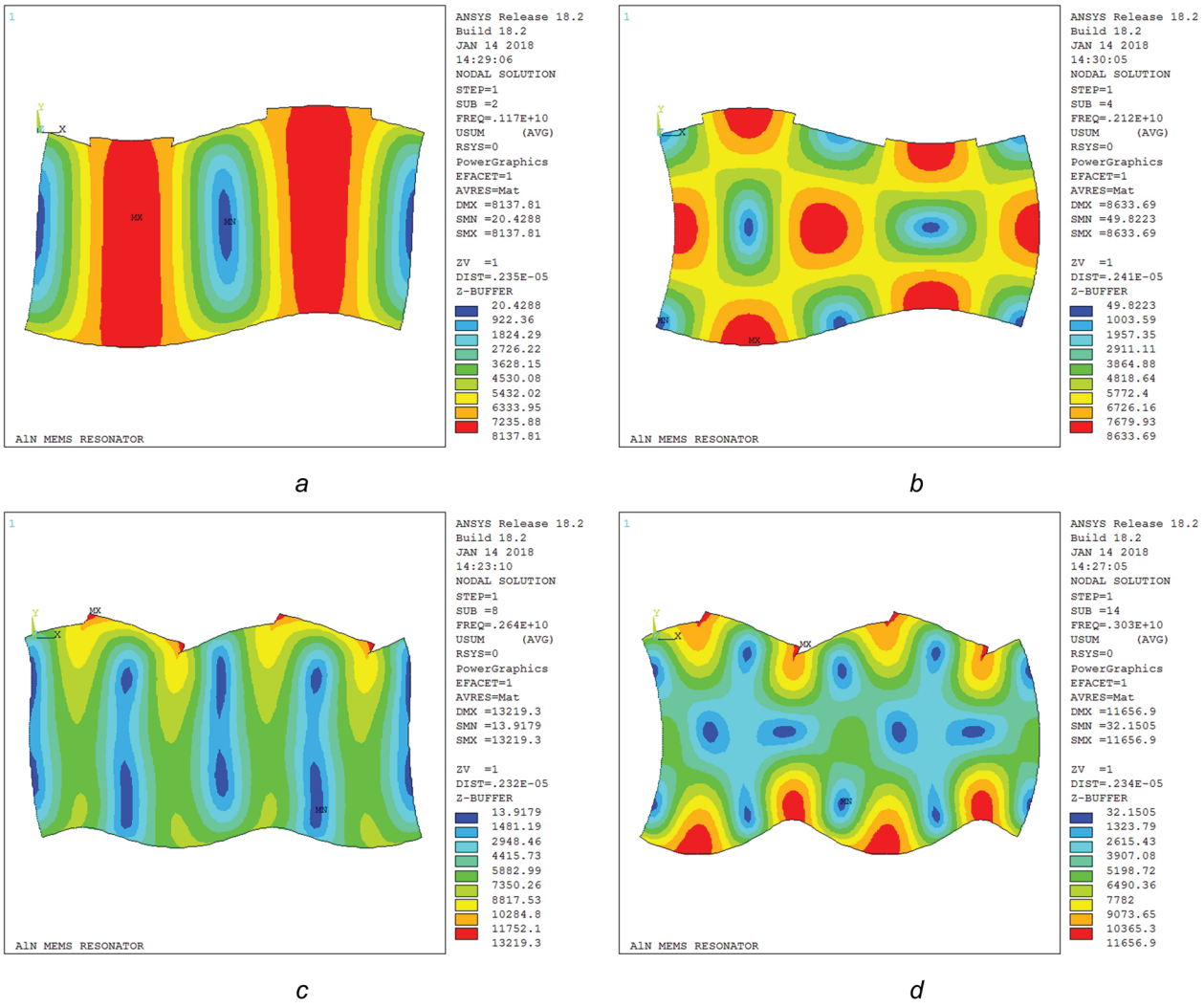


**Figure 5:** Lamb modes in the structure based on AlN: *a* – asymmetric $A_0$ (1.17 GHz), *b* – symmetric $S_0$ (2.12 GHz), *c* – asymmetric $A_1$ (2.64 GHz), *d* – symmetric $S_1$ (3.03 GHz).

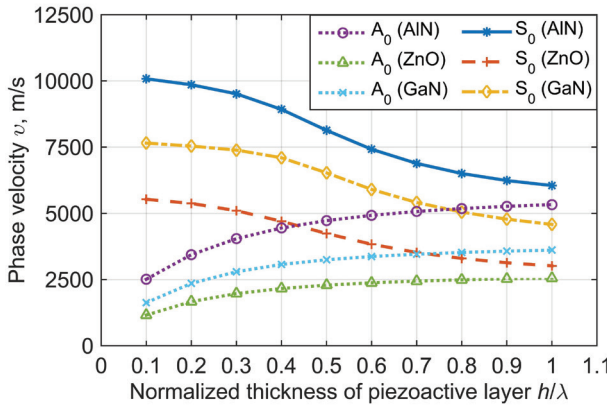


**Figure 6:** Dependence of Lamb wave propagation phase velocity for zero symmetric mode in film made of AlN, ZnO and GaN with orientation (0001) from their relative thickness (calculations are made for single IDT with grounded bottom electrode, thickness of top and bottom Al-electrodes is 0.1 μm, variable parameter is acoustic waveguide thickness *t*).

The dependence represented in Fig.6 allows determining spatial period *p* between antiphase excited IDT electrodes from the selected excitation frequency *f* and the corresponding phase velocity $\upsilon_0$: $p = \upsilon_0 / (2f)$.

The results show that zero symmetric Lamb mode $S_0$ has the main practical value in terms of working frequency increase of micro-resonators with contour modes. In case of aluminum nitride use the wave velocity for this mode may reach the value of 10000 m/s with small relative thickness of film – $t/\lambda < 0.2$. Acoustic wave velocity in structures based on GaN and ZnO is much lower, as a result the size of resonators may be extremely small. With the same electrodes spatial period, working frequency of aluminum nitride resonators is 1.3 times higher than working frequency of GaN resonators and almost twice higher than that of ZnO resonators.

## 4 Calculation of electromechanical coupling coefficients

One of the main issues during development of resonator elements with high *f*·*Q* is provision of efficient transformation of electric signals into acoustic ones and vice versa. Aside from piezoelectric properties of material's active layer it is also determined by IDT configuration, electrodes thickness and piezoelectric film ratio, and other design parameters. The best combination of these connected parameters can be obtained by taking an electromechanical coupling effective coefficient as an optimization criterion.

The value of the effective coupling coefficient can be set by calculating frequencies of (resonance) pole and (antiresonance) zero of input micro-resonator's admittance [4, 28]:

$$k_{\text{eff}}^2 = \frac{\pi^2}{4}\frac{f_s}{f_p}\frac{f_p - f_s}{f_p}, \tag{7}$$

where $f_s$ and $f_p$ are series and parallel resonance frequencies respectively.

Frequencies $f_s$ and $f_p$ can be found using the harmonic analysis procedure, allowing to determine steady vibrations – resonator's response to the electric harmonic action applied to it with given amplitude and frequency. To acquire frequency dependence of resonator's admittance *Y*(*f*) we calculated the values of *Y* for a given frequency from the charges induced on electrodes (or current flowing through electrodes) found on the basis of a modal analysis and corresponding electric potential.

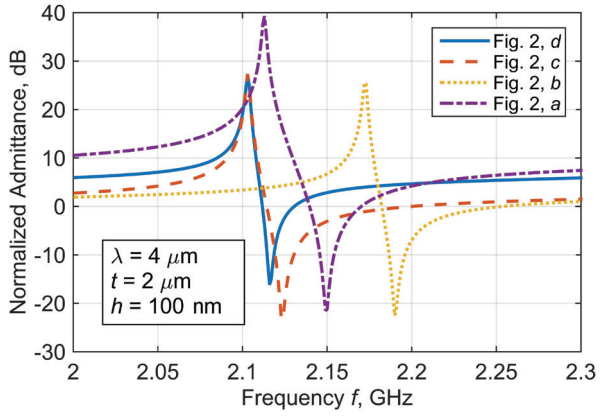


**Figure 7:** Frequency dependences of conductivity module (normalized to conductivity unit) of a single input AlN-resonator designed for center frequency of 2.72 GHz for different electrode location options. Thickness of top and bottom Al-electrodes is 0.1 μm, thickness of piezoelectric layer AlN is 2 μm. ξ = 0.0005.

During computational experiments in the ANSYS package, value of damping parameter ξ (using DMPRAT command) was set based on theoretical limit value of resonator's quality factor $Q_m$ determined by mechanical quality factor of acoustic transmission line material (1500–2500 for aluminum nitride and 1000 for zinc oxide and gallium nitride):

$$\xi = \frac{1}{2\text{Qm}}, \tag{8}$$

At the charts (Fig. 7) obtained after modelling you may see that conductivity module frequency dependences |*Y*(*f*)| pass through a minimum at preliminary resonance frequency $f_s$ and pass through maximum at parallel resonance $f_p$.

Figures 8 shows dependencies $k_{\text{eff}}^2$ calculated in accordance with (7) for symmetric mode $S_0$ in films of (0001) AlN, ZnO and GaN from relative thickness of piezoactive layer *t*/λ for different electrode location options (Fig.2).

## 5 Results

As follows from the results, electrode structure with double IDT (Fig. 2, *a*) has the highest acoustical transformation efficiency and single IDT with grounded bottom electrode (Fig. 2, *d*) has the lowest acoustical transformation efficiency. In aluminum nitride film (Fig. 8) electromechanical coupling coefficient for mode $S_0$ in resonators with double IDT reaches its maximum at film relative thickness of *t*/λ ≈ 0.4 and has a value ~ 5%. As you may see at Fig. 8, in the structure based on zinc oxide coupling coefficient may be higher (~ 11.5% at *t*/λ ≈ 0.3).For GaN the coupling coefficient is the lowest (~ 1% at *t*/λ ≈ 0.4).

## 6 Discussion

As calculations demonstrated, double IDT (Fig. 2, *a*) provides the highest electromechanical coupling coefficient value and maximum distance between adjacent resonant frequencies. The increase in coupling coefficient can be attributed to the better match of the working mode shape to the electrode placement inherent in this design. Besides the higher excitation efficiency, double IDT provides significantly lower level of extraneous waves excitation (Fig. 9). Excitation of extraneous oscillations along with working mode leads to resonator's quality factor decrease. At *t*/λ = 0.5 working oscillation mode $S_0$ is excited above all, while the rest of modes are largely suppressed (for double IDT).

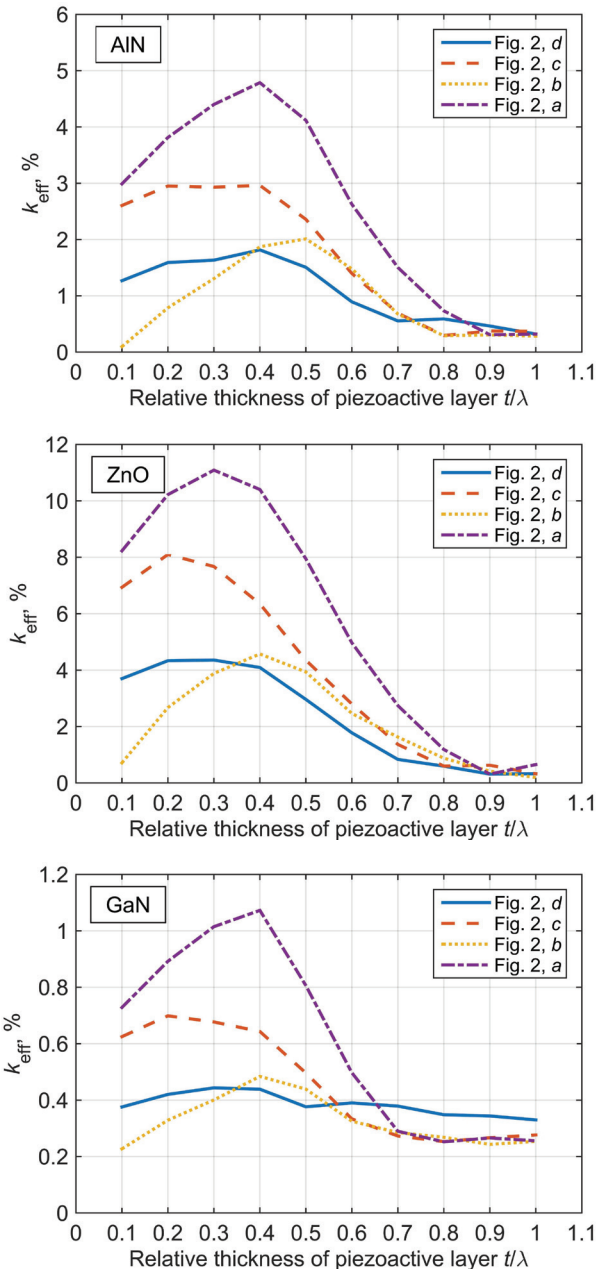


**Figure 8:** Dependence of electromechanical coupling coefficient value for zero symmetric Lamb mode $S_0$ from piezoactive layer thickness referred to working wavelength $\lambda \approx 4$ μm for different acoustic transmission line materials.

At the same time, construction of double IDT resonators is troubled by difficulties associated with technological process, i.e. difficulties of high-quality piezoelectric film growing and inaccuracies in top and bottom photolithographic templates combination.

Single IDT resonators stand out for the simplest technology that requires minimum photomasks and, as a result, less manufacturing phases. Therefore, at frequencies higher than 1 GHz, where growing piezoelectric layer quality requirements obstruct double IDT structures implementation, it is more appropriate to implement single IDT.

## 7 Conclusions

According to the results, we may determine the main constructive solutions that allow to create single input MEMS resonators based on Lamb waves with suspended structure at gigahertz wavelength range.

Results of numerical analysis show that double IDT resonators, which electrodes are placed at the top and the bottom of suspended piezoelectric layer, allow reaching higher electromechanical coupling factor values in comparison to single IDT options. Implementation of double IDT structures is more complex than implementation of single IDT ones.

As working frequencies increase and restriction of requirements for combination accuracy and technology resolution while micro-resonators manufacturing, it seems more appropriate to use single IDT structures. Resonator's working frequencies may be increased by 5-10 GHz using higher modes.

## 8 Acknowledgments

The authors thank Filipp A. Baron for critical reading of manuscript, fruitful discussions and valuable input.

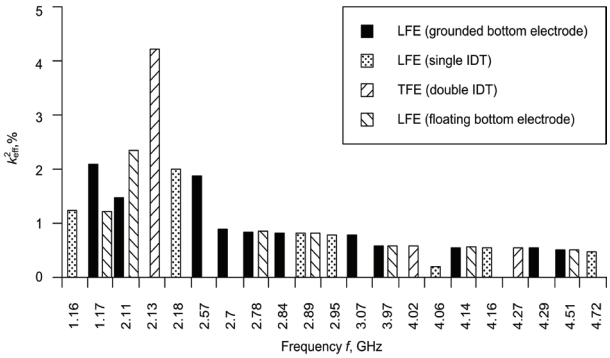


**Figure 9:** Histogram of the $k^2_{\text{eff}}$ dependency from frequency for different resonator excitation circuits (Fig. 2). Acoustic transmission line material is aluminum nitride, $t/\lambda = 0.5$. Each histogram column's height represents a value of coupling coefficient at corresponding natural frequency.

## 9 Conflict of interest

The authors declare no conflicts of interests.

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Arrived: 06. 11. 2020
Accepted: 08. 09. 2020

Original scientific paper
https://doi.org/10.33180/InfMIDEM2020.304

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 50, No. 3(2020), 189 – 203

# Novel Electronically Tunable Biquadratic Mixed-Mode Universal Filter Capable of Operating in MISO and SIMO Configurations

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**Abstract:** In this paper, a novel electronically tunable biquadratic universal mixed-mode filter is presented. The filter is based on extra X current conveyor transconductance amplifier (EXCCTA), recently introduced by authors. The proposed filter employs two EXCCTAs, two capacitors, a switch, and four resistors. The filter can work in both multi-input-single-output (MISO) and single-input-multi-output (SIMO) configurations without change in its structure. The filter provides all five responses in voltage-mode (VM), current-mode (CM), transimpedance-mode (TIM), and transadmittance-mode (TAM). The attractive features of the filter include (i) ability to operate in both MISO and SIMO configurations in all four modes, (ii) no requirement of capacitive matching, (iii) tunability of quality factor (*Q*) independent of natural frequency ($\omega_0$) in MISO & SIMO configurations and (iv) no requirement for double/negative input signals (voltage/current) in MISO configuration. The non-ideal gain and sensitivity analysis is also carried out to study the effects of process variations and passive components spread on filter performance. The filter is designed in Cadence Virtuoso using Silterra Malaysia 0.18μm PDK. The complete layout of the EXCCTA is designed and the parasitic extraction is done. The filter is tested at a supply voltage of ±1.25 V and the obtained results validate the theoretical findings.

**Keywords:** analog signal processing, voltage-mode, current-mode, transimpedance-mode, transadmittance-mode, extra X current conveyor transconductance amplifier, EXCCTA, universal filter

# Nov elektronsko nastavljiv bikvadratičen univerzalen filter v mešanem načinu delovanja sposoben delovanja v MISO in SIMO konfiguraciji

**Izvleček:** Članek predstavlja nov elektronsko nastavljiv bikvadratičen filter v mešanem načinu delovanja. Filter sloni na dodatnem X tokovnem transkonduktančnem ojačevalniku (EXCCTA). Filter je sestavljen iz dveh EXCCTA-jev, dveh kondenzatorjev, stikala in štirih tranzistorjev. Filter lahko deluje v eno-vhodni multi izhodni (MISO) ali multi-vhodno eno-izhodni (SIMO) konfiguraciji brez spremembe v strukturi. Ponuja vseh pet odzivov v napetostnem (VM), tokovnem (CM), transimpedančnem (TIM) in transadmitančnem načinu (TAM). Prednostne lastnosti filtra so (i) delovanje v MISO ali SIMO načini, (ii) ni potrebe po kapacitivnem ujemanju, (iii) nastavljivost faktorja kvalitete (*Q*) brez odvisnosti od osnovne frekvence v MISO in SIMO načinu in (iv) brez potrebe po dvojnem negativnem vhodu signal v MISO načinu. Opravljena je tudi analiza občutljivosti in ojačenja filtra zaradi variacij procesa in toleranc pasivnih komponent. Filter je narejen v Cadence Virtuoso z uporabo Silterra Malaysia 0.18μm PDK. Načrtano je celotna shema EXCCTA in opravljen test pri napajalni napetosti ±1.25 V.

**Ključne besede:** analogno procesiranje signalov, EXCCTA, univerzalen filter, transkonduktančni tokovni ojačevalnik

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## 1 Introduction

The design and development of frequency filters is an important field of communication engineering and research. The filters are an integral part of almost every electronic system [1–3]. The universal filter structure is the most versatile and sought-after filter configuration as it provides all five generic filter responses namely, low-pass (LP), high-pass (HP), band-pass (BP), band-reject (BR), and all-pass (AP) from same configuration. It serves as a stand-alone solution for all filtering requirements. They are employed in data acquisition systems as analog front-end, in communication systems, biomedical signal processing, instrumentation, and oscillator design, etc. [3-15]. Owing to their wide bandwidth, high slew-rate, simple circuit, good linearity, and better performance under low-voltage low-power (LVLP) environment current-mode (CM) active building blocks (ABBs) are preferred for designing analog filters [2,5,6]. The most popular CM ABBs are the second-generation current conveyor (CCII) [1-6], current feedback operational amplifier (CFOA) [16], fully differential current conveyor (FDCCII) [18], differential voltage current conveyor (DVCC) [20], current controlled current conveyor transconductance amplifier (CCCCTA) [21], differential difference current conveyor (DDCC) [23], etc. In present day complex signal processing systems the need for interaction between current-mode and voltage-mode (VM) circuits arises often. This requirement can be met by employing transadmittance-mode (TAM) and transimpedance-mode (TIM) circuits to facilitate distortion free interfacing between CM and VM units [7–11, 23]. Although several TAM and TIM filter structures have been proposed, but a single topology providing the CM, VM, TAM, and TIM responses will be an added advantage in terms of area and power requirements. Numerous mixed-mode universal filters can be found in the open literature [7-34] that were designed to cater to the above-mentioned requirements. The filter structures can be classified in three basic groups such as single-input-multi-output (SIMO), multi-input-multi-output (MIMO), and multi-input-single-output (MISO). The comparison between the filter structures can be done based on following important criteria:

**Table 1:** Comparative study of the state-of-the-art mixed-mode designs with the proposed filter

| References/ Year | Mode of Operation | (i) | (ii) | (iii) | (iv) | (v) | (vi) | (vii) | (viii) | (ix) | (x) | (xi) | (xii) | (xiii) | (xiv) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| [16]/2005 | SIMO | 3-CFOA | 9C+2R | Yes | No | Yes | No | Yes | No | Yes | N.A. | N.A. | N.A. | 112.5 KHz | No |
| [17]/2006 | SIMO | 2-FTFN | 2C+3R | Yes | Yes | No | No | Yes | No | No | N.A. | N.A. | N.A. | 31.8 KHz | No |
| [18]/2008 | SIMO | 1-FDCCII | 2C+3R | Yes | Yes | Yes | Yes | No | Yes | No | N.A. | N.A. | N.A. | 3.78 MHz | No |
| [19]/2008 | SIMO | 5-MOCCCII | 2C | Yes | Yes | Yes | Yes | No | Yes | No | N.A. | N.A. | N.A. | 638.4 KHz | Yes |
| [20]/2009 | SIMO | 3-DVCC | 2C+3R | Yes | Yes | Yes | Yes | Yes | Yes | No | N.A. | N.A. | N.A. | 16 MHz | No |
| [21]/2010 | SIMO | 2-CCCCTA | 2C | Yes | Yes | Yes | Yes | No | No | No | N.A. | N.A. | N.A. | 1.134 MHz | Yes |
| [22]/2010 | SIMO | 2-CCCCTA | 2C | Yes | Yes | Yes | No | Yes | No | No | N.A. | N.A. | N.A. | 1.63 MHz | Yes |
| [23]/2011 | SIMO | 3-DDCC | 2C+4R | Yes | Yes | Yes | Yes | No | Yes | Yes | N.A. | N.A. | N.A. | 3.97 MHz | No |
| [24]/2017 | SIMO | 3-CCCCTA | 2C | Yes | Yes | Yes | Yes | Yes | Yes | Yes | N.A. | N.A. | N.A. | 3.183 MHz | Yes |
| [25]/2017 | SIMO | 3-VDTA | 2C | Yes | N.A. | Yes | Yes | N.A. | Yes | No | N.A. | N.A. | N.A. | 3.04 MHz | Yes |
| [26]/2017 | SIMO | 6-OTA | 2C | Yes | Yes | Yes | Yes | No | No | Yes | N.A. | N.A. | N.A. | 1.5 MHz | Yes |
| [27]/2017 | SIMO | 1-DVCC+ 1-MOCCII | 2C+3R | Yes | No | Yes | Yes | No | Yes | No | N.A. | N.A. | N.A. | 1.59 MHz | No |
| [36]/2016 | SIMO | 2-FDCCII | 2C+5R | Yes | Yes | Yes | Yes | No | No | Yes | N.A. | N.A. | N.A. | 1.59 MHz | No |
| [37]/2018 | SIMO | 2-FDCCII | 2C+4R | Yes | Yes | Yes | Yes | No | No | Yes | N.A. | N.A. | N.A. | 1.59 MHz | No |
| [28]/2004 | MISO | 7-CCII | 2C+8R | Yes | Yes | N.A. | N.A. | N.A. | No | Yes | No | Yes | Yes | - | No |
| [29]/2006 | MISO | 3-CCII | 3C+4R+ 2-switch | No | No | N.A. | N.A. | N.A. | No | Yes | No | Yes | Yes | - | No |
| [30]/2009 | MISO | 4-OTA | 2C | Yes | Yes | N.A. | N.A. | N.A. | No | Yes | No | Yes | No | 1.59 MHz | Yes |
| [31]/2010 | MISO | 2-MOCCCII | 2C+2R | Yes | Yes | N.A. | N.A. | N.A. | Yes | Yes | No | Yes | Yes | 1.27 MHz | Yes |
| [32]/2013 | MISO | 4-MOCCCII | 2C | Yes | Yes | N.A. | N.A. | N.A. | No | Yes | Yes | Yes | No | - | Yes |
| [33]/2016 | SIMO/ MISO | 1-FDCCII+ 1-DDCC | 2C+6R | Yes | Yes | Yes | Yes | Yes | Yes | Yes | No | Yes | No | 1.59 MHz | No |
| [34]/2018 | MISO | 5-DVCC | 2C+5R | Yes | Yes | N.A. | N.A. | N.A. | Yes | No | No | Yes | Yes | 1 MHz | No |
| Proposed | MISO/ SIMO | 2-EXCCTA | 2C+4R+ switch | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | 8 MHz | Yes |

*N.A. (not applicable) [points (v)-(vii) are not applicable in case of MISO filters, points (x)-(xii) are not applicable in case of SIMO filters, point (iv) is not applicable in case of resistor less filters]

(i) number of ABBs employed,
(ii) number of passive components needed,
(iii) no need for capacitive matching,
(iv) no requirement for resistive matching except for AP response,
(v) use of grounded capacitors in SIMO configuration,
(vi) availability of explicit current output from high impedance node in SIMO configuration,
(vii) low input impedance for CM and TIM in SIMO configuration,
(viii) provision to control quality factor independent of the natural frequency,
(ix) ability to provide all five filter responses in all four modes of operation,
(x) low output impedance for MISO (VM and TIM),
(xi) availability of explicit current output for MISO (CM and TAM),
(xii) no requirement for double/negative input signals (voltage/current) in MISO configuration,
(xiii) test natural frequency,
(xiv) inbuilt tunability.

A detailed comparison of the state-of-the-art mixed-mode filters with the proposed design is presented in Table 1.

It can be inferred from the table that the filter structures [16, 19-26, 28-30, 32, 34] employ three or more ABBs for the design. The designs in [16, 28, 29, 33, 34] utilize seven or more passive components. The design in [29] requires capacitive matching, which is undesirable in today's submicron technologies. In filters [16-17, 21, 22, 26, 28-30, 32] the quality factor cannot be controlled independent of the natural frequency. The filter structures [17-22, 25, 27, 34] are not truly universal mixed-modes since they cannot realize all five filter responses in VM, CM, TAM and TIM operation. None of the above mixed-mode filters except [20] is designed at natural frequency higher than 4 MHz. The filter structures [16-18, 20, 23, 27-29, 33, 34] lack inbuilt tunability. None of the existing filters (with the exception of [33]) can work in both MISO and SIMO configurations and provide all five filter responses in all Four modes of operation. In addition, some other drawbacks of the design [33] are: (i) the design is not modular as it uses two different ABBs, namely FDCCII and DDCC, also it requires five input voltages and six input currents in MISO configuration, (ii) both capacitors are connected to X terminals which is undesired as it effects the high frequency performance as shown in [35], (iii) use negative and double inputs in MISO configuration, and (iv) lack of built-in tunability. The literature survey points out that although many exemplary mixed-mode filter designs exists, the research in the mix-mode filter design is still limited and newer designs need to be developed to cater to increasing demand of mixed-signal processing systems. In context, this paper aims to introduce a novel mixed-mode filter structure composed of two extra X current conveyor transconductance amplifier (EXCCTA), one switch, two capacitors, and four resistors, which employs only three input current/voltage signals in MISO operation and is free from the above drawbacks of [33]. The striking features of the proposed filter are: (i) provides all five filter responses in all four modes of operation, (ii) it can work in both MISO and SIMO configuration without change in topology, (iii) it has inbuilt tunability, and (iv) the filter exhibits low active and passive sensitivities to passive elements. Beside these the filter enjoys all the properties mentioned in Table 1. The precise design, layout and simulation of the EXCCTA, is done in Cadence Virtuoso using Silterra Malaysia 0.18µm PDK. The layout verification and parasitic extraction is carried out using Mentor Graphics Calibre. The post layout results bear close resemblance with the theoretical predictions.

## 2 Extra X current conveyor transconductance amplifier (EXCCTA)

The EXCCTA is a versatile electronically tunable ABB carrying features of extra X current conveyor (EXCCII) [13] and operational transconductance amplifier (OTA) [14] in one compact integrated circuit implementation. The EXCCTA provides two independent low impedance current input terminals $X_{P,N}$ together with a high impedance voltage input terminal Y. It also has OTA at the output stage imparting tunability to the structure. The block diagram and voltage-current relations of the EXCCTA are given in Figure 1 and Equation (1), respectively. The complete CMOS implementation [15] is presented in Figure 2. The class AB output stage is utilized in the first stage to minimize supply voltage and power dissipation.

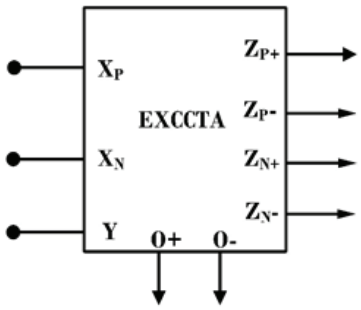


**Figure 1:** Block diagram of EXCCTA

$$\begin{bmatrix} I_Y \\ V_{XP} \\ V_{XN} \\ I_{ZP+} \\ I_{ZP-} \\ I_{ZN+} \\ I_{ZN-} \\ I_{O\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{XP} \\ I_{XN} \\ V_{ZP+} \\ V_{ZP-} \\ V_{ZN+} \\ V_{ZN-} \\ V_{O\pm} \end{bmatrix} \quad (1)$$

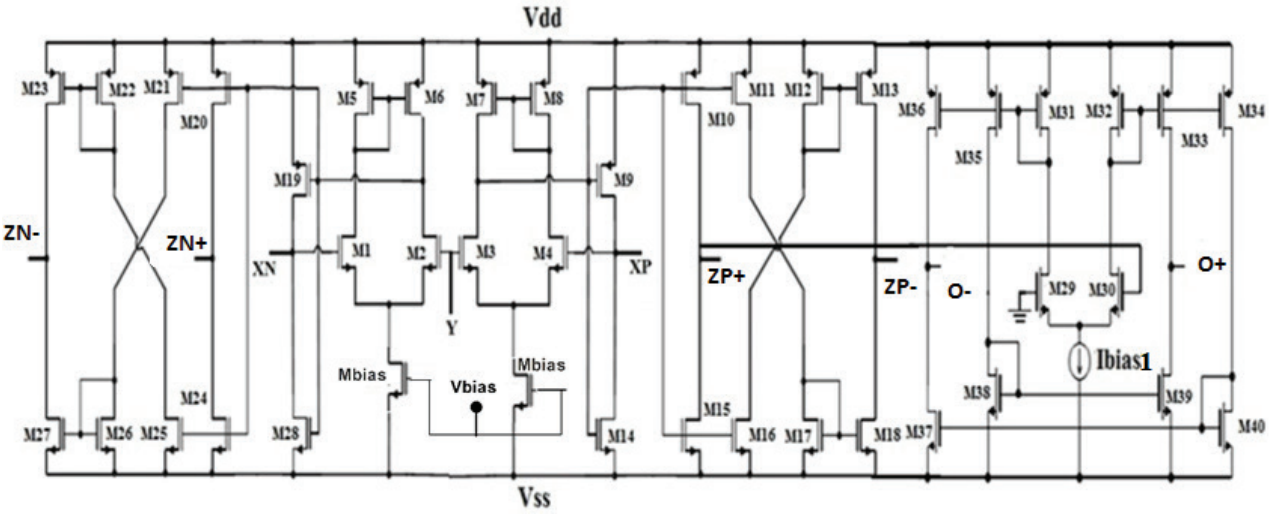


**Figure 2:** CMOS implementation of the EXCCTA

The number of current output terminals ($I_{ZP+}$, $I_{ZP-}$, $I_{ZN+}$, $I_{ZN-}$, $I_{0+}$, $I_{0-}$) can be increased by simply adding two MOS transistors.

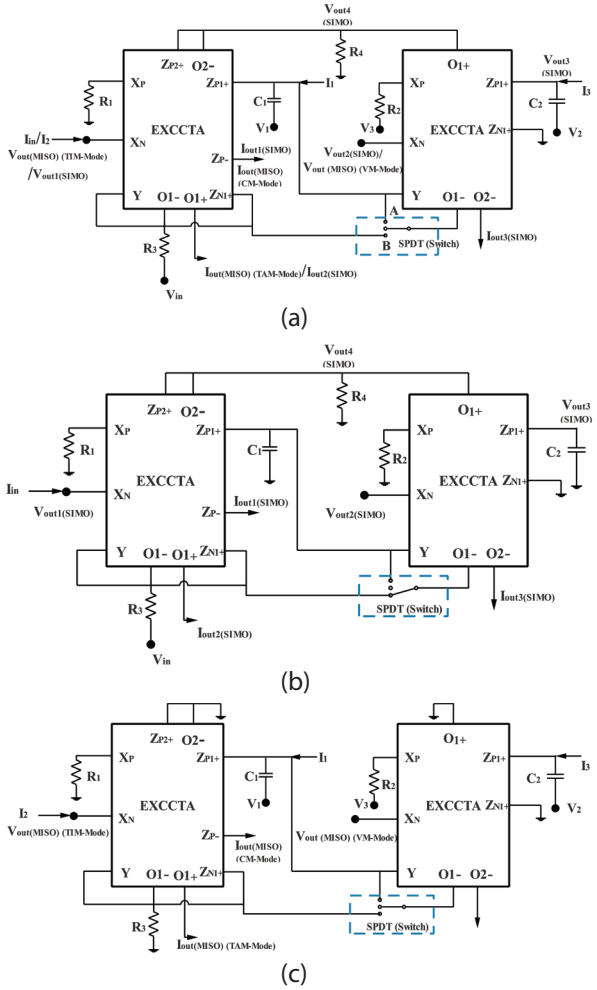


**Figure 3:** Proposed mix-mode filter: (a) generalized diagram, (b) SIMO configuration, (c) MISO configuration

## 3 Proposed electronically tunable mixed-mode universal filter

The proposed mixed-mode universal filter is presented in Figure 3. The filter employs four resistors, two capacitors, and two EXCCTAs. The filter can work in both SIMO and MISO configurations by adding a single pole double throw (SPDT) switch. The operation and features of the filter in each configuration are discussed below.

### 3.1 SIMO configuration

In SIMO configuration, the currents $I_1$ to $I_3$ and input voltages $V_1$ to $V_3$ are set to zero. This grounds all the passive components except $R_3$ as can be inferred from Figure 3(b). In addition, in SIMO configuration no switch is needed for generating filter responses in all four modes. In SIMO configuration the filter has following attributes: (i) inbuilt tunability, (ii) use of grounded capacitors and no capacitive matching requirement, (iii) high input impedance in CM and TIM, (iv) CM and TAM output available form explicit high impedance nodes, (v) tunability of $Q$ independent of $\omega_0$, (vi) AP gain tunability in VM and TIM, and (vii) availability of all filter function in all four mode.

#### 3.1.1 SIMO voltage-mode and transadmittance-mode operation

To obtain VM and TAM responses, the input current $I_{in}$ is set to zero and the input voltage $V_{in}$ is applied as shown in Figure 3(b). The routine analysis of the circuit leads to the transfer functions as given in Equations (2-6). The VM responses are obtained from terminals $V_{out1(SIMO)}$ to $V_{out4(SIMO)}$ as follows:

$$T_{VM_{LP}}(s) = \frac{V_{out3(SIMO)}(s)}{V_{in}(s)} = \frac{1}{s^2 C_1 C_2 R_1 R_2 + s C_2 g_{m1} R_2 R_3 + g_{m2} R_3} \quad (2)$$

$$T_{VM_{HP}}(s)=\frac{V_{out1(SIMO)}(s)}{V_{in}(s)}=\\ =\frac{s^2C_1C_2R_1R_2}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \tag{3}$$

$$T_{VM_{BP}}(s)=\frac{V_{out2(SIMO)}(s)}{V_{in}(s)}=\\ =\frac{sC_2R_2}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \tag{4}$$

To obtain unity gain AP response a simple resistive matching of $R_1 = R_3$ is required and the response is obtained across resistor $R_4$.

$$T_{VM_{AP}}(s)=\frac{V_{out4(SIMO)}(s)}{V_{in}(s)}=\\ =\frac{R_4\left(s^2C_1C_2R_2-sC_2g_{m1}R_2+g_{m2}\right)}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \tag{5}$$

If the O2- terminal is disconnected from the resistor $R_4$, Equation (5) turns to:

$$T_{VM_{BR}}(s)=\frac{V_{out4(SIMO)}(s)}{V_{in}(s)}=\\ =\frac{s^2C_1C_2R_2R_4+g_{m2}R_4}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \tag{6}$$

and a BR response is obtained.

The TAM responses are obtained from high impedance $I_{out1(SIMO)}$ to $I_{out3(SIMO)}$ terminals. The transfer functions are given in Equations (7-11).

$$T_{TAM_{LP}}(s)=\frac{I_{out3(SIMO)}(s)}{V_{in}(s)}=\\ =-\frac{g_{m2}}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \tag{7}$$

$$T_{TAM_{HP}}(s)=\frac{I_{out1(SIMO)}(s)}{V_{in}(s)}=\\ -\frac{s^2C_1C_2R_2}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \tag{8}$$

$$T_{TAM_{BP}}(s)=\frac{I_{out2(SIMO)}(s)}{V_{in}(s)}=\\ =\frac{sC_2R_2g_{m1}}{s^2C_1C_2R_1R_2+sC_2R_2g_{m1}R_3+g_{m2}R_3} \tag{9}$$

$$T_{TAM_{BR}}(s)=\frac{I_{out1(SIMO)}(s)+I_{out3(SIMO)}(s)}{V_{in}(s)}=\\ -\frac{s^2C_1C_2R_2+g_{m2}}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \tag{10}$$

$$T_{TAM_{AP}}(s)=\frac{I_{out1(SIMO)}(s)+I_{out2(SIMO)}(s)+I_{out3(SIMO)}(s)}{V_{in}(s)}=\\ -\frac{s^2C_1C_2R_2-sC_2R_2g_{m1}+g_{m2}}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3}. \tag{11}$$

In TAM, the BR and AP responses can be obtained by appropriately connecting the HP, LP and BP currents. It must be pointed out that, if the filter is designed to work in SIMO configuration then there is no need for the SPDT switch.

*3.1.2 SIMO current-mode and transimpedance-mode operation*

To obtain CM and TIM response, input voltage $V_{in}$ is set to zero and the input current $I_{in}$ is applied to the filter. In CM operation all passive elements are grounded. The CM responses are available from high impedance terminals $I_{out1(SIMO)}$ to $I_{out3(SIMO)}$ and TIM responses are obtained from terminals $V_{out1(SIMO)}$ to $V_{out4(SIMO)}$. The CM filter transfer functions are given in Equations (12-16). In CM, the BR and AP responses can be obtained by appropriately summing the output currents ($I_{HP}$, $I_{LP}$, $I_{BP}$).

$$T_{CM_{HP}}(s)=\frac{I_{out1(SIMO)}(s)}{I_{in}(s)}=\\ =\frac{s^2C_1C_2R_2R_3}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \tag{12}$$

$$T_{CM_{BP}}(s)=\frac{I_{out2(SIMO)}(s)}{I_{in}(s)}=\\ =\frac{-sC_2g_{m1}R_2R_3}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \tag{13}$$

$$T_{CM_{LP}}(s)=\frac{I_{out3(SIMO)}(s)}{I_{in}(s)}=\\ =\frac{g_{m2}R_3}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \quad (14)$$

$$T_{CM_{BR}}(s)=\frac{I_{out1(SIMO)}(s)+I_{out3(SIMO)}(s)}{I_{in}(s)}=\\ =\frac{R_3\left(s^2C_1C_2R_2+g_{m2}\right)}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \quad (15)$$

$$T_{CM_{AP}}(s)=\frac{I_{out1(SIMO)}(s)+I_{out2(SIMO)}(s)+I_{out3(SIMO)}(s)}{I_{in}(s)}=\\ =\frac{R_3\left(s^2C_1C_2R_2-sC_2g_{m1}R_2+g_{m2}\right)}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \quad (16)$$

The TIM filter transfer functions are given in Equations (17-21) as follows:

$$T_{TIM_{HP}}(s)=\frac{V_{out1(SIMO)}(s)}{I_{in}(s)}=\\ -\frac{s^2C_1C_2R_1R_2R_3}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \quad (17)$$

$$T_{TIM_{BP}}(s)=\frac{V_{out2(SIMO)}(s)}{I_{in}(s)}=\\ -\frac{sC_2R_2R_3}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \quad (18)$$

$$T_{TIM_{LP}}(s)=\frac{V_{out3(SIMO)}(s)}{I_{in}(s)}=\\ -\frac{R_3}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \quad (19)$$

Note that to obtain unity gain AP response a simple resistive matching of $R_1 = R_3$ is required and the response is obtained across resistor $R_4$:

$$T_{TIM_{AP}}(s)=\frac{V_{out4(SIMO)}(s)}{I_{in}(s)}=\\ -\frac{R_3R_4\left(s^2C_1C_2R_2-sC_2R_2g_{m1}+1\right)}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \quad (20)$$

while BR response is obtained, if the O2- terminal is disconnected from resistor $R_4$:

$$T_{TIM_{BR}}(s)=\frac{V_{out4(SIMO)}(s)}{I_{in}(s)}=\\ -\frac{R_3R_4\left(g_{m2}+s^2C_1C_2R_2\right)}{s^2C_1C_2R_1R_2+sC_2g_{m1}R_2R_3+g_{m2}R_3} \quad (21)$$

Subsequently, the expression for natural frequency and *Q* of the SIMO mixed-mode filter are:

$$f_0=\frac{1}{2\pi}\sqrt{\frac{g_{m2}R_3}{C_1C_2R_1R_2}} \quad (22)$$

$$Q=\frac{1}{g_{m1}}\sqrt{\frac{C_1g_{m2}R_1}{C_2R_2R_3}} \quad (23)$$

### *3.2 MISO configuration*

In MISO configuration, the input current $I_{in}$ and input voltage $V_{in}$ are set to zero. The input currents $I_1$ to $I_3$ and input voltages $V_1$ to $V_3$ are applied to obtain the required filter responses. In this configuration only three resistors are employed, resistor $R_4$ is not required and can be eliminated as shown in Figure 3(c). The attractive features of the filter include: (i) low output impedance for VM and TIM, (ii) high output impedance explicit current output for CM and TAM, (iii) no requirement for double/negative input signals (voltage/current), (iv) tunability, (v) simultaneous availability of VM and TIM/CM and TAM responses from same input sequence, and (vi) filter is cascadable in all four modes. The operation of the filter is described below.

#### *3.2.1 MISO voltage-mode and transadmittance-mode operation*

To obtain VM and TAM responses, the input voltage $V_1$ to $V_3$ are applied according to the Table 2 and the SPDT switch is connected to point B.

**Table 2:** Input voltage excitation sequence

| Response | Inputs | | | Passive Matching Condition | Active Matching |
|---|---|---|---|---|---|
| | $V_1$ | $V_2$ | $V_3$ | | |
| LP | 0 | 0 | 1 | No | No |
| HP | 1 | 0 | 0 | No | No |
| BP | 0 | 1 | 0 | No | No |
| BR | 1 | 0 | 1 | No | No |
| AP | 1 | 1 | 1 | No | $g_{m1}=g_{m2}$ |

The output responses are obtained from low impedance terminal $V_{out(MISO)(VM\text{-}Mode)}$ and high impedance terminal $I_{out(MISO)(TAM\text{-}Mode)}$. The transfer functions for VM and TAM modes are given as:

$$V_{out\,(MISO)(VM-Mode)} = \\ = \frac{s^2C_1C_2R_1R_2V_1 - sC_2g_{m2}R_2R_3V_2 + g_{m2}R_3V_3}{s^2C_1C_2R_1R_2 + sC_2g_{m1}R_2R_3 + g_{m2}R_3} \quad (24)$$

$$I_{out\,(MISO)(TAM-Mode)} = \\ = g_{m1}\left[\frac{s^2C_1C_2R_1R_2V_1 - sC_2g_{m2}R_2R_3V_2 + g_{m2}R_3V_3}{s^2C_1C_2R_1R_2 + sC_2g_{m1}R_2R_3 + g_{m2}R_3}\right] \quad (25)$$

while $f_0$ and $Q$ correspond to Equations (22) and (23), respectively.

*3.2.2 MISO current-mode and transimpedance-mode operation*

To obtain CM and TIM responses, the input voltages $V_1$ to $V_3$ are set to zero, the SPDT switch is connected to point A, and input current signals $I_1$ to $I_3$ are applied according to Table 3.

**Table 3:** Input current excitation sequence

| Response | Inputs | | | Passive Matching Condition | Active Matching |
|---|---|---|---|---|---|
| | $I_1$ | $I_2$ | $I_3$ | | |
| LP | 0 | 0 | 1 | No | No |
| HP | 0 | 1 | 1 | No | $g_{m1}R_2 = 1$ |
| BP | 1 | 0 | 0 | No | No |
| BR | 0 | 1 | 0 | No | No |
| AP | 1 | 1 | 0 | $R_3 = R_1$ | No |

The CM responses are obtained from high impedance terminal $I_{out(MISO)(CM\text{-}Mode)}$ and TIM responses from low impedance terminal $V_{out(MISO)(TIM\text{-}Mode)}$. The transfer functions and expression for quality factor and pole frequency are given as:

$$I_{out\,(MISO)(CM-Mode)} = \\ = \left[\frac{sC_2R_2g_{m1}R_3I_1 - (s^2C_1C_2R_2R_3 + g_{m2}R_3)I_2 + g_{m1}g_{m2}R_2R_3I_3}{s^2C_1C_2R_1R_2 + sC_2g_{m1}R_2R_3 + g_{m2}R_1}\right] \quad (28)$$

$$V_{out\,(MISO)(TIM-Mode)} = \\ = R_1R_3\left[\frac{sC_2g_{m1}R_2I_1 - (s^2C_1C_2R_2 + g_{m2})I_2 + g_{m1}g_{m2}R_2I_3}{s^2C_1C_2R_1R_2 + sC_2g_{m1}R_2R_3 + g_{m2}R_1}\right] \quad (29)$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m2}}{C_1C_2R_2}} \quad (30)$$

$$Q = \frac{R_1}{g_{m1}R_3}\sqrt{\frac{C_1g_{m2}}{C_2R_2}} \quad (31)$$

Note that except for AP there is no requirement for matching passive components. In case of HP response, the value of transconductance $g_{m1}$ should be adjusted to achieve $g_{m1}R_2 = 1$, which can be easily accomplished by adjusting the bias current $I_{bias}$ of the first EXCCTA.

As a brief conclusion it must be emphasised that the proposed filter can realize SIMO (all modes) and MISO (VM and TAM) responses without requiring any switch. The switch is only required to obtain MISO (CM and TIM) responses.

## 4 Non-Ideal and sensitivity analysis

The non-ideal model of the EXCCTA is presented in Figure 4. As can be deduced, the various parasitic resistances and capacitances appear in parallel with the input and output nodes of the device. The low impedance X node has a parasitic resistance and inductance in series with it. The other non-ideal effects that influences the response of the EXCCTA are the frequency dependent non-ideal current ($\alpha_P$, $\alpha_N$), voltage ($\beta_P$, $\beta_N$), and OTA transconductance transfer (γ, γ′) gains. These gains cause a change in the current and voltage signals during transfer leading to undesired response.

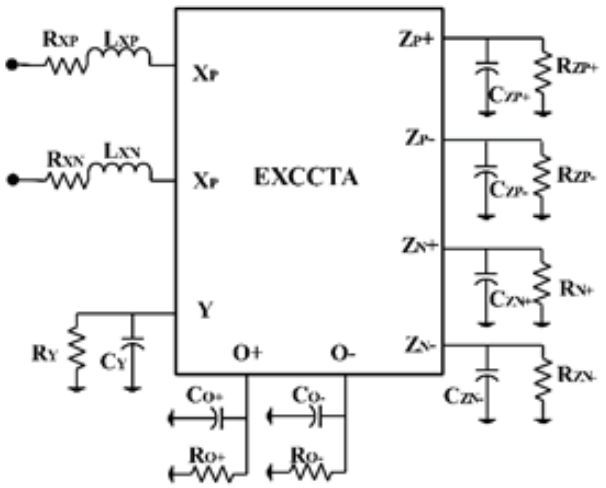


**Figure 4:** Non-ideal model of EXCCTA with parasitics

Taking into account the non-ideal gains the V-I characteristics of the EXCCTA in (1) will be modified as follows: $I_Y = 0$, $V_{XP} = \beta_P V_Y$, $V_{XN} = \beta_N V_Y$, $I_{ZP+} = \alpha_P I_{XP}$,

$I_{ZP-} = \alpha_P^{'} I_{XP}$, $I_{ZN+} = \alpha_N I_{XN}$, $I_{ZN-} = \alpha_N^{'} I_{XN}$, $I_{O+} = \gamma g_m V_{ZP+}$, $I_{O-} = -\gamma^{'} g_m V_{ZP+}$, where $\beta_{Pm} = 1 - \varepsilon_{vPm}$, $\beta_{Nm} = 1 - \varepsilon_{vNm}$, $\alpha_{Pm} = 1 - \varepsilon_{iPm}$, $\alpha_{Pm}^{'} = 1 - \varepsilon_{iPm}^{'}$, $\alpha_{Nm} = 1 - \varepsilon_{iNm}$, $\alpha_{Nm}^{'} = 1 - \varepsilon_{iNm}^{'}$, $\gamma_m = 1 - \varepsilon_{g_m m}$, and $\gamma_m^{'} = 1 - \varepsilon_{g_m m}^{'}$ for m = 1, 2, which refers to the number of EXCCTAs. Here, $\varepsilon_{vPm}$ and $\varepsilon_{vNm}$ $\left(|\varepsilon_{vPm}|, |\varepsilon_{vNm}| \ll 1\right)$ denote voltage tracking errors, $\varepsilon_{iPm}$, $\varepsilon_{iPm}^{'}$, $\varepsilon_{iNm}$, $\varepsilon_{iNm}^{'}$ $(|\varepsilon_{iPm}|, |\varepsilon_{iPm}^{'}|, |\varepsilon_{iNm}|, |\varepsilon_{iNm}^{'}| \ll 1)$ denote current tracking errors, and $\varepsilon_{g_m m}$, $\varepsilon_{g_m m}^{'}$ $\left(|\varepsilon_{g_m m}|, |\varepsilon_{g_m m}^{'}| \ll 1\right)$ denote transconductance errors of the EXCCTA.

The non-ideal analysis considering the effect of non-ideal current, voltage, and transconductance transfer gains is carried out for SIMO (VM and CM) and MISO (VM and CM) configurations to see its effect on the transfer function, $f_0$, and $Q$ of the proposed filters. The modified expressions of filter transfer functions, $f_0$, and $Q$ for the SIMO, and MISO configurations are presented in Equations (32-44).

$$T_{VM_{LP}}^{'}(s) = \frac{\alpha_{P1}\beta_{P1}\alpha_{P2}\beta_{P2}}{s^2 C_1 C_2 R_1 R_2 + sC_2 g_{m1} R_2 R_3 \gamma_1^{'} \alpha_{P1}\beta_{P1} + g_{m2} R_3 \gamma_2^{'} \alpha_{P1}\beta_{P1}\alpha_{P2}\beta_{P2}} \quad (32)$$

$$T_{VM_{HP}}^{'}(s) = \frac{s^2 C_1 C_2 R_1 R_2}{s^2 C_1 C_2 R_1 R_2 + sC_2 g_{m1} R_2 R_3 \gamma_1^{'} \alpha_{P1}\beta_{P1} + g_{m2} R_3 \gamma_2^{'} \alpha_{P1}\beta_{P1}\alpha_{P2}\beta_{P2}} \quad (33)$$

$$T_{VM_{BP}}^{'}(s) = \frac{sC_2 R_2 \alpha_{P1}\beta_{P1}}{s^2 C_1 C_2 R_1 R_2 + sC_2 g_{m1} R_2 R_3 \gamma_1^{'} \alpha_{P1}\beta_{P1} + g_{m2} R_3 \gamma_2^{'} \alpha_{P1}\beta_{P1}\alpha_{P2}\beta_{P2}} \quad (34)$$

$$T_{VM_{AP}}^{'}(s) = \frac{R_4 (s^2 C_1 C_2^{'} R_2 \alpha_{P1}\beta_{P1} - sC_2 R_2 \gamma_1^{'} g_{m1} \alpha_{P1}\beta_{P1} + \gamma_2^{'} g_{m2} \alpha_{P1}\beta_{P1}\alpha_{P2}\beta_{P2})}{s^2 C_1 C_2 R_1 R_2 + sC_2 g_{m1} R_2 R_3 \gamma_1^{'} \alpha_{P1}\beta_{P1} + g_{m2} R_3 \gamma_2^{'} \alpha_{P1}\beta_{P1}\alpha_{P2}\beta_{P2}} \quad (35)$$

$$T_{CM_{LP}}^{'}(s) = \frac{g_{m2} R_3 \alpha_{N1} \gamma_2^{'} \alpha_{P1}\beta_{P1}\alpha_{P2}\beta_{P2}}{s^2 C_1 C_2 R_1 R_2 + sC_2 g_{m1} R_2 R_3 \gamma_1^{'} \alpha_{P1}\beta_{P1} + g_{m2} R_3 \gamma_2^{'} \alpha_{P1}\beta_{P1}\alpha_{P2}\beta_{P2}} \quad (36)$$

$$T_{CM_{HP}}^{'}(s) = \frac{s^2 C_1 C_2 R_3 R_2 \beta_{P1} \alpha_{N1}}{s^2 C_1 C_2 R_1 R_2 + sC_2 g_{m1} R_2 R_3 \gamma_1^{'} \alpha_{P1}\beta_{P1} + g_{m2} R_3 \gamma_2^{'} \alpha_{P1}\beta_{P1}\alpha_{P2}\beta_{P2}} \quad (37)$$

$$T_{CM_{BP}}^{'}(s) = \frac{-sC_2 R_2 R_3 \alpha_{P1}\beta_{P1}\alpha_{N1}\gamma_1^{'} g_{m1}}{s^2 C_1 C_2 R_1 R_2 + sC_2 g_{m1} R_2 R_3 \gamma_1^{'} \alpha_{P1}\beta_{P1} + g_{m2} R_3 \gamma_2^{'} \alpha_{P1}\beta_{P1}\alpha_{P2}\beta_{P2}} \quad (38)$$

$$f_{0\left[SIMO\ \&\ MISO\,(VM\ \&TAM)\right]}^{'} = \frac{1}{2\pi}\sqrt{\frac{\gamma_2^{'}\alpha_{P1}\beta_{P1}\beta_{P2} g_{m2} R_3}{C_1 C_2 R_1 R_2 \alpha_{P2}}} \quad (39)$$

$$Q_{\left[SIMO\ \&\ MISO\,(VM\ \&TAM)\right]}^{'} = \frac{1}{\gamma_1^{'} g_{m1}}\sqrt{\frac{\gamma_2^{'}\beta_{P2} C_1 g_{m2} R_1}{C_2 R_2 \alpha_{P1}\alpha_{P2}\beta_{P1}}} \quad (40)$$

$$f_{0\left[MISO\,(CM\&TIM)\right]}^{'} = \frac{1}{2\pi}\sqrt{\frac{\gamma_2^{'}\alpha_{P2}\beta_{P2} g_{m2}}{C_1 C_2 R_2}} \quad (43)$$

$$Q_{\left[MISO\,(CM\&TIM)\right]}^{'} = \frac{R_1}{\alpha_{P1}\beta_{P1}\gamma_1^{'} g_{m1} R_3}\sqrt{\frac{\gamma_2^{'}\alpha_{P2}\beta_{P2} C_1 g_{m2}}{C_2 R_2}} \quad (44)$$

As a result of component tolerance and non-idealities in EXCCTA the response of the practical filter deviates from the ideal one. To get a measure of the deviation, the relative sensitivity is applied. Mathematically, relative sensitivity is defined as $S_x^y = \lim_{\Delta X \to \infty}\left\{\frac{\Delta y / y}{\Delta x / x}\right\} = \frac{x}{y}\frac{\partial y}{\partial x}$, where x is the component that is varied and y is the $\omega_0$ and $Q$ in our case.

The sensitivities of $\omega_0$ and $Q$ with respect to the non-ideal gains and passive components are given below.

$$V_{out\,(MISO)(VM-Mode)}^{'} = \frac{s^2 C_1 C_2 R_1 R_2 \alpha_{P2} V_1 - sC_2 g_{m2} R_2 R_3 \gamma_2^{'} \alpha_{P1}\beta_{P1} V_2 + g_{m2} R_3 \gamma_2^{'} \alpha_{P1}\beta_{P1} V_3}{s^2 C_1 C_2 R_1 R_2 \alpha_{P2} + sC_2 g_{m1} R_2 R_3 \gamma_1^{'} \alpha_{P2}\alpha_{P1}\beta_{P1} + \gamma_2^{'}\beta_{P1}\beta_{P2}\alpha_{P1} g_{m2} R_3} \quad (41)$$

$$I_{out\,(MISO)(CM-Mode)}^{'} = \left[\frac{sC_2 g_{m1} R_2 R_3 \gamma_1^{'} \alpha_{P1}\beta_{P1} I_1 - (s^2 C_1 C_2 R_3 R_2 \alpha_{P1}\beta_{P1} + g_{m2}\gamma_2^{'} R_3 \alpha_{P1}\beta_{P1}) I_2 + \alpha_{P1}\beta_{P1}\gamma_1^{'}\gamma_2^{'} g_{m1} g_{m2} R_2 R_3 I_3}{s^2 C_1 C_2 R_1 R_2 + sC_2 g_{m1} R_2 R_3 \alpha_{P1}\beta_{P1}\gamma_1^{'} + g_{m2} R_1 \alpha_{P2}\beta_{P2}\gamma_2^{'}}\right] \quad (42)$$

The sensitivities obtained from Equations (39, 40) for the SIMO and MISO (VM and TAM) configurations are given in (45-47). The sensitivity analysis results for MISO (CM and TIM) for (43, 44) are given in Equations (48-50).

$$-S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = -S_{R_1}^{\omega_0} = -S_{R_2}^{\omega_0} = -S_{\alpha_{P2}}^{\omega_0} = S_{\gamma_2'}^{\omega_0} = \\ = S_{\alpha_{P1}}^{\omega_0} = S_{\beta_{P1}}^{\omega_0} = S_{\beta_{P2}}^{\omega_0} = S_{g_{m2}}^{\omega_0} = S_{R_3}^{\omega_0} = \frac{1}{2} \quad (45)$$

$$S_{C_1}^{Q} = -S_{C_2}^{Q} = S_{R_1}^{Q} = -S_{R_2}^{Q} = S_{g_{m2}}^{Q} = -S_{\alpha_{P1}}^{Q} = \\ = -S_{\alpha_{P2}}^{Q} = -S_{\beta_{P1}}^{Q} = S_{\beta_{P2}}^{Q} = S_{\gamma_2'}^{Q} = \frac{1}{2} \quad (46)$$

$$S_{\gamma_1'}^{Q} = S_{g_{m1}}^{Q} = -1 \quad (47)$$

$$-S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = -S_{R_2}^{\omega_0} = S_{\gamma_2'}^{\omega_0} = S_{g_{m2}}^{\omega_0} = S_{\alpha_{P2}}^{\omega_0} = S_{\beta_{P2}}^{\omega_0} = \frac{1}{2} \quad (48)$$

$$S_{C_1}^{Q} = -S_{R_2}^{\omega} = -S_{C_2}^{Q} = S_{\alpha_{P2}}^{Q} = S_{g_{m2}}^{Q} = S_{\beta_{P2}}^{Q} = S_{\gamma_2'}^{Q} = \frac{1}{2} \quad (49)$$

$$S_{R_1}^{Q} = -S_{\alpha_{P1}}^{Q} = -S_{\beta_{P1}}^{Q} = -S_{g_{m1}}^{Q} = -S_{R_3}^{Q} = -S_{\gamma_1'}^{Q} = 1 \quad (50)$$

The sensitivities are low and have absolute values not higher than unity.

## 5 Simulation results

To validate the proposed mixed-mode filter, the EXCCTA is designed in Cadence Virtuoso software using 0.18µm PDK provided by Silterra Malaysia. The widths and lengths of the MOS transistors are given in Table 4. The supply voltage is set to ±1.25 V and the bias current of th OTAs is set to120µA resulting in transconductance of $g_{m1} = g_{m2} = 1.0321$ mS. The complete layout of the EXCCTA is designed as presented in Figure 5. The layout verification and parasitic extraction are done using Mentor Graphics Calibre verification tool. The high performance nhp and php MOSFETs from the PDK library are employed in the design. The EXCCTA occupied a total chip area of (52.78×22.085)µm².

Table 4: Width and length of the MOS transistors

| Transistor | Width (µm) | Length (µm) |
|---|---|---|
| M1-M4 | 3.06 | 0.36 |
| M5-M8 | 4 | 0.36 |
| M9-M11, M19-M21 | 2.16 | 0.36 |
| M12, M13, M22, M23 | 1.08 | 0.72 |
| M14-M18, M24-M28 | 0.72 | 0.72 |
| M29-M32 | 1.8 | 0.36 |
| M33-M36 | 5.4 | 0.36 |
| M37-M40 | 1.8 | 0.72 |

### *5.1 SIMO configuration operation*

First of all, the SIMO configuration of the proposed filter is validated. The filter is designed for centre frequency of 7.622 MHz by setting passive components and OTA bias current values as follows: $R_1 = 1$ kΩ, $R_2 = 2$ kΩ, $R_3 = 1$ kΩ, $R_4 = 1$ kΩ, $C_1 = 15$ pF, $C_2 = 15$ pF, and $g_{m1} = g_{m2} = 1.0321$ mS. For the sake of comparison, the EXCCTA based filter responses are plotted along with the ideal filter results obtained using the Matlab software. The VM responses are shown in Figure 6. The AP response is obtained across resistance $R_4$. In addition, the gain of the AP response can be tuned through $R_4$ without affecting other filter parameters as is evident from Figure 7.

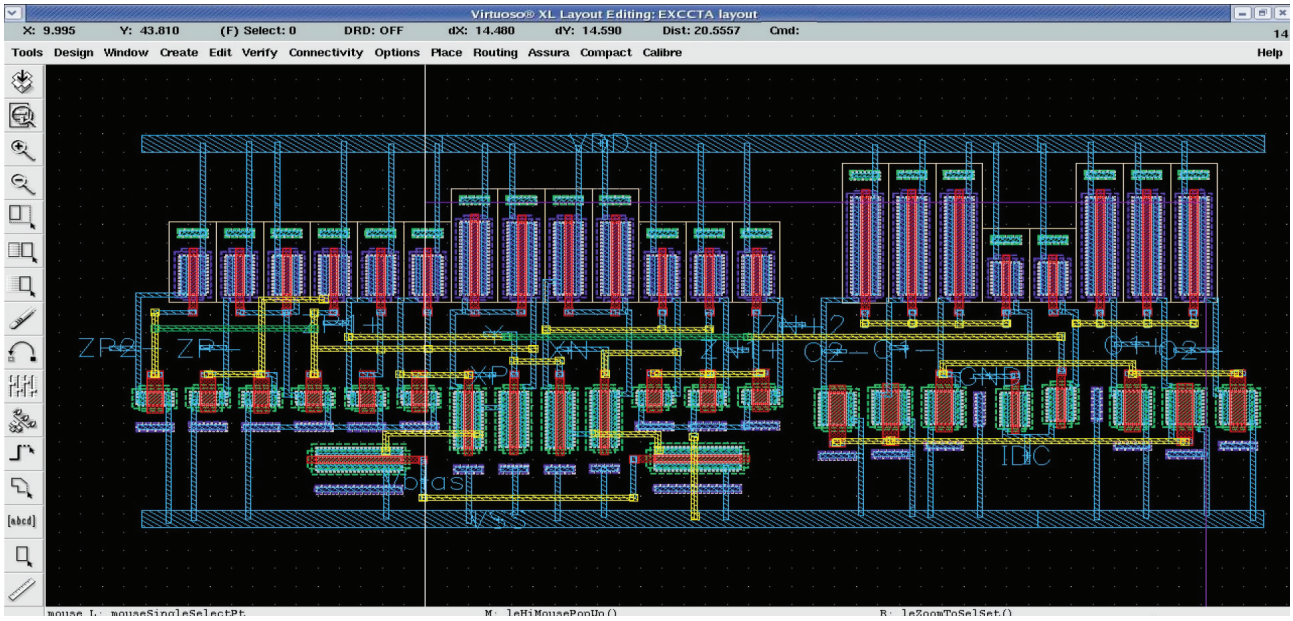


**Figure 5:** Layout of the EXCCTA used in proposed filter design

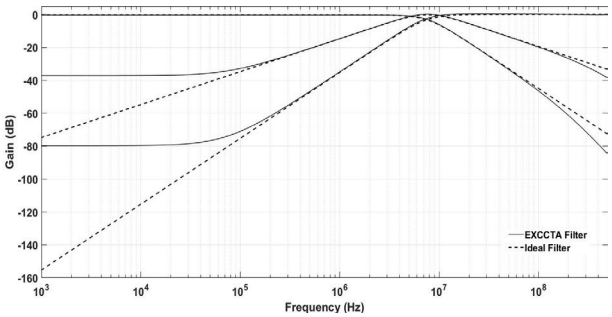


**Figure 6:** VM SIMO configuration: Frequency responses of the LP, BP, and HP filter

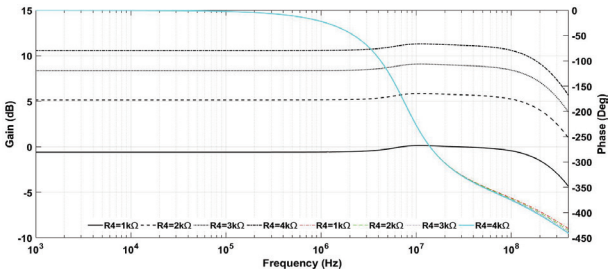


**Figure 7:** VM SIMO configuration: Gain and phase responses of the AP filter

To analyse the quality factor tuning, the BP response is plotted for different values of $I_{Bias1}$ current of $OTA_1$. It can be deduced from Figure 8 that the quality factor can be tuned independent of the centre frequency. The signal processing capability of the VM filter is verified by examining the transient response of the filter. A sinusoidal voltage input signal at 7.622 MHz is applied and the observed LP, BP, HP responses are plotted as given in Figure 9. The total harmonic distortion (THD) of the filter for LP, BP, HP and AP responses is plotted for different input signal amplitudes. The THD remains within acceptable limits for large input range as presented in Figure 10.

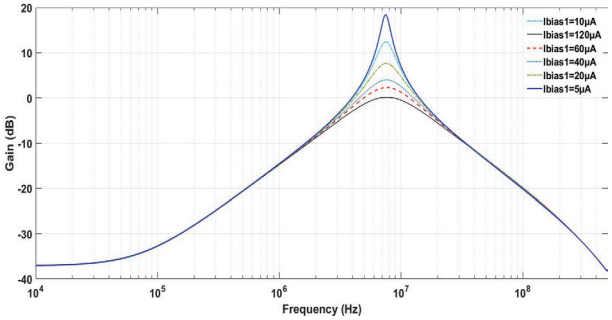


**Figure 8:** VM SIMO configuration: Quality factor tuning for different bias currents in BP filter

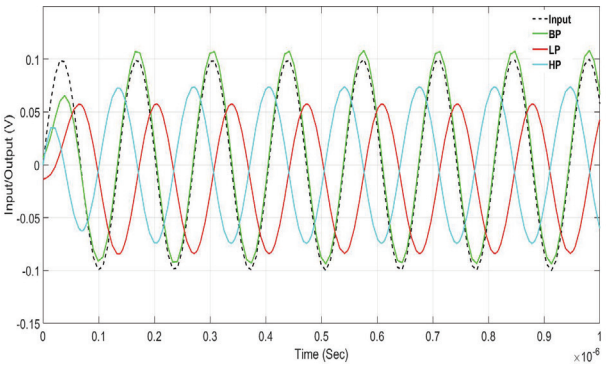


**Figure 9:** VM SIMO configuration: Transient analysis of the filter

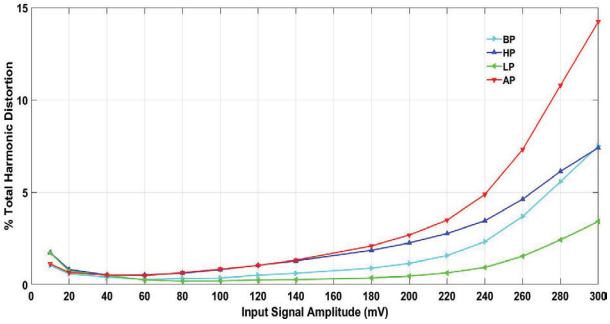


**Figure 10:** VM SIMO configuration: The THD analysis results of the filter

To study the effect of process variation on the proposed filter Monte Carlo analysis is carried out for 10% variation in both capacitor $C_1$ and $C_2$ values for BP response. The analysis is done for 200 runs and the results are presented in Figure 11.

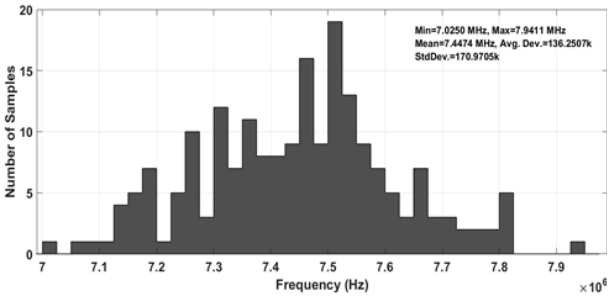


**Figure 11:** VM SIMO configuration: The Monte Carlo analysis results

The results for CM SIMO filter are presented in Figures 12 and 13. The BR and AP responses are obtained by summing $I_{HP}$, $I_{LP}$, and $I_{BP}$ currents appropriately as discussed in section 3. The quality factor variation with OTA1 bias current $I_{Bias1}$ is depicted in Figure 14.

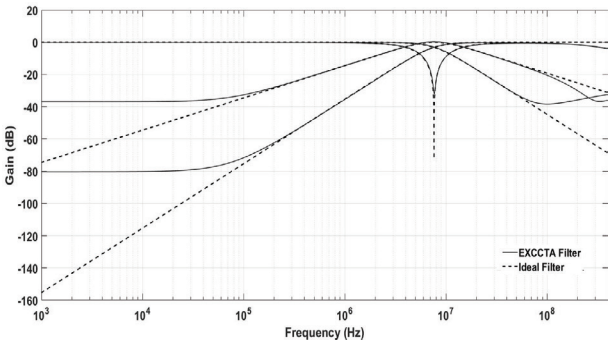


**Figure 12:** CM SIMO configuration: Frequency responses of the LP, BP, HP, and BR filter

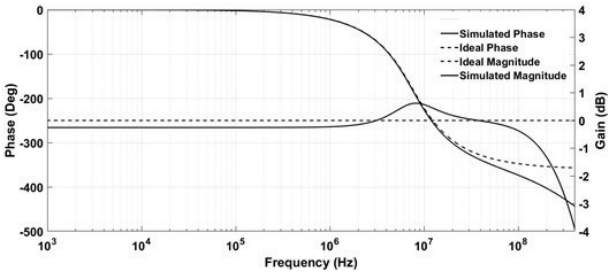


**Figure 13:** CM SIMO configuration: Gain and phase responses of the AP filter

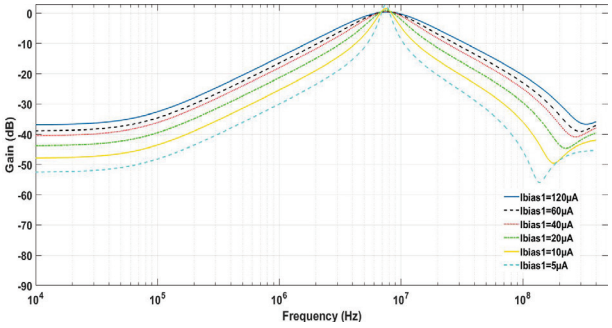


**Figure 14:** CM SIMO configuration: Quality factor tuning for different bias currents in BP filter

The Monte Carlo analysis is carried out for 10% variation in both capacitor $C_1$ and $C_2$ values for LP response in CM operation. The analysis is done for 200 runs and the results are given in Figures 15. To further see the effect of process variability another Monte Carlo analysis is done using the Monte Carlo parameters given in the product design kit (PDK) for the MOS transistors. The results are presented in Figure 16. As can be deduced the mean value of frequency showed a deviation of approximately 6.1% for designed frequency. The THD for LP, HP, and BP responses are presented in Figure 17.

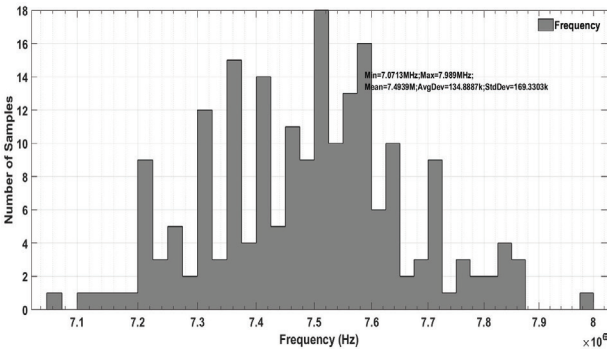


**Figure 15:** CM SIMO configuration: The Monte Carlo analysis results

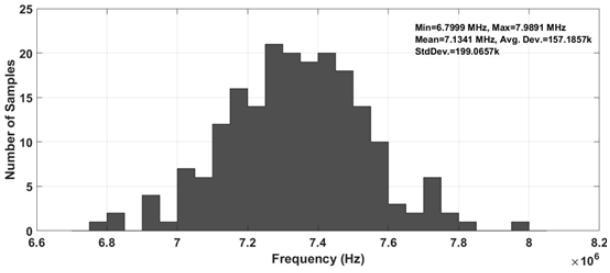


**Figure 16:** CM SIMO configuration: The Monte Carlo analysis results for transistor variability

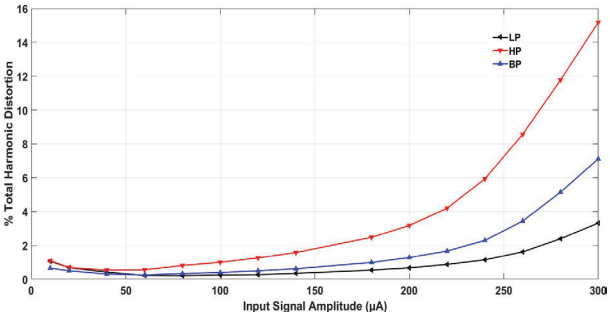


**Figure 17:** CM SIMO configuration: The THD analysis results of the LP, HP, and BP filter

The TAM filter responses are given in Figures 18 and 19, which prove that the filter can generate all five responses in this mode. The BR and AP responses can be obtained by summing the $I_{HP}$, $I_{LP}$, and $I_{BP}$ currents.

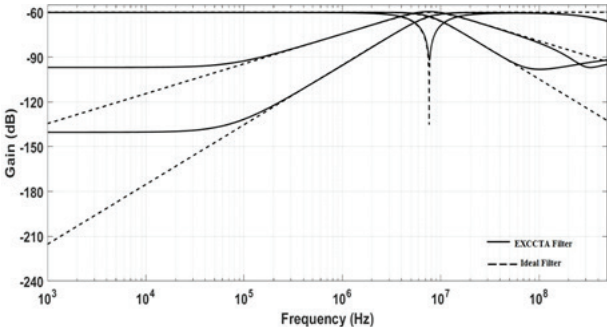


**Figure 18:** TAM SIMO configuration: Frequency responses of the LP, BP, HP, and BR filter

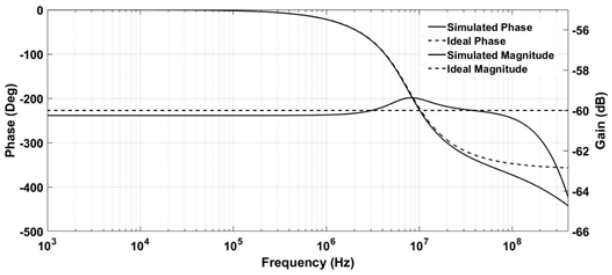


**Figure 19:** TAM SIMO configuration: Gain and phase responses of the AP filter

The LP, BP, and HP responses in TIM configuration are shown in Figure 20. The AP response is given in Figure 21. To verify the frequency tunability the LP response is plotted for different values of resistance $R_2$. Figure 22 shows that the frequency tuning also effects the *Q* of the filter, however, it can be adjusted independent of frequency by varying $I_{Bias1}$ of OTA1.

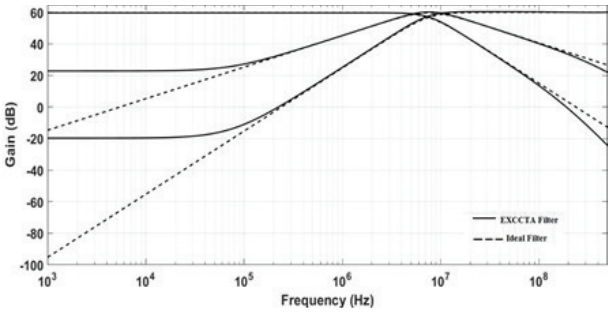


**Figure 20:** TIM SIMO configuration: Frequency responses of the LP, BP, and HP filter

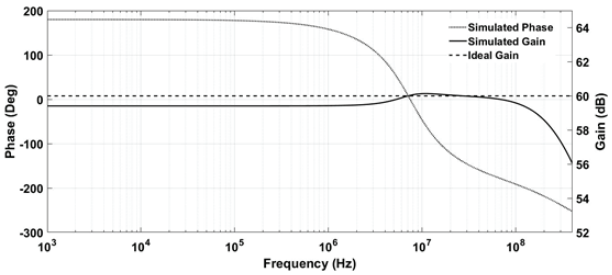


**Figure 21:** TIM SIMO configuration: Gain and phase responses of the AP filter

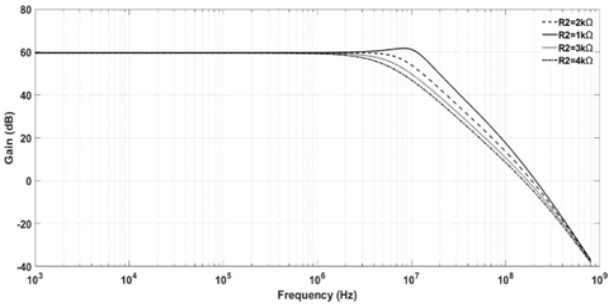


**Figure 22:** TIM SIMO configuration: Frequency tunability for different values of $R_2$ in LP filter

### *5.2 MISO VM and TAM configuration operation*

The filter is designed for $f_0$ = 7.9577 MHz by setting passive component and OTA bias current values as follows: $R_1$ = 1 kΩ, $R_2$ = 1 kΩ, $R_3$ = 969 Ω, $C_1$ = 20 pF, $C_2$ = 20 pF, and $g_{m1} = g_{m2}$ = 1.0321 mS. It must be noted that in MISO configuration resistor $R_4$ is not required and will be removed. The inputs are applied according to conditions outlined in Table 2. The filter provides VM and TAM responses simultaneously from the same input sequence. The VM filter responses are presented Figure 23. The VM AP response is given in Figure 24. The independent tunability of the *Q* is depicted in Figure 25 for different bias currents $I_{Bias1}$ of $OTA_1$. To check the phase and signal processing accuracy of the filter, transient analysis is done at 7.9577 MHz with sinusoidal voltage input of 200mV (p-p) for BP configuration. Figure 26 validates the correct functioning of the filter.

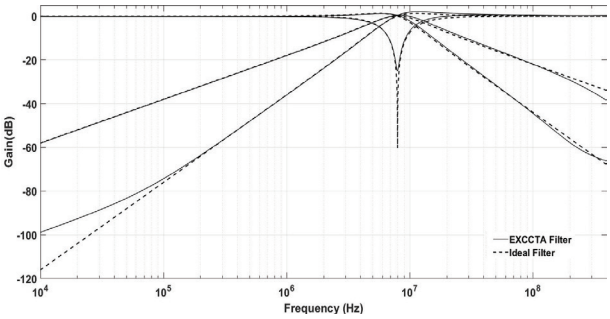


**Figure 23:** VM MISO configuration: Frequency responses of the LP, BP, HP, and BR filter

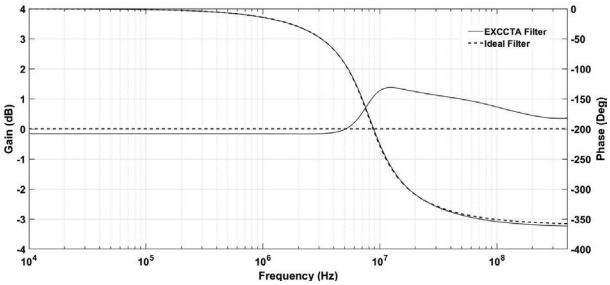


**Figure 24**: VM MISO configuration: Gain and phase responses of the AP filter

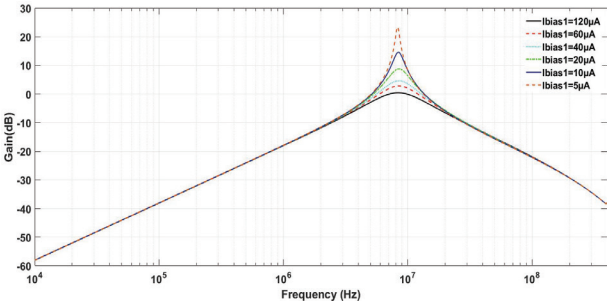


**Figure 25:** VM MISO configuration: Quality factor tuning for different bias currents in BP filter

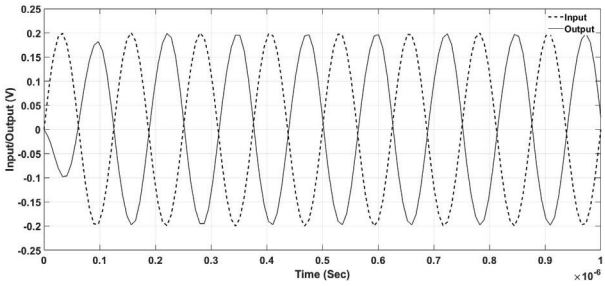


**Figure 26:** VM MISO configuration: Transient analysis of BP filter

The TAM responses of the MISO filter are presented in Figure 27. The AP response is given in Figure 28. The VM outputs are obtained from low impedance node and TAM outputs are obtained from explicit high impedance node which make this filter cascadable.

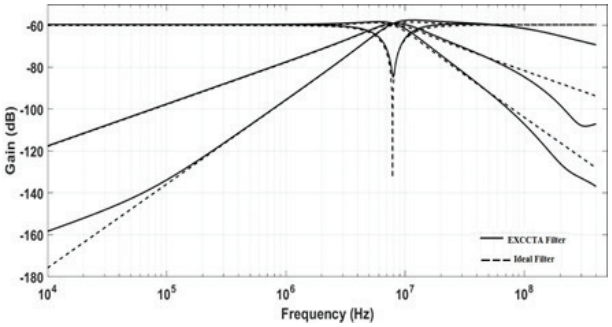


**Figure 27:** TAM MISO configuration: Frequency responses of the LP, BP, HP, and BR filter

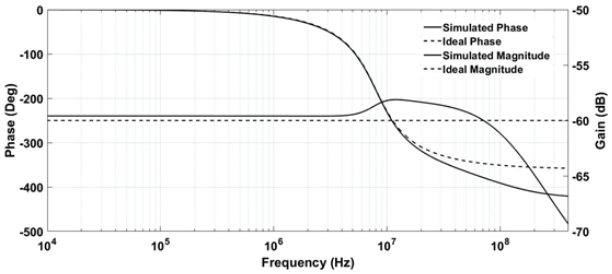


**Figure 28:** TAM MISO configuration: Gain and phase responses of the AP filter

### *5.3 MISO CM and TIM configuration operation*

The CM and TAM filter is designed for $f_0$ = 8.16 MHz by setting passive component and OTA transconductance values as follows: $R_1$ = 1 kΩ, $R_2$ = 1 kΩ, $R_3$ = 969 Ω, $C_1$ = 20 pF, $C_2$ = 20 pF, and $g_{m1} = g_{m2}$ = 1.0321 mS. In MISO filter there is again no need for $R_4$. The inputs currents are applied according to sequence given in Table 3. The filter provides CM and TIM responses simultaneously from the same input sequence. The CM outputs are available from explicit high impedance node and the TIM outputs are available from low impedance node making the filter cascadable. The CM responses are given in Figures 29, 30 and the TIM responses are presented in Figures 31, 32.

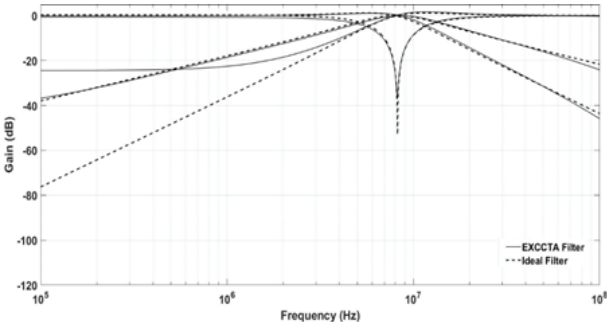


**Figure 29:** CM MISO configuration: Frequency responses of the LP, BP, HP, and BR filter

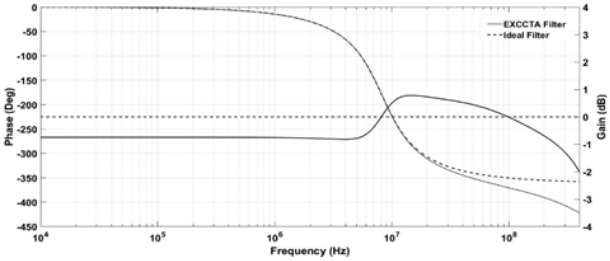


**Figure 30:** CM MISO configuration: Gain and phase responses of the AP filter

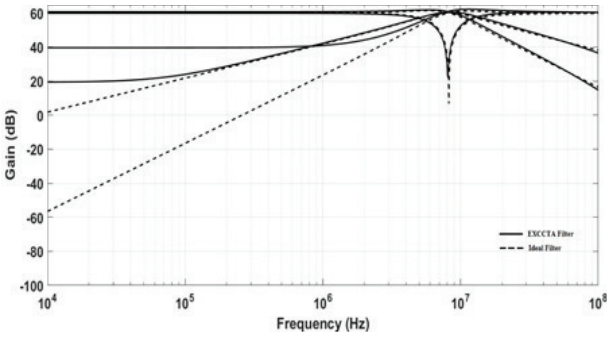


**Figure 31:** TIM MISO configuration: Frequency responses of the LP, BP, HP, and BR filter

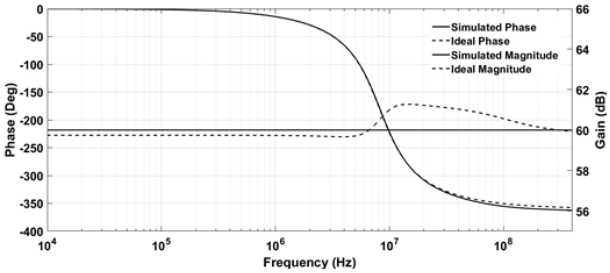


**Figure 32:** TIM MISO configuration: Gain and phase responses of the AP filter

The proposed filter is validated in both MISO and SIMO configurations. The filter responses are found close to the theoretical ones. In CM and TAM operation, the filter response degrades beyond 350 MHz as seen from the graphs. This problem can be mitigated by increasing the output impedance of $Z_P$ and $Z_N$ terminals by employing cascode transistors in the output stage. Moreover, careful layout can further increase the accuracy of the filter.

## 6 Conclusion

In this study, a new EXCCTA based electronically tunable mixed-mode filter structure is proposed. The filter employs two EXCCTAs, four resistors, two capacitors, and a single switch. This is the first presented filter to date that has inbuilt tunability and can realize all five filter responses in all four modes of operation (VM, CM, TAM, and TIM) in both MISO and SIMO configurations. The detailed theoretical analysis, non-ideal gain analysis, and sensitivity study are given. The layout of the EXCCTA is designed in Cadence software and extensive simulations are carried out to examine and validate the proposed filter in all four modes of operation. The proposed filter has the following advantages: (i) ability to operate in both MISO and SIMO configurations in all four modes, (ii) no requirement of capacitive matching, (iii) low input impedance in SIMO (CM and TIM) configuration, (iv) high output impedance explicit current output for SIMO (CM and TAM), (v) tunability of *Q* independent of frequency in MISO and SIMO configurations, (vi) use of grounded capacitors in SIMO configuration, (vii) low output impedance for MISO (VM and TIM), (viii) high output impedance explicit current output for MISO (CM and TAM), (ix) no requirement for double/negative input signals (voltage/current) in MISO configuration, and (x) low active and passive sensitivities. The simulation results are consistent with the theoretical predictions.

## 7 Acknowledgement

This work is funded by Minister of Education Malaysia under grant FRGS/1/2018/TK04/UKM/02/1 and AKU254:HICoE (Fasa II) 'MEMS for Biomedical Devices (artificial kidney).

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Arrived: 15. 05. 2020
Accepted: 14. 10. 2020

Original scientific paper
https://doi.org/10.33180/InfMIDEM2020.305

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 50, No. 3(2020), 205 – 214

# Modeling of Static Negative Bias Temperature Stressing in p-channel VDMOSFETs using Least Square Method

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**Abstract:** Negative bias temperature instability (NBTI) is a phenomenon commonly observed in p-channel metal-oxide semiconductor (MOS) devices simultaneously exposed to elevated temperature and negative gate voltage. This paper studies threshold voltage shift under static stress associated with the NBT stress induced buildup of both interface traps and oxide trapped charge in the commercial p-channel power VDMOSFETs IRF9520, with the goal to design an electrical model. Change of threshold voltage follow power law $t^n$, where parameter $n$ is different depending on the stressing phase and stressing conditions. Two modeling circuits are proposed and modeling circuit elements values are analyzed. Values of modeling circuits elements are calculated using least square method approximation conducted on obtained experimental results. Modeling results of both circuits are compared with the measured results and then further discussed.

**Keywords:** NBTI; VDMOSFET; electrical circuit; modeling; least square method;

# Modeliranje statičnega stresa temperature zaradi negativne napetosti v p-kanalnem VDMOSFETu z metodo najmanjših kvadratov

**Izvleček:** Temperaturna nestabilnost pri negativni napetosti (NBTI) je fenomen p kanalnih metal-oksid polprevodnikov, ki so hkrati izpostavljeni povišani temperaturi in negativni napetosti. V študiji je opazovana sprememba pragovne napetosti komercialnega VDMOSFET tranzistorja IRF9520 pri NBT stresu in pojav naboja v spojnih in oksidnih pasteh z namenom razvoja električnega modela. Sprememba pragovne napetosti sledi zakonu moči $t^n$, kjer je $n$ odvisen of faze in oblike stresa. Predlagana sta dva modela, pri čemer so vrednosti elementov izračunani z metodo najmanjših kvadratov na osnovi izmerjenih vrednosti. Modelni rezultati so primerjani z meritvami.

**Ključne besede:** NBTI; VDMOSFET; električno vezje; modeliranje; metoda najmanjših kvadratov

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## 1 Introduction

As the device dimensions in CMOS technologies have been continuously scaled down, a phenomenon called Negative Bias Temperature Instability (NBTI) has gained in importance as one of the most important degradation mechanisms. Degradation of transistor parameter values due to NBTI has emerged as a major reliability concern in current and future technology generations, especially in p-channel MOSFETs [1-3]. During the stress period, the transistor parameters slowly deviate from the nominal value. Longer the stress period, higher is the impact of NBTI on transistor parameters. NBTI

effects are manifested as the changes in device threshold voltage ($V_T$), transconductance ($g_m$) and drain current ($I_D$), and have been observed mostly in p-channel MOSFETs operated under negative gate oxide fields in the range 2 - 6 MV/cm at temperatures around 100 °C or higher [1-5]. Change in these parameters is dependent on the stress parameters (time, temperature, gate voltage). Considering the effects of NBTI related degradation on device electrical parameters, NBT stress-induced threshold voltage shift ($\Delta V_T$) seems to be the most critical one [6, 7].

Despite notable scale down in the device dimensions, ultra-thick gate oxide reliability studies are still of significance because of broad use of MOS technology. Taking this into consideration, our earlier papers were dealing with NBTI in p-channel power vertical double diffused MOS (VDMOS) transistors [6, 8-13]. Their reliability has been investigated under various stress conditions, such as irradiation, high electric field, NBTI, NBTI under low magnetic field, and NBTI and irradiation [13-16]. NBTI is critical for normal operation of power MOSFETs since they are routinely operated at high current and voltage levels, which lead to both increased gate oxide fields and self-heating, thus favor NBTI.

First thorough explanation of processes on negative bias temperature instabilities was made by Jeppson and Svensson [17]. Even though more than 40 years have passed since then, many mechanisms of NBTI are not very well understood yet. In the last decade, many different working groups are addressing NBTI effects, with accent on both description and modeling of voltage threshold shifts [19, 20]. Swami presented a model for nano MOSFET for FinFET technologies [20], while Aleksandrov reported a model that is based on a reaction-diffusion principle [21]. Still, an appropriate electrical model to describe instabilities corresponding to different stressing conditions is lacking [22]. A model by Danković is RC based model and describes both static and pulsed NBT stressing [23]. However, further mathematical improvements are needed in order to overcome time-bounded flaws of the model, and to make use of the dependencies between temperatures and bias values. Ma presented a model that attempts to explore these dependencies [24], although they aren't analyzed on the accelerated NBT stressing conditions. Maricau used similar approach of RC based model [25], but it analyses short stressing periods, while this paper focuses on modeling of the effects caused by longer stressing periods.

The use of this type modeling is to create a model that can be mathematically calculated in order to incorporate the model into SPICE. That will enable the designers to consider these instabilities of the circuit during the design phase.

The primary part of this study is to propose an equivalent electrical circuit for modeling of $\Delta V_T$ based on experimental data using least square method. In the section 2, experimental setup and results will be briefly described and discussed. Section 3 deals with the modeling approach, and evaluates the model and gives comparison between measured and modeled results.

## 2 Experimental setup

Used devices for this research are commercial p-channel power VDMOSFETs IRF9520 with initial threshold voltage of $V_{T0}$ = -3.6 V [26]. Devices are built in standard silicon-gate technology with 100 nm thick gate oxide and packed in plastic TO-220 packages.

To properly investigate NBTI in p-channel power VD-MOS transistors in which gate oxides thickness are 100 nm, special stress voltages are needed. These voltages need to be several times larger than typical operating voltage of these transistors (more than – 40 V). To ensure these specific signals, it is needed to develop an additional separate circuit that provides appropriate higher stress voltages for stressing. In years during the research, we have developed a system that automates both NBT stress and measurement on p-channel power VDMOS transistors [12].

System consists of high voltage stress circuit and of low voltage measurement circuit that are controlled with software-controlled switches. Stressing circuit includes an external amplifier between the stress voltage source unit and the device under test (DUT). The transfer I–V characteristics were measured at the drain voltage value of 100 mV, so the device was kept in the linear region of operation. Gate voltage was swept from −2 to −4.75 V, with −50 mV step. Designed system allows full range measurement of transfer I-V characteristics, that is used to extract threshold voltage using second derivative method [27]. This measurement method has previously been used by several research groups [9-13, 15, 16].

Several sets of p-channel devices were tested under different conditions. Devices were subjected to stress for 24 hours during which 36 interim measurements were performed. Two different negative voltages were applied to gate (- 45 V and - 50 V) while source and drain terminals were grounded. Experiments were done at two different temperatures (150 °C and 175 °C) and values of threshold voltage shifts are obtained. Our ear-

lier experiments included testing devices under many different conditions in terms of both gate voltage and temperature [9-13]. Experimental results are given in Figure 1. For the comprehensiveness of the proposed model, only four combinations of stress conditions are shown.

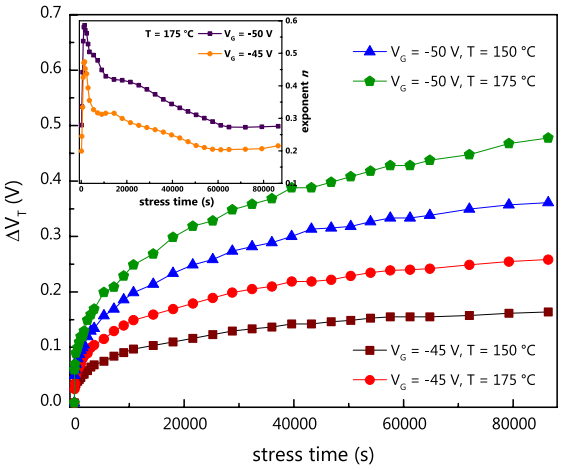



**Figure 1:** Threshold voltage shifts caused by static NBT stress with value of parameter *n* during stressing.

NBT stress under static conditions results in notable threshold voltages shifts. These changes become more pronounced at higher stress voltages and temperatures, which is in line with other investigations [18, 22, 28, 29]. A lot of results, including ours indicate that $\Delta V_T$ saturates with increase in stress time [4, 6, 11].

NBT stress causes threshold voltage shifts with widely different rate in different time periods [28, 29]. Evolution of $\Delta V_T$ through time is presented in Figure 1 Inserted graphic, and given with power law ($t^n$). During this evolution, distinct phases can be distinguished [4, 13, 30]. For every phase, the value of parameter *n* is different. Through each of the phases, parameter *n* is as close as constant (not exactly constant, but in the very limited range). During our earlier researches that involved extensive NBT stress [4, 6, 8, 9-13], in the case of long-term experiments, three different phases are detected in evolution of *n* [6]. Starting phase, where $n = 0.4$. In this phase, *n* is highly dependent on the stressing temperature and bias [4, 6]. Second phase, where *n* drops to $n = 0.25$, and is almost independent on stressing conditions. Third, final phase, where *n* in again dependent on the stressing conditions and steadily declines to $n = 0.14$, continuing to saturation. Similar results are obtained for all stressing temperatures in the experiments. All of the results are suggesting similar development of the parameter *n* [6, 13, 31]. So, it can be concluded that parameter *n* is overall higher at the start phase of the stressing, but tends to saturate in later phases of stressing.

Described progress of the parameter *n* is caused by originated oxide trapped charge and interface traps, which directly influence the changes in the threshold voltage during NBT stress [4]. These occurrences are product of numerous electrochemical processes and reactions concerning oxide and interface defects, holes and other and species related to hydrogen. Depending on the stressing conditions and the number of defects, these reactions can occur in either forward or reverse direction. Since reversed reactions are characteristic for recovery of the degradation that occurs during pulsed stressing, in the case of static stress, forward reactions are dominant [4]. Starting phase of stressing, which explain creation of interface traps is explained with the reaction:

$$Si_3 \equiv Si - H \leftrightarrow Si_3 \equiv Si^{\bullet} + H^{\bullet} \tag{1}$$

The released hydrogen atoms ($H^{\bullet}$) are highly reactive, and they also can dissociate the *SiH* bonds at the interface or in the oxide near the interface. These reactions lead to creation of additional interface traps or positively charged oxide defects.

$$Si_3 \equiv Si - H + H^{\bullet} \leftrightarrow Si_3 \equiv Si^{\bullet} + H_2 \tag{2}$$

$$O_3 \equiv Si - H + H^{\bullet} + h^{+} \leftrightarrow O_3 \equiv Si^{+} + H_2 \tag{3}$$

Released unstable hydrogen atoms react with the holes to form ions.

$$H^{\bullet} + h^{+} \rightarrow H^{+} \tag{4}$$

However, hydrogen ions also dissociate *SiH* bonds in the oxide near the interface leading to creation of positively charged oxide defects.

$$O_3 \equiv Si - H + H^{+} \leftrightarrow O_3 \equiv Si^{+} + H_2 \tag{5}$$

Oxide trapped charge and interface traps buildup described in the given reactions is notably enhanced in the early phase while concentration of *SiH* trap precursors is still high. As the stress time increases, the number of both positively charged defects and interface traps is getting higher. However, probability for reverse reaction (passivation processes) occurring rises as well.

The $H_2$ molecules released in reactions (2), (3) and (5) diffuse deeper into oxide and can be cracked at positively charged oxide traps:

$$O_3 \equiv Si^{+} + H_2 \rightarrow O_3 \equiv Si - H^{+} + H^{\bullet} \tag{6}$$

As a product of reaction (6), $H^{\bullet}$ is released. It can take part in either forward reaction or reverse reaction, thereby rounding the chain of reaction. Increased amount of reverse reaction occurences lead to change in the slope of a function interpreting parameter *n*. Key step for appropriate modeling is to tackle the change of parameter *n* in phases, in order to follow the evolution of $\Delta V_T$.

## 3 Modeling approach

Analytical models for NBT stressing have been researched throughout the years [19-25, 32-37]. This model assumes continuous stress on the PMOS devices. Model is built to follow $\Delta V_T$ during stress time. Since the change of $\Delta V_T$ is given with the power law ($t^n$), a capacitor *C* charged through resistor *R* is chosen for the central element of the modeling circuit. Capacitor charging equation is given with:

$$V_C = V_S\left(1-e^{-\frac{t}{\tau}}\right) \tag{7}$$

Capacitor is chosen because the capacitor voltage is given in exponential form, which is a type of the power law, needed for $\Delta V_T$ modeling. So, the capacitor voltage, $V_C$ models $\Delta V_T$. In given modeling circuit, rise of the capacitor voltage should correspond to the rise of the $\Delta V_T$, so that in any moment $t_1$, $V_C$ should be as much as accurate as $\Delta V_T$. To accomplish that, specific controlled charging rate of the capacitor must be achieved. Value of time constant, $\tau$, must be calculated first, and then values of capacitance of capacitor *C* and resistance of the resistor *R* must be fitted. Value of $V_S$ is acquired using stretch exponential (SE) equations [3, 6] and listed in Table 1. The SE fit predicts that value of $\Delta V_T$ will saturate after extended stressing and it estimates the saturation value. Increased stressing time leads to better estimation of the saturation value, as can be seen for parameter *n*. Stretch exponential equation is given with:

$$\Delta V_T(t) = \Delta V_{Tmax}\,\Delta\left[1-e^{-\left(\frac{t}{\tau_0}\right)^{\beta}}\right] \tag{8}$$

In the equation (8), $\beta$, $\tau_0$ and $\Delta V_{Tmax}$ are fitting parameters. Parameter $\beta$ is defined as a distribution width, and $\tau_o$ represents a characteristic time constant of the distribution. Parameter $\Delta V_{Tmax}$ is a value of $\Delta V_T$ saturation [6, 42]. Value of $V_S$ is actually value of $\Delta V_{Tmax}$ given in equation 8. Through this value, dependence of the modeling results on bias and temperature values is given. Therefore, for different stressing conditions, value of $V_S$ is different as well. Although at first this looks as a serious limitation, based on our earlier studies, it is possible to estimate the interdependence of time, voltage, temperature and $\Delta V_T$ of investigated VDMOSFETs using the results obtained by accelerated NBT stressing [39, 40].

To do modeling based on experimental data, it is needed to find a function that describes experimental data sets, and then to calculate modeling circuit element values based on a fitting function parameter. Most appropriate method for this fitting is Least Square Method (LSM) [41]. LSM is one of the most widely used method to find or estimate the numerical values of the parameters.

**Table 1:** Values of $V_S$ for different stressing conditions calculated by SE equations.

| Stressing Temperature [°C] | Stressing Voltage [V] | Value of $V_S$ [V] |
|---|---|---|
| 150 | - 45 | 0.182 |
| | -50 | 0.395 |
| 175 | - 45 | 0.312 |
| | -50 | 0.513 |

It can also be used to fit a function to a set of data and to characterize the statistical properties of the estimates [42-44]. LSM is a mathematical method for finding the best-fitting curve to a given set of points by minimizing the sum of the squares of the offsets of the points from the curve. Basic principle of the LSM implies that a set of *I* pairs of data points given with $(x_1, y_1)$, $(x_2, y_2)$, … $(x_I, y_I)$ is used to find a function that describes dependence of *y* from independent variables *x*. A curve that is created from the experimentally measured data points can be presented in the generic power form given as:

$$y^* = A \cdot t^B \tag{9}$$

In equation (9), $y^*$ represent modeled function, while *A* and *B* are free fitting parameters. This form of the modeling function is the most suitable one since the parameter $t^n$ that should be relevant with modeled data also has power evolution. Parameters *A* and *B* specify the slope of the modeling function and determine the regression line. LSM defines the estimate of these parameters as the value which minimizes the sum of squares between the measurement (*y*) and the model ($y^*$) which leads to expression:

$$\varepsilon = \sum_i \left(y_i - y_i^*\right)^2 = \sum_i \left(y_i - \left(A \cdot t^B\right)\right)^2 \tag{10}$$

In the equation (10), $\varepsilon$ stands for error which is a value to be minimized. The most suitable way to calculate parameters *A* and *B* is to introduce matrix notation in the following way:

$$\vec{a} = \begin{bmatrix} A \\ B \end{bmatrix} \tag{11}$$

$$X = \begin{bmatrix} 1 & x_1 \\ 1 & x_2 \\ 1 & x_3 \\ \vdots & \vdots \\ 1 & x_i \end{bmatrix} \tag{12}$$

$$G = \begin{bmatrix} \ln f(x_1) \\ \ln f(x_2) \\ \ln f(x_3) \\ \vdots \\ \ln f(x_i) \end{bmatrix} \tag{13}$$

Vector $\vec{a}$ consists of the parameters that need to be calculated. Matrix *X* is created from the time points when the measurements were done, while the matrix *G* consists of logarithm of values being measured in the time points. Calculation of a vector $\vec{a}$ is given with the equation:

$$\vec{a} = \left(X^T X\right)^{-1} X^T \cdot G \tag{14}$$

After performing matrix calculus for different stressing conditions, parameters A and B are calculated and given in the Table 2.

**Table 2:** Calculated parameters *A* and B for different NBTS conditions.

| Stressing Temperature [°C] | Stressing Voltage [V] | Parameter A | Parameter B |
|---|---|---|---|
| 150 | -45 | 0.00772 | 0.27032 |
| | -50 | 0.01254 | 0.29692 |
| 175 | -45 | 0.00798 | 0.31088 |
| | -50 | 0.01453 | 0.30617 |

After acquiring fitting parameters, A and B, it is needed to equalize equation (9) with the equation that describes capacitor charging (7). Even though it is mathematically simpler to use exponential form with least square approximation, negative exponent in the capacitor charging formula reverses the convexity of the function. Reversed convexity can introduce a lot of mathematical problems, delivering inadequate poor modeling results. After solving equations, variable $\tau$ is calculated. However, even after that calculation is concluded, problem of calculating precise resistance *R* and capacitance *C* that compose $\tau$ still remains. For modeling purpose, value of capacitance is set to 1 mF. Basic modeling circuit is given in Figure 2.

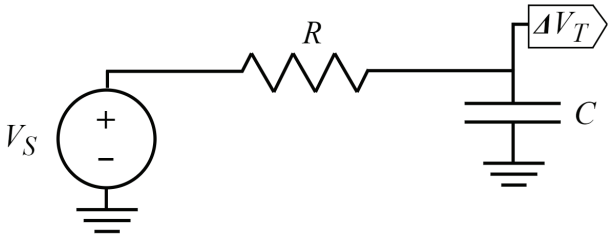



**Figure 2:** Basic RC circuit for $\Delta V_T$ modeling.

Since the variety of the time constants can be found in the progress of the $\Delta V_T$, modeling with only one specific RC connection could lead to considerable dissent in the particular parts of the curve. Parameters *A* and *B* are calculated for the full period of stressing time.

The concept of improved modeling is to present the experimental curve as the product of multiple parts. These parts are to be determined by the phases of parameter *n* evolution, in favor of increasing of the accuracy of the model. To conduct this improvement, additions to the modeling circuit must be made. To follow evolution of $\Delta V_T$, charging rate of the capacitor is to be different in different time intervals. A method for enabling charging rate diversity is to increase the number of RC connections. With the range of different time constants, capacitor voltage can adapt more precisely to $\Delta V_T$. Adding switches and enabling only specific RC connections in determined time periods leads to capacitor voltage being additionally determined. Greater number of RC connections can be achieved in multiple ways, either by increasing number of resistors that are charging one capacitor, either by increasing number of capacitors that are charged through one resistor or either by increasing number of both resistors and capacitors. Since the principle of this modeling is that capacitor voltage models $\Delta V_T$, number of capacitors is set to one. This way, complicate procedure of summing of capacitor voltages that corresponds to $\Delta V_T$ in different time periods is avoided, while concept is sustained. With only one capacitor, only way to increase number of RC connections is with increasing number of resistors.

With the goal to link phases of degradation with number of RC connections, modeling circuit is expanded with two additional resistors and switches. Expanded circuit is given in Figure 3.

In the starting moment, both switches, $S_1$ and $S_2$ are closed. Capacitor *C* is charged through all of three resistors. Since the resistors are connected in parallel, equivalent resistance is lower than the resistance of the

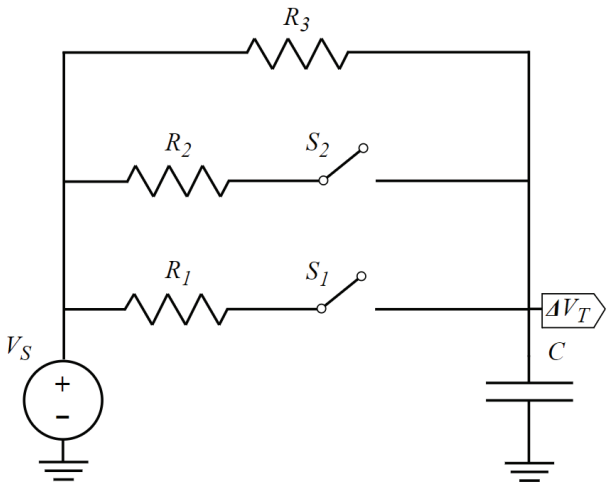



**Figure 3:** Expanded circuit for modeling of static stress.

resistor with lowest resistance. Growth of $\Delta V_T$ is largest in starting phase of stressing, so the capacitor $C$ is charged through lowest resistance, which is in line with model expectations. After starting phase, switch $S_1$ opens, so that capacitor $C$ continues to charge through parallel resistance of resistors $R_2$ and $R_3$ only.

To provide suitable results and follow properly $\Delta V_T$, it is important that $R_3 > R_2 > R_1$. That way, equivalent resistance of resistors $R_2$ and $R_3$ is greater than the equivalent resistance of all three resistors. After opening switch $S_1$, capacitor is charged through higher resistance than before opening the switch, leading to slower capacitor charging and lower slope of the charging curve.

Higher charging resistance leads to even slower charging, which is, once again, in line with the model expectations, and describes development of $\Delta V_T$ during stressing. To find appropriate values of resistance LSM is used again. This time, every phase is approximated separately, LSM is applied 12 more times, leading to parameters $A_1$, $A_2$, $A_3$ and $B_1$, $B_2$ and $B_3$. According to these parameters and in consideration with equivalent resistance equations, resistance of resistors $R_1$, $R_2$ and $R_3$ are calculated. Results of different stressing conditions are given in the Table 3. Error of the estimated parameter is calculated using R-squared method and is between 0.95043 and 0.98268 for modeling with basic circuit and between 0.98764 and 0.99262 for modeling with expanded circuit. Modeled results using expanded modeling circuit are given in Figure 4 and 5.

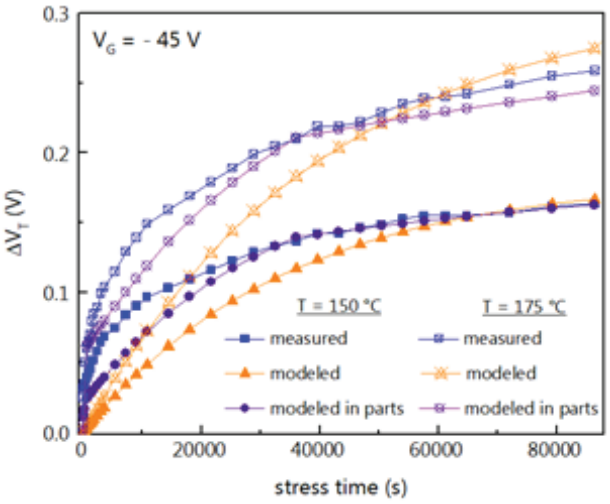



**Figure 4:** Values of $\Delta V_T$ obtained by measuring and with modeling for T = 150 ˚C and for T = 175 ˚C where $V_G$ = -45 V.

Results given in the Figure 4 and Figure 5 show that modeling error is considerably reduced if the modeling is done with taking in mind phase division of the pa-

**Table 3:** Values od parameters $A_1$ – $A_3$, $B_1$ – $B_3$ and resistances $R_1$ – $R_3$ for different stressing conditions.

| Stressing Temperature [°C] | 150 | | 175 | |
|---|---|---|---|---|
| Stressing Voltage [V] | -45 | -50 | -45 | -50 |
| Phase 1 (0 < t < 600 s) | | | | |
| A1 | 0.02191 | 0.02191 | 0.00544 | 0.00475 |
| B1 | 0.08548 | 0.20024 | 0.38145 | 0.53067 |
| R1 [MΩ] | 10.1215 | 2.9499 | 2.9304 | 3.2873 |
| Phase 2 (600 s < t < 36000 s) | | | | |
| A2 | 0.00504 | 0.00926 | 0.00793 | 0.01092 |
| B2 | 0.31566 | 0.32872 | 0.31336 | 0.33571 |
| R2 [MΩ] | 46.7246 | 71.4286 | 56.5297 | 82.6446 |
| Phase 3 (36000 s < t < 86400 s) | | | | |
| A3 | 0.01731 | 0.02279 | 0.01754 | 0.01857 |
| B3 | 0.19832 | 0.24382 | 0.23718 | 0.28539 |
| R3 [MΩ] | 87.8942 | 58.7951 | 128.9552 | 53.6646 |

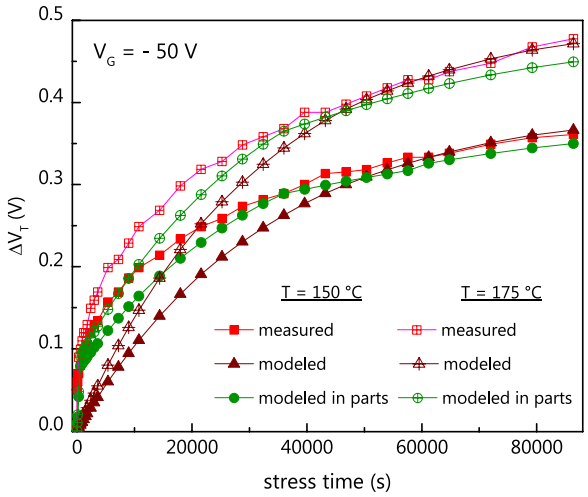
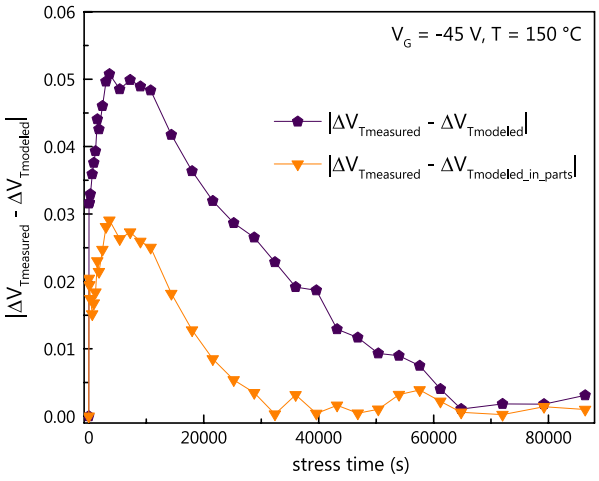



**Figure 5:** Values of $\Delta V_T$ obtained by measuring and with modeling for T = 150 ˚C and for T = 175 ˚C where $V_G$ = -50 V.

rameter *n* evolution. This is notable especially during the second phase of $\Delta V_T$ development. Since the third phase occurs after approximately 10 hours of stressing [6, 38], during the experiment, samples are subdued to this phase the longest. When approximating full range of experimental data, LSM adapts parameters better for the longest lasting phase, and thereby, creating a slightly greater mismatch for the rest of the data. With this type of phase division, modeling error is more than twice decreased, as can be seen in Figure 6.

**Figure 6:** Difference in absolute errors of proposed modeling approaches for T = 150 ˚C and $V_G$ = -45 V.




Results given in Figure 6 show that modeling error has very similar form to the evolution of the parameter *n*, given in the Figure 1 (inserted graphic), which is fundamental signature of NBTI. With additional resistors and switches, used in the expanded modeling circuit, slope of the curve that shows modeling error is decreased (peak of the error is reduced by half, and error is reduced even more in the other parts of the curve). This result is in line with the modeling approach. Further expansion of the circuit (adding more RC connections, and splitting degradation phases into more phases that are shorter, would impact in even more decreased slope).

However, even with further increase in number of resistors, in the specific shorter time interval, time constant will be uniform. To design even more accurate model, number of RC connections is to depend not only on stressing time or phase, but on the actual numbers of individual defects in the circuit itself [29]. With increasing the number of defects, number of RC connections rises, thereby increases the overall sum of the voltages that comprise $\Delta V_T$.

## 4 Conclusions

Impacts of static negative bias temperature stressing in p-channel power VDMOSFETs IRF9520 have been reported. An equivalent electrical circuit is designed in order to model the behavior of $\Delta V_T$. Mathematical method of least square approximation is described and conducted to determine and to acquire parameters for values of modeling circuit elements. Phase division of parameter *n* evolution during modeling leads to better overall results in terms of accuracy and precision, regardless of stressing conditions. Future steps of work include improving the model with adapting it to the modeling of pulsed stress as well, since p-channel power VDMOSFETs are widely used in switching circuits because of their good switching characteristics.

## 5 Acknowledgments

This work has been supported by the Ministry of Education, Science and Technological Development of the Republic of Serbia and in part by the Serbian Academy of Science and Arts.

## 6 Conflict of Interest

The author declares no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results

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Arrived: 24. 07. 2020
Accepted: 21. 10. 2020

Original scientific paper
https://doi.org/10.33180/InfMIDEM2020.306

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 50, No. 3(2020), 215 – 230

# A High Voltage Gain Multiport Zeta-Zeta Converter for Renewable Energy Systems

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**Abstract:** In this paper, a zeta-zeta coupled non-isolated multiport converter is proposed and implemented. This new dc-dc multiport converter facilitates the access of two renewable energy sources in the input side with a single output. Zeta converter topology facilitates high voltage gain with a reduced output voltage ripple. Multiport converters have become very prominent in the recent past due to the prevalent establishments of distributed energy resources. But in the research arena, there is no literature evidence for Zeta –Zeta converters used in multiport converters. This research work proposes a Zeta-Zeta multiport converter with reduced number of switches for renewable energy systems. The proposed converter is simulated in MATLAB/ Simulink environment and is also realized as a hardware prototype. The voltage gain and efficiency of the proposed circuit is compared with its counterpart multiport topologies. The simulation and hardware results show that the proposed topology is having a clear edge on its counter parts in voltage gain and efficiency.

**Keywords:** renewable energy; dc-dc converter; multiport converter; zeta converter; photovoltaic; battery.

# Več vhodni zeta-zeta pretvornik z visokim napetostnim ojačenjem za sisteme obnovljivih virov

**Izvleček:** Članek opisuje neizoliran več vhodni zeta-zeta pretvornik. Nov dc-dc pretvornik omogoča priklop dveh obnovljivih virov na vhodu in skupen izhod. Topologija zeta pretvornika omogoča visoko napetostno ojačenje in znižan izhoden ripple. Več vhodni pretvorniki so postali pomembni v zadnjih letih s pojavom distribuiranih virov energije. Kljub temu v literaturi ni opaziti navedb zeta-zeta pretvornikov. Predlagan več vhodni pretvornih z znižanim številom stikal je simuliran v MATLAB/Simulink okolju in realiziran kot prototip. Napetostno ojačenje in izkoristek sta primerljiva s konkurenčnimi topologijami.

**Ključne besede:** obnovljivi viri; dc-dc pretvornik; več vhodni pretvornik; zeta pretvornik; fotovoltaika; baterije.

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## 1 Introduction

In the present scenario, the increase in power demand with depleting conventional energy resources urges to have power generation through renewable energy sources. Renewable energies like solar, wind and fuel cells of different capacities are being deployed to meet the additional demand. Thus, high penetration of sustainable energy into the grid paves way for the development of integrated power converters which facilitates appropriate synchronization. These are capable of interfacing and controlling the energy from the various input terminals. Multiport converters are capable of optimizing the power from various renewable sources with optimum switches. Owing to the striking merits such as low cost and small structure, many multiport configurations have been offered for numerous applications such as for satellites, hybrid electric vehicle etc,[1]. The multiport converter topologies are competent enough to interface and regulate many power sources as shown in Figure1. But due to this

there is a chance of increase in number of switches in the circuit and the efficiency may reduce[2].Hence, the research on proposing new topologies with multi input structures thereby optimizing the number of switches has become very vital. H.Matsuo proposed a buck-boost converter that accommodates two inputs with a magnetic coupling reactor [3]. A solid-state transformer (SST) based quad active converter bridge is implemented in [4], wherein SST provides isolation from the load. Here, the number of active devices involved in the circuit is more which is a major drawback. Hence, isolated multiple dc-dc converter for effective power management with multiple renewable sources is proposed [5, 6]. The output of these multiple converters were fed to a common dc bus and then delivered to the load. These converters require more control strategies. In order to avoid multiple converters for multiple energy sources, new multiport converters (MPC) were designed. MPCs are classified based on i) port placement structures such as a)Multi Input Single Output (MISO), b) Single Input Multi Output (SIMO) and c) Multi Input Multi Output (MIMO)), ii)based on coupling (isolated and non-isolated) [7] iii)based on connections (series and parallel) and iv) based on conversion process (unidirectional and bidirectional).

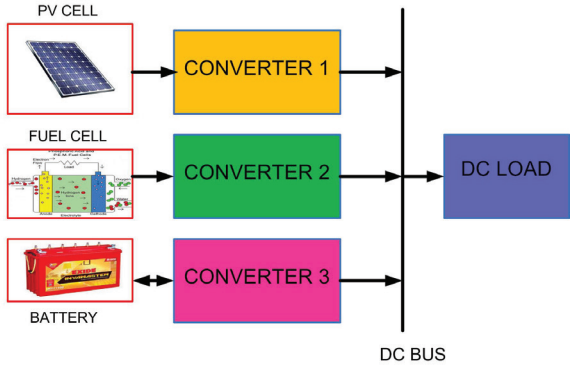


**Figure 1:** Conventional multi-input, multiple converters.

A systematic way of synthesizing multiport converter from a full bridge, bidirectional dc-dc converter is reported in [8, 9]. Interesting topologies of multiport converters are derived by a combination of full bridge, half bridge/series resonant topologies via magnetic coupling using utility multi winding transformer [10-12]. Most of the literature focuses on the development of multiport converter (MPC) using traditional buck boost topology [13]. A three port converter with three active full bridges with three winding transformer is proposed in [14, 15] wherein two series resonance tanks added for reliable high frequency operation. The converter seemed to be bulky and hence three port bridge converters came into existence. In [16], cross coupling control strategy is investigated for a photovoltaic (PV) based three port dc-dc TAB (triple active bridge) converter. In [17], the author discussed different parallel circuit topologies. For multiple energy resources the multiport converter was then modified to multi-input single output (MISO) structure, that combines different sources at the input side and supplies a single output [18,19]. In single input multi output (SIMO), the outputs can be fed to different applications. In series topology, current in the weakest link blocks the current of the whole string [20], introduces high electrostatic potential and causes voltage sag problem [21]. So, parallel connected topologies are mostly preferred over series connected topologies.

Bidirectional power flow topologies were investigated for efficient power control. To allow bidirectional power flow and to integrate different sources, DC link and magnetic coupling inductors were incorporated in deriving multiport converters [22, 23]. A high step up bidirectional converter with high voltage is discussed in [24, 25]. Also, large number of electric vehicles connected to the grid affects the supply voltage quality.

Therefore, to meet the high current demand, bidirectional high-power three-phase three-port converter is designed for fast charging stations [27, 28]. With increase in high voltage, high voltage ripples were also increased. So, in order to minimize the voltage ripple [26] an active clamping circuit is incorporated that increased the efficiency too. These multiport converters are designed both for off grid and on grid utility. Conventional grid systems are designed for specific power demand. In [29], a high frequency transformer is incorporated in an isolated multiport converter system for effective power flow management between high voltage dc transmissions (HVDC), networks in Electric aircraft (MEA) etc.

After extensive use of buck, boost, buck boost topologies, special converters such as Cuk, Zeta and Sepic converters came into existence. Comparative analyses of Cuk, Zeta, Sepic, Buck and Boost converters were performed [38]. Cuk converter gives a negative output voltage, while Sepic converter gives a positive output voltage but requires a continuous input current. Zeta converter gives a high voltage gain with lesser output voltage ripples. Owing to these disadvantages of Cuk and Sepic, Zeta converters are preferred for use in multiport converters for renewable energy applications because of compatibility. Zeta converter is a buck boost derived converter, where power factor correction is done. It is applied for LED lightings and welding purposes, but with low output power in [30,31]. [32] Explains that zeta converter takes maximum power from photovoltaic cells. A comparative analysis of boost and zeta converters have been dealt in [33, 34]. Though iso-

lated converters provide electrical galvanic isolation, they house more number of components resulting in large size. In [35], a deduction method is proposed which is based on a series of voltage balancers. Zeta converter was designed to feed a four phase switched reluctance motor whose input is from a PV source. Zeta converter and Landsman converter were integrated to form a multiport converter with different control circuits in [36]. This zeta converter also called as dual sepic converter is derived from a buck boost dc-dc converter to obtain a high voltage gain [37].The converter proved to show greater efficiency, but the disadvantages are that it uses more number of passive elements and is isolated. In order to rectify the issues cited in few of the above converters, a single stage non isolated power converter utilizing zeta converter has been designed in this paper.

## 2 Multiport converter

From the research on multiport converters, it has been observed that non isolated zeta converters have not been used so far. The zeta converter contributes in either increasing or decreasing the input voltage and also gives a low ripple output voltage that can be applied for applications that needs constant output voltage. This non isolated structure is compact with a single switch control. Depending on the advantages and feasibility of zeta, the multiport converter is designed as a zeta-zeta combination suitable for renewable input sources.

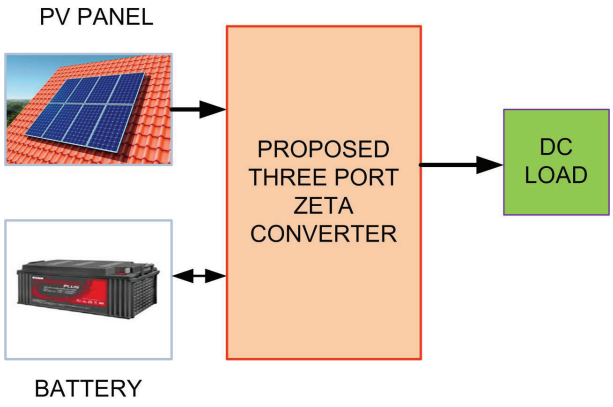


**Figure 2:** Proposed Zeta-Zeta Multiport converter

The primary focus of this paper is therefore to design a novel non isolated DC-DC converter based on zeta topology using DC link capacitors. This multiport converter (MPC) circuits accommodate one or more renewable input sources and a battery source. Based on the applications, the developed MPC can work as unidirectional or bi-directional circuit as shown in Figure2.

The zeta converter gives a high voltage gain with lesser output voltage ripples. Discontinuous input current can also be fed to the zeta converter.

The different operating modes of the three-port zeta converter have been analyzed. The circuit has been designed using small ripple approximation method. The simulation and hardware results have been shown in this paper.

## 3 Proposed multiport zeta-zeta converter

The Zeta converter shown in Figure 3 is a fourth order converter that has two capacitors ($C_1$, C2), two inductors ($L_1$, $L_2$) which can step up and also step down the input voltage. It is used in power factor correction and regulation of voltages. It gives a non-

inverting output with a continuous input current [30]. The second order harmonic output voltage ripples are smaller.

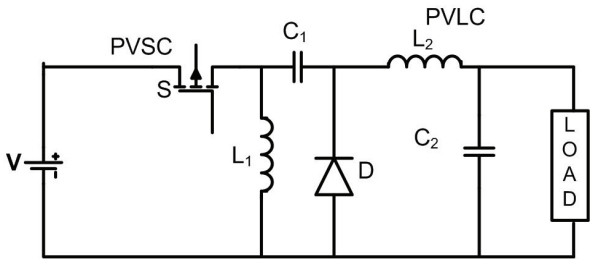


**Figure 3:** Basic Zeta converter circuit

Owing to the advantages of zeta, the proposed three port Dual Input Single Output (DISO) Zeta converter has been constructed by paralleling the basic structure.

In this paper, the basic Zeta structure is decomposed into two parts namely Pulsating Voltage Source Cell (PVSC) and Pulsating Voltage Load Cell (PVLC) to form a multiport converter, as shown in Figure 4. Two PVSCs have been developed from two basic zeta converters and coupled with PVLC in the proposed circuit.

Two topologies of multiport converters (unidirectional and bidirectional) are presented. Three ports are designed here, which can further be increased to 'n' number of ports.

### 3.1 Operation and Control Approach

The three-port zeta converter presented in Figure 4 has two input ports and one output port. The three-port zeta converter is provided with a photovoltaic source along

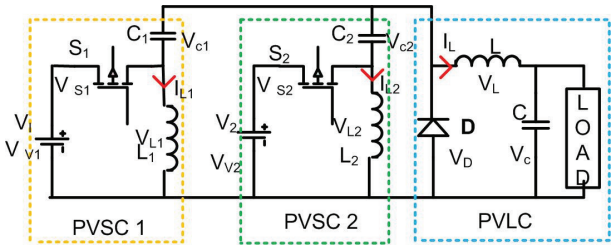


**Figure 4:** Non isolated three port zeta converter

with a battery backup or with a rectified input source from wind or with a fuel cell. Depending upon the available inputs, the converter works in unidirectional mode as shown in Figure 4 and in bidirectional mode as shown in Figure 8. Both topologies have been explained as topology 1 (unidirectional) and topology 2(bidirectional).

*3.1.1 Topology 1: Three Port zeta as unidirectional converter*

To understand the operation, assume the converter is interfaced with a PV source and a rectified input from a wind energy system. Let the input voltage from source 1 be $V_1$ and source 2 be $V_2$ with duty cycles $D_1$ and $D_2$ respectively. With the same voltage and duty cycles, the converter acts like an individual zeta converter and supply power simultaneously.

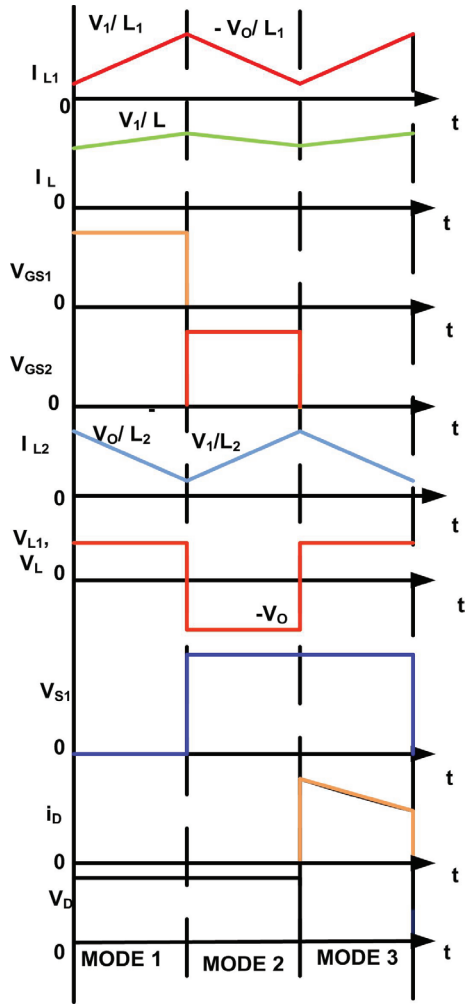


**Figure 5:** Key waveforms for Topology 1, when the converter is operating in unidirectional mode

The key waveforms of the three-port zeta-zeta converter operating in continuous conduction mode are depicted in Figure 5. The waveforms of the current through the inductors, voltage across the switches $S_1$ and $S_2$, current through the diode, voltage across the inductors are shown when the converter is operating in unidirectional mode.

If $V_1 = V_2 = V$, the output voltage expression will be,

$$Vo = \frac{DV}{1-D} \tag{1}$$

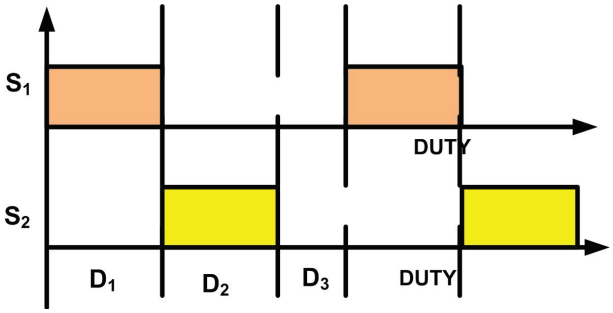


**Figure 6:** Operating modes of the proposed converter

Assuming $V_1 > V_2$ and $D_2 > D_1$, ($D_1$ and $D_2$ – duty cycles) as given in Figure 6, there are three modes of operations that are explained below:

Mode-1 ($S_1$ on, $S_2$ off): The equivalent circuit of mode 1 is shown in Figure 7a. In mode 1, as $V_1$ is greater than $V_2$, $S_1$ is switched ON and switch $S_2$ is switched OFF, the output voltage across R load is contributed by $V_1$ only. When $S_1$ is closed, inductor $L_1$ gets charged by $V_1$. The capacitor $C_1$ is assumed to be pre-charged. It later discharges along the inductor L and load.

Applying the concept of voltage-second balance on inductors and charge balance on capacitors, the follow-

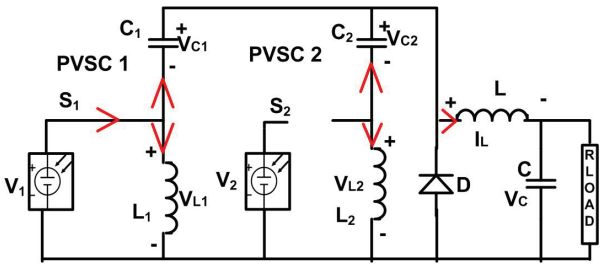


**Figure 7a:** When PVSC 1 feeds the load

ing expressions have been developed. Let "$T_S$"–be the total conducting time of the switch.

$$V_1 = V_{L1} \tag{2}$$

$$V_1 + V_{C1} - V_{C2} = V_{L2} \tag{3}$$

$$I_C = I_L - \frac{V_o}{R} \tag{4}$$

Mode-2 ($S_1$ off, $S_2$ on): After a duty cycle of $D_1$, switch $S_1$ is switched off and instantly switch $S_2$ is closed (mode-2). So $V_2$ starts supplying the load (Figure 7.b)

$$V_2 = V_{L2} \tag{5}$$

$$V_2 + V_{C2} - V_{C1} = V_{L1} \tag{6}$$

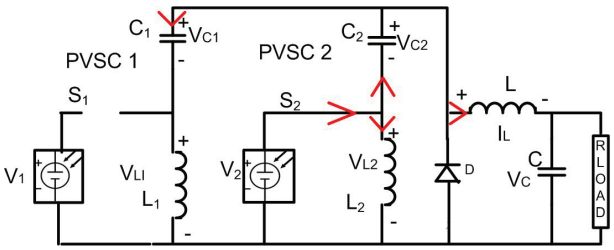


**Figure 7b:** When PVSC 2 feeds the load

Mode-3 ($S_1$ and $S_2$ off): When both switches are open, the charge stored in the inductors will support the conduction. Now the diode is forward biased and acts as a closed switch allowing current to move from its anode towards cathode as shown in Figure 7.c.

$$V_{L1} = V_{C1} \tag{7}$$

$$V_L = V_0 \tag{8}$$

Assuming $V_{C1} = V_{C2}$,
Equation (9) has been framed by applying the voltage-second balance to inductors and charge balance on capacitors.

$$\int_0^{T_s} V_{L2}(t)\,dt = (V_1 + V_{C1} - V_0)D_1T_s + \\ +(V_2 + V_{C2} - V_0)D_2T_s + V_0\left[1-(D_1+D_2)\right] = 0 \tag{9}$$

$$Vo = \frac{\left(V_1 - \frac{V_1D_1 + V_2D_2}{1-(D_1+D_2)}\right)D_1 + \left(V_2 - \frac{V_1D_1 + V_2D_2}{1-(D_1+D_2)}\right)D_2}{D_1 + D_2 - (1-(D_1+D_2))} \tag{10}$$

So the capacitor $C_1$ gets charged by the inductor $L_1$ and $C_2$ gets charged by inductor $L_2$. In topology 1, since both sources are renewable energy resources, the converter behaves as unidirectional converter and the flow of energy is from source to load.

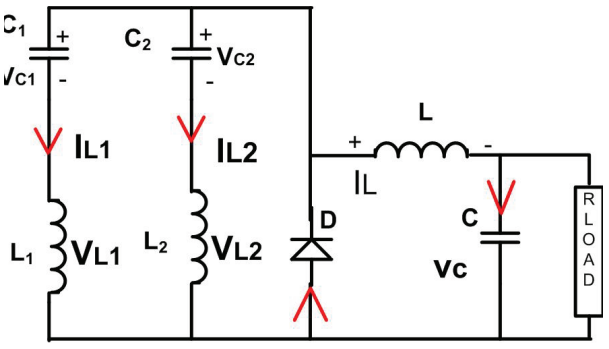


**Figure 7c:** When both $S_1$ and $S_2$ are OFF

*3.1.2 Topology 2: Three Port zeta as bidirectional converter*
To analyze the working, the proposed three port bidirectional Zeta converter is reconstructed with an additional switch $S_3$ as shown in Figure 8.The first input port is connected to a PV source and the second is connected to a battery whereas the output port is connected to the load.

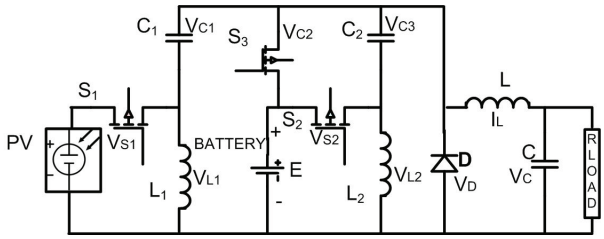


**Figure 8:** Three Port bidirectional Zeta converter-Topology 2

The energy transfer in this converter can be explained in four ways

1) From PV Source to load
2) From PV Source to battery and load
3) From battery to load
4) From load to battery.

After harvesting maximum power from PV source, it is interfaced to the load via a dc link capacitor. Any unbalancing that occurs during integration will be controlled by charging and discharging action of the battery. Here the switches $S_2$ and $S_3$ complement each other. For charging the battery, $S_3$ is to be turned ON and corresponding $S_2$ is OFF. In case of back EMF, all the PVSCs are turned off and only $S_3$ is turned on. The operation of integrated power system has four possible operating modes which are consolidated in Table 1. Here "E" is the voltage across the battery.

Mode 1: When V > E, battery charges through switch $S_3$ and the (source1) PV supplies power to the load. We can say that the converter acts as a partial bidirectional converter in Single Input Dual Output (SIDO) mode as in Figure 9a.

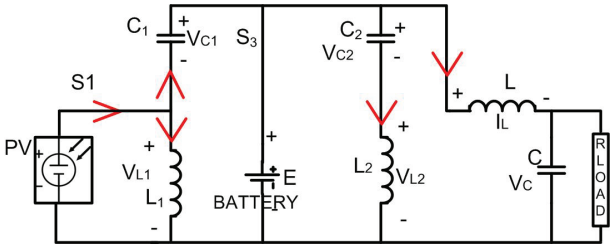


**Figure 9a:** When V >E, $S_1$ and $S_3$ are ON, $S_2$ is OFF

Mode 2: When V < E, battery discharges through switch $S_3$ as in Figure 9.b and the load receives power from the battery and the converter operates in SISO mode.

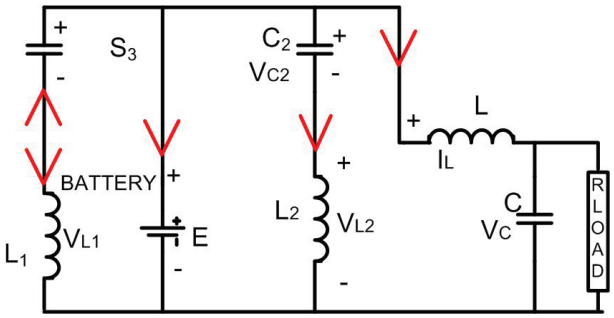


**Figure 9b:** V < E , $S_1$ and $S_2$ are OFF, $S_3$ is ON

Mode 3: When V = E, the load receives power from the PV and battery. The converter operates in Dual Input Single Output (DISO) mode as shown in Figure 9c.

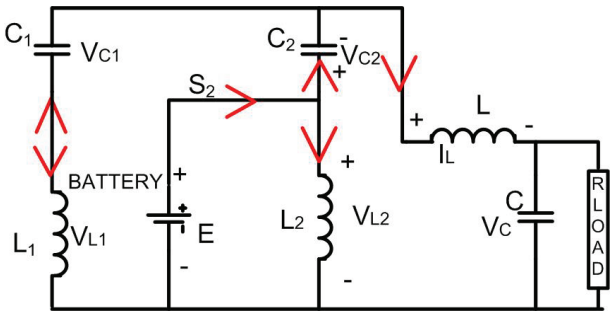


**Figure 9c:** When V=E, $S_2$ is ON, $S_1$ and $S_3$ are OFF

Mode 4: When V = 0 and E< state of charge (SOC), the load supplies power by the charging action of the battery through switch $S_2$. The converter in Figure 9d operates as a bidirectional converter in SISO mode.

With respect to the operating modes, the equivalent circuit for each mode is developed as shown from Figure 9.a to Figure 9.d. When PV voltage is greater than or equal to battery, PV will be supplying the load. Table 1 shows the different modes of operation of PV and battery.

The steady state equations of the converter are as follows.

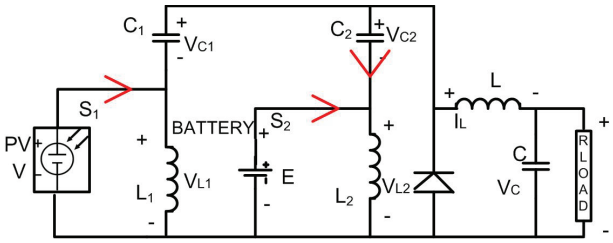


**Figure 9d:** When V=0, $S_1$ and $S_2$ are ON, $S_3$ is OFF

**Table 1:** Different Modes of Operation of PV and Battery

| Mode | Switch Status | Source1 (PV) | Source 2 (Battery) |
|---|---|---|---|
| V > E | $S_1$ and $S_3$ are ON and $S_2$ is OFF | Supplies power to load | Charges |
| V < E | $S_3$ is ON and $S_1$ , $S_2$ are OFF | - | Discharges |
| V = E | $S_1$ and $S_3$ are OFF and $S_2$ is ON | Supplies power to load | Discharges and Supplies power to load |
| V = 0 and E < SOC | $S_1$ and $S_2$ are ON and $S_3$ is OFF | - | Charges due to EMF present in the load |

When battery is charging:

When both $S_1$ and $S_3$ are ON

$$V_1 + V_{C1} - V_{C2} = V_{L2} \tag{11}$$

$$V_1 + V_{C1} - V_0 = V_L \tag{12}$$

When battery is discharging:

When both $S_1$ and $S_3$ are OFF, $S_2$ is ON

$$V_1 + V_{C2} - V_0 = V_2 \tag{13}$$

When $S_1$ and $S_2$ are ON and $S_3$ is OFF

$$V_{C1} = V_{L1} \tag{14}$$

$$V_{C2} = V_{L2} \tag{15}$$

Applying the voltage-second balance inductors and charge balance on capacitors

$$V_0 = \frac{V_1 D_1 - \frac{V_1 D_1^2}{1 - D_1}}{2D_1 - 1} \tag{16}$$

### *3.2 Determination of circuit parameters:*

For the converter in CCM, the ripple voltage should be kept at minimum value. Applying the concept of small ripple approximation, the expressions of $L_1$, $L_2$, L, $C_1$, $C_2$, and C with reference to current and voltage ripples are derived. In mode 1 and mode 2 the current of the inductor increases from a lower level to higher level, say $I_{L11}$ to $I_{L12}$ and in next mode, the current drops from $I_{L11}$ to $I_{L12}$. So, the current ripple is observed to be

$$\Delta I_{L1} = I_{L12} - I_{L11}$$, f – frequency

$$L_1 \frac{di_{L1}}{dt} = V_1 + V_2 \tag{17}$$

f = 1 / T where T is the total switching time period.

$$\Delta I_{L1} = \frac{(V_1 + V_2)(D_1 + D_2)}{fL_1} \tag{18}$$

Assuming $L_2$ is charged linearly during the period $t_2$ and $t_3$ from $I_{L21}$ and $I_{L22}$, the inductor current ripple is

$$\Delta I_{L2} = \frac{(V_1 + V_2)(D_1 + D_2)}{fL_2} \tag{19}$$

The values of inductors and capacitors are obtained from the following equations

$$L_1 = \frac{(V_1 + V_2)(D_1 + D_2)}{f\Delta I_{L1}} \tag{20}$$

$$L_2 = \frac{(V_1 + V_2)(D_1 + D_2)}{f\Delta I_{L2}} \tag{21}$$

$$C_1 = \frac{I_{L1}(1 - D_1)}{f\Delta V_{C1}} \tag{22}$$

$$C_2 = \frac{I_{L2}(D_1 + D_2)}{f\Delta V_{C2}} \tag{23}$$

## *4 Simulation and experimental results*

### *4.1 Simulation:*

The simulation model of the non-isolated zeta-zeta converter is developed with the help of MATLAB Simulink. The simulation results of the converter operating in CCM are shown in Figure 10.a and Figure 10.b. These waveforms were observed when the converter was operated in unidirectional topology.ie only switches $S_1$ and $S_2$ are turned on and switch $S_3$ remains off. The current flows only from source to the load in unidirectional mode of operation. The voltage across the switches $S_1$ and $S_2$ varies with change in duty cycles. The inductor currents $I_{L1}$ and $I_{L2}$ prove that the converter is operated in CCM mode and shows variations in time graph. The converter was simulated with the parameters as follows: $L_1$ and $L_2$ with 33mH, $C_1$and $C_2$ with 100 µF. The filter inductor $L_3$ = 1000µH and filter capacitor $C_3$= 140 µF. The inductor currents $I_{L1}$ and $I_{L2}$ prove that the converter is operated in CCM mode and shows variations in time graph. Also, the variations of charging and discharging voltages across capacitors $C_1$ and $C_2$ are shown in the plot. The simulation results of the converter operating in CCM are shown in Figure 10.a and Figure 10.b.

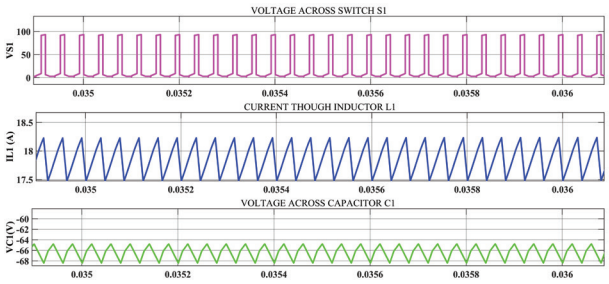


**Figure 10a:** Waveforms when PVSC1 supplies

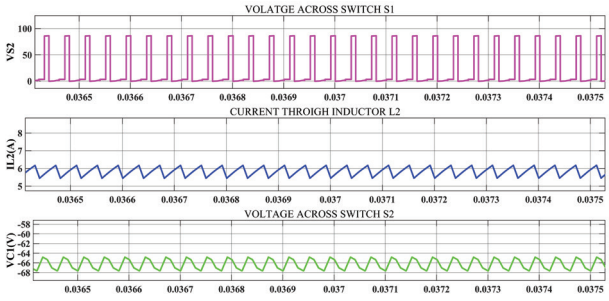


**Figure 10b:** Waveforms when PVSC2 supplies

These waveforms were observed when the converter was operated in unidirectional topology (only switches $S_1$ and $S_2$ are turned on and switch $S_3$ remains turned off). With duty cycles $D_1$ = 30% and $D_2$ =50%, the converter boosts the input voltages, $V_1$=$V_2$ = 20 V to $V_O$ = 60.73 V and $I_o$ = 1.084 A at R= 42 Ω. The output voltage and output current waveforms are depicted in Figure 11.

During turn on process of switches $S_1$ and $S_3$, the battery charges from the initial state of charge as shown in Figure 12. The initial state of charge (SOC) is taken as 5%. From the waveforms of battery parameters, the battery is charging in this case, as the SOC is increasing in nature. Therefore, when supply voltage is greater than the battery EMF, Source 1 (PV) supplies power to the load.

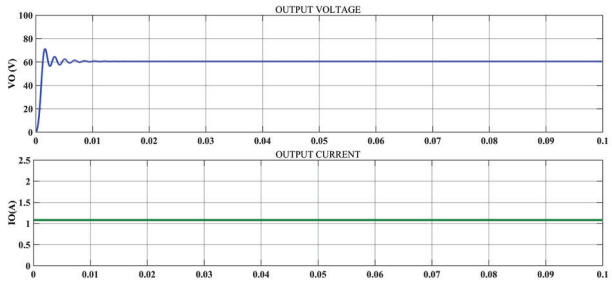


**Figure 11:** Output voltage and output current waveforms.

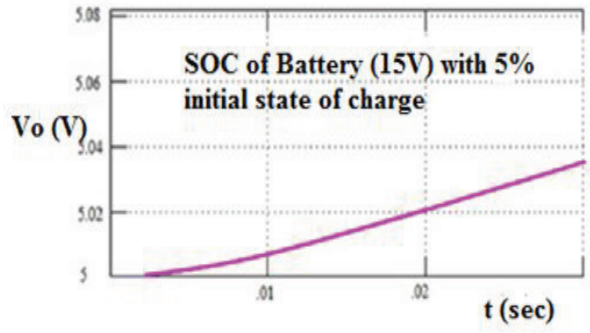


**Figure 12:** State of charge (SOC) of battery while charging

Figure 13, shows the MATLAB simulink outputs obtained for an input voltage of $V_1$ = 25V and the boosted output voltage is $V_O$ = 42V for a duty cycle of 70%., obtained across an output load resistor of 10 Ω.

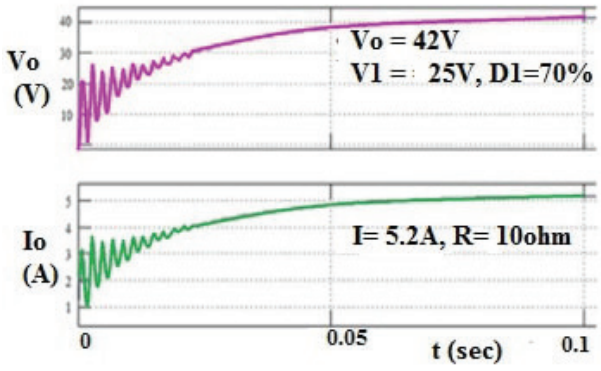


**Figure 13:** Output voltage and current when battery is charging.

As soon as switch $S_2$ is closed, the current through inductor and voltage across the capacitor increases due to discharging action of the battery as shown in Figure14.

When E > V, the battery which has charged in the previous cycle discharges and gives power to load which is shown in Figure 15.

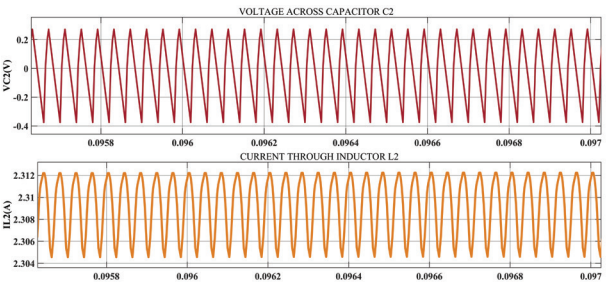


**Figure 14:** Inductor currents and capacitor voltages in bidirectional converter when battery is discharging

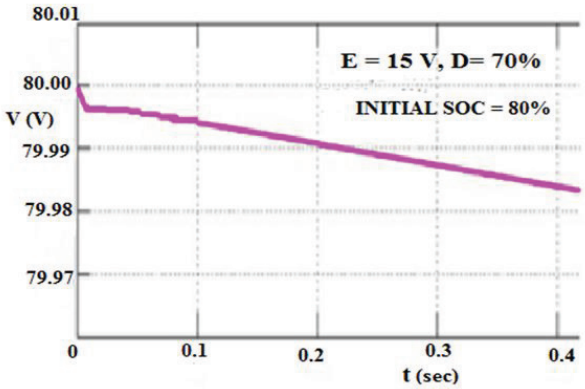


**Figure 15:** State of charge of battery while discharging.

The initial state of charge (SOC) is taken as 80%. From the waveforms of battery parameters, it is clear that the battery is discharging in this case, as the SOC is decreasing in nature.

The measured output voltage, Vo(actual) from the simulink model are cross-verified with the estimated output voltage Vo(estimated) for different sets of voltage inputs ($V_1$, $V_2$) along with duty cycles ($D_1$, $D_2$) and are tabulated in Table 2 and Table 3.

**Table 2:** Actual Values and Estimated Values of Output Voltage for different supply Voltages

| $V_1$ (V) | $V_2$ (V) | $D_1$ (%) | $D_2$ (%) | Vo (V) (actual) | Vo (V) (estimated) |
|---|---|---|---|---|---|
| 24 | 12 | 30 | 40 | 37 | 40 |
| 30 | 15 | 30 | 50 | 75 | 82.5 |
| 20 | 20 | 30 | 50 | 63 | 65 |
| 25 | 20 | 30 | 40 | 48.5 | 51 |
| 30 | 20 | 30 | 50 | 90 | 93 |
| 36 | 24 | 30 | 40 | 65 | 68 |
| 36 | 24 | 30 | 50 | 109 | 112.5 |

**Table 3:** Actual Values and Estimated Values of Output Voltage when the Battery is charging

| $V_1$ (V) | E (V) | D (%) | Vo (V) (actual) | Vo (V) (estimated) |
|---|---|---|---|---|
| 24 | 12 | 30 | 8 | 10.28 |
| 30 | 15 | 30 | 11 | 12.85 |
| 25 | 20 | 30 | 10.5 | 10.7 |

The results in the tables above further helps in plotting voltage gain and regulation curves. The estimated and actual values were compared.

*4.2 Design of controller for the proposed zeta-zeta converter:*

The intention of controlling a converter is to maintain a constant output voltage on the load side. Hence a closed loop feedback controller has been provided in the three-port zeta converter circuit. This is such that it feeds the dc load with constant output voltage with low ripple. Figure 16 shows the block diagram of the closed loop controller used for controlling the switches in the multiport converter.

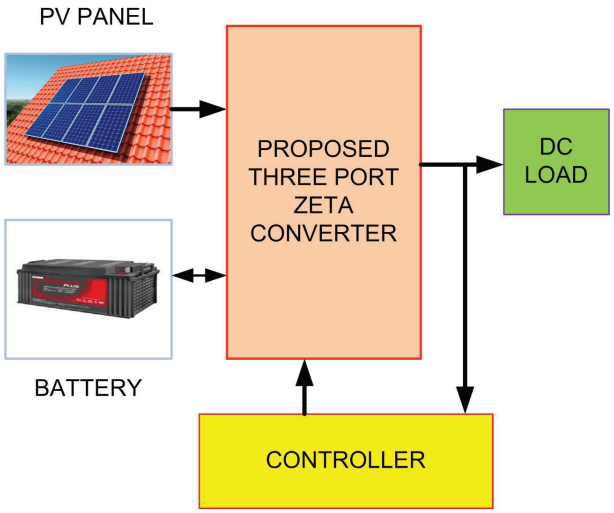


**Figure 16**: Block diagram of the multiport converter with controller

Small-Signal model of the controller:

When the converter is operating in continuous conduction mode, the circuit is realized in two modes. They are when the MOSFET turns on, it is in charging mode and when the MOSFET turns off, it is in discharging mode. In order to design a suitable controller for this system, a small signal model is developed using state-space averaging (SSA) technique.

The state space equations are given by

$$\frac{dx(t)}{dt} = Ax(t) + Bu(t) \tag{24}$$

$$y(t) = Cx(t) + Eu(t) \tag{25}$$

Where A is the system matrix, B is the control matrix, C is the output matrix and E is the identity matrix. On perturbation, the steady state solution for the proposed converter can be determined from the above equations resulting in

$$X = -A^{-1}BU \tag{26}$$

$$Y = \left(-CA^{-1}B + E\right)U \tag{27}$$

Where X is the state vector, U is the control vector and Y is the output vector.

The transfer functions of the closed loop controller system are derived by using SSA method.

i) The voltage gain of the zeta-zeta converter (when PV is supplied):

$$Vo(s)/Vin(s) = [\left(4x[10]\text{^}6\left(s\text{^}2+[10]\text{^}6\right)\right)/ \left(s\text{^}2+20.1s+1.208x\ [10]\text{^}5\right) \left(s\text{^}2+29.9s+8.279x\ [10]\text{^}6\right)] \tag{28}$$

ii) The voltage gain of the zeta-zeta converter (when battery is supplied):

$$\frac{Vo(s)}{Vin(s)} = \frac{6.5x10^6}{\left(s^2+50s+5x10^6\right)} \tag{29}$$

The transient state of the converter can now be determined using these transfer function relations. Since PV is used as input, the output voltage may vary with respect to the input. Hence PI Controller has been designed for the multiport converter in order to maintain a constant output voltage. This closed loop control system has been performed in MATLAB environment. The proportional gain constant $K_p$ and integral constant $K_I$ were obtained by Zeigler-Nichols PI tuning method. The $K_p$ was taken as 100 and $K_I$ as 0.1 in the PI controller.

A constant output voltage of 61V was obtained for an input voltage of 20V. When there is a change in load, the voltage slightly changes from one state to another, but still resumes the same constant output voltage of 61V. This change is known as transient as shown in Figure 17.

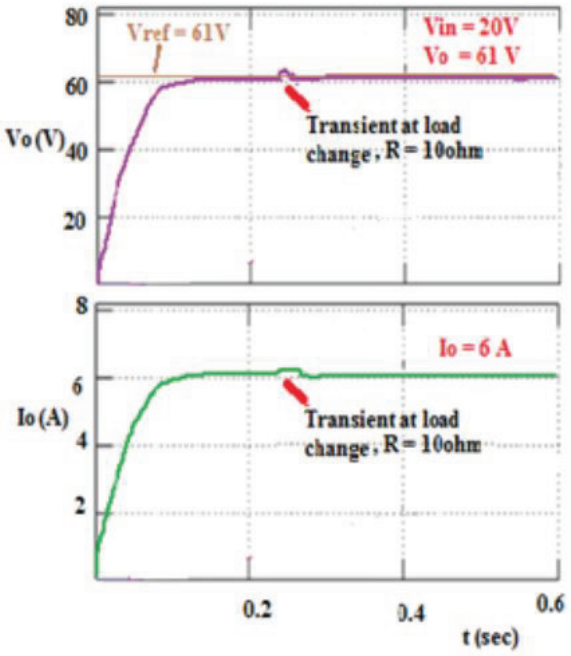


**Figure 17:** Simulated Output voltage and output current waveforms of closed loop converter.

A reference voltage of 61V was set in the controller. The output voltage was observed as 61V for a 15Ω load resistor. When the load was varied to 10Ω, there was a small transient (at t = 0.25sec) in the output voltage and output current. But the output voltage and current were maintained at the same constant values due to the action of the controller as depicted in Figure 17. The peak overshoot during open loop is 23% and it is 1.6% in closed loop. The steady state error has also been reduced to 0.01. In case of load changes, the multiport converter delivers a constant output voltage. Thus the use of controller results in constant output voltage.

The proposed zeta-zeta converter was simulated using MATLAB Simulink environment. The waveforms of voltage across the switches $S_1$, $S_2$, inductor currents and capacitor voltages are shown. When both sources are supplied with 20V input, the converter boosts to 61V output voltage and 6.29A output current, with 30% and 50% duty cycles. When PV voltage is greater than the battery voltage, then PV will supply the load. The initial SOC for charging is 5% and for discharging it is 80%. From tables 3 and 4, the simulated values are closer to the estimated values of output voltages.

### *4.3 Hardware results*

To illustrate the performance, a prototype model of bidirectional three port zeta converters, controlled by dSPACE real time controller is built with the specified parameters. The hardware set up is as presented in Figure 18.a and Figure 18.b. The power stage of this system consists of three port zeta topology with a load resistance of 50 Ohms. Switching devices IRFP 450 MOSFETs with switching frequency 38 kHz act as switches $S_1$, $S_2$ and $S_3$.

The view of the proposed multiport zeta–zeta converter is clearly shown in the hardware circuit of Figure 18a. The output voltage is shown in a closer view. Figure 18b shows the complete hardware set up of the proposed converter with dSPACE controller.

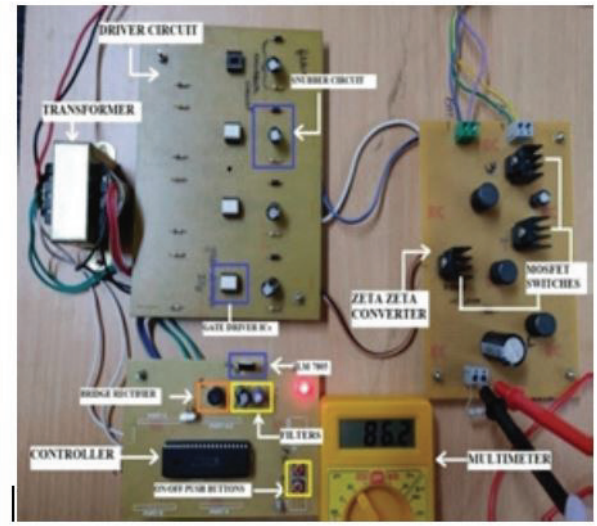


**Figure 18a:** Zeta-Zeta Hardware prototype

In this zeta-zeta converter prototype we have three MOSFET switches ($S_1$, $S_2$ and $S_3$), three inductors ($L_1$, $L_2$ and L) and capacitors $C_1$, $C_2$ with a coupling capacitor C. In the input side a photovoltaic cell of 3 watt power and a lead battery with voltage of 12 volts is applied. The developed circuit behaves as a dual input single output converter.

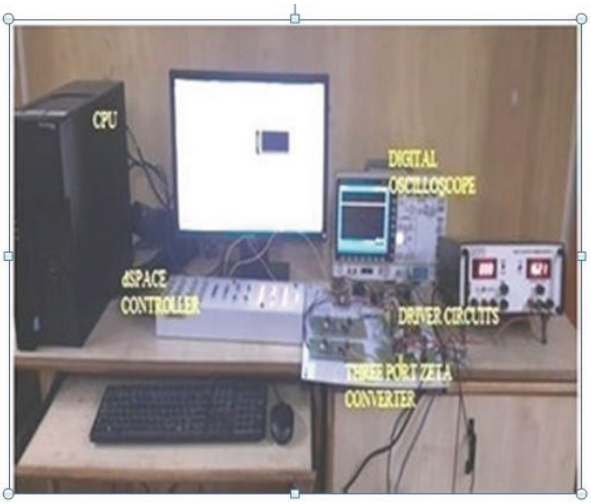


**Figure18b:** Zeta-Zeta Hardware Interfaced with dSPACE Controller

Here dSPACE controller DS1104 is employed as real time controller to interface the hardware with the software based modeling framework in MATLAB SIMULINK. It is a real time processor with comprehensive I/O, on a single board. Using MATLAB in dSPACE control desk, the PWM pulses are generated. The digital signal is converted to analog signal through D/A converter within the controller. These PWM pulses help in driving the three MOSFET switches IRFP450. The response of the real time system was observed to verify the designed converter topology. By varying the duty ratios of both switches, the amount of power drawn from each source could be varied. The switches are triggered by applying suitable gate pulses.

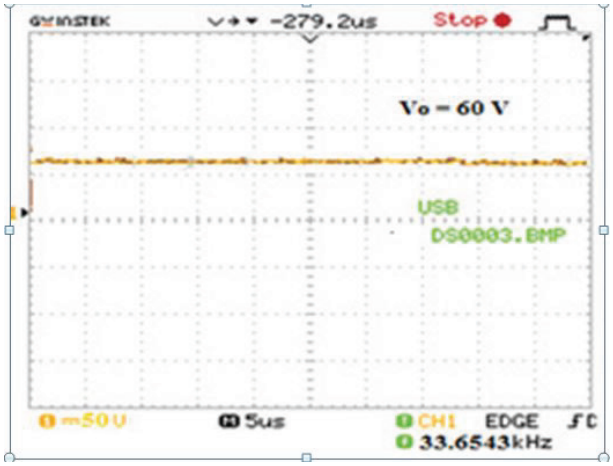


**Figure 19:** Output Voltage of the hardware prototype. (y –axis: 1div = 50V)

Input voltages of 20 V with 30% and 50% duty cycles were fed to the converter. An output voltage, $V_O$ = 60V and output current of 6A were obtained with load resistance of 10 Ω as shown in Figure 19. From the Figure, it is evident that the proposed three port zeta converter does not lose the advantages of conventional zeta converter such as low output voltage ripple.

The reverse charging property of the input ports can also be shown if one of the input sources is a battery. The input source which is a rectified dc supply can be replaced by a battery. This can be used in battery charging applications.

**Table 4:** Major specifications of the prototype

| SI.NO | PARAMETERS | VALUES |
|---|---|---|
| 1 | V mp | 14 V |
| 2 | I mp | 6 A |
| 3 | V oc | 17.5 V |
| 4 | I sc | 6.67 A |
| 5 | min Input Voltage | 20 V |
| 6 | min Battery Voltage | 12 V |
| 7 | Max Load Resistance | 50 Ω |
| 8 | Inductances, $L_1$, $L_2$ | 33 m H |
| 9 | Capacitances, $C_1$, $C_2$ | 100 µF |
| 10 | Max Output Voltage | 110 V |
| 11 | Output Current | 6.4 A |
| 12 | Max Output Power | 450 W |
| 13 | Max Efficiency | 96% |
| 14 | Switching Frequency | 38 kHz |
| 15 | Filter inductor | 1000 µH |
| 16 | Filter capacitor | 140 µF |

The PV cell structure has been designed in accordance with the proposed dc-dc converter. The input and output voltage values, for a particular duty cycle is shown in Table 4.

The waveforms of the inductor current across inductor $L_1$ is shown in Figure 20a and Figure 20 b. The inductor current waveform provides continuous conduction mode of operation.

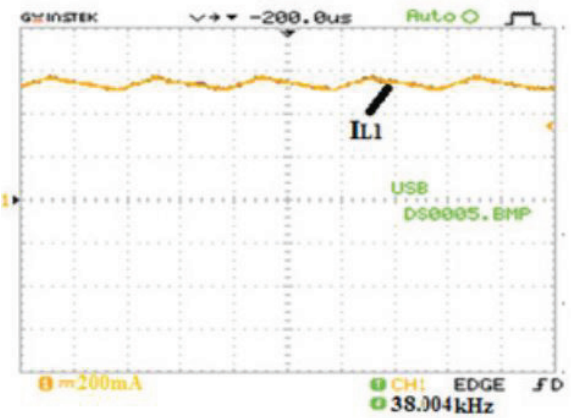


**Figure 20a:** Waveform for Inductor current ($I_{L1}$)

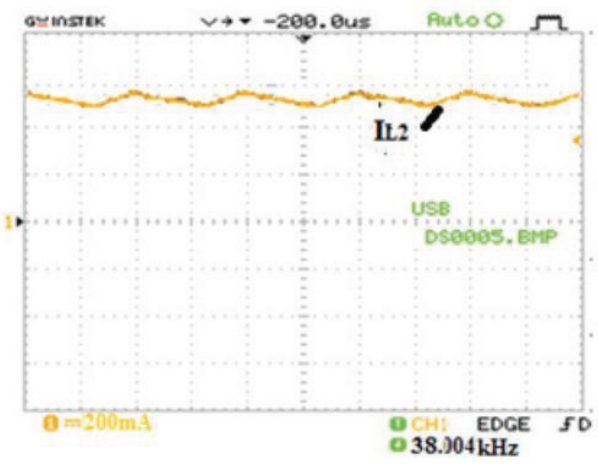


**Figure 20b**: Waveform for Inductor current ($I_{L2}$)

Figure 21.a and Figure 21.b depicts the voltage waveforms across the switches $S_1$ and $S_2$ respectively.


**Figure 21 a:** Voltage across Switch $S_1$

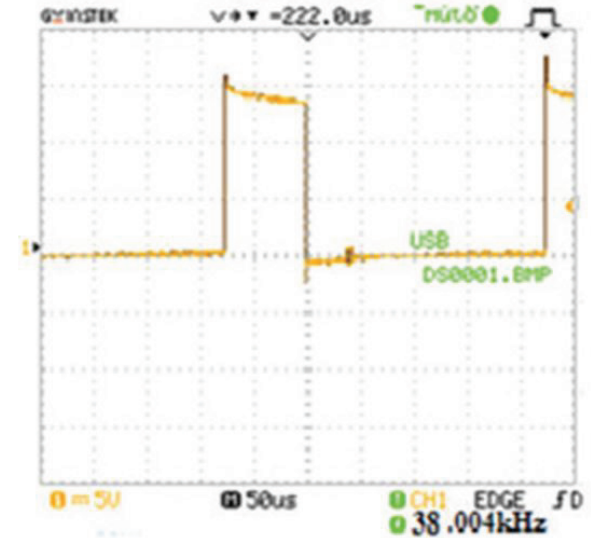


**Figure 21b:** Voltage across Switch $S_2$.

Two separate sources with varying power sharing capability could be interfaced using the proposed converter with a common load.

For obtaining proper control on battery charging, a bidirectional switch could be implemented in one port. The charging current of the battery could be adjusted with a control algorithm. When pulses are simultaneously given to both switches, power is drawn equally from both sources. This proves the validity of our circuit. This makes the topology applicable in hybrid systems. In the case of a hybrid system, the maximum power tracking from the sources could be controlled individually independent of the other source.

The practical values of ripple currents and ripple voltages have been calculated as follows:

The output voltage ripple, $\Delta V_o$ = 60.724 - 60.715 = 9mV and the output ripple current, $\Delta I_o$ = 1.08415-1.08435 = 0.2mA. This low output voltage ripple makes it well suitable for dc load applications such as biomedical instruments, LED lightings etc. that require low ripple input voltage.

### *4.4. Comparative Evaluation*

The implemented hardware of zeta-zeta multiport converter was operated with varying load resistances fed with input source $V_1$ and battery voltage E. The efficiency, voltage gain and regulation of the converter were determined and compared with existing conventional converters.

#### *4.4.1 Efficiency*

The main causes of power dissipation in any dc-dc converter are due to the conduction losses in the inductors and switching and conduction losses present in the switches and diodes in the converter.

$$P_{SWITCH} + P_{DIODE} + P_{INDUCTOR} + P_{OUT} = P_{IN} \quad (30)$$

Since the converter is operating in continuous conduction mode, the inductor current ripple is fairly small, compared to the other dc losses in the converter. Hence considering those losses alone, the operating efficiency, ή for varied output power is determined for the multiport converter.

$$\acute{\eta} = \frac{P_{OUT}}{P_{OUT} + P_{LOSSES}} \quad (31)$$

The efficiency curve shown in Figure 22 depicts that maximum efficiency of the proposed converter is obtained around 335W with input voltages $V_1$ and E both being supplied. The efficiency curve of the proposed three port zeta-zeta converter was compared with the

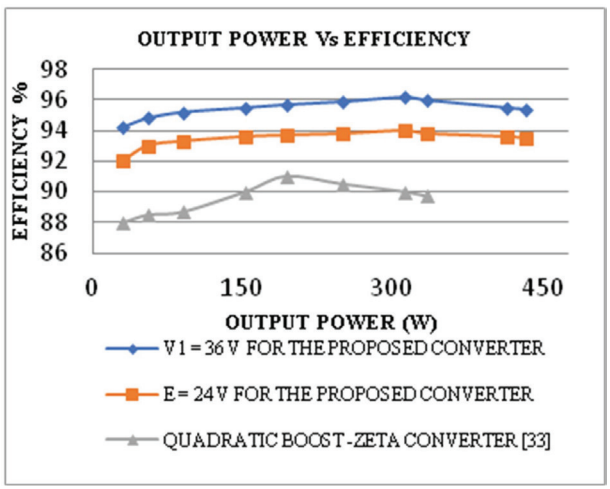


**Figure 22:** Output power Vs Efficiency curve

quadratic boost-zeta converter [33] with an input voltage of 24V.The proposed converter has proved to show an efficiency of 96.2% higher than the conventional converter.

*4.4.2. Voltage gain*

The voltage gain of the converter (equation 10) with voltages $V_1$ and $V_2$ of topology 1 has been determined by varying the duty cycles. The voltage gain curve plotted for the proposed zeta-zeta converter has been shown below.

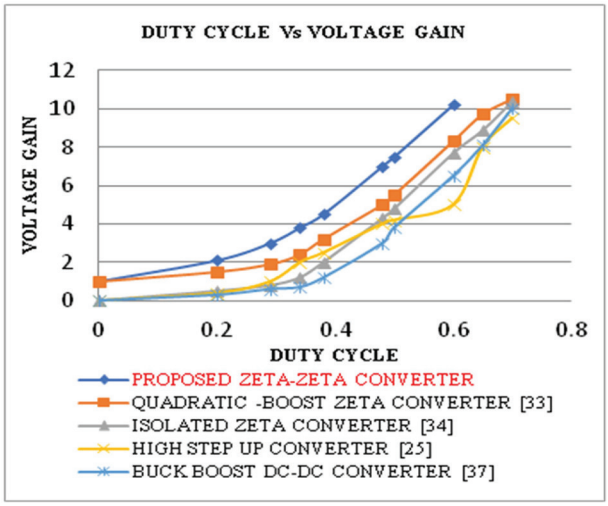


**Figure 23:** Duty cycle Vs Voltage gain-Comparison of different converters

The voltage gain curve of the proposed zeta-zeta converter was compared with the existing quadratic boost–zeta multiport converter [33], an isolated zeta converter [34], high step up converter [25] and buck boost dc-dc converter [37] as shown in Figure 23. From the comparison plots, it is visible that high voltage gain is obtained at 50% duty cycle, from the proposed zeta-zeta multiport converter. Whereas the voltage gain for the other conventional converters are slightly lesser than the proposed converter shown in this paper. This shows that the three-port zeta-zeta converter has high voltage gain at lower duty cycle.

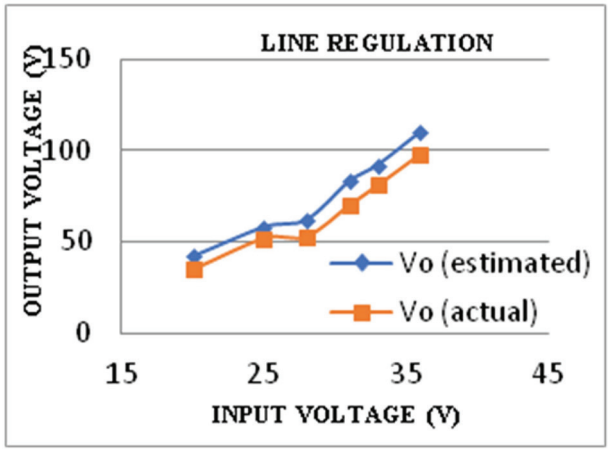


**Figure 24:** Line regulation curve-comparison of estimated and actual values

*4.4.3 Line regulation and Load regulation*

The power supply regulation is another vital factor to consider in the design of a dc-dc converter. The proposed multiport converter is supposed to maintain a

constant output voltage for variable load conditions. The regulation curves were plotted and the actual and estimated values are compared. For varying input voltages, the output voltages (Table 2) were compared with the hardware prototype and the line regulation curves were plotted. Figure 24 shows the line regulation curve that was plotted by maintaining the output current constant and compared with the estimated output voltage.

By maintaining a constant input voltage, the output currents were varied by changing the load and the corresponding output voltages were measured. Figure 25 shows the load regulation curves that compare the calculated and estimated values.

When the converter is applied to a load, where a constant output voltage is required, there might be conditions wherein some sudden variations in load occur. But even then, the converter output must cast a constant output voltage. The load regulation curve proves to show constant output voltage.

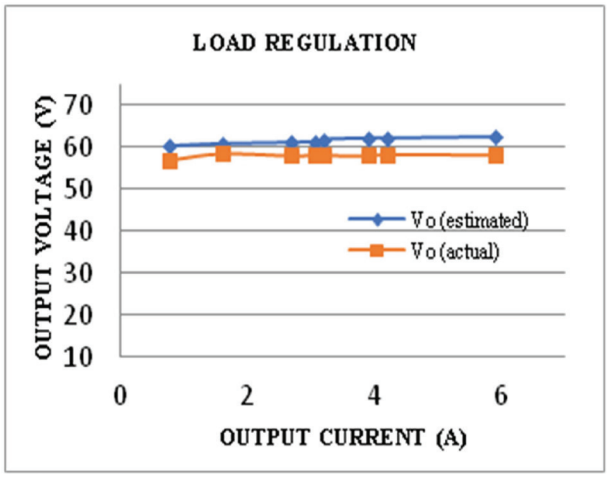


**Figure 25:** Load regulation curve – comparison of estimated and actual values

*4.4.4 Voltage Stress*

The voltage stresses across semiconductor devices occur during the transition period and when the device is reverse biased. It depends on the applied worse case voltage and the rating of the semiconductor device.

The voltage stress across the switch $V_{SW}$, for the proposed three port converter is determined as,

$$V_{SW} = \left( \frac{V_O}{(1+D)} \right) \tag{32}$$

The peak switching current stress is approximately the reversal ratio of the resistance of the load.

$$I_{Sp} = I_O \left( \frac{1}{1-D} \right) + \left( \frac{RD}{2Lf(1+D)} \right) \tag{33}$$

where $I_{SP}$ is the peak switching current of the switch.

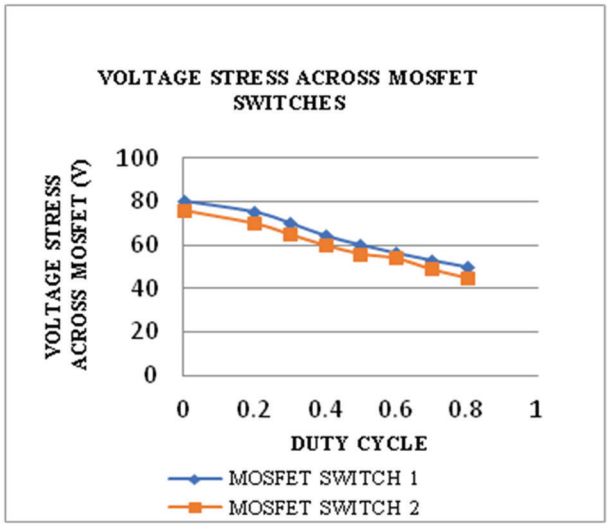


**Figure 26:** Variation of voltage stress across switches Vs duty cycle.

Figure 26 shows the comparison graph of voltage stress across MOSFET switches $S_1$ and $S_2$ with variations in duty cycle. During the turn on and turn off of the switches of both topologies, there occurs voltage stress across the switches. As the duty cycle given to the switches increases, the voltage stress curve steeps down wherein the steep is very lesser in a conventional buck boost converter.

Thus the comparison graphs of varied parameters such as efficiency, voltage gain, line regulation and load regulation curves have been illustrated above to prove the versatility of the designed three port zeta converter.

## 5 Discussion

The utilization of renewable energy persuades the development of new dc-dc converters. In particular, usage of more than one renewable source at the same time has led to the invention of multiport converters. The proposed zeta-zeta multiport converter is a multi input single output converter operable in unidirectional and bidirectional modes. The converter has been analyzed and designed to meet the load criteria. Simulated and hardware outputs have been shown. With input voltages of 20V, the converter delivers output voltage of 60V and output current of 6.29A. The converter provides a very low output voltage ripple of 0.5 mV.

The efficiency curve has been plotted and compared with an existing converter. It shows higher efficiency. The converter proves to show high voltage gain for the same values of duty cycle when compared with other existing converters for which plots have been shown. The voltage conversion ratio is 10.1 at 60% duty cycle, whereas the other conventional converters that were compared shows higher gain at higher percentage of duty cycles only. The converter is proficient to deliver a wide range of output power from 20W- 450W. The estimated and actual values of output voltages and currents have been depicted through regulation characteristic curves. This multiport converter proves that renewable energy can be imparted and maximum utility of the converter can be obtained to obtain uninterrupted power supply. Focusing on the current electrical power issue scenario, the proposed converter is highly feasible for renewable energy applications.

## 6 Conclusion

A non-isolated three port zeta converter proposed in this work facilitates the inclusion of additional sources due to its inherent multiport topology. The proposed three port zeta converter holds PV sources and battery as its essential embodiments. The control approach that has been discussed, has elaborated the versatility of the work with different constraints. The circuit has been simulated in MATLAB Simulink. A prototype of the multiport zeta converter with the real time dSPACE controller has been implemented and their experimental results have been discussed. The steady state analysis and the results reveal the effectiveness of the proposed system for various cases. Even for a low voltage input, the converter is capable of giving a large output voltage. Efficiency, voltage gain, current and voltage ripples and switch voltage stress have been determined. This converter with high voltage gain and low output voltage ripple complements for biomedical instruments and LED lighting purposes that require input voltages with less ripples. The proposed non isolated multiport converter thus finds the optimum way of utilizing renewable energy sources.

## 7 Conflict of interest

The authors declare that there exists no conflict of interest with any third parties. There is no role for sponsors or any funding agency in this research work.

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Arrived: 24. 07. 2020
Accepted: 22. 10. 2020

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**Informacije MIDEM**
*Journal of Microelectronics, Electronic Components and Materials*
ISSN 0352-9045

*Publisher* / Založnik:
*MIDEM Society* / Društvo MIDEM
*Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia*
Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, Ljubljana, Slovenija

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