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Ultra Low-Power Low-Complexity Tunable 3–10 GHz IR-UWB Pulse Generator

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Abstract: A new very low power impulse radio ultra-wideband (IR-UWB) pulse generator is investigated in the paper. The low complexity and tunable architecture is composed of a glitch generator, a switched ring oscillator, a two-stage energy efficient buffer and a pulse shaping filter (two versions). It is designed and simulated in low-cost 0.18 µm UMC CMOS technology. Post-layout simulation results showed spectrum that covers whole UWB band and fully complies with the corresponding FCC spectral mask. The pulse duration is around 0.5 ns, and the peak-to-peak amplitude is 211 mV on 50 Ω output load. Since the impulse radio-based generator operates in burst mode with low duty cycle, it has ultra low power consumption of 0.89 mW corresponding to energy consumption of 8.9 pJ per pulse for 100 MHz pulse repetition frequency (PRF). For the output filter with additional off-chip inductor and PRF of 200 MHz, Power Spectral Density reaches the maximum value of –41.33 dBm/MHz at 6.4 GHz, consuming average power of 2 mW. The peak-to-peak amplitude in this case is 250 mV with pulse duration of around 0.75 ns. The chip occupies very small area of only 558 × 556 µm^2 mainly due to simple pulse generator architecture.

Key words: CMOS technology, impulse radio ultra-wideband (IR-UWB) communications, pulse generator, radio frequency integrated circuits (RFIC), ultra-wideband systems.

Enostaven in spremenljiv 3–10 GHz IR-UWB pulzni generator nizke moči

Povzetek: V članku je obravnavan ultra-širokopasovni (IR-UWB) pulzni generator z impulzi zelo nizkih moči. Enostavno in spremenljivo arhitekturo sestavljajo generator motečih impulzov, preklopni zankasti oscilator, dvostopenjski energijsko učinkovit ojačevalnik in filter za oblikovanje impulzov (v dveh različicah). Načrtovan in simuliran je na nizkocenovni 0.18 µm UMC CMOS tehnologiji. Rezultati simulacij so prikazali spekter, ki pokriva celotno nizko UWB območje in popolnoma ustreza ustrezni FCC maski. Dolžina impulza je okoli 0.5 ns z vrh-vrh amplitudo 211 mV pri 50 Ω bremenu. Kljub kontinuitetnemu delovanju generator izkazuje zelo nizko porabo 0.89 mW, kar ustreza porabi energije 8.9 pJ na impulz pri ponavljajoči frekvenci (PRF) 100 MHz. Pri 200 MHz spektralna gostota moči doseže maksimum -41.33 dBm/MHz pri 6.4 GHz in porabi 2 mW. V tem primeru je vrh-vrh amplituda 250 mV in dolžina impulza 0.75 ns. Čip zaseda le 558 x 556 µm^2 prostora, kar je posledica enostavne arhitekture pulznega generatorja

Ključne besede: CMOS tehnologija, pulzna radio ultra-širokopasovna (IR-UWB) komunikacija, pulzni generator, integrirano vezje radijskih frekvenc (RFIC), ultra-širokopasovni sistemi.

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1. Introduction

Since the Federal Communications Commission (FCC) allocated the 3.1 – 10.6 GHz unlicensed spectrum for commercial ultra wideband (UWB) application in February 2002, several technologies have been developed to satisfy the communication market requirements [1]. Multiband orthogonal frequency division multiplexing (MB-OFDM) UWB and direct-sequence (DS) UWB protocols are mainly focused on the high data rate communications such as streaming multimedia applications. However, these techniques do not utilize efficiently the whole UWB frequency range (3.1 – 10.6 GHz) because they divide it into several sub-bands/channels in system design [2], [3]. This reduces the data throughput capacity and demands complex digital-signal processing, modulation and deep compression for achieving necessary data rate. As the carrier-based transmission approaches require mixers and power amplifiers (usually noisy, power hungry and complex blocks), such UWB

transceivers apparently increase the complexity, power and costs of the UWB chip. Impulse Radio Ultra Wide Band (IR-UWB) technique is a carrier-less approach that transmits extremely short pulses (pulse duration is less than 1 ns) occupying the full UWB frequency spectrum. It has advantageous features such as low complexity (without mixer and power amplifier), low-cost and energy efficient UWB transmitter architecture allowing simple modulation scheme (e.g. on-off keying – OOK). Additionally, the protocol offers high fading margin for communication systems in multipath environments [4]. The IR-UWB appears to be good candidate for very high data rate short-range communication, and low data rate communication related to localization or/and positioning systems [5], [6]. Nowadays, it is mostly used in the IEEE 802.15.3a high data rate and IEEE 802.15.4a low data rate standards, sensor networks, tag networks and biomedical applications.

A pulse generator plays the core role in an IR-UWB system design because it produces pulse train which spectrum, with sufficient power level, has to satisfy all FCC requirements. Therefore, it is extremely challenging to design UWB transmitter that satisfies such difficult demands while achieving low-power and high-throughput operation to enable low-cost systems. Recently reported UWB pulse generators have generally used all-digital [7 – 9], analogue-digital [10] or all-analogue [10], [11] design approach. Digital solutions offer higher integration, lower power consumption and better controllability whereas all-analogue techniques demonstrate circuit simplicity. In some cases, the all-digital architectures require power amplifier (PA) at the output to provide sufficient signal strength increasing the total power consumption and further degrading system complexity by introducing additional PA design constraints. The analogue designs that generate the UWB pulses by LC resonant circuits require considerable die area, making these architectures less suitable for area constrained applications. The slow transient response of the pulsed LC oscillators restricts the bandwidth and the pulse amplitude, as the oscillation is not able to settle sufficiently in a short time.

In this paper, a new low-power and low-complexity pulse generator, addressing the whole FCC spectrum band, is proposed. The presented topology, designed in low cost 0.18 μm UMC CMOS technology, is analyzed in Section III. Due to not high enough speed of CMOS inverters available in the used technology, it was necessary to increase the ring oscillator frequency by introducing negative feedback in each inverter stage. One of them was chosen even to be variable to provide adjustment of the output signal central frequency. Post-layout simulations results are given in Section IV followed by discussion and comparison with the other published pulse generator designs. The Section V concludes the paper.

2. FCC spectral mask and UWB pulse design

The UWB transmitter power level in the FCC allocated frequency range (3.1 – 10.6 GHz) should be lower than –41.3 dBm/MHz [1], in order not to interfere with the already existing communication systems such as WiMax, Bluetooth and GSM. In the GPS band (0.96 – 1.61 GHz), there is even more stringent regulation: less than –75.3 dBm/MHz is needed to avoid interference problem. The Power Spectral Density (PSD) in frequency interval from 1.61 GHz to 3.1 GHz depends on the type of application (indoor, outdoor, GPS, wall & medical imaging, through-wall imaging & surveillance system). Fig. 1 shows the FCC mask for the indoor and outdoor UWB communications (including the Part 15 limit) [1] that pulse spectrum has to meet.

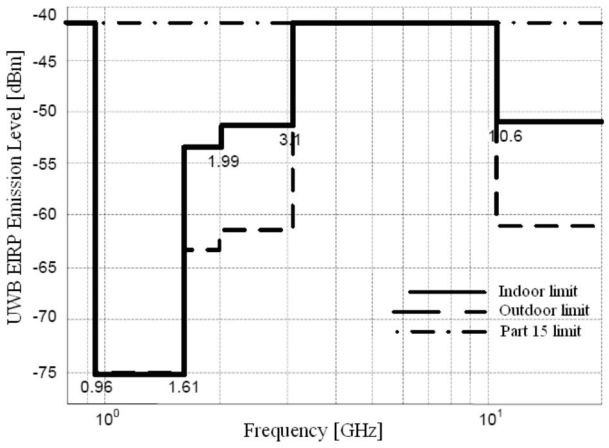

Figure 1: The FCC indoor and outdoor mask for UWB [1].

The FCC rules define only the frequency bands and the radiated PSD but there are no requirements on the time-domain wave shape. However, as the shape of the pulse generator signal determines its spectrum characteristic and effectively dictates specific system (UWB transmitter) requirements, its generation is one of the essential considerations in the UWB design. Pulse shapes usually used in the impulse radio UWB technology are based on the Gaussian pulse and its derivatives. For indoor systems, the 5th or higher order derivative of the Gaussian pulse should be used to comply with the allocated indoor spectrum mask [8].

3. Proposed IR-UWB pulse generator design

The proposed topology is shown in Fig. 2. It is composed of a glitch generator, a switched oscillator, a two-stage buffer, and a pulse shaping filter. Two versions of the output filter (without and with off-chip inductor L_b) are presented in Fig. 3. It should be noted that enhancement-mode transistors have been used in the design.

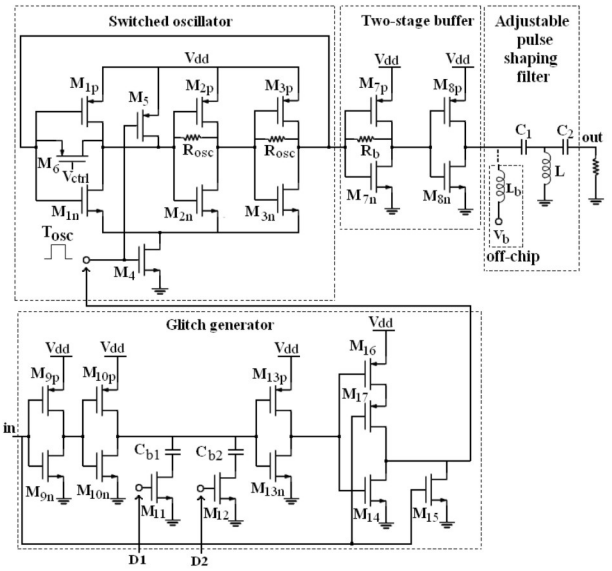

Figure 2: Proposed IR-UWB pulse generator.

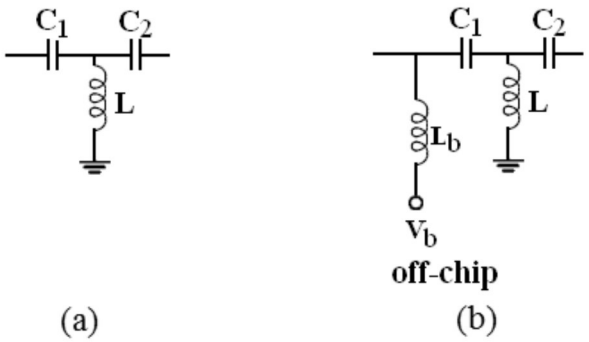

Figure 3: Two versions of pulse shaping filter: (a) without off-chip inductor L_b, and (b) with off-chip inductor L_b.

The switched oscillator consists of a three-stage ring oscillator, (inverter stages M_1 – M_3), two feedback resistors R_{osc}, a control transistor M_6, and a pair of oscillation-enabling switches (transistors M_4 and M_5). The ring oscillator is one of the most commonly used topology in the pulse generator design due to its simple architecture occupying small chip area (without passive components). Furthermore, it offers fast transient response as it has short start-up time and small resistance at each inverter feedback nod. The resistors R_{osc}, feedbacks in the second and third inverter stage, increase the ring oscillating frequency by decreasing the input (Miller) capacitance [12]. PMOS transistor M_6 is used for the frequency tuning to enable compensation due to the process-voltage-temperature (PVT) variations and additional spectrum fitting within the FCC spectral mask [12]. This can be accomplished by changing the transistor M_6 gate control voltage V_{ctrl}.

The oscillation-enabling switches control the oscillation process in accordance with the T_{osc} signal state (produced by the glitch generator). The ring oscillator is turned on by transistor M_4 at the T_{osc} signal rising edge, and the inverter stages output voltage values are determined by the size ratio of the corresponding PMOS and NMOS transistors. The transistor M_4 is switched off and transistor M_5 is switched on while the T_{osc} signal is "low". During this interval, the inverter stages are turned off, while the transistors M_6 (operating in linear region) and M_5 connect the ring oscillator output (the buffer input) to supply voltage. The exact voltage value of the nod (1.6 V) is determined by the voltage divider consisting of four resistors in series: resistor R_b and channel resistances of transistors $M_{5,}$ $M_{6,}$ and M_{7n}. This results in negligible power consumption of the first buffer stage having output voltage close to zero. As M_{8n} transistor is turned off, the power consumption of the second buffer stage can also be neglected minimizing the total power consumption. Since the M_1 transistor output (the M_2 transistor input) is connected to V_{dd} by the transistor M_5, at the next rising edge of the T_{osc} signal the oscillation starts from the same initial state.

It can be noticed that the ring oscillator output signal length and thus its bandwidth are approximately defined by the duration of the T_{osc} signal. The shorter the control impulse, the wider the output signal bandwidth is obtained. To cover the whole FCC frequency range (3.1 GHz – 10.6 GHz), the T_{osc} signal should be short and narrow (duration less than 1 ns). As a microcontroller could not produce such a short signal, the oscillation-enabling pulse is created by the glitch generator considering the input trigger *in* signal usually controlled by a microcontroller. The glitch generator consists of three inverters, a digitally controlled capacitor bank and a NOR gate. The duration of the generated signal is determined by the digitally controlled capacitor bank, composed of capacitors C_{b1} and C_{b2}, and transistor switches M_{11} and M_{12}. To provide sharp both rising and falling edge of produced signal, the capacitor bank was introduced between the inverter stages. Digital signals D_1 and D_2 switch off/on adequate capacitors determining the total bank capacitance that is directly proportional to the T_{osc} signal duration. This provides indirectly control of the pulse generator output signal

length and bandwidth. By the bank capacitance digitally tuning, the duration of the control signal can be adjusted from 250 ps to 660 ps.

The two-stage buffer isolates the ring oscillator from the high-pass filter load (the inductor L and two capacitors C_1 and C_2, Fig. 3a) and improves the pulse generator current driving capability. The first buffer stage has small gain and low input impedance due to resistive feedback used to increase the ring oscillator frequency. The second stage prevents this effect to change the output filter shaping characteristics and simultaneously amplifies the signal. Although the buffer seems to be some kind of output power amplifier, it does not endanger the IC design requirements as it occupies very small area and has negligible power consumption. The off-chip inductor L_b connected to constant voltage (the second type of the output filter presented in Fig. 3b) is used only in case better suppression at low frequencies is required. For its realization, a bond-wire can be used. It can be noticed that this inductor could be integrated on chip to create the on-chip band-pass filter, but this would increase the die-area and thus the fabrication costs.

4. Post-layout simulation results and comparison

The proposed topology has been designed in mixed mode/RF UMC 0.18 µm CMOS technology with supply voltage of 1.8 V. Simulations have been performed using SpectreRF Simulator from Cadence Design Environment. It should be emphasized that this software is one of the most commonly used for IC design. In order to perform post-layout simulations, the Assura (Cadence parasitic extractions) tool has been used. Furthermore, the obtained results have been checked with Calibre (Mentor Graphics) tool as well.

Since one of the portable system's biggest issues is battery life, the pulse generator was optimized with the main aim to minimize the power consumption and meet efficiently the FCC spectrum demands while still keeping acceptable values for remaining Figures of Merits (FOMs). Regarding the circuit's spectrum characteristics or the spectrum center frequency, the main problem was limited set of transistor sizes available in the used technology as the ring oscillator frequency depends directly on transistors sizes. The period of the oscillation T rises proportionally with increase in transistors sizes, while the oscillating frequency decreases (f_0=1/T). For the standard three-stage ring oscillator design with the smallest NMOS transistors (W/L= 25 µm/0.18 µm) and approximately two times larger PMOS transistors (W/L= 45 µm/0.18 µm), the oscillation frequency of 3.77 GHz has been obtained. Although the resistive feedbacks have been used in the ring oscillator and the first buffer stage to increase the oscillating frequency, its value has not been large enough to utilize efficiently the whole UWB band in the spectrum domain. Therefore, a new approach of the pulse generation is proposed to overcome the technology constraint. The output high-pass filter frequency has been chosen to have around two times higher value than the ring oscillating frequency and the signal with the spectrum center frequency (6.25 GHz) in the middle of the UWB range has been obtained (shown in Fig. 4). It can be seen that spectrum covers the whole UWB frequency band and fully complies with the FCC spectral mask. The post-layout simulation results for the generated UWB pulse in the time domain is given in Fig. 5. The pulse duration is around 0.5 ns and the peak-to-peak amplitude V_{pp} on a 50 Ω output load is 211 mV. The pulse generator operates in burst mode with low duty cycle and pulse repetition frequency (PRF) of 100 MHz, and thus has very low power dissipation. The average power consumption including the glitch generator, the buffer stages and the filter is only 0.89 mW, corresponding to 8.9 pJ energy consumption per pulse (for the PRF of 100 MHz). In general, the nature of the IR-UWB communication allows saving power between every two adjacent pulses and consuming power just at the moment when the pulse is generated.

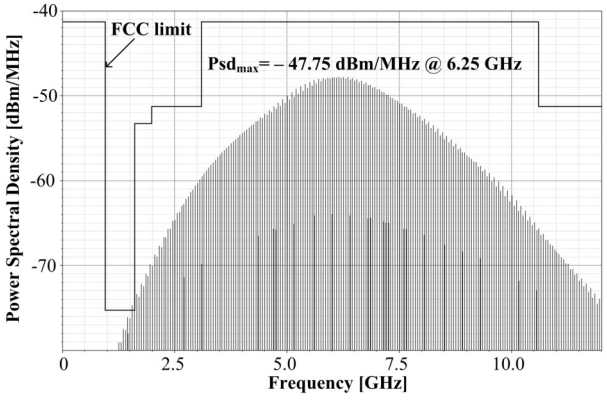

Figure 4: Post-layout simulations of the output signal in the spectral domain.

The circuit components values and transistors sizes are given in Table 1 and 2, respectively. The transistors channel length, fixed by the manufacturing process, is 0.18 µm.

Since transistors are made as multi-finger devices, the total transistors gate width is calculated by W= ng·5 µm, where 5 µm represents the gate finger width, and parameter ng, the gate finger number, is in the range from 5 to 21. Additional technology recommendation

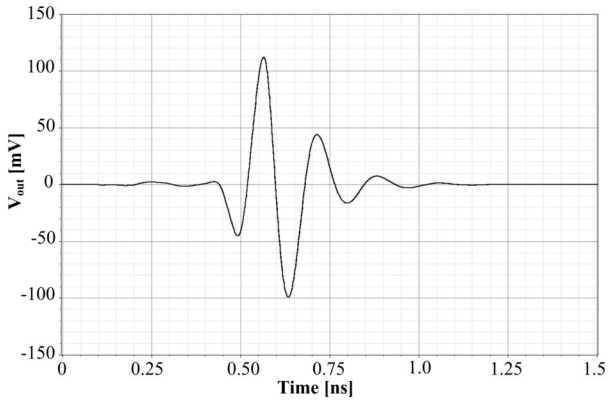

Figure 5: Post-layout simulation of the output signal in the time domain.

of 558 × 556 μm² including bonding pads, and the active circuit area is only 352 × 378 μm². It supports the on-off keying (OOK) modulation. This type of the modulation is chosen because of its simplicity and thus less complex transmitter realization.

It can be seen from Fig. 4 that the pulse generator PSD must be lower than the maximum value allowed by the FCC due to very large bandwidth to avoid emission in the forbidden frequency band around 1 GHz. Moreover, even wider bandwidth can be achieved with smaller value of bank capacitance in the glitch generator, but the lower part of the FCC mask would be slightly unsatisfied. To overcome the problem of emission at frequencies around 1 GHz, the off-chip inductor L_b is added in

Table 1: Values of the circuit components.

Component	Rosc	Rb	C1	C2	L	Cb1	Cb2
Value	530 Ω	1500 Ω	0.20 pF	0.13 pF	1.6 nH	1 pF	2 pF

Table 2: Transistors sizes.

Transistor	M1-3n	M1-3p	M4	M5	M6	M7,8n	M7,8p	M9,10n	M9,10p	M11	M12	M13n,p	M14,15	M16,17
Width [μm]	25	45	105	35	25	25	45	25	25	75	95	25	25	75

is to use only odd values for parameter *ng*. It can be noticed that transistor M_6 has the largest size because it has to provide enough current for the three-stage ring oscillator.

The photograph of the pulse generator layout is shown in Fig. 6. The integrated circuit (IC) occupies a die area

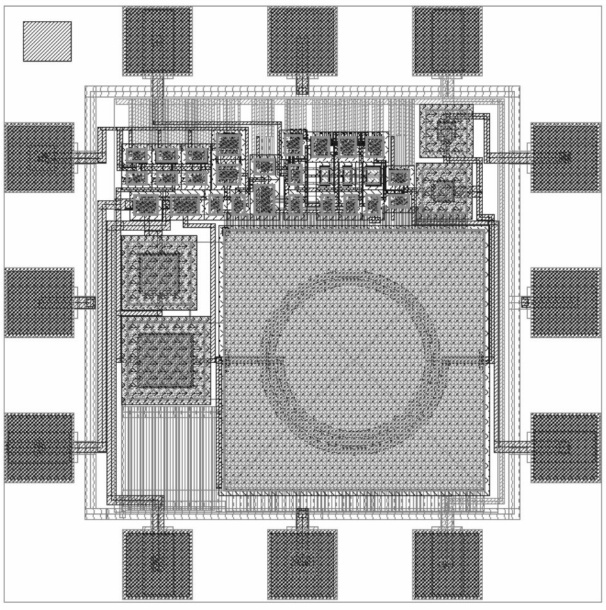

Figure 6: Photograph of the IR-UWB pulse generator layout.

the output filter (Fig. 3b, or shown with dashed line in Fig. 2). The post-layout simulation results (in time and spectrum domain) for L_b = 2.3 nH and V_b = 0.25 mV are shown in Figs. 7 and 8. It can be observed that the signal spectrum is significantly improved (flatter response and higher 10 dBm bandwidth have been obtained). Furthermore, the spectrum components at lower frequencies close to the most critical band around 1 GHz are suppressed as expected. The pulse duration is about 0.75 ns with the V_{pp} parameter of 248 mV. There was a small increase in the power consumption 1.41 mW (corresponding to energy consumption of 14.1 pJ/pulse). However, this does not represent a problem as the ef-

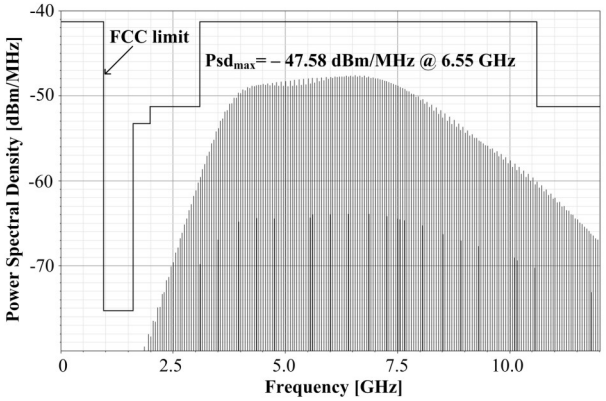

Figure 7: Pulse generator spectrum in the case of the output band-pass filter includes the off-chip inductor L_b.

ficiency remained the same (the total signal power was also increased). Additionally, in the case of the pulse generator signal power around the maximum allowed value is required, the spectrum value can be enlarged by increasing the PRF. The pulse generator PSD for the pulse repetition frequency of 200 MHz is given in Fig. 9. It can be seen that the FCC spectrum mask is fully satisfied with the maximum PSD of –41.33 dBm/MHz at 6.4 GHz. The energy consumption is a little decreased and is around 10 pJ/pulse.

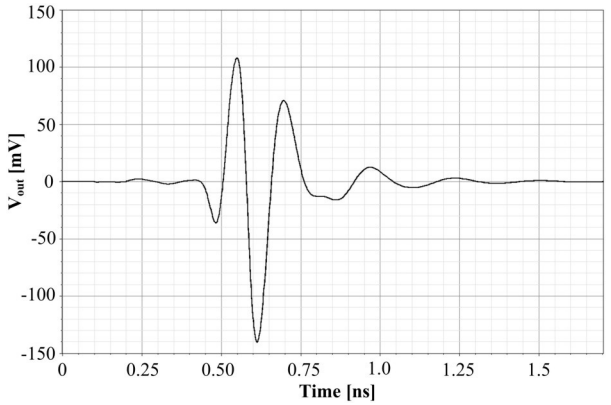

Figure 8: Pulse generator time response in the case of the output band-pass filter includes the off-chip inductor L_b.

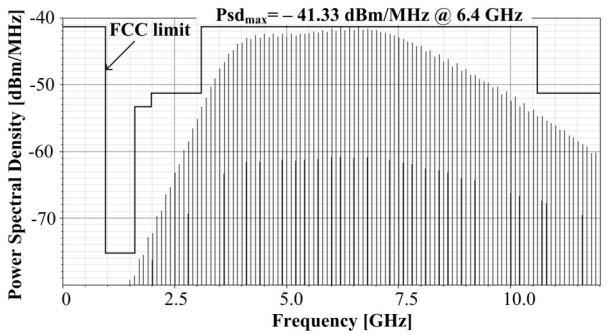

Figure 9: Pulse generator PSD in case *PRF*=200 MHz.

Table 3 summarizes the performance of the proposed IR-UWB pulse generator compared to the FOMs of the recently published works. Although, it can be difficult to make fair comparisons when different specifications and technologies are used, it is clear that the proposed circuit is more efficient than the other design as it has by far the lowest power consumption and the peak-to-peak amplitude higher than in Refs [13], [14], and [15]. The pulse generator presented in Ref [16] has higher V_{pp} parameter, but consumes significantly more power compared to the presented design. Other FOM achieved in the work are comparable to the results given by the authors. The proposed architecture is suitable for low voltage and ultra-low power UWB wireless applications.

5. Conclusion

A new energy-efficient tunable pulse generator is developed in 0.18 µm UMC CMOS technology for high data rate 3.1 – 10.6 GHz UWB applications. The time and spectrum domain signal adjustment is proved by applying the adequate PMOS gate control voltage and tuning capacitance of the digitally controlled capacitor bank. Additional spectrum suppression at lower frequency (especially in the 1 GHz to 1.6 GHz band where tight limits are imposed for GPS systems) is enabled with the off-chip inductor inserted. The post-layout simulation results demonstrate that the proposed ring oscillator-based architecture has significantly lower power consumption compared to the previously reported UWB pulse generators. Moreover, it was shown that the design has high peak-to-peak amplitude and small chip area.

Acknowledgments

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Table 3: Performance comparison of the IR-UWB pulse generators.

Reference	Power cons. [mW]	BW (-10 dB) [GHz]	Vpp [mV]	Pulse width [ns]	Die area [mm2]	PRF [MHz]	Technology
/13/	N/A	3.1 – 10.6	68	0.45	0.27	200	90 nm CMOS
/14/	27.0	3.6 – 10.2	127	0.31	N/A	50	0.18 µm BiCMOS
/15/	3.8	3.0 – 6.0	150	0.5 – 0.9	0.44	910	0.13 µm CMOS
/16/	23.0	N/A	300	0.75	0.50	50	0.18 µm CMOS
This work*	2.0	3.1 – 10.6	250	0.75	0.31	200	0.18 µm CMOS
This work**	0.89	3.3 – 9.3	211	0.50	0.31	100	0.18 µm CMOS

* with the off-chip inductor L_b.
** without the off-chip inductor L_b

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