A/D AND D/A CONVERTERS - BASIC BUILDING BLOCKS FOR TELECOM APPLICATIONS

J. Hauptmann, W. Pribyl
Siemens Entwicklungszentrum für Mikroelektronik Ges.m.b.H, Villach, Austria
J. Sevenhans, Z.-Y. Chang
Alcatel Bell, Antwerpen, Belgium

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Abstract: Emerging telecom systems such as ADSL, VDSL demand state-of-the-art high speed and high resolution A/D and D/A converters. Moreover, cost and power consumption issues require the use of specific A/D and D/A architectures to achieve the wanted resolution at the required speed for the minimum power. In the first part of this paper an overview is given of various A/D and D/A converter architectures used in Alcatel telecom systems over the past 15 years. Emphasis is placed on the evolution of A/D and D/A converters for today's ADSL applications. Then design considerations for high speed and high resolution pipelined A/D converters for future VDSL technology will be addressed.

A/D in D/A pretvorniki - osnovni gradniki telekomunikacijskih vezij

Ključne besede: sistemi telekomunikacijski, polprevodniki, CMOS tehnologije, tehnologije submikronske, IC vezja integrirana, moči napajalne male, ADSL linije naročniške digitalne asimetrične, VDSL linije naročniške digitalne s hitrostjo bitov zelo veliko, A-D pretvorniki analogno-digitalni, D-A pretvorniki digitalno-analogni, ALCATEL družba proizvodna, SIEMENS družba proizvodna

Povzetek: Telekomunikacijski sistemi bližnje prihodnosti, kot so ADSL in VDSL zahtevajo moderne hitre A/D in D/A pretvornike z visoko ločljivostjo. Dodatne zahteve po nizki ceni in porabi narekujejo uporabo posebnih A/D in D/A arhitektur, s katerimi dosegamo željeno ločljivost pri narekovani hitrosti in majhni porabi. V prvem delu tega prispevka podajamo pregled različnih arhitektur A/D in D/A pretvornikov, ki so bili v uporabi zadnjih 15 let v telekomunikacijskih sistemih firme Alcatel. Poseben poudarek smo dali na opisu razvoja A/D in D/A pretvornikov za uporabo v današnjih ADSL sistemih. Prispevek zaključimo z opisom načrtovanja visokoločljivih serijskih A/D pretornikov za bodoče VDSL tehnologije.

1. INTRODUCTION

The telecom exchanges and subscriber lines have gone through an amazing evolution over the past 15 years where A/D and D/A conversions have played an important role. Over the past 15 years telecom switching and subscriber lines have gone from reed relays and transformers to digital switching and semiconductor subscriber line interface circuits (SLIC). The availability of the semiconductor technology has modified the size of a public exchange from a building full of racks to a rack full of ASIC's and the key to this success story of new technology is the CMOS A/D and D/A conversion.

CMOS transistors in A/D and D/A conversion in the late seventies had gate lengths over 5 μm and supply voltages + and -5 V, V_T´s over 1 V, etc. So supply voltage has gone down by a factor of 3 and transistor sizes by a factor of 20 since those days, and both supply voltage and gate length continue to go down hand in hand now. Yes, for the cost, the transistor size has to go further down into very deep submicron, 0.25 micron is almost in production and the ambition of technology research to further reduce the gate length is stronger than ever.

New telecom applications need high resolution, high speed A/D and D/A at very low power consumption. This is what's driving the use of specific A/D and D/A architectures: provide the wanted resolution at the required speed for the minimum power consumption and the minimum silicon cost. To achieve this, circuitry in A/D and D/A has gone through the evolution from single ended to balanced, from vertical cascodes to folded cascodes, from differential input pairs to constant gm complementary inputs. And many architectures have been applied such as successive approximation, full flash, sigma delta, pipelined and etc. Each of these architectures have their specific advantages and drawbacks: a switched capacitor CMOS SD A/D for 4 MHz Nyquist sampling and 12 bit resolution will cost you 0.9 W power consumption /1/, can you afford it on a subscriber line in a low cost rack containing 200 line interfaces? Using a pipelined architecture the power consumption will be an order of magnitude better, but you need a correction algorithm to compensate for the errors in the sub-ADC and a careful circuit and layout design to guarantee the required capacitor matching accuracy in your pipeline.

2. A/D AND D/A CONVERTERS IN TELECOM

Some of the above mentioned A/D and D/A architectures have been applied in telecom applications (see Table 1.). Sometimes for the right reason. For example the use of SD modulators for speech /2/.

Since the early eighties, second order SD modulators are used on analog phonelines for A/D and D/A conversion (Fig. 1,2) for several good reasons. The first reason is the high sampling frequency or the large oversampling ratio (OSR). In the decimator filter this high sampling rate is divided down to the 8 kHz speech sampling and the bit resolution is going from 1 bit to 11...12 bit. The digital decimator filter separates the speech spectrum much more accurate than the analog filters and for less power consumption. The 1 MHz sampling frequency gives us room for a simple anti-aliasing filter, e.g. an RC second order active filter. The integrated R and C are linear enough to meet the 60...70 dB dynamic range and the tolerance on the absolute value is easy because of the high oversampling.

Table 1. A/D and D/A architectures for telecom application

Applic.	Year	Vdd	Techn	SNR	OSR	A/D & D/A Type	P mW
Speech	1980	±5V	5 µ NMOS	8bit A/u	8kHz	Succ appr. A/D A-law/u-law	50mW
	1985	±5V	2,4 µ CMOS	12 bit	1 MHz 128x	2nd order SD A/D	20 mW
	1990	+5V	1,2 µ CMOS	13 bit	2 MHz 256x	2nd order SD A/D	6 mW 4 mW
	1995	-5V	0,7 µ CMOS	14 bit	2 MHz 256x	2nd order SD A/D	5 mW 3 mW
ISDN	1987	+5V	2 µ CMOS	10 bit	16 MHz 128x	2nd order SD A/D	15 mW
	1996	+3V	0,5 µ CMOS	10 bit	8 MHz 64x	4th order SD A/D	35 mW 10 mW
GSM	1990	+5V	1,2/2 µ CMOS	8 bit 8 bit	270 kHz 1x	Suc appro A/D Binary weig D/A	10 mW
	1993	+5V	0,7 µ CMOS	8 bit 8 bit	270 kHz 1x	Sucess appr A/D Binary-weig D/A	10 mW
	1995	+3V	0,5 µ CMOS	13 bit 8 bit	6,5 MHz 24x	4th order SD A/D Binary-weig D/A	14 mW 3mW
ADSL	1993	+5V	0,7 µ CMOS	12 bit	53 MHz 24x	4th order SD A/D	850 mW 700 mW
	1997	+3V	0,5 µ CMOS	12 bit	8.8 MHz 4x	pipelined A/D switched-I D/A	120 mW 30 mW
VDSL	1997 1998	+3V	0,35 µ CMOS	12 bit	40 MHz 1x	pipeline A/D switched-I D/A	250 mW 60 mW

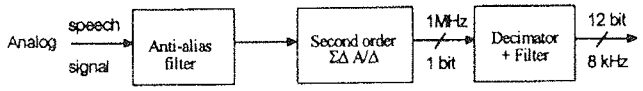

Figure 1. Speech A/D conversion

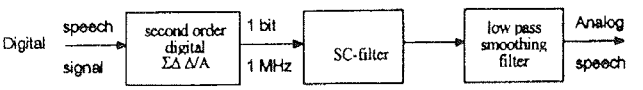

Figure 2. Second generation SD D/A for speech

For speech D/A conversion SD modulator is applied as successfully as for A/D, without a dependancy on clock jitter.

Also in ISDN U-interfaces, SD A/D & D/A conversion are used since 1987 /3/. The 144 kbit/s on the U-interface subscriber line in the 120 kHz 4B3T code or the 80 kHz 2B1Q code were handled by a 16 MHz 1 bit PDM-code. A resistive 3rd order smoothing filter in the transmit path and 1 capacitor C on the resistive echo bridge act as anti-aliasing filter as shown in Fig. 3.

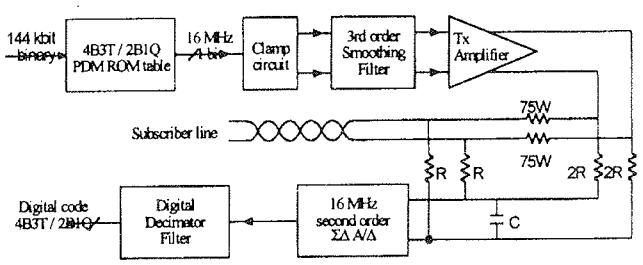

Figure 3. U-interface analog front-end anno 1987

Another strong application for SD A/D is GSM. The use of SD A/D for digital I/Q quadrature mixing is well known /4, 5/, but also in a zero IF receiver the use of SD A/D is very attractive because the high sampling rate offers the necessary bandwidth to pass the adjacent channels and the blocking levels without aliasing them in the band of interest and the decimator filter also performs the channel filtering that was implemented in analog switched capacitor filters in the first generation GSM ASIC's.

In the first generation GSM ASIC's the 8 bit A/D was implemented as a successive approximation algorithm. In fact the transmit D/A was reused in the receivers A/D. The transmitter D/A was realized in switched capacitor circuitry using weighted capacitors in a sign-magnitude algorithm.

A 13 bit SD A/D is now converting the receive I/Q signals from the analog to the digital domain. The extended dynamic range covers for both filtering and offset suppression: 4 bits for wanted signal, 7 bits for the blocking levels and the adjacent channels and 2 bit for the offset. In zero IF a wide dynamic range A/D solves all the worries about self mixing and local oscillator leakage. Every bit additional dynamic range in the A/D allows for a factor of 2 less gain in the analog receiver circuitry, so allowing for a factor of 4 more offset in the zero IF down convertor.

The use of 13 bit SD A/D GSM receivers reduces the amount of analog circuitry in favour of digital filtering. And this is exactly the trend in telecom: less analog, more digital, because analog circuitry is difficult in design at low supply voltage and often requires very expensive analog technologies.

This is the area where switched current circuits have big potential. Switched current second order sigma delta modulators have proven the required performance for speech analog telephone /6/. The switched current technology is available, pioneers have used it and published sufficiently to prove the case /7/ and moreover it reduces the chip costs.

Besides the trend to go to pure digital processes, the supply voltage is also rapidly decreased to minimize power consumption. And precisely the low supply voltage is the reason for needing higher resolution and higher speed A/D and D/A due to less analog filtering and therefore higher unwanted out of band signals.

Conclusion: analog design must focus on A/D and D/A, because the necessary area and power consumption in digital filtering benefits more from the deep submicron technology progress. One of major tasks for analog designers in the coming years is to make A/D and D/A converters for high resolution, high speed, low power and low cost.

3. A/D AND D/A CONVERTERS FOR ADSL

Asymmetrical Digital Subscriber Loop (ADSL) technology makes it possible to transmit high bit rate video signals over the conventional telephone twisted pair copper network. Discrete Multi Tone (DMT) modulation is used to map the high speed digital data (e.g. 6 Mb/s) onto a large number of Quadrature Amplitude modulated (QAM) carriers. The upper frequency band of the DMT analog signal over the twisted pair is 1.1 Mhz. To cope with the copper wire's high attenuation and the large echo return, 12 bit A/D and D/A converters at 2.2 MHz Nyquist rate are required.

In the first and second generation ADSL systems, SD modulators are used to achieve the required resolution in a 0.7 μm CMOS technology. To limit the maximal sampling frequency high order SD modulator architectures are adopted. The ADC is a 4th order SD modulator based on the cascaded approach as shown in Fig. 5.

The main disadvantage of the cascaded topology is its high sensitivity to the non-ideal effects which can result in a large noise leakage. Non-ideal effects include integrator gain errors due to capacitor mismatching, finite dc gain, finite gain-band-width (GBW) and finite slew-rate (SR) of the opamps. These non-ideal effects are analyzed by using time-domain behavioral simulations and FFT analysis.

The D/A converter in the transmit path is a 6th order digital SD modulator using the multiple feedback technique as shown in Fig. 6. Feedback coefficients B0, B1...B5 determine the pole positions of the modulator, while coefficients A0, A1 and A2 realize three transmission zero's in the noise transfer function (NTF) to maximize the peak SNR. These coefficients are determined by the requirements of pole/zero positions, stop band frequency and stop band attenuation. For an oversampling ratio of 32 the stop band frequency of the filter is fixed at $f_S/32$ where f_S = 49.15 Mhz is the oversampling frequency. The stop band attenuation is a trade off between the in band noise and the stability of the modulator. As a compromise, a stop band attenuation of 68dB is chosen yielding a 14.5 bit theoretical resolution. The integrator gain factors are determined by internal scaling to maximize the dynamic range so as to avoid any internal overload.

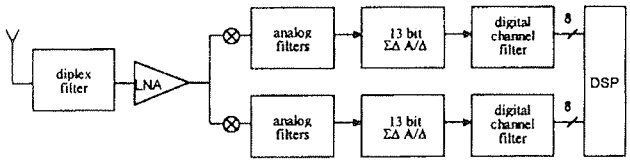

Figure 4. Second generation GSM radio receiver

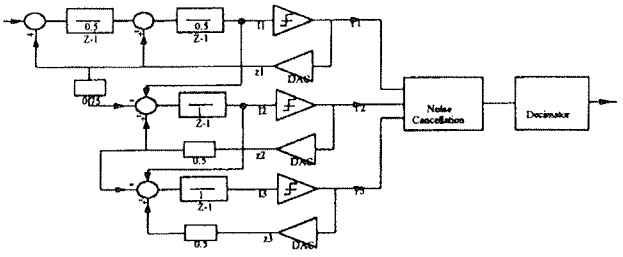

Figure 5. 4th order cascaded SD

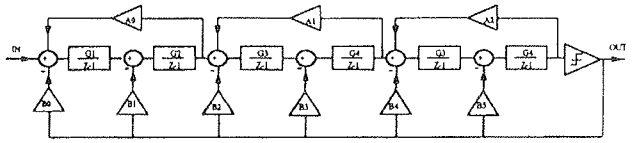

Figure 6. Sixth order SD DAC topology

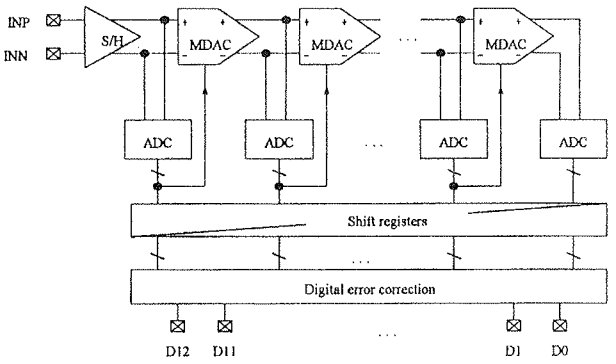

Figure 7. Pipelined ADC for 3rd generation ADSL

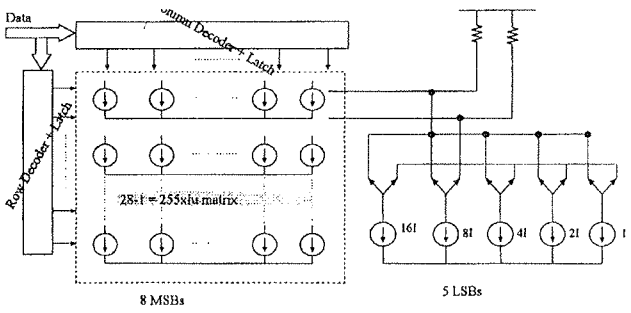

Figure 8. Switched current DAC for 3rd generation ADSL

The PDM output is converted to an analog signal in a first order SC-filter. The total power consumption of the complete SDD/A converter is 140 mA or 0.7 W.

At the moment, the third generation ADSL system is in the development phase. To allow more modem lines in a single rack, power consumption becomes a big issue. For the analog front-end the total power consumption must be reduced from the present 1.9 W to 0.4...0.5 W. This drastic power reduction is realized by using on the one hand a 3 V 0.5 µm CMOS process and low power A/D and D/A converters on the other hand. For the A/D conversion, a CMOS pipelined A/D architecture is chosen as shown in Fig. 7. The converter consists of six stages and each stage resolves two effective bit with one redundant bit for digital correction. The sampling frequency is 8.8 MHz corresponding with an OSR=4 for the ADSL band. The total power consumption including reference buffers is 35 mA which is a factor of five lower than the 4th order SD ADC. However, in contrast to SD ADC, pipelined ADCs require much tougher capacitor matching and careful device level design.

For the D/A conversion, a switched current architecture is adopted as shown in Fig. 8. For the first 8 MSBs a unit current cell matrix approach is used to achieve the best INL(Integral Non-Linearity), while for the last 5 LSBs the binary weighted current cells are used to reduce silicon area. The static accuracy of a switched current DAC is determined by the matching of the current sources in the unit cell matrix. The minimal required current source matching can be derived by the requirement that the INL <1/2LSB as given by:

$$\sigma^2(\Delta I/I) < 1/2^{N+2}$$

For N=12 bit, the required current source matching is s(DI/I) = 0.78% which can easily be realized in modern CMOS technologies. Expression (2) takes only random error effects into account and assumes that the systematic errors are eliminated by good layout techniques and switching sequence. The dynamic performance is determined by the current switch design and switching sequence. For the last 5 LSBs a direct switching method is used, while for the first 8 MSBs digital predecoding is employed and dedicated switching sequence is used to eliminate systematic and gradient errors. The full scale output current is 10 mA which is more than an order of magnitude lower than the SD approach.

4. CONCLUSIONS

In this paper an overview is given of various A/D and D/A converter architectures used in Alcatel and Siemens telecom systems over the past 15 years. Telecom systems are in a continuous evolution over different applications from analog telephony, ISDN, GSM to the most recent ADSL and VDSL. A range of different A/D and D/A converters is in use to cover all those applications. For today's ADSL and VDSL applications pipelined A/D and switched current D/A converters are proposed as the most promising conversion architectures to achieve high speed and high resolution with minimum power consumption.

Acknowledgement

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Joerg Hauptmann and Wolfgang Pribyl
Siemens Entwicklungszentrum für Mikroelektronik Ges.m.b.H,
Siemensstrasse 2, Villach, A 9500
Jan Sevenhans and Zhong-Yuan Chang
Alcatel Bell, Francis Wellesplein 1, B-2018 Antwerp, Belgium

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