A 12-BIT FLASH ADC

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Key words: digital-to-analog, converter, precision, accuracy, INL, DNL, linearity

Abstract: A 12 bit, single step flash digital-to-analog converter (DAC) in 0.6um CMOS was realized on 1.5mm2 silicon area and has power consumption of 0.5mW at 5V supply. Converter architecture based on resistor-string having 2**N resistor taps and layout-efficient coding scheme. The system features a precision, fast settling, offset canceling operational amplifier and has 0.002% linearity. The conversion time is 4us.

12-bitni bliskovni DAC

Ključne besede: digitalno-analogni, pretvornik, precizija, točnost, integralna nelinearnost, diferencialna nelinearnost

Izvleček: Bliskovni digitalno-analogni pretvornik, izdelan v standardni 0.6um tehnologiji CMOS na površini silicija1.5mm2 , ima minimalno porabo 0.5mW. Arhitekturo pretvornika sestavlja uporovna veriga z napetostnimi odcepi in CMOS stikali, ki so krmiljena na način, ki optimizira porabo silicija. Doseženo linearnost pretvornika (0.002%) zagotavlja ustrezno povprečenje, ki minimizira gradient spreminjanja upornosti polisilicija po silicijevi rezini. Z ustrezno optimizacijo internih zaklasnitev je dosežena hitrost pretvorbe 4us.

I. Introduction

The paper will discuss the digital-to-analog converter having the fast conversion time of 4μs at worst-case process. Concept based on resistors matching which guarantee the linearity of monolithic DAC to be in the 9 to 10 bit range. Performances can be extended to more then 12 bits, using so called layout averaging technique, which includes proper interleaving of passive components. Technique will be described in detail later in this paper. The result of such a technique is desensitizing the DAC to doping, thermal and misalignment gradients.

In present paper we will describe the layout efficient architecture of the 12 bit flash DAC with proposed algorithm to extend linearity to 0.003%. We will discuss the basic flash system, followed by section with detail description of the DAC converter blocks, DAC converter operational amplifier and the concept for offset compensation. The layout averaging and gradient-over-silicon analysis using Matlab and in final section the measurement and performances will be presented.

II. Basic Flash DAC

A single step flash DAC converter , based on resistive chain and digitally controlled switches are shown from Fig. 1. The input digital code is converted to switch-control signals. Only one switch is close at a time. Resistor-chain is supplied from constant, temperature and supply stable reference voltage. Ideally, here are only two current contacts - on bottom and on top of the chain where the voltage reference is connected. There are 2**N taps which are voltage contacts to switches and no current flows through them. The large number of switches with their parasitic capacitance loaded the sensitive - internal analog line. The resistance of the chain, the parasitic capacitance, switch resistance and internal - analog line (IVA) parasitic have influence on converter settling performances and therefore conversion time.

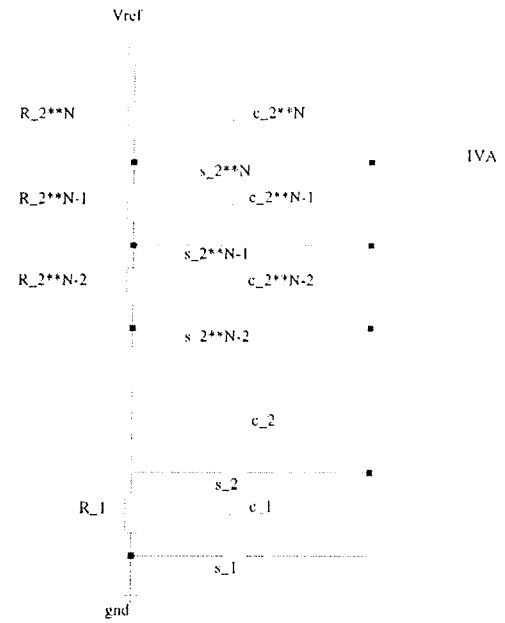

Fig. 1 DAC12 basic architecture.

It is therefore important to make the resistance small enough to speed up the conversion. Lower chain resistivity requires larger driving capability of the voltage reference. The optimum exists between switch resistance, chain resistance and capacitance. To reduce the number of switches, connected to the IVA, the so called tree-decoding scheme might be a solution. As we will show later in this paper,

the good compromise can be found between layout density and the settling performances. Using additional resistive parallelism, the equalizing of the settling performances over full scale can be achieved.

III. Circuit Realization

A. Layout efficient decoding

The principle is shown from Fig. 2. The 12 input NOR gate is realized by 12 N-channel devices in serial. The P-channel devices are omitted, the single PMOS current generator is used instead. There are 2**N current generators in the circuit, only one delivers current into system at a time. Overall required bias current is therefore single generator current which is in the range of 5uA for 12 bits converter. The complete decoding is optimized to fast controlled of the switch having on IAL side the capacitive loading, including the operational amplifier input capacitance.

The layout concept including four-bit intersection is in Fig. 2. Twenty metal lines (double metal process) passes the N-channel area. One kilo-bit block is organized as binary coded area from 1, 2, 4, and 8 bits sub-blocks inserted into 9-bit converter. Last - 10-th bit select between the two 9-bit converters. To get 12-bit converter, four such a 10-th stages are organized in proper way. Voltage reference was chosen to be 4.1V at 4.5V minimum supply. To minimize the parasitic, the switches are realized from negative reference side to be NMOS only, around mid-area switches are T-gates and on positive-reference side, switches are again single channel-PMOS only.

B. Interleaving and layout averaging

The principle of operation of presented DAC guarantee the monotonisity and therefore the analog output always increasing with increasing of the digital code. No matter how large is poly1 resistivity gradient, It will mainly influence on integral non-linearity (INL) and can be expressed as a difference between actual analog value (Vana_i) and ideal one (Vana_ideal) on internal analog bus (IVA - Fig. 1) and is equal to:

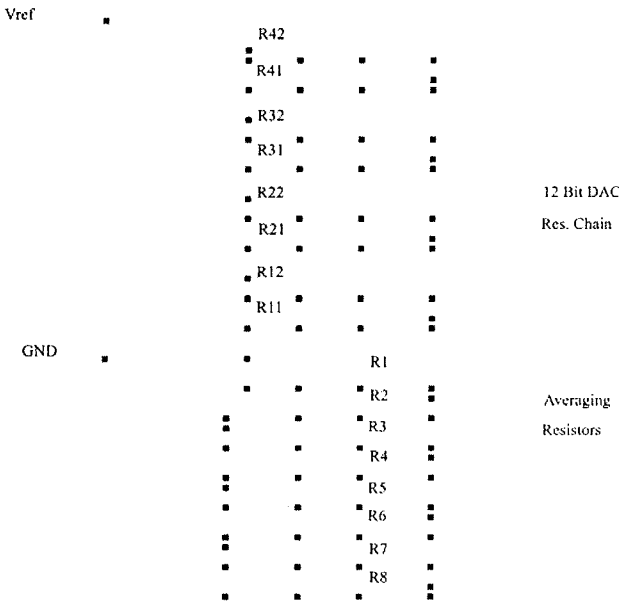

Fig. 3. Layout averaging. Dark dots represent the current-poly1-metal1 contacts. This scheme corresponds to "lay2" curves on MatLab analysis figures.

$$INL = V_{ANA\_i} - V_{ANA\_ideal} = \frac{V_{ref}}{2^N} \cdot \sum_{k=1}^{i} \frac{dR_k}{R}$$

R is resistor-unit (ideal), dRk is difference from unit value,

If we assume that all mismatch terms are zero over resistors chain, then the worst-case error will occur at the middle of the chain:

$$i = 2^{N-1}$$

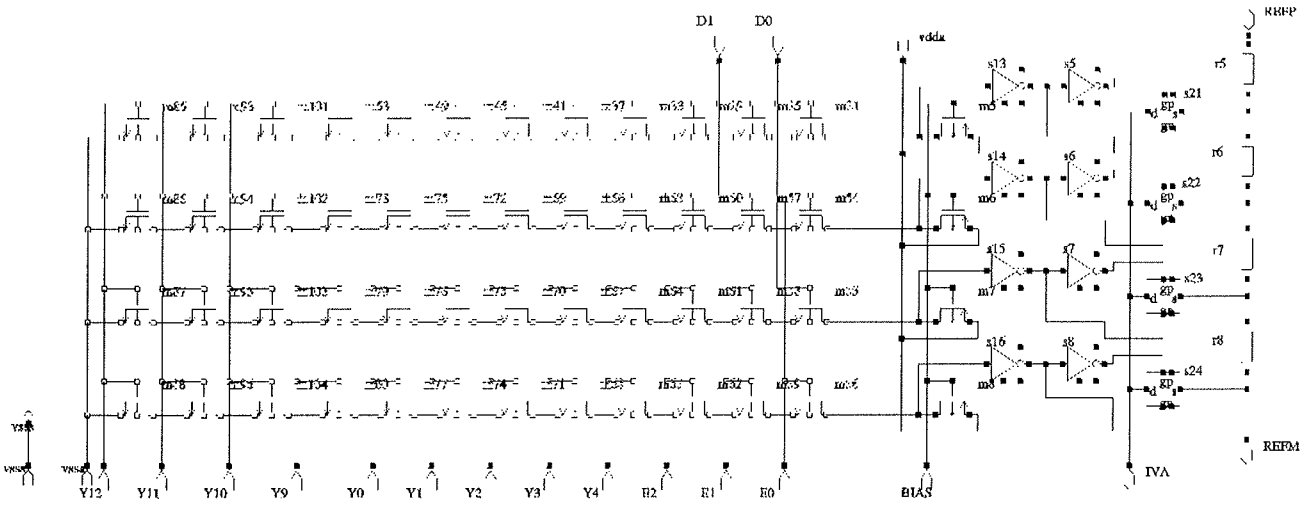

Fig. 2: Four - bit segment from 12 bit DAC

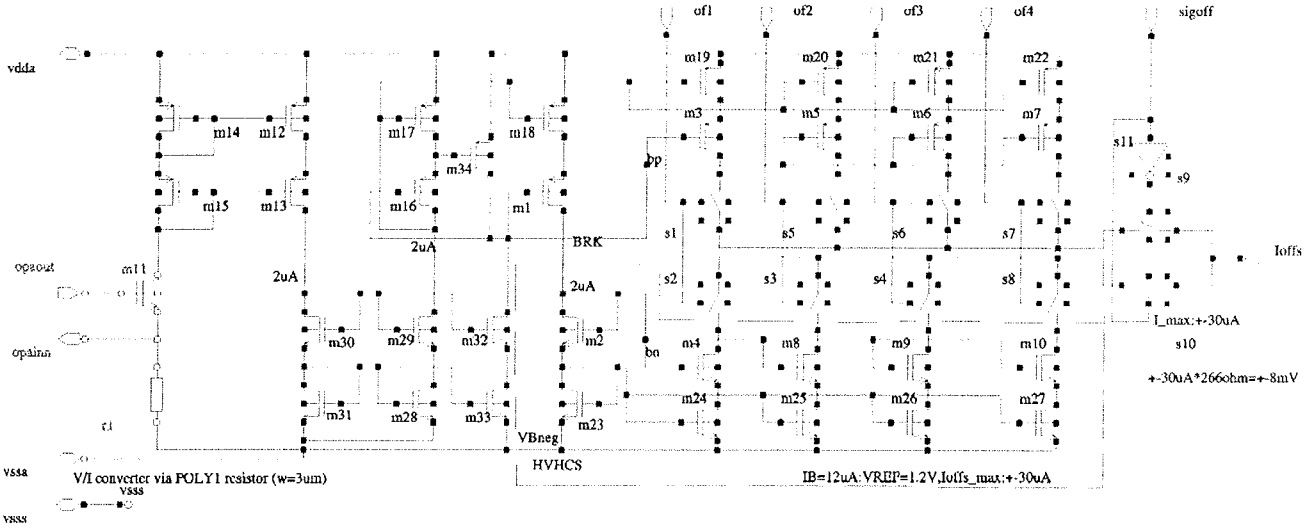

Fig. 4: Stable current generator for offset calibration. Binary weighted source and sink currents are generated from stable bandgap reference voltage.

And the maximum value of INL is:

$$INL_{\max} = \frac{V_{ref}}{2} \cdot \left[\frac{dR_k}{R}\right]_{\max}$$

It is evident that there is also an amplifier offset voltage contribution to INL. It contributes directly to INL. For high precision conversion, offset cancellation is a must (Fig. 4, Fig.5 and Fig. 6).

Maximum negative mismatch dominates at all the resistors in the lower half of the chain and the maximum positive mismatch occurs in the upper half of the chain or vice-versa, depends on resistivity gradient. Fig. 8 shows the INL error over all 12 bit on digital input.

Layout averaging principle uses additional parallel resistors to each sub-block of the DAC (Fig.3). The number of sub-blocks and the appropriate number of additional resistors define the possible layout mirroring and scrambling combinations. The different types of mismatches may occur randomly in X and Y direction on silicon. The sub-blocks mirroring and scrambling are therefore required in all directions (Fig. 8, Fig. 9, and Fig. 10). The number of sub-blocks is limited by the connectivity between sub-blocks and between the averaging resistors. The poly1-to-metal contact resistivity may vary from 2 Ohm to 20 Ohm, which could be more the one LSB unit resistor. Serial connections are required (metal1 and metal2), but they need to be done in proper way (temperature coefficient of Al metal resistivity). These contacts conduct the all-resistors main-chain current and may cause the majority of INL and DNL error.

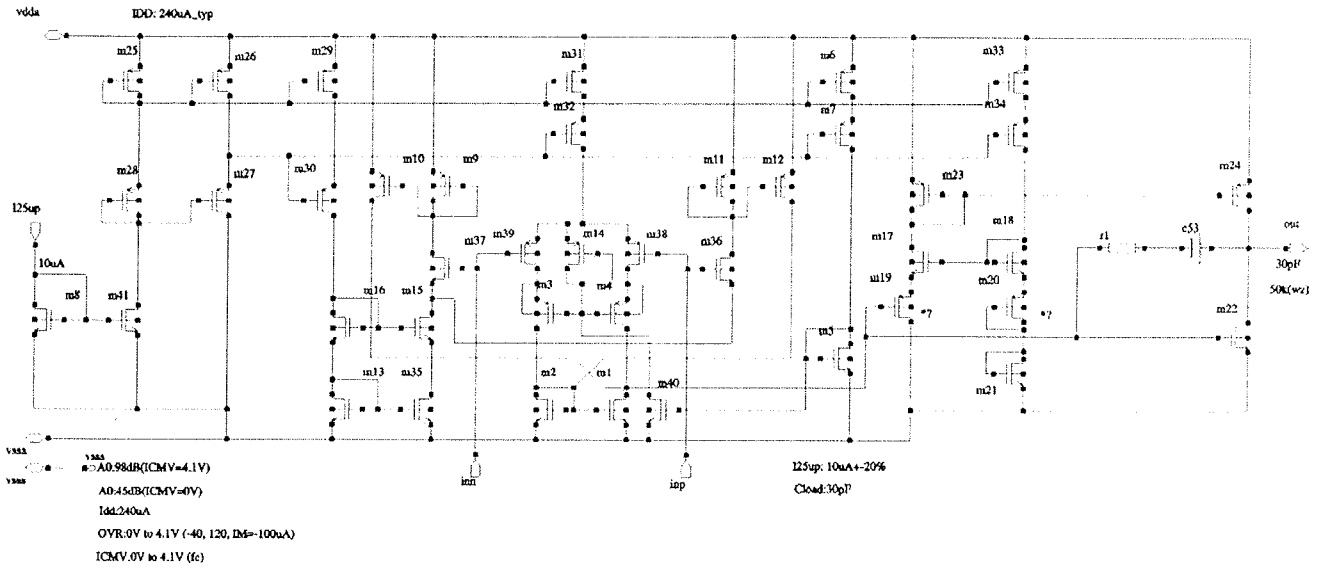

Fig. 5: High gain class AB amplifier having input voltage range from negative rail to 300mV from positive rail.

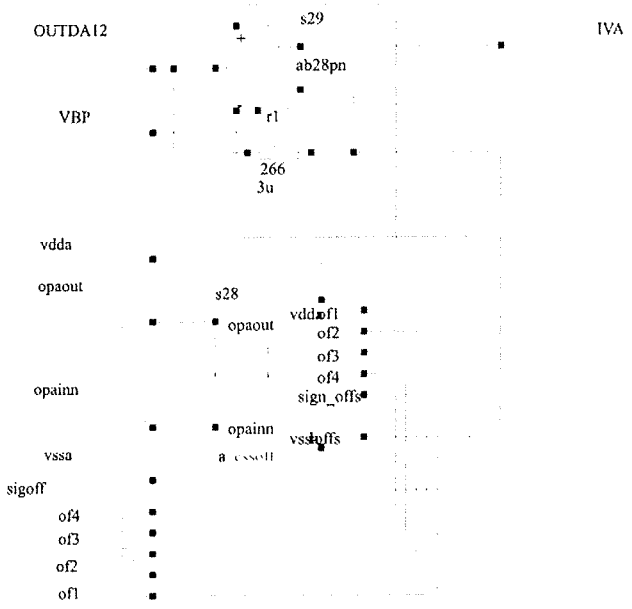

Fig. 6: Amplification of internally generated analog voltage Viva and offset correction circuitry.

Next important layout constraint is mismatch minimization. The resistor-unit value and its width on layout influence on analog output delay and on mismatch between units. Huge mismatch occurs when equal units have different neighbors.

IV. Conclusion

The required matching of resistors in chain using so called end-point analysis is relatively high and is derived from INL expression:

$$INL < 0.5LSB..... \frac{1}{2^N} [\%matching]$$

N is converter precision. The 12 bit DAC require 0.025% resistors matching which is theoretical and practical possible limit when all available techniques are implemented. That means the layout is very critical part of the analog circuit design. Again, theoretically is possible to realize the active element matching. As a result, the mismatch and drift occur and the conversion accuracy may again be much lower then is converter precision. Our first measurements using code density principle and end-point approach without layout averaging give an encouraging result for INL, which was within +-2LSB at more then 50% samples. Layout averaging may improve the result for more then +-1.5LSB as is shown from Fig. 8 to Fig. 10. Much better result gives so called "best-fit" approach. Nevertheless, the proposed layout averaging, as is shown from Fig. 3 for 12 bit flash DA converter, is a challenge for designers to improve the result where fast conversion is of the most importance in integrated system on silicon. The principle itself guaranty the DNL performance to be much better then +-0.5LSB.

The layout - four bit intersection is shown from Fig. 7.

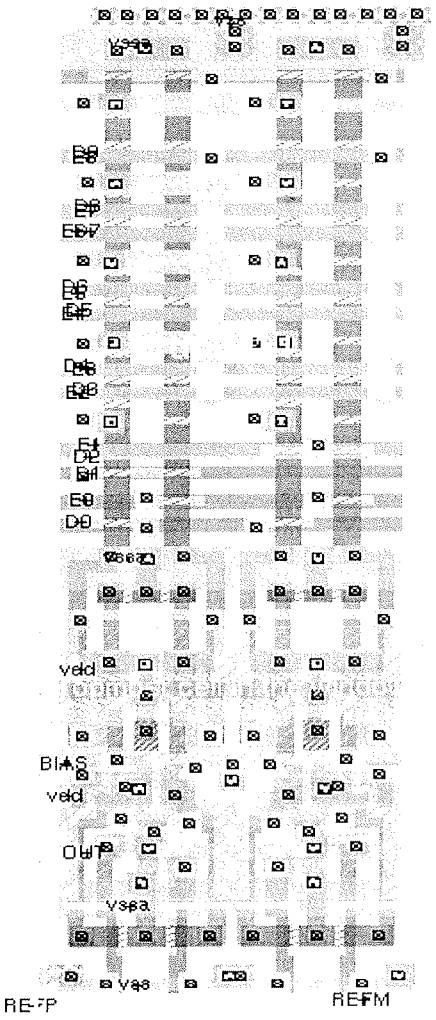

Fig. 7: Four - bit segment from the layout, as is shown from schematic in Fig. 2.

There are a number of different possible approaches like dual-ramp DAC /1/, where the accuracy depends on current generation accuracy, comparators offset and on clock frequency stability. Encouraging approach is a self-calibration method /2/, but it requires a long calibration period. It is clear that all improvements are possible mainly when using scaled down technologies which allows operation at much higher clock frequencies. Both principles may give conversion time better then 10us.

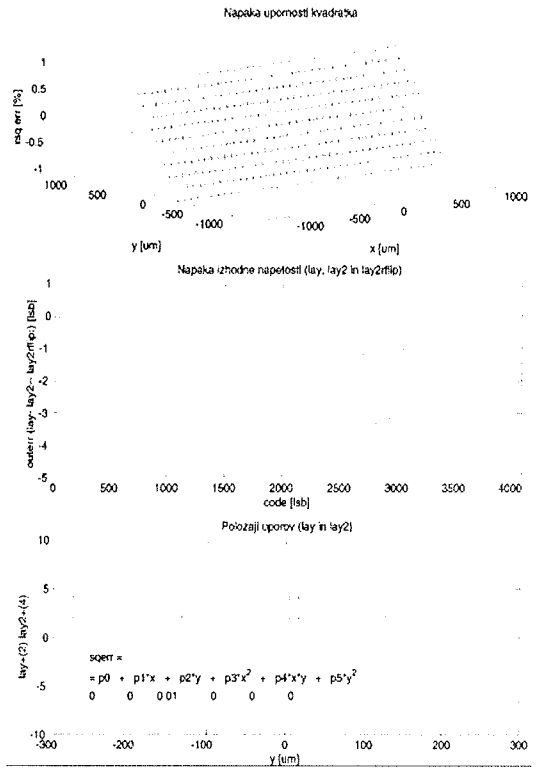

Fig. 8: Three curves are as follows: -4LSB maximum INL at the middle of the string, mirroring-parallelism - -1.5LSB and layout averaging 8:4 give accuracy of 1LSB. Gradient in Y direction is (0.5K-code-direction).

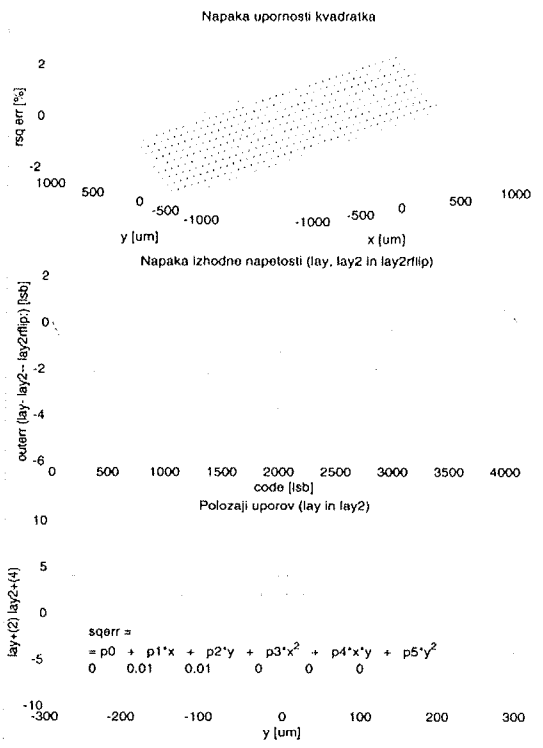

Fig. 9: Linear gradient in X/Y direction gives four max. and four minimums. They correspond to the number of segments that alternate in direction X.

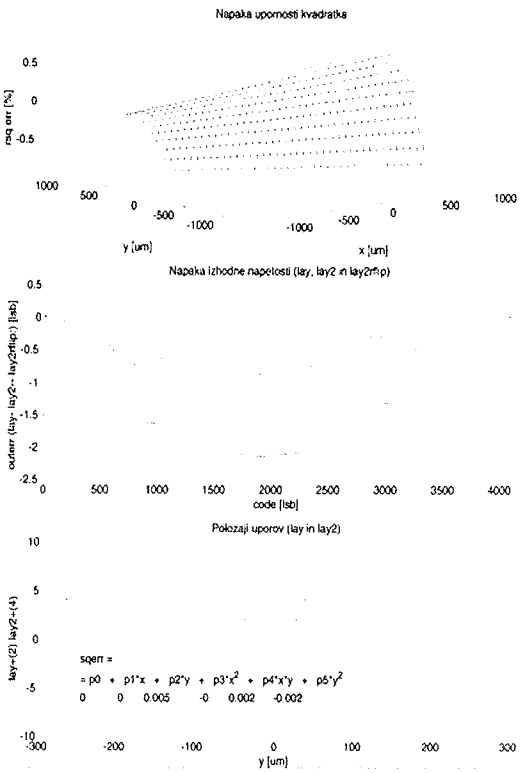

Fig. 10: Random mismatch and random weighting as is shown on first and last canvas. In X direction are resistors string of 0.5k codes, in Y direction are 8 times 0,5k codes and parallel string.

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