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Design of Low-Power Temperature Sensor Architecture for Passive UHF RFID Tags

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Abstract: A low-power wide-range CMOS temperature sensor architecture is proposed based on temperature-to-frequency conversion using supply voltage controlled sub-threshold ring oscillator. The principles of operation are investigated and proved via analytic and simulation results. Most errors are canceled out by this ratio-metric design. An inaccuracy of -0.84°C to +0.34°C occurs over a range of -40°C to 80°C after using a novel in-field digital two-point calibration. The entire sensor consumes less than 93nW to 305nW over the temperature range and can be digitally reconfigured for setting sample rate and resolution in a tradeoff.

Keywords: CMOS temperature sensor; temperature-to-frequency; low-cost calibration; wireless sensing; RFID tags

Dizajn arhitekture temperaturnega senzorja nizke moči za pasivne UHF RFID etikete

Izvleček: Predlagana je arhitektura CMOS temperaturnega senzorja nizke moči, ki temelji na pretvorbi temperatura-frekvenca z uporabo napajalne napetosti kontroliranega pod pragovnega oscilatorja. Principi delovanja so raziskani in utemeljeni analitično in z rezultati simulacij. Večina napak je odpravljena z metričnim dizajnom. Negotovost, z uporabo nove dvotočkovne digitalne kalibracije je, znaša od -0.84 °C do +0.34 °C v širokem pasu od -40 °C do 80 °C. Poraba senzorja je od 93 nW do 305 nW in je lahko digitalno spremenljiva za določanje optimalnega vzorčenja in resolucije.

Ključne besede: temperaturni senzor CMOS; temperatura-frekvenca; cenena kalibracija; brezžično tipanje; RFID etikete

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1 Introduction

Integrating Radio-Frequency Identification (RFID) tags with sensors has becomes the mainstream of realizing sensor nets [1]. Integrating passive RFID tags with external temperature sensor is reported in [2]. While external sensors require separate readout circuitry, smart sensors combine a sensor and interface electronics in a single chip. Most smart temperature sensors in CMOS technologies make use of temperature dependent characteristics of substrate PNP transistors. These sensors could reach a high accuracy over a wide temperature range [3] but usually consume power in the order of tens of micro watts and their performance deteriorates once the supply voltage falls below 0.6 V.

Using threshold voltage and thermal voltage variation of sub-threshold MOS transistors, low silicon area voltage-output temperature sensors [4] or front-end thermal sensing elements [5] could be implemented. However, adding analog to digital converters and other associated digital signal processing electronics, the power consumption of these sensors, is still higher than the power budget of passive RFID tags, few hundreds of nano watts.

Using time-domain readout techniques and terminating power-hungry analog to digital converters, low power sub-microwatt smart sensors could be implemented in temperature-to-frequency and temperature-to-time (pulse width) converter architectures in cost of sacrificing sensor gain linearity and operating range. Temperature-to-frequency architectures are reported using temperature-dependent bias current ring oscillator [6, 7, 8] and temperature-dependent voltage-controlled LC oscillator [9]. Main architectures of temperature-to-time sensors are: converting temperature-dependent current to pulse-width [10, 11], temperature-dependent voltage to current to pulse-width

[12, 13], leakage current to logarithmic pulse-width [14], temperature to delay time using delay line [15, 16] temperature to pulse-width of variable ring oscillator instead of delay line [17].

Sub-threshold ring oscillators are highly sensitive to the supply voltage, while consuming low power. Wide-range low power temperature sensors could be implemented using such an oscillator as a PTAT frequency generator. Compared to a similar oscillator as a reference, the common source of errors will be canceled in a ratio-metric design and the linearity will improve. Based on this concept, in this paper, a new wide-range, reconfigurable, nano-watt smart sensor architecture is proposed. RFID tag applications need a low-cost calibration technique. Avoiding the conventional costly two-point calibration process, a novel low-cost in-field group digital calibration technique is presented too.

The rest of this paper is organized as follows. Section II introduces the temperature sensor architecture and its measurement principles. Building blocks of the sensor architecture are theoretically analyzed and described in circuit level in Sections III and IV. Digital sensor gain, temperature calculation and calibration mechanisms are described in Section V. Section VI shows the simulation results. The conclusion is presented in Section VII.

2 Temperature sensor architecture and operation principle

2.1 Low Power Temperature Sensor Architecture

The architecture of the proposed temperature sensor is shown in Fig. 1. The sensor consists of two frequency paths. One of them is a constant-with-temperature reference frequency oscillator and the other one is a proportional to absolute temperature (PTAT) frequency oscillator. Two similar counters start to count the number of the output signal pulses of each oscillator as soon as *Reset* is asserted. N_{count} is the number of reference frequency oscillator pulses indicating the period of comparison and N_{times} is the number of times that the comparison is repeated. The digital bit of E_n enables the current bias of both oscillators.

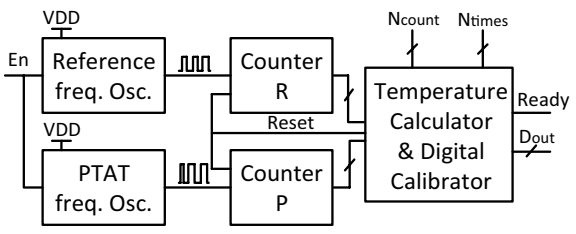


Figure 1: The architecture of the proposed temperature sensor.

2.2 Compensated temperature measurement

Digital temperature readout could be produced comparing the temperature dependent frequency of the PTAT oscillator to the reference frequency. Considering the frequency change across the temperature variation range as:

$$\Delta f_{sen} = f_{sen(T_{max})} - f_{sen(T_{min})} \tag{1}$$

the sensor gain S_G can be defined as:

$$S_G = \Delta f_{sen} / \left(T_{max} - T_{min}\right) \tag{2}$$

Dividing the frequency change by the reference frequency f_{ref}, the sensor digital output could be defined as:

$$\Delta D_{sen} = \Delta f_{sen} / f_{ref} \tag{3}$$

Finally, the digitized sensor gain D_{SG} can be expressed as:

$$D_{SG} = \Delta D_{sen} / \left(T_{max} - T_{min}\right) = S_G / f_{ref} \tag{4}$$

which is the ratio of the sensor gain and the reference frequency and compensate for the bulk of common sources of error and nonlinearity in the ratio-metric design.

3 Temperature and process variation compensated oscillator

For low-power low-cost oscillator, needed in RFID tag applications, ring oscillator architecture seems to be the best candidate. The frequency of the ring oscillator could be controlled robustly via current bias of the chain inverters. Another technique to control the frequency of the ring oscillators is supply voltage control [18]. The frequency of the ring oscillator is highly sensitive to the supply voltage, temperature and process variations. This sensitivity will increase even more in sub-threshold regime. Considering this, a compensation technique is proposed to control the frequency of a sub-threshold ring oscillator using an adaptive supply voltage.

Fig. 2 (a) shows the architecture of the reference frequency generator. A series voltage regulator generates the adaptive sub-threshold supply voltage of the ring oscillator V_a, from a supply voltage V_{DD}, using an adaptive voltage reference V_b. V_b is generated by biasing a diode-connected PMOS with a digitally enabled current mirror in the sub-threshold region. E_n enables the

M_{ref} bias which sets the level of the reference voltage V_b and thus the sub-threshold supply voltage V_a.

The circuit schematic of the adaptive voltage regulator is shown in Fig. 2 (b). The digitally enabled current mirror generates the reference current I_{ref}. The series-voltage regulator compares the sample of V_a with the reference V_b and control the output transistor M_p which causes V_a to be a fixed ratio of V_b as $V_a = \alpha V_b$.

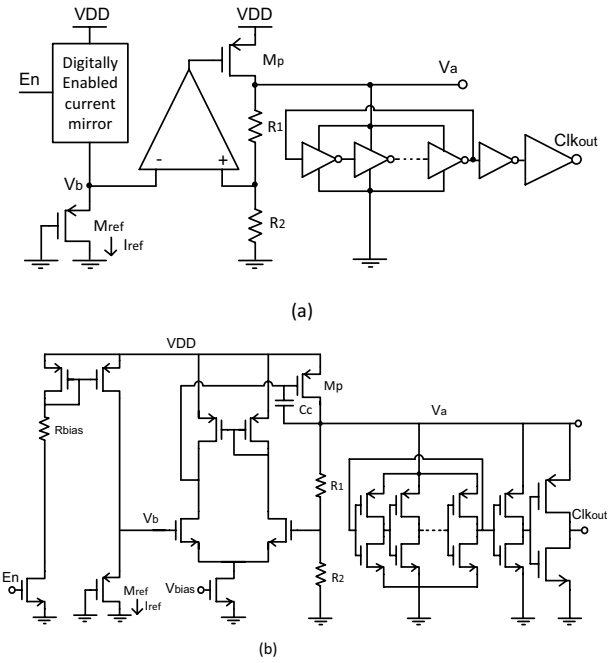


Figure 2: (a) The architecture of the reference frequency generator; (b) Complete circuit schematic of the adaptive voltage regulator and the reference frequency generator.

Biasing M_{ref} in sub-threshold regime with the fixed current I_{ref}, V_a and V_b are decreasing with temperature and show a complementary to absolute temperature (CTAT) behavior. The oscillation frequency of the ring oscillator is decreasing with reduction of sub-threshold supply voltage V_a too. Therefore using V_a as supply voltage, the oscillation frequency of the ring oscillator is decreasing with temperature and represents a CTAT behavior. On the other side considering a fixed sub-threshold supply voltage, the oscillation frequency of the ring oscillator is increasing with temperature due to increase of the sub-threshold current of the transistors and shows a PTAT behavior. It is sufficient to adjust α to set the sub-threshold supply voltage V_a in a range that the CTAT behavior of the oscillation frequency of the ring oscillator compensates the PTAT one to make the reference frequency constant with temperature.

Now we proceed with propagation delay calculation. The propagation delay of a CMOS inverter can be calculated as:

$$t_p = \ln(2)\left(\left(R_{eqn} + R_{eqp}\right)/2\right)C_L \tag{5}$$

where R_{eq_P} and R_{eq_N} are the equivalent resistors of pull-up and pull-down transistors in an inverter and C_L is the total output capacitance. The drain current equation in the sub-threshold region can be expressed as [19]:

$$I_{DS} = I_{S0}\left(1 - exp\left(-\frac{V_{ds}}{v_t}\right)\right)exp\left(\frac{V_{gs} - V_{th} - V_{off}}{nv_t}\right) \tag{6}$$

where the parameter v_t is the thermal voltage and is given by $K_B T / q$. V_{th}. V_{th} is the threshold voltage of the transistor. V_{off} is the offset voltage which determines the drain current at $V_{gs} = 0$. The parameter n is the sub-threshold swing parameter (or slope factor) which is a function of channel length and the interface state density [19] and can be illustrated by slope of logarithmic drain current versus gate voltage plot, with fixed drain, source, and bulk voltage in sub-threshold regime. I_{S0} is a temperature and process dependent parameter which its dependency on the temperature can be expressed as:

$$I_{S0} = k_{S0} T^{\beta} \tag{7}$$

Where the constant parameter k_{S0} and the power factor β can be calculated form technological parameters. Considering $V_{ds} >> v_t$, channel length modulation can be neglected and sub-threshold drain current can be simplified to:

$$I_{DS} \approx I_{S0} \times exp\left(\left(V_{gs} - V_{th} - V_{off}\right)/nv_t\right) \tag{8}$$

For an inverter operating in sub-threshold region, R_{eq_P} and R_{eq_N} can be calculated as follows:

$$R_{eq} = \frac{1}{V_a/2}\int_{V_a/2}^{V_a} \frac{V}{I_{S0}exp\left(\frac{V_a - V_{th}}{nv_t}\right)}dV = \frac{3}{4}\frac{V_a}{I_{S0}exp\left(\frac{V_a - V_{th}}{nv_t}\right)} \tag{9}$$

where V_a is the supply voltage (See Fig. 2). Replacing (9) in (5), the propagation delay of each inverter can be written as:

$$t_p \approx 0.5\frac{V_a C_L}{I_{S0}exp\left(V_a - V_{th}/nv_t\right)} \tag{10}$$

The above equation confirms the simulation results which represented in Fig. 3 (b) and shows the inverse relation between the propagation delay and the supply voltage V_a at 25 ℃. V_a in turn is proportional to the reference voltage V_b, and is expressed as:

$$V_a = \left(1 + R_1 / R_2\right) V_b \triangleq \alpha V_b \tag{11}$$

The adaptive reference voltage can be calculated as:

$$V_b = nv_t \ln\left(I_{ref} / I_{S0_{ref}}\right) + V_{th_{ref}} \tag{12}$$

based on the current bias I_{ref}, and the values of threshold voltage and technological parameters n and $I_{S0_{ref}}$ for the reference diode-connected PMOS transistor M_{ref}.

The threshold voltage of transistor with substrate junction connected to source [19] can be expressed as:

$$V_{th} = V_{th}\left(T_0\right) + k_t\left(T / T_0 - 1\right) \tag{13}$$

which is a linear function of temperature and is derived from the threshold voltage in the reference temperature $V_{th}(T_0)$ and constant temperature coefficient k_t Based on (12), (13) and (7), V_b can be rewritten as:

$$V_b = V_{th}\left(T_0\right) - k_t + \left(\frac{k_t}{T_0} + n\frac{K}{q}\ln\frac{I_{ref}}{k_{S0_{ref}}}\right)T - \\ - \beta n\frac{K}{q}T\ln T \triangleq k_1 + k_2 T + k_3 T\ln T \approx k_1 + k_2 T \tag{14}$$

Where k_1, k_2 and k_3 are the corresponding coefficients of each term. The simulation results in Fig. 3 (a) shows that V_b is an approximately linear function of temperature with an R-squared regression of 0.9997 from -40°C to 80°C therefore $k_3 \approx 0$ and the corresponding term can be eliminated from the equation. Substituting V_a from (11) and V_b from (12) in (10) and using a few mathematical operations, t_p can be expressed as:

$$t_p = \frac{0.5\alpha V_b C_L}{\left(\frac{k_{S0}I_{ref}{}^{\alpha}}{k_{S0_{ref}}{}^{\alpha}}\right)T^{\left(\beta-\alpha\beta_{ref}\right)}exp\left(\frac{\alpha V_{th_{ref}} - V_{th}}{nv_t}\right)} \tag{15}$$

Substituting V_b from (14) and V_{th} from (13), (15) can be rewritten as:

$$t_p\left(T\right) \approx t_{p0}\left(k_1 + k_2 T\right)T^{\gamma}exp\left(k_{tp0} / T\right) \tag{16}$$

Where:

$$t_{p0} = 0.5\alpha C_L\left(k_{S0_{ref}} / k_{S0}I_{ref}\right)^{\alpha}\left(\left(\alpha - 1\right)k_t q / \left(nK_B T_0\right)\right)$$

$$k_{tp0} = \left(\alpha - 1\right)\left(V_{th}\left(T_0\right) - k_t\right)q / nK_B$$

$$\gamma = \alpha\beta_{ref} - \beta,$$

and b_{ref} and β, are the power factors for the reference and the ring oscillator transistors, as expressed in (7). α is the constant ratio of supply voltage to adaptive reference voltage and can be set with fine tuning of the ratio of R_1 and R_2 in the adaptive bias voltage regulator as in (11). The offset voltage of the amplifier, which directly adds to the supply voltage, will tune out in the calibration process too.

Taking the first derivative of t_p with respect to T from (16) and setting its value to zero results in t_p to be constant with temperature variations. Taking this derivative and eliminating the negligible terms (the terms with lower order of T) renders:

$$t'_p\left(T\right) = \partial t_p / \partial T = t_{p0}\left[k_2\left(\gamma + 1\right) + \left(k_1\gamma - k_2 k_{tp0}\right)T^{-1} + \right. \\ \left. + \left(k_1 k_{tp0}\right)T^{-2}\right]T^{\gamma}exp\left(k_{tp0} / T\right) \approx \\ \approx t_{p0}\left[k_2\left(\gamma + 1\right)\right]T^{\gamma}exp\left(k_{tp0} / T\right) \tag{17}$$

setting $t'_p(T) = 0$ results in $\gamma = -1$. Since $\gamma = ab_{ref} - \beta$, the parameter α can be set to a value which satisfy $\gamma = -1$. The desired condition obtained by tuning the ratio of R_1 and R_2 via parameter sweep in the simulation which resulted in $\alpha = 1.15$.

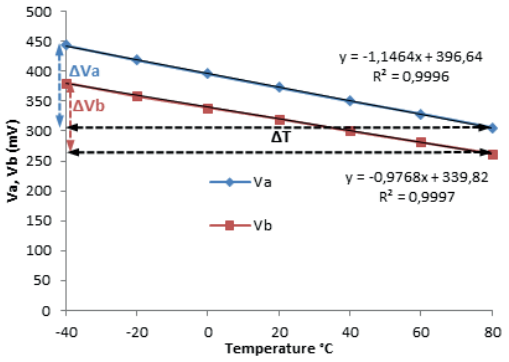
Fig. 3 (a) shows the variation of V_a and V_b versus temperature. With temperature variation of ΔT from -40°C to 80°C reduction value of ΔV_a and ΔV_b in the both supply and reference voltages are observed which conforms the CTAT behavior of the voltages.

Fig. 3 (b) represents the propagation delay and the oscillation frequency of the ring oscillator versus supply voltage at fixed 25°C temperature. It can be seen that the oscillation frequency will reduces with reduction of supply voltage and proportionally shows the CTAT behavior. Adjusting α and therefore ΔV_a in a proper range, the desired frequency variation value of Δf_a will be occurred with ΔV_a. In Fig. 3 (c) a frequency increase of Δf_T is observed due to full range temperature variation of ΔT from -40°C to 80°C which shows the PTAT behavior of the oscillation frequency of subthreshold ring oscillator with a fixed 0.4V supply voltage. In order to make the oscillation frequency stable with temperature the parameter α is adjusted to equate Δf_a with Δf_T which balances the CTAT and PTAT behavior of the oscillation frequency.

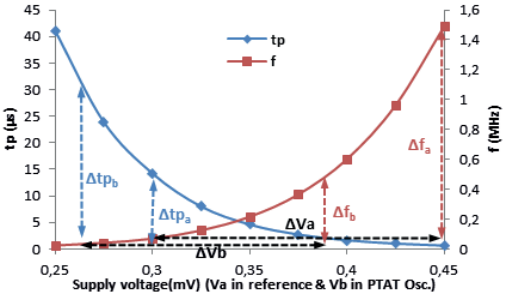
The propagation delays of the reference oscillator t_p versus temperature from 500 Monte Carlo simulation runs are shown in Fig. 3 (d). As expected from (16), the propagation delay is nearly constant across wide ranges of process and temperature variation. It can be seen that delay to temperature ratio of $\Delta t_p / \Delta T = 0.002$ *ppm* is resulted from -40°C to 80°C. Total ratio of the oscillation frequency variation to temperature across process corners and -40°C to 80°C temperature range is $\Delta f_{ref} / \Delta T$

= *980 ppm* and phase noise for center frequency of 310 KHz at 1KHz offset is -48dBC/Hz at 20°C.

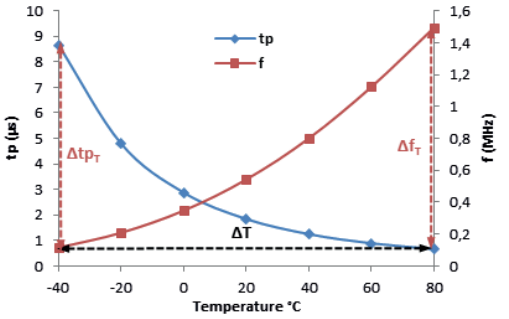
(a)



(b)



(c)



(d)

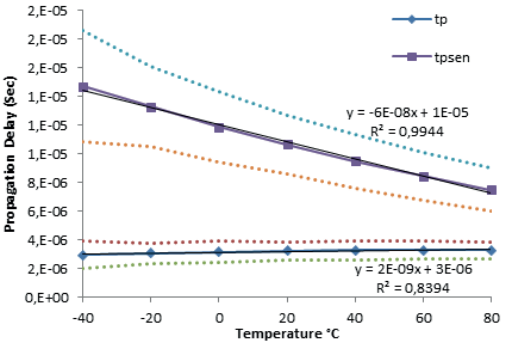


Figure 3: (a) Variation of reference voltage V_b and supply voltage V_a with temperature variation setting α = ***1.15;*** (b) Propagation delay t_p and oscillation frequency of the ring oscillator ***f*** vs. supply voltage at 25 °C; (c) Propagation delay and oscillation frequency of the ring oscillator ***f*** vs. temperature variation with a fixed 0.4 V supply voltage; (d) Average and its ±3σ boundaries of the propagation delay of the reference clock (t_p) and the PTAT frequency generator (t_{psen}) versus temperature based on Monte Carlo simulations.

4 Temperature dependent process variation compensated oscillator

In the previous section it was demonstrated how the reference frequency was made stable with temperature by adjusting α to set the sub-threshold supply voltage V_a in a range that the CTAT and PTAT behaviors of oscillation frequency counteract each other in the reference oscillator. Setting V_a higher than the adjusted range in the stabilized reference oscillator causes the oscillation frequency to show a CTAT behavior and setting V_a lower than the range, the PTAT behavior will be achieved.

The PTAT frequency generator circuit is similar to the circuit shown in Fig. 2 (b) except for $R_1 = 0$ which results in $a_{sen} = 1+R_1/R_2 = 1$, hence the regulated sub-threshold supply voltage output is equal to the adaptive bias voltage. The circuit uses the same adaptive voltage reference V_b and a separate ring oscillator with similar size and number of stages.

Fig. 3 (a) shows the variation of V_b versus temperature which is the same supply voltage for the PTAT oscillator. Fig. 3 (b) shows variation of the oscillation frequency Δf_b due to variation of the supply voltage ΔV_b at fixed 25°C temperature. It can be seen adjusting supply voltage in lower range ΔV_b by setting $a_{sen} = 1$, lower frequency variation Δf_b is resulted which is smaller than PTAT frequency variation Δf_T in Fig. 3 (c) as mentioned before. Therefore the PTAT behavior is dominant and make the frequency of the oscillator temperature dependent.

Considering $a_{sen} = 1+R_1/R_2 = 1$, similar to (16), the propagation delay for the PTAT frequency generator circuit can be derived as:

$$t_{p_{Sen}} \approx t_{p0_{Sen}} \left(k_1 + k_2 T\right) T^{\alpha_{sen}\beta_{ref} - \beta} exp\left(\frac{k_{tp0_{Sen}}}{T}\right) \quad (18)$$

As the R_1 value and therefore α_{sen} is optimized to make the digital output of the sensor linear (as described in section 5), the propagation delay of the PTAT frequency generator remains slightly nonlinear.

The propagation delay of the PTAT oscillator t_{psen}, versus temperature at different process corners are shown in Fig. 3 (d). Compared to the reference oscillator delay, the PTAT oscillator delay varies in inverse proportion to the absolute temperature while the reference oscillator delay is relatively constant. At room temperature (20°C) the propagation delay of the reference clock is $t_p = 3.21ms$, and the propagation delay of the PTAT frequency generator is $t_{psen} = 0.10ms$, which render $f_{ref} = 1/t_p = 310KHz$ and $f_{sen} = 1/t_{psen} = 94KHz$.

5 Digital sensor gain and temperature calculator

Although the PTAT frequency generator is a slightly non-linear function of temperature, the digital output of the sensor, which is the ratio of the PTAT frequency to the reference frequency, is an approximately linear function of temperature. To see this, assume the digital output to be:

$$D_{sen} = f_{sen} / f_{ref} = t_p / t_{p_{sen}} = \alpha / \alpha_{sen} \, exp\left(\frac{(\alpha_{sen} - \alpha) V_b}{n v_t} \right) \quad (19)$$

and substituting the exact equation of V_b from (14) and rewriting (19), the digital sensor output can be expressed as:

$$D_{sen} = \frac{\alpha}{\alpha_{sen}} exp\left(\frac{(\alpha_{sen} - \alpha) k_3 lnT}{nK/q} \right) exp$$

$$exp\left(\frac{(\alpha_{sen} - \alpha) k_2}{nK/q} \right) exp\left(\frac{(\alpha_{sen} - \alpha) k_1}{nK/qT} \right) \triangleq \quad (20)$$

$$\triangleq D_0 T^{\delta} exp\left(k_{D0} / T\right)$$

Where $\gamma = (\alpha - a_{sen})\, b_{ref}$ and D_0 and k_{D0} are constant coefficients. In order to make the digital sensor output a linear function of temperature, the second derivative of D_{sen} with respect to T should equals to zero. The first and second derivatives of (20) can be written as:

$$D'_{sen}(T) = \frac{\partial D_{sen}}{\partial T} = D_0 \left(\delta T^{\delta-1} - k_{D0} T^{\delta-2} \right) exp\left(k_{D0} / T\right) \quad (21)$$

$$D''_{sen}(T) = \partial^2 D_{sen} / \partial T^2 = D_0 \left[\left(\delta^2 - \delta \right) T^{\delta-2} + \right.$$

$$\left. + \left(2k_{D0} - \delta k_{D0} \right) T^{\delta-3} + {k_{D0}}^2 T^{\delta-4} \right] exp\left(k_{D0} / T\right) \approx \quad (22)$$

$$\approx D_0 \left[\left(\delta^2 - \delta \right) T^{\delta-2} \right] exp\left(k_{D0} / T\right)$$

neglecting the terms with lower order of T, the parameter δ can be set as δ = 1 to make $D''_{sen}(T) = 0$. It means $(\alpha - a_{sen})\beta_{ref} = 1$. By tuning the ratio of R_1 and R_2 via parameter sweep in the simulation, it reveals that, despite of the approximations, $\alpha_{sen} = 1$ satisfy this equation and results in the best linearity for the digital sensor output.

Practically the second derivative of D_{sen} remains slightly non-zero and for high-precision digital sensor output it should be presented in a second-order polynomial equation form (neglecting higher order terms) as:

$$D_{sen}(T) = D_{sen}(T_0) + (T - T_0) D_{sen}'(T_0) + \quad (23)$$

$$+ (T - T_0)^2 D_{sen}''(T_0) / 2 = a_0 + b_0 T + c_0 T^2$$

which is almost a perfect second-order polynomial function of temperature.

Fig. 4 shows the digital sensor output vs. temperature from 500 Monte Carlo simulation runs. The graphs fit second-order polynomial trend functions with an R-squared regression of 1 from -40°C to 80°C. According to the average D_{sen} fitted equation, equation (23) can be written as:

$$D_{sen}(T) = 0.2672 + 0.0018T + 0.000004T^2 \quad (24)$$

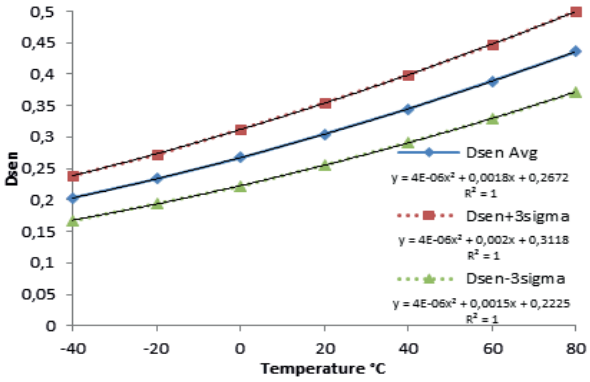


Figure 4: Average and its ±3σ boundaries of the digital sensor output with temperature variation based on Monte Carlo simulations.

5.1 Temperature Calculator

In section 2.2, we showed how the digital readout circuit principally measures the temperature. Here, we illustrate how the temperature calculator computes the temperature using N_{count} and N_{times} signals. The time period of each comparison is defined by:

$$T_P = N_{count} / f_{ref} \quad (25)$$

Where N_{count} is the number of reference frequency oscillator pulses at frequency of f_{ref} In this period of time, the number of PTAT oscillator pulses with frequency of f_{sen} can be calculated as:

$$N_{Sen} = T_P f_{sen} = N_{count} f_{sen} / f_{ref} \quad (26)$$

This results in:

$$N_{sen} / N_{count} = f_{sen} / f_{ref} \quad (27)$$

so the sensor digital output can be directly obtained by:

$$\Delta D_{sen} = \Delta f_{sen} / f_{ref} = \left(N_{sen2} - N_{sen1}\right) / N_{count} \quad (28)$$

Therefore the sample rate can be calculated as:

$$Sample\,Rate = 1 / T_P = f_{ref} / N_{count} \quad (29)$$

To calculate the temperature measurement resolution or the minimum measurable change in temperature DT_{min}, note that:

$$\Delta D_{senmin} = D_{SG} \Delta T_{min} \quad (30)$$

Considering (28), the minimum calculated frequency variation will be given by:

$$\Delta D_{senmin} = \left(N_{S2} - N_{S1}\right)_{min} / N_{count} = 1 / N_{count} \quad (31)$$

Finally, from the recent two equations, the digital readout resolution of the temperature measurement can be calculated as:

$$Resolution = \Delta T_{min} = 1 / \left(N_{count} D_{SG}\right) \quad (32)$$

5.2 Sensing Errors and Calibration

The process parameters' spread, the supply noise, and the nonlinearity of the frequency variation with temperature are the dominant sources of error. Due to the highly similar architecture of the two oscillators which differ only in the value of R_1, and their highly symmetric layout, most of the errors are expected to be canceled out in this ratio-metric design.

The supply and device noises of the ring oscillator are directly translated to the jitter of the output oscillation waveforms, which will be eliminated in digital counters.

As seen in Fig. 4, the nonlinearity of the frequency variation with temperature results in less error while perfectly fitting D_{sen} to a second-order polynomial function of temperature. Needless to say, this nonlinearity could be digitally compensated by implementing the inverse function of (24) in the temperature calculator to calculate the measured temperature from the resulting D_{sen} as below:

$$T = 500\left[\sqrt{(D_{sen} - 0.0647)} - 0.45\right] \quad (33)$$

The process parameters' spread causes an offset in both y-intercept and slope of the digital sensor output curve in Fig. 4. Thus a two-point calibration is required to trim the sensor for the 120°C temperature range.

5.3 Digital Group Calibration

There are some low-cost after packaging calibration techniques using an extra on-chip calibration transistor and calibrating the sensor by measuring die temperature [20], or batch mode calibration by calibrating a limited number of samples from a production batch, obtaining an estimate of average error and trim the entire batch using the information [21]. Due to ease of group communication in RFID applications, for the proposed temperature sensor, an In-field group-mode calibration at two different temperatures is proposed to digitally trim the sensor tags after packaging.

Fig. 5 shows the error of the digital sensor output vs. temperature from 500 Monte Carlo simulation runs. In the first-point calibration, all sensor tags are placed in the minimum operating temperature, e.g. T_1 = - 40°C, an interrogator announces the field temperature. Each sensor calculates the ideal corresponding digital sensor output D_{1ref} using the digitally implemented equation (24) and measures the real digital sensor output D_1. The y-intercept offset of the digital sensor output curve is calculated as follows:

$$\Delta D_1 = D_{1ref} - D_1 \quad (34)$$

ΔD_1 for a sample on the +3σ boundary is shown in Fig. 5. From then on, the sensor adds the above offset ΔD_1 to any measured output as a one-point calibration. Fig. 6 shows the error of the digital sensor output vs. temperature after the one-point calibration.

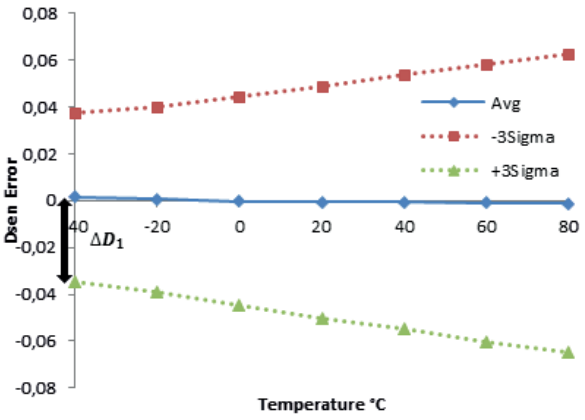


Figure 5: Error of the average and its ±3σ boundaries of the digital sensor output with temperature variation based on Monte Carlo simulations.

Again all sensor tags are placed in the maximum operating temperature, e.g. T_2 = 80°C, and an interrogator announces the field temperature. Each sensor calculates the ideal corresponding digital sensor output D_{2ref} and measures the real digital sensor output D_2. The slope offset of the digital sensor output curve is calculated as below:

$$\Delta D' = \left(D_{2ref} - D_2\right) / \left(T_2 - T_1\right) \quad (35)$$

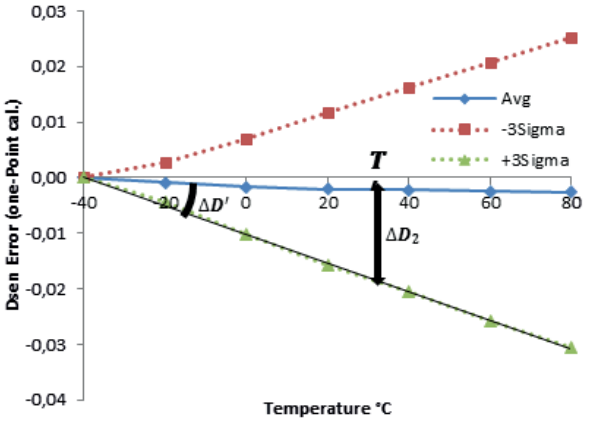


Figure 6: Error of the average and its ±3σ boundaries of the digital sensor output with temperature variation after one-point calibration.

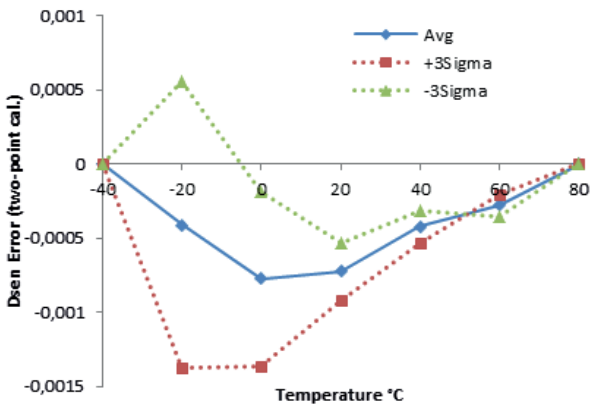


Figure 7: Error of the average and its ±3σ boundaries of the digital sensor output with temperature variation after two-point calibration.

At any working temperature, the sensor calculates the offset of the digital sensor output using the latest measured temperature T' as follows:

$$\Delta D_2 = \Delta D'\left(T' - T_1\right) \tag{36}$$

$\Delta D'$ and ΔD_2 at T' for a sample on the +3σ boundary are shown in Fig. 6. The sensor adds the above offset ΔD_2 to the latest measured digital output to calculate the new temperature, T and replaces T' with T and then recalculates ΔD_2 to find a more accurate temperature value, in an iterative way. The digital parameter N_{times} determines the number of iterations for temperature calculation. Fig. 7 shows the error of the digital sensor output vs. temperature after the two-point calibration. Being compared to Fig. 5, offsets in both y-intercept (ΔD_1) and slope ($\Delta D'$) of the digital sensor output curves are cancelled out for average and its ±3σ boundaries after the proposed two-point calibration.

The controlling signal N_{count} defines the programmable resolution and the sampling rate. The temperature sensor can be digitally reconfigured. There are two options: reducing the sampling rate while decreasing the resolution, or keeping the sample rate high while increasing the resolution.

6 Simulation results

The layout of the sensor core circuit is designed using an industrial 0.18 µm technology library and shown in Fig. 8. The size of the core sensor layout is 52.6µm×51µm. The netlist of the sensor circuit is extracted for post layout simulation and 500 Monte Carlo simulations were run. The functionality of the counters and the temperature calculator is evaluated using a software on a PC. In practice digital modules can be implemented with

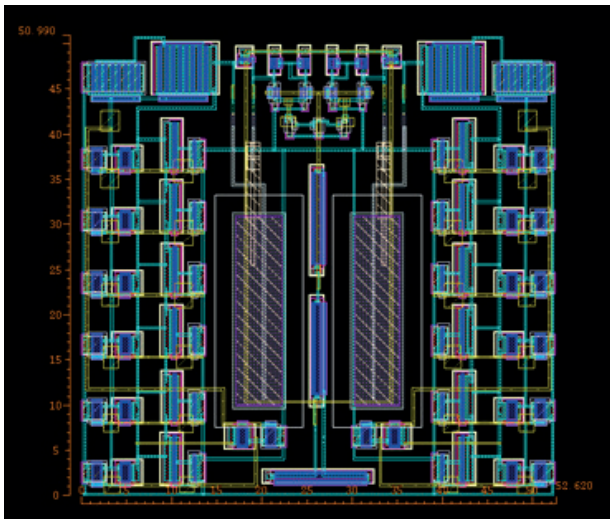


Figure 8: Layout of the sensor core.

sub-threshold static CMOS logic gates alongside with other digital parts of the RFID tag IC using the same supply voltage of the reference oscillator (V_d).

Fig. 9 shows the sensor error vs. temperature after the two-point calibration. It is shown that error ranging from -0.84°C to 0.34°C occurs over a range of -40°C to 80°C which is less than 1% of the measurement range.

N_{count} is set to 4600 to achieve a resolution of less than 0.3°C and the sample rate is calculated from (29). Fig. 10 shows the resolution of the sensor vs. temperature. This N_{count} value renders a sample rate of higher than 66 samples per second. Diagram of sample rate vs. temperature is shown in Fig. 11. The dynamic power consumption of the core sensor at different temperatures is calculated from the simulation and is shown in Fig. 12. The total power consumption varies from 93nW to 305nW over the full temperature range. The dynamic

(ac) power consumption changes depending on the oscillation frequency and supply voltage of the Reference and PTAT oscillators. The static (DC) power consumption increases with temperature due to increase in the sub-threshold currents and change in supply voltage even with decrease of the supply voltage V_a.

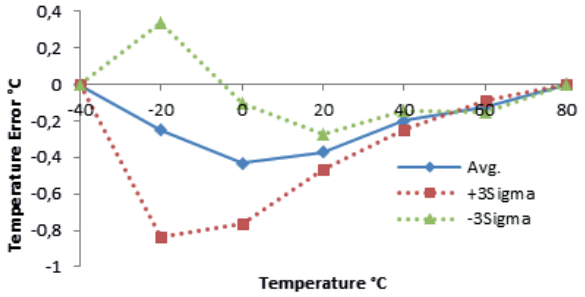


Figure 9: Temperature measurement error after two-point calibration.

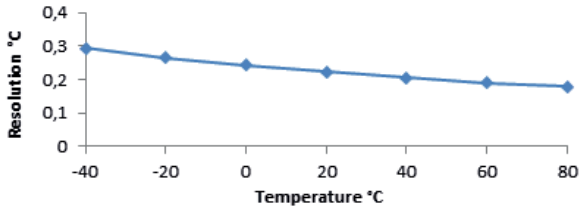


Figure 10: Sensor resolution vs. temperature with N_{count} = 4600.

The results are given in Table 1. Compared with the references, the proposed sensor architecture exhibits higher accuracy over a wider temperature range of 120°C, while having a nano-watt power consumption and comparable resolution and sample rate (See Table 1).

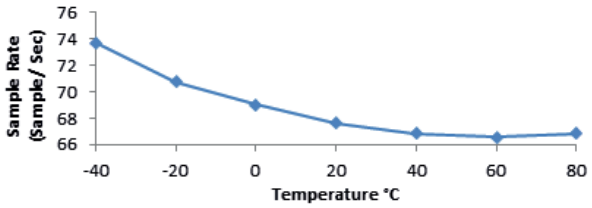


Figure 11: Sensor sample rate vs. temperature with N_{count} = 4600.

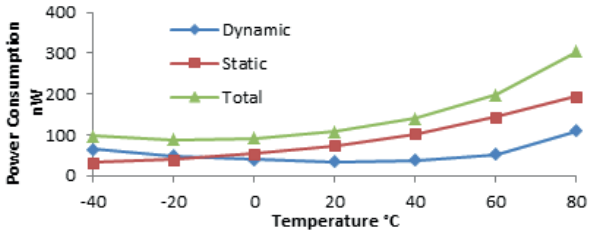


Figure 12: Power consumption of the sensor core vs. temperature.

7 Conclusions

Using supply voltage controlled sub-threshold ring oscillators, a wide-range, accurate and low-power temperature sensor architecture is demonstrated which can be dynamically reconfigured for setting resolution and sample rate. The architecture uses a ratio-metric design which cancels out most of the common sourc-

Table 1: Simulation results and comparison with references.

Parameter	[6]	[7]	[8]	[10]	[11]	[12]	[13]	[14]	[15]	[16]	[17]	This Work
Resolution (°C)	0.035	0.5	0.3	0.35	0.3	0.3	0.21	0.28	0.5	0.2	0.595	0.294
Error (°C)	±0.1	±1.5	-1.4/+1.5	±0.8	±1.5	-0.8/+1	-0.8/+1	±1.97	±1	-0.8/-1	-0.63/+1.04	-0.84/+0.34
Temp. Range (°C)	35~45	-40~85	0~100	-20~30	-30~60	0~100	-10~30	20~100	0~75	0~100	20~120	-40~80
Power Consumption (nW) @SR	110 @10	600 @-	71 @33	2400 @25	350 @68	405 @5	119 @333	1.05~65.5 @5	9000 @20	1500 @10	288100 @430K	93~305 @66
Energy/ Conversion (nJ per conversion)	11	-	2.2	96	5.2	81	0.35	0.2~13	450	150	0.67	1.4~4.6
Sampling Rate (Sample/Sec)	10	-	33	25	68	1K	333	12	1M	10	430K	66
Calibration	2-point	1-point	2-point	1-point	1-point	2-point	2-point	Without Cal.	2-point	2-point	1-point	2-point
Area (mm^2)	0.084	0.005	0.09	-	0.14	0.0324	0.0416	0.000843	0.4	0.025	0.031	0.00268
CMOS Technology	0.35µm	0.18µm	0.18µm	0.18µm	0.18µm	0.18µm	0.18µm	0.35µm	0.35µm	0.35µm	0.13µm	0.18µm

es of error. The difference between the reference and PTAT oscillators is only the value of a resistor which guarantees perfect tracking over process and temperature variations. Temperature inaccuracy of -0.84°C to 0.34°C occurs over a wide-range of -40°C to 80°C while the entire sensor consumes less than 93nW to 305nW over the measurement range, digital circuits excluded. While most of low-power temperature sensors have limited accuracy or temperature range, the proposed sensor accurately works over a wide range of 120°C. The proposed in-field digital calibration provides an appropriate low-cost method for sensor calibration. The sensor is suitable to be embedded in passive RFID tags and any other low-power wireless sensing application.

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