AREA AND POWER CONSUMPTION EFFICIENT VLSI IMPLEMENTATION OF PROGRAMMABLE COMB DECIMATION FILTER WITH LOW SWITCHING NOISE

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Key words: Decimation filters, comb structure, VLSI design, Σ–Δ A/D converters, switching noise reduction, power consumption minimization, IIR-FIR comb decimator.

Abstract: Power consumption, switching noise and area are among the most important parameters of decimation filters used in Σ–Δ A/D converters. We found that IIR-FIR implementation of a comb decimator gives the best compromise regarding this 3 parameters by using systematic method for switching noise and power consumption reduction and besides it is very easy to change the decimation factor. A programmable A/D converter has been built using noise optimized 2nd order modulator and optimized 3rd order comb decimator with f_{ovs}=4MHz and programmable oversampling ratios M=256, 128, 64. The area needed using 0.6μm CMOS technology is slightly less than 0.7mm^2. Average current consumption is approx. 2 times smaller and switching noise injected into the substrate is reduced almost 5 times compared to standard implementation. Measured results suggest that because of very low switching noise it is possible to use such IP block in high-resolution mixed-signal ASICs.

Površinsko in močnostno učinkovite VLSI implementacije programabilnega comb decimacijskega filtra z majhnim preklopnim šumom

Ključne besede: Decimacijski filtri, strukture comb, načrtovanje VLSI vezij, Σ–Δ A/D pretvorniki, zmanjševanje digitalnega šuma, IIR-FIR comb decimacijski filtri.

Izvleček: Najpomembnejši parametri pri načrtovanju decimacijskih filtrov uporabljenih v Σ–Δ A/D pretvornikih so poraba moči, preklopni šum in površina. Ugotovili smo, da struktura IIR-FIR omogoča najboljši kompromis glede navedenih treh parametrov pri uporabi sistematične metode za zmanjševanje porabe moči in "digitalnega" šuma. Poleg tega predlagana struktura omogoča enostavno implementacijo programiranja. Realizirali smo programabilni A/D pretvornik sestavljen iz optimiziranega modulatorja drugega reda in optimiziranega decimatorja comb tretjega reda, ki tečeta z vzorčevalno frekvenco f_{ovs}=4MHz in mu lahko programiramo decimacijski faktor. Površina silicija, ki jo potrebujemo za realizacijo takega comb decimacijskega filtra je manjša kot 0.7mm^2 v tehnologiji CMOS z dolžino kanala 0.6μm. Povprečen napajani tok comb decimatorja je približno 2 krat manjši, "digitalni šum" pa približno 5 krat manjši v primerjavi s standardno VLSI implementacijo. Izmerjeni rezultati dokazujejo, da je zaradi majhnega "digitalnega šuma" tak gradnik mogoče uporabiti pri načrtovanju občutljivih mešanih analogno-digitalnih vezjih z veliko ločljivostjo.

1 Introduction

Decimation filters are used in single or multi-bit Σ–Δ A/D converters to attenuate shaped quantization noise coming from one or multi-bit modulator and to reduce oversampling frequency to the Nyquist rate /5/. Out-of-band quantization noise must be attenuated before decimation in such a way that negligible amount of aliasing occur. Different realizations are possible and one of the most efficient in terms of hardware complexity is comb decimation structure /3/, using only additions, delays and down sampling. The order of a decimator is usually higher than the order of the modulator to be able to efficiently attenuate shaped quantization noise before decimation /5/. Other important concerns are area, power consumption and generation of "digital noise". Digital part of the A/D converter must inject minimum amount of "digital noise" into the substrate, must have as small power consumption as possible and must occupy as small silicon area as possible. In this paper we present such VLSI implementation, which also generates small amount of switching noise and has a possibility to program over-sampling ratio M in a simple and efficient way.

In section 2 short overview of possible implementations is given comparing characteristics regarding silicon area, power consumption, programmability and generation of digital noise. In section 3 we discuss programmability of the decimator, while section 4 shows simulation and measured results of a complete 16-bits A/D converter using programmable oversampling ratio. Section 5 presents the conclusions.

2 COMB decimator implementations

Transfer function of a comb decimator is defined in (1):

$$H(z)=\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^{k} \quad (1)$$

where M is decimation factor and k is the order of the filter. Possible signal processing implementations that do not require any multiplications are presented on figure 1: direct implementation on figure 1a, IIR-FIR implementation on figure 1b /5/, FIR2 cascade: figure 1c /8/. Two other possible implementations, POLY-FIR2 /7/ and RS implementation presented in /4/ are not really useful because they both need multipliers and thus significant amount of silicon area.

Direct implementation is the most straight-forward but not useful in really because the whole filter runs with oversampling frequency and thus consumes a lot of power and in addition it requires too much silicon area. Popular implementation for fixed oversampling ratio is a cascade of IIR-FIR filter and decimation in between, where the IIR part runs with f_{ovs} and FIR section runs with frequency $f_{FIR}=f_{ovs}/M$ taking every M^{th} sample from the IIR as the input for the FIR section. IIR section is composed of cascaded digital integrators. The arithmetics must be so called modulo or wrap-around arithmetics with Word length W defined in equation (2) /6/:

$$W=(W_{in}+k\log_2(M)) \quad (2)$$

where W_{in} is input word length, k is order of the filter and M is decimation factor. During integration the integrator states in IIR section increase until wrap-around happens. Difference realized in cascaded FIR sections gives correct result even if overflow was produced and the number in IIR registers has flipped. This is of course possible only if the register length in IIR and FIR stage conforms to the equation (2) above. The arithmetics used is two's complement modulo or wrap-around arithmetics.

The drawback of presented structure is that the registers of the whole IIR stage are wide (having for example for W_{in} =1, M=128, k=3 : W=22 even if possible resolution of an A/D converter is just 16 bits) and that the whole IIR section runs with oversampling rate f_s. Nevertheless as others have proved all other implementations except FIR2 need bigger area because of multipliers. Besides, other structures are so irregular that it is very hard to use systematic methods for reduction of switching noise defined in /1/. For IIR-FIR structure it is very easy to add programmability as is suggested in next section. The only competing architecture regarding area, power consumption, switching noise and programmability is FIR2 architecture, so let us briefly discuss it. Rewriting equation (1) using commutative rule we get (3):

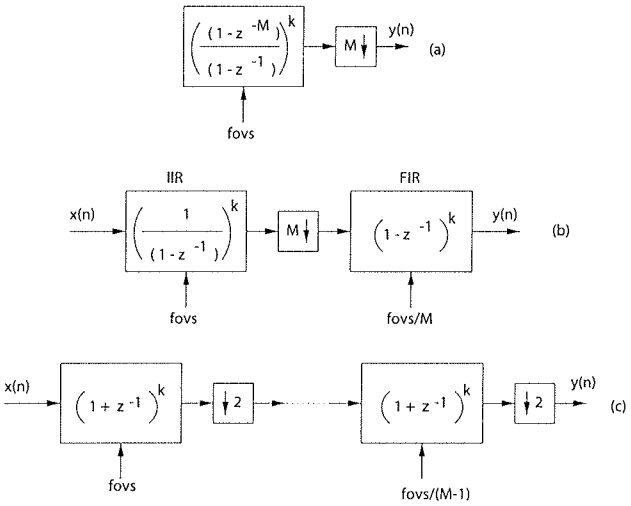

Figure 1: Possible implementations of a comb decimation filter

$$H(z)=\sum_{k=0}^{M-1}z^{-k}=\prod_{i=0}^{k\log_2 M-1}\left(1+z^{-2^i}\right)^{k} \quad (3)$$

It can be implemented as a cascade of equal first order FIR sections and decimation by 2 in between(see figure 1c). The word-lengths are different for every register in a cascade and need to be $W=(W_{in}+k_i)$. The first FIR stage calculates $(1+z^{-1})^k$ running with f_{ovs} and the word length need to be 2, 3 and 4 bits for k=3 and W_{in}=1 followed by decimation by factor 2. It is implemented by taking every 2^{nd} sample to the next stage which calculates again $(1+z^{-1})^k$ running with $f_s/2$ having word lengths of 5, 6 and 7 bits and so on. If we compare IIR-FIR and FIR2 signal processing requirements regarding number of bits in all registers (R), needed bit-additions/sec (A) and bit-shifts/sec (S) neglecting control logic the results are presented in table 1.

Table 1: Comparison of processing requirements for IIR-FIR and FIR2 structure

structure	R	A	S
IIR-FIR	150	$76*f_{ovs}$	$76*f_{ovs}$
IIR2	324	$36*f_{ovs}$	$36*f_{ovs}$

From this table we can easily see that IIR-FIR structure occupies smaller area compared to FIR2 because it needs smaller number of registers, besides the implementation is very regular and easy to design. The power consumption and switching noise seems to be bigger for IIR-FIR implementation if we consider just number of arithmetic operations and shifts. In reality FIR2 implementation is not so regular and up to now it was not possible to use systematic design methodology defined in /1/ for reduction of power consumption and switching noise. In addition, irregular structure requires bigger controller to implement

the algorithm, which further increases the area and also power consumption and switching noise. Since we are interested in area, power consumption, programmability and substrate noise generated in decimator (because modulator is built on the same substrate as the decimator) it seems that the approach giving optimum solution regarding all 4 requests is the IIR-FIR cascade improved in several ways: programmability, using VLSI implementation in which part of the switching energy is recycled /1/ and in this way low power consumption and very small switching noise is achieved. Because of the reasons above we selected suggested approach.

3 Programmable comb decimator

Detailed signal processing block diagram of 3rd order IIR-FIR decimator is presented on figure 2. Higher order is possible by cascading more IIR and FIR stages having decimation in between or by cascading several comb filters. We selected 3rd order decimator because we wanted to built programmable speed/resolution A/D converter using 2nd order modulator and 3rd order decimator. Programmability is achieved simply by extending the word-lengths to the maximum needed according to the variables M, k and W_{in} in equation (2) and taking every M^{th} result from the IIR stage. The new condition for the word lengths is given by equation (4):

$$W \geq (W_{in} + k \log_2(M)) \qquad (4)$$

using only so many bits at the output of the decimator as it is necessary for proper operation of a wrap-around arithmetic without loosing any information under any condition.

In next section some simulation and measured results are presented for programmable A/D converter having programmable oversampling ratio: M=64, 128, 256. In this way it is possible to program the speed and resolution of the A/D converter using only one 2nd order modulator and one 3rd order programmable decimator. Minimum word-length that would be needed for proper calculation is given in table 2 using parameters: k=3, W_{in}=1 and M=64, 128, 256.

Table 2: Word length of a 3rd order decimator for different M's

M	DUB	DLB	W	Wout
256	0	8	25	17
128	3	5	22	17
64	6	2	19	17

The names of the constants are: DUB is number of upper redundant bits at the output, DLB is number of lower redundant bits, W is minimum register lengths and W_{out} is the length of the output word. The decimator's word-length is: W=25 for all M's. Because quantization and thermal noise is constrained by the modulator's 16 bits resolution at M=256 and further signal processing needs, the word length taken out of the decimator is 17 bits for all M's. Each register has a length of 25 bits so wrap around arithmetics in IIR and FIR stage always performs 25 bits modulo arithmetics whatever the M is. We take out 17 bits (we need more bits because of further signal processing) according to figure 3. We could easily take out smaller number of bits for M=128 and M=64 but because of regularity 17 bits are taken out. The principle could be easily extended to other decimation factors M as long as M is a power of 2. The IIR section runs with f_{ovs} and the FIR section runs with f_{ovs}/M and is thus implemented in a serial processor. Because of its very regular structure it was possible to use systematic approach for power consumption minimization and for reduction of switching noise injected into the substrate /1/. Figure 4 shows layout of the decimator. Regular structure is clearly evident from the picture and needs only 0.7mm^2 in 0.6μm CMOS technology.

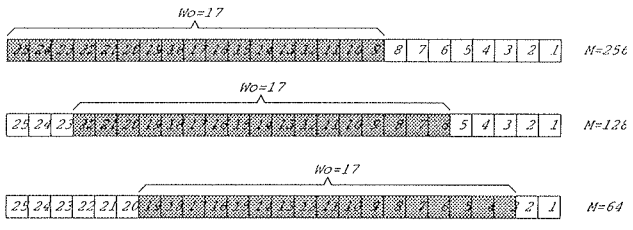

Figure 3: Output word formation

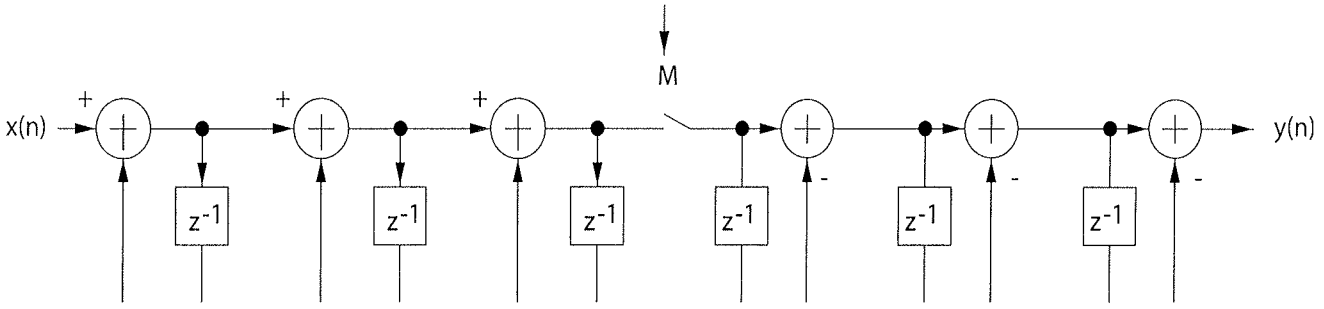

Figure 2: Signal processing block diagram of a 3rd order decimator

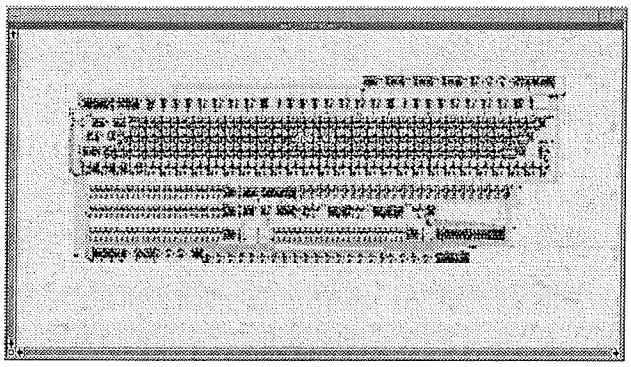

Figure 4: Layout of the decimator

4 Simulation and measured results

Σ–Δ A/D converter using 2nd order modulator optimized for noise performances /2/ and 3rd order decimator described in this article has been implemented in 0.6μm CMOS technology using f_{ovs}=4MHz according to the block diagram on figure 5. Time domain simulation of 1 bit 2nd order Σ–Δ modulator including kT/C and thermal noise sources of the S-C loop filter and making FFT on the bit stream (bs node on figure 5) gives $\frac{S}{N} = 96dB$ for M=256, which is slightly less than 16 bits in 8kHz band. The simulation results are presented on figure 6. 2 characteristics are presented lower, which does not include kT/C noise sources and the upper that includes all circuit noise sources.

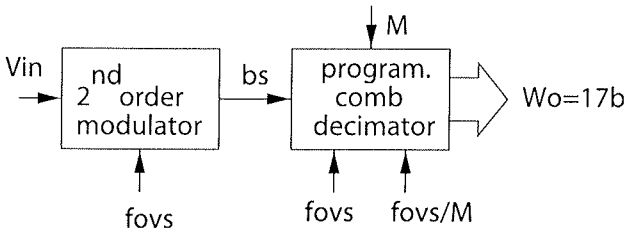

Figure 5: Block diagram of programmable A/D converter

Figure 7 shows transfer functions of a programmable comb decimator with M=256,128,64, which is used to attenuate out of band quantization noise of the bit-stream and to reduce sampling rate to f_s/M. To prove the behavior, a complete A/D converter was built in 0.6μm CMOS technology using systematic methodology to reduce switching noise and power consumption in comb decimator according to /1/. Power consumption and noise of the modulator has been optimized carefully, too. Figure 8 shows measured results of a complete A/D converter consisting of 2nd order modulator and programmable 3rd order decimator. Equal input signal was used for simulation of the modulator (see figure 6) and measurements. On the upper part of figure 8 M=128 is used and on the lower part M=64, that is why we have 1 bit difference in resolution. A factor of 2 difference can be observed between bandwidths of figure 6 and figure 8. This ratio is used for offset cancella-

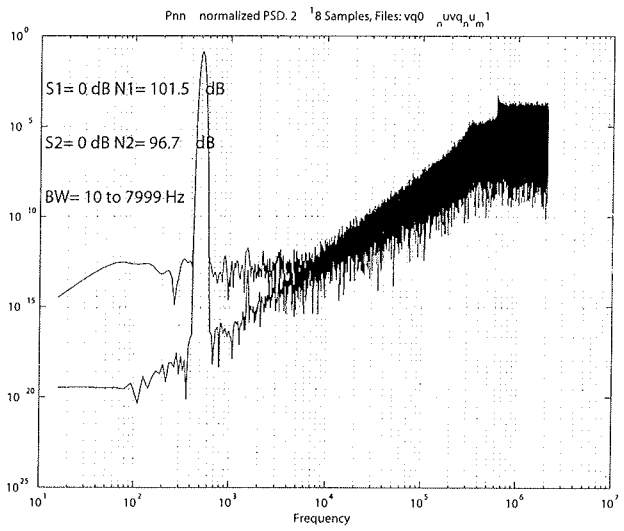

Figure 6: PSD of a bit stream

tion. It is evident that offset and 1/f noise components are highly attenuated. Current consumption of a complete A/D converter running with f_{ovs}=4MHz is less than 600mA at V_{sup}=5V. Measured switching noise observed on the substrate pin of a chip is much smaller (up to 5 times) compared to traditional standard cell approach.

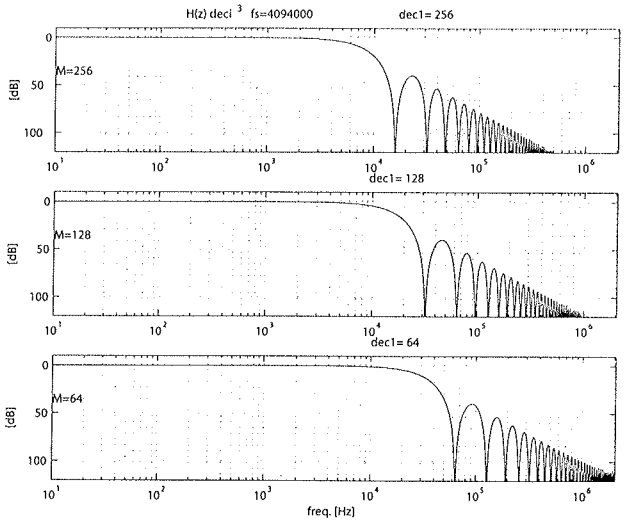

Figure 7: Programmable decimator frequency characteristics

5 Conclusions

Area and power consumption efficient programmable 3rd order comb decimator with very low switching noise has been implemented together with noise optimized 2nd order Σ–Δ modulator using 0.6μm CMOS technology. Several different implementations of a comb decimators have been analyzed. The IIR-FIR decimator architecture was selected because it is easy to implement, it is possible to

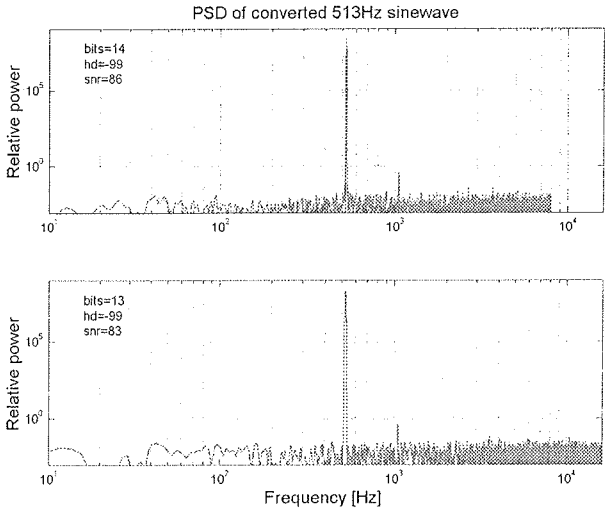

Figure 8: PSD of a measured sine wave

program decimation factor in a simple way, it occupies small silicon area and it is possible to use systematic method to reduce power consumption and switching noise. Measurements of implemented A/D converter show that it is possible to use it in a "low-noise" mixed-signal environment because of very low switching noise.

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