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Low-Voltage FGMOS Based Voltage-to-Current Converter

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Abstract: This paper proposes a novel floating-gate MOSFET (FGMOS) based voltage-to-current (VTC) converter. The proposed VTC converter has rail-to-rail input dynamic range, low THD (total harmonic distortion) and low power dissipation. The VTC converter has been simulated using SPICE in 0.25-μm CMOS technology with the supply voltages of ±0.75V. The simulation results of the VTC converter demonstrate THD of less than 1%, 3-dB frequency of 1.63GHz and maximum power dissipation of 0.84mW.

Keywords: Floating gate MOSFETs, low-voltage, mobility degradation, SPICE, VTC converter.

Nizkonapetostni napetostno-tokovni pretvornik na osnovi FGMOS

Izvleček: Članek predlaga nov napetostno-tokovni pretvornik (VTC) na osnovi MOSFET (FGMOS) s plavajočimi vrati. Predlagan VTC pretvornik ima polni vhodni napetostni obseg, nizko THD (dinamično harmonično distorzijo) in nizko disipacijo moči. VTC pretvornik je bil simuliran s SPICE v 0.25-μm CMOS tehnologiji z napajalno napetostjo ±0.75V. Simulacije VTC pretvornika izkazujejo THD manjši od 1 %, 3 dB pri 1.63 GHz in največjo disipacijo moči 0.84 mW.

Ključne besede: MOSFET s plavajočimi vrati, nizka napetost, degradacija mobilnosti, SPICE, VTC pretvornik

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1 Introduction

Low-voltage operation has become a major design issue for the analog signal processing applications. This is because a low-voltage power supply reduces the power dissipation which increases the battery lifetime and the reliability of the portable systems. Some of the low-voltage techniques used to reduce supply voltages are level shifters, self-cascode MOSFETs, sub-threshold MOSFETs, bulk-driven MOSFETs and floating-gate MOSFETs (FGMOS) [1-2]. Out of these, FGMOS presents a unique advantage of programmability of the threshold voltage. The other advantage of FGMOS is its compatibility with standard double-poly CMOS process technology. The FGMOS transistors have found many applications in electronic programming [3], digital-to-analog (D/A) and analog-to-digital converters [4], neural networks [5], voltage-controlled resistors [6]-[9], operational transconductance amplifier [10], multipliers [11], squarers [11]-[12], etc.

The voltage-to-current (VTC) converter is extensively used in the design of mixers/ modulators, voltage-to-frequency converters and interface units between circuits employing voltage-mode signal processing and those using current-mode processing. In addition, VTC converters are used as basic building blocks to perform various computational functions, such as square-rooting, squaring, multiplying, sum of squares and difference of squares, etc. [13]-[14]. The linearity and bandwidth are the usually concerned specifications of VTC converter which dominate whether its performance is adequate. The nonlinear effects of VTC mainly including nonlinear second-order V-I characteristic, body effect, mobility degradation, temperature variation and so on [15-19]. Recently, many researchers have been developed a fixed gain V-I converter input stage with programmable gain current mirrors [20]-[23]. However, these structures increase

complexity and power dissipation. In this paper, we have proposed a wide band linear VTC converter with mobility degradation and channel length modulation compensation.

The paper is organized as follows. The operation of the FGMOS is described in section 2. In section 3, the FGMOS based VTC converter is proposed. The detailed analysis of second-order effects on the performance of the proposed VTC converter is discussed in section 4. In section 5, SPICE simulation results are presented to verify the theoretical analysis and to demonstrate the effectiveness of the proposed circuit. The paper is concluded in section 6.

2 Operation of FGMOS

The basic structure of n-type, N-input FGMOS is shown in Figure 1. The first poly-silicon layer over the channel forms the floating gate and the second poly-silicon layer forms N-input gates that are located over the floating gate. The symbol and equivalent circuit model for an N-input FGMOS are shown in Figures. 2 (a) and (b), respectively. In both the figures, V_i (for i = 1, 2,…, N) are the control input voltages and D, S and B are the drain, source and substrate, respectively.

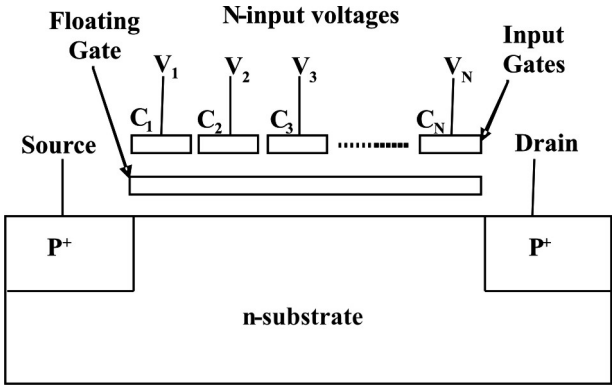

Figure 1: N-input FGMOS

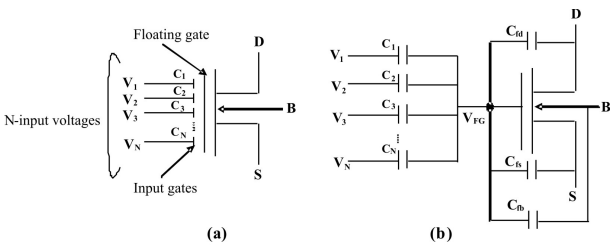

Figure 2: FGMOS (a) Symbol (b) Equivalent circuit

The N-input control gates are capacitively coupled to the floating gate. Hence, the voltage on the floating gate (V_{FG}) can be determined using the charge conservation law as [24]:

$$\sum_{i=1}^{N} C_i (V_i - V_{FG}) + C_{fd} (V_{DS} - V_{FG}) + C_{fs} (V_{SS} - V_{FG}) + C_{fb} (V_{BS} - V_{FG}) + Q_{FG} = 0 \quad (1)$$

Where C_1, C_2, C_3, …, C_N are the input capacitances between control gates and floating gate, $\sum_{i=1}^{N} C_i$ is the sum of N-input capacitances, C_{fd} is the parasitic capacitance between floating-gate and drain, C_{fs} is the parasitic capacitance between floating-gate and source, C_{fb} is the capacitance between floating gate and substrate, V_i is the input voltage of i^{th} input gate, V_{DS} is the drain-to-source voltage, V_{SS} is the source voltage, V_{BS} is the substrate-to-source voltage (usually, the value of V_{BS} is chosen as zero volt to avoid body effect), and Q_{FG} is the residual charge.

The residual charge Q_{FG} is trapped in the oxide-silicon interface during the fabrication process. The trapped residual charge gives rise to large variations in the threshold voltage of the FGMOS. The removal of the trapped charge in the FGMOS is possible by using the method suggested in [25-26], in which the first poly-silicon layer is connected to the metal-k (where k represents the top most metal layer, which is deposited and etched last) layer. By this contact, the floating gate is not connected to any other part of the circuit, so it will not affect the operation of the FGMOS. Therefore, Eq. (1) reduces to

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{fd} V_{DS} + C_{fs} V_{SS}}{C_T} \quad (2)$$

where C_T is the total capacitance and is given as

$$C_T = \sum_{i=1}^{N} C_i + C_{fd} + C_{fs} + C_{fb} \quad (3)$$

If $\sum_{i=1}^{N} C_i >> C_{fd}, C_{fs}$, Eqs. (2) and (3) are modified as:

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i}{C_T} \quad (4)$$

$$C_T = \sum_{i=1}^{N} C_i \quad (5)$$

The current equation of N-input FGMOS has been obtained by modifying the current equation of conventional MOSFET. The current I_p in the saturation region is expressed as follows:

$$I_p = \frac{K_p}{2} \left\{ V_{DD} - \left(\frac{\sum_{i=1}^{N} C_i V_i}{C_T} \right) - |V_{Tp}| \right\}^2 \quad (6)$$

where $K_p = \mu_p C_{ox}$ (W/L) is the transconductance parameter, μ_p is the mobility of holes, C_{ox} is the gate-oxide capacitance per unit area, (W/L) is the aspect ratio and V_{Tp} is the threshold voltage.

3 FGMOS based voltage-to-current converter

The proposed FGMOS based voltage-to-current (VTC) converter is shown in Figure 3. In this figure, the FGMOS transistors M_1, M_2, M_3 and M_4 are used to develop voltage-to-current conversion whereas the conventional MOS transistors M_5, M_6, M_7 and M_8 are used to provide proper biasing condition. All these transistors are biased in the saturation region. The transistors M_1, M_2, M_3 and M_4 are perfectly matched i.e. $K_{pi} = K_p$, $V_{Tpi} = V_{Tp}$ and $k_{i1} = k_{i2} = k_1$, where i = 1,2,3,4. The applied bias & input gate voltages of transistors M_1, M_2, M_3 and M_4 are V_b &V_{IN1}, V_b &-V_{IN2}, V_b &-V_{IN1} and V_b &V_{IN2}, respectively.

The transistors M_5 and M_6 form the current mirror and transistors M_7 and M_8 set the bias current. From Figure 3, it is evident that there is no body effect in the proposed circuit. The output current I_o is given as

$$I_o = I_1 - I_2 = \left(I_{p1} + I_{p2}\right) - \left(I_{p3} + I_{p4}\right) \quad (7)$$

Where I_{p1}, I_{p2}, I_{p3}, and I_{p4}, are the currents of transistors M_1, M_2, M_3 and M_4, respectively.

Using Eq. (6), the currents I_{p1}, I_{p2}, I_{p3}, and I_{p4} are given as

$$I_{p1} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN1}\right) - \left|V_{Tp}\right|\right)^2 \quad (8)$$

$$I_{p2} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN2}\right) - \left|V_{Tp}\right|\right)^2 \quad (9)$$

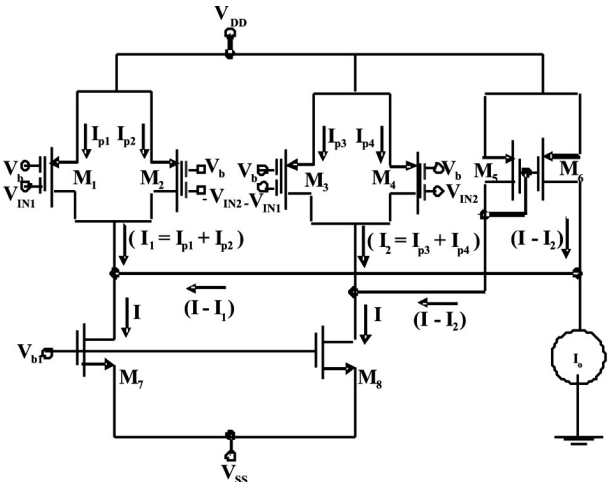

Figure 3: Proposed FGMOS based VTC converter

$$I_{p3} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN1}\right) - \left|V_{Tp}\right|\right)^2 \quad (10)$$

$$I_{p4} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN2}\right) - \left|V_{Tp}\right|\right)^2 \quad (11)$$

Where $k_1 = C_1/C_T$ is capacitive coupling ratio, V_{IN1} & V_{IN2} are input voltages, V_b is the bias voltage and V_{DD} is the supply voltage.

Substituting Eqs. (8) - (11) in Eq. (7), the output current I_o is given as

$$I_o = A\left(V_{IN2} - V_{IN1}\right) \quad (12)$$

where $A = 2K_p\ k_1\left(V_{DD} - k_1 V_b - \left|V_{Tp}\right|\right)$.

Equation (12) gives the linear relationship between the output current (I_o) and the differential input voltage (V_{IN2} - V_{IN1}). Hence, Figure 3 behaves as VTC converter.

4 Second order effects

In this section, the effects of channel length modulation and mobility degradation on the proposed VTC converter are discussed.

4.1 Channel Length Modulation Effect

The current I_p of 2-input FGMOS including channel length modulation effect is given as

$$I_p = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - \left|V_{Tp}\right|\right)^2\left(1 + \lambda V_{DS}\right) \quad (13)$$

where λ is the channel length modulation parameter.

Considering this effect, Eqs. (8)- (11) are modified as

$$I_{p1} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN1}\right) - \left|V_{Tp}\right|\right)^2\left(1 + \lambda V_{DS1}\right) \quad (14)$$

$$I_{p2} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN2}\right) - \left|V_{Tp}\right|\right)^2\left(1 + \lambda V_{DS2}\right) \quad (15)$$

$$I_{p3} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN1}\right) - \left|V_{Tp}\right|\right)^2\left(1 + \lambda V_{DS3}\right) \quad (16)$$

$$I_{p4} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN2}\right) - \left|V_{Tp}\right|\right)^2\left(1 + \lambda V_{DS4}\right) \quad (17)$$

From Figure 3, it can be seen that $V_{DS1} = V_{DS2}$ and $V_{DS3} = V_{DS4}$. Substituting the values of I_{p1}, I_{p2}, I_{p3}, and I_{p4}, from Eqs. (14)-(17) and $V_{DS1} = V_{DS2}$ & $V_{DS3} = V_{DS4}$ in Eq. (7), the output current I_o is given as

$$I_o = A\left(V_{IN2} - V_{IN1}\right) + B + C + D \quad (18)$$

where $A = 2K_p\ k_1\left(V_{DD} - k_1V_b - |V_{Tp}|\right)$;

$B = \lambda K_p\left(V_{DD} - k_1V_b - |V_{Tp}|\right)^2 (V_{DS1} - V_{DS3})$;

$C = \frac{\lambda}{2}k_1^2K_p\left(V_{IN1}^2 + V_{IN2}^2\right)(V_{DS1} - V_{DS3})$ and

$D = \lambda k_1 K_p\left(V_{DD} - k_1V_b - |V_{Tp}|\right)(V_{DS1} + V_{DS3})(V_{IN2} - V_{IN1})$.

For smaller values of (V_{DS1} - V_{DS3}) and (V_{IN2} - V_{IN1}), the effect of channel length modulation in Eq. (18) can be neglected.

4.2 Mobility Degradation Effect

The current I_p of 2-input FGMOS including mobility degradation effect is given as

$$I_p = \frac{K_p}{2}\left[\frac{\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - |V_{Tp}|\right)^2}{1 + \theta\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - |V_{Tp}|\right)}\right] \quad (19)$$

In Eq. (19), $\theta\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - |V_{Tp}|\right) << 1$, where Θ is the mobility degradation parameter. Using Binomial theorem expansion and neglecting the higher order terms, Eq. (19) is approximated as

$$I_p = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - |V_{Tp}|\right)^2 \cdot \left(1 - \theta\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - |V_{Tp}|\right)\right) \quad (20)$$

Including this effect, Eqs. (8)- (11) are modified as

$$I_{p1} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN1}\right) - |V_{Tp}|\right)^2 \left(1 - \theta\left(V_{DD} - k_1\left(V_b + V_{IN1}\right) - |V_{Tp}|\right)\right) \quad (21)$$

$$I_{p2} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN2}\right) - |V_{Tp}|\right)^2 \left(1 - \theta\left(V_{DD} - k_1\left(V_b - V_{IN2}\right) - |V_{Tp}|\right)\right) \quad (22)$$

$$I_{p3} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN1}\right) - |V_{Tp}|\right)^2 \left(1 - \theta\left(V_{DD} - k_1\left(V_b - V_{IN1}\right) - |V_{Tp}|\right)\right) \quad (23)$$

$$I_{p4} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN2}\right) - |V_{Tp}|\right)^2 \left(1 - \theta\left(V_{DD} - k_1\left(V_b + V_{IN2}\right) - |V_{Tp}|\right)\right) \quad (24)$$

Using Eqs. (21)-(24) in Eq. (7), the output current I_o is given as

$$I_o = 2K_p\ k_1\left(V_{DD} - k_1V_b - |V_{Tp}|\right)(V_{IN2} - V_{IN1}) - 3\theta k_1K_p\left(V_{DD} - k_1V_b - |V_{Tp}|\right)^2(V_{IN2} - V_{IN1}) - \theta K_p k_1^3\left(V_{IN2}^3 - V_{IN1}^3\right) \quad (25)$$

or

$$I_o = A\left(V_{IN2} - V_{IN1}\right)\left(1 - \frac{3\theta}{2}\left(V_{DD} - k_1V_b - |V_{Tp}|\right) - \frac{\theta}{2}k_1^2\frac{\left(V_{IN2}^2 + V_{IN1}^2 + V_{IN2}V_{IN1}\right)}{\left(V_{DD} - k_1V_b - |V_{Tp}|\right)}\right) \quad (26)$$

From equation (26), it can be seen that the second and third terms are very smaller than the unity, causes only the gain error. Since output current (I_o) is varied with the differential input voltage ($V_{IN2} - V_{IN1}$), mobility degradation effect can be neglected.

5 Results and Discussion

The proposed VTC converter has been simulated using SPICE in $0.25\mu m$ CMOS technology. The VTC converter operates with the supply voltages of $\pm 0.75V$. The various parameters of the designed VTC converter are listed in Table 1.

Table 1: Various circuit parameters

Circuit parameters	Values
CMOS Technology	0.25µm
Vb	0.75V
VTp	-0.55
λ	9.6X10-3
θ	0.05

Figure 4 shows the I-V characteristic of VTC converter and plots the output current I_o versus differential input voltage V_{IN2} - V_{IN1}. In this figure, blue and red lines denote the current/voltage characteristic for V_{IN2} while V_{IN1} = 0 and for V_{IN1} while V_{IN2} = 0 respectively. Figure 5 shows the THD obtained in the output waveform as a function of the peak-to-peak differential input voltage. From this figure, it is observed that for differential input voltage swings as large as 1.5V, distortion is still low (< 0.9%).

The total power dissipation of this circuit is .84mW. Figure 6 shows the frequency response of VTC converter and it is observed that the response remains constant till 1.63GHz.

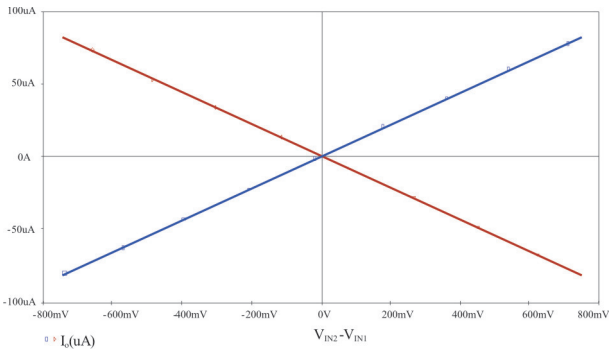

Figure 4: I-V characteristic of the proposed VTC converter

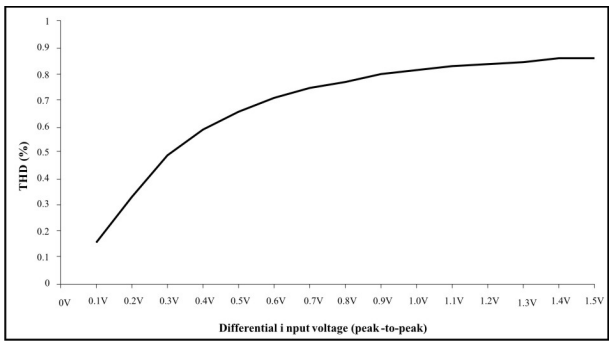

Figure 5: THD vs. differential input voltage amplitude

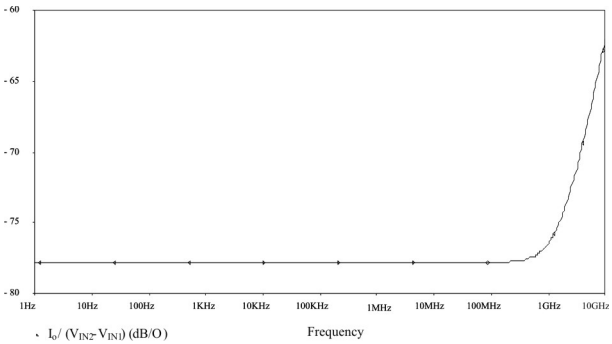

Figure 6: Transconductance ($I_o/(V_{IN2}-V_{IN1})$) curve for Figure 3

Table 2 compares the proposed FGMOS based voltage-to-current converter and the voltage-to-current converter reported by Srinivasan et al. in [27]. It is observed that FGMOS based voltage-to-current converter proposed in this manuscript has lower supply voltage requirement, lower power dissipation and wider input voltage range as compared to the existing circuit.

Table 2: Comparison of FGMOS based voltage-to-current converter with the voltage-to-current converter reported in [27]

Circuit parameters	Voltage-to-current converter [27]	Proposed FGMOS based voltage-to-current converter
Supply voltage	Not available	± 0.75V
CMOS technology	0.25 µm	0.25 µm
Input voltage range	± 500 mV	± 750 mV
Power dissipation	Not available	840 µW
-3dB frequency	200 MHz	1.63 GHz
THD	Not available	Less than 0.9%

Conclusion

In this paper, a new low-voltage FGMOS based VTC converter operates with the supply voltages of ± 0.75V has been presented. The inherent advantages of this circuit are wide input range, low power dissipation, low THD and wide frequency range which make it suitable for low-voltage signal processing applications. The analysis of the channel length modulation and mobility degradation effects show that they have little influence on the proposed circuit.

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