HOT WIRE DEPOSITED MATERIALS FOR THIN FILM TRANSISTORS

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Abstract : Thin film transistors (TFTs) find widespread application as the switching element in active matrix (AM) liquid crystal displays (LCD), such as the TFT display used in lap top computers, but also in 2-dimensional imaging devices, such as document scanners or in digital X-ray imagers for medical applications.

This paper addresses the new challenges that exist in research and development of TFTs: 1) TFTs on plastic substrates, 2) low-temperature poly-silicon (LTPS) for the pixel TFTs and for row and column drivers on glass; 3) addressing of OLEDs (Organic Light Emitting Diodes) by silicon TFTs. For these advanced applications of TFTs the relevant issues are: (i) higher electron mobility, (ii) stability, and (iii) defect free, uniform deposition of thin silicon films and gate dielectrics at a high deposition rate (for reduced cost). Whereas a high deposition rate is generally needed to reduce the production cost, for novel high current applications the latter two issues have recently become more essential.

At Utrecht University, we are investigating Hot Wire (Catalytic) CVD as a deposition technique for novel TFTs that have a high potential to meet the above mentioned requirements. In Hot Wire CVD, the source gases are catalytically decomposed at heated tungsten or tantalum filaments (~1800 °C), whereas the substrate is kept at a low temperature. Hydrogenated amorphous silicon (a-Si:H) with device quality can be deposited at a high rate of 1-5 nm/s. Bottom gate, inverted staggered TFTs with Hot Wire CVD silicon films have been made with an electron mobility of 1.5 cm^2/Vs, and with field effect characteristics that are completely stable under operating conditions. Top gate, coplanar TFTs with polycrystalline silicon films have been made, showing a mobility of 4.7 cm^2/Vs, in agreement with the Hall mobility measured in individual thin films. This has been obtained without any post deposition treatment, and the Hot Wire technology can thus avoid expensive, time-consuming steps such as the laser recrystallization step that is currently used in the production of the latest poly-Si lap top displays. Hot Wire CVD is also suitable for the deposition of silicon nitride (SiN_x:H) gate dielectrics. TFTs with a Hot Wire silicon nitride gate dielectric, deposited below 400 °C, have reached a mobility of 0.6 cm^2/Vs and a threshold voltage of 2.9 V.

Nanos materialov z metodo vroče žice pri izdelavi tankoplastnih tranzistorjev

Ključne besede: polprevodniki, mikroelektronika, tehnologije žice vroče, CVD nanosi kemični s paro, HWCVD nanosi kemični s paro in žico vročo, naprave upodabljalne, senzorji slik, zasloni slikovni, skenerji, upodabljalniki X-žarkov, TFT transistorji tankoplastni, a-Si:H TFT tehnologije silicija amorfnega hidrogeniziranega za transistorje tankoplastne, zmanjšanje stroškov

Izvleček : Tankoplastni tranzistorji (TFT - Thin Film Transistors) se na široko uporabljajo kot stikalni elementi v aktivnih matrikah (AM - Active Matrix), prikazalnikih na tekoče kristale (LCD - Liquid Crystal Displays), kot npr. pri TFT zaslonih prenosnih računalnikov ali tudi pri dvodimenzionalnih slikovnih napravah kot so skenerji ali x žarkovni upodabljalniki v medicini.

V prispevku obravnavamo nove izzive v razvoju in raziskavah TFT tranzistorjev : 1) TFT tranzistorji na plastičnih substratih, 2) nizkotemperaturni nanos polisilicija (LTPS) za izdelavo točkovnih (pixel) TFT tranzistorjev, oz. za izdelavo krmilnikov vrstic in stolpcev na steklu , 3) krmiljenje OLED diod (OLED - Organic Light Emitting Diodes) s TFT tranzistorji. Za vse te naštete napredne uporabe TFT tranzistorjev so pomembne naslednje njihove lastnosti: i) visoka gibljivost elektronov, ii) stabilnost, iii) enakomeren nanos tankih plasti silicija in dielektrika za krmilno elektrodo brez napak pri visokih hitrostih nanašanja. Visoke hitrosti nanašanja so sicer potrebne za zmanjšanje proizvodnih stroškov, vendar zadnje čase postajata vse bolj pomembna zadnja dva dejavnika predvsem zaradi zahtev po visokih tokovih.

Na Univerzi v Utrechtu raziskujemo tehniko kemičnega nanosa silicija (CVD) z metodo vroče žice, s katero si obetamo doseči vse zgoraj naštete lastnosti TFT tranzistorjev. Pri tej metodi se plini katalitično razgradijo na greti tantalovi ali volframovi nitki (temperatura okoli 1800°C), med tem ko je substrat na nizki temperaturi. Ustrezno kvaliteten hidrogeniran amorfni silicij (a-Si:H) lahko nanašamo s hitrostjo 1 - 5 nm/s. S CVD nanosom z metodo vroče žice smo izdelali TFT tranzistorje z obrnjeno krmilno elektrodo z gibljivostjo elektronov 1.5 cm^2/Vs in z električnimi karakteristikami, ki so bile popolnoma stabilne. Koplanarni TFT tranzistorji iz polikristaliničnega silicija s krmilno elektrodo na vrhu pa so imeli elektronsko gibljivost 4.7 cm^2/Vs, kar je enako Hallovi gibljivosti merjeni v samostojnih tankih filmih. Omenjene lastnosti smo dosegli brez kakršnihkoli dodatnih obdelav, iz česar lahko sklepamo, da se pri CVD nanosu silicija z metodo vroče žice lahko izognemo dragemu in dolgotrajnemu postopku laserske rekristalizacije tanke plasti, ki je trenutno v rabi v proizvodnji najnovejših polisilicijevih zaslonov za prenosne računalnike.

CVD nanos z metodo vroče žice je primeren tudi za nanos dielektrika za krmilno elektrodo iz silicijevega nitrida (SiN_x : H). Tovrstni TFT tranzistorji nanešeni pri temperaturi pod 400°C so dosegli gibljivost elektronov 0.6 cm^2/Vs in pragovno napetost 2.9 V.

1. Introduction

The application of Thin Film Transistors (TFTs) in image sensors and displays is very widespread. Amorphous silicon (a-Si:H) TFT technology has shown to be a mature technology and thus TFTs are widely used for individually switched display elements (pixels) in Liquid Crystal Displays (LCDs) /1/, primarily in portable laptop computers, but also in 2-dimensional imaging devices, such as document scanners or in digital X-ray imagers for medical applications.

In an LCD, the display elements comprise liquid crystals of which the transmissive or reflective optical properties can be altered by electrically charging or discharging them. These elements are arranged in large matrices along with their switching TFTs to form an Active Matrix Liquid Crystal Display (AMLCD). Although the mobility of a-Si:H TFTs is quite low (≈ 1 cm^2/Vs), these TFTs are very suitable as the pixel switches in AMLCDs, since they can be fabricated over large areas (so that displays with > 15" diameter are no longer an exception), with high yield, and showing very uniform performance, while the low mobility is amply sufficient to charge the pixels within the row addressing time. A possible drawback of a-Si:H TFTs is the threshold voltage shift after prolonged applied bias to the gate electrode. Given the high quality of the currently available gate dielectrics, this effect has been proven to be an intrinsic property of a-Si:H rather than charge trapping in the gate dielectric /2/. Nevertheless, the threshold voltage shift is not an issue in AMLCDs, since the total integrated duration of applied bias to each transistor ("ON time") over the life of a display is too short to produce any significant threshold voltage shift. The duty cycle is very short, because the pixels can be charged within a very short time and the TFT is switched back to the OFF condition once a pixel is charged.

2. Requirements to TFTs

2.1 Mobility

Although a-Si:H TFTs are used in mass-produced displays and sensor arrays, new challenges to this field have surfaced recently. The performance of very high-resolution displays is mainly determined by the electron mobility of the pixel TFTs. This is one reason why TFTs with higher mobility would have advantages. Further, one would like to avoid the need for external IC mounting of the row and column drivers. For on-glass peripheral driver circuitry integration, a higher carrier mobility of TFTs is required. For driver circuitry, n-channel and p-channel TFTs are required. This would enable Complementary Metal-Oxide-Semiconductor (CMOS) circuits, which would make low-power (< 1 mW) on-glass drivers possible and, consequently, the displays could become extremely flat. For row drivers a mobility of 10 cm^2/Vs is amply sufficient and for column drivers the mobility would need to be 100 cm^2/Vs /3/. Using multiplexed row and column drivers however, just a moderate improvement of the mobility of TFTs would already be sufficient /4/ while the number of interconnects could already be greatly reduced. For driver TFTs the stability, in addition to the mobility, becomes an issue.

2.2 Stability

The stability of the devices has again become an important issue in the following technology fields. *(i) Low-temperature deposited Thin Film Transistors on polymer substrates* /5,6/. Such low-temperature deposited matrices of TFTs could ultimately be made by roll-to-roll production and be used in curved consumer products, such as mobile phones, and in rollable "electronic paper". The maximum processing temperature that can be used on, e.g., transparent polyethylene terephthalate (PET) is ≈ 150 °C. *(ii) TFTs that are used in multiplexed drivers*. In such driver circuits, TFTs have a high duty ratio (i.e., the ON time is long compared to the OFF time) implying prolonged gate bias stress conditions. The threshold voltage shift that results from such prolonged gate bias conditions would lead to a too short life of the driver circuitry. *(iii) TFTs for the addressing of Organic Light Emitting Diodes (OLEDs)*. When OLED displays become large (i.e., laptop size), *active* matrix addressing (AMOLEDs) is required in order to reduce the power losses due to capacitive charging, which is a problem in *passive*-matrix addressed OLEDs. In contrast to the pixel switching scheme in *charge-driven* LCDs, the *current-driven* LED pixels have to be addressed in a *constant current* mode, which means that the switching transistors remain in the ON state as long as the pixel is required to be ON. Therefore, the TFTs have to be capable of enduring orders of magnitude longer durations of applied bias and should therefore be essentially stable.

2.3 Cost reduction

The solution to mobility and stability issues is often found by the introducing poly-Si TFTs. At present, these TFTs are already used in finer pitched displays, such as in the high quality segment of avionics products or in projection displays. In small size display panels, poly-Si TFTs are in use in the driver ICs as well as in the switching transistors /7/. These TFTs always have a top gate structure as this has the advantage that they can be structured using self-aligned photolithographic definition. The challenge in this segment is to produce poly-Si at a low temperature (LTPS; Low Temperature Poly-Silicon), so that inexpensive and larger substrate plates can be used.

One of the approaches to LTPS is to deposit amorphous or microcrystalline thin films that which are subsequently (re-)crystallized. The common crystallization techniques are furnace annealing (Solid Phase Crystallization; SPC) /8/, rapid thermal annealing (RTP) with lamps /9/, and excimer laser annealing /10/. For glass substrates, furnace annealing is restricted to temperatures < 600 °C due to the softening point of commonly used glass (Corning 1737) and is therefore a method that is very time consuming (in excess of 10 hours). In excimer laser annealing, the short

wavelength (308 nm for a XeCl laser) and the short pulse duration (20 -200 ns) promotes rapid melting and fast solidification. This, in principle, enables the use of substrates that are not resistant to high temperatures, such as glass and plastic foil.

The base materials for laser recrystallization are either made with Low Pressure Chemical Vapor Deposition (LPCVD) /11/ or with Plasma Enhanced CVD (PECVD) /12/. In the latter case, while PECVD allows for a lower deposition temperature, the recrystallization is actually a two-step process or even a three-step process. It is required to dehydrogenate the film (e.g., at 450 °C for 1 hour) in order to prevent explosive outgassing of hydrogen from the film leading to delamination. After completion of the TFTs, an rf hydrogen plasma (for several hours) is needed to passivate defects, reduce leakage currents, and to enhance the electron mobility. The multitude of complicated processing steps with a long duration that are associated with laser annealing is not straightforwardly compatible with the requirement of a throughput of one plate per minute in the single-substrate processing tools currently employed in the fabrication of AMLCDs /13/. Further, there are problems with the homogeneity of the performance of TFTs over large area substrates due to pulse-to-pulse energy fluctuations and the energy distribution in the beam /10/. This results in mobility and threshold voltage variations in the TFTs, which cause unacceptable non-uniformity in display brightness.

Direct deposition of poly-Si TFTs is of interest for obtaining uniformity over large area and for reducing the manufacturing costs. Early results obtained using catalytic chemical vapor dissociation (Cat-CVD) of SiH_4 gas at a hot tungsten wire and deposition of the reactants on a substrate held at 300 °C resulted in thin films with a Hall mobility of 10 cm^2/Vs /14/. Subsequently, a report appeared on TFTs that were deposited on a thermally-grown SiO_2 gate dielectric and had a remarkably high optimum in the field effect mobility of 70 cm^2/Vs /15/. Microcrystalline films can also be made using the Layer-by-Layer (LBL) variant of radio frequency (rf) Plasma Enhanced CVD (PECVD) /16/, leading to a mobility of 0.6 cm^2/Vs in TFTs. The Princeton group recognized that fluorinated silane promotes crystallization in PECVD of thin layers /17/ and produced 50 nm thick TFTs with an electron mobility of 10 cm^2/Vs /18/. Although the deposition rate is only 0.5 Å/s, the deposition time of the active layer could be limited to 15 min, because only a small thickness was required.

Recent results on large area deposition include the achievement of a thickness uniformity of +/- 2.5 % on 20 cm x 20 cm at the University of Kaiserslautern /19/ and a uniformity of +/- 7.5 % on substrates as large as 40 cm x 96 cm, using a novel showerhead design, at Anelva Corporation in Japan /20/.

3. Hot Wire CVD

At Utrecht University, we are investigating two deposition techniques for the fabrication of TFTs: Plasma Enhanced CVD in the Very High Frequency domain (VHFCVD) /18c/ and Hot Wire (Catalytic) CVD. This paper will discuss Hot Wire CVD only; for results obtained with VHFCVD we refer to Ref. 21.

In Hot Wire CVD, the source gases are catalytically decomposed at heated tungsten or tantalum filaments (~1800 °C), whereas the substrate is kept at a low temperature.

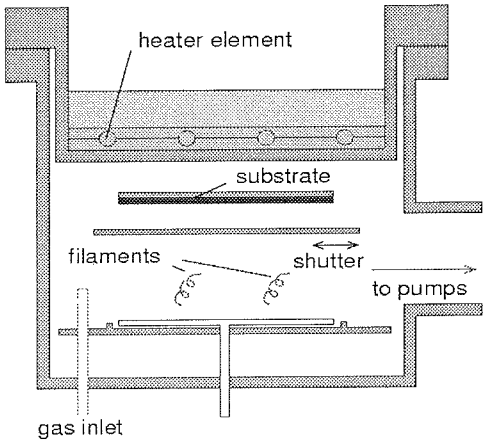

Fig. 1: *Schematic cross section of a Hot Wire deposition chamber.*

Figure 1 shows a schematic cross section of a Hot Wire deposition chamber at Utrecht University. It basically contains a substrate holder, a shutter, a hot wire assembly, a gas inlet, and a pump port. The substrate holder is optionally heated with an external heater. One or multiple filaments are located at 3 - 8 cm from the substrate. The gases flow perpendicular to the length of the filaments. In contrast to the conventional PECVD technique, no ions are created: though the hot filament emits a considerable electron current, the energy of these electrons is generally too low to cause impact ionization. At our laboratory, two Hot Wire deposition chambers are connected to one of our multichamber ultrahigh vacuum (UHV) systems. This offers the opportunity to create geometry and deposition parameters optimized for two types of intrinsic layers: amorphous and micro/polycrystalline silicon. Hydrogenated amorphous silicon (a-Si:H) films are obtained using 100 % silane (SiH_4), whereas polycrystalline silicon films are made using mixtures of hydrogen (H_2) and silane (SiH_4) gases with a flow ratio of 10 to 15. As a result of systematic and careful optimization procedures we have chosen different substrate-to-wire distances, different wire temperatures, and even different wire materials for a-Si:H and poly-Si:H deposition, respectively (see Table 1).

There are two issues of concern in HWCVD, which have been addressed recently: (1) *Breakage of the wires*. This can be avoided by preventing excessive silicide formation. This is prevented by avoiding high concentrations of silane near the points where the wire is relatively cool /20/. The life of the wire can be further lengthened by an appropriate annealing treatment with H_2 gas prior to deposition;

(2) *Metallic contamination of the films*. This is avoided under normal operating conditions. For instance, for depositions using a W wire at temperatures between 1800 - 2000 °C, it has been verified from SIMS measurements that the tungsten concentration in the deposited films is less than 10^{16} cm^{-3}.

Parameter	Poly-Si:H	a-Si:H
Wire material	W	Ta
$d_{substr-wire}$	40 mm	50 mm
T_{wire}	1800°C	1700°C
T_{sub}	500°C	250°C
Dilution ratio H_2/SiH_4	15	1
Pressure (mbar)	100	20
Deposition rate (Å/s)	5	10
Band gap (eV)	1,1	1,8
Activation energy (eV)	0,55	0,8
Photo-/dark conductivity ratio	10^2	10^6

Table 1: *Key deposition parameters and materials properties of the two intrinsic absorber layers*

At present, high quality amorphous silicon films can be deposited at a rate between 10 and 50 Å/s and micro- or polycrystalline silicon films at a rate between 5 and 20 Å/s. Using pure SiH_4 at a substrate temperature of 430 °C, our best material has an ambipolar diffusion length of 260 nm and is deposited at a rate of 18 Å/s. The hydrogen content is 8 at.-%, leading to an optical (Tauc) band gap of 1.70 eV. The first a-Si:H TFTs made with this material immediately showed that the HWCVD technique leads to very stable devices /22/.

Polycrystalline or microcrystalline silicon materials are typically obtained using dilution of the SiH_4 with H_2. We distinguish two main types of poly-Si:H. Type 1 has random oriented small crystals (denoted as *Poly1*) and type 2 has columnar, strongly oriented (220) crystals (denoted as *Poly2*). The random-oriented *Poly1* is obtained at high H_2 dilution of the silane. These layers are quite porous and are subject to bulk post oxidation if not shielded by a capping layer. They are useful because they typically show *immediate* nucleation on *any* kind of substrate. The deposition rate is relatively low (1 Å/s). The columnar-oriented Poly2 is obtained at moderate H_2 dilution and at a higher deposition rate (5 - 10 Å/s). This deposition rate is comparable to the highest deposition rates available for device quality μc-Si:H by VHFCVD /23,24/.

Poly2 has unique properties, such as a very intrinsic nature (oxygen levels down to 3 x 10^{18} cm^{-3}) and a very high compactness, due to good coalescence of the crystals /25/. The latter is illustrated by (i) SiH stretching mode IR absorption only at 2000 cm^{-1}, typical for isolated SiH bonds, (ii) H effusion only at 550-650 °C, (iii) low ESR spin density at 7 x 10^{16} cm^{-3}, and (iv) low activation energy of the Hall mobility (0.012 eV) /26/. The intrinsic nature of the material is also illustrated by the midgap position of the Fermi-level at 0.54 eV, as deduced from temperature dependent dark conductivity (σ_d) measurements. The value of s_d at room temperature is also low, at 1.5 x 10^{-7} $\Omega^{-1}cm^{-1}$. This helps in achieving low leakage currents in TFTs. The hydrogen content in *Poly2* films is only 0.5 at.-%. The compactness makes these films very suitable as capping layer against penetration of oxygen and water vapor. Typically, the *Poly2* growth regime shows an incubation time leading to amorphous or heterogeneous nature near the substrate interface during the first ≈ 50 nm.

3.1 Mobility

We applied the *Poly2* growth regime to the preparation of high quality bottom gate TFTs as well as top gate TFTs. The presence of an incubation layer, however, prevents the achievement of typical "polysilicon-like" behavior and therefore these TFTs behave predominantly "amorphous-like", along with the high ON/OFF ratio that is typical for amorphous silicon TFTs. Nevertheless, these TFTs showed an electron mobility of 1.5 $cm^2V^{-1}s^{-1}$ /27/, which is higher than that of conventional amorphous TFTs. Moreover, the I-V characteristics were remarkably stable /28/, which will be elucidated in the next subsection.

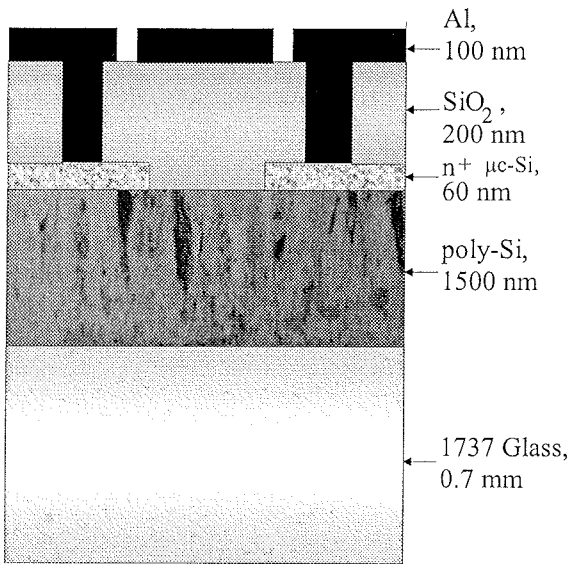

Fig. 2: *Schematic cross section of the top gate TFT structure.*

To investigate the mobility potential of as-deposited polysilicon layers made by HWCVD, Utrecht University and S. Wagner's group at Princeton University have fabricated *top gate* TFTs using the above *Poly2* layer. In the top gate configuration, the conducting channel is near the surface of the layer. Fig. 2 shows a cross section of the *top gate* structure. Since the crystals extend conically in the growth direction, the size of the crystals increases from the substrate to the film surface and hence it was expected that

the electron mobility at the top of the layer would be higher /29/ (for a film thickness of 1.5 μm).

The transfer characteristics at 0.1 V (linear regime) and 10 V (saturated regime) are shown in Fig. 3. It can be seen that at the lowest V_{ds} the drain currents are suppressed. This is possibly due to a small barrier at the source and drain contacts. At V_{ds} = 10 V, the currents are not limited by the contacts. Here, the ON current is 4.8 x 10^{-5} A and the OFF current is 7.5 x 10^{-11} A. Such a low OFF current is not usually obtained for poly-Si TFT. The subthreshold slope $S = \partial V/\partial(\log_{10} I_d)$ is 1.5 V/decade and the threshold voltage V_{th} is 8.0 V. The mobility in the saturated regime is calculated from the slope of the square root of I_d versus V_g measured at V_d = 10 V (for V_g < 15 V) and amounts to 4.0 $cm^2V^{-1}s^{-1}$. The maximum field effect mobility that was obtained is 4.7 $cm^2V^{-1}s^{-1}$.

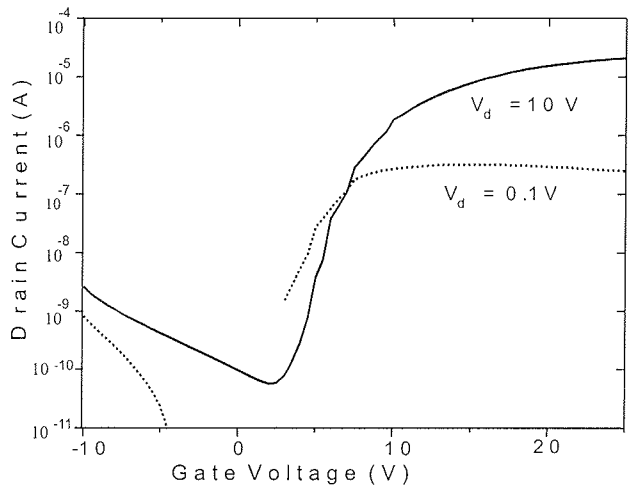

Fig. 3: The transfer characteristics at 0.1 V (linear regime) and 10 V (saturated regime) of a HWCVD poly-Si:H TFT

The transistor parameters are fully consistent with the individual thin film properties: the OFF current is in agreement with the dark conductivity of the *Poly2* layer and the field effect electron mobility is similar to the result of the Hall measurement, which was 5 $cm^2V^{-1}s^{-1}$. The mobility is also consistent with the mobility determined from Time-Resolved Microwave Conductivity (TRMC) measurements performed on the same layers, showing an electron mobility of 4 to 5 $cm^2V^{-1}s^{-1}$ /30/. In the TMRC technique, short wavelength pulsed laser illumination of the top surface was used to probe the mobility of the corresponding channel region of the TFT. The lateral current flow does not experience noticeable barriers due to crystal boundaries (consistent with the low activation energy of the Hall mobility of 12 meV).

In addition to this 1.5 μm film, we investigated the effect of a reduced thickness of the silicon film on the TFT characteristics. We employed 750 nm and 300 nm thick films. The results are shown in Table 2. *Top-gate* TFTs with films have reduced electron field effect mobility.

Thickness (nm)	V_{th} (V)	ON/OFF ratio	mobility ($cm^2V^{-1}s^{-1}$)
300	12	30	1.1 x 10^{-3}
750	6	2 x 10^5	1.5
1500	8	4 x 10^5	4.0
1500	9.5	6 x 10^5	4.7

Table 2: Summary of the HWCVD poly-Si TFT characteristics for three thicknesses of the silicon film on Corning 1737 glass. The threshold voltages and mobilities are taken in the saturated regime. The ON and OFF current are taken at V_{ds} = 10 V, and V_g = 25 V and 0 V, respectively.

For the thinnest film of 300 nm, the characteristics are very poor. It is interesting to note that the same thin films, implemented in *bottom gate* TFTs, yield an electron mobility of 1.5 $cm^2V^{-1}s^{-1}$. In those TFTs, the channel region is amorphous, due to the incubation stage that *Poly2* requires for the crystals to develop. Thus the reason for the poor mobility for the 300 nm thick *top gate* TFT is most likely the fact that the amorphous and crystalline phases at this stage of the growth are mixed in an unfavorable volume ratio, leading to local porosity, poor carrier transport between isolated grains (low mobility values) and a Fermi level that is pinned by the intergrain defect density (small ON/OFF ratio).

3.2 Stability

We studied the defect creation under prolonged bias voltage stress in TFTs based on silicon deposited by HWCVD and compared them with state-of-the-art devices prepared by PECVD. Purely amorphous as well as heterogeneous silicon conducting channel regions, incorporating a small fraction of crystallites, were exposed to the gate bias stress. A gate bias voltage of 25 V was applied at temperatures between 40 °C and 100 °C for periods between 10 s and 5 x 10^5 s. For the analysis of the data we used the thermalization-energy concept /31,32/ and we fitted stretched hyperbola functions to the relative threshold-voltage shift ΔV_{th}^{rel} versus the thermalization energy E_{th}

$$\Delta V_{th}^{rel} = (V_t - V_t^{ini})/(V_g - V_t^{ini}) = 1 - (\exp[(E_{th} - E_A)/k_BT_0] + 1)^{-1/(\alpha-1)}, \quad (1)$$

where

$$E_{th} = k_BT \cdot \ln(\nu t). \quad (2)$$

It is noteworthy that, although this concept was developed for a-Si:H TFTs, it appears to be equally well applicable to heterogeneous or microcrystalline silicon. Fig. 4 shows the relative threshold shift versus E_{th}.

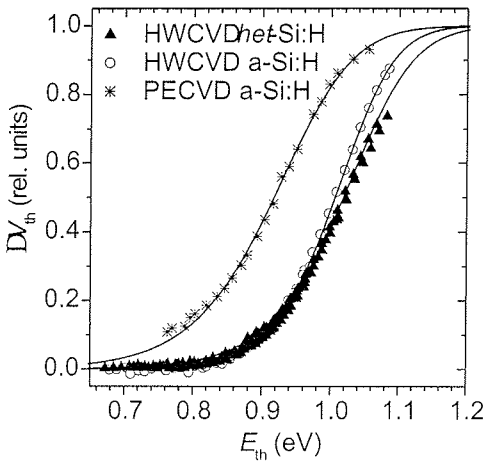

Fig. 4: Measured and fitted relative threshold voltage shift of PECVD a-Si:H and HWCVD silicon TFTs versus thermalization energy.

For HWCVD a-Si:H TFTs the fits resulted in E_A = 1.052 eV, which is high compared to the E_A value of 0.977 eV for the reference PECVD TFT. For the TFT with the heterogeneous material in the channel, which is the result of the initial growth under *Poly2*-type deposition conditions, the E_A value is even better than for the HW a-Si:H TFT, namely 1.073 eV. For this TFT the mobility was 1.18 cm^2/Vs. This demonstrates the superior stability of TFTs using HWCVD deposited silicon for the channel layer /33/.

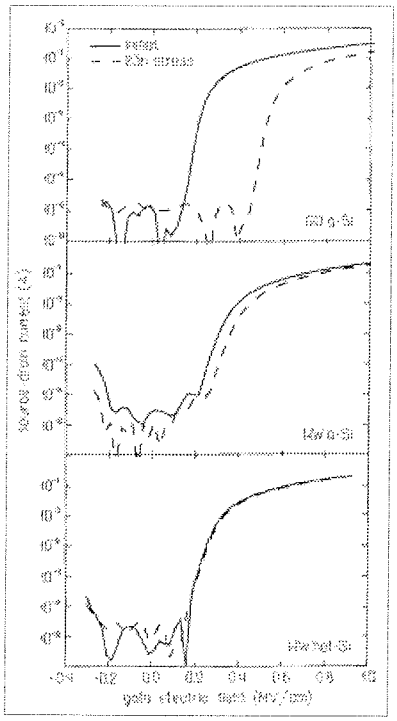

Fig. 5: Transfer characteristics of a PECVD a-Si:H TFT, a HWCVD a-Si:H TFT, and a HWCVD heterogeneous silicon TFT. The solid curves are the initial characteristics and the dashed curves are taken after 23 h of continuous stress at room temperature.

The improved stability is made more clearly visible by showing a snapshot of the I-V transfer characteristics for the three TFTs at an equal stressing dose of 23 h of continuous stress at room temperature. Fig. 5 shows the characteristics for initial and stressed conditions. Whereas the PECVD TFT shows a ΔV_{th} as high as 6.2 V, the HWCVD a-Si:H TFT shows a ΔV_{th} of only 0.9 V and the HWCVD with the heterogeneous silicon channel shows virtually no shift at all.

As all hot-wire TFTs have a better stability than state-of-the-art PECVD devices, these TFTs have the potential to fulfill the requirements for application as the pixel TFTs in AMOLEDs and as the driver TFTs in AMLCDs.

3.3 Cost reduction

The cost of manufacturing AMLCDs is determined, among others, by the thermal budget of the process (via the cost of heat-resistant substrates), the number and duration of processing steps (such as annealing and defect passivation steps), the complexity of the processes (which influences the yield), the cost of equipment (such as laser-annealing equipment), and the throughput. As Hot Wire CVD has already demonstrated that highly stable, high mobility TFTs can be produced, this technology, due to its large area capability, high deposition rates, and simplicity, can contribute greatly to cost-effective manufacturing of active matrices of TFTs. The potential contribution to cost reduction would even be large if both the channel material and the gate dielectric could be made with the same technique. For this reason we have also ventured the demonstration of "all-hot-wire" TFTs.

A HWCVD silicon nitride (SiN_x:H), that is suitable as the gate dielectric in bottom gate TFTs, has recently been developed in our lab /34/ as well as in Matsumura's lab /35/. For the deposition of HWCVD SiN_x gate dielectrics we used a mixture of ammonia (NH_3) and silane. The substrate temperature was kept below 400 °C.

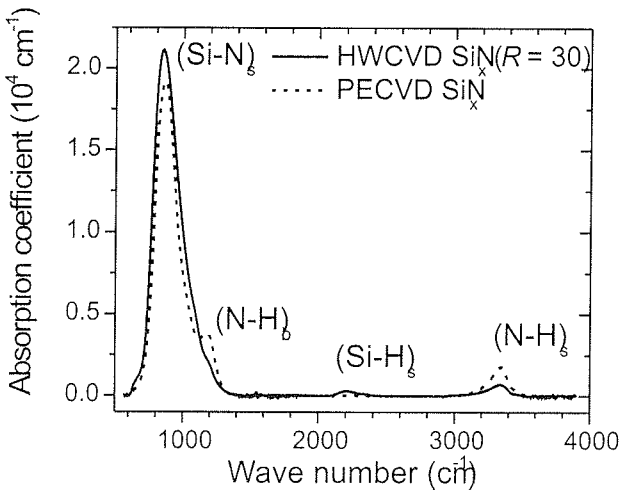

Fig. 6: Infrared absorption spectrum of a HWCVD and a PECVD SiN_x:H layer.

The composition can be tuned over a wide range by varying the SiH_4/NH_3 gas flow-rate ratio. We used a flow-rate ratio of R = 30 - 60 at a pressure of (8 - 15) x 10^{-3} mbar. The filament temperature was 1900 °C. The substrate temperature was 340 °C. A high breakdown field (> 5 MV/cm) and a high electrical resistivity (> 10^{15} Ωcm) have been achieved. Fig. 6 shows the FTIR absorption spectrum of HWCVD SiN_x deposited with R = 30. For comparison the spectrum of typical nitrogen-rich PECVD SiN_x deposited at a substrate temperature of 400 °C /34/ is also shown in this Figure. The composition of HWCVD SiN_x was measured with Elastic Recoil Detection (ERD). We determined x = N/Si = 1.35 ± 0.05, which is near to the value of x = 1.33 for stoichiometric Si_3N_4. In the semiconductor industry, Si_3N_4 is conventionally deposited by LPCVD at a high temperature of ~ 800 °C and therefore it cannot be applied to glass or plastic substrates. The hydrogen content of our films is (10 ± 1) at.-%. This is very low compared to the 22 at.-% present in the PECVD SiN_x sample. In the case of the PECVD SiN_x the hydrogen is bonded to N only, apparent in the N-H stretching mode at 3340 cm^{-1} and the N-H bending mode at 1180 cm^{-1}. The HWCVD layer, on the other hand, also shows a contribution from $Si-H_x$ stretching at 2100 - 2300 cm^{-1}. A refractive index of 1.95 ± 0.02 and a band gap of E_{04} = 4.2 ± 0.1 eV (energy where the absorption coefficient is 10^4 cm^{-1}) was determined by spectroscopic ellipsometry. The relatively low bandgap (E_{04} ~ 5 eV for the PECVD SiNx) and the presence of the $Si-H_x$ mode in the FTIR spectrum indicate that the SiN_x network contains a considerable fraction of Si-Si bonds and, thus, Si dangling bonds, may act as charge-trapping centers as in case of PECVD SiN_x /36/.

TFTs with a PECVD channel layer and a Hot Wire silicon nitride gate dielectric, have reached a mobility of 0.6 cm^2/Vs and a threshold voltage of 2.9 V. 'All-hot-wire' TFTs with both layers made by HWCVD have reached a mobility of 0.3 cm^2/Vs and a threshold voltage of 4.0 V /37/. Although more development work is needed to improve the compatibility between the two layers, it is thus demonstrated that the TFTs can in principle be made using a single process.

4. Conclusion

We have addressed the current issues in the development of TFTs for AMLCDs or AMOLEDs and grouped them in the categories mobility, stability, and cost. With reference to these issues we have discussed the potential of Hot Wire CVD for the fabrication of thin film amorphous, micro-, or polycrystalline silicon channel materials and silicon nitride dielectrics. Although there are still large challenges in the further development of the Hot Wire CVD technique, its simplicity makes it a very favorable technique for the formation of the active layers of TFT matrices and driver circuits.

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