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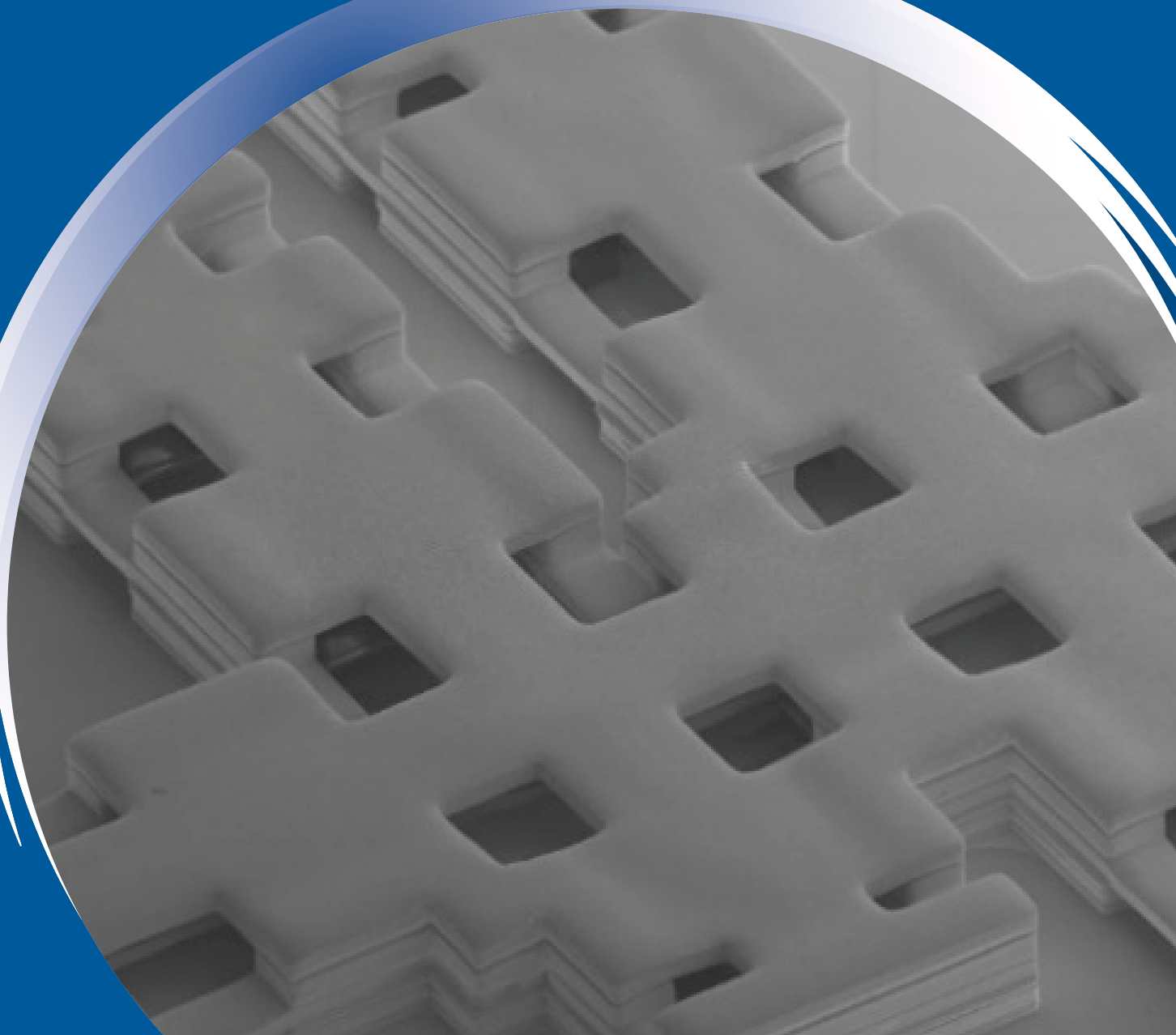

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# Design of a New MISO Mixed-Mode Universal Biquad OTA-C Filter in 130nm CMOS Technology

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**Abstract:** This paper presents the design of a MISO (multiple-input single-output) universal biquad filter in 130 nm CMOS UMC technology. The proposed filter consists of three operational transconductance amplifiers (OTAs), two grounded capacitors and one inverter stage. The topology, which has three inputs and one output, operates in all modes: voltage, transconductance, current, and transresistance. In addition, the filter generates all types of transfer functions (LP, HP, BP, BS, and AP). First, the filter topology with an inverter at the output is designed and analyzed in detail. Next, an improved topology with a differential amplifier as the output stage is proposed. The designed filter has a cutoff frequency of approximately 250 MHz and a current consumption of 4.5 mA. The impact of process, temperature, and voltage variations is examined through corner analysis.

**Keywords:** universal biquad filter, operational transconductance amplifier, OTA-C filter, analog IC design

# Oblikovanje novega MISO univerzalnega biquad OTA-C filtra z mešanim načinom v 130 nm tehnologiji CMOS

**Izvleček:** V tem članku je predstavljena zasnova univerzalnega biquad filtra MISO (multiple-input single-output) v 130 nm tehnologiji CMOS UMC. Predlagani filter je sestavljen iz treh operacijskih transkonduktančnih ojačevalnikov (OTA), dveh ozemljenih kondenzatorjev in ene inverterske stopnje. Topologija, ki ima tri vhode in en izhod, deluje v vseh načinih: napetostnem, transkonduktančnem, tokovnem in tranzistorskem. Poleg tega filter ustvarja vse vrste prenosnih funkcij (LP, HP, BP, BS in AP). Najprej je zasnovana in podrobno analizirana topologija filtra z inverterjem na izhodu. Nato je predlagana izboljšana topologija z diferencialnim ojačevalnikom kot izhodno stopnjo. Zasnovani filter ima mejno frekvenco približno 250 MHz in porabo toka 4,5 mA. Vpliv procesnih, temperaturnih in napetostnih sprememb je preučen z analizo vogalov.

**Ključne besede:** univerzalni biquad filter, operacijski transkonduktančni ojačevalnik, filter OTA-C, MISO, zasnova analognih integriranih vezij

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## 1 Introduction

Analog active filters are essential building blocks for various analog signal processing systems. The design of second-order or biquad universal filters, which provide all five filtering responses, low-pass (LP), band-pass (BP), high-pass (HP), all-pass (AP), and band-stop (BS), has been shown to be appealing in recent years. OTA-C or OTA-Gm universal filters are advanced analog filters capable of achieving versatile filtering functions [1]. They are highly valued for their ability to realize multiple filter responses within a single circuit configuration [2]. OTA-C filters offer several advantages, including low power consumption, wide frequency range operation, and the ability to operate in various signal modes (voltage, current, transresistance, and transconductance) [2]. They are particularly useful in applications requiring compact, efficient, and reconfigurable filtering solutions, such as biomedical devices, communication systems, and sig-

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nal processing circuits [2]. The design of OTA-C universal filters involves optimizing various parameters, such as sensitivity, frequency performance, parasitic effects, dynamic range, noise, low-voltage operation, power consumption, and chip area [1]. By carefully selecting the constituent devices and filter structure, OTA-C filters can achieve high performance and reliability in integrated circuit applications [1].

There are several types of universal OTA-C filters. One notable example is the single-input multiple-output (SIMO) universal OTA-C filter. These filters can manage multiple outputs from a single input signal, using OTAs and capacitors to perform various filtering functions [3]. Paper [3] introduces a universal SIMO filter composed of eight OTAs and two grounded capacitors. This filter has five outputs, enabling the realization of different filter functions in voltage mode. It achieves a center frequency of 2.89 MHz and a quality factor of 1.

Paper [4] presents a universal multiple-input multiple-output (MIMO) filter. The circuit consists of eight single-ended OTAs and two grounded capacitors. It can operate as a two-input and four-output filter or a three-input and single-output filter. The quality factor can be adjusted using capacitors, while the center frequency can be controlled with the OTA's transconductance without disturbing the quality factor. The filter achieves a center frequency of 2.89 MHz and a quality factor of 1.

Paper [5] introduces a multiple-input, single-output (MISO) universal OTA-C filter. This filter contains six OTAs and two grounded capacitors. It operates in voltage mode with four inputs and one output. The quality factor can be adjusted without affecting the center frequency.

Paper [6] presents a universal active MISO filter employing three OPAs, two capacitors, and seven resistors. This filter is capable of realizing three filter functions: BP, LP, and HP. It features one input and four outputs. The inclusion of resistors contributes to a more complex design compared to OTA-C filters. In contrast, filters [3]-[5] offer additional functionalities, including BS and AP functions, demonstrating their superior versatility.
Two additional topologies are presented in [7]. Both topologies operate in mixed-mode regimes (voltage, current, transconductance and transresistance mode) and can realize all filter functions from a single topology. The first proposed circuit consists of four OTAs and two grounded capacitors, while the second topology contains five OTAs and two grounded capacitors. The center frequency is 1.59 MHz.

Paper [8] introduces a mixed-mode universal MISO OTA-C filter. The circuit consists of six single-output and one dual-output OTA in combination with two grounded capacitors. This filter can realize all filter functions and can be driven with voltage or currents. It offers the ability to adjust the center frequency and quality factor independently. Two working modes (current and voltage) are presented.

Paper [9] presents a voltage-mode MISO OTA-C filter. This filter uses five single-output OTAs and two grounded capacitors and can realize all filter functions. The MIMO filter described in paper [10] consists of four OTAs, two grounded capacitors, and one resistor.

This paper builds upon a universal MISO biquadratic filter presented in [11] that operates in all four modes and realizes all five filter functions. This topology employs a minimal number of active and passive components to realize a mixed-mode universal biquad OTA-C filter, resulting in reduced area and power dissipation. The main issue in this approach is the high sensitivity of the output inverter stage to process, voltage, and temperature (PVT) variations, which causes changes in the inverter characteristics and the DC output voltage. This can be seen as significant fluctuation of the filter response in the current and transconductance modes. This paper addresses this challenge comprehensively and proposes a new topology using a simple OTA instead of the inverter. The circuit uses only three additional transistors while significantly reducing sensitivity to PVT variations. In addition, the filter center frequency has been considerably increased compared with the results presented in [11].

The rest of the paper is organized as follows: Section 2 describes in detail the proposed filter topology, its building blocks, and enhancements. The post-layout simulation results, including the corner analysis, are presented in Section 3. Section 4 provides a summary of the paper's main conclusions.

## 2 Proposed filter topology

The initial MISO multi-mode universal biquad OTA-C filter topology, with the minimum number of active and passive components [11], is shown in Figure 1. The filter comprises four amplifier stages and two grounded capacitors; the first stage is an OTA with two inputs, the second and third stages are OTAs with four inputs, and the final stage is an inverter (used as a transconductance amplifier).

This filter has one output and three inputs: $V_1$, $V_2$, and $V_3$ in voltage and transconductance mode and $I_1$, $I_2$, and $I_3$ in the current and transresistance mode. $V_{out}$ repre-

sents the voltage and transresistance mode output, while $I_{out}$ represents the current and transconductance mode output. The inverter is essential for the current and transconductance modes.

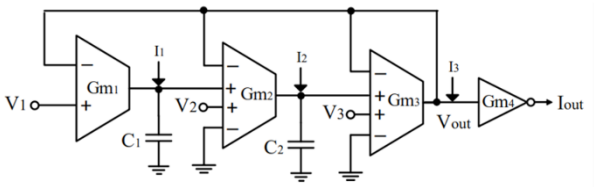


**Figure 1**: The filter topology proposed in [11]

The first filter stage consists of differential OTA, as shown in Fig. 2 [12]. The second and third stages are OTAs with four inputs (two pairs of differential input), Fig. 3 [11]. The initial filter uses a standard CMOS inverter circuit, Fig. 4.

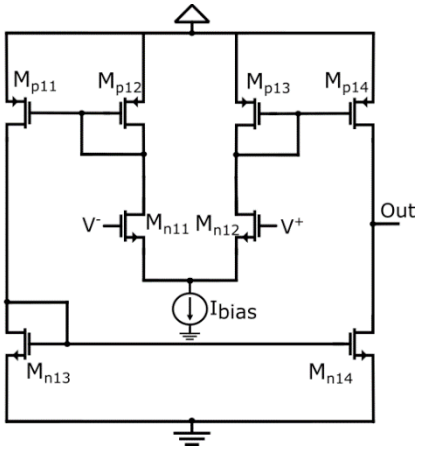


**Figure 2:** The first filter stage – differential OTA [11]

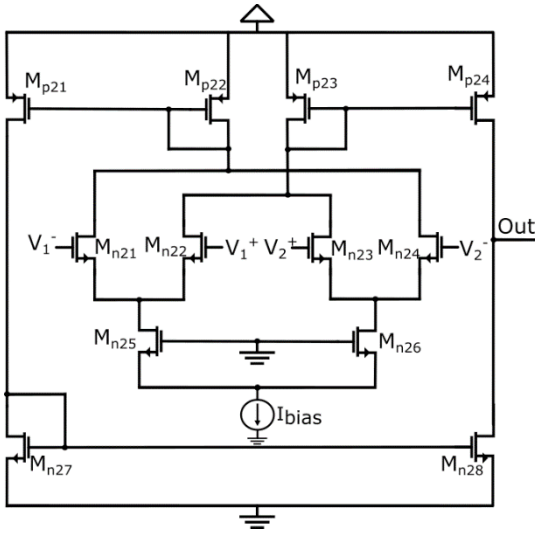


**Figure 3:** The second and third filter stage – OTA with four inputs [11]

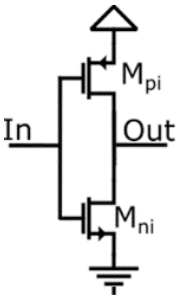


**Figure 4:** The filter output stage: inverter [11]

The filter transfer function in the voltage mode is as presented in [11]

$$V_{out} = \frac{Gm_1Gm_2(V_1)}{D(s)} + \frac{SC_1Gm_2(V_2)}{D(s)} + \frac{S^2C_1C_2(V_3)}{D(s)} \quad (1)$$

The filter transfer function in the current mode is as described in [11]

$$I_{out} = -\left(\frac{Gm_2Gm_3Gm_4(I_1)}{D(s)} + \frac{SC_1Gm_3Gm_4(I_2)}{D(s)} + \frac{S^2C_1C_2(I_3)}{D(s)}\right). \quad (2)$$

The filter transfer function in the transresistance mode is as presented in [11]

$$V_{out} = \left(\frac{1}{Gm_3}\right)\left(\frac{Gm_2Gm_3(I_1)}{D(s)} + \frac{SC_1Gm_3(I_2)}{D(s)} + \frac{S^2C_1C_2(I_3)}{D(s)}\right). \quad (3)$$

The filter transfer function in the transconductance mode is as defined in [11]

$$I_{OUT} = -\left(\frac{Gm_1Gm_2Gm_4(V_1)}{D(s)} + \frac{SC_1Gm_2Gm_4(V_2)}{D(s)} + \frac{S^2C_1C_2Gm_4(V_3)}{D(s)}\right). \quad (4)$$

The polynomial in the denominator is represented by

$$D(s) = S^2C_1C_2 + SC_1Gm_2 + Gm_1Gm_2. \quad (5)$$

The quality factor is given by [11]

$$Q = \sqrt{\frac{C_2Gm_1}{C_1Gm_2}}. \quad (6)$$

The center frequency is described by [11]

$$\omega_0 = \sqrt{\frac{Gm_1Gm_2}{C_1C_2}}. \quad (7)$$

By examining Equations (6) and (7), it can be observed that both the center frequency and the quality factor are determined by the same parameters (transconductances and capacitances). If the transconductances are of equal value ($G_{m1} = G_{m2} = G_m$), the center frequency can be ad-

justed by changing the transconductance values without affecting the quality factor (see Equations (8) and (9)).

$$Q = \sqrt{\frac{C_2}{C_1}} \tag{8}$$

$$\omega_0 = G_m \sqrt{\frac{1}{C_1 C_2}} \tag{9}$$

The filter realizes various transfer functions (LP, BP, HP, BS, and AP) in four different modes, as presented in Table 1. Additional details about the transfer functions and modes can be found in [11]. This filter topology faces challenges related to PVT variations in transconductance and current modes. Detailed analysis has shown significant fluctuations in the inverter output DC voltage during corner analyses, resulting in substantial gain variation. These changes considerably affect the filter characteristics in the current and transconductance modes. Therefore, this paper proposes a modified topology, as shown in Fig. 5. The final stage ($G_{m4}$) is replaced by a simple OTA circuit or a standard differential amplifier with a current source as the load, operating in unity feedback, Fig. 6. The complete biasing circuit, which provides the biasing (reference) currents for all filter stages, is shown in Fig 7. It is based on the self-biasing reference presented in [14] and includes additional current mirrors, consisting of transistors $M_4$–$M_7$, which generate the biasing currents, $I_{bias1}$, $I_{bias2}$, $I_{bias3}$, and $I_{bias4}$, for the filter stages. The proposed filter topology employs three more transistors than the initial circuit but substantially improves the sensitivity of the filter (see the post-layout simulation results in the following section).

**Table 1:** The filter frequency response in different modes [11]

| Filter type | Mode | | | | | |
|---|---|---|---|---|---|---|
| (noninverting) | Voltage | | | Transresistance | | |
| | $V_1$ | $V_2$ | $V_3$ | $I_1$ | $I_2$ | $I_3$ |
| LP | $V_{in}$ | 0 | 0 | $I_{in}$ | 0 | 0 |
| BP | 0 | $V_{in}$ | 0 | 0 | $I_{in}$ | 0 |
| HP | 0 | 0 | $V_{in}$ | 0 | 0 | $I_{in}$ |
| BS | $V_{in}$ | 0 | $V_{in}$ | $I_{in}$ | 0 | $I_{in}$ |
| AP | $V_{in}$ | $V_{in}$ | $V_{in}$ | $I_{in}$ | $I_{in}$ | $I_{in}$ |
| (inverting) | Current | | | Transconductance | | |
| | $I_1$ | $I_2$ | $I_3$ | $V_1$ | $V_2$ | $V_3$ |
| LP | $I_{in}$ | 0 | 0 | $V_{in}$ | 0 | 0 |
| BP | 0 | $I_{in}$ | 0 | 0 | $V_{in}$ | 0 |
| HP | 0 | 0 | $I_{in}$ | 0 | 0 | $V_{in}$ |
| BS | $I_{in}$ | 0 | $I_{in}$ | $V_{in}$ | 0 | $V_{in}$ |
| AP | $I_{in}$ | $I_{in}$ | $I_{in}$ | $V_{in}$ | $V_{in}$ | $V_{in}$ |

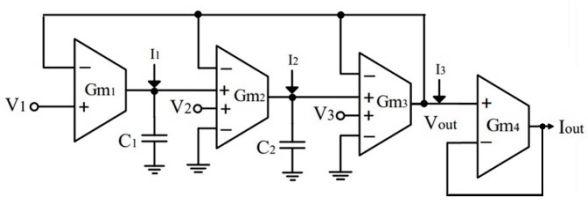


**Figure 5:** The proposed filter topology

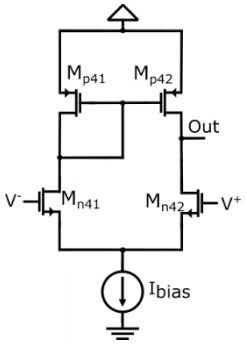


**Figure 6**: The proposed filter output stage ($G_{m4}$) – a differential amplifier with a current source as load [13]

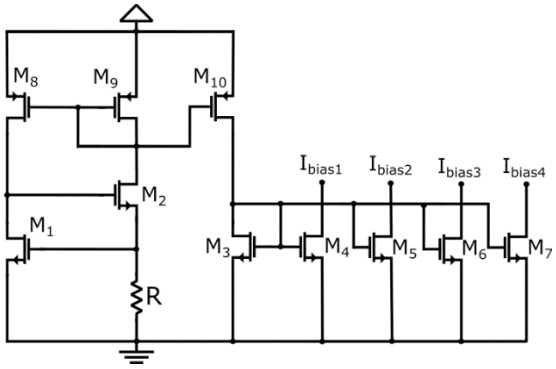


**Figure 7:** The proposed filter biasing circuit

## *3 Post-layout simulation results and discussion*

The proposed filter topology is designed using the UMC 130 nm MM/RF CMOS process with Cadence Virtuoso Tools. The transistor gate widths are presented in Table 2. All filter stages are designed with the minimum gate length of 120 nm, while the devices in the current mirrors have gate length of 200 nm. The resistor value is 5.65 kΩ. The proposed circuit layout is shown in Fig. 8. The integrated filter occupies a die area of 230 µm x 130 µm.

To demonstrate the advantages of the proposed topology, this section presents the post-layout simulation results for both topologies, which have been simulated using the Spectre Simulator from Cadence Design Sys-

**Table 2:** The transistor gate widths

| Transistor | Fingers | Number of devices | W [µm] |
|---|---|---|---|
| $M_{p11}$, $M_{p14}$ | 4.0 | 6.0 | 2.0 |
| $M_{p12}$ $M_{p13}$ | 4.0 | 2.0 | 2.0 |
| $M_{n11}$, $M_{n12}$ | 4.0 | 4.0 | 3.5 |
| $M_{n13}$, $M_{n14}$ | 4.0 | 1.0 | 0.9 |
| $M_{p21}$, $M_{p24}$ | 4.0 | 8.0 | 2.0 |
| $M_{p22}$, $M_{p23}$ | 4.0 | 2.0 | 2.0 |
| $M_{n21}$, $M_{n22}$ $M_{n23}$, $M_{n24}$ | 4.0 | 4.0 | 3.5 |
| $M_{n25}$, $M_{n26}$ | 4.0 | 6.0 | 2.0 |
| $M_{n27}$, $M_{n28}$ | 4.0 | 1.0 | 1.1 |
| $M_{p1}$ | 4.0 | 1.0 | 4.0 |
| $M_{n1}$ | 4.0 | 1.0 | 2.0 |
| $M_1$, $M_2$ | 4.0 | 4.0 | 2.0 |
| $M_3$ | 4.0 | 2.0 | 2.0 |
| $M_4$ | 4.0 | 6.0 | 2.0 |
| $M_5$, $M_6$ | 4.0 | 12.0 | 2.0 |
| $M_7$ | 4.0 | 2.0 | 2.0 |
| $M_8$, $M_9$, $M_{10}$ | 4.0 | 1.0 | 2.0 |

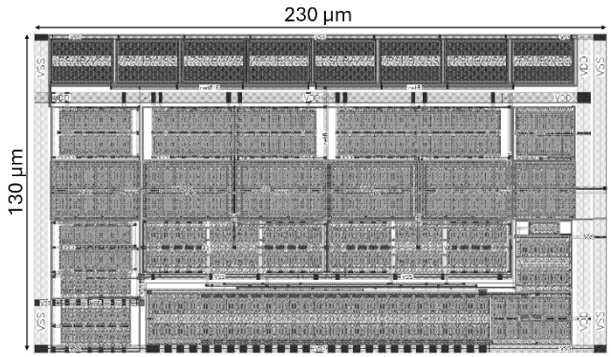


**Figure 8:** The proposed filter layout

tems. A corner analysis has been conducted for each topology to evaluate performance under various process, voltage, and temperature conditions. Only the most critical results have been presented for the initial topology, whereas a more detailed analysis has been provided for the proposed circuit. It should be emphasized that in this work, much higher center frequency values were achieved compared to the results obtained in [11]. Unfortunately, this was achieved at the expense of higher transconductance values and, consequently, increased overall circuit power consumption.

The transconductance values of the OTA circuits are $G_{m1} = G_{m2} \approx 4$ mS. The capacitance values are $C_1 = C_2 = 2.6$ pF. The symmetrical power supply of ±0.6 V is used. The center frequency at the nominal corner is 251 MHz with a quality factor of 1. The total current consumption of the proposed filter is 4.5 mA. The bias currents are $I_{bias1} = 150$ µA, $I_{bias2} = I_{bias3} = 300$ µA, and $I_{bias4} = 50$ µA.

Figures 9, 10, 11, and 12 demonstrate the post-layout simulation results for the initial filter topology (Fig. 1). In these figures, the initial topology is labeled as T1, while the proposed topology is denoted as T2 (in the following figures). Process variation corners including typical-typical (TT), fast-fast (FF), slow-slow (SS), slow-fast (SF) and fast-slow (FS) of NMOS and PMOS transistor parameters has been simulated. Process and voltage variations are presented for transconductance mode in Figs. 9 and 10, and for current mode in Figs. 11 and 12, respectively.

The nominal center frequency is 251 MHz. These results highlight the critical corners associated with the DC voltage shift at the inverter output and the gain changes due to voltage and process variations. The critical process variations are FS and SF corners.

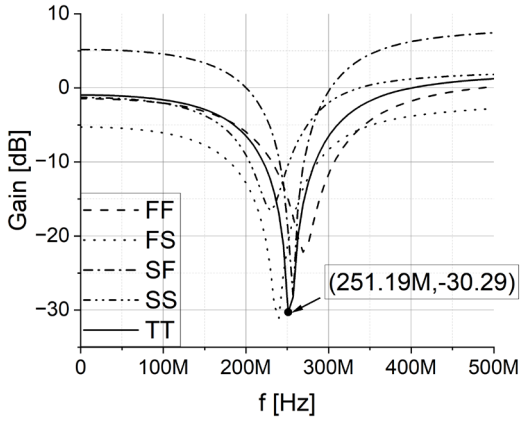


**Figure 9:** Post-layout simulations for process variations in transconductance mode (T1)

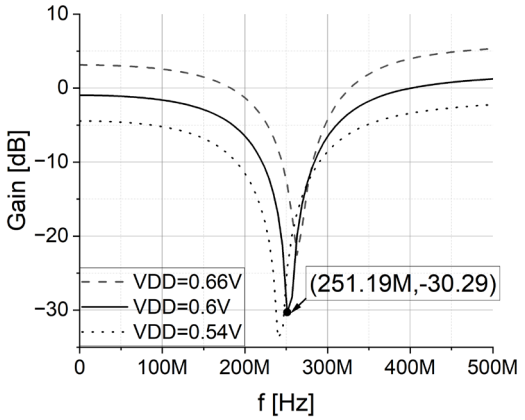


**Figure 10:** Post-layout simulations for voltage variations in transconductance mode (T1)

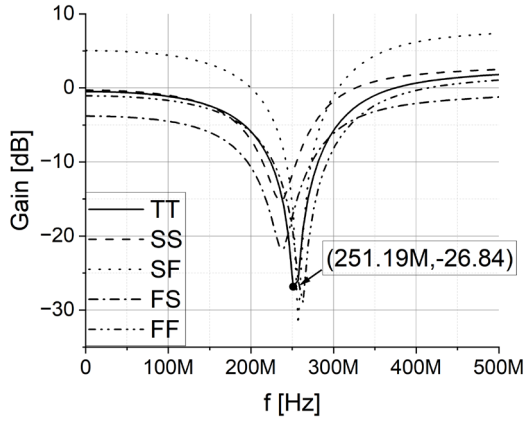


**Figure 11:** Post-layout simulations for process variations in current mode (T1)

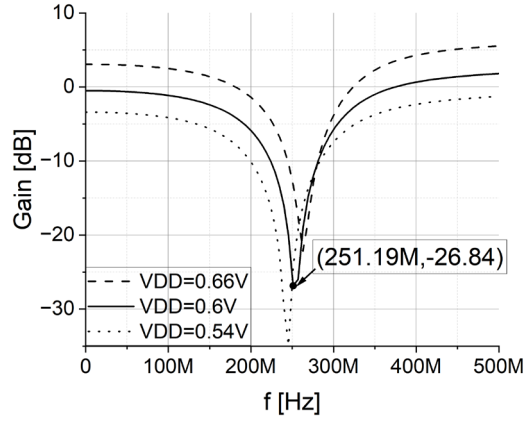


**Figure 12:** Post-layout simulations for voltage variations in current mode (T1)

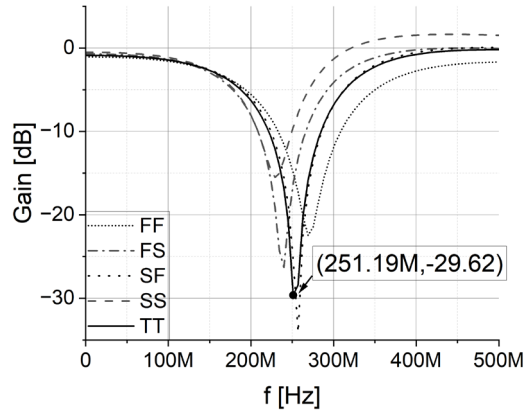


**Figure 13:** Post-layout simulations for process variations in transconductance mode (T2)

Figures 13, 14, 15, and 16 illustrate the post-layout simulation results for the proposed filter topology (Fig. 5). Process and voltage variations for the transconductance mode are shown in Figs. 13 and 14, while those for the current mode are displayed in Figs. 15 and 16, respectively. These results present critical corners for voltage and process variations in both sensitive modes,

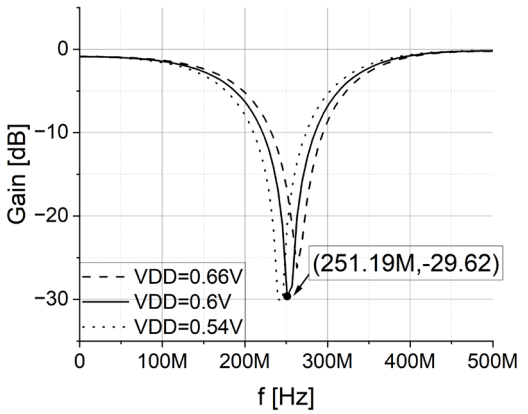


**Figure 14:** Post-layout simulations for voltage variations in transconductance mode (T2)

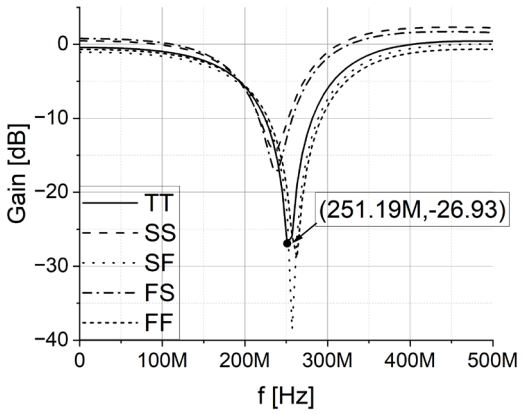


**Figure 15:** Post-layout simulation for process variations in current mode (T2)

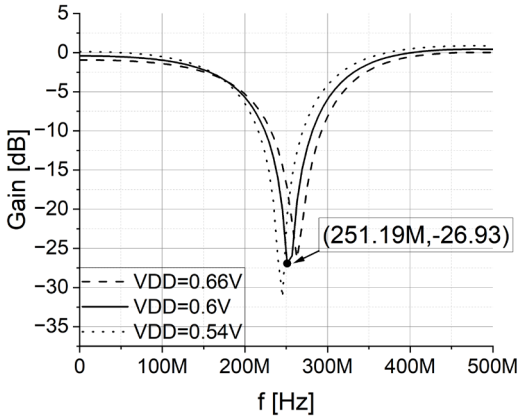


**Figure 16:** Post-layout simulation for voltage variations in current mode (T2)

demonstrating significant improvements in the proposed filter topology by eliminating gain variations. Additionally, it can be observed that the changes in the characteristics across all operating modes are smaller compared to those in the previous circuit.

Figures 17, 18, 19, and 20 present the post-layout simulation results for all transfer functions (LP, HP, BP, AP and BS) of the proposed MISO universal OTA-C filter while showcasing the nominal results for all modes

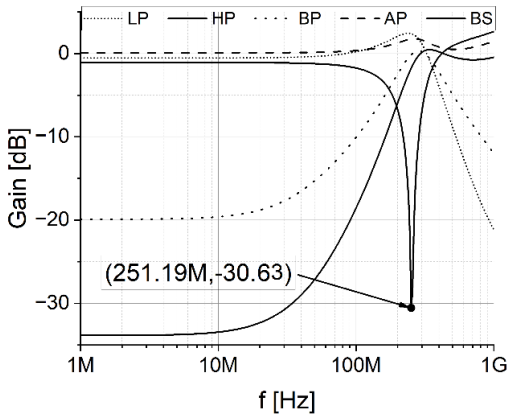


**Figure 17:** Post-layout simulation results for voltage mode (T2)

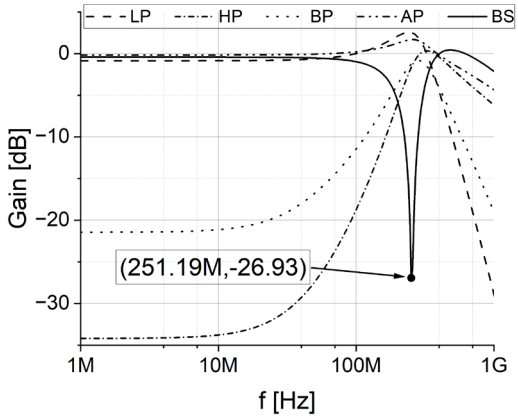


**Figure 18:** Post-layout simulation results for current mode (T2)

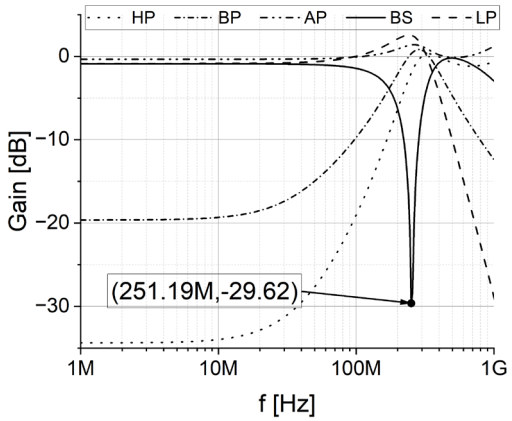


**Figure 19:** Post-layout simulation results for transconductance mode (T2)

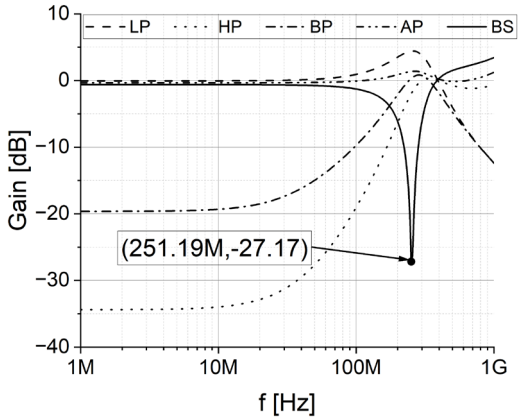


**Figure 20:** Post-layout simulation results for transresistance mode (T2)

(voltage, current, transresistance, and transconductance). It can be noted that the center (cutoff) frequency of all filter characteristics is approximately 251 MHz. Moreover, no significant attenuation is observed in the passband, and the attenuation in the stopband is acceptable.

To fully verify the filter sensitivity, additional analyses including process variations in MOSFET, bias resistor, and capacitor parameters have been simulated. Furthermore, the dependence of the filter key parameters (e.g. the center frequency and the attenuation at the center frequency) on voltage and temperature variations has been tested. To save space, the post-layout simulation results of the corner analyses have been presented only for the voltage mode. The nominal center frequency is 251.19 MHz, while the nominal attenuation at the center frequency is -30.63 dB.

Figure 21 illustrates the influence of the process variations of the MOSFET parameters. The minimum center frequency is 229.09 MHz in the SS corner, while the maximum center frequency reaches 269.15 MHz in the FF corner. The influence of the process variations of the resistor in biasing circuit is shown in Fig 22. The minimum center frequency is 234.42 MHz in the maximal corner, while the maximum center frequency reaches 281.84 MHz in the minimal corner. Figure 23 displays the process variations of the capacitor parameters. The minimum center frequency is 234.42 MHz in the maximal corner, while the maximum center frequency reaches 275.42 MHz in the minimal corner.

The influence of the voltage is simulated with a ±10% variation around the nominal voltage supply value, as shown in Fig. 24. The center frequency ranges from a minimum of 234.42 MHz to a maximum of 275.42 MHz. Figure 25 presents the filter characteristics under different temperature from -40° to 125°. The center fre-

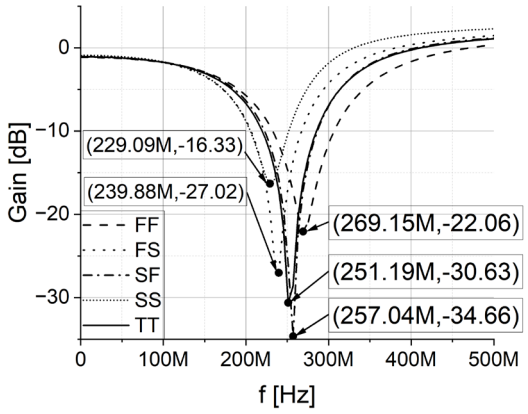


**Figure 21:** Post-layout simulation results for process variations of the MOSFET transistors (T2)

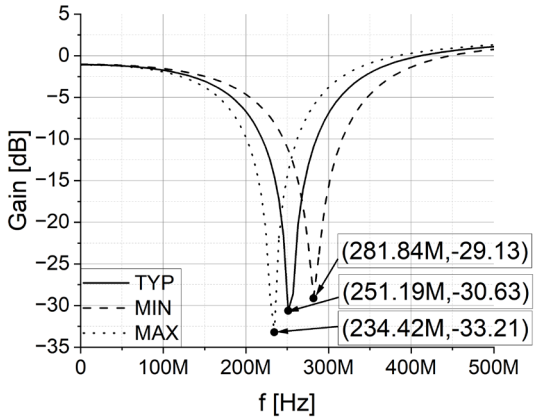


**Figure 22:** Post-layout simulation results for process variations of the resistor in the biasing circuit (T2)

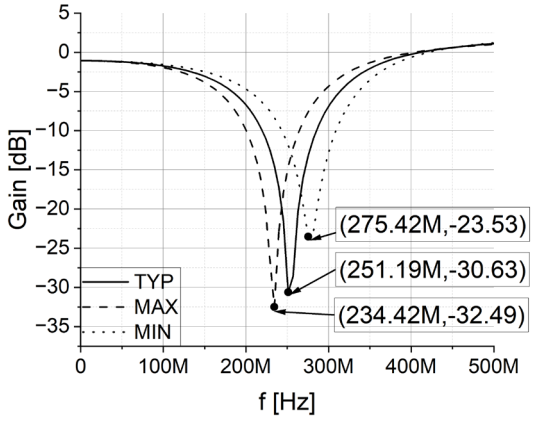


**Figure 23:** Post-layout simulation results for process variations of the capacitor in biasing circuit (T2)

quency ranges from a minimum of 204.17 MHz to a maximum of 269.15 MHz. In the worst case, when the temperature is 125°, the change in center frequency is less than 19%. As can be observed, the proposed filter is not highly sensitive to different corners.

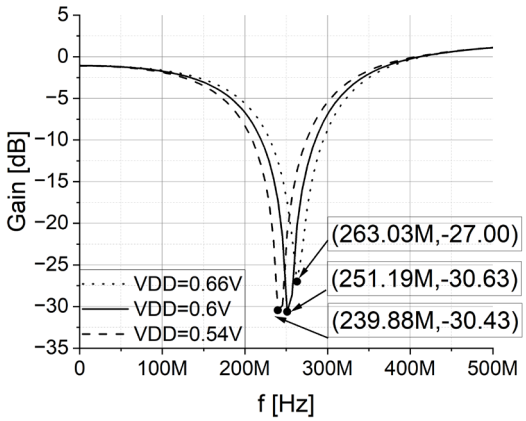


**Figure 24:** Post-layout simulation results for voltage variations (T2)

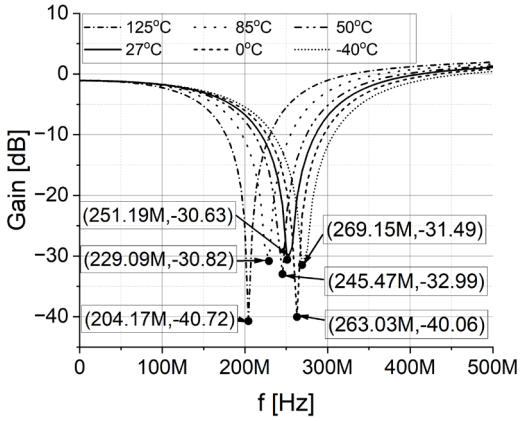


**Figure 25:** Post-layout simulation results for temperature variations (T2)

A summary of all corner analysis results for all filter operating modes is presented in Table 3. The performance (e.g. the center frequency ($f_0$ [MHz]) and the attenuation at the center frequency) are provided for the band-stop filter transfer function. Parameters $\alpha_N$ [dB], $\alpha_{TK}$ [dB], $\alpha_C$ [dB], and $\alpha_{TR}$ [dB] represent the attenuations at the center frequency in the voltage, transconductance, current, and transresistance mode, respectively. It can be observed that there are no significant changes in results across PVT variations.

Table 4 presents a comparison of the simulation results obtained in this paper and the reference research presented in [11]. As previously discussed, the filter topology proposed in [11] uses an inverting amplifier at the output (Fig. 1) to decrease the number of transistors and save die area. This study proposes the improved filter topology with the differential amplifier at the output (Figs. 5 and 6) to reduce the impact of process and voltage variations in transconductance and current operating modes (proved by the obtained simulation results). Moreover, this paper operates at a significantly higher frequency but with higher power consumption.

**Table 3:** Corner analysis results

| Process variations of MOSFET | | | | | |
|---|---|---|---|---|---|
| | TT | SS | FS | SF | FF |
| $f_0$ | 251.2 | 229.1 | 239.9 | 257.0 | 269.0 |
| $\alpha_N$ | -30.6 | -16.3 | -27.0 | -51.8 | -22.1 |
| $\alpha_{TK}$ | 29.6 | -15.5 | -26.3 | -34.1 | -22.5 |
| $\alpha_C$ | -26.9 | -14.8 | -17.1 | -38.5 | -28.7 |
| $\alpha_{TR}$ | -27.2 | -14.8 | -17.1 | -38.5 | -28.7 |
| Temperature variations [oC] | | | | | |
| | 125 | 85 | 50 | 27 | 0 | -40 |
| $f_0$ | 204 | 229 | 245 | 251 | 263 | 269 |
| $\alpha_N$ | -41 | -31 | -33 | -30.6 | -40 | -31 |
| $\alpha_{TK}$ | -38 | -30 | -32 | -30 | -40 | -31 |
| $\alpha_C$ | -21 | -24 | -26 | -26.9 | -35 | -35 |
| $\alpha_{TR}$ | -21 | -24 | -26 | -27.2 | -35 | -35 |
| Process variations of resistor | | | |
| | MIN | TYP | MAX |
| $f_0$ | 281.8 | 251.2 | 234.4 |
| $\alpha_N$ | -29.2 | -30.6 | -30.8 |
| $\alpha_{TK}$ | -28.2 | -29.6 | -33.8 |
| $\alpha_C$ | -26.0 | -26.9 | -28.3 |
| $\alpha_{TR}$ | -25.7 | -27.2 | -28.1 |
| Process variations of capacitor | | | |
| | MIN | TYP | MAX |
| $f_0$ | 275.4 | 251.2 | 223.9 |
| $\alpha_N$ | -23.5 | -30.6 | -32.6 |
| $\alpha_{TK}$ | -22.9 | -29.6 | -33.0 |
| $\alpha_C$ | -20.5 | -26.9 | -36.5 |
| $\alpha_{TR}$ | -20.8 | -27.2 | -37.0 |
| Voltage variations [mV] | | | |
| | 540 | 600 | 660 |
| $f_0$ | 239.9 | 251.2 | 263.0 |
| $\alpha_N$ | -30.4 | -30.6 | -27.0 |
| $\alpha_{TK}$ | -30.0 | -29.6 | -26.2 |
| $\alpha_C$ | -31.8 | -26.9 | -26.6 |
| $\alpha_{TR}$ | -31.2 | -27.2 | -26.3 |

**Table 4:** Comparison of the filter performance

| Characteristics | [11] | This work |
|---|---|---|
| Technology | 0.18 µm | 0.13 µm |
| Power supply | ±0.5 V | ±0.6 V |
| Power consumption | 35 µW | 5.4 mW |
| Center frequency | 2.5 MHz | 251 MHz |
| Number of OTAs | 3 | 4 |
| Number of inverters | 1 | 0 |
| Number of transistors | 34 | 37 |

## 4 Conclusion

This paper proposes a new MISO mixed-mode universal OTA-C filter. The filter consists of four OTAs and two capacitors. A simple differential amplifier with unity feedback is used as the final OTA stage to convert the voltage signal to a current signal at the filter output. This approach achieves better stability of the OTA characteristics compared to a simple inverter amplifier, resulting in significantly lower filter sensitivity to PVT variations. The filter is designed using the UMC 130 nm MM/RF CMOS process. Post-layout simulations performed using Cadence Design Systems software with the Spectre simulator confirmed the features of the proposed topology. The results verified the superiority of the proposed filter in terms of sensitivity to PVT variations, particularly in transconductance and current modes, with no variations in attenuation within the passband. Furthermore, the results indicate that this study achieved a significantly higher center (cut-off) frequency for the filter compared to the reference work, albeit at the cost of increased overall circuit power and area consumption.

## 5 Acknowledgments

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## 6 Conflict of interest

The authors declare that they have no conflict of interest.

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# *Microcontroller Realization of a Novel 4D Hyperchaotic System and Its Autonomous Mobile Robot Application*

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**Abstract:** The chaotic systems offer benefits in diverse domains, including encryption and communication systems, particularly in the upkeep of intricate and safeguarded systems. This study introduces a new hyperchaotic system with four dimensions (4D), seven parameters, and four quadratic non-linear terms. An extensive analysis is conducted on the suggested hyperchaotic system to investigate its dynamic properties, such as chaotic attractors, stability of equilibrium points, spectrum of Lyapunov exponents (LE), bifurcation diagram, etc. The proposed system is validated both by experimental tests using an embedded hardware STM32 microcontroller and MATLAB simulations. The microcontroller-based chaotic systems proposed in the literature and the given hyperchaotic system in this study are compared in a tabular form. The outcomes of these trials constantly correspond, offering theoretical validation for the utilization of this hyperchaotic system in real-world applications. An application example of an autonomous mobile robot (AMR) driven by the presented hyperchaotic system is provided in this work, as efficient and fast terrain exploration is a crucial problem in AMR path planning research.

**Keywords:** chaos; hyperchaotic systems; embedded systems; microcontroller-based implementation; Autonomous mobile robots; chaotic path planning

# *Mikrokrmilniška realizacija novega 4D hiperkaotskega sistema in njegova avtonomna uporaba za mobilne robote*

**Izvleček:** Kaotični sistemi so koristni na različnih področjih, vključno s šifrirnimi in komunikacijskimi sistemi, zlasti pri vzdrževanju zapletenih in zaščitenih sistemov. Ta študija uvaja nov hiperkaotični sistem s štirimi dimenzijami (4D), sedmimi parametri in štirimi kvadratnimi nelinearnimi členi. Na predlaganem hiperkaotičnem sistemu je opravljena obsežna analiza, da bi raziskali njegove dinamične lastnosti, kot so kaotični atraktorji, stabilnost ravnovesnih točk, spekter Ljapunovovih eksponentov (LE), bifurkacijski diagram itd. Predlagani sistem je potrjen z eksperimentalnimi preskusi z vgrajenim strojnim mikrokrmilnikom STM32 in simulacijami v programu MATLAB. V literaturi predlagani kaotični sistemi, ki temeljijo na mikrokrmilnikih, in dani hiperkaotični sistem v tej študiji so primerjani v obliki tabele. Rezultati teh poskusov se dobro ujemajo, kar ponuja teoretično potrditev uporabe tega hiperkaotičnega sistema v realnih aplikacijah. V članku je podan primer uporabe avtonomnega mobilnega robota (AMR), ki ga poganja predstavljeni hiperkaotični sistem, saj je učinkovito in hitro raziskovanje terena ključni problem pri raziskavah načrtovanja poti AMR.

**Ključne besede:** kaos; hiperkaotični sistemi; vgrajeni sistemi; implementacija na osnovi mikrokrmilnika; avtonomni mobilni roboti; kaotično načrtovanje poti

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## 1 Introduction

Chaos theory unveils the fascinating duality of complex systems: governed by deterministic equations yet exhibiting seemingly random and unpredictable behavior. This paradoxical blend, aptly described as a "completely predictable state of confusion" [1], lies at the heart of numerous natural and engineered phenomena. Its study sheds light on diverse systems, ranging from weather patterns and ecological dynamics to population fluctuations and economic models [2 – 4]. Rossler conducted the initial research on the notion of hyperchaos [5]. The number of positive LE in the system frequently determines how complex the chaotic behavior of these systems is. Systems with one or more positive LE are considered chaotic, whereas those with two or more are considered hyperchaotic.

4D hyperchaotic systems belong to a fascinating class of complex systems. These systems are highly sensitive to initial circumstances and display complex dynamics, resulting in butterfly effects where small variations in the starting point can cause significantly different and unforeseen consequences [6]. This very sensitivity, however, allows for potential control and manipulation, making them alluring objects of research for engineers and mathematicians alike [6, 7]. An increasing number of researchers have started looking for chaotic systems with more sophisticated dynamic behaviors to increase the security of chaotic information encryption and chaotic secure communication [8 – 10].

In recent times, there has been a proliferation of proposed hyperchaotic systems that have gained extensive utilization across various domains such as information processing, neuroscience, electronics, communications, and information technology [11] – [28]. Their more intricate dynamics have facilitated the development of secure communication, audio encryption, video encryption, and image encryption.

A 4D autonomous chaotic system with cubic nonlinear terms in each equation is presented in [11]. The given system can produce complex dynamics over a wide range of parameter values, such as chaos, period doubling bifurcation, Hopf bifurcation, periodic orbit, source, sink, and so forth. The study in [12] delves into a novel 4D chaotic system built on cubic non-linear terms. The proposed system exhibits two double-wing chaotic attractors that exist simultaneously. In Ref [13], an efficient method to design S-boxes based on the Qi Hyperchaos System is proposed. It is aimed at creating more robust S-boxes that can provide diffusion and confusion properties together.

A new hyperchaotic attractor has been proposed by combining a uniform flux-controlled memristor and a cross-product term to the 3D autonomous chaotic system [14]. In the study conducted in [15], a 4D chaotic system includes four non-linear terms and four variable parameters. In [16], a hyperchaotic system with a butterfly effect is given. Numerical simulations and circuit implementation investigate the system's fundamental dynamic properties.

Embedded hardware such as Field Programmable Gate Arrays (FPGAs) are widely used to simulate and control hyperchaotic systems [17] – [20]. A five-dimensional (5D) hyperchaotic system is presented and realized in FPGA [17]. It has an exponential-term and memristive model. The fundamental properties are examined using bifurcation diagrams, phase diagrams, and the LE. 4D and 5D hyperchaotic systems based on the classical Sprott-C three-dimensional (3D) system are presented in [18]. The proposed systems were realized by an FPGA and demonstrated by an experimental result. The main characteristics of the proposed system are demonstrated using LE spectra, phase diagrams, and bifurcation diagrams. A multistable 4D hyperchaotic system is implemented using an FPGA and a MultiSim circuit simulator in [19]. The fundamental characteristics of the suggested system are also analyzed. In [20], a 4D hyperchaotic system is proposed. There are two nonlinear terms among the nine terms in the presented system's dynamics. Additionally, the system exhibits multistability behavior within a certain range. Phase plots, Lyapunov spectra, Kaplan-Yorke dimension, and bifurcation diagrams are utilized to examine the system's intricate dynamic behavior. The implementation of FPGA is also realized.

Real-time capabilities, low costs, power consumption, connectivity, and digital signal processing all contribute to the STM32's widespread use in numerous industries, including communications, industrial automation, control, and the Internet of Things (IoT) [21] – [26]. Some researchers have worked on the realization of chaotic systems using microcontrollers such as Arduino, STM32, PIC18F, etc.

Based on a 3D Lü chaotic system, a 4D hyperchaotic system is built in [21]. The properties of the presented system, including chaotic attractors, the spectrum of LE, equilibrium point stability, and the bifurcation diagram, are investigated. Experimental validation is performed on STM32 embedded hardware. The simulations using Matlab and Multisim were also completed. In [22], a novel class of hyperjerk chaotic systems exhibiting megastability is introduced. Using the Lyapunov spectrum and bifurcation diagrams, different dynamical behaviors of one of the proposed systems are examined. For one of the suggested systems, PSpice simulation

and PIC18F microcontroller realization are performed. An FO 3D system derived from a modified Chua's circuit system is introduced in [23]. Bifurcation analysis, multistability, and coexisting attractors are investigated. A microcontroller-based 3D FO system was implemented with an Arduino UNO board. In addition, PSpice simulations are done. Reference [24] introduces a novel 4D autonomous hyperchaotic system that is built upon the 3D chaotic system described in [25]. Numerical and analytical studies of the dynamic properties are investigated. The LEs are calculated. The presented system is simulated and implemented using a Proteus circuit simulator. In addition, two external digital-to-analog converters (DACs) and a 16-bit dsPIC microcontroller are utilized to operate the system. An autonomous chaotic system in 3D is introduced in [25]. This system produces a chaotic attractor through the changing of two parameters. The dynamic properties were investigated analytically and numerically through the utilization of an electronic circuit consisting of operational amplifiers (OAs). Its microcontroller-based realization was implemented with the PIC32 and external DACs. In [26], a 3D chaotic system with five terms is introduced. The MATLAB/Simulink program uses numerical simulations to demonstrate how the system is synchronized. The secure communication implementation is done on the STM32 development board. The dynamical behaviors of the suggested system, including equilibria, bifurcation, phase plains, time series, and LE, are analyzed. A chaotic 3D attractor with seven terms involving a line and unstable equilibria is proposed in [27]. A comprehensive analysis is conducted on the intricate dynamical behavior of the system through the examination of its equilibria, LE, and bifurcation diagram. Analog circuit implementation and numerical and PSpice simulations are utilized to analyze the periodic states of the system. The realization of the system is performed utilizing an STM32 microcontroller. A 4D chaotic system is developed, and its dynamic behaviors are examined in Reference [28]. The system is implemented using analog active components and validated using PSpice simulation. The C8051 8-bit microcontroller-based random number generator, which uses the proposed chaotic system is designed. The comparison of the chaotic systems using the embedded microcontrollers in the literature with the present hyperchaotic system in this work is shown in Table 1.

As seen in Table 1, some of the chaotic circuits using microcontrollers proposed in the literature are 3D implementations [23], [25] – [27]. Some of these circuits do not exhibit hyperchaotic behavior [22], [23], 25 - 28]. They contain a limited number of non-linear terms [22] – [25], [28] and a smaller number of variable parameters [22], [26], [27]. Chaos applications have been implemented using low bit size microcontrollers [22], [23], [28]. It can be concluded that the hyperchaotic system presented in this work is advantageous compared to similar studies proposed in the literature.

The main goal of path planning research is to construct an AMR system that can completely cover any environment containing dynamic or static obstacles at a given time. Due to the unpredictable nature of chaos, chaotic systems are one of the methods used in path planning. In the literature, studies on chaotic path planning using various chaotic equations such as Lorenz, Chen, and Chua have been presented [29]-[36].

We introduce a new 4D hyperchaotic system in this paper. Dynamic properties such as chaotic attractors, equilibrium point stability, spectrum of LE, and bifurcation diagrams are examined in the suggested hyperchaotic system. The 4D hyperchaotic system is validated using embedded hardware (STM32 microcontrollers) and MATLAB simulations. A path planning application example is provided in the form of an AMR controlled by the proposed hyperchaotic system.

**Table 1:** The comparison of the chaotic systems implemented with the microcontroller.

| Ref. | Dimension of system | Type of system | Number of non-linear terms | Number of variable parameters | Used MC | Bit size of MC |
|---|---|---|---|---|---|---|
| [21] | 4D | Hyperchaotic | 3 quadratic terms | 4 | STM32 | 32-bit |
| [22] | 4D | Chaotic | 1 sinusoidal term | 1 | PIC18F | 8-bit |
| [23] | 3D | Chaotic | 1 quadratic term | 4 | Arduino UNO | 8-bit |
| [24] | 4D | Hyperchaotic | 2 quadratic terms | 4 | dsPIC33FJ | 32-bit |
| [25] | 3D | Chaotic | 2 quadratic terms | 4 | PIC32 | 32-bit |
| [26] | 3D | Chaotic | 2 quadratic terms and 1 cubic term | 1 | STM32 | 32-bit |
| [27] | 3D | Chaotic | 5 quadratic terms | 2 | STM32 | 32-bit |
| [28] | 4D | Chaotic | 2 cubic terms | 5 | C8051 | 8-bit |
| Prop. | 4D | Hyperchaotic | 4 quadratic terms | 7 | STM32 | 32-bit |

MC: Microcontroller

## 2 Novel 4D hyperchaotic system and its analysis

A novel autonomous hyperchaotic system with 4 dimensions, 7 parameters, and 4 quadratic non-linear terms are given below:

$$\dot{x} = ay - bx \tag{1a}$$

$$\dot{y} = cxz \tag{1b}$$

$$\dot{z} = d - exy \tag{1c}$$

$$\dot{u} = fy^2 - gu^2 \tag{1d}$$

where x, y, z, and u are the state variables, and a, b, c, d, e, f, and g are the positive constant parameters. For the presented hyperchaotic system, the initial values of the state parameters and the constant parameters are selected as (*x, y, z, u*) = (5.5, 2.8, 0.3, 0.1) and (*a, b, c, d, e, f, g*) = (4.8, 3, 0.8, 5.5, 1, 1.2, 2.58), respectively. The equilibrium points are calculated as follows:

$$E_{1,2}(x,y,z,u) = \left( \pm\sqrt{\frac{ad}{be}}, \pm\sqrt{\frac{bd}{ae}}, 0, \pm\sqrt{\frac{bdf}{aeg}} \right) \tag{2}$$

To examine the stability, the Jacobian matrix is obtained. For this, the differential equations of the system must be differentiated for each variable. Accordingly, the matrix is found as follows:

$$J = \begin{pmatrix} -b & a & 0 & 0 \\ cz & 0 & cx & 0 \\ -ey & -ex & 0 & 0 \\ 0 & 2fy & 0 & -2gu \end{pmatrix} \tag{3}$$

After the equilibrium points, $E_1$ and $E_2$, found are substituted in the Jacobian matrix, and it is calculated as in Equation (4):

$$J_{1,2} = \begin{pmatrix} -b & a & 0 & 0 \\ 0 & 0 & \pm c\sqrt{\frac{ad}{be}} & 0 \\ \mp\sqrt{\frac{bde}{a}} & \mp\sqrt{\frac{ade}{b}} & 0 & 0 \\ 0 & \pm 2f\sqrt{\frac{bd}{ae}} & 0 & \mp 2\sqrt{\frac{bdfg}{ae}} \end{pmatrix} \tag{4}$$

**Table 2:** Eigenvalues for both equilibrium points.

| Equilibrium point | $\lambda_1$ | $\lambda_2$ | $\lambda_3$ | $\lambda_4$ |
|---|---|---|---|---|
| $E_1$ | -6.5246 | -3.9370 | 0.4685 + j3.2418 | 0.4685 - j3.2418 |
| $E_2$ | 6.5246 | -3.9370 | 0.4685 + j3.2418 | 0.4685 - j3.2418 |

The characteristic equations of the system are found by using the matrix found as det (*J* - *λI*), where the matrix I is a 4x4 diagonal unit matrix. Equation (5a) and (5b) are obtained for the equilibrium points $E_1$ and $E_2$, respectively.

$$\begin{aligned} \det(J_1 - \lambda I) = {} & \lambda^4 + \left( b + 2\sqrt{\frac{bdfg}{ae}} \right)\lambda^3 + \\ & + \left( \frac{acd}{b} + 2b\sqrt{\frac{bdfg}{ae}} \right)\lambda^2 + \\ & + 2cd\left( a + \sqrt{\frac{adfg}{be}} \right)\lambda + 4cd\sqrt{\frac{abdfg}{e}} \end{aligned} \tag{5a}$$

$$\begin{aligned} \det(J_2 - \lambda I) = {} & \lambda^4 + \left( b - 2\sqrt{\frac{bdfg}{ae}} \right)\lambda^3 + \\ & + \left( \frac{cad}{b} - 2b\sqrt{\frac{bdfg}{ae}} \right)\lambda^2 + \\ & + 2cd\left( a - \sqrt{\frac{adfg}{be}} \right)\lambda - 4cd\sqrt{\frac{abdfg}{e}} \end{aligned} \tag{5b}$$

Here, in this study, $a > 0$, $b > 0$, $c > 0$, $d > 0$, $e > 0$, $f > 0$ and $g > 0$ are taken. For both equilibrium points, roots of the characteristic equation are obtained in two different regions of the complex domain. For the first equilibrium point $E_1$, $\lambda_1$ and $\lambda_2$ are obtained as negative real numbers. The other roots $\lambda_3$ and $\lambda_4$ are obtained as two complex numbers that conjugate with each other. These complex numbers have a positive real part. For the second equilibrium point $E_2$, $\lambda_1$ and $\lambda_2$ are obtained as positive and negative real numbers, respectively. As in the $E_1$, $\lambda_3$ and $\lambda_4$ eigenvalues are obtained as the same complex numbers. Hence, this hyperchaotic system is unstable. In Table 2, the calculated eigenvalues for both equilibrium points are given.

Figure 1 illustrates the LE of the suggested 4D hyperchaotic system in time. When the LE of the proposed system are calculated with these values, the values obtained are $L_1$ = 0.5168, $L_2$ = 0.0155, $L_3$ = -3.5305, and $L_4$ = -6.9981 [37]. Here, the positive maximum LE confirms the chaotic nature of the signals produced. If the Kaplan-Yorke Dimension of the proposed 4D hypercha-

otic system is founded using these exponents according to Equation (6), 2.1507 is obtained [38], when j is the maximum index to provide $\sum_{i=1}^{j} K_i > 0$ , by arranging the exponents descending order as $L_1 > L_2 > \ldots > L_n$.

$$D_{KY} = j + \frac{\sum_{i=1}^{j} L_i}{\left|L_{j+1}\right|} \tag{6}$$

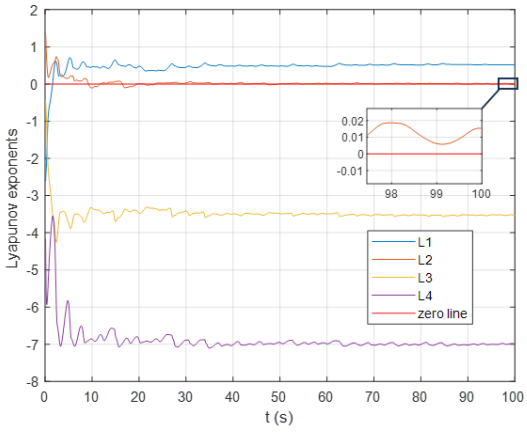


**Figure 1:** Lyapunov exponents of the system in time.

Furthermore, the Jacobian matrix for the suggested system is used to obtain the divergence value ΔV value, which determines the dissipativity of the system. If this ΔV value is negative, the system exhibits chaotic attractors and chaotic behavior under specified beginning conditions. The divergence value of the system is – 9.5245689. Since $\Delta V < 0$, the system behaves chaotically.

**Table 3:** The parameter region showing chaotic behavior.

| Parameters | Parameter Range of Chaotic Behavior | Parameter Range of Hyperchaotic Behavior |
|---|---|---|
| a | 0 < a < 14.2<br>15.6 < a < 20 | 4.2 < a < 5<br>9.1 < a < 14.5<br>15.6 < a < 20 |
| b | 0 < b <20 | 1.7 < b <3.2 |
| c | 0.3 < c < 5.2<br>5.8 < c < 12.8<br>13.9 < c < 20 | 0.4 < c <1.4<br>2.4 < c < 5.2 |
| d | 1.0 < d < 1.6<br>1.9 < d < 20 | 7.5 < d < 8.3<br>9.6 < d < 16.9 |
| e | 0 < e < 20 | 1.5 < e < 3<br>5.3 < e < 5.9 |
| f | 0 < f < 20 | 0.8 < f < 1.4<br>13.8 < f < 15.9 |
| g | 0 < g < 20 | 2 < g < 2.7<br>6.7 < g < 7.4 |

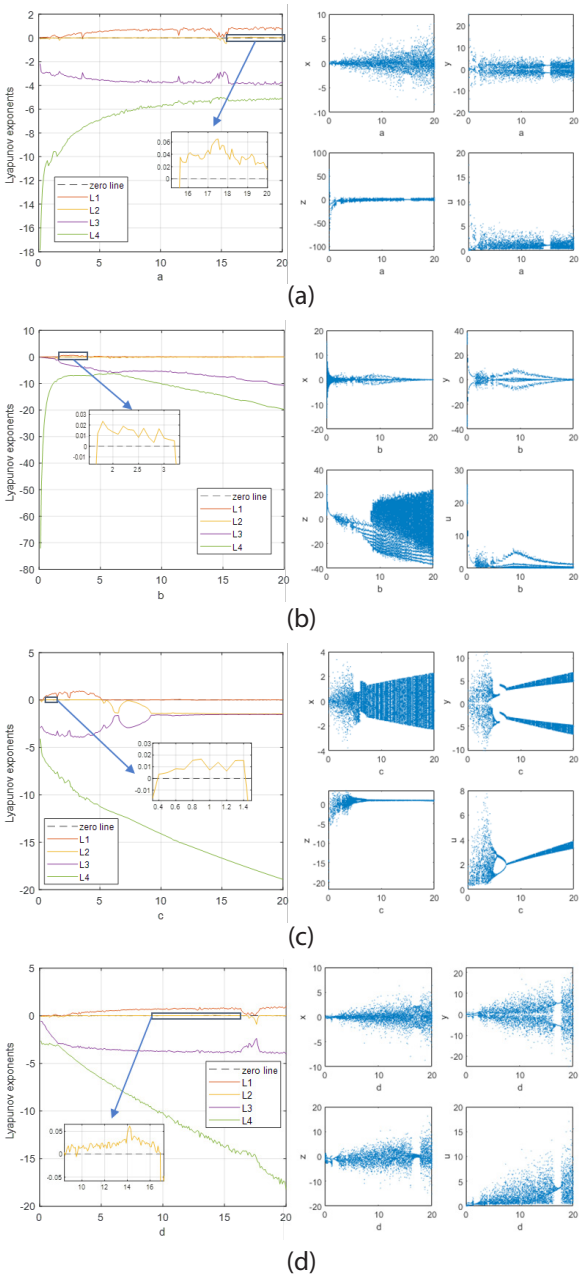


**Figure 2:** Lyapunov exponents and bifurcation diagrams of the system.

Lyapunov exponents and bifurcation diagrams of the suggested system according to the a, b, c, and d parameter values are also given in Figure 2. Table 3 illustrates the regions where the proposed chaotic system shows chaotic and/or hyperchaotic behavior according to its parameters. These ranges are obtained from the LE diagrams in Figure 2, and Table 3 shows the ranges in which certain parameters exhibit chaotic and hyperchaotic behavior. These ranges are crucial for understanding the dynamic properties of the system. When the initial values and constant parameters given above were applied to the hyperchaotic system given by Equation

(1), the Lyapunov spectra seen in Figure 1, the LEs and the bifurcation diagrams seen in Figure 2 and Table 3 were examined, and it was determined that the system showed chaotic behavior for a very wide range of values. Parameter *a* exhibits a wide range of chaotic behavior with distinct intervals interspersed with non-chaotic regions. For the parameter *a*, chaotic behavior is observed in the ranges 0 to 14.2 and 15.6 to 20. The parameter *a* shows hyperchaotic behavior in the ranges 4.2 to 5, 9.1 to 14.5 and 15.6 to 20. Parameter *b* exhibits continuous chaotic behavior between 0 and 20, while hyperchaotic behavior occurs in the range 1.7 to 3.2.

The parameter *c* exhibits chaotic behavior in two distinct intervals and hyperchaotic behavior in one interval. Parameters *d*, *e*, and *g* show similar patterns of chaotic and hyperchaotic behavior over multiple intervals. Interestingly, parameter *f* exhibits a continuous range of chaotic behavior, with no hyperchaotic regions within the given parameter range. Overall, the dynamics of the system appear to be highly sensitive to parameter changes, particularly for parameters *a*, *c*, *d*, and *g*. This sensitivity is evident from the distinct intervals of chaotic and hyperchaotic behavior observed for these parameters. Further analysis using mathematical tools such as Lyapunov exponents could provide more detailed insights into the dynamics of the system and the transitions between chaotic and hyperchaotic regimes.

Based on the above-mentioned findings, it can be said that the system parameter values that put the system into chaotic behavior are in a wide range. In this way, if the system parameters are selected at appropriate values during an application, the proposed 4D hyperchaotic system will show chaotic behavior without being affected much by the tolerances or deviations of the circuit components and power supplies to be used in the application.

## 3 Simulation and experimental results

The system in (1) were defined in the MATLAB program, and the changes with time of the state variables were obtained for (*a, b, c, d, e, f, g*) = (4.8, 3, 0.8, 5.5, 1, 1.2, 2.58) values. The results obtained are given in Figure 3.

The changes of the variables relative to each other were also plotted with the MATLAB program for the same (*a, b, c, d, e, f, g*) values. Figure 4 shows the plots of the changes of the variables over time relative to each other in the following order: x-y variables in (a), x-u variables in (b), x-z variables in (c), y-z variables in (d), y-u variables in (e), u-z variables in (f), x-y-u variables in (g), x-y-z variables in (h), z-u-x variables in (i), and y-z-u variables in (j).

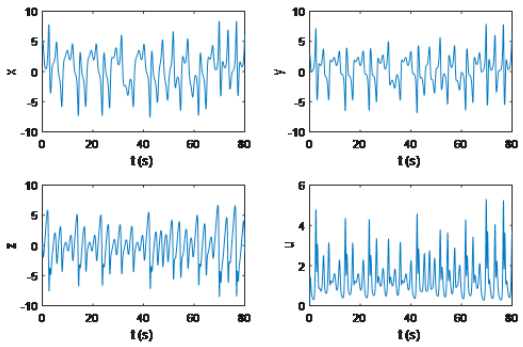


**Figure 3:** MATLAB results for state variables.

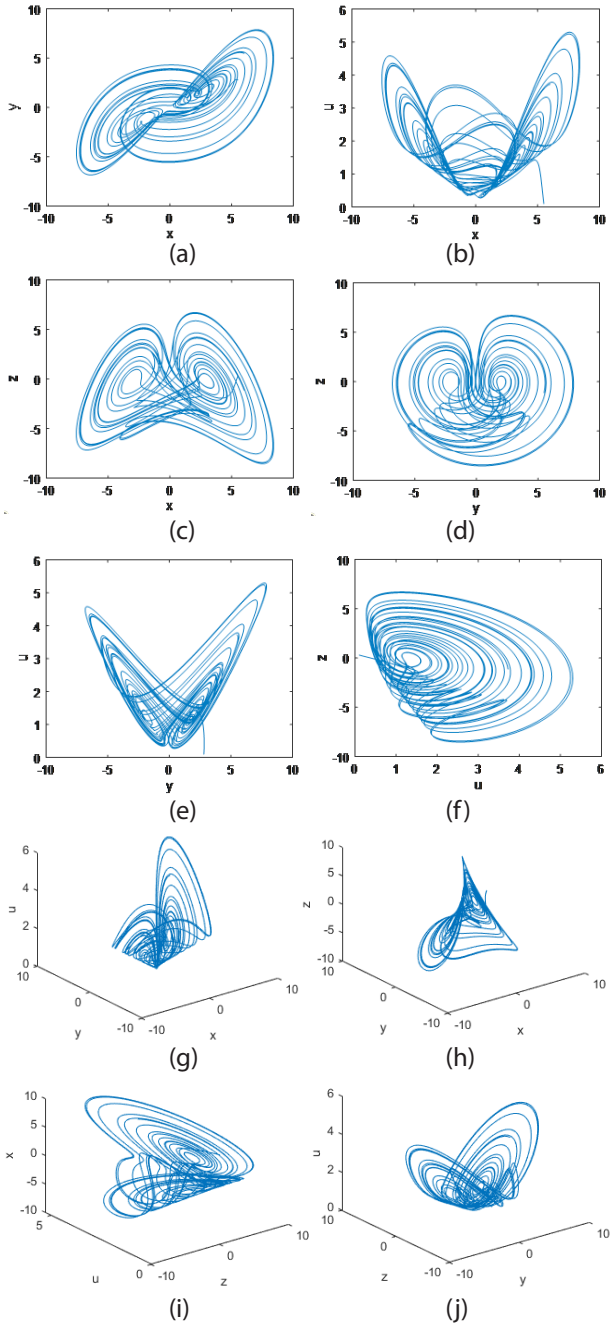


**Figure 4:** Change of state variables relative to each other.

After obtaining the ideal responses of the system through simulation processes, the system was also physically realized. For this, the electrical signals of the state variables were produced using the STM32 microcontroller. First, two separate DAC outputs were set from the STM32 settings. Then, the system state variables are defined in the coding section. When the ideal signals obtained with MATLAB were examined, it was observed that negative values were also obtained. At the same time, values higher than the voltage value that the microcontroller can provide were observed. Since the values for these two cases cannot be obtained with the microcontroller, the obtained values are normalized to be between 0 V and 3.3 V. The algorithm diagram of the written code is given in Figure 5.

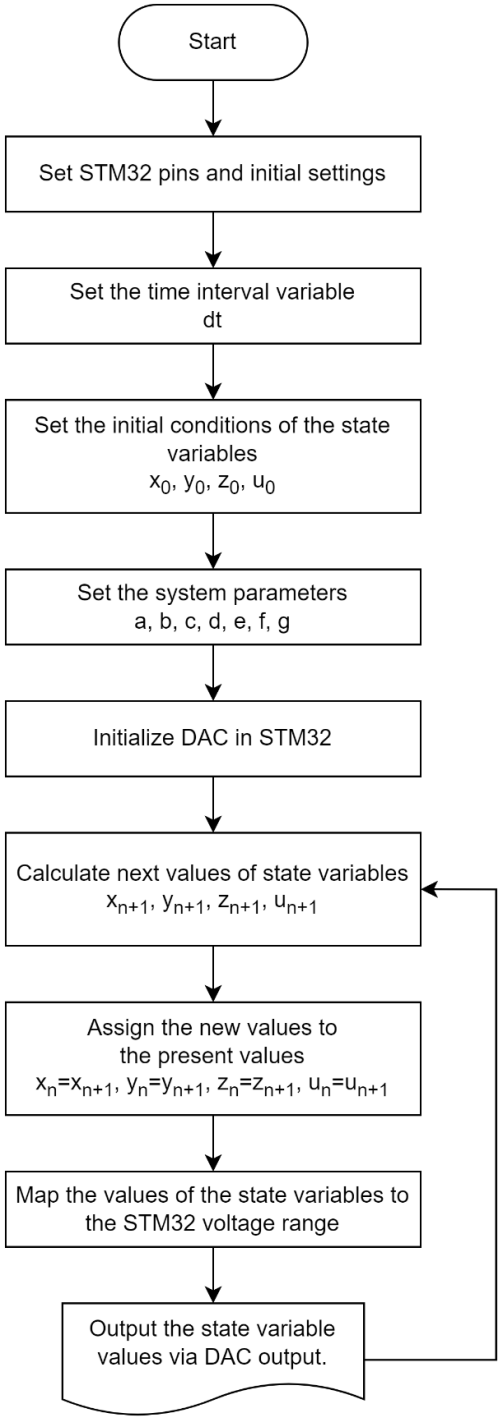


**Figure 5:** The flow chart of the microcontroller program.

The time variation of the signals produced by the microcontroller was measured and displayed with an oscilloscope. The oscilloscope results of the variables x in Figure 6 (a), y in Figure 6 (b), z in Figure 6 (c), and u in Figure 6 (d) have been added.

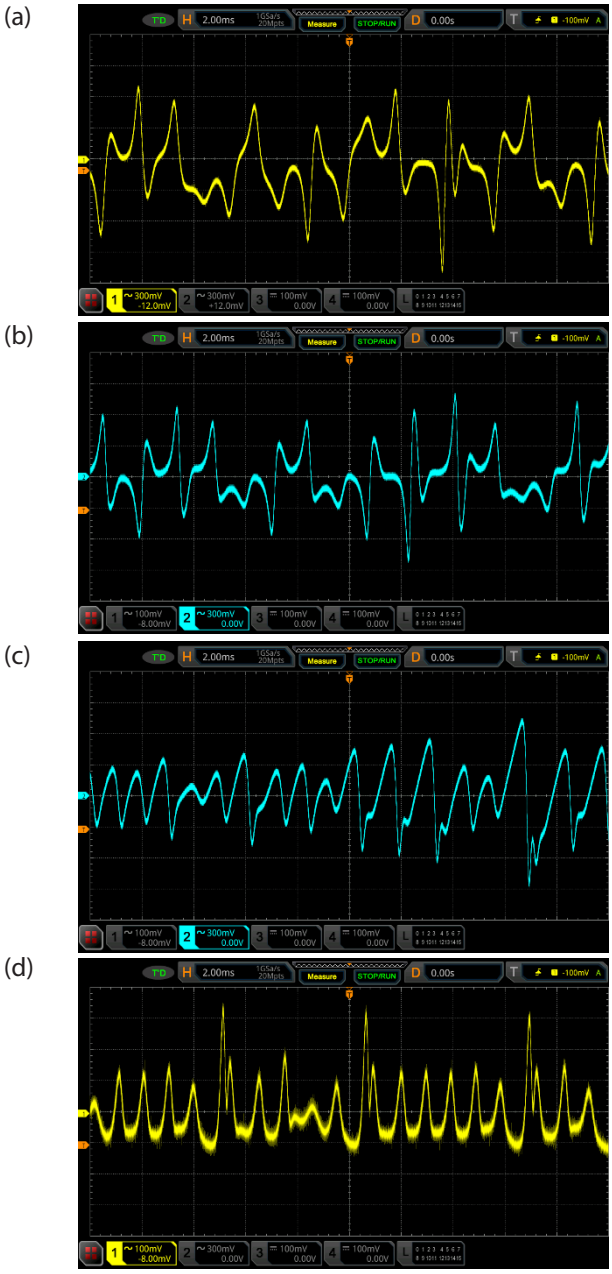


**Figure 6:** Change of state variable signals obtained from the microcontroller over time, (a) x state, (b) y state, (c) z state, and (d) u state.

As in the simulation steps, the changes between the signals obtained with the microcontroller were also observed using the XY mode on the oscilloscope. The obtained results are given in Figure 7. The measured state variable signals relative to each other are in the following order: x-y variables in (a), x-u variables in (b), x-z variables in (c), y-z variables in (d), y-u variables in (e), and u-z variables in (f).

## *4 Chaos-driven autonomous mobile robot application*

Chaotic path planners use chaotic dynamical systems to generate paths within an environment. Path planners are critical for surveillance efforts involving hostile agents, as they require unusual routes and comprehensive coverage of the area. When exploring unknown terrain online, chaotic path planning algorithms can be used without relying on an environmental map. These methods give the designer greater control over the paths generated than random walk algorithms [31]. Recently, many researchers have applied chaotic complex systems to mobile robots [29]-[36]. They have been used in many applications, such as mobile robot patrols, cleaning robots, and many others. However, the simulated trajectories of robots in most of the existing works in the literature show that their coverage is generally low.

The two active wheels are controlled by linear velocity *v(t)* and angular velocity *ω(t)*, as shown in Figure 8. The nonlinear dynamic response of the mobile robot's motion and steering is determined by two independent actuators of analog DC motors that apply appropriate torques to the right and left wheels of the mobile robot [33].

Eq. (7) defines the position vector of the mobile robot's local reference frame, while the global reference frame is [$X_{axis}$, $Y_{axis}$].

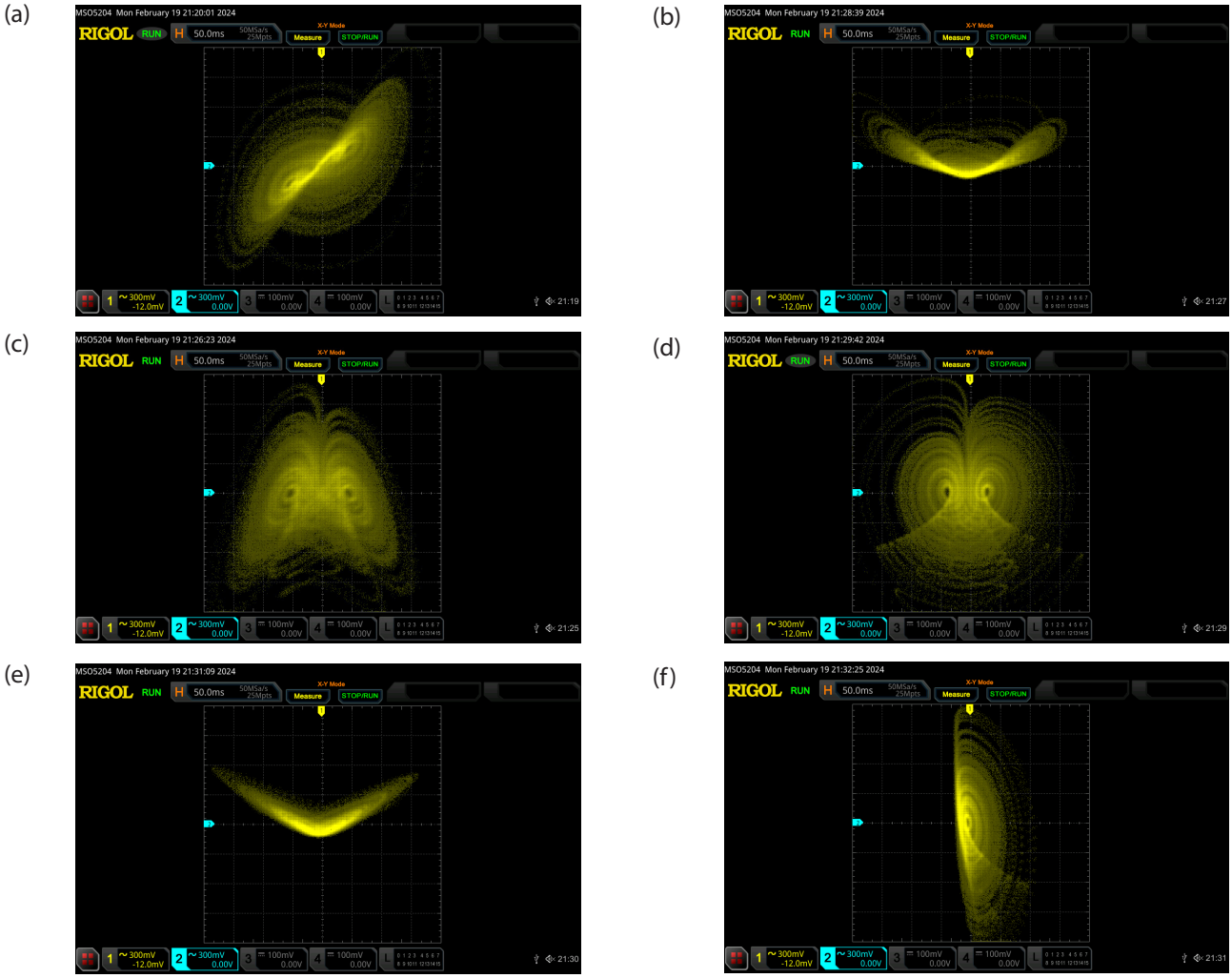


**Figure 7:** Change of state variable signals obtained from the microcontroller to each other, (a) x-y states, (b) x-u states, (c) x-z states, (d) y-z states, (e) y-u states, and (f) u-z states.

$$Q = \left[X_r, Y_r, \theta_r\right]^T \tag{7}$$

Where $X_r(t)$ and $Y_r(t)$ are the position and $\theta_r(t)$ is the orientation of the three-wheeled mobile robot at the midpoint which indicates the location where the left and right wheels meet in the center.

Two primary requirements must be met to confirm the mobile robot's motion and orientation capabilities: each wheel must roll in a pure manner and must not slip for the mobile robot's lateral velocity to equal zero, as stated in Eq. (8).

$$-\dot{X}_r \sin\theta(t) + \dot{Y}_r \cos\theta(t) = 0 \tag{8}$$

As a results, the navigation equation of a three-wheeled mobile robot can be defined as follows [32], [33]:

$$\begin{bmatrix} \dot{X}_r \\ \dot{Y}_r \\ \dot{\theta}_r \end{bmatrix} = \begin{bmatrix} \cos\theta(t) & 0 \\ \sin\theta(t) & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v(t) \\ \omega(t) \end{bmatrix} \tag{9}$$

where $v(t) = [v_r(t) + v_l(t)]/2$ and $\omega(t) = [v_r(t) - v_l(t)]/L$. The variables $v_r(t)$ and $v_l(t)$ represent the velocity of the right and left wheels, respectively. The direct distance between both wheels is denoted by $L$.

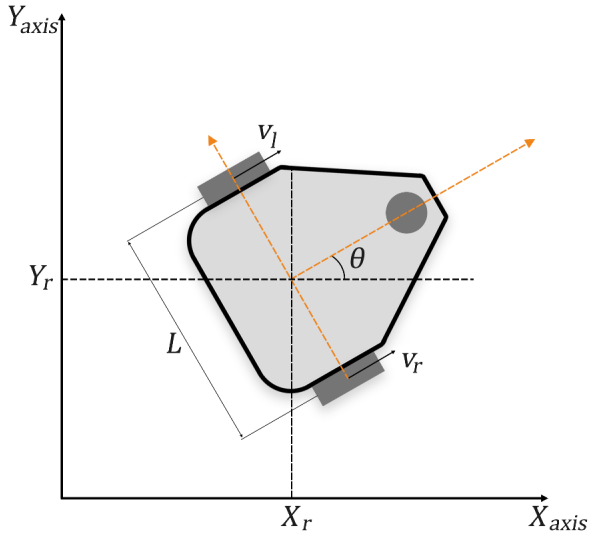


**Figure 8:** Schematic of the three-wheeled AMR navigation

In order to improve the understanding of the robot's chaotic path planning generator, a discontinuous control rule is used, which offers advantages in terms of terrain scanning time. Under this control rule, the robot performs two independent actions. First, to steer the robot directly to the next target coordinate, it rotates around its center with a constant angular velocity $\omega(t)$, as defined by Equation (10). Equation (11), which defines the target, is the path taken by the second action, which is a straight trajectory with constant velocity $v(t)$.

$$\begin{bmatrix} \dot{X}_r \\ \dot{Y}_r \\ \dot{\theta}_r \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \omega(t) \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} \dot{X}_r \\ \dot{Y}_r \\ \dot{\theta}_r \end{bmatrix} = \begin{bmatrix} \cos\theta(t) \\ \sin\theta(t) \\ 0 \end{bmatrix} \tag{11}$$

The idea behind employing a chaotic system for navigation is to substitute two state values from the chaotic equation for the linear velocities of the left and right wheels in the navigation equation. $x(t)$ replaces $v_r(t)$ and $y(t)$ replaces $v_l(t)$. A seven-dimensional system can be created by combining the given hyperchaotic system and the three-wheeled AMR navigation equation in (9).

$$\begin{cases} \dot{x} \\ \dot{y} \\ \dot{z} \\ \dot{u} \\ \dot{X}_r \\ \dot{Y}_r \\ \dot{\theta}_r \end{cases} = \begin{cases} ay - bx \\ cxz \\ d - exy \\ fy^2 - gu^2 \\ \dfrac{x(t)+y(t)}{2}\cos\theta(t) \\ \dfrac{x(t)+y(t)}{2}\sin\theta(t) \\ \dfrac{x(t)-y(t)}{L} \end{cases} \tag{12}$$

Equation (12) shows how the AMR navigates around the suggested hyperchaotic system.

A 20×20 m area is used to test the above equation for robot motion through numerical simulations. The starting position of the mobile robot is ($x$ = 10 $m$, $y$ = 10 $m$) and the system is simulated for 1000, 2000, 3000, and 4000 iterations. Assuming that the limits are located at the horizontal and vertical lines $x$ = 0, $x$ = 21 m, $y$ = 0, $y$ = 21 m. Wheel distance is $L$=0.1 m, initial values of state parameters and constant parameters are chosen as ($x$, $y$, $z$, $u$) = (5.5, 2.8, 0.3, 0.1) and ($a$, $b$, $c$, $d$, $e$, $f$, $g$) = (4.8, 3, 0.8, 5.5, 1, 1.2, 2.58), respectively. As a results, the simulation result generated by MATLAB program the

motion trajectory of the AMR for 1000, 2000, 3000, and 4000 iterations as it is in Figure 9 (a), (b), (c), and (d), respectively.

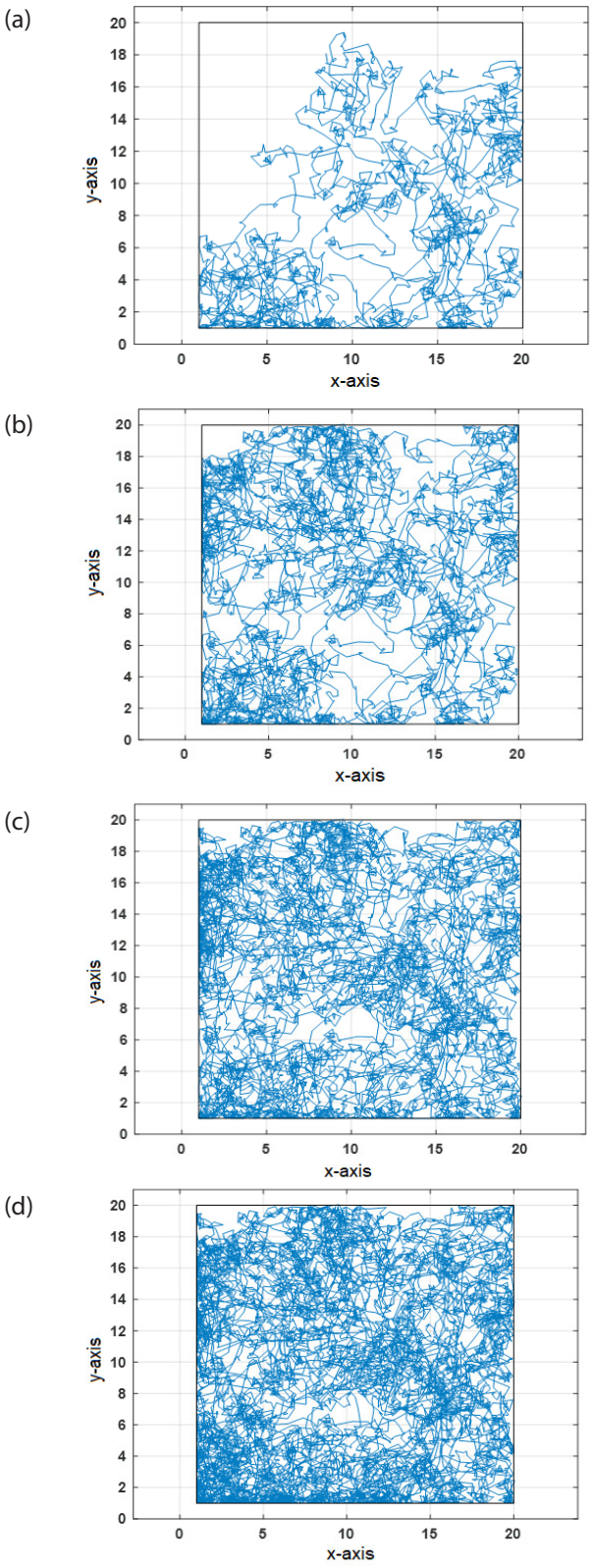


**Figure 9:** Simulation result of navigation path of chaos-driven AMR: a) 1000, b) 2000, c) 3000, d) 4000 iterations.

The above simulations also work for different scenarios in areas of different sizes and shapes. One such scenario is shown in the three simulations in Figure 10. For this, the simulation was repeated by placing a 10×10 m obstacle in the 20×20 m area above. In the simulations, the starting position of the AMR is ($x$ = 10 $m$, $y$ = 10 $m$), the other parameters are chosen as in the previous simulations. The gray areas indicate the obstacles. It is possible to place more than one obstacle of different sizes in different parts of the area.

Simulations with 2000 and 4000 iterations are shown in Figure 10 (a) and (b). As can be seen in Figure 10,

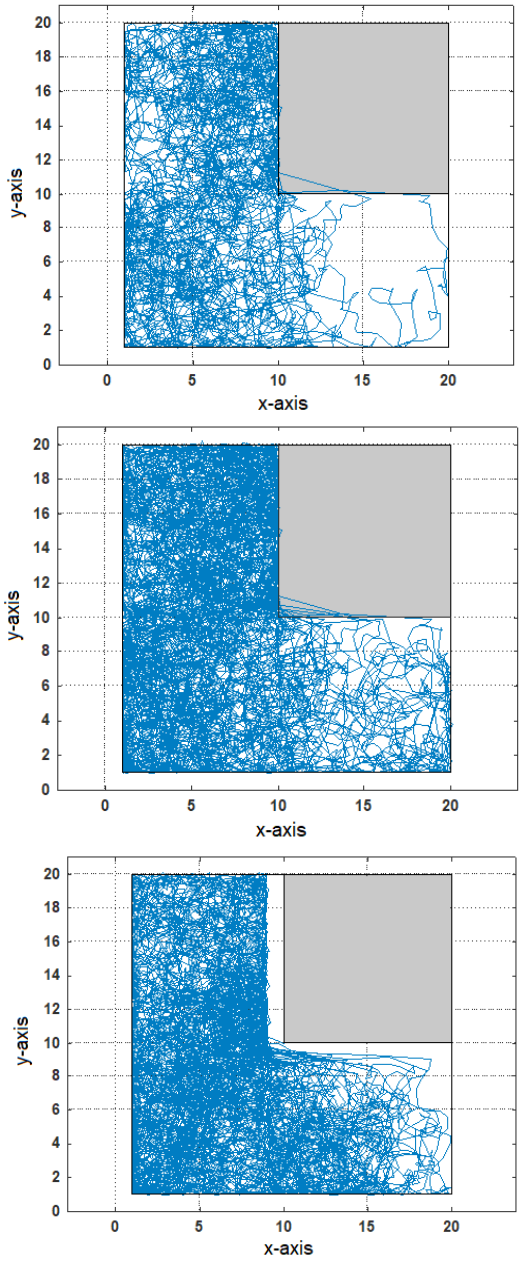


**Figure 10:** Simulation result of the AMR with obstacle: a) 2000, b) 4000, and c) 4000 iterations with 1 m safety distance.

the AMR scanned almost the entire obstacle area as the number of iterations increased. In some cases, the mobile robot entered the obstacle area. To avoid this situation, a robot safety distance can be set. This will prevent the AMR from entering the obstacle area. Another simulation is performed and given as Figure 10 (c), which shows the simulation results of a 20×20 m area with a robot safety distance of 1 m. As can be seen in Figure 10 (c), the AMR is prevented from entering the obstacle area thanks to the safety distance created.

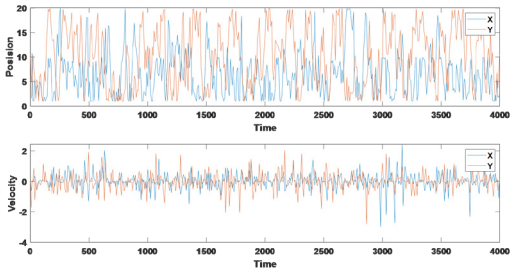


**Figure 11:** Simulation result of the AMR with obstacle: a) Position vs time, b) Velocity vs time graph for 1 m safety distance.

Using acceleration, deceleration, and velocity values of the AMR, a trapezoidal velocity profile trajectory was generated by interpolating waypoints along each dimension (X, Y) using the above parameters in the 20x20 meter with obstacle area [39]. Figure 11 shows the plots the position and velocity with respect to time. As can be seen from Figure 11, the velocity of the AMR varies unpredictably between -2 and +2 m/s depending on the parameters of the proposed hyperchaotic system.

Figure 12 depicts a graph illustrating the average coverage percentage of a specific area by the AMR as a function of the number of iterations. Each iteration is done for one second. Figure 12 presents three distinct curves corresponding to 0.05, 0.1, and 0.2 values of the parameter *L*, representing the wheel distance in meters. For this example, the coverage percentage was achieved at 50% in almost 7900$^{th}$, 4900$^{th}$, and 4300$^{th}$ seconds respectively for the given *L* values. Additionally, when the times for 90% coverage were examined, it was observed that this value was reached at almost 20600$^{th}$, 15600$^{th}$, and 14300$^{th}$ seconds. At the end of this simulation, that is, at the 40000$^{th}$ second, 98.84%, 99.84%, and 99.74% of the 20×20 m area was covered by AMR for each wheel distance, respectively. The number of iterations of the robot increases the coverage percentage also increases. This shows that the AMR scans the area more thoroughly over time, leaving fewer gaps. As the *L* wheel distance increases, more area is scanned in each second and the coverage percentage increases faster.

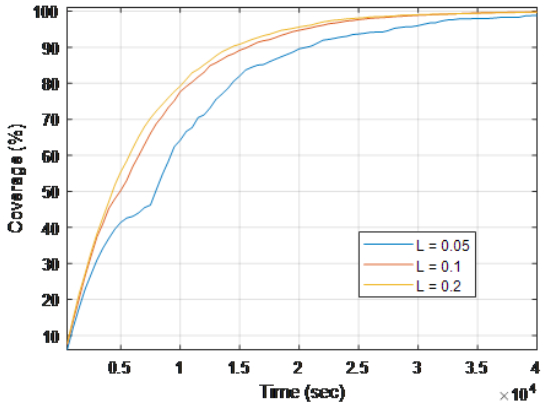


**Figure 12:** Coverage performance of the AMR

## 5 Statistical evaluation of randomness

In order for the proposed hyperchaotic system to be used in various applications, such as cryptography, it must be tested using statistical tests that require long bitstreams of random binary bits. The National Institute of Standards and Technology (NIST) widely uses the NIST SP800-22 test set [40].

We first quantized the values from the chaotic system to prepare the data for testing. We determined the amount of shift to apply to the variables based on their current values in order to increase randomness. For instance, we apply a shift operation in the form of $2^{32}/x[n]$ to shift the variable *x*. We provide the procedures used to prepare the test data below:

Step 1: x, y, z and u variables were converted to 32 bits.
Step 2: The variable y was shifted and XORed with the variable x.
Step 3: The z variable was shifted and XORed with the y variable.
Step 4: The values obtained in steps 2 and 3 were XORed.
Step 5: The variable u was shifted and XORed with the variable z.
Step 6: The variable u is shifted and XORed with the variable x.
Step 7: The results of steps 5 and 6 were XORed.
Step 8: The most significant 16 bits of the result obtained in step 4 and the least significant 16 bits of the result obtained in step 7 were combined.
Step 9: The least significant 16 bits of the result obtained in step 4 and the least significant 16 bits of the result obtained in step 7 were combined.
Step 10: The results obtained in steps 8 and 9 were XORed.

After data preparation, we obtained approximately 14 Mbits. We tested the data for randomness using the NIST 800-22 test tool. There are a total of 15 tests in the NIST 800-22 test suite, and the parameters of each test are described in detail in [40]. For each test to be considered successful, the p-value must be greater than 0.001. The parameters used in the test are shown in Table 4, and the results are shown in Table 5. As seen in Table 5, all standard tests are passed and the test results indicate that the proposed hyperchaotic system exhibits strong randomness properties suitable for secure applications, such as autonomous mobile robot path planning.

**Table 4:** NIST 800-22 test parameters

| Parameter Name | Value |
|---|---|
| Block Frequency Test - block length (M) | 12 |
| Non-Overlapping Template Test - block length (m) | 9 |
| Overlapping Template Test - block length (m) | 9 |
| Approximate Entropy Test - block length (m) | 10 |
| Serial Test - block length (m) | 16 |
| Linear Complexity Test - block length (M) | 50 |

**Table 5:** Microcontroller-based 4D hyperchaotic system NIST 800-22 test results

| Test | p-value | Proportion | Result |
|---|---|---|---|
| Frequency | 0.911413 | 10/10 | Passed |
| Block Frequency | 0.534146 | 8/10 | Passed |
| Cumulative Sums 1 | 0.350485 | 10/10 | Passed |
| Cumulative Sums 2 | 0.739918 | 10/10 | Passed |
| Runs | 0.534146 | 10/10 | Passed |
| Longest Run | 0.534146 | 10/10 | Passed |
| Rank | 0.035174 | 10/10 | Passed |
| FFT | 0.534146 | 10/10 | Passed |
| Non-overlapping Template* | 0.474107 | 10/10 | Passed |
| Overlapping Template | 0.911413 | 10/10 | Passed |
| Universal | 0.739918 | 9/10 | Passed |
| Approximate Entropy | 0.739918 | 10/10 | Passed |
| Serial 1 | 0.739918 | 10/10 | Passed |
| Serial 2 | 0.534146 | 9/10 | Passed |
| Linear Complexity | 0.122325 | 10/10 | Passed |

* Average

## 6 Conclusion

In this study, a novel hyperchaotic system was defined and realized with the embedded hardware STM32 microcontroller. A table comparing the microcontroller-based chaotic systems from existing research with the hyperchaotic system introduced in this study is provided. The proposed structure has several benefits when compared to similar structures in existing literature.

The equilibrium points of the system were calculated using the state variable equations, and the stability of the system was investigated with a bifurcation diagram and LE. Then, to examine the ideal changes in time of these variables, their graphs were plotted according to time and relative to each other in the MATLAB environment, and the simulations were carried out. After that, the state variables were generated as electrical signals using the microcontroller. These signals were produced by converting digital signals to analog signals with a microcontroller and were observed on the oscilloscope screen. As a result, the experimental results obtained by the microcontroller-based implementation of the presented hyperchaotic system coincide with the simulation results from MATLAB.

Efficiently and rapidly exploring a given terrain is a critical challenge in path planning research for autonomous mobile robots. Therefore, an application example of a chaotic path planning of the AMR is provided in order to test the presented hyperchaotic system. For these simulations, a 20×20 m area with and without obstacles is used. The effect of the change in wheel distance on area coverage is also examined.

## 7 Credit author statement

Betul Yurdem: Methodology, Software, Writing - Original Draft, Validation, Writing - Reviewing and Editing. Mustafa Furkan Aksu: Writing - Original Draft, Validation, Writing - Reviewing and Editing. Mehmet Sagbas: Writing - Original Draft, Validation, Writing - Reviewing and Editing.

## 8 Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## 9 Declaration of generative AI and AI-assisted technologies in the writing process

During the preparation of this work the authors used generative AI in order to improve language and read-

ability. After using this tool/service, the authors reviewed and edited the content as needed and took full responsibility for the content of the publication.

## 10 Data availability

Data sharing is not applicable to this article as no datasets were generated or analysed during the current study.

## 11 Conflict of interest

The authors declare that they have no conflict of interest.

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# An Air-gapped Cavity Filter Based on MEMS Process for 5G Millimeter Wave Applications

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**Abstract:** This article presents a 5G millimeter Wave bandpass filter using air-gapped structure, which is fabricated through high-precision micro electromechanical system (MEMS) process. The grounded and open stub lines, as well as impedance transformation stub lines, which generating four transmission poles (TPs) and two transmission zeros (TZs), are proposed to achieve the design goal. Four TPs support a 24.25-27.5-GHz passband, while two TZs provide a sharp out-of-band rejection. Step-to-step design process is given to guide the 24.25-27.5-GHz bandpass filter design. The 24.25-27.5-GHz bandpass filter is fabricated and measured, which has a minimum insertion loss of 0.9dB within the passband.

**Keywords:** Millimeter Wave ; Bandpass filter ; Micro Electromechanical System (MEMS) ; Insertion loss

# Zračni votlinski filter na MEMS osnovi za 5G aplikacije

**Izvleček:** V članku je predstavljen pasovni filter 5G za milimetrske valove, ki uporablja strukturo z zračnimi kapami in je izdelan z visoko natančnim postopkom mikroelektromehanskega sistema (MEMS). Za dosego cilja zasnove so predlagani ozemljeni in odprti kraki ter kraki s transformacijo impedance, ki ustvarjajo štiri prenosne pole (TP) in dve prenosni ničli (TZ). Štirje TP podpirajo prepustni pas 24,25-27,5 GHz, dva TZ pa zagotavljata zavrnitev izven frekvenčnega pasu. Podan je postopek načrtovanja 24,25-27,5-GHz prepustnega pasu. Izdelan in izmerjen je 24,25-27,5-GHz pasovni filter, ki ima najmanjšo izgubo 0,9 dB znotraj prepustnega pasu.

**Ključne besede:** Milimetrsko valovanje ; Pasovni filter ; Mikroelektromehanski sistem (MEMS) ; Vložna izguba

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## 1 Introduction

Millimeter wave bandpass filter as one of the important circuit blocks in 5G wireless communication system has attracted great attention in recent years. Most of reported bandpass filter are designed by planar transmission lines based on printed circuit board (PCB) [1], [2]. Some researchers use some new technologies, such as the substrate integrated waveguide (SIW) in [3], integrated passive devices (IPD) in [4], and the low-temperature co-fired ceramic (LTCC) in [5], to design high-performance bandpass filters. However, traditional substrate-based PCB, SIW, IPD, and LTCC technologies suffer from high loss that associated with dielectric loss, especially at mm-wave frequency.

With the rapid expansion of 5G millimeter wave wireless communication system, extensive studies have been attracted on the structures presenting the lowest loss. The recta-coax is a 3-D transmission structure which is completely shielded and has air-gapped cavity, allowing for wideband, low loss, and high-power handling capacity [6]. The low-loss phase shifter with

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wide tunable range in [7], the 8-40GHz broadband integrated antenna array in [8], and the ultra-compact G-band 16-way power splitter/combiner with low insertion loss in [9] exhibits the great advantages of the air-gapped recta-coax structure.

The aim of this paper is to design and fabricate an air-gapped cavity bandpass filter for 5G millimeter wave frequency bands. The frequency response of the filter can be customed by controlling TPs and TZs. The proposed air-gapped cavity filter is excited by ground-signal-ground (GSG) probe pad [10] which allow the on-chip measurement and easy integration with planar circuits. The implemented bandpass filter exhibits the characteristics of wide bandwidth and low insertion loss. The detailed design and discussion are given in the following texts.

## 2 Design and Simulation

The schematic of proposed bandpass filter can be given by Fig. 1.

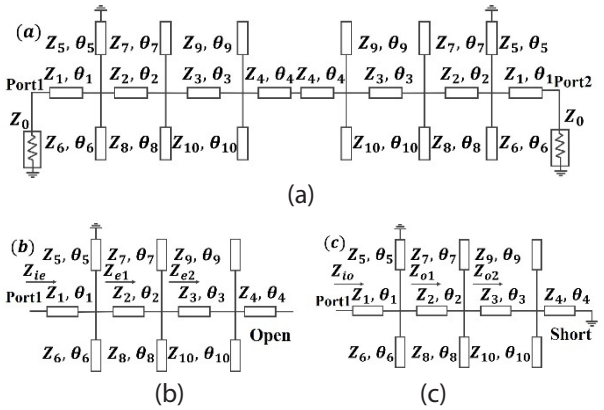


**Figure 1:** (a)schematic diagram of proposed bandpass filter (b) equivalent even-mode circuit (c) equivalent odd-mode circuit.

$Z_i$ and $\theta_i$ are the characteristic impedance and electrical length of stub lines. The open stubs ($i$ = 6, 7, 8, 9, 10) and ground stubs ($i$ = 5), as well as impedance transformation lines ($i$ = 1, 2, 3, 4) are employed to obtain multiple resonant points and desired bandwidth. The equivalent even and odd mode circuits are used to analyze the structure, and the input impedance $Z_{ie}$, $Z_{io}$ can be derived as:

$$Z_{ie} = Z_1 \frac{\left( Z_{e1} \left\| \frac{Z_6}{j\tan(\theta_6)} \right\| jZ_5\tan(\theta_5) \right) + jZ_1\tan(\theta_1)}{Z_1 + j\left( Z_{e1} \left\| \frac{Z_6}{j\tan(\theta_6)} \right\| jZ_5\tan(\theta_5) \right)\tan(\theta_1)} \quad (1)$$

$$Z_{io} = Z_1 \frac{\left( Z_{o1} \left\| \frac{Z_6}{j\tan(\theta_6)} \right\| jZ_5\tan(\theta_5) \right) + jZ_1\tan(\theta_1)}{Z_1 + j\left( Z_{o1} \left\| \frac{Z_6}{j\tan(\theta_6)} \right\| jZ_5\tan(\theta_5) \right)\tan(\theta_1)} \quad (2)$$

Where $Z_{e1}$ can be represented by $Z_{e2}$, $Z_i$ and $\theta_i = (i = 2,7,8)$, and $Z_{e2}$ can be represented by $Z_i$ and $\theta_i = (i = 3,4,9,10)$, so as the $Z_{o1}$ and $Z_{o2}$.

The S parameters of the two-port network can be represented as [11]:

$$S_{12} = S_{21} = \frac{Z_0\left(Z_{ie} - Z_{io}\right)}{\left(Z_0 + Z_{ie}\right)\left(Z_0 + Z_{io}\right)} \quad (3)$$

$$S_{11} = S_{22} = \frac{\left(Z_{ie}Z_{io} - Z_0^2\right)}{\left(Z_0 + Z_{ie}\right)\left(Z_0 + Z_{io}\right)} \quad (4)$$

The impedance at the port can be derived for impedance invariance property of the grounded stub line ($Z_5$, $\theta_5$), and it can be expressed as:

$$Z_{in} = Z_5 \frac{0 + jZ_5\tan(\theta_5)}{Z_5 + j*0*\tan(\theta_5)} = jZ_5\tan\left(\frac{\pi}{2}\frac{f}{f_0}\right) \quad (5)$$

$Z_{in}$ equals to 0 at frequency 0 and $2f_0$, which contribute TZs out-of-band. According to Eq. (3), when $Z_{ie} = Z_{io}$, $S_{12} = S_{21} = 0$, and the remaining TZs can be solved. The frequency points of TPs can be derived by $Z_{ie} = Z_{io} = 0$. However, it is hard to solve complex analytic equations, so we used EDA software for research. The initial length of the stub lines is fixed at $f_0$, and is set as quarter-wavelength. The TPs and TZs can be adjusted by $Z_i$ and $\theta_i$, good in-band return loss and bandwidth are finally obtained by appropriate parameters. Fig. 2 shows the distribution of TPs from 15GHz to 35GHz. It can be seen that three even TPs and four odd TPs are generated. TPs with frequencies below 20 GHz are significantly outside the intended design frequency range and they are difficult to adjust into the band, so the three TPs are ignored. The corresponding frequency response is shown in Fig. 3. The 24.25-27.5-GHz bandwidth is obtained, and the out-of-band rejection is better than 30dB at 22GHz and 30GHz. The return loss within band is near 20dB and there are four poles in the band.

Fig. 2 and Fig. 3 are the simulation results based on ideal transmission lines. In order to reflect the effects of actual physical structures, such as parasitic parameters and coupling effects, 3D model using air-gapped recta-

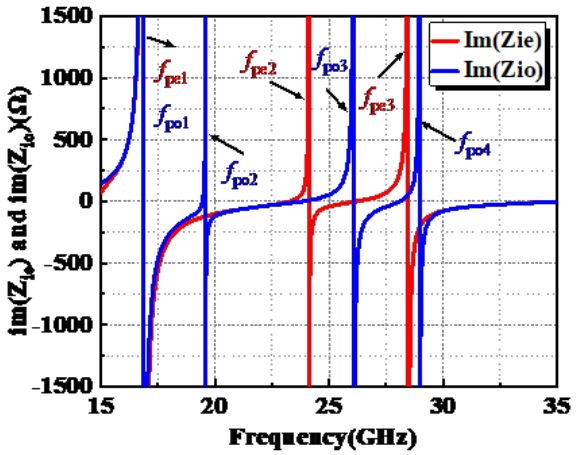


**Figure 2:** Distribution of TPs from 15GHz to 35GHz.

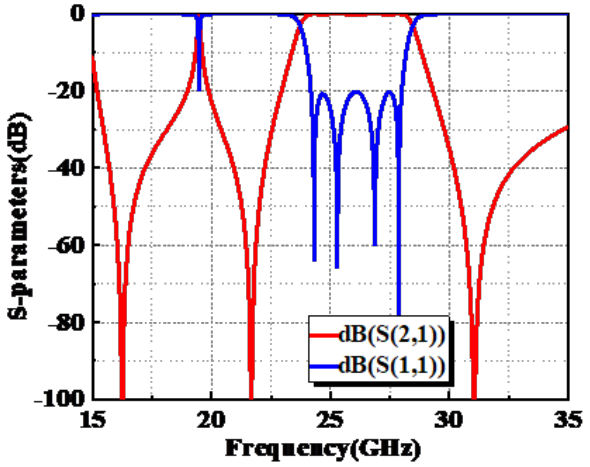


**Figure 3:** Frequency response corresponding to fig. 2.

coax is built in high frequency structure simulator. Fig. 4 shows the cross-section of five-layers recta-coax. The outer conductor and inner conductor are made by copper with height of 50 $\mu m$ for each layer. The height of inner conductor is 34 $\mu m$ for it is supported by a dielectric strap with a relative permittivity $\varepsilon_r$ about 3.2 with a height of 16 $\mu m$. The outer section is 750 $\mu m$ by 250 $\mu m$, while the inner section is 500 $\mu m$ by 150 $\mu m$. With the thickness of each layer increases, the range of impedance changes is wider, but the process complexity also increases. The 50 $\mu m$ thickness of each layer is chosen to facilitate the realization of proposed filter. The line is highly isolated, as the outer conductor is a natural shield for the field contained within the transmission line. The 750 $\mu m$ periodic release holes and dielectric support straps are arranged and have been proved by previous experiments to release photoresist effectively and provide enough mechanical strength strongly. The size of release hole is 300 $\mu m$ *x* 240 $\mu m$, and the width of dielectric support strap is 150 $\mu m$.

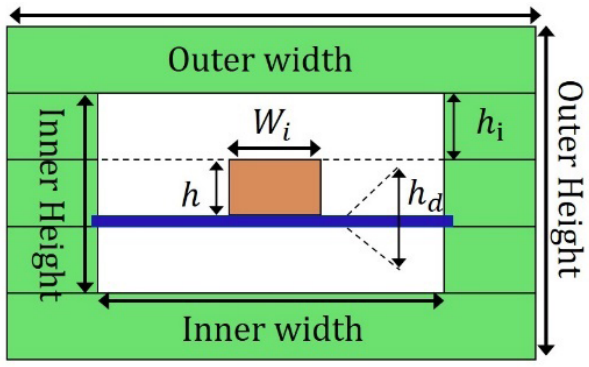


**Figure 4:** Cross-section of 5 layers recta-coax.

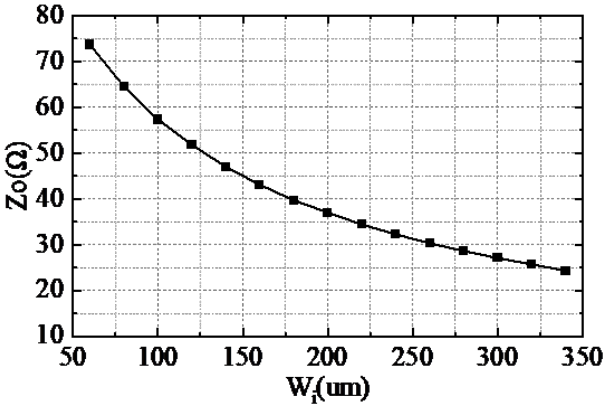


**Figure 5:** Simulated possible characteristic impedance with different $W_i$.

The physical lengths of full waveguide length at the desired frequency $f_0$ can be achieved by $c/f_0$. Different characteristic impedances are obtained by different $W_i$, and the range of possible characteristic impedances is shown in fig. 5. The initial length and width of the proposed 3D air-gapped filter using recta-coax are set according to the ideal values obtained in EDA software. The physical dimensions are optimized by finite element simulation, considering discontinuities and parasitic effects.

Fig. 6 shows the 3D view and the electric field of the 24.25-27.5-GHz bandpass filter. In order to reduce the total size of the filter, the feeder of input port and output port are bent by 90 degrees. The release holes, dielectric support straps, and GSG transitions are then added to fig. 6 to participate in optimization. The finally optimized physical dimensions of proposed 24.25-27.5-GHz bandpass filter are shown in Table 1. Fig.7 shows the finally layout of the proposed 24.25-27.5-GHz bandpass filter.

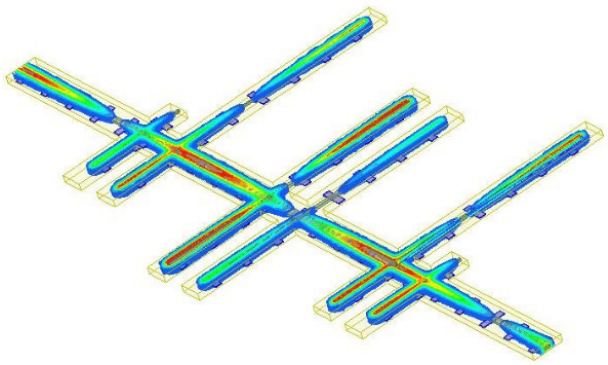

**Figure 6:** 3D view and the electric field of the 24.25-27.5-GHz bandpass filter.

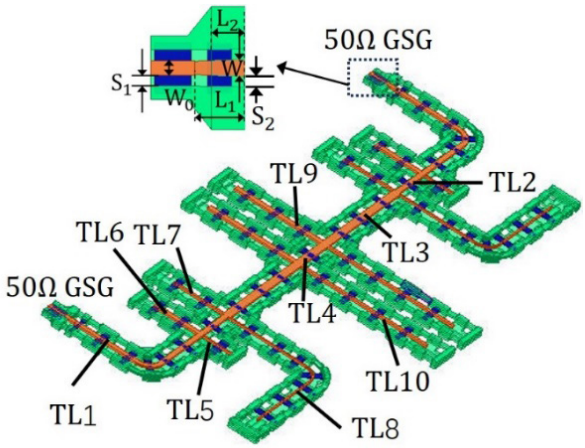


**Figure 7:** Layout of the proposed 24.25-27.5-GHz bandpass filter.

**Table 1:** Optimized physical dimensions of proposed 24.25-27.5-GHz bandpass filter (Unit: $\mu m$).

| TL | $Z_i$, $\theta i$ | Wi | length | GSG | |
|---|---|---|---|---|---|
| TL1 | $Z_1$, $\theta_1$ | 105 | 3243 | $W_0$ | 90 |
| TL2 | $Z_2$, $\theta_2$ | 118 | 866 | W | 107 |
| TL3 | $Z_3$, $\theta_3$ | 157 | 2551 | $S_1$ | 50 |
| TL4 | $Z_4$, $\theta_4$ | 157 | 485 | $S_2$ | 37.5 |
| TL5 | $Z_5$, $\theta_5$ | 45 | 727 | $L_1$ | 340 |
| TL6 | $Z_6$, $\theta_6$ | 108 | 1178 | $L_2$ | 180 |
| TL7 | $Z_7$, $\theta_7$ | 52 | 1350 | height | |
| TL8 | $Z_8$, $\theta_8$ | 36 | 4085 | h | 34 |
| TL9 | $Z_9$, $\theta_9$ | 112 | 2300 | $h_i$ | 50 |
| TL10 | $Z_{10}$, $\theta_{10}$ | 68 | 3250 | $H_d$ | 16 |

Fig. 8 plots the S-parameters of the proposed 24.25-27.5-GHz bandpass filter. Within the 24.25-27.5-GHz passband, the insertion loss is less than 0.7dB, and the return loss is near -20dB. The out-of-band rejection is better than 38dB at 22GHz and 30GHz.

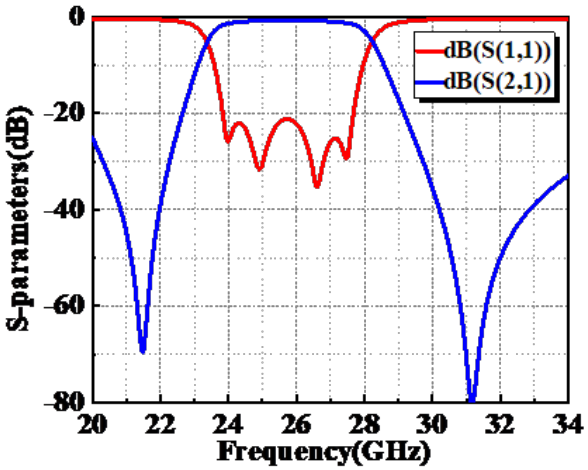


**Figure 8:** S-parameters of the proposed 24.25-27.5-GHz bandpass filter.

## 3 Fabrication and measurement

The air-gapped cavity filter is fabricated using standard MEMS processes on a silicon substrate with a thickness of 700 $\mu m$. Fig. 9 shows the detailed steps, including repeated deposition, lithography and electroplating processes. Finally, photoresist is removed through release holes, leaving a wafer filled with recta-coax.

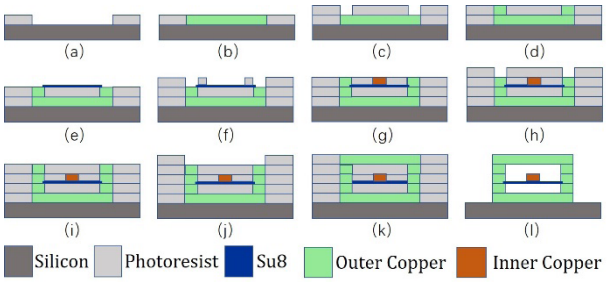


**Figure 9:** standard MEMS processes for recta-coax (a) lithography (b) electroplating and planarization (c) Photoresist spun and patterned (d) second copper layer is formed (e)deposition of dielectric strap (f) ~(k) repeat the previous steps (l) Photoresist is removed through release holes.

Fig. 10 shows the partial microscopic photograph of the proposed bandpass filter, and the conductors stacked on top of each other, as well as release holes can be seen clearly. The global photograph of the filter is shown in Fig. 11 with size of 9670 $\mu m$ x 5550 $\mu m$ x 250 $\mu m$. The filter was measured using a vector network analyzer, and the simulated and measured results are plotted for comparison in fig. 12. The measured center frequency is 25.875GHz with fractional bandwidth (FBW) of 12.5%, and a frequency shift of 120MHz (<0.5%) is observed between the simulated and measured re-

sults. Within 24.25-27.5-GHz bandpass, the measured minimum insertion loss is 0.9dB, which is 0.2dB larger than the simulation result. In addition, the return loss of a better sample is less than -14dB.

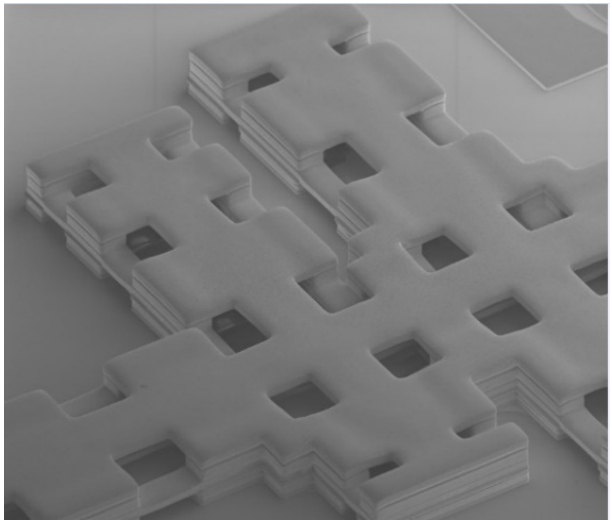

**Figure 10:** Partial microscopic photograph of the proposed bandpass filter.

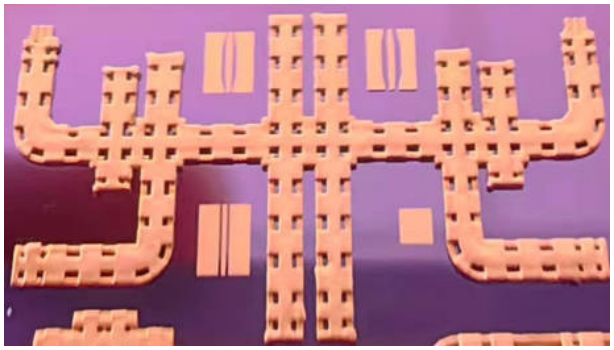

**Figure 11:** Photograph of the proposed filter.

The reason for differences between measured and simulated results is the inaccuracies of the manufacturing and measurement. The fabrication error includes over-etching, surface roughness, deviation of thickness. During the photoresist removal process, the etching solution might not react adequately with the photoresist, resulting in an incomplete removal. The deviations from the ideal structure mentioned above can result in changes to the equivalent capacitance or inductance of the filter structure, thereby degrading its performance. With the advancement of process technology, there is hope for further enhancing the performance of the filters.

**Table 2:** Performance comparison with some reported bandpass filters and proposed filters.

| Ref | Form | $f_0$ (GHz) | FBW (%) | IL (dB) | Size mm$^3$ |
|---|---|---|---|---|---|
| This work | Recta-coax | 25.875 | 12.5 | 1.4 | 13 |
| [12] | SIW (Si) | 29.8 | 5 | 3.5 | 4 |
| [13] | SIW (PCB) | 21 | 1.59 | 1.1 | 4219 |
| [14] | Recta-coax | 36 | 0.59 | 2.57 | 16 |

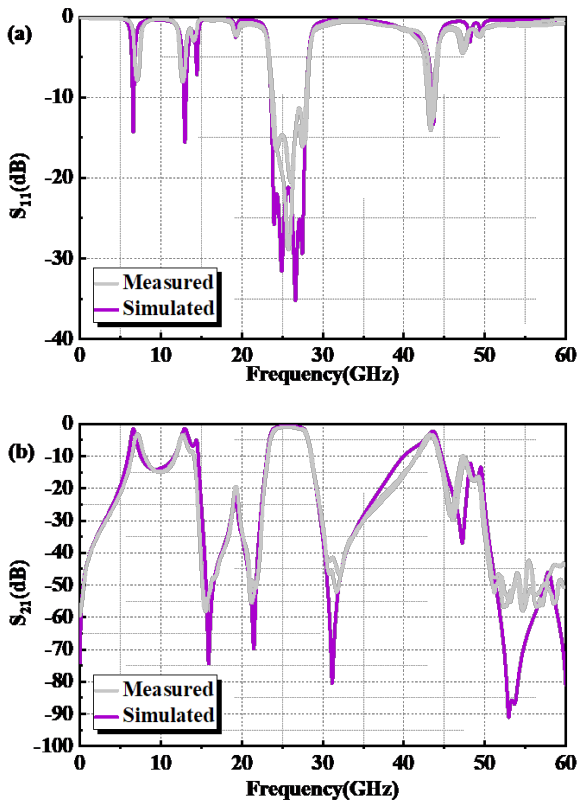


**Figure 12:** Measured and simulated results of the proposed filter (a) S11 (b) S21

Table 2 presents a comparison between some typical bandpass filters for 5G millimeter wave applications and the proposed structures. Filters using silicon based SIW technology in [12], has a compact structure and high selectivity, but suffer from relatively high insertion loss. The PCB-based SIW technology in [13] has mature manufacturing and low cost, but has very big footprint. Compare with recta-coax based filter in [14], a wider frequency response and lower loss have been successfully achieved. Furthermore, the 3-D air-gapped cavity enhances heat dissipation compared to planar circuits and boosts power handling capability.

## 4 Conclusions

A 24.25-27.5-GHz air-gapped cavity bandpass filter using MEMS process is presented in this study. Measured results show that the proposed 24.25-27.5-GHz band pass filter

has the merits of low loss, wide bandwidth, and high out-of-band rejection. The proposed 24.25-27.5-GHz bandpass filter has the potential advantages in the application of the 5G millimeter wave wireless communication system, satellite communications, RF telemetry, and so on.

## 5 Acknowledgments

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## 6 Conflict of interest

The authors declare no conflict of interest.

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# A Beam-Split and Gain-Enhanced Patch Antenna Using Metamaterial Superstrate for Wireless Communications

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**Abstract:** This paper proposes multiband antenna-based Metamaterial (MTM) for beam splitting and gains improvement. Here, the focus is on developing the smart antenna using a Metamaterial Superstrate technique for modern wireless applications. The proposed antenna consists of two patches, the first one has a square shape placed on a Taconic FR-30 substrate, followed by the second patch constructed as a meander ring with two stubs for increasing the generated frequency bands. At the end of the design process, the proposed patch seems U-shaped to ensure the antenna beam is splitting at the desired frequency bands. In addition, the capacitive coupling is used for exciting the second patch, whereas the first patch is excited by conduction with a 50 Ω discrete port. Furthermore, a metasurface layer is designed and mounted on the second patch as a superstrate to increase the antenna gain toward the bore-sight direction. The results show a maximum gain of 8 dBi at 4.2 GHz with maximum dimensions of 108 × 108 mm2. Moreover, this antenna operates at additional frequency bands (2.6 GHz, 4.2 GHz, and 5.6 GHz), with a minimum reflection coefficient of -16.8 dB, -12.3 dB, and -30.6 dB, respectively. The proposed antenna is designed and analyzed using the CST MWS simulator.

**Keywords:** patch antenna, metamaterial, superstrate, gain, beam splitting

# Krpična antena z razcepljenim snopom in povečanim dobitkom z uporabo metamaterialne podlage za brezžične komunikacije

**Izvleček:** Članek predlaga večpasovno anteno na osnovi metamateriala (MTM) za razdelitev snopa in izboljšanje dobička. Pri tem se osredotočamo na razvoj pametne antene s tehniko metamaterialnega superstrata za sodobne brezžične aplikacije. Predlagana antena je sestavljena iz dveh krpic, prva je kvadratne oblike in je nameščena na substrat Taconic FR-30, sledi ji druga krpica, zgrajena kot meandrski obroč z dvema krakoma za povečanje generiranih frekvenčnih pasov. Predlagana krpica je v obliki črke U, da se zagotovi, da se antenski žarek razdeli na želene frekvenčne pasove. Poleg tega se za vzbujanje druge krpice uporablja kapacitivi sklop, medtem ko se prva krpica vzbuja s prevodnostjo z diskretnim priključkom 50 Ω. Poleg tega je zasnovana in nameščena metapovršinska plast na drugo krpico kot superstrat za povečanje ojačitev antene. Rezultati kažejo največje ojačenje 8 dBi pri frekvenci 4,2 GHz z največjimi dimenzijami 108 × 108 mm2. Poleg tega antena deluje v dodatnih frekvenčnih pasovih (2,6 GHz, 4,2 GHz in 5,6 GHz) z najmanjšim koeficientom odboja -16,8 dB, -12,3 dB in -30,6 dB. Predlagana antena je zasnovana in analizirana s simulatorjem CST MWS.

**Ključne besede:** krpična antena, metamaterial, superstrat, ojačenje, delitev žarka

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## 1 Introduction

The rapid development of wireless communications pushed the user to become greedy to obtain the highest capacity and high speed, and this rapid development in the next generations of communications [1]. The fifth generation (5G) helped change the concept of speed and high productivity. On the other hand, this development needs a high gain. Therefore, arrays are proposed in several research to get the best results in terms of high gain and the ability to change the system's characteristics and avoid interference [2, 3]. Multi-beam antennas are used in many fields, whether in communications or in other areas. These antennas are assembled in fifth-generation stations to obtain better compatibility, high capacity, and efficiency [4, 5]. In wireless communications, especially in the fifth generation, the antennas must be different from the rest of the generations in terms of weight and size, Therefore, microstrip antennas are used to improve the performance of the antennas with their integration using planar manufacturing [6, 7].

The proposed structure consists of three main parts, as shown in Fig. 1. The first part is the microstate antenna based on a square patch. The antenna is excited with a 50 Ω input impudence along with weight. The second part is represented as a Hilbert U-shaped structure of the second iteration. The proposed Hilbert is designed as an open fractal which excited with T-ring stubs, as shown in figure 1 (c). The loop of two rings helps achieve minimum field fringing [8]; this would realize surface current mitigation to a certain direction that reduces the back radiation [9]. Besides that, the advantage of introducing the proposed T-ring steps is accumulating electrical charges which excites the proposed Hilbert U-shaped capacitively to improve the bandwidth [10].

Meanwhile, the proposed U-turns are proposed to achieve multiple frequency harmonic generation from the fractal corner. Moreover, fractal geometric provides a significant size reduction [11]. Finally, the proposed antenna has a symmetrical profile around the length and an asymmetrical shape along the weight. Hence, the basic antenna radiation would be asymmetrical around the importance of generating beam splitting [12]. This helps the designer develop a stigmatized wave configuration [13]; the antenna beam could be focused significantly with minimum size reduction, which will be further explained in the next paragraph after the Metasurface layer introduction and realize beam splitting at the same time. This is due to the creation of two areas with high concentrations of the surface current on the second patch, which inherently increases the beam splitting around the antenna length [14, 15].

Next, the metamaterial (MTM) is designed and integrated with a proposed antenna to maximize the antenna gain in the bore-sight direction [16]. Finally, the proposed metamaterial is structured in an asymmetrical form.

This paper is organized as follows. Section II presents the antenna configuration and design procedures for the proposed structure, followed by simulation results in Section III. Then, the metamaterial cases results are demonstrated in section IV. Finally, some concluding remarks are discussed in Section V.

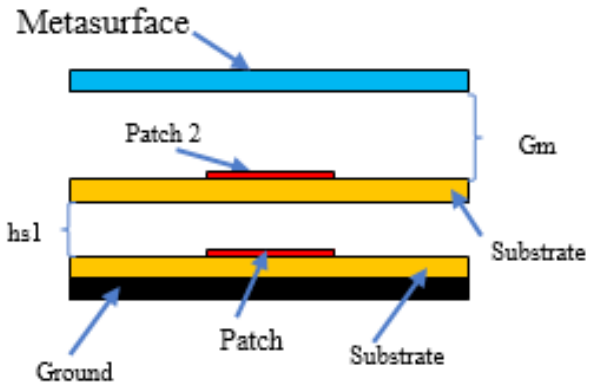



**Figure 1**: Schematic view of the antenna.

### 1.1 Design of U-shape cell

In this section, the second patch with a U-shape structure is designed, and its dimensions are (a width of 71.28 mm and a length of 66.47 mm). Different attempts are performed to adjust the dimensions of the U-shape patch length and width for various thicknesses to get better results of the antenna performance. The basic structure of the U-shape proposed antenna is portrayed in Fig.2.

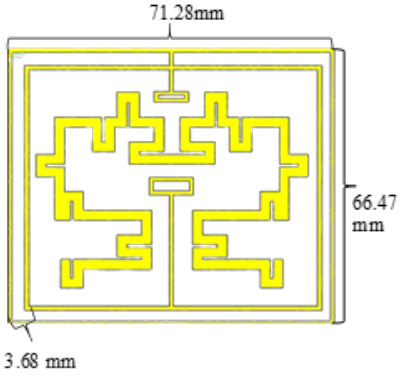



**Figure 2:** U-shape antenna.

### *1.2 Design of microstrip patch antenna*

Several methods have been proposed in designing patch antennas (PN), and the most popular model is the transmission line model (*TL*). It models the rectangular patch (RP) as two slots separated by a low impedance transmission line (Zc) of length *L*. In this study, the proposed patch antenna is designed using a Taconic FR-30 substrate with a width and length of 50 mm, respectively (see Fig. 3).

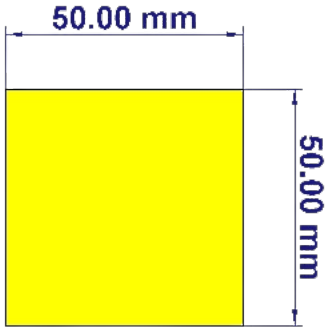



**Figure 3:** Patch dimensions.

### *1.3 Metamaterial unit cell structure*

The MTM is used with a certain distance from the substrate [17], as shown in Fig. 1. This method prepares the radio transmitters in the same direction as the antenna and works to increase the antenna gain [18]. Designing MTM depends mainly on the frequencies at which they will work. In this research, the study of effect of square precipitation on the antenna to obtain the best result. MTM are placed over the supersubstate focus with the patch to correct the radiation emitted [19, 20]. After checking the antenna in terms of the first layer, it caused an increase in the outgoing radiation, so the first layer is considered a source was feeding for the second layer, and the second layer caused the radiation to split into two beams and make it more directed [21, 22]. The distance between the layers determines the best possible result, as shown in Table 1. Also, the distance between the layers and the MTM is discussed, as illustrated in Table 2, and this inferred distance is the best possible result. In the case of the search for the presence of two layers of the substrate in the manufactured antenna, the distance between the first layer of the ground layer must be $\lambda/3$ [23, 24]. And the distance between the second layer and the first layer, $\lambda/2$ to $\lambda$, $\lambda/3$ is the wavelength of the antenna frequency in free space. Therefore, the metamaterials layer of the second layer is the distance $\lambda/4$ [25]. Fig. 4 shows a metamaterial unit cell configuration.

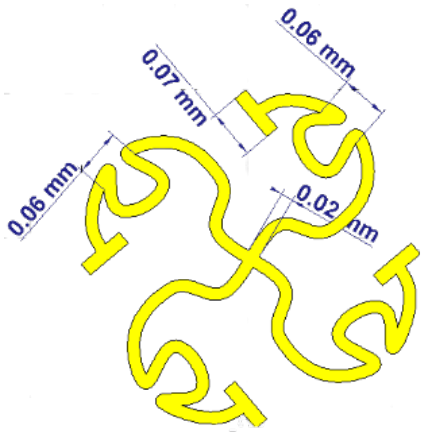



**Figure 4:** Metamaterial unit cell.

### *1.4 Superstrate*

The aim of designing the supersubstate materials is to enhance and increase the antenna gain by creating a high electric field above the substrate phase. This helps to control the practice of transmitting radiation by making holes inside the Superstrate, which reduces the permittivity. This process is achieved by reducing the

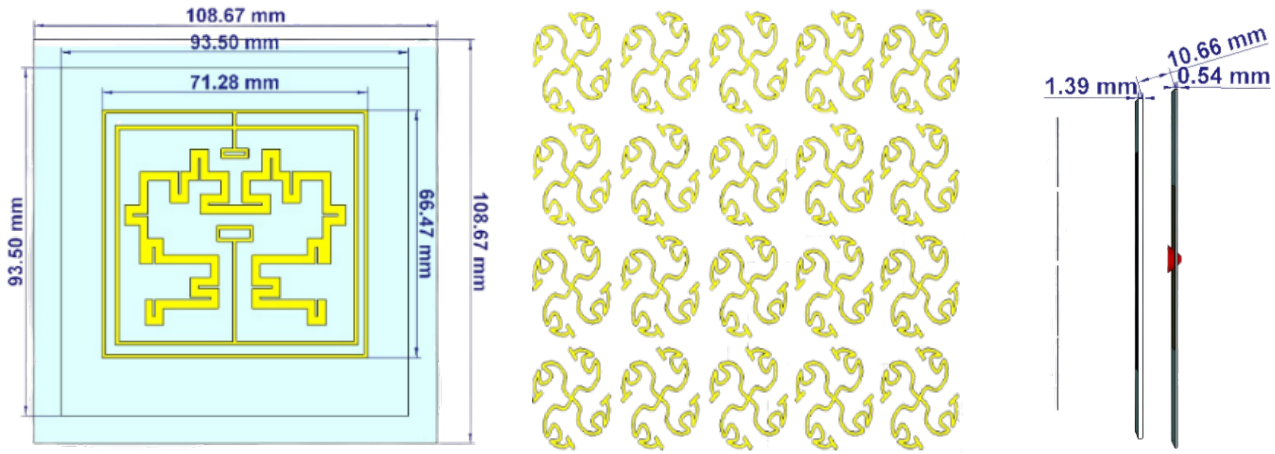



**Figure 5:** Overall antenna structure.

front-to-back ratio (FBR), which increases the antenna's efficiency and improves the gain and in turns, achieving the best antenna performance [13, 26].

## 2 Antenna configuration

This section describes the design details of the patch antenna with a superstrate placed at an optimum level. The configuration of a three-patches antenna array with the Superstrate is shown in Fig. 5. The lower substrate layer is backed by a ground plane. The overall dimension of the antenna structure is illustrated in Table 1. The space between the lower, upper, and Superstrate is 10.66 mm. Four U-shape patches, each of size 71.28 mm × 66.47 mm, are printed on the upper surface of the upper substrate. The feed is (-10.5, -2.5), with the patch elements fed using a corporate feed with quarter-wave impedance transformers. The lower layer of the Superstrate consists of a patch of square apertures in a ground plane, with the gap between the patch and the metamaterial layer being $d$ = 29.52 mm.

**Table 1:** Values of the antenna parameters

| Name | Parameter | Value (mm) |
|---|---|---|
| Subst 1 | A1 | 108.67 |
| | B1 | 108.67 |
| Subst 2 | A2 | 93.5 |
| | B2 | 93.5 |
| Gap between Subst | Hs1 | 10.6 |
| Thickness of upper substrate | h1 | 0.54 |
| Thickness of lower substrate | h2 | 1.39 |
| Patch 1 | A | 50 |
| | B | 50 |
| Patch 2 | A | 71.28 |
| | B | 66.47 |
| Metasurface width | MW | 88.24 |
| Metasurface high | MH | 88.25 |
| Gap Metasurface and patch 2 | Gm | 28.25 |

## 3 Results and discussion

To discuss the principal work of the proposed antennas, the designer first understands the effect of antenna structure on the gain and reflection coefficient parameters. So, the antenna in the first part is designed as a rectangle (traditional antenna). Next, the second part is modified using the U-shaped superstructure, followed by the MTM design with a matrix of (5 × 4) at the last step of the designing process. Finally, the parameters of S are calculated individually for each unit. The three modes are portrayed in Fig. 6. Results obtained in Fig. 7 demonstrated the minimum reflection coefficient achieved at 2.68 GHz.

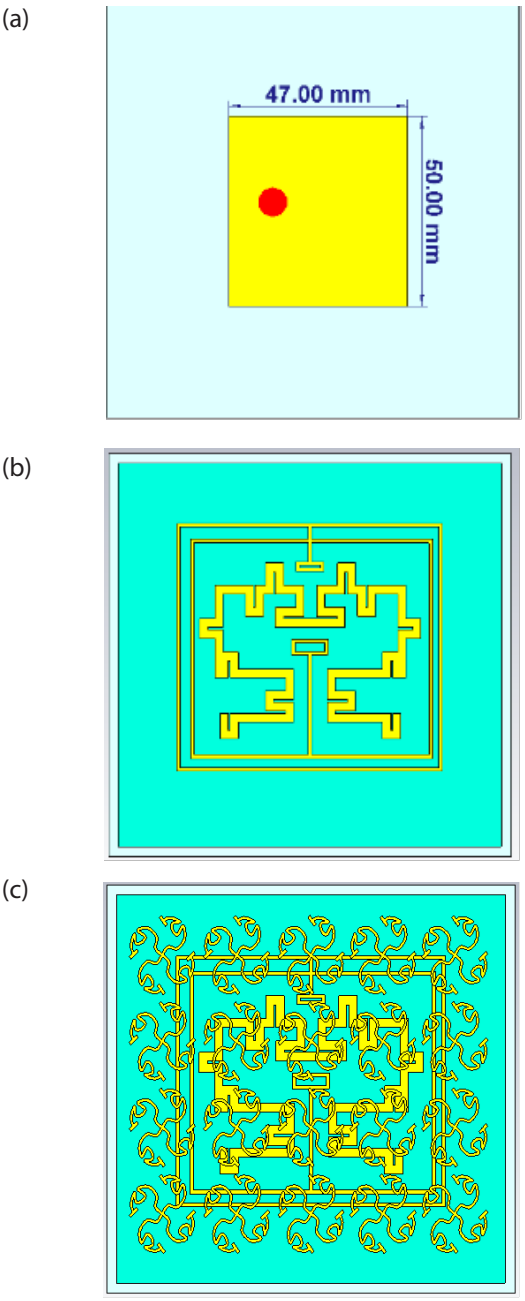



**Figure 6:** The structure of the antenna (a) patch plane (b) the supersubstate with U-shape (c) the MTM design.

Moreover, it's noted that the gain is significantly increased to a high value by using the MTM at 5.4 GHz, attained to 8.61 dBi. From the results illustrated in Fig. 8, it is found that the antenna achieves a high gain at the frequencies of 4.7, 4.9, and 5.5 GHz, and this is due to the current distributions between the radiator and the ground plane, which leads to an increase in the gain and bandwidth in the antenna while decreasing the value of the reflection coefficient at certain frequency.

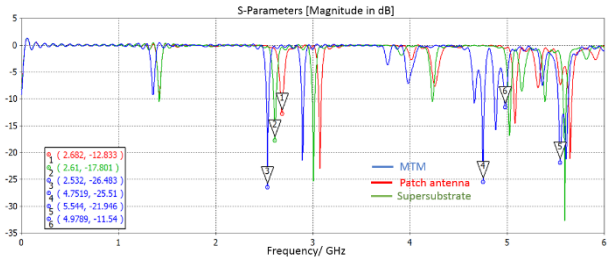



**Figure 7:** Reflection coefficient results of the proposed antenna at different cases of design.

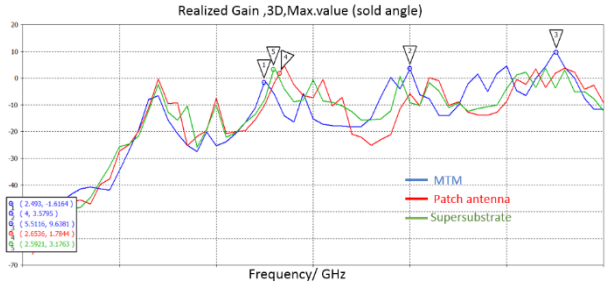



**Figure 8**: Gain results of the proposed antenna at different cases of design.

To further explain the idea of the split property, Fig. 9 shows the step-by-step evaluation process of the surface current distribution of the antenna. Firstly, the structure proposed of the antenna arranges the split beam property, and the unit cells are rearranged to produce opposite current flow. Then, by observing the current flow for every two cells in one column, the beam is directed differently.

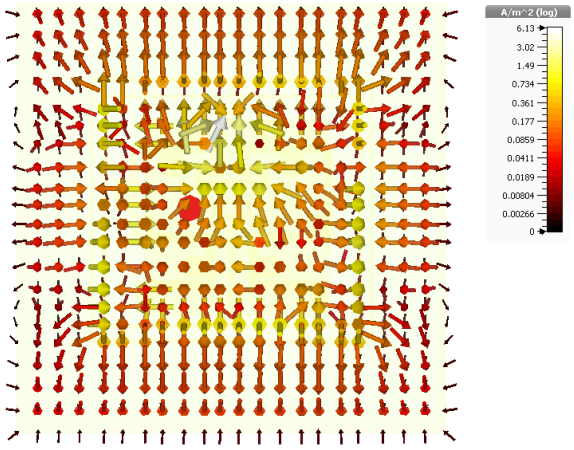



**Figure 9:** Current distribution of the antenna.

# 4 Results of metamaterial cases

## 4.1 Even number of MTM arrays

In telecommunication networks, especially antennas, the antenna's dimensions, gain, and reflection coefficient significantly impact the antenna's performance. Hence, this study aims to design and use MTM with an even number or odd arrays for observing the effects on the antenna's efficiency. Based on the results in Fig. 10, matrices significantly improved some frequencies. In this paragraph, the even number is adopted in the MTM matrix, represented as (2 × 2), (4 × 4), (8 × 8), and (10 × 10). As a result, as the number of matrices is increasing, the reflection coefficient increases and achieves (-15.8, -15.8, -10.5, -9.8) dB at 2.6 GHz at various matrices sizes.

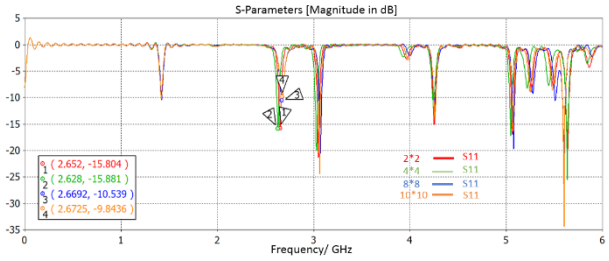



**Figure 10:** Reflection coefficient results of even MTM.

At a frequency of 2.6 GHz at (4 × 4) matrix, the result demonstrated a minimum reflection coefficient compared with the rest of the results at other operating frequencies. On the other hand, the gain result at the frequency of 2.6 GHz is 4.33 dBi, as shown in Fig. 11, which also includes the gains result at the rest of the frequencies. For this, results achieved at (4 × 4) MTM are more acceptable among the other matrices of the even array.

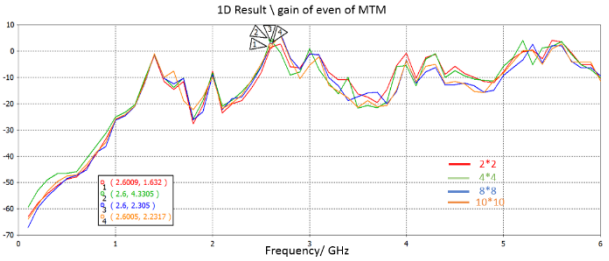



**Figure 11:** Realized gain results at different MTM even arrays.

## 4.2 Odd number of MTM arrays

The second part of this section is to make an individual matrix of numbers (3 × 3), (5 × 5), (7 × 7), and (9 × 9). The results illustrated that the reflection coefficient parameter at (5 × 5) is -16.882 dB at 2.6 GHz, as shown in Fig. 12. On the other hand, it's observed that this value

is slightly deteriorated at the (9 × 9) matrix due to the impact of antenna size.

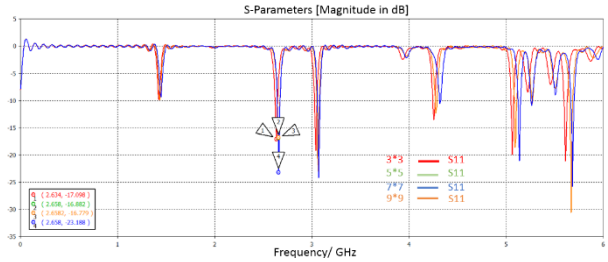



**Figure 12:** Reflection coefficient results of odd MTM.

In addition, the results show that the (5 × 5) matrix is more appropriate for achieving a minimum reflection coefficient but with less gain. Thus, at a frequency of 2.6 GHz, the gain attained 1.18 dBi, as shown on Fig. 13. The MTM designing process depends on using the even and odd matrices.

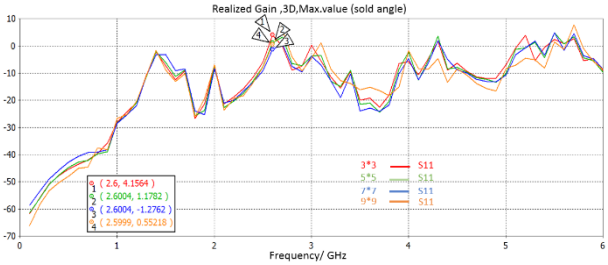



**Figure 13:** Realized gain results at different MTM odd arrays.

### *4.3 Hyper MTM array*

This section presents the simulation results of the metasurface structure integrated with the antenna. The results obtained using the CST simulator software represent the reflection coefficient and the radiation. Results show that five resonant frequencies were obtained at (2.6, 3, 4.2, 5.2, and 5.6) GHz (see Fig. 14).

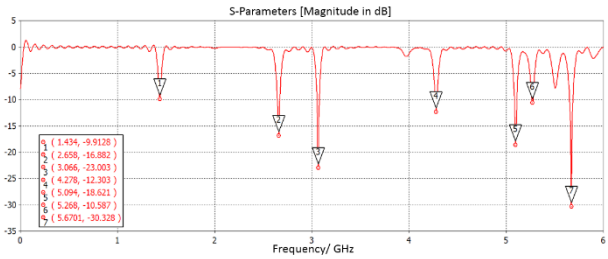



**Figure 14:** Reflection coefficient results of hyper MTM.

The analysis and simulation in Fig. 15 (a), (b), (c), and (d) indicate that bare Microstrip patch antenna (MPA) has a radiation efficiency of 73% at a frequency of 2.6 GHz. The spread beam with the main lobe direction toward is 34 deg. The offender side lobe showed a result of -1.3 dB. At a frequency of 3 GHz, the one beam with the

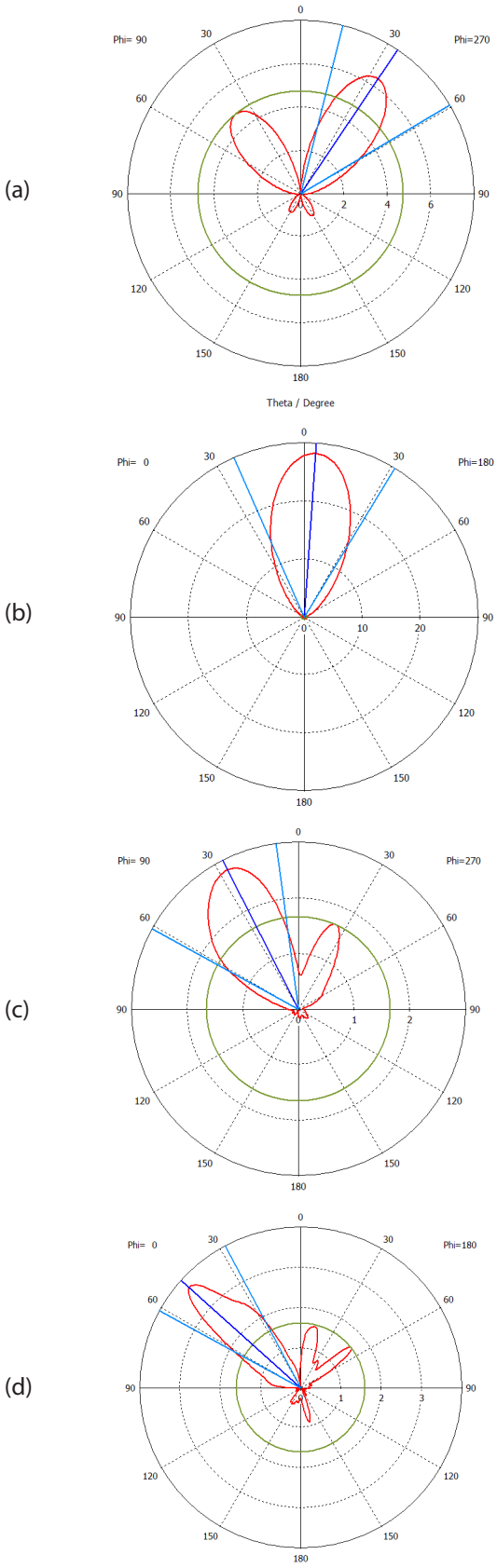
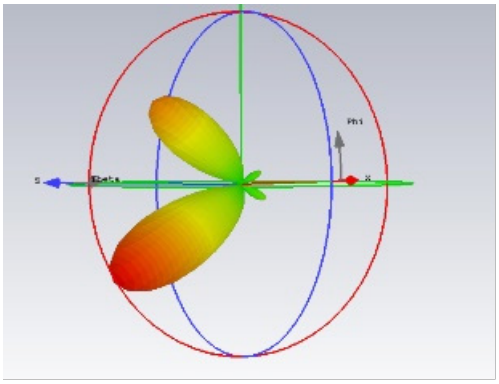



**Figure 15:** Radiation pattern of the metasurface antenna (a) split beam in 2.6 GHz, (b) one beam in 3 GHz, (c) split beam in 4.2 GHz, (d) split-beam in 5.6 GHz.

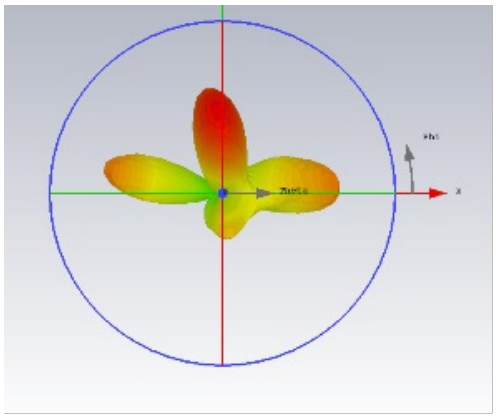
main lobe direction toward is 4 deg, and the offender side lobe showed a result of -17 dB with a radiation efficiency of 99%. Besides that, at a frequency of 4.2 GHz, the one two-beam with the main lobe direction goes toward 27 deg. The offender side lobe showed a -2.3 dB with a radiation efficiency of 32%. Moreover, at the frequency of 5.6 GHz, the one beam with the main route is clearly shown toward 48 deg. Meanwhile, the offender side lobe demonstrated a -3.7 dB with a radiation efficiency of 37%.

Next, Fig. 16 shows the 3-dimensional results of the antenna, which shows the splitting in the radiation pattern based on the antenna with the MTM structure. Moreover, the antenna proposed in this work is compared

(a)



(b)



(c)

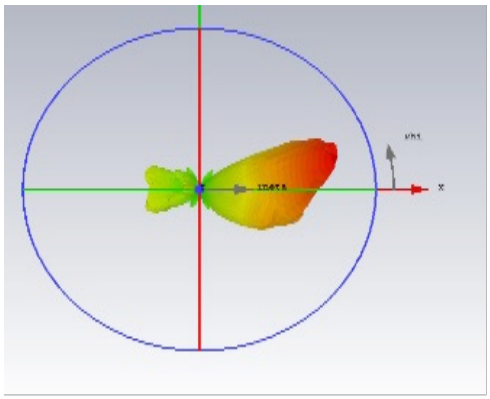


**Figure 16:** 3D radiation pattern of the antenna (a): at 2.6 GHz, (b): at 4.2 GHz, (c): at 5.6 GHz.

with other studies in literature in terms of the operating frequency, antenna dimensions, gain, techniques used, and beam split. This comparison and the overall results of the antenna at different cases of split degrees are summarized in Tables III and IV, respectively.

**Table 2:** comparison of the proposed antenna with others works in literature

| Ref. | Frequency band (GHz) | Size (mm) | Gain (dBi) | Technique | Bean split |
|---|---|---|---|---|---|
| [18] | (4.95 - 5.42 | 65 × 65 × 4.862 | 8.62 | metasurface | Yes / Two |
| [26] | 3.5 | 300 ×300 | 2.3/ | MS supersubstrate | Yes / Two |
| [27] | (11.2/12.2) | 96 ×13 | 13 | Pin diode / two feed | NO |
| This work | 2.6/4.2/5.6 | 108 ×108 | 8.2/4.49 /6.24 | supersubstrate | Yes / Three |

**Table 3:** Summary of the antenna results

| fr (GHz) | Reflection coefficient (dB) | Gain (dBi) | Total eff. | Spilt deg. |
|---|---|---|---|---|
| 2.6 | -16.8 | 8.04 | 76.9% | Two lobs |
| 4.2 | -12.3 | 4.49 | 84.9% | Three lobs |
| 5.6 | -30.6 | 6.24 | 83.8% | No lobs |

## 5 Conclusions

This work presented a MTM antenna based on supersubstate and U-shaped unit cells for improving the antenna's gain and splitting beam. The proposed antenna operates at frequency bands of 2.6 GHz, 4.2 GHz, and 5.6 GHz with a minimum reflection coefficient of -16.8 dB, -12.3 dB, and -30.6 dB, respectively. The proposed antenna is designed and analyzed using the CST MWS. As a result, a gain is improved to 8.04 dBi, 4.49 dBi and 6.24dBi at the broad side of the direction of the antenna at the required impedance bandwidth. In addition, a split beam is significantly observed in the E-plane with a 2.65 dBi gain for each beam.

## 6 Conflict of interest

The authors declare no conflict of interest.

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# Multi-user Task Offloading for Mobile Edge Computing Based on Reinforcement Learning

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**Abstract:** Mobile Edge computing (MEC) enables network functions and control programmable and operates key constituents of social networks in terms of increasing user's support on devices to carry out compute. It requires traffic offloading and task scheduling to improve the storage and fast computing. In this paper, a novel method, including data driven traffic modeling enabled by a Reinforcement learning algorithm (RLTOA), is proposed for offloading traffic and improving the computing speed and minimizing the application latency of the social network. The result of the proposed data driven modeling is compared with existing methods and validate how the data driven traffic modeling for providing the computation offloading service in terms of energy budget and the mobile drop and execution of edge server. The presented computation offloading, and energy management solutions can provide valuable perceptions for practical applications of MEC. Extensive numerical findings are presented to endorse the efficacy of RLTOA and display the effect of the social network requirement.

**Keywords:** MEC; Reinforcement Learning; Traffic offloading; Task scheduling

# Razbremenitev večuporabniških nalog za mobilno robno računalništvo na podlagi okrepljenega učenja

**Izvleček:** Mobilno robno računalništvo (MEC) omogoča programiranje omrežnih funkcij in nadzora ter upravlja ključne sestavne dele družbenih omrežij z vidika povečanja podpore uporabnikom na napravah za izvajanje računalniških operacij. Za izboljšanje shranjevanja in hitrega računalniškega delovanja je potrebno razbremenjevanje prometa in načrtovanje nalog. V članku je predlagana nova metoda, vključno z modeliranjem prometa na podlagi podatkov, ki ga omogoča algoritem okrepljenega učenja (RLTOA), za razbremenitev prometa in izboljšanje hitrosti računalniškega obdelovanja ter zmanjšanje zakasnitve aplikacij družbenega omrežja. Rezultat predlaganega modeliranja na podlagi podatkov so primerjani z obstoječimi metodami in potrjujejo modeliranje prometa na podlagi podatkov za zagotavljanje storitve razbremenitve računalniških operacij v smislu energijskega proračuna in mobilnega padca ter izvajanja robnega strežnika. Predstavljene rešitve za razbremenitev računalniških operacij in upravljanje z energijo lahko zagotovijo dragocene ugotovitve za praktične aplikacije MEC. Predstavljeni so obsežni numerični rezultati, ki potrjujejo učinkovitost RLTOA in prikazujejo učinek zahtev družbenega omrežja.

**Ključne besede:** MEC; okrepljeno učenje; razbremenitev prometa; načtovanje nalog

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## 1 Introduction

Beyond 5G network (B5G) is assessed through the intensive and sensitive applications through traffic and computation offloading by increasing computational capacity to the edge of B5G networks. Reinforcement Learning (RL) can solve this problem using sparse and inaccurate network data. In this paper, we employ RL to develop an ideal task scheduling and computation offloading technique that reduces system energy usage. A framework for reinforcement learning based

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edge computing is introduced in B5G networks for mobile edge computing (MEC) server for social related network applications and for battery-powered and resource-controlled devices [1]. In this paradigm, these social related delay-sensitive applications are shifted from resident users to nearby network edge server; edge computing is a promising technology to address the problem [2]. Since the processing capacity of these pervasive mobile edge servers are frequently constrained, offloading all work from devices to edge servers may, on the other hand, result in larger latency. [3-5] Additionally, compute task offloading, particularly in 5G networks that are diverse and ultra-dense, can result in increased interference and unanticipated transmission delays. On the other hand, local computing can considerably minimize the latency of job execution [6]. The contradiction is found between computation delay with energy consumption is essentially what determines whether to execute tasks locally or offload them when creating an offloading strategy [7-9]. There are various algorithms focusing on minimizing the transmitted powers, and to maximize throughput [10]. In the framework of the B5G network, computation complexity and task scheduling are handled by means of adding Small base stations (BS) as indoor base stations that have expanded significant attention [11]. Heterogeneous network (Hetnet) comprises of Macro BS (MBS) overlapped with small BS (SBS) and an autonomous power distribution is possible with the aid of RL. This heterogeneity structure offers features such as network data rate, connectivity, and energy efficiency [12-16]. In this B5G Hetnet, Co-operative and distributive learning outcomes optimization have been playing significant role in addressing energy related problem [17-22]. Many researchers suggested binary offloading and partial offloading to adopt the system flexibly [23], the game-theoretic modeling and the quadratic programs are also implemented with non-convex optimization. Then, the design concepts for B5G networks with MEC are different from those for MEC systems with SBS to minimize system energy consumption. A deep Q-Network (DQN) is based on the reinforcement learning working with deep neural networks, enabling more effective decision-making in complex MEC environments. Battery-powered device systems are preferable in B5G networks [24]. Collaborative design is important in task offloading since it is difficult to make decision on when to offload and when to execute, in this case, the key parameters are the CPU-cycle frequencies and time interval for execution [25]. The design goal is to minimize battery energy usage to optimize computation performance in contrast to MEC systems with battery-powered components. Along with these novel design considerations, managing the service constraints and the battery energy dynamics presents additional difficulties, this paper contributes to reduce the latency and computational cycle of MEC server using RL algorithm. The key ideas of this research are as follows:
By jointly optimizing the offloading decision, compute the total computation capability, energy consumption, and battery energy. The co-operative problem is formulated.

To optimize the traffic offloading process, the Enhanced RL algorithm is introduced so that the decision making of task scheduling and computational speed is increased. In each time slot, the algorithm tries to optimize the CPU-cycle frequency and battery energy through trial and error.

To analyze and compare the simulated results with prevailing algorithms reported with greedy allocation so as to impart the effectiveness of the proposed RL based MEC system

The articulation of proposed B5G MEC system is illustrated in Section 2 and figure 1. The experimental findings and a comparison with the current approaches are discussed open in Section 3. The conclusion part is given in Section 4.

## 2 System methodology

MEC is an effective system to equip the management of mobile devices and is illustrated in figure 1. MEC server acts as a cloud head and runs a virtual machine offloading the computational task for edge mobile users. We consider the communication model consists of one macrocell and smallcells which are surrounded by the mobile devices and MEC server. The Euclidean distance between the macrocell and MEC server is defined as

$$d_{j,t} = \sqrt{\| w_t^{MC} - w_{j,t}^{MEC} \|^2}, \ \forall t \in \mathfrak{F}, j \in \mathrm{M}. \quad (1)$$

The channel gain between communication model is considered as free space path loss and is denoted as

$$h_{j,t} = \eta d_{j,t}^{-2} = \frac{\eta}{\| w_t^{MC} - w_{j,t}^{MEC} \|^2} \ \forall t \in \mathfrak{F}, j \in \mathrm{M}. \quad (2)$$

Frequency division multiple access serves the time intervals between the MEC server and all users. The complete bandwidth is divided into G smaller bands and each mobile device gets assigned B5G bands.[4] The signal-to-noise ratio (SNR) is calculated as

$$SNR_{j,t} = \frac{h_{j,t} P_{j,t}}{\mu B / G} \quad (3)$$

$$SNR_{j,t} = \frac{\eta p_{j,t}}{\frac{\mu B}{G \| w_t^{MC} - w_{j,t}^{MEC} \|^2}} \quad \forall t \in \mathfrak{F}, j \in \mathrm{M}. \tag{4}$$

where $P_{j,t}$ is the transmit power of j[th] mobile edge device and μ specifies additive white Gaussian noise. The data rate of the MEC system is

$$R_{j,t} = \frac{B}{G} log_2 \left( 1 + \frac{\rho_0 p_{j,t}}{\frac{\mu B}{G \| w_t^{MC} - w_{j,t}^{MEC} \|^2}} \right) \forall t \in \mathfrak{F}, j \in \mathrm{M}. \tag{5}$$

Similarly, the optimality of MEC is a process to attain the best outcomes when the j[th] mobile device offloads the duty to the edge MEC server. It can effectively located in a fixed coordinates and denoted as $w_t^{EC} = (x_{EC}, y_{EC}, 0)$ and the corresponding distance between j[th] mobile device and edge MEC server in time slot is represented as

$$d_{EC,t} = \| w_{j,t}^{M} - w_t^{EC} \| \tag{6}$$

The channel gain is defined as

$$h_{EC,t} = \frac{g}{\left[ d_{Ec,t} \right]^2} \tag{7}$$

G is denoted as the power gain and the Euclidean distance assumed as 5 meters. The data rate in the specified duration t is assumed as

$$R_{EC,t} = B_u log_2 \left( 1 + \frac{h_{EC,t} P_{j,t}}{\sigma^2} \right), \forall t \in \mathfrak{F}, j \in \mathrm{M} \tag{8}$$

$B_u$ is the total bandwidth and σ is the noise power.

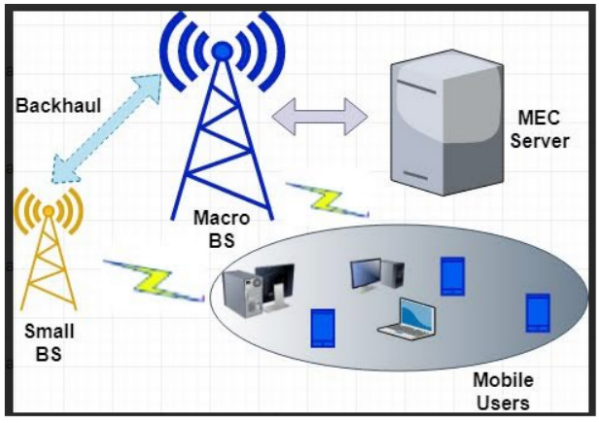


**Figure 1:** Articulation of B5G MEC system

The articulation of the proposed B5G MEC system is shown in figure 1, It comprised of heterogeneous network with small BS and Macro BS to the core network or MEC server. If the wireless backhaul is overloaded due to resource allocation, task offloading may suffer from high transmission delays. Task scheduling and computational offloading plays vital role in the backhaul communication.

### *2.1 Task scheduling model*

In this work, each mobile device has a computational task computed locally in the region of MEC server which deployed near the SBS in the time slot t. The computing decision action is assumed as $a_j^l = 1$ representing task is offloaded if it is $a_j^l = 0$ means the task is computed. Execution time and battery usage are used to differentiate between local and edge computing.

#### *2.1.1 Local computing*

The computational ability is discriminated by means of the frequency cycle of CPU and is denoted as $f_{h,K}$. The local task execution time is calculated using [5]

$$T_k^{exe} = \frac{L_{j,t}}{f_{h,K}} \tag{9}$$

where $L_{j,t}$ is the CPU cycle essential to complete a task of the edge device. At the same time the energy consumption for execution is given by

$$E_K^{local} = kL_{j,t} f_{kj,t}^2 \tag{10}$$

The switched capacitance of the edge device is denoted as K. we consider that $k = 10^{-28}$ [11].

The inclusion of local execution time and energy consumption results in the overall cost of task execution [5],

$$U_k^{local} = \alpha_1^l \frac{T^{local}}{\max T^{local}} + \beta_2^l \frac{E_k^{local}}{\max E_k^{local}} \tag{11}$$

$\alpha_1^l$ and $\beta_2^l$ are the weights to control over the computing phase.

### *2.2 Task offloading model*

Task is offloaded when the computing resources are running out of memory, The task are of two types such as delay-sensitive and energy-sensitive which are varying with sizes and computational requirements. so the generated tasks are continuously dropped. The formula for calculating transmission delay and energy consumption are as follows,

$$T_k^{MEC,tx} = \frac{s_{j,t}}{R_{j,t}} \tag{12}$$

$$T_k^{MEC,exe} = \frac{L_{j,t}}{f_{h,k}} \tag{13}$$

$$E_k^{MEC,tx} = P_{j,t} T_k^{MEC,tx} \tag{14}$$

$$E_k^{MEC,exe} = k_H L_{j,t} f_{h,k}^2 \tag{15}$$

The effective switched capacitance $k_H$ and is set to the value of $10^{-28}$ Farad. We consider a high speed processor with a clock frequency of f = 2.4 GHz, the cycle length is derived from the clock frequency $L_{j,t}$ = 1/f, which results approximately as 0.5 ns, using an effective switched capacitance value and clock cycle values, the energy consumption is calculated as 1 x $10^{-28}$ watts. Smartphones and Internet of Things end nodes are edge devices that must adhere to strict energy constraints. The effective switched capacitance should be chosen to guarantee practical viability in energy models for low-power processors. The theoretical extreme energy efficiency in computational modeling is reflected in this ultra-small power consumption estimate, especially in mobile edge computing scenarios with advanced nanotechnology concerns. For this reason, in accordance with CMOS standards, we have selected the switching capacitance value $10^{-28}$ Farad as low as feasible on MEC energy consumption, particularly with task offloading and computational efficiency in order to stay consistent with earlier benchmarks.

The computational delay of a task can be calculated using the sum of communication/transmission delay and the execution delay from MEC server to edge devices.

$$T_k^{MEC} = T_k^{MEC,tx} + T_k^{MEC,exe} \tag{16}$$

$$E_k^{MEC} = E_k^{MEC,tx} + E^{MEC,exe} \quad ( \tag{17}$$

The total cost is calculated as

$$U_k^{MEC} = \alpha_1^{MEC} \frac{T_k^{MEC}}{\max T_k^{MEC}} + \beta_2^{MEC} \frac{E_k^{MEC}}{\max E_k^{MEC}} \tag{18}$$

The total cost for edge execution is derived as

$$U_k^{MC} = \alpha_1^{MC} \frac{T_k^{MC}}{\max T_k^{MC}} + \beta_2^{MC} \frac{E_k^{MC}}{\max E_k^{MC}} \tag{19}$$

The computational effort is determined by weights in the areas of energy consumption and latency in the task transmission, edge computing, and result transmission phases.

The main objective is to formulate the sequential task function R and is denoted as

$$U_j = \sum_{k=1}^{B} U_{kj,i} = \sum_{i=0}^{l} a_j^1 a_j^2 U_{kj,i}^{MEC} + \\ + a_j^1 \left(1 - a_j^2\right) U_{kj,i}^{MC} + a_j^1 \left(1 - a_j^2\right) U_{kj,i}^{local} \tag{20}$$

The total size is represented as B in a set R. Furthermore the above problem is formulated as

$$min_A = \sum_j U_j \\ s.t\, a_j^1 a_j^2 T_{kj,i}^{MEC} + a_j^1 \left(1 - a_j^2\right) U_{kj,i}^{MC} + \\ + \left(1 - a_j^1\right) T^{loc,exe} \le T_{kj,i}^{max}, \forall k = 1, \ldots\ldots, B \tag{21}$$

A is the set of tasks to be completed within the time slot $T_k^{min}$. The optimal offloading action is needed to be a decision variable that indicates the decision to reduce the overall system cost. In order to determine the best choice within a time slot, network data such as job information and processing capacity are utilized. The traditional methods such as NP-hard, MINLP and non-convex optimization are not much effective due to the intelligence. That's why we consider the RL based Markov decision process making (MDP) learning to provide more efficient decision to schedule/offload a task.

## 3 RL based MDP framework

The traditional methods are not efficient in optimization due to the following reasons. 1. The task specific environments are dynamic in nature due to traffic, load, and delay characteristics. Traditional optimization techniques cannot handle the dynamic behavior of the MEC B5G network. 2. Due to the lengthy convergence of time and scalability problem intelligent decision making is required to offload. 3. Prior knowledge about the network environment is a challenging task for the traditional techniques. But RL based MDP technique follows the learning by using trial and error method. To address the above shortcomings, we propose the RL based MDP algorithm as a model-free methodology so as to make intelligent decisions and information exchange between agents (Mobile Edge device). To demonstrate the RL understanding of the suggested MEC system, following are the brief description,

#### *3.1.1 State Space $S_{j,t}$*

The set of input metrics of each agent for task offloading decision occupies as a state space $S_{j,t}$ = {*D, c, f and dt*}. The symbol set represents the size D of the network, c is the cycle with computational capability f and

energy-sensitive or delay sensitive is the type of task and can be chosen as $dt \in [0,1]$

*3.1.2 Action Space $a_{j,t}$*

Each mobile device can choose a particular action in a given time slot t. according to the local information from the MEC network. The action can be of binary offloading either to be executed or to be offloaded.

*3.1.3 Reward function $r_{j,t}$*

The proposed RL framework optimizes the computational capacity by means of selecting the cumulative reward function as the decision based upon the reward function as follows

$$r_{j,t} = -a_j^2 a_j^1 \frac{U_{kj,i}^{MEC}}{\max U_{kj,i}^{MEC}} - a_j^1 \left(1 - a_j^2\right) \frac{U_{kj,i}^{MC}}{\max U_{kj,i}^{MC}} - \\ - \left(1 - a_j^2\right) \frac{U_{kj,i}^{local}}{\max U_{kj,i}^{local}} \quad (22)$$

I t indicates that the negative reward is given for higher cost function and vice versa. Then the utility function of each agent is denoted as

$$R_{j,k} = \sum_{k=1}^{B} r_{j,k} \quad (23)$$

The reward utility function is formulated as

$$u_t^j = \begin{cases} p\, if\, r_{j,t} - r_{j,t-1} < 0 \\ q\, if r_{j,t} - r_{j,t-1} > 0 \\ 0 \qquad otherwise \end{cases} \quad (24)$$

Case 1: p represents the positive reward if the computational cost is low.

Case 2: q represents the negative reward if the computational cost is high.

We consider co-operative Q-learning for the information exchange between the agents. As number of tasks is sent to the edge server, the pressure on mobile devices is lessened, as evidenced by the MEC server execution steadily increasing. Meanwhile, mobile execution remains relatively low but stable, suggesting that certain jobs are still completed locally.

| RL based Task offloading Algorithm (RLTOA) | | |
|---|---|---|
| Initialize | : | Task Values for {D, c, f and dt} |
| Ensure | : | $dt \in [0,1]$ Episode counter b = 1 to Max |
| for | | episode =1 to max do<br>for j=1 to M do<br>for t=1 to T do |
| Choose action | : | Random action<br>Or based on ε-greedy policy Schedule Task or offload task based on the MEC server |
| Calculate and Return | : | Reward utility function based on equation (24) |
| Apply | | Trial and error until b > max |
| Return | | end if<br>end for<br>end for |

### *3.2 RL based task offloading algorithm*

The de-centralized multi-agent task computation offloading technique, which combines a MDP with Q-learning to create an ideal offloading decision as illustrated, is the subject of the proposal in this section. It is built on the discussion from the previous section.

In Figure 2, each agent will compute locally or on the MEC server whenever new tasks are created in each time slot. As per algorithm, researches the distributing policy offloading, and then decides on a course of action based on its knowledge of the surrounding area. It is then promptly rewarded for that action. The action probability and state function is updated every iterations to optimize the weights.

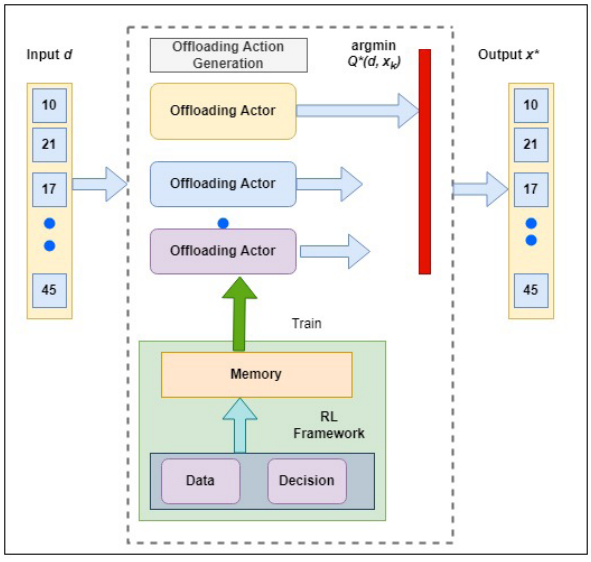


**Figure 2:** Articulation of RL based task offloading.

Because the edge servers and BSs in a cluster are limited in this scenario, we may cycle through every conceivable combination of BSs and edge servers to find the optimal task offload rate. algorithm for task offloading based on reconstruction from reinforcement learning. It seeks to create a single collection of data by combining the Action policy and offloading.

## *4 Results and discussion*

The experimental results of RL based task offloading algorithm is tested and the comparison of results with conventional study through MATLAB simulation environment.

MEC eanbled Hetnet is simulated to assess the effectiveness of our proposed offloading decision algorithm for MEC edge systems. We regard the mobile edge devices as being dispersed randomly and uniformly within a 500 m radius disc. Femtocells that enable multiple edge users (MUEs and FUEs) range in number from two to forty. Every time slot has exactly one active FUE and MUE. The following are the detailed tabulation of simulation parameters.

**Table 1:** Simulation Parameters

| Parameters | Value |
|---|---|
| Macro cell | 1 |
| No. of small cells | 15 |
| Bandwidth | 20 MHz |
| Edge Bandwidth | 1 MHz |
| Channel Power gain | 1.42 x 10-4 |
| Noise Power spectrum density | -174 dBm |
| CPU cycles | 0~1.75 GHz |
| Task size | 2-25 Mb |
| Computational capacity of MEC server | 20 GHz |
| Computational capacity of MC server | 15 GHz |
| Effective switched capacitance | $10^{-28}$ Farad |
| Learning Rate | 0.001 |
| Discount factor | 0.9 |
| Total episode (max) | 2000 |
| Weights $\alpha_1^l = \alpha_1^h = \alpha_1^e$ Weights $\beta_1^l = \beta_1^h = \beta_1^e$ | 0.5 |
| Total time steps per episode | 100 |
| Length of each slot | 1 sec |

The evaluation parameters are verified using MATLAB with a machine learning toolbox. RL enabled edge-computing setup is evaluated with average ratio of chosen modes to enable execution, drop and MEC server execution.

The cumulative reward is assessed for the convergence analysis. Due to this fact, average cumulative reward values are stored. The proposed problem is formulated with a delay restriction, and A penalty factor of 3 is added to the reward value if tasks exceed the deadline in order to manage the learning advancement.. The number of iterations was set to 500, 1000 and 2000 respectively to reduce the computational complexity. The proposed RLTOA show that when the iteration is reached to 500 times, the convergence stability is shown by using the loss function. The accuracy is validated with 96.34% , Figures 3 and 4 represent the mobile drop, MEC edge computing and local computing. That requires numerous interactions. Speciously,. The QoS parameters SNR, Battery energy, computational speed and energy efficiency (EE) are the key parameters for performance analysis. The results include the training phase and evaluation shows the training phase of the proposed RLTOA. The online learning system trains the agent to learn from the dynamic environment through trial and error. The delay-sensitive and intensive operation is checked with the MUEs and FUEs. The reward function designed to guarantee the QoS of UEs at the time slot. The RL optimization for the computational execution cost and average energy is shown in figures 3 and 4. To ensure that the task is completed, the MUE must meet a specific QoS standard that is consistently higher than a set threshold at all times.

Figure 3 and 4 depict the average ratio of execution and drop in a given time, There are different access possibilities for executing the total number of tasks in s given slot. The number of agents and their capacity to do the computing work determine the overall average cost. When compared to local, edge, and Q-learning networks, RLTOA is found to have a lower average cost. The suggested RLTOA controls the computational complexity as the number of agent's increases. As a result, the outcomes were better than the handling capacity when there were more agents. When compared to the three benchmarks, RLTOA eliminates the scalability problem. Overall, the pattern points to an adaptive execution strategy in which task offloading improves with time, resulting in fewer task drops and better use of available resources. Figures 5 and 6 represent the average execution cost and battery energy level of the edge user. The graphical illustration shows how effective the computing capacity interms of their execution cost and battery energy. The computation-intensive application from the ground edge level to the MEC server execution cost is reduced due to the shifting from local computing to edge node. The processing delays are significantly reduced thereby improving energy efficient task transmission.

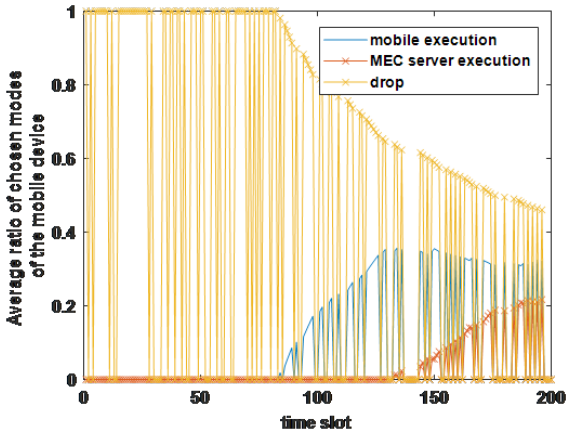


**Figure 3:** Average ratios of task execution strategies in mobile edge computing

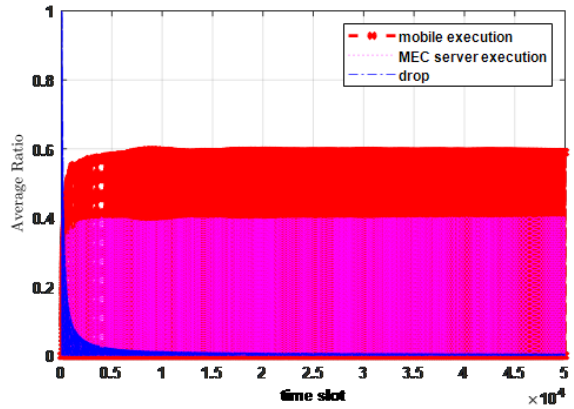


**Figure 4:** Average performance metrics of task execution strategies

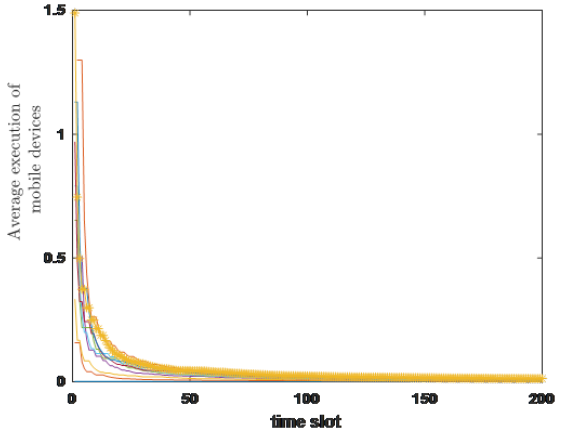


**Figure 5:** Temporal evolution of cumulative cost of MEC

The battery energy level based on the the latency is shown in Figure 7. Whenever the job size increases, so increases task execution delay, since they depends on the CPU cycles to complete the process. Computational speed depends on how large the task size and how the delay rises.

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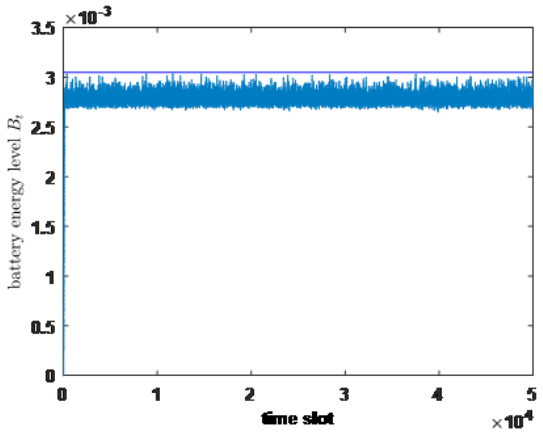


**Figure 6:** Battery energy consumption dynamics in MEC

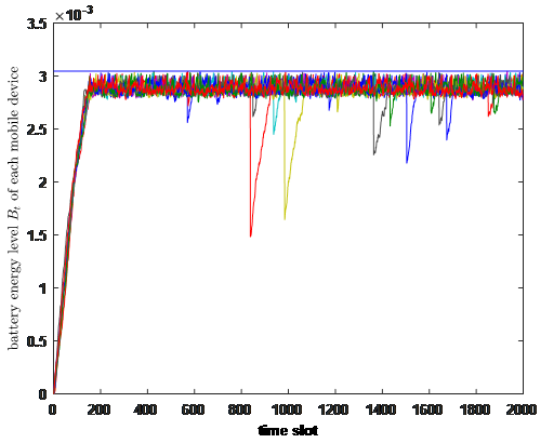


**Figure 7:** Dynamic resource allocation strategies across different execution modes

Tables 2 and 3 present the computational power and task size results for the RLTOA in terms of cost and delay performance. The speed of computing for edge users is influenced by the time it takes to execute tasks.

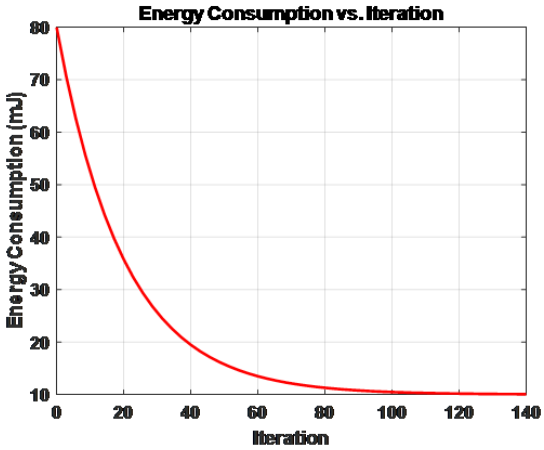


**Figure 8:** Energy consumption decay of RLTOA

The ability of processing capacity was 2.4 GHz, It is evidenced that the computing power increases when the computation time decreases. As a result agents are monitored as energy-intensive applications. The convergence of RLTOA is shown in figure 8 for the energy-intensive applications. The algorithm operates by learning optimal computational offloading strategies between mobile devices and edge servers through a deep reinforcement learning approach. The energy consumption decays over iterations.

Table 2 and 3 comparative analysis with existing system

**Table 2:** Total cost performance

| Contributers | Algorithm | Avg cost | Avg cost with computational capacity | Avg cost varying with offloading task size |
|---|---|---|---|---|
| [11] | Local | 40.25 | 70.55 | 26.50 |
| [18] | Edge | 35.20 | 68.95 | 20.20 |
| [22] | DQN | 24.35 | 63.50 | 17.50 |
| Proposed method | RL TOA | 20.2 | 55 | 12.5 |

**Table 3:** Energy consumption performance

| Contributers | Algorithm | Avg EC(Joules) | Avg EC with computational capacity | Avg EC varying with offloading task size |
|---|---|---|---|---|
| [11] | Local | 28.36 | 48.45 | 49.25 |
| [18] | Edge | 22.45 | 43.25 | 45.50 |
| [22] | DQN | 19.10 | 39.35 | 40.87 |
| Proposed method | RLTOA | 18.16 | 37.62 | 38.25 |

The suggested RL-based edge computing algorithm's effectiveness was demonstrated by the average total cost associated with computing power and energy consumption. . The numbers in the list are [18, 22, 23, 11]. The suggested RLTOA lowered the offloading expense and average execution cost by 52.13%, 43.5%, and 28.7% in computational cost, task size, and drop. Tables 2 and 3 thoroughly analyzed the impact of the suggested RLTOA when compared DQN, as well as local and edge computing. The results show how battery energy usage and job execution timing are affected by task size and processor power. RLTOA outperforms conventional techniques by 4% and 10%, respectively, during testing. Energy utilization is adequate since it has a major effect on overall expenses and task completion time. The hierarchical architecture for task execution is one of the parameters attributed to the RLTOA method. 2) A new reward function for task delegation in an RL framework. 3) By implementing RLTOA with reduced complexity and minimal processing delay, the overestimation problem is intended to be addressed.

## 5 Conclusion

The suggested RLTOA approach has been executed with successful outcomes in computation offloading. Offloading facilitation is carried out by the ground edge server, assisting edge users with demanding computations, ensuring the successful fulfillment of all offloading and execution responsibilities. Energy consumption and task execution latency are reduced by offloading the task. The RL framework assists in optimizing costs and computational power by calculating a weighted sum average. An agent achieves optimal results by undergoing intense training and selecting the most effective offloading strategy, while making decisions based on the new reward functions of the suggested RLTOA plan. Finally, the RLTOA convergence is evaluated using simulation. The performance analysis is compared with the DQN, Edge and local system performance.

## 6 Data availability statement

The raw data of this article will be made available from the authors upon request.

## 7 Conflict of interest

The authors declare no conflict of interest.

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# *Effect of the Nitrogen Environment On Indium Gallium Zinc Oxide Thin Film Transistors with Low Temperature Ultraviolet Annealing*

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**Abstract:** This study explores the influence of nitrogen gas flow rate on the electrical characteristics of indium-gallium-zinc-oxide (IGZO) thin-film transistors (TFTs) annealed under heat-assisted UV illumination. The aim is to understand how nitrogen flow rates impact the performance of solution-processed IGZO TFTs annealed at low temperatures, which is crucial for developing high-performance devices for next-generation electronics and temperature-sensitive applications. The IGZO TFTs were fabricated on glass substrates using a bottom-gate top-contact configuration, with the IGZO thin film deposited by inkjet printing and annealed in a chamber with varying nitrogen gas flow rates (0.5, 1, 2, and 5 L/min) at 250°C for 2 hours under UV illumination. The electrical characteristics were extracted from transfer characteristics measurements. The results show that a nitrogen flow rate of 1 L/min enhances the electrical properties of IGZO TFTs, likely due to a suitable concentration of oxygen vacancies. Excessive N2 flow rates (>1 L/min) negatively impact on the TFT characteristics, while lower flow rates (<1 L/min) result in more negative threshold voltages and lower on/off current ratios. The study concludes that optimizing the nitrogen gas flow rate is critical for achieving desired TFT properties, offering a valuable tool for fine-tuning IGZO TFTs to meet specific application requirements.

**Keywords:** MEC; IGZO TFTs; Low temperature; Nitrogen Annealing Effect; Oxide Semiconductor; Thin Film Transistor

# *Vpliv dušikovega okolja na tankoplastne tranzistorje iz indij-galij-cinkovega oksida z nizkotemperaturnim ultravijoličnim žarjenjem*

**Izvleček:** Študija raziskuje vpliv pretoka dušikovega plina na električne lastnosti tankoplastnih tranzistorjev (TFT) iz indij-galij-cink-oksida (IGZO), žarjenih pod toplotno podprto UV-osvetlitvijo. Cilj je razumeti, kako pretok dušika vpliva na delovanje IGZO TFT, obdelanih s tekočino in žarjenih pri nizkih temperaturah, kar je ključnega pomena za razvoj visoko zmogljivih naprav za elektroniko naslednje generacije in temperature občutljive aplikacije. IGZO TFT so bili izdelani na steklenih podlagah z uporabo konfiguracije spodnjih vrat in zgornjega kontakta, pri čemer je bil IGZO tanek film nanesen s tiskanjem z inkjet tiskalnikom in žarjen v komori z različnimi pretoki dušika (0,5, 1, 2 in 5 l/min) pri 250 °C 2 uri pod UV-osvetlitvijo. Električne lastnosti so bile izmerjene iz meritev prenosnih lastnosti. Rezultati kažejo, da pretok dušika 1 l/min izboljša električne lastnosti IGZO TFT, verjetno zaradi ustrezne koncentracije kisikovih praznin. Prekomerni pretoki N2 (>1 l/min) negativno vplivajo na lastnosti TFT, medtem ko nižji pretoki (<1 l/min) povzročajo bolj negativne pragovne napetosti in nižja razmerja med vklopnim in izklopnim tokom. Študija zaključuje, da je optimizacija pretoka dušika ključna za doseganje želenih lastnosti TFT, kar ponuja dragoceno orodje za natančno nastavitev IGZO TFT, da izpolnjujejo specifične zahteve aplikacij.

**Ključne besede:** IGZO TFTs; nizka temperatura; učinek dušikovega žarjenja; oksidni polprevodnik; tankoplastni tranzistor

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## 1 Introduction

In recent years, solution processed IGZO TFTs have emerged as potential technology for a wide range of applications, including displays, sensors, and wearable devices, due to their elevated mobility, elevated transparency, and small power consumption characteristics [1]–[5]. The performance of IGZO TFTs is significantly influenced by the fabrication process, particularly the annealing process, which is vital for enhancing the electrical transport properties and stability of the transistors. Traditionally, thermal annealing has been generally applied in the fabrication of IGZO TFTs to enhance the thin film quality and carrier mobility. Heat annealing typically involves annealing the IGZO thin films at elevated temperatures classically above 300°C for an extended period [6]. During heat annealing, the high temperature can help to remove the defects and impurities in the thin film, decreased oxygen vacancies, resulting in improved carrier mobility of the IGZO TFTs [7]. However, there are several disadvantages associated with heat annealing. Firstly, the high temperature may cause thermal damage to the substrate, leading to substrate warping or degradation of other components in the device structure. Secondly, temperature control during the annealing process can be challenging, as it requires precise control to avoid over-annealing or under-annealing, which can affect the uniformity and reproducibility of the TFT performance[8]. Lastly, the long annealing times required for heat annealing may not be conducive to high throughput manufacturing processes, resulting in reduced productivity and increased fabrication costs) [9], [10].

To overcome the limitations of traditional heat annealing, UV annealing has been studied as an alternative approach for the construction of IGZO TFTs. UV annealing has several advantages, including shorter annealing times, reduced substrate damage, and improved uniformity of the TFT performance [9], [11]–[14]. UV annealing has also been reported to decrease the defects and enhance the electrical properties of IGZO TFTs [15]. Additionally, UV annealing has been found to be compatible with low-temperature substrates, making it suitable for flexible electronics and other temperature-sensitive applications[16]. However, this annealing method alone may not be sufficient to fully optimize the performance of IGZO TFTs, as it may not effectively remove all the defects and impurities in the thin film, resulting in suboptimal electrical characteristics [17]–[19].

A combination of heat and UV annealing has been studied as a new method for the fabrication of IGZO TFTs, aiming to synergistically leverage the benefits of both approaches and overcome their constraints [3], [20]. For example, Zhang et al. demonstrated that the combination of heat and UV annealing led to a meaningful improvement in the carrier mobility of IGZO TFTs compared to heat annealing or UV annealing alone [21]. They attributed enhanced performance to the synergistic effects of heat and UV annealing, which led to improved crystallinity and reduced defect density in the IGZO films.

Among the backdrop of exploring various annealing techniques to enhance IGZO TFT performance, including the novel approach of combining heat and UV annealing, there is a mounting interest in the role of annealing environments, particularly the use of high-pressure gases[22]. Research has shown that high-pressure annealing with gases like nitrogen[23]and hydrogen [24] can significantly enhance the electrical characteristics of IGZO based TFTs by promoting carrier mobility and reducing oxygen vacancies [24]– [27].

This investigation focuses on describing the role of N2 flow rate at low pressure during heat-assisted UV annealing process, indicating the electrical attributes of IGZO TFTs. By precisely altering the N2 flow rates, we have observed consequential shifts in the transistors electrical behavior which pinpoint the profound impact of annealing environment on defect dynamics within the IGZO films. Our results demonstrate that a carefully calibrated nitrogen environment at low pressure is key to modulating defect-related phenomena, thereby refining the electrical performance of IGZO TFTs. This work not only advances the methodologies for defect control in low-temperature at low pressure, solution- processed semiconductors but also enriches the fundamental understanding of defect behavior under low pressure annealing environment, aligning with the ongoing discourse on defect engineering in semiconductor technology.

## 2 Materials and methods

IGZO TFTs were fabricated on glass substrates utilizing a bottom-gate top-contact (BGTC) configuration as presented in Fig.1. The TFT channel length and the width were 10 µm and 150 µm, respectively. The gate electrode was made of platinum Pt, and the gate dielectric consisted of a SiO2/Si3N4 layer. A 2.5M IGZO solution was prepared using nitrate salts of In:Ga:Zn in a ratio of 6.8:1:2.2, dissolved in a blend of 2-Methoxyethanol, Propanediol, and Glycerol in a ratio of 7:2:1. The IGZO solution was deposited onto the substrate using an inkjet printing method with a drop spacing of 60 µm and 3 drops. The deposited IGZO thin film was then annealed inside a chamber with a nitrogen gas flow. The annealing was performed using a hot plate set at 250°C

and a UV lamp with a power density of 33 mW/cm2 and a wavelength of 184 nm, respectively. Four different N2 gas flow rates: 0.5 L/min, 1 L/min, 2 L/min, and 5 L/min were used at the same annealing temperature, with each condition being annealed for a duration of 2 hours. The annealing process is illustrated in Fig. 2. Aluminum was deposited onto the IGZO thin film by physical vapor deposition to create the source/drain electrodes. The transfer characteristics of the fabricated devices were recorded by utilizing a semiconductor parameter analyzer. The electrical characteristics of the TFTs, Subthreshold swing, on/off current ratio, threshold voltage, and off current were extracted from the transfer characteristics measurements.

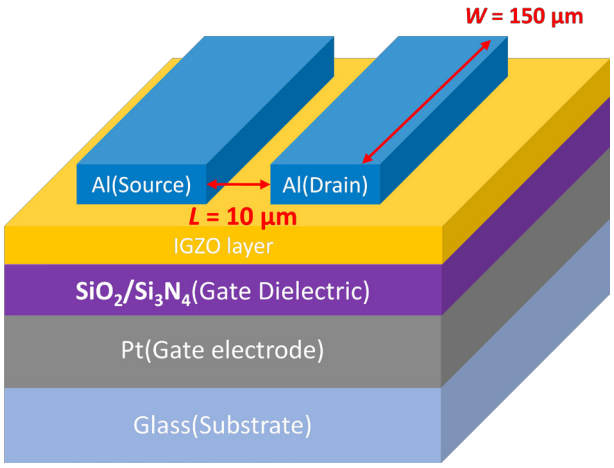


**Figure 1:** Cross-sectional representation of a bottom-gate IGZO TFT with a SiNx/SiO2 gate dielectric layer, constructed on a glass substrate.

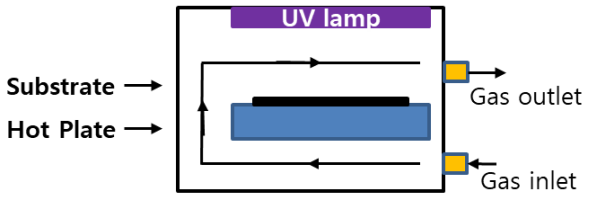


**Figure 2:** Annealing chamber with UV lamp and hot plate.

## 3 Results and discussions

Figure 3 illustrates the transfer characteristics of the TFTs annealed at 250°C for 2h with varying nitrogen flow rates. Specifically, Figs.3(a), Figs.3(b), Figs.3(c) and Figs.3(d) display transfer curves for flow rates of 0.5, 1, 2, and 5 L/min, respectively. The on-current slightly increases as the gas flow rate changes from 0.5 L/min to 1 L/min, which reveals an improvement in the electrical behavior of the device. This could be ascribed to the moderate presence of oxygen vacancies from the IGZO film surface due to the exposure to UV and heat under the following nitrogen, which enhances the carrier concentration. 1 L/min to 2 L/min, the on-current slightly decreases, Furthermore, as the N2 flow rate increases to 5 L/min the on-current decreases dramatically.

The electrical characteristics of the devices based on the N2 gas flow are summarized in Table I. The $V_{TH}$ was determined by extrapolating the ID square root against the $V_G$ curve in the saturation region. The threshold voltage of the devices varies between –8.3 V and –12.5 V as the N2 flow changed from 0.5 L/min to 5 L/min.

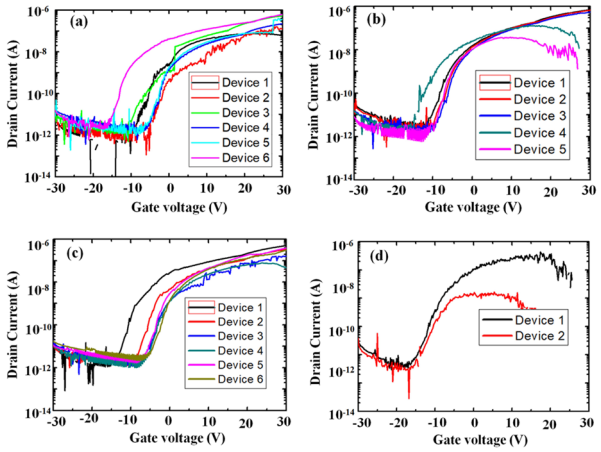


**Figure 3:** The transfer characteristics of TFTs annealed at varied Nitrogen gas flow rate a) 0.5 L/min, b) 1 L/min, c) 2 L/min and d) 5 L/min

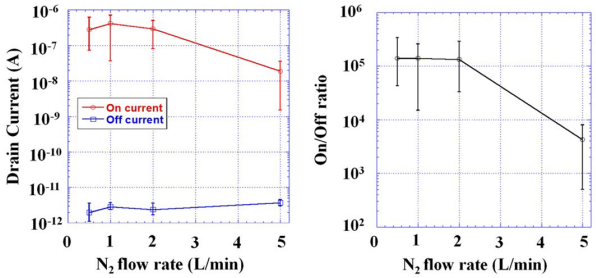


**Figure 4:** a) On-current(red) and off-current (blue) b) On/Off current ratio.

For a broader perspective, Table 1 also includes data for IGZO TFTs annealed in a stable nitrogen environment (0.0 L/min), as reported by Huang et al. [28] Under these conditions, the device exhibited a threshold voltage of -14.77 V, an on/off current ratio of $2.22\times10^4$, and a subthreshold swing of 7.37 V/dec. These values are significantly inferior to those achieved in this work at an optimized flow rate of 1 L/min, which yielded a less negative threshold voltage (–2.6 V), a much higher on/off ratio ($5.13\times10^5$), and a lower subthreshold swing (1.84 V/dec). This comparison demonstrates that a

**Table 1:** Summary of transistor characteristics corresponding to the N2 flow rate.

| $N_2$ flow rate(L/min) | Vth(V) | $I_{off}$(A) | I(On)/I(off) | Subthreshold. Swing (V/dec) | References |
|---|---|---|---|---|---|
| 0.0 (stable N2) | -14.77 | N/A | $2.22 \times 10^{4}$ | 7.37 | [28] |
| 0.5 | -8.3 | $1.16 \times 10^{-12}$ | $5.90 \times 10^{4}$ | 1.87 | This work |
| 1 | -2.6 | $1.25 \times 10^{-12}$ | $5.13 \times 10^{5}$ | 1.84 | |
| 2 | -4.8 | $2.71 \times 10^{-12}$ | $1.21 \times 10^{5}$ | 2.17 | |
| 5 | -12.5 | $2.17 \times 10^{-6}$ | $9.80 \times 10^{2}$ | 5.31 | |

static nitrogen environment (no flow) results in poorer device performance compared to controlled nitrogen flow during annealing.

A negative $V_{TH}$ indicates more electron carriers making the transistor operate in depletion mode. The increase in the negative direction of $V_{TH}$ at higher flow rate is ascribed to an increase of deficiencies, specifically oxygen vacancies. However, as the nitrogen flow rate increases from 1 L/min, the primary source of free electrons in oxide semiconductors based on Zinc Oxide (ZnO) is largely associated with the creation of oxygen vacancies[29]–[31] whereas the current ratio slightly increases and significantly decreases as the gas flower changes from 2 to 5 L/min. Furthermore, the increase in the gas flow rate results in higher off current. Consequently, it is anticipated that annealing at an elevated N2 flow rate improves the creation of oxygen vacancy defects[32]. Thus, an elevated N2 flow rate results in more electron carriers which leads to negative $V_{TH}$ shifts with higher off current as nitrogen flow rate increases. The occurrence of oxygen deficiencies similarly negatively impacts the subthreshold swing (S.S.) value resulting in higher S. S [33]. On the other hand, lowering the nitrogen flow rate leads to lower off-current level and lower threshold voltage value, and lower subthreshold swing. While a very low nitrogen flow level gives a more negative $V_{TH}$ and lower ratio of on/off current. This indicates that annealing in nitrogen environment is beneficial to regulate the electrical properties of the TFTs based on IGZO simply by altering the nitrogen quantity.

## 4 Conclusions

We have demonstrated the effects of annealing process in flowing N2 ambient on IGZO TFTs with low Temperature Ultraviolet Annealing. Our research shows that nitrogen gas flow rate is a critical parameter influencing the electrical characteristics of IGZO based TFTs. Improving electrical properties, a reasonable flow rate of 1 L/min suggests the creation of suitable oxygen vacancies in the IGZO film. In contrast, elevated flow rates lead to an increased carrier concentration, which results in a higher off current, implying the formation of detrimental defects. This study highlights the delicate optimization required in nitrogen-assisted annealing processes for refining the performance of IGZO TFTs. The findings offer a pathway for enhancing low-temperature solution-processed semiconductors, a step forward in semiconductor defect engineering. Further investigations are warranted to deepen the understanding of nitrogen's role in adjusting the defect landscape of IGZO thin films.

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## 6 Conflict of interest

The authors affirm that they have no known financial conflicts of interest or personal connections that could have potentially influenced the research presented in this paper.

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