ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 53, No. 3(2023), September 2023

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 53, številka 3(2023), September 2023

UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *3-2023*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 53, NO. 3(187), LJUBLJANA, SEPTEMBER 2023 | LETNIK 53, NO. 3(187), LJUBLJANA, SEPTEMBER 2023

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.
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Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 53, No. 3(2023)

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Original scientific paper
https://doi.org/10.33180/InfMIDEM2023.301

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 53, No. 3(2023), 121 – 135

Existence of Capacitive Effects in a Tungsten-based SDC Memristive System

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Abstract: Following the discovery of a thin-film memristive system behaving as a memristor in 2008, memcapacitor and memcapacitive systems have also been described and become hot research areas. Tungsten-based SDC (Self-Directed Channel) memristors are already in the market and have already been used in circuit applications. They are modeled with the mean metastable switch memristor model in the literature. A memristor must have the three fingerprints described by Chua et al. In this paper, it is shown that the behavior of the Tungsten-based memristors is more complex than a memristive system and they do not always meet the three fingerprints of the memristor. It has been experimentally found that the capacitive effects are dominant at low frequencies when it is excited with a square wave voltage source when the Tungsten-based memristor is connected in series with a capacitor. It is important to model the new circuit element memristor accurately. "The Tungsten-based memristors" cannot be modeled just as a memristive system and only with the mean metastable switch memristor model. It is suggested that, perhaps, it can be modeled considering memcapacitive effects.

Keywords: memristor, memristive systems, zero-crossing hysteresis curve, memcapacitive effects, memcapacitor

Obstoj kapacitivnih učinkov v memristivnem sistemu SDC na osnovi volframa

Izvleček: Potem ko je bil leta 2008 odkrit memristivni sistem s tanko plastjo, ki se obnaša kot memristor, so bili opisani tudi kondenzatorji in memkapacitivni sistemi. Memristorji SDC (Self-Directed Channel) na osnovi volframa se že uporabljajo v komercialnih vezjih. V literaturi so modelirani z modelom srednjega metastabilnega stikala memristorja. Memristor mora imeti tri prstne odtise, ki so jih opisali Chua et al. V članku je prikazano, da je obnašanje memristorjev na osnovi volframa bolj zapleteno kot memristivni sistem in ne izpolnjujejo vedno treh prstnih odtisov memristorja. Eksperimentalno je bilo ugotovljeno, da pri nizkih frekvencah prevladujejo kapacitivni učinki, ko je memristor na osnovi volframa vzbujen z napetostnim virom s kvadratnim valovanjem in je zaporedno povezan s kondenzatorjem. Pomembno je, da se novi element vezja memristor natančno modelira. „Memristorjev na osnovi volframa" ni mogoče modelirati samo kot memristivni sistem in samo z modelom srednjega metastabilnega stikala memristorja. Predlagano je, da ga je morda mogoče modelirati ob upoštevanju memkapacitivnih učinkov.

Ključne besede: memristor, memristivni sistemi, krivulja histereze z ničelnim prehodom, memkapacitivni učinki, mem-kondenzator

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1 Introduction

Memristor was claimed as a missing nonlinear fundamental circuit element in 1971 [1]. In 1976, it was shown that there were systems with similar properties to memristors and they are called memristive systems [2]. A thin-film TiO_2 memristive system was shown to behave as a memristor in 2008 [3]. Memristor is a highly nonlinear circuit element, and its electromagnetic theory is elusive unlike other circuit elements [4]. It has emerged as a popular nonlinear circuit element in the last two decades [5]. The memristive effects are quite common in nano dimensions [6, 7]. Some memristor research has focused on finding new materials behaving as memristors [6, 7]. Resistive RAMs are also

How to cite:
C. Dalmış et al., "Existence of Capacitive Effects in a Tungsten-based SDC Memristive System", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 53, No. 3(2023), pp. 121–135

regarded as memristors [8]. Memristors may cause new analog and digital circuit applications to be found [5, 9]. Programmable circuit applications of the memristor are also promising [10, 11]. An ideal memristor has not been found yet [12]. Nowadays, memristive systems are also called memristors [12]. An ideal memristor must have a zero-crossing hysteresis curve [2]. The three fingerprints of memristors are commonly used to identify them [13]. Some memristor research focused on modeling nonlinear dopant drift memristors with window functions [14-20]. Such memristor models possess the three fingerprints of memristors.

A memcapacitor is a flux-dependent capacitor and a memcapacitive system is a system with similar properties to memcapacitors [6, 21]. An ideal memcapacitor or a memcapacitive system is also a nonlinear circuit element [21]. An ideal memcapacitor's charge-voltage characteristic or hysteresis loop is also frequency-dependent [21, 22]. The memcapacitive effects are also common in the literature [6, 23, 24]. The capacitance of some memcapacitive systems may be negative [25]. Memcapacitive effects can also be found in nanopores [26]. Solid-state memcapacitors can be used to make circuits that cannot be made with LTI capacitors [27]. Memcapacitive effects are shown to exist in an HP TiO_2 memristor [28]. An Au/Ti–HfO2-InP/InGaAs diode needs both memristive and memcapacitive effects to be modeled correctly [29]. A memcapacitor device showing chaotic behavior is described in [30]. Memcapacitors can be used in oscillator circuits [31-32]. There are already memcapacitor-based chaotic oscillators made in the literature [33-35]. In opposite to memristors, memcapacitors store energy and their charging efficiency can be polarity-dependent [36]. Memcapacitors can also be used for computing [37].

The market has already seen the emergence of Carbon- and Tungsten-based memristors [38]. They are also reported to have zero-crossing hysteresis curves [38] and have already been used in chaotic circuits and for educational purposes [39-40]. They are suggested for use in a machine-learning circuit [41]. The usage of Knowm memristors in threshold logic circuits is examined in [42]. These memristors are suggested to be used with a series protection resistor [38]. According to [1], the equivalent circuit of a memristor connected in series with a resistor is also a memristor. That's why a Knowm memristor with a protection resistor is also a memristor. The Mean Metastable Switch Memristor Model (MMSMM) is presented for Tungsten-based Knowm memristors in [43]. In [44], the model is modified to include chaotic dynamics. The model in [43-44] gives a zero-crossing hysteresis curve. The models in [43-44] should be able to predict the waveforms of the circuits in which the Tungsten-based memristors are used.

A memristor-capacitor circuit can be found in a programmable filter [11]. A memristor-capacitor discharge circuit is examined in [14]. HP memristor-capacitor series circuit under DC excitation is examined analytically in [45]. In [46], it is shown that the Lambert W function can be used to analyze the charging and discharging of memristor-capacitor circuits. An analytical and experimental examination of a parallel memristor-capacitor circuit is made using the memristor's flux-charge characteristic [47]. To the best of our knowledge, the charging and discharging of the Tungsten-based memristor-capacitor circuit have not been examined experimentally. In this paper, we report the experimental results that were observed while examining a Tungsten-based memristor-capacitor-protection resistor (M-C-R_s) series circuit excited with a square wave signal, it has been found that the Tungsten-based memristors exhibit a non-zero crossing hysteresis curve, it is interesting that the same memristor has a zero-crossing hysteresis curve when excited with a sinusoidal wave or even a square wave, and this means that hysteresis behavior of a Tungsten-based memristor may not have zero-crossing hysteresis curve depending on its usage with other circuits. The implications of the experimental results are also discussed. This study is important because there is no other study in the literature examining the effect of the polarity of the memristor on the charging of the capacitor in an M-C-R_s circuit experimentally.

The paper is arranged as follows. The memristive and memcapacitive systems are briefly introduced in the second section. Information on a Tungsten-based Self-Directed Channel Memristor is given in the third section. Experimental results are given in the fourth section. The experimental results are discussed in the fifth section. The last section concludes the paper.

2 Memristive and memcapacitive systems

In this section, the memristive and memcapacitive systems are briefly explained.

2.1 Memristor and memristive systems

Memristive systems can be classified as either current-controlled or voltage-controlled. In [21], Ventra et al. have described an n^{th} degree voltage-controlled memristive system as

$$i(t) = G\left(x(t), v(t), t\right).v(t) \tag{1}$$

$$\frac{dx}{dt} = f\left(x(t), v(t), \mathrm{t}\right) \tag{2}$$

where $v(t)$, $i(t)$, and $G(x(t), v(t), t)$ are the voltage, the current, and the electrical conductance or the memductance of the memristive system, respectively, and $x(t)$ is the set of n state variables describing the internal state of the memristive system, that may be dependent on $v(t)$ and $x(t)$.

If ($x(t)$ is the flux of the system and its memductance is only dependent on it, the system describes an ideal memristor [2, 21]. The memristor symbol, which is defined in [1] and shown in Figure 1.a, is nowadays used for both memristors and memristive systems.

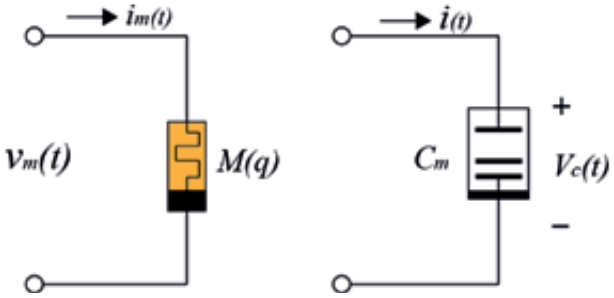


Figure 1: a) Memristor and b) Memcapacitor symbols.

For a memristor, the memductance must be always positive:

$$0 < G\left(x\left(t\right), \mathrm{v}\left(\mathrm{t}\right), t\right) < \infty \tag{3}$$

A memristor cannot store energy and it is a power-dissipating circuit element [1]. Memristive systems also dissipate power and do not store energy.

$$p\left(t\right) = v\left(t\right) i\left(t\right) \geq 0 \tag{4}$$

Under AC excitation, a memristor or a memristive system must have a zero-crossing hysteresis loop that has been first described in [2]. In [13], the claim has been made that all memristors or memristive systems must have the three fingerprints. They are given as:

- A memristor's current and voltage must be both zero at the same time or it must have a zero-crossing hysteresis loop under AC excitation.
- The hysteresis loop must be frequency-dependent, i.e., its shape varies with frequency. Its area decreases when frequency increases.
- The hysteresis loop converges to a single value function when the frequency becomes very high.

2.2 Memcapacitive systems

Some nonlinear capacitors obey the memcapacitive system definition [21]. Ventra et al. have described a voltage-controlled memcapacitive system as

$$q\left(t\right) = C\left(x, v_c, t\right) v_c\left(t\right) \tag{5}$$

$$\frac{dx}{dt} = f\left(x\left(t\right), \mathrm{v}\left(\mathrm{t}\right), \mathrm{t}\right) \tag{6}$$

where $q(t)$, $v_c(t)$, and $C(x, v_c, t)$ are the charge, the voltage, and the nonlinear capacitance (memcapacitance) of the memcapacitive system, respectively, and $x(t)$ is the set of n state variables describing the internal state of the memcapacitive system, that may be dependent on $v_c(t)$ and $x(t)$.

If $x(t)$ is the flux of a memcapacitive system and equal to the integral of its voltage with respect to time, the system describes an ideal memcapacitor, i.e., a memcapacitor is a special case of a memcapacitive system [21]. The memcapacitor symbol, which is defined in [21] and shown in Figure 1.b, is nowadays used for both memcapacitors and memcapacitive systems.

If there is only one state variable, the current of a memcapacitive system can be calculated as

$$i_c\left(t\right) = \frac{dq_c\left(t\right)}{\mathrm{dt}} = \frac{d\left(C\left(x\left(t\right), v_c\left(t\right), t\right) v_c\left(t\right)\right)}{\mathrm{dt}} = \frac{d\left(C\left(x\left(t\right), v_c\left(t\right), t\right)\right)}{\mathrm{dx}} \frac{dx}{\mathrm{dt}} v_c\left(t\right) + C\left(x\left(t\right), v_c\left(t\right), t\right) \frac{dv_c\left(t\right)}{\mathrm{dt}} \tag{7}$$

$$i_c\left(t\right) = \frac{d\left(C\left(x, v_c\left(t\right), t\right)\right)}{\mathrm{dx}} f\left(x\left(t\right), v\left(t\right), t\right) v_c\left(t\right) + C\left(x, v_c\left(t\right), t\right) \frac{dv_c\left(t\right)}{\mathrm{dt}} \tag{8}$$

2.3 Mean metastable switch memristor model

The Tungsten-based Knowm memristor symbol and the equivalent circuit of the MMSMM model are shown in Figure 2. A Tungsten-based Knowm memristor is modeled as a Schottky diode connected in parallel with a memristor or a memristive system, and Φ is a parameter that determines the contributions of these parallel connected circuit elements. The mean metastable switch memristor model (MMSMM) of a Tungsten-based Knowm memristor [43] is given as

$$i\left(t\right) = \left(\frac{\phi x}{R_{ON}} + \frac{\phi\left(1-x\right)}{R_{OFF}}\right) v\left(t\right) + \left(1-\Phi\right) \alpha \left(e^{\beta_1 v(t)} - e^{-\beta_2 v(t)}\right) \tag{9}$$

$$\frac{dx}{dt} = \frac{1}{\tau}\left(\frac{1}{1+e^{-\beta\left(v-V_{ON}\right)}}\left(1-x\right) - \left(1-\frac{1}{1+e^{-\beta\left(v+V_{OFF}\right)}}\right)x\right) \tag{10}$$

Where $v(t)$ and $i(t)$ are the voltage and current of the Tungsten-based memristor, $x(t)$ is the state variable of the Tungsten-based memristor, R_{ON} and R_{OFF} are the minimum and maximum memristance of the memristive memory element shown in Figure 2, α, β_1, and β_2 are Schottky parameters, τ is a time constant that defines the rate of change of the state variable, V_{ON} is the positive threshold voltage, V_{OFF} is the negative threshold voltage, β is a temperature dependent parameter, reciprocal to thermal voltage, V_T, and equal to

$$\beta = \frac{1}{V_T} = \frac{e}{kT} \tag{11}$$

Where k is the Boltzmann constant, e is the electron charge, and T is the absolute temperature.

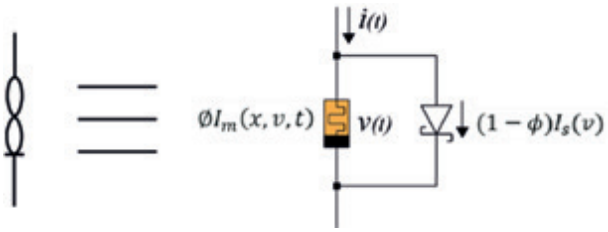


Figure 2: The equivalent circuit of a Tungsten-based Knowm memristor [43].

The state variable $x(t)$ ranges from 0 to 1. Tungsten-based memristor current considering the equivalent circuit shown in Figure 2 is given as

$$i(t) = \Phi I_m(x,v,t) + (1-\phi) I_s(v) \tag{12}$$

Where $I_m(x, v, t)$ is the current of an ideal memristor and $I_s(v)$ is the current of an ideal Schottky diode.

Φ is a positive parameter between zero and one. If Φ=1, the Schottky diode current is zero, and the equivalent circuit in Figure 2 turns into an ideal memristor. If Φ=0, the equivalent circuit in Figure 2 turns into a Schottky diode.

In [44], the threshold of the memristor is given as

$$V_{ON} = \frac{0{,}1\cos\left(\left(4\pi\sqrt{x}\right)/\left(1{,}7-x\right)\right)}{1+10\sqrt{x}} + 0.14 \tag{13}$$

The chaotic memristor model given in [44] was not used in this study since the memristor was not examined at above the threshold voltages.

Considering Eq.s (9) and (10) and the three fingerprints of a memristor, the current and voltage of a Tungsten-based memristor must become zero at the same time since the MMSMM model also obeys memristive system equations.

3 Tungsten-based self-directed channel (SDC) memristor

The Self-Directed Channel (SDC) Tungsten-based Knowm memristor structure is shown in Figure 3.a. The integrated circuit shown in Figure 3.b, which has 8 Tungsten-based Knowm memristors in a 16 pin ceramic DIP package, is used in this study. More information about Knowm memristors can be found in [38]. The pin connections of the memristors are given in Figure 3.c. Knowm memristors require using a series protection resistor to limit its current [38]. One of the Knowm memristors is placed in series with a protection resistor and excited with a sinusoidal signal as shown in Figure 4. A series resistor and a memristor also behave as a memristor as explained in [1]. The series resistor is used to measure the memristor current since its voltage and current are proportional. All of the operational Tungsten-based memristors are used in the experiments but only the results of one of them are given due to space considerations. Its current and voltage waveforms and its zero-crossing pinched hysteresis curves acquired for three different frequencies and are shown in Figures 5 and 6, respectively. It can be seen that with increasing frequency, the area of the hysteresis loop gets smaller in size which is a fingerprint of memristive systems [13]. The Tungsten-based Knowm memristor is also excited with a square wave and its current and voltage waveforms and hysteresis curves are shown in Figures 7 and 8, respectively.

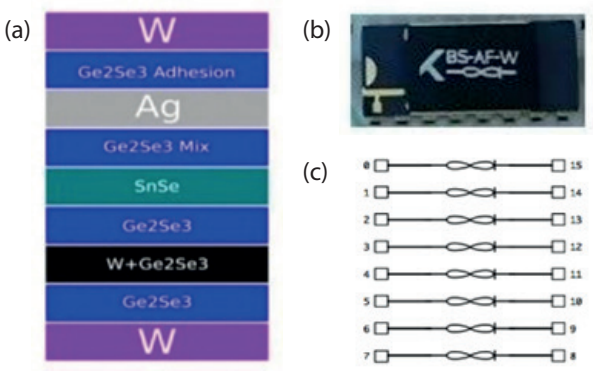


Figure 3: a) The Tungsten-based Knowm Memristor Topology [38], b) The SDC Tungsten(W)-based Knowm Memristor Integrated Circuit, and c) its pin connections [38].

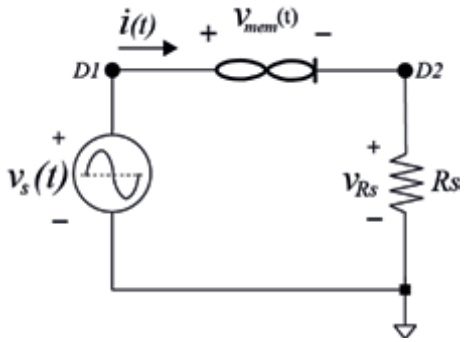
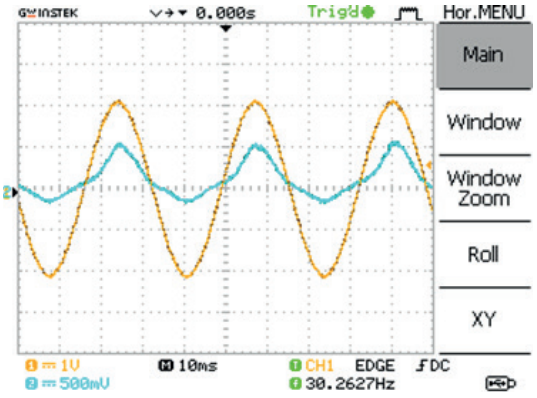


Figure 4: The Tungsten-based Knowm memristor excited with a signal source.

(a)



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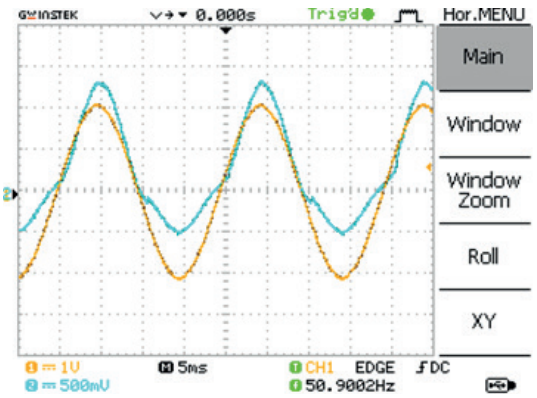

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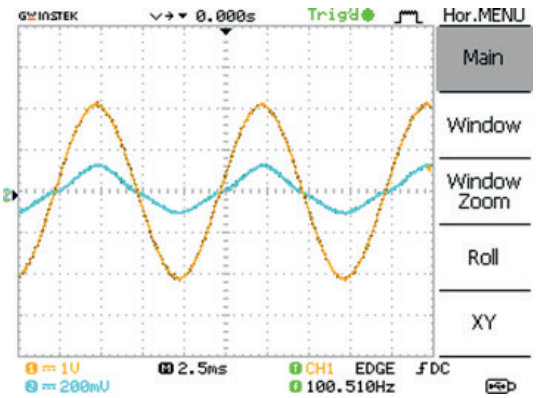
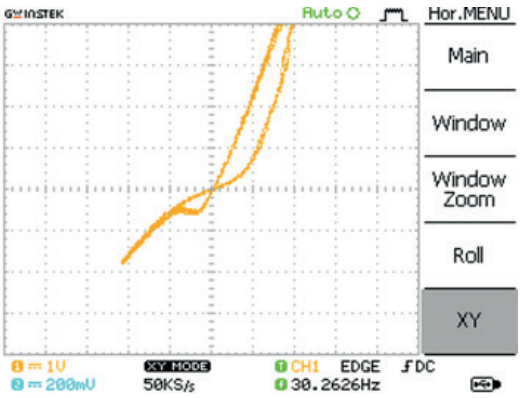


Figure 5: The time-dependent current and voltage waveforms of the Tungsten-based memristor fed with a a) 30, b) 50 Hz, and c) 100 Hz and a 2 V peak-to-peak sinusoidal voltage.

(a)



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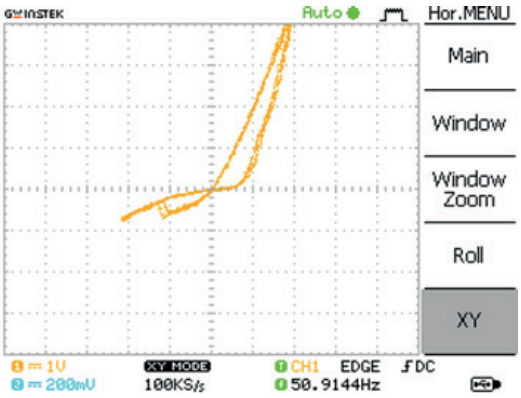

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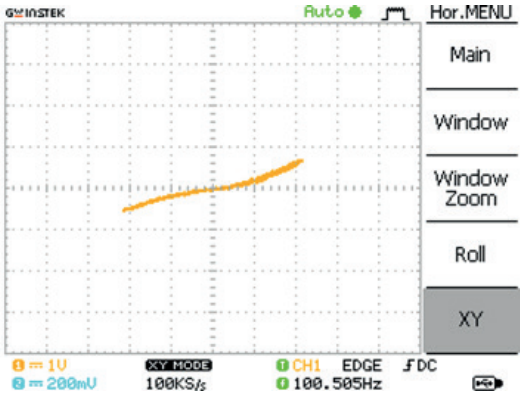


Figure 6: The hysteresis curve of the Tungsten-based memristor fed with a a) 30, b) 50 Hz, and c) 100 Hz and a 2 V peak-to-peak sinusoidal voltage.

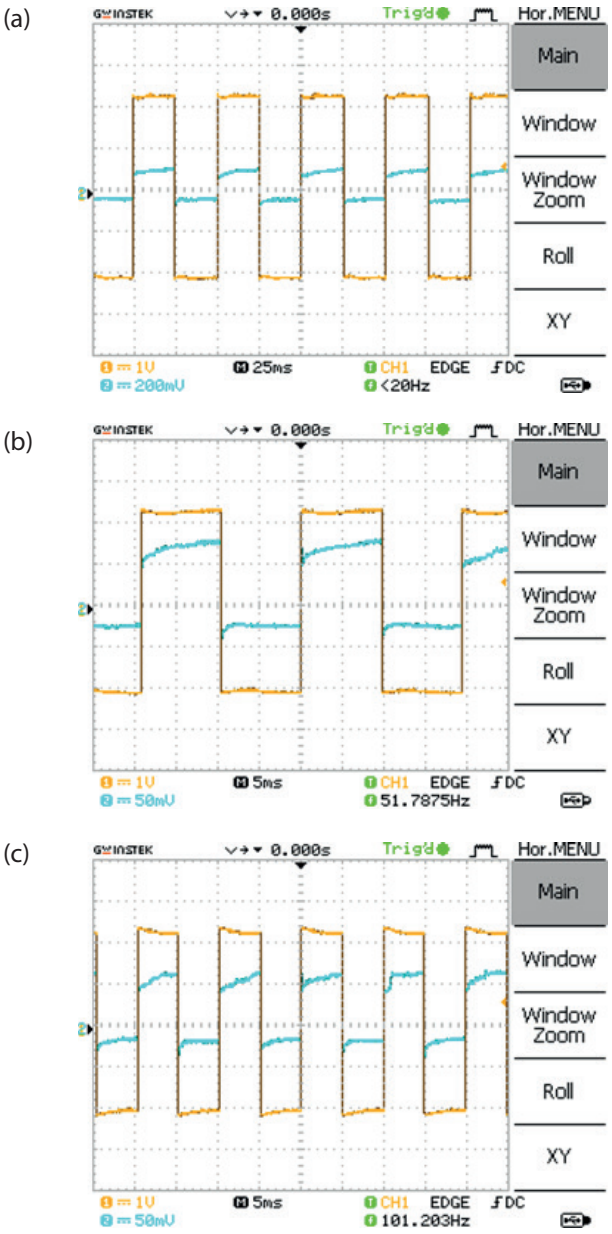


Figure 7: The time-dependent current and voltage waveforms of the Tungsten-based memristor fed with a a) 20 Hz, b) 50 Hz, c) 100 Hz and an approximately 2.4 V peak-to-peak square voltage.

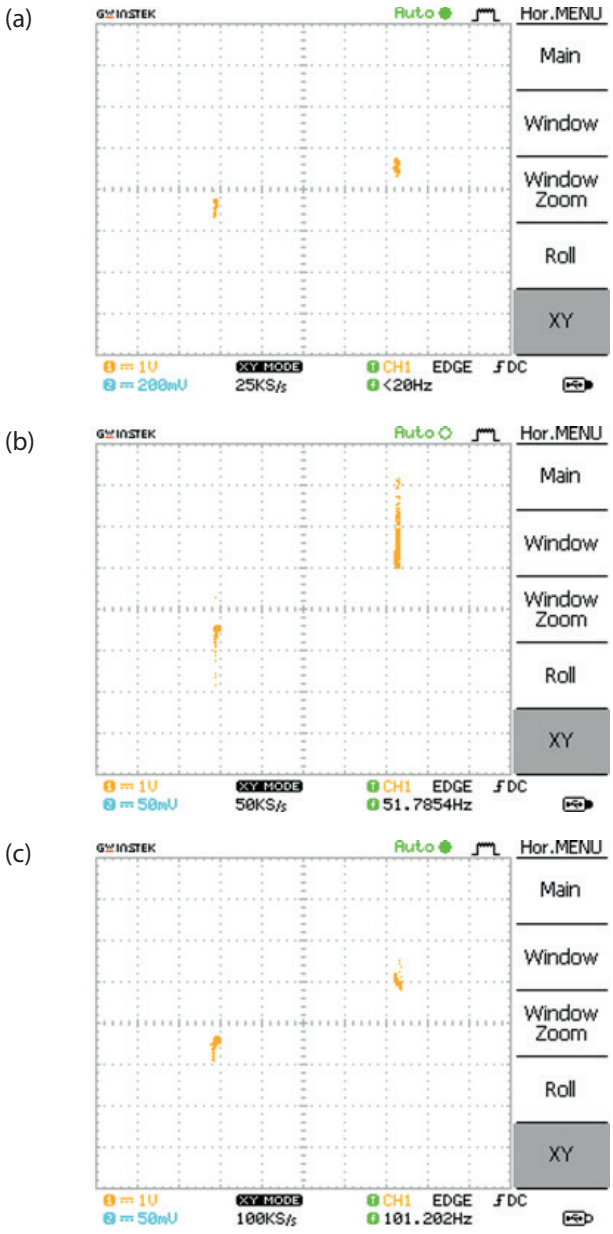


Figure 8: The hysteresis curve of the Tungsten-based memristor fed with a a) 20 Hz, b) 50 Hz, c) 100 Hz, and an approximately 2.4 V peak-to-peak square voltage.

4 Experiments

In this section, the experimental results of the Tungsten-based memristor-capacitor-protection resistor (M-C-R_s) series circuit shown in Figure 9 are given. A series protection resistor is used in all the experiments as suggested in [38] for protection and measuring the memristor current as shown in Figure 9. The circuit parameters are given in Table 1. With the M-C-R_s series circuit, the charging and discharging of the capacitor through the protection resistor and the memristor was investigated using an oscillator as a square wave voltage source and an oscilloscope. A square wave can be described as

$$V(t)=\begin{cases} V_p & , \quad 0<t<T/2 \\ -V_p & , \quad T/2<t<T \end{cases} \tag{14}$$

where V_p and T are the amplitude and the period of the square wave, respectively.

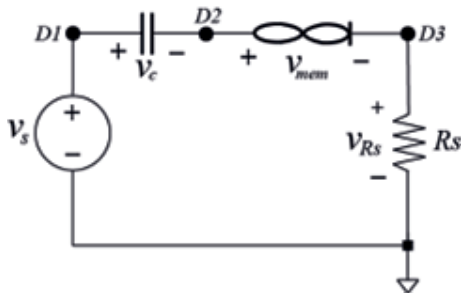


Figure 9: The Tungsten-based memristor-capacitor-protection resistor (M-C-R_s) series circuit excited with a square wave voltage source.

Table 1: The circuit parameters

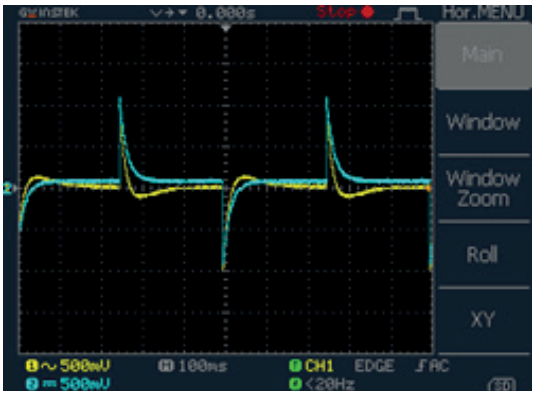
Parameter	Value
C	200 nF
R_S	99.8 kΩ

The square wave is chosen due to having both polarities which makes the examination of the polarity-dependent charging possible. The experimental results are shown in Figure 10. It can be seen that the current of the Tungsten memristor becomes negative for a while when the Tungsten memristor voltage is positive or vice versa. Also, the circuit's charging behavior is not exponential.

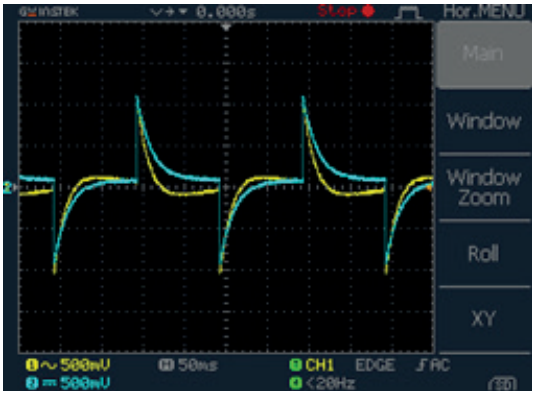
As seen in Figure 10.a, at 2 Hz, the SDC Tungsten-based memristor current and the voltage at node D2 do not always have the same polarity. The current also goes negative when the voltage at node D2 is positive or vice versa. The negative maximum value of the device current gets is low compared to the positive maximum value. The current looks like a critically damped circuit current and has a bump at the bottom. At the beginning of the positive half period, the current is maximal, then, it falls down and becomes zero, it takes negative values after that, it becomes minimal, and then it starts increasing again. The polarity of the voltage at node D2 changes before the current becomes zero or changes its polarity again. A similar description can also be made for the negative half period. The memristor current and the voltage at node D2 do not have half wave symmetry.

As seen in Figure 10.b, at 5 Hz, the SDC Tungsten-based memristor current and the voltage at node D2 do not always have the same polarity. The current also goes negative when the voltage at node D2 is positive or vice versa. The negative maximum value the device current is low compared to the positive maximum value. The current looks like a critically damped circuit current and has a bump at the bottom. At the beginning of the positive half period, the current is maximal,

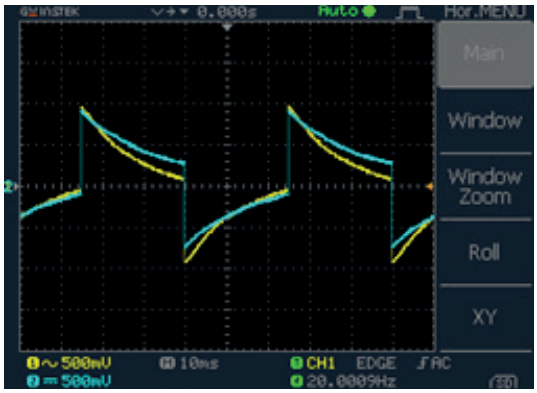
(a)



(b)



(c)



(d)

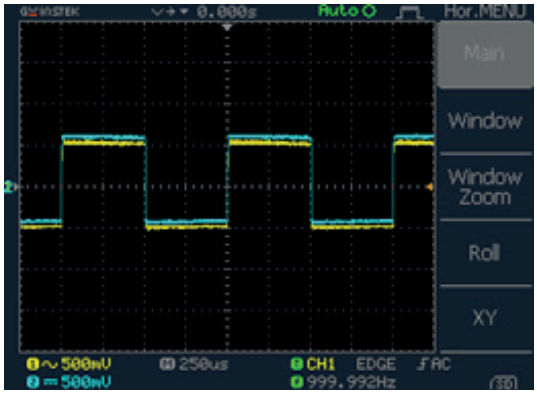


Figure 10: The current of the Tungsten-based memristor and the voltage waveform at node D2 when the M-C-R_s series circuit is fed with a a) 2 Hz, b) 5 Hz, c) 20 Hz, and d) 1 kHz, and a 2 V peak-to-peak square wave voltage.

it falls down, it becomes zero, it takes negative values, it becomes minimal, then it starts increasing again, and the polarity of the voltage at node D2 changes before the current becomes zero or changes its polarity again. A similar description can also be made for the negative half period. The current and the voltage at node D2 do not have half wave symmetry. The bump width seen in Figure 10.b is almost around the half period since the frequency of the signal is increased from 2 Hz to 5 Hz and its period is decreased.

As seen in Figure 10.c, at 20 Hz, the SDC Tungsten-based memristor current and voltage have the same polarity. The capacitive current also exists in this case. This can be explained by the fact that before the capacitive current component starts taking negative values, the polarity of the voltage changes. As seen in Figure 10.d, at a frequency high enough, at 1 kHz, in this case, the SDC Tungsten-based memristor starts behaving as a nonlinear resistor as described with one of the three fingerprints of a memristor.

Using MATLAB with the acquired data, the memristor current is calculated using Ohm's law:

$$i(t) = \frac{v_{R_S}(t)}{R_S} \tag{15}$$

The memristor current and voltage are shown in Figure 11. When excited with a sinusoidal or a square wave voltage source, the Tungsten-based SDC memristor has a zero-crossing curve as seen in Figures 6 and 8. However, when the M-C-R_s series circuit is excited with a square wave voltage source, the hysteresis curve of the memristor is not zero-crossing and its behavior is capacitive as seen in Figure 11. This phenomenon has not been reported in the literature or the datasheet until now [38]. More data on the polarity-dependent charging and discharging of capacitor circuits containing Tungsten- and Carbon-based Knowm memristors and using square waves and clock signals for forward and reverse polarities can be found in [48].

5 Discussions and model suggestions

The experimental waveforms show that a Tungsten-based SDC memristor is actually not a memristor and even not a memristive system due to lacking a zero-crossing hysteresis curve [2, 13]. Chua has described a memristor as a power-dissipating circuit component [4]. According to Chua, a memristor dissipates power and should not provide power. Also, the hysteresis of a memristor should only exist in the first and third quadrants [2, 13]. The Lissajous curves in Figure 12 show that the SDC Tungsten-based memristive system behaves as a nonlinear capacitive system since its hysteresis curves or v-i characteristics also exist in the second and the fourth quadrants where the system supplies power instead of consuming since, in the second and the fourth quadrants, its instantaneous power becomes negative:

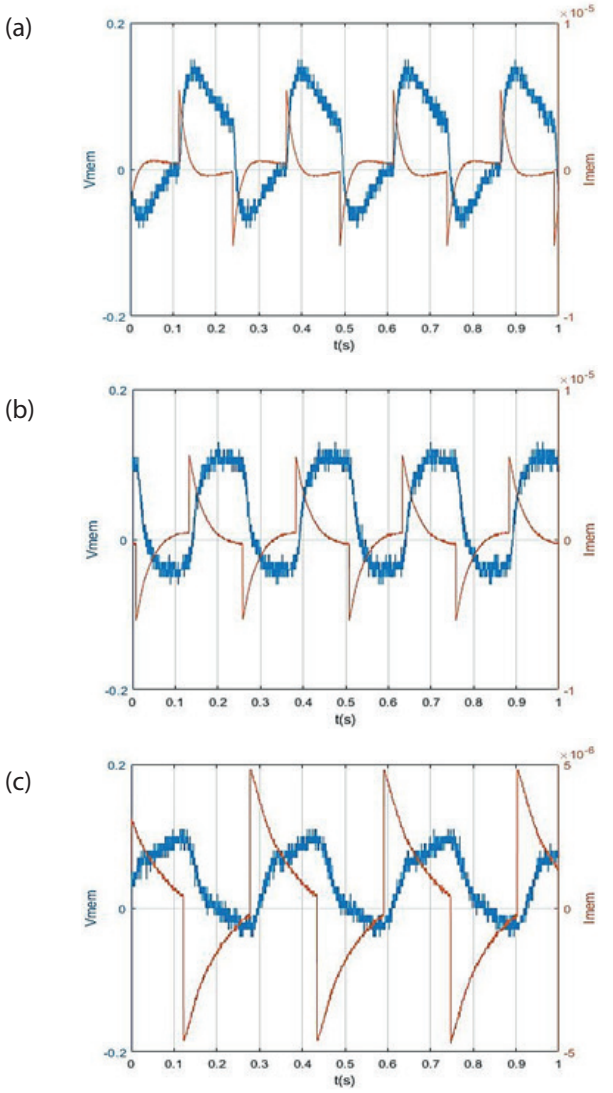


Figure 11: The time-dependent current and voltage waveforms of the Tungsten-based memristor when the M-C-R_s series circuit is fed with a a) 5 Hz, b) 10 Hz, and c) 20 Hz, and a 2 V peak-to-peak square wave voltage.

$$p(t) = v(t)i(t) < 0 \tag{16}$$

Its hysteresis curves are also in the second and fourth quadrants of the Cartesian coordinate system as shown in Figure 12.

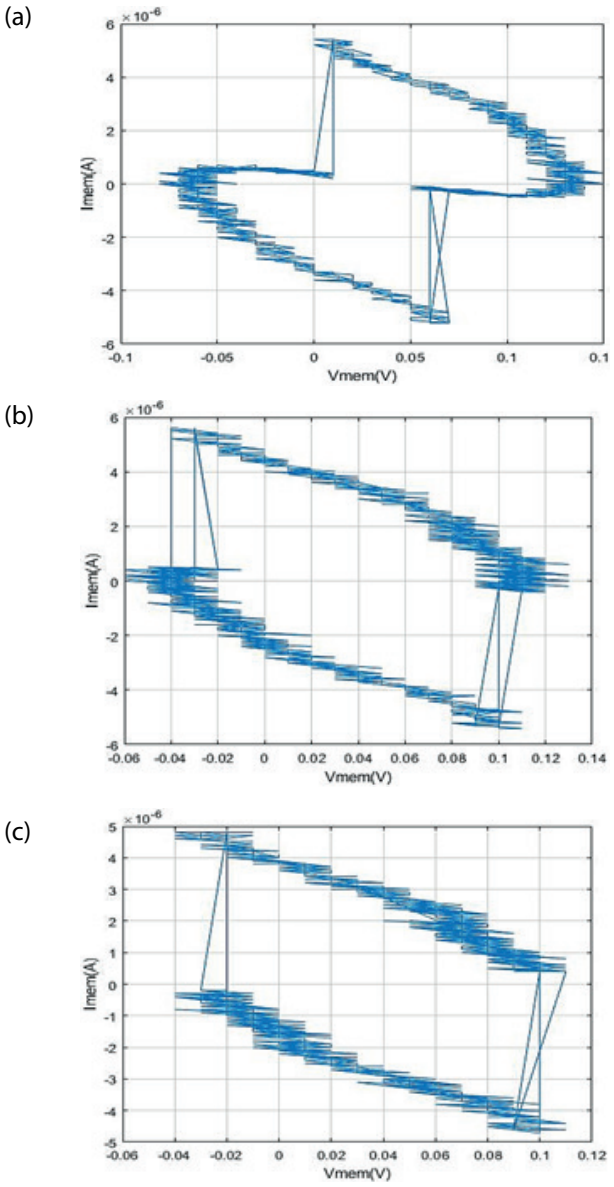


Figure 12: The hysteresis curve of the Tungsten-based memristor when the M-C-Rs series circuit is fed with a a) 5 Hz, b) 10 Hz, and c) 20 Hz, and a 2 V peak-to-peak square wave voltage.

The constitutive law of a capacitor is given as

$$i_c(t) = C\frac{dv_c(t)}{\mathrm{dt}} \tag{17}$$

A presumed current and voltage waveform of a capacitor is shown in Figure 13. The intervals where the derivatives of the memristor current are positive or negative have been marked in Figure 13. A capacitor current is positive when its voltage increases, or it charges and vice versa. If the derivative of the capacitor voltage is positive, its current is positive, and vice versa. Figure 13 is quite similar to the waveforms shown in Figure 11. However, there is a small shift at the point where the capacitor current becomes zero. This also means the memristive or resistive current component is quite low, compared to the capacitive current component. The Tungsten-based SDC memristor is actually a more complex system since it also shows a capacitive effect. Considering the voltages and currents shown in Figure 11, the Tungsten-based SDC memristor device has a capacitive behaviour. The current becomes negative even though the memristive behaviour does exist. We propose the following circuit model given in Figure 14 that explains all the phenomena. The model is made of a memristor and a memcapacitor connected in parallel.

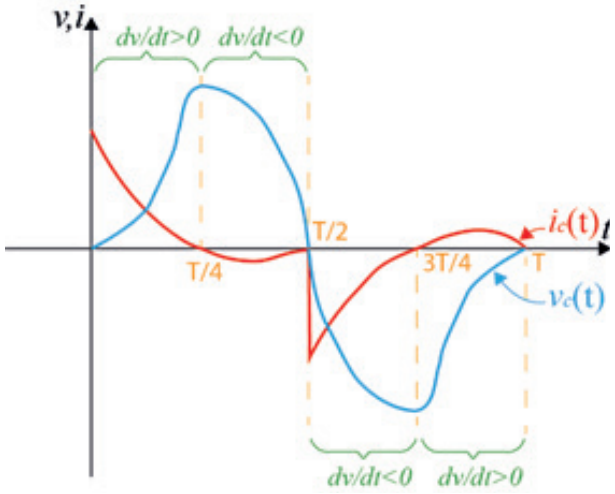


Figure 13: The representative capacitive behavior of the Tungsten memristor.

It should be examined where the capacitive current or the capacitance comes from. The simplest solution is to assume that the Schottky diode shown in the equivalent circuit given in Figure 2 has a capacitance. It is well-known that, assuming that Schottky barriers were formed at the top and bottom interfaces, the capacitance of a Schottky diode [49, 50] can be represented by:

$$C_m = \sqrt{\frac{q\varepsilon_i\ \varepsilon_0 N_D A^2}{2\left(\mathrm{V}_{bi} - V\right)}} \tag{18}$$

Where N_D is the donor density, ε_i is the relative permittivity of the interfacial layer, ε_0 is the permittivity of vacuum V_{bi}, is the built-in voltage, and V is the applied voltage.

The capacitance is dependent on the Schottky diode voltage. The lower the Schottky-diode voltage, the higher the Schottky-diode capacitance. More information on Schottky diode capacitance can be found in [49, 50]. As seen in Eq. (18), Schottky diode capacitance has

a nonlinear dependency on the Schottky diode voltage. Therefore, it is a nonlinear capacitance. The SDC Tungsten-based memristor topology and the Schottky diode topology in [49, 50] are not the same. That's why Eq. (19) cannot be used for calculation of the capacitance of the SDC Tungsten-based memristor but the Schottky diode capacitance of the SDC Tungsten-based memristor can still be assumed to be a nonlinear capacitance. A new equivalent circuit with it is given in Figure 14.a.

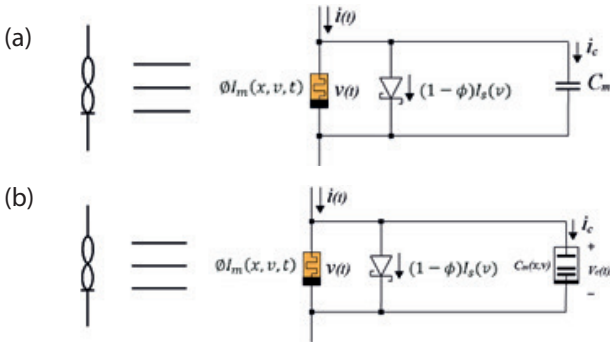


Figure 14: The new equivalent circuit of the Tungsten-based memristor a) with a nonlinear capacitor and b) a memcapacitor connected in parallel with the memristive element and the Schottky diode.

The threshold voltages of the SDC Tungsten-based memristor is given in Table 2. The forward threshold voltage of the SDC Tungsten-based memristor, ranges from 0.15 V to 0.35 V, and the reverse threshold voltage of the SDC Tungsten-based memristor, ranges from -0.27 V to -0.05 V according to [38]. Considering the voltage level of the SDC Tungsten-based memristor is less and around the threshold voltages in Figures 11 and 12, the capacitive effect may be higher if the voltage of the SDC Tungsten-based memristor is low or less than the threshold voltages.

Table 2: The threshold voltages of the SDC Tungsten-based memristor [38] W, Sn, C Types

Characteristic	Condition	Min	Typ	Max
Forward Threshold	DC/Quasi-static	0.15V	0.26V	0.35V
Reverse Threshold	DC/Quasi-static	-0.27V	-0.11V	-0.05V
Cycle Endurance	1.5Vpp, 500Hz sine wave, series resistor	50M	100M	5B

The existence of the polarity dependence of the memristor voltage and current can be seen in Figures 11 and 12. The current and voltage waveforms shown in Figure 11 also lack half-wave symmetry. The hysteresis curves are not symmetric with respect to origin as seen in Figure 12.

A Schottky diode capacitor's current is given as

$$i_c(t)=\frac{dq}{\mathrm{dt}}=\frac{dq}{\mathrm{d}v_c}\frac{dv_c(t)}{\mathrm{dt}}=C_m(v_c)\frac{dv_c(t)}{\mathrm{dt}}= \\ =C_m(v)\frac{dv(t)}{\mathrm{dt}} \tag{19}$$

where q is the Schottky diode charge.

The Schottky diode capacitance function, $C_m(v)$, is not written explicitly, and it requires further work to find its expression. The equation set describing the Tungsten-based memristor equivalent circuit with the nonlinear capacitor is given as

$$i(t)=\left(\frac{\phi x}{R_{ON}}+\frac{\phi(1-x)}{R_{OFF}}\right)v(t)+ \\ (1-\Phi)\alpha\left(e^{\beta_1 v(t)}-e^{-\beta_2 v(t)}\right)+ \\ +C_m(v)\frac{dv(t)}{\mathrm{dt}} \tag{20}$$

$$\frac{dx}{dt}=\frac{1}{\tau}\left(\frac{1}{1+e^{-\beta(v-V_{ON})}}(1-x)-\left(1-\frac{1}{1+e^{-\beta(v+V_{OFF})}}\right)x\right) \tag{21}$$

The Tungsten-based SDC memristor may be showing a memcapacitive effect. The Schottky diode capacitance may be dependent on the state variable of the Tungsten-based memristor, $x(t)$, besides its voltage. In this case, it can be modeled as a memcapacitor as shown in Figure 14.b. If there is only one state variable, the current of a memcapacitive system can be given as

$$i_c(t)=\frac{dq_c(t)}{\mathrm{dt}}=\frac{d\left(C\left(x(t),v_c(t),t\right)v_c(t)\right)}{\mathrm{dt}}= \\ =\frac{\partial\left(C\left(x,\,v(t),\,t\right)\right)}{\partial \mathrm{x}}\frac{dx}{\mathrm{dt}}v_c(t)+ \\ +C\left(x(t),v_c(t),t\right)\frac{dv_c(t)}{\mathrm{dt}} \tag{22}$$

By substituting Eq. (21) to Eq. (22), its current turns into:

$$i_c(t)=\frac{\partial\left(C\left(x,\,v(t),\,t\right)\right)}{\partial \mathrm{x}}\left(\frac{(1-x)}{1+e^{-\beta(v-V_{ON})}}- \right. \\ \left.-\left(1-\frac{1}{1+e^{-\beta(v+V_{OFF})}}\right)x\right)\frac{v_c(t)}{\tau}+ \\ +C\left(x(t),v_c(t),t\right)\frac{dv_c(t)}{\mathrm{dt}} \tag{23}$$

As seen in Eq. (23), a memcapacitor is a more complex component than a nonlinear capacitor with only voltage dependence given in Eq. (19). Since a Knowm memristor is used with a protection resistor, the equivalent circuits given in in Figure 15.

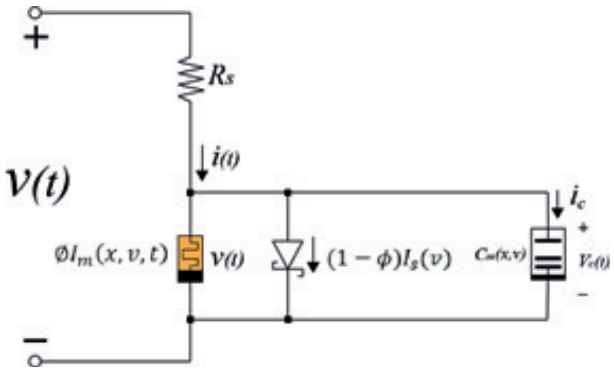


Figure 15: The equivalent circuit of the Tungsten-based Knowm Memristor.

The equation set describing the Tungsten-based memristor equivalent circuit with a memcapacitor and the series protection resistor can be given as

$$\begin{aligned} i(t) = &\left(\frac{\phi x}{R_{ON}} + \frac{\phi(1-x)}{R_{OFF}}\right) v_c(t) + \\ &+ (1-\Phi)\alpha\left(e^{\beta_1 v_c(t)} - e^{-\beta_2 v_c(t)}\right) + \\ &+ \frac{\partial\left(C\left(x,\, v(t),\, t\right)\right)}{\partial \mathrm{x}} \frac{dx}{\mathrm{dt}} v_c(t) + \\ &+ C\left(x, v_c(t), t\right) \frac{dv_c(t)}{\mathrm{dt}} \end{aligned} \tag{24}$$

$$\frac{dx}{dt} = \frac{1}{\tau}\left(\frac{1}{1+e^{-\beta(v_c - V_{ON})}}(1-x) - \left(1 - \frac{1}{1+e^{-\beta(v_c + V_{OFF})}}\right)x\right) \tag{25}$$

$$\frac{dv_c}{dt} = \frac{v(t) - v_c(t)}{R_s} \tag{26}$$

Eq. (26), the rate of change of the Tungsten voltage, is added to the Tungsten-based memristor system to distinguish Schottky diode charge and the memristive element charge, which are different or their state variables might be different or the Schottky diode memcapacitance might be dependent on two variables while the memristive element has only one state variable.

Mouttet has described memadmittance systems in [51]. Due to the existence of both the memristive and nonlinear capacitive or memcapacitive effects, the Tungsten-based memristor, in fact, must be called a Tungsten-based memadmittance system. Tungsten-based memadmittance system is abbreviated as (TBMS). The TBMS has actually richer dynamics than those described by Eq.s (10)-(11) as seen from Eq.s (24)-(26). The equations describing the behaviour of the chaotic circuits given in [39, 40] can also be modified or should be rewritten after finding a better model for the TBMS.

Since the the Tungsten-based memristor has a different topology than a Schottky diode, it is not obvious whether its capacitance is maximal at zero voltage. Under sinusoidal excitation, a zero-crossing hysteresis curve is possible as shown in Figure 6. Under square-wave excitation as shown in Figure 8, the hysteresis curve is in the first and the third quadrants, but the oscilloscope is unable to catch the curve passing through the origin. In our opinion, the capacitive current does also exist under square-wave excitation, but it needs further inspection why the hysteresis curve has zero crossing. Perhaps, it is not a zero-crossing curve, and the capacitive current component is much lower than the resistive current component, and the curve only looks like a zero-crossing hysteresis curve. If the device capacitance satisfies the following condition, the zero-crossing of the hysteresis curves becomes possible for both square and sinusoidal waves. If the device voltage *v(t)* = 0, the device capacitance is always zero:

$$C\left(x,0,t\right) = 0 \tag{27}$$

Therefore, when *v(t)* = 0, the capacitive current component of the device given by Eq. (22) turns into

$$i_c(t) = \frac{\partial\left(C\left(x,\, v(t),\, t\right)\right)}{\partial \mathrm{x}} \frac{dx}{\mathrm{dt}} 0 + C\left(x(t), 0, t\right) \frac{dv_c(t)}{\mathrm{dt}} = 0 \tag{28}$$

This causes the capacitive effect or the current of the capacitance of the system to vanish and a zero-crossing of the hysteresis curve to occur when the memristor voltage becomes zero. However, it should be examined whether this is true or not.

Due to having sufficiently high slopes, the waveforms in Figure 11 create a very high capacitive current large enough to make the device current become negative. This is not possible under square wave excitation since the square wave voltage has a very high slope while changing polarity but a zero slope after that.

If the capacitive current is much lower than the memristive current, its effect may not appear in the waveforms acquired and this may be the reason why the capacitive effects were not discovered and reported in the literature previously.

6 Conclusions

In this paper, the charging of the capacitor placed in series with a Tungsten-based memristor, and a resistor are examined experimentally by taking the polarity of the memristor into account. As a result of the experiments made:

- The charging of the capacitor is analyzed for both polarities of the memristor in the M-C-Rs series circuit. The charging of the M-C-R_s series circuit is found to be polarity dependent.
- In these experiments, it can be seen that the capacitor is not charged exponentially since the memristor current flows also in the opposite direction to the applied voltage for a while.
- In the literature review we conducted, it was seen that the Silver-Carbon-Silver (Ag-Carbon-Ag) topology was reported to behave as a system showing both memristive and memcapacitive effects without zero-crossing behavior [52]. We report that the tungsten-based memristor used in this study also exhibits capacitive or memcapacitive behavior.
- One of the findings of the paper is that "the SDC Tungsten-based Knowm Memristor" is not an ideal memristive system beside not being an ideal memristor.
- Another finding is that zero-crossing hysteresis curve and three fingerprints of a memristor is not always a signature of a memristive system, i.e., having the three fingerprints does not guarantee that it is a memristive system. All frequencies and voltage levels of a system must be considered. There may be a need for describing merged memristive and memcapacitive systems.
- It has been observed that the tungsten-based SDC memristor in the M-C-Rs circuit does not exhibit a considerable stochastic behavior as a Carbon-based SDC memristor does [48], but it behaves like a nonlinear R-C circuit at low frequencies and at the voltage levels examined.
- In this study, it has been found that Tungsten-based SDC memristor exhibit a capacitive behavior and a non-zero-crossing hysteresis curve. Therefore, it cannot be described only by the MMSMM model. Perhaps, the memcapacitive system equations, coupled with the equations of the MMSMM model can be used to model such a (memristive!) system. Here, we have suggested such a model without giving much detail. We suggest studying of the details of the memadmittance model as future work.
- The capacitance effects might be more dominant below threshold voltages and low frequencies.
- Since the MMSMM model, that does not include the capacitive effects, cannot accurately model the Tungsten-based memristors, the M-C-Rs series circuit cannot be analyzed using the MMSMM model.
- It is also true that the nonlinear dopant drift models [14-20] are not sufficient to model the Tungsten-based memristors since the models lack capacitive effects. Therefore, the M-C-Rs series circuit cannot be analyzed accurately using the nonlinear dopant drift models.
- As future work, the capacitive effects may be included using Shottky capacitance equation or modifying it to have a state variable dependency to include the memcapacitive effects. The behavior of the capacitance may be polarity dependent as shown in the experimental results section.
- Complete analysis of the M-C-Rs circuit can only be done after the Tungsten-based memristor is understood better and a more accurate Tungsten-based memadmitance model emerges.
- The Knowm memristor is shown to keep its state and its resistance can be tuned [38, 53]. This means that when its voltage is equal to zero its memristance value stays constant. If the condition given in Equation (27) is true and when the device voltage is zero, the memristor keeps its state. However, if the device capacitance is not zero when the device voltage is zero, this may result in information loss of the state of the device. Due to its importance, we also suggest this as future work.

More experimental data for M-C-Rs charging and discharging circuits with Tungsten- and Carbon-based Knowm memristors can be found in [48]. The resistive switching device measuring techniques are reviewed in [54], and it is implied that the parasitic capacitances existent in the test setup systems must also be considered and their effect on the measurements of the oxygen-ion-based ReRAMs must be minimized. Although SDC memristors belong to the metal-ion memristive systems, the same techniques suggested in [54] can be utilized to obtain better accuracy while acquiring the data to model their capacitive behavior by also considering the effect of the suggested protection resistor together with the parasitic capacitances on the device dynamics. This study can guide the researchers who will work in this direction in terms of methodology and experimental data. Tungsten-based Knowm memristors have complex structures [38]. Circuits such as programmable oscillators, comparators, and learning circuits [11] can be made with them. They need accurate models or more complex equivalent circuits perhaps involving memcapacitors to obtain the best performance from them.

7 Acknowledgment

This study was supported using the memristors bought by the project supported by the Scientific Research Projects Coordination Unit of Tekirdağ Namık Kemal University. Project number: NKUBAP.42.GA.19.206.

8 Conflict of interest

No conflict of interest was declared by the authors.

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Arrived: 20. 07. 2023
Accepted: 06. 11. 2023

Original scientific paper
https://doi.org/10.33180/InfMIDEM2023.302

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 53, No. 3(2023), 137 – 144

Parallel Routing for FPGA Using Improved Lagrange Heuristics with Sub-Gradient Method and Steiner Tree

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Abstract: One of the most time-consuming processes in the Field Programmable Gate Array (FPGA) design cycle is the routing of the nets. For this reason, versatile Place and Route (VPR), a widely used algorithm, routes efficiently but takes a long time to complete. Using parallelization is one approach to quicken this design flow. A method based on Linear Programming (LP) might be employed to enhance the speed of this routing process further. This strategy, however, has two drawbacks: a local minimum and the solution's violation of boundaries. So, to overcome these issues, this paper proposed Parallel Routing for FPGA Using Improved Lagrange Heuristics with a Sub-Gradient method and Steiner tree (PR-ILH). The Lagrange relaxation process is enhanced by a series of innovative Lagrange heuristics presented in this work. Lagrange heuristics and sub-gradient optimization are both made use of by PR-ILH, which combines their advantages to provide more effective routing while reducing the complexity of parameter tuning. The use of the Steiner tree further improves the usage of resources and overall performance. It has also provided an improved method for updating the step size that this iterative process takes. Tests have been conducted on standard metrics, demonstrating that the proposed approach surpasses the ParaLaR and other existing improved techniques. Compared to ParaLaR, the proposed PR-ILH approach can enhance the minimum channel width and the violation of the restrictions by up to 25.1%. Compared to ParaLaR, PR-ILH realizes savings of roughly 15.4% in the total wire length. PR-ILH algorithm effectively reduces route latency, improving circuit speed and responsiveness in the FPGA routing process.

Keywords: Parallel Routing, FPGA, VPR, Sub-gradient, Improved Lagrange Heuristics, Steiner tree.

Vzporedno usmerjanje FPGA-ja z uporabo izboljšane Lagrangeove hevristike s podgradientno metodo in Steinerjevim drevesom

Izvleček: Usmerjanje mrež je eden najbolj zamudnih procesov v načrtovalskem ciklu FPGA (Field Programmable Gate Array). Zaradi tega pogosto uporabljen in vsestranski Place and Route (VPR) algoritem usmerja učinkovito, vendar časovno potratno. Uporaba paralelizacije je eden od pristopov za pospešitev tega načrtovanja. Za nadaljnje povečanje hitrosti tega procesa usmerjanja bi lahko uporabili metodo, ki temelji na linearnem programiranju (LP). Ta strategija pa ima dve pomanjkljivosti: lokalni minimum in kršitev robnih pogojev. Da bi premagali ta vprašanja, članek predlaga vzporedno usmerjanje za FPGA z uporabo izboljšane Lagrangeeve hevristike z metodo podgradienta in Steinerjevim drevesom (PR-ILH). Lagrangeev sprostitveni proces je izboljšan z nizom inovativnih Lagrangeovih hevristik. Lagrangevo hevristiko in podgradientno optimizacijo uporablja PR-ILH, ki združuje njune prednosti za zagotavljanje učinkovitejšega usmerjanja in hkrati zmanjšuje kompleksnost prilagajanja parametrov. Uporaba Steinerjevega drevesa dodatno izboljša uporabo virov in splošno učinkovitost. Opravljeni so bili testi na standardnih metrikah, ki dokazujejo, da predlagani pristop presega ParaLaR in druge obstoječe izboljšane tehnike. V primerjavi s ParaLaR lahko predlagani pristop PR-ILH poveča minimalno širino kanala in kršitev omejitev za do 25,1 %. V primerjavi s ParaLaR, PR-ILH realizira približno 15,4 % prihranek pri skupni dolžini žice. Algoritem PR-ILH učinkovito zmanjša zakasnitev poti, izboljša hitrost vezja in odzivnost v procesu usmerjanja FPGA.

Ključne besede: Vzporedno usmerjanje, FPGA, VPR, podgradient, izboljšana Lagrangeeva hevristika, Steinerjevo drevo.

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How to cite:
P. Balasubramaniam, "Parallel Routing for FPGA Using Improved Lagrange Heuristics with Sub-Gradient Method and Steiner Tree", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 53, No. 3(2023), pp. 137–144

1 Introduction to FPGA routing

Moore's law states that an integrated circuit's transistor count doubles roughly every two years. One of the most demanding processes in the FPGA [1] design cycle is the routing of nets, which are groups of two or more linked devices. One barrier to the broad usage of FPGA technology is the slow performance of conventional CAD software. Routing is frequently the most crucial stage in a normal CAD flow concerning runtime and overall performance since it directly impacts the clock frequency that may be used. Almost all contemporary FPGA routers can be traced back to 1995 by introducing the PathFinder algorithm [2].

Therefore, it is necessary to create fast routing algorithms that address the issue of the growing number of transistors per chip and, as a result, the lengthened runtime of FPGA-CAD tools. There are two methods to do this. First, run the routing algorithms in parallel on systems with several cores. The pathfinder method [3] is essentially sequential among the most popular FPGA routing algorithms. Therefore, this method is unsuitable for parallel running the FPGA routing algorithms.

Second, users may split their designs, build each component one at a time, and combine all the pieces to create the complete design rather than compiling it all at once. This strategy has been suggested in [4]. There is no certainty that there will be balanced partitioning because another could own the routing assets needed by one partition. In other words, this strategy must address the issues when routing resources are shared.

The suggested routing method is built on the Improved Lagrange Heuristics. By iteratively changing the Lagrange multipliers for every constraint, the Lagrange heuristics have previously been used in FPGA routing to produce workable solutions [5]. Innovative techniques are added to the Lagrange heuristics in the present work to address the intrinsic complexity of contemporary FPGA designs. The suggested approach considerably speeds up the routing process while maintaining the ability to provide superior routing alternatives by using the parallelism present in FPGA systems.

The Sub-Gradient approach, a practical optimization approach, is used to improve the effectiveness of the routing process further [6]. The suggested strategy effectively examines the solution space by utilizing sub-gradients, gradually getting closer to almost ideal routing topologies. With this improvement, the FPGA router can handle more complicated designs with less computing effort and reach quicker convergence.

Another crucial component of the suggested strategy is the development of the Steiner tree. Wire length and communication delays are significantly decreased by using Steiner trees for connecting logic components efficiently and compactly [7]. The parallel routing approach displays its capacity to produce routing strategies that maximize crucial parameters, such as wire length and signal propagation time, by including Steiner tree building into the enhanced Lagrange heuristics and sub-gradient method. The suggested way demonstrates its superiority over conventional routing strategies through thorough simulations and evaluation across multiple FPGA designs, making it an intriguing contender for enhancing the performance of contemporary FPGA-based systems.

The rest of the paper has been organized as follows: Section 2 describes related research on heuristic modelling for parallel FPGA routing. Section 3 Parallel Routing for FPGA Using Improved Lagrange Heuristics with Sub-Gradient method and Steiner tree (PR-ILH). Results and discussion have been given in section 4. Finally, the conclusion, limitations, and scope for further research have been shown in section 5.

2 Related works on heuristic modelling for parallel FPGA routing

The success of the semiconductor sector over the past fifty years has primarily been attributed to the Electronic Design Automation (EDA) method. However, routing accounting for a sizable portion of this takes a lot of time. This work concentrates on a sizable portion of this issue, namely the expensive FPGA routing procedure. Heuristic modelling for parallel FPGA routing has received a lot of research attention.

A parallel FPGA router based on Lagrangian relaxation was suggested by Hoo et al. (2015) called ParaLaR [8]. The routing task was divided into minor problems that could be handled in parallel using Lagrangian relaxation. Compared to conventional approaches, the ParaLaR router reduced routing time by an average of 20%, considering several benchmarks. A real-time Monte Carlo optimization method for FPGA was provided by Lee and Kim (2019) to create efficient and dependable message chain topologies [9]. They used Monte Carlo simulations to optimize the message chain topology in FPGA designs and increase performance and reliability. The suggested method was tested on several FPGA architectures and showed a mean performance gain of 15%. A novel face algorithm employing Lower-Upper (LU) factorization for LP was presented by PAN (2020) [10]. The suggested approach sought to resolve LP is-

sues using LU factorization techniques effectively. In several LP examples, the algorithm's performance was evaluated, and it produced results that were competitive with those of already available methods.

Fuzzy Linear Programming (FLP) problems were addressed by models and methods provided by Ghanbari et al. in 2020. To deal with limitations and goal function inconsistencies, the study developed an FLP technique [11]. Various FLP situations were used to test the suggested models and remedies, demonstrating how well they handled uncertainty. For multi-FPGA systems, Pui and Young (2020) presented a Lagrangian relaxation-based Time-Division Multiplexing (TDM) optimization [12]. To maximize resource efficiency and minimize communication overhead, their solution used Lagrangian relaxation to optimize the objectives of multi-FPGA systems. Two benefits of this method are the potential to reduce connectivity constraints and make optimum use of resources in multi-FPGA systems. The requirement for meticulous parameter tuning in the Lagrangian relaxation process is a constraint, though.

The parallel FPGA router Agrawal et al. (2018) developed uses the Steiner tree and sub-gradient approach [13]. By applying the sub-gradient approach to enhance Steiner trees, the method attempted to parallelize the routing procedure. Several metrics were used to assess the parallel router, which showed a 30% decrease in routing time compared to sequential techniques. Using the primal-dual sub-gradient approach, Agrawal et al. (2019) proposed ParaLarPD, a parallel FPGA router [14]. The primary goals of the strategy were to parallelize the router and apply the primal-dual sub-gradient technique to improve Steiner trees. On several evaluations, the ParaLarPD router reduced routing time by 25% compared to sequential methods. The authors suggested a parallel FPGA router called ParaLarH, based on Lagrange heuristics, in [15]. The approach sought to improve FPGA routing by parallelizing the router and applying Lagrange heuristics. On numerous evaluations, the ParaLarH router significantly shortened the routing time compared to sequential techniques.

The studies above suggest multiple parallel FPGA routers using optimization methods, including Steiner trees, sub-gradient techniques, and Lagrangian relaxation. There are, however, several flaws that these studies have. Firstly, the complete examination of various FPGA designs and circumstances is lacking, which hurts the generalizability and applicability of the suggested methodologies. Second, the techniques are less appropriate for resource-constrained FPGA designs due to the additional complexity of parallelization, which may require significant FPGA resources and provide implementation difficulties. Furthermore, tuning and parameter sensitivity concerns may impact the efficiency of some heuristic-based systems. A unified and thorough methodology has been required to overcome these shortcomings and enhance the effectiveness of FPGA routing. So, the PR-ILH approach has been suggested in this paper.

3 Parallel routing for FPGA using improved lagrange heuristics with sub-gradient method and steiner tree (PR-ILH)

Lagrange heuristics and sub-gradient optimization are both made use of by PR-ILH, which combines their advantages to provide more effective routing while reducing the complexity of parameter tuning. The use of Steiner trees further improves the usage of resources and general efficiency. PR-ILH guarantees increased performance, decreased latency, and wire length reductions by completing thorough assessments of various FPGA designs and scenarios. In the end, PR-ILH solves the shortcomings of prior works by providing a more usable, effective, and flexible parallel routing solution for FPGA designs.

A weighted matrix grid MG(Vx, Ed) with a collection of vertices Vx and edges Ed, where a cost is linked with each edge, is a common formulation for the routing problem in FPGA or EDA. There are three different kinds of vertices in this grid matrix: Net Vertices (NV), Steiner Vertices (SV), and Additional Vertices (AV). A set N⊆Vx that contains all of the NV is how a net is defined. The route of a net, or a sub-tree ST of the grid matrix MG, is built using an SV, which is not an integral component of the NV. The term "Steiner tree" can also refer to a net tree.

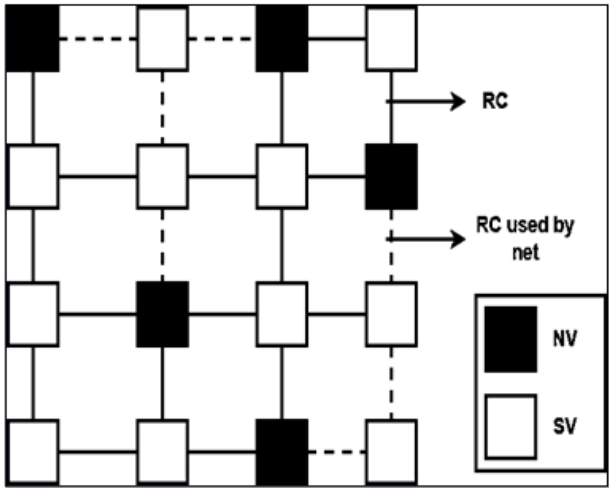

Figure 1: A weighted matrix grid MG(Vx, Ed)

An example of a 4x4 matrix grid is shown in Figure.1. In Figure 1, the NV is represented by the green colour squares, the SV by the blue colour squares, and the AV by the white colour squares. The horizontal and vertical lines represent the edges; these edges carry a cost, which is not indicated here. The dotted borders depict two net trees. The continuous lines represent the Routing Channel (RC), and the dotted lines represent the RC used by the net.

Each net's vertices and a total number of nets are specified. Finding a route for every net must be done so that the sum of all the routes minimizes the matrix MG overall path cost. Here, reducing the required channel width for every edge is also important. The routing of nets problem is presented as the following objective function (LP problem) to accomplish the two goals mentioned above:

$$F(y) = Min_{y_{ed,j}} \sum_{j=1}^{N_{net}} \sum_{ed \in Ed} C_{ed} y_{ed,j} \quad (1a)$$

$$\sum_{j=1}^{N_{net}} y_{ed,j} < T, y_{ed,j} = 0/1 \quad (1b)$$

where, $NA_j y_j = b_j, j = 1,2,\ldots.N_{net}$

N_{net} is the number of nets, *ed* is the set of edges, and C_{ed} is the cost or latency linked with each edge Ed. The proposed optimization issue seeks to reduce the overall route cost of FPGA routing. NA_j is the node-arch occurrence matrix, b_j is the demand or supply vector, and y_i is an array of all $y_{ed,j}$ for net j corresponding to the jth net's path tree. $y_{ed,j}$ is the choice factor that signals whether an edge (routing channel) *ed* is employed by the net j (value 1) or not (value 0). The channel width restrictions, or disparity constraints, limit the number of nets that can use an edge to a constant T (which is also consistently reduced). The equality requirements, which ensure that a legitimate route tree is created for each net, have been inherently met by the technique to solve the problem. The LP mentioned above must be parallelized to locate a workable path for each net effectively. The following discussion will focus on the two primary difficulties present.

To limit the Channel Width (CW) of routing pathways in a design, CW restrictions are applied to the basic objective function in optimization problems. The purpose is to identify an ideal solution that minimizes or maximizes the objective function while satisfying these limitations. The Lagrange relaxation method addresses constraints in optimization problems by transforming restrictions into penalty factors inside the objective function. As a result, the limitations might be loosened up and considered indirectly throughout the optimization procedure. For every constraint, the approach entails the introduction of Lagrange multipliers, also referred to as dual factors. When the restrictions are broken, these Lagrange multipliers are weights that punish the goal function. For an LP issue with an objective function F(y) and CW constraints $\Sigma(j-1)(N_{net})(y_{ed,j})-T$ where $y_{ed,j}$ signifies the decision variables, the revised LP with Lagrange relaxation is given as ∂_{Ed} times (Lagrange multiplier) the CW constraints and has been characterized as:

$$Min_{y_{ed,j}}[\sum_{j=1}^{N_{net}} \sum_{ed \in Ed} C_{ed} y_{ed,j} + \sum_{ed \in Ed} \partial_{Ed} (\sum_{j=1}^{N_{net}} y_{ed,j} - T)] \quad (2)$$

$$[NA] - jyj = b - j, j = 1,2,\ldots\ldots N, \partial_{ed,j} \geq 0$$

where, ⟦NA⟧_j y_j=b_j,j=1,2,….N_net,∂_Ed≥0

The Lagrange multiplier linked to the CW restriction

$$\left(\sum_{ed \in Ed} C_{ed} \partial_{ed} \sum_{(j=1)(N_{net})} [y_{ed,j} - T] \right)$$

is represented by the symbol ∂_Ed in the equation (2). The CW constraints in the problem are represented by the $\sum_{ed \in Ed} C_{ed} \partial_{ed}$. By including penalty factors proportionate to each constraint's violation, the Lagrange relaxation effectively integrates the restrictions into the objective function F(y).

The Simplex technique or interior-point methods are popular optimization algorithms used to find the solution to the modified LP with Lagrange relaxation. The technique converges to an ideal state that meets the CW constraints while lowering the objective function by iteratively changing the Lagrange multipliers and the decision factors. Lagrange relaxation is a versatile and powerful method for handling design constraints in optimization problems that may be used for a variety of optimization problems in engineering, operations management, and other disciplines.

The choice factors $y_{ed,j}$ present the second difficulty in solving the LP given by (1) or the revised LP with the Lagrange multiplier given by equation (2). As mentioned previously, if the net j uses the edge Ed, then the choice factor $y_{ed,j}$ must take a value of either 0 or 1; otherwise, $y_{ed,j}$ must take a value of 0. This is a Binary Integer Linear Program (BILP), which cannot be addressed with standard techniques like the Simplex or interior point approach because it is non-differentiable. Sub-gradi-

ent-based techniques, the approximation approach, etc., are some ways to handle non-differentiable optimization problems.

3.1 Sub-gradient method

The techniques based on sub-gradients are frequently used for minimizing non-differentiable functions F(y). These are recursive and refresh the factor y as $y^{l+1} = y^{1} - lh^{l}$, where l and h^{l} are the step size and a sub-gradient of the objective function at iteration l, respectively. A sub-gradient-based technique only yields the Lagrange relaxation multipliers rather than directly solving the LP provided in equation (2). The minimal Steiner tree approach is then applied in parallel for FPGA routing after this (i.e., after calculating Lagrange relaxation multipliers). The choice variables $y_{ed,j} \in 1,2,\ldots.N\_net$ in this situation can only have binary values. Sub-gradient methods alone will not always produce binary outcomes.

3.2 Steiner tree approach

Determining the shortest tree that links a specific number of nodes (terminals) in a graph is a common optimization issue that may be solved using the minimum Steiner tree methodology. Due to the Steiner tree problem's NP-hardness, it can be time-consuming and costly to compute the precise answer for large graphs. In the framework of FPGA routing, the graph depicts the routing architecture of the FPGA, and the terminals stand in for the source and destination locations that have to be linked.

The minimum Steiner tree method seeks to concurrently optimize the routing pathways for multiple links when used in parallel for FPGA routing. It considers all source and destination pairs and identifies the shortest trees that effectively link them. This method is particularly helpful in FPGA routing, where several routing pathways between different design elements must be built. The FPGA router can effectively determine the best routing pathways for multiple links simultaneously by addressing the minimum Steiner tree issue in parallel. This decreases the total routing time and boosts the efficiency of the FPGA design.

4 Improved lagrange heuristics with sub-gradient method and steiner tree (PR-ILH)

At first, the ParaLarPD technique described in [14] was used to perform FPGA routing in the suggested PR-ILH strategy. Since the acquired solution frequently violates some restrictions, a heuristic has been designed that makes the impossible solution possible (i.e., addresses the problem of the constraint violation). The Lagrangian multipliers are introduced, and the sub-gradient approach and minimal Steiner tree method are used to solve them. As anticipated, the discovered solutions are not always workable. Thus, a Lagrange heuristic has been developed. This allocates the likelihood of the restrictions violation based on particular solution aspects.

Figure.2 depicts the Lagrange heuristics verified with a sub-graph. The fundamental Lagrangian heuristic to fix the constraints violation in [14] comprises the following phases. Here, at first, these phases are described with the help of the example in Fig. 2, and then an algorithm is provided. For example, the channel widths calculated by [14] have been written adjacent to the relevant edge in fig. 2. Three edges have been present where the constraints are violated since T is assumed to be forty, and the three edges in Fig. 2 that are depicted as bolded lines, such as AE, BF, and DH.

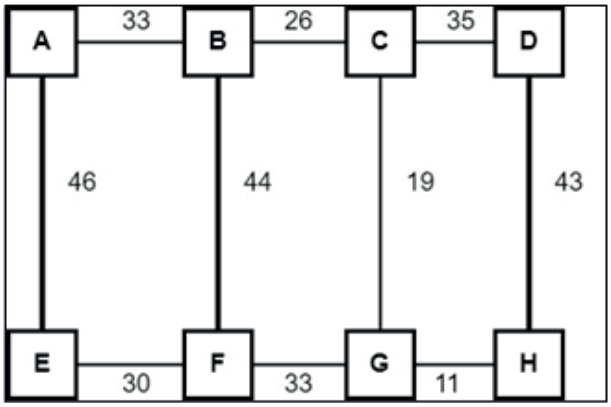

Figure 2: The Lagrange Heuristics verified with a sub-graph

Step 2: Calculate each edge's ability to route more nets down the new route without violating the limitations. The lowest of these capabilities is the Threshold and is employed when in the future. Mathematically, the Threshold has been given as follows:

$$\text{Threshold} = minimize\left[T - \sum_{j=1}^{N_{net}} y_{ed_l,j}\right], \quad (3)$$

l∈(Ed in the new route)

From equation (3), the value of Threshold is found to be 8.

Step 3: The amount of constraint violation has been given as:

$$f = \sum_{j=1}^{N_{net}} y_{ed,j} - T \quad (4)$$

Compute the number of nets where the constraints-violating edge has to be substituted with the chosen new route for the edge being considered, Ed. It is calculated such that no Ed in the new path has the constraint violation and is given as

$$R = minimum\left(Threshold, f\right) \quad (5)$$

For the edge BF, based on equation (4) f=44-40=4 and from equation (5), R=minimum (8,4) = 4.

Step 4: In R number of nets, finally, swap out this edge under investigation with the chosen path. This equates to changing BF in three nets from BF to BC→CG→GF in this case.

Step 5: The restriction violation in the edge under examination has not been removed entirely if the Threshold in equation (5) is less than f. If this is the case, the search for a different route must be restarted until the violation is eradicated or a different route cannot be found.

The processes as mentioned above have been repeated for each edge that deviates from the restrictions. The minimal CW is directly involved in this violation. . For large optimization problems, Lagrangian relaxation may be used to take advantage of the problem's structure and generate constraints on the optimum goal. These limitations form the backbone of several numerical algorithms and serve as an indicator of the algorithm's overall performance. Many heuristics and approximation methods have a Lagrangian solution as their starting point or reference point

5 Results and discussion

Tests have been carried out on a computer with a single Intel(R) Xeon(R) CPU E5-1620 v3 operating at 2.5 GHz and 64 GB of RAM. The kernel version is 3.13.0-100, and the operating system is Ubuntu 14.04 LTS. The code is written in C++11 and compiled with GCC version 4.84; the code that has been compiled is then executed utilizing various thread counts. ParaLaR [8], ParaLarPD [14], and ParaLarH [15] methods have been compared to the proposed approach. ParaLaR and VPR, 7.0 from the Verilog-to-Routing (VTR) package, were built using the same GCC version for comparison. Several settings in the input-output pad and the configuration logic blocks (CLBs) of ParaLarPD and ParaLaR have been updated to operate them identically as in the proposed model. MCNC benchmark circuits [16], which come in various sizes for the logic blocks, have been evaluated. The maximum number of sub-gradient technique iterations that have been utilized is 45.

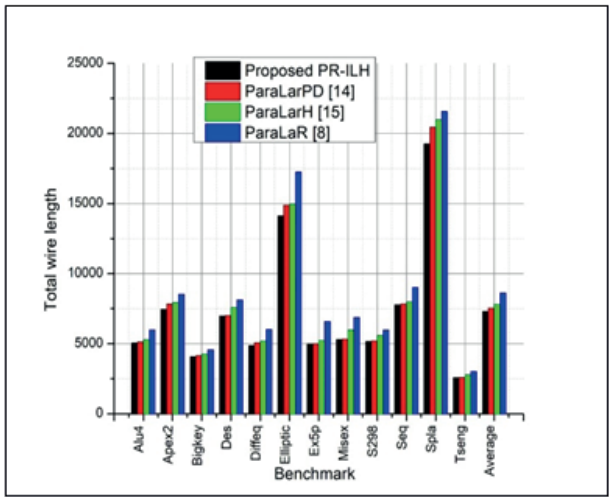

Figure. 3: Comparison of total wire length for the proposed PR-ILH, ParaLarPD [14], ParaLarH [15], and ParaLaR [8].

ParaLarH [15] and ParaLaR [8]. With an average total wire length of 7307.5, the suggested PR-ILH algorithm exhibits comparable performance across most benchmarks. In contrast, the average wire lengths for ParaLarPD [14], ParaLarH [15], and ParaLaR [8] are 7543.83, 7813.42, and 8632.42, respectively. The proposed PR-ILH represents a percentage reduction of approximately 15.4% compared to ParaLaR [8], which has an average total wire length of 8632.42. Additionally, PR-ILH reduces the overall length of the wire by around 3.3% and 6.0% when compared to ParaLarPD [14] and ParaLarH [15], respectively, underscoring its competitive advantage in wire routing optimization. Better

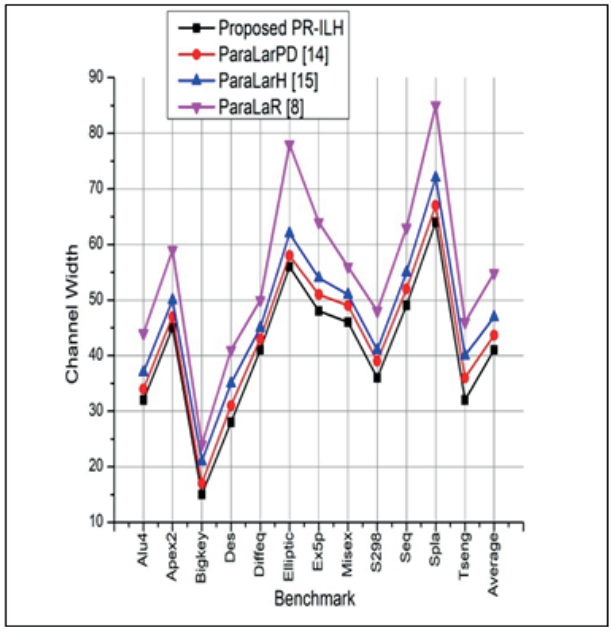

Figure 4: Comparison of Channel Width (CW) for the proposed PR-ILH, ParaLarPD [14], ParaLarH [15], and ParaLaR [8].

GPGA circuit designs with shorter wire lengths, which are essential for maximizing the effectiveness and productivity of FPGA routing, are indicated by lower overall wire lengths. The results reveal that the new PR-ILH algorithm outperforms some of the current ParaLaR-based approaches in this assessment, indicating that it has good potential for decreasing wire lengths. More in-depth study and benchmarking are required to draw firm conclusions on the algorithm's superiority over a wider range of circuits and design scenarios.

Fig. 4 shows the comparison of Channel Width (CW) for the proposed PR-ILH, ParaLarPD [14], ParaLarH [15] and ParaLaR [8]. As it directly affects the functionality and dependability of the circuits, CW is a critical component in the design of FPGA circuits. The suggested PR-ILH method outperforms ParaLarPD [14], ParaLarH [15], and ParaLaR [8], which have mean CW of 43.67, 46.92, and 54.83, respectively. Comparing this to ParaLaR [8], which has a mean CW of 54.83, results in an amazing percentage decrease of almost 25.1%. Additionally, PR-ILH reduces CW by around 6.5% and 12.0% when compared to ParaLarPD [14] and ParaLarH [15], respectively, demonstrating its capacity to create circuit topologies that are smaller and more efficient. It also shows good performance with an average CW of 41. Lower CW suggests more effective use of the area and resources, which is crucial for developing high-performance and compact FPGA routing circuits. The findings imply that the proposed PR-ILH algorithm excels at CW optimization, possibly making it a good contender for sophisticated FPGA circuit design applications.

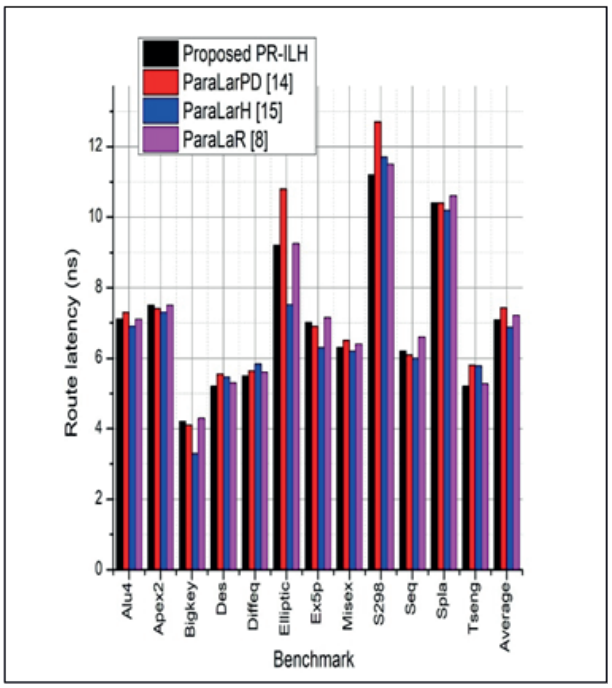

Figure 5: Comparison of route latency (ns) for the proposed PR-ILH, ParaLarPD [14], ParaLarH [15] and ParaLaR [8].

Fig. 5 shows the comparison of route latency (ns) for the proposed PR-ILH, ParaLarPD [14], ParaLarH [15] and ParaLaR [8]. The suggested PR-ILH method outperforms ParaLarPD [14], ParaLarH [15], and ParaLaR [8], which have mean route latencies of 7.433 ns, 6.875 ns, and 7.214 ns, respectively, is notable for its competitive average route latency of 7.085 ns. This shows that the PR-ILH algorithm effectively reduces route latency, improving circuit speed and responsiveness in the process. The lowest average route latency is demonstrated by ParaLarH [15], highlighting its competence in this area of circuit design. However, PR-ILH has the potential to be a dependable and effective method for lowering route latency and improving overall circuit performance because of its consistent performance across a range of evaluations.

6 Conclusion and scope of future work

This work proposed Parallel Routing for FPGA Using Improved Lagrange Heuristics with a Sub-Gradient method and Steiner tree (PR-ILH). Several novel Lagrange heuristics introduced in this study improve the Lagrange relaxation process. By combining the benefits of Lagrange heuristics with sub-gradient optimization, PR-ILH offers more efficient routing while lessening the complexity of parameter tweaking. Steiner trees are used to optimize resource use and overall efficiency further. Comparison of the proposed PR-ILH to ParaLaR (which has an average total wire length of 8632.42), indicates a decrease of about 15.4% in total wire length.

Additionally, compared to ParaLarPD and ParaLarH, PR-ILH shortens the wire's total length by around 3.3% and 6.0%, highlighting its competitive edge in wire routing optimization. Furthermore, PR-ILH decreases CW by around 6.5% and 12.0% when compared to ParaLarPD and ParaLarH, respectively, proving its ability to design circuit topologies that are more compact and effective. The additional effort required to implement the heuristic significantly reduces ParaLarH's parallelization speedups relative to ParaLarPD, which is readily remedied by adding more threads. In the future, we intend to focus on creating algorithms that would eliminate the violation of.constraints. The work can also be intended to adapt the proposed methods to the Internet of Things (IoT) industry, which faces significant design difficulties.

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Arrived: 11. 08. 2023
Accepted: 14. 11. 2023

Original scientific paper
https://doi.org/10.33180/InfMIDEM2023.303

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 53, No. 3(2023), 145 – 166

High -Frequency Tunable Grounded and Floating Incremental-Decremental Meminductor Emulators and its application as AM Modulator

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Abstract: This paper proposes new design for realizing grounded and floating meminductor emulators built with two operational transconductance amplifiers (OTAs) and two second-generation current conveyors. The proposed grounded and floating emulators claim that the circuits are much simpler in design and can be utilized in incremental and decremental topologies. The proposed circuits' performance has been verified with Cadence Virtuoso Spectre using standard CMOS 180nm technology. Furthermore, the layout of the proposed circuits has been designed, and post-layout simulations have been performed. The non-ideal and Monte Carlo analyses have been carried out in detail. This paper also proposes the application of a meminductor as an Amplitude Modulator (AM). Moreover, the experimental results are presented to verify the theoretical and simulation analyses of proposed meminductor emulator circuits.

Keywords: Current-mode circuits, Floating meminductor emulator, Grounded meminductor emulator, Incremental configuration, Decremental configuration, Pinched hysteresis loop

Visokofrekvenčni nastavljivi ozemljeni in plavajoči inkrementalno-dekrementalni meminduktorski emulatorji in njihova uporaba kot AM modulator

Izvleček: V članku je predlagana nova zasnova ozemljenih in plavajočih emulatorjev meminduktorjev, ki so zgrajeni iz dveh operacijskih transkonduktančnih ojačevalnikov (OTA) in dveh tokovnih transporterjev druge generacije. Predlagani ozemljeni in plavajoči emulatorji omogočajo, da so vezja veliko enostavnejša pri načrtovanju in jih je mogoče uporabiti v inkrementalnih in dekrementalnih topologijah. Delovanje predlaganih vezij je bilo preverjeno s programom Cadence Virtuoso Spectre z uporabo standardne CMOS 180 nm tehnologije. Poleg tega je bila zasnovana postavitev predlaganih vezij. Podrobno so bile izvedene neidealne analize in analize Monte Carlo. V članku je predlagana tudi uporaba meminduktorja kot amplitudnega modulatorja (AM). Poleg tega so predstavljeni eksperimentalni rezultati za preverjanje teoretičnih in simulacijskih analiz predlaganih vezij emulatorja meminduktorja.

Ključne besede: tokovna vezja, emulator plavajočega meminduktorja, emulator ozemljenega meminduktorja, inkrementalna konfiguracija, decrementalna konfiguracija, zanka s stisnjeno histerezo

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1 Introduction

Resistor, inductor, and capacitor were three traditional fundamental basic electrical elements; now, the memristor represents the fourth fundamental element. Chua postulated the memristor in 1971 [1] as the fourth basic electrical element. In 1980 this postulation was then generalized to an infinite variety of basic circuit elements [2] and can be generalized into elements quadrangle. It was highlighted only after 2008 when HP fabricated a memristor based on thin-film TiO_2. From then onward, there has been a boom of research in this field.

How to cite:
G. Shukla et al., "High -Frequency Tunable Grounded and Floating Incremental-Decremental Meminductor Emulators and its application as AM Modulator", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 53, No. 3(2023), pp. 145–166

Chua's circuit 4 element diagram was then extended to propose higher-order elements (which require two or more than two capacitors), such as memcapacitors (MCs) and meminductors (MLs). The meminductor provides a relationship between the charge q and the time integral of flux ρ. Unlike capacitors and inductors, meminductors can store information for a long time without power because of their non-volatility. Although the device is still a theoretical concept, some device-level memelements (mostly memristors) have been fabricated [3], and hence emulators are essential to analyze the characteristics and study their applications. The research on solid-state memelements is yet to mature completely, especially for MCs and MLs. Solid-state MCs have not been commercialized, and there has been no information on solid-state MLs. Some models, though directly labeled as "memristors" or "memcapacitors," are essentially practical memrestive emulators [3]. Therefore, a substantial number of circuit implementations have been proposed through the use of emulators. In [4], a relationship on the doubly periodic table of 4 element diagram, also called the four elements torus, is given in correlation with the basic circuit element quadrangle of all four basic electrical elements. Furthermore, an extension of the memristive system to capacitive and inductive elements whose properties depend on the state and history of the system is presented in [5]. Physical characteristics analysis of these memory-based elements and mathematical examples for memristors, meminductors, and memcapacitors are presented in [6, 7].

Several circuits for emulating memristor-less meminductors are proposed in [8-23], while meminductors formed using mutators are proposed in [24-28]. In [8], a memristor-less current and voltage-controlled meminductor emulator are reported using a second-generation current conveyor (CCII), adder, multiplier, and several passive components in the count. A charge-controlled meminductor emulator using an inductor, op-amps, multiplier, transistors, and several other passive components is reported in [9]. In 2014, a practical implementation of the meminductor using many active and passive components was reported [10]. It consists of four current feedback operational amplifiers (CFOAs), one buffer, two op-amps, one multiplier, and some passive components making the circuit quite complex and bulky. A flux-controlled meminductor is reported in [11] but consists of many active blocks and passive components. The meminductor reported in [12] is based on six op-amps and one multiplier, whereas the design in [13] employs three CFOAs, one op-amp, one operational transconductance amplifier (OTA), and one multiplier. The design reported in [14] is based on two voltage differencing transconductance amplifiers (VDTAs) and one multiplier. In 2017, a much simpler circuit for emulating a meminductor was reported using multioutput OTA [15], but it uses an inductor and has a low frequency of operation. All the reported circuits in [8-14] are complex as they employ a multiplier along with an excessive number of active blocks, and [15] has a low frequency of operation, which very much limits the practical use and, further, it realizes only grounded meminductor. The meminductor design in [16] is based on three OTAs and two capacitors. The design reported in [17] is based on two OTAs and one differential voltage current conveyor (DVCC), and the design in [18] is based on one OTA and one VDTA. The topology in [19] reports a meminductor employing two OTAs and one current differencing buffered amplifier (CDBA), whereas [20] is based on two OTAs and one current differencing transconductance amplifier (CDTA). Meminductor design in [21] employs two CCIIs and one OTA, whereas design [22] is based on two VDTAs. Moreover, [23] reports a design based on one modified voltage differencing current conveyor (MVDCC) and one OTA. However, all the designs reported in [8-12, 15-18, 20-23] realize only one type of meminductance emulator, i.e., the grounded or floating meminductor; only [19] realizes both grounded and floating meminductance emulator. Furthermore, the designs reported in [21-23] realize only one type of meminductance emulator and possess a low frequency of operation. Moreover, [22, 23] realize only the incremental type of configuration.

Another method of emulating meminductors is with mutators proposed in [24-28]. Mutators simulating second-order elements using their inherent relationship are reported in [24, 25] and represent the simplified meminductor emulator using the multiplier approach, but the memristor used here is bulky, complex, and has a low operating frequency. A mutator based on one CCII and three op-amps is reported in [26]. A universal mutator using many active and passive components is also available in [27]. Moreover, a mutator circuit based on two current buffered transconductance amplifiers (CBTAs) and one multiplier is reported in [28]. Apart from these mutators, the PSpice model of meminductor and its nonlinear model with its study on device parameter variations are available in [29, 30]. A detailed composite behavior in series and parallel meminductor topologies is reported in [31]. The applications of meminductors in chaotic oscillators and their dynamic studies are reported in [32-34], whereas application as a low-power filter design is available in [35].

This paper proposes two meminductor emulators, one grounded and other one floating, built with active blocks consisting of two OTAs and two-second generation current conveyors. The proposed meminductor emulators possess the following important features: (i) simple circuitry with no multipliers, (ii) option for both

incremental and decremental configurations to increase the range of values of meminductance (the value of meminductance can be increased and decreased from its base value in incremental and decremental types of topology respectively), and also application flexibility, (iii) high-frequency range of operation, (iv) electronic control of meminductance value in addition to the control by frequency and amplitude of the applied voltage signal across the emulator.

2 Employed analog building blocks and general meminductor model

Employed analog building blocks in proposed meminductor emulator circuits and a generalized model of a meminductive system are illustrated in this section.

2.1 Operational transconductance amplifier (OTA), second generation current conveyor (CCII) and cecond-generation current controlled current conveyor (CCCII)

OTA, CCII, and CCCII circuit symbols are shown in Figure. 1(a)-(c). CMOS implementation of OTA, CCII and CCCII are presented in Figure. 1(d), 1(e) and 1(f) respectively. V_B controls the OTA's transconductance gain (G_m), while I_b controls the internal resistance R_X of CCCII, making the circuits electronically tunable.

The port relationships of OTA are expressed as:

$I_{o\pm} = \pm G_m V_{in}$, $V_{in+} - V_{in-}$ = differential input = V_{in}

Where G_m is the transconductance of OTA. The routine analysis results in the following expression for G_m:

$$G_m = \frac{k}{\sqrt{2}}\left(V_B - V_{ss} - 2V_{th}\right), \quad (1)$$

Here, k is a parameter of the MOS device given by:

$$k = \mu_n C_{ox} \frac{W}{L}$$

The W, L, μ_n, C_{ox}, and V_{th} are, respectively, channel width, length, the mobility of the carrier, capacitance per unit area, and the threshold voltage of MOS.
The port relationship CCII± is given by:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

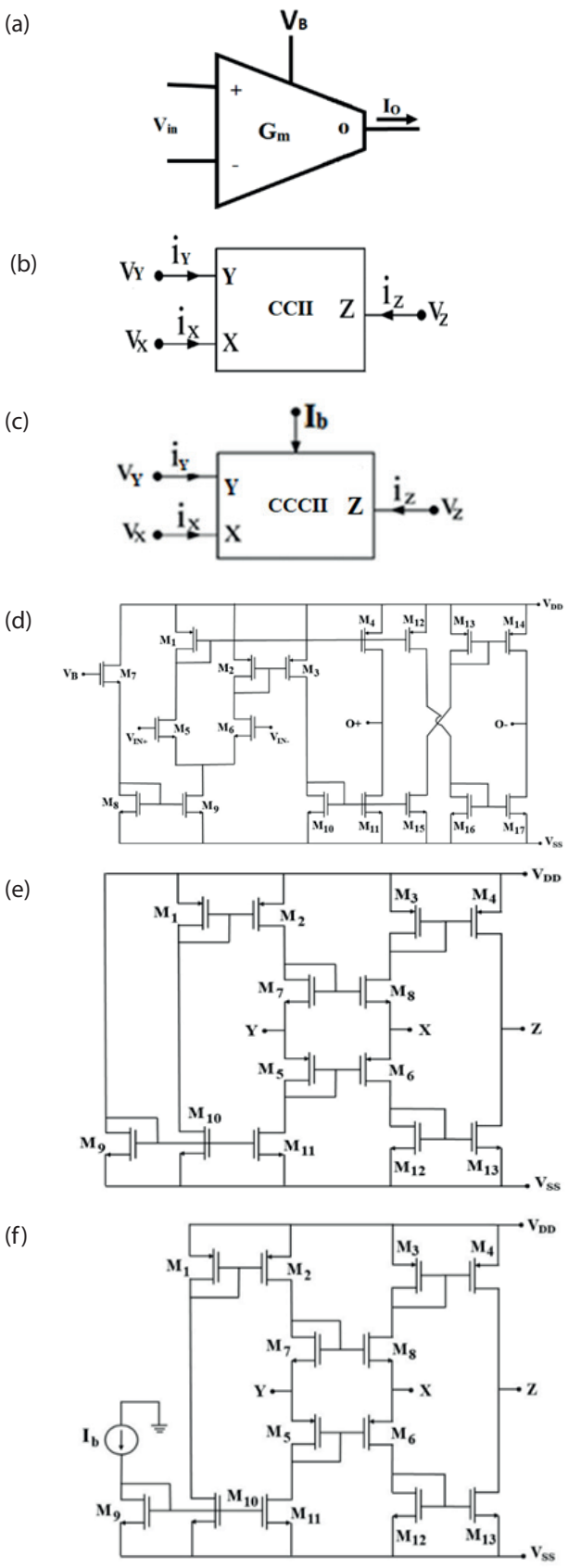


Figure 1: Symbolic representations of (a) OTA, (b) CCII, (c) CCCII; CMOS implementations of; (d) OTA, (e) CCII, (f) CCCII.

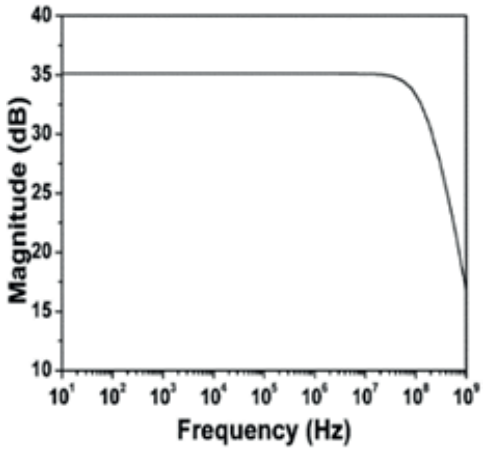
Similarly, port relationship CCCII± is given by:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & \mathrm{R}_X & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

where, $R_X = \dfrac{1}{\sqrt{2I_b C_{ox}}\left(\sqrt{\dfrac{\mu_p W_p}{L_p}} + \sqrt{\dfrac{\mu_n W_n}{L_n}}\right)}$

Figure. 2(a-b) shows the OTA, CCII, and CCCII frequency responses. They result in a bandwidth of 80 MHz for OTA and 1 GHz and 800 MHz for CCII and CCCII, respectively.

(a)



(b)

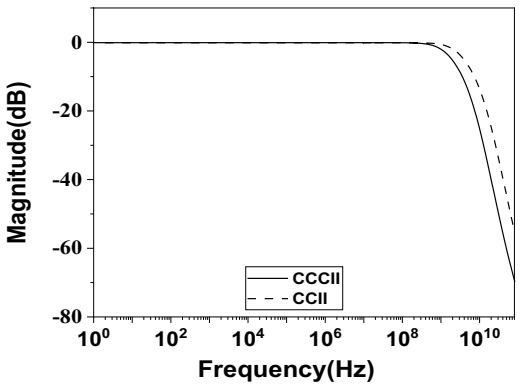


Figure 2: Frequency response of (a) OTA, (b) CCII and CCCII.

2.2 Basic model of a meminductor emulator

Symbolic representation of meminductor is shown in Figure. 3. Meminductor is a mem-element with three constitutive variables as; ϕ(t), ρ(t), and I(t), where ϕ(t) is the flux, which is defined as the integral of input voltage i.e.

$$\Phi(\mathrm{t}) = \int \mathrm{V}_{\mathrm{in}}(\mathrm{t})\,\mathrm{dt} \qquad 2(a)$$

Figure 3: Symbolic representation of meminductor.

ρ(t) is the integral of ϕ(t), i.e.

$$\rho(\mathrm{t}) = \int \Phi(\mathrm{t})\,\mathrm{dt} \qquad 2(b)$$

The relation between input current I(t) and ϕ(t) of meminductor is defined as;

$$\frac{I(t)}{\phi(t)} = L_M{}^{-1} \qquad 3(a)$$

$L_M{}^{-1}$ is inverse meminductance and the general representation of flux controlled meminductor having an initial value of inverse meminductance given by 'm' and decremental or incremental product term given by n is expressed as [14, 18];

$$\frac{I(t)}{\phi(t)} = m \pm n\rho(\mathrm{t}) \qquad 3(b)$$

or, $I(t) = \left(m \pm n\rho(\mathrm{t})\right)\phi(\mathrm{t})$

It can be inferred from (3b) that a meminductor model contains 'm' as a fixed term and nρ(t) as a time varying term.

3 Proposed grounded and floating meminductor emulator circuit

Schematic diagrams of the proposed grounded and floating meminductor emulators are shown in Fig. 4 and Figure. 5, respectively. The Incremental and decremental nature of the meminductor can be configured by a switching mechanism between pins M, N, O, and P of circuits as given in Table 1. These mechanisms apply to both grounded and floating meminductor emulators.

Table 1: Connection topology for pins M, N, O, and P for two modes of operations.

S. No.	Switch Connections	Mode of operation
1	M-N; O-P	Incremental
2	M-P; O-N	Decremental

3.1 Grounded meminductor emulator

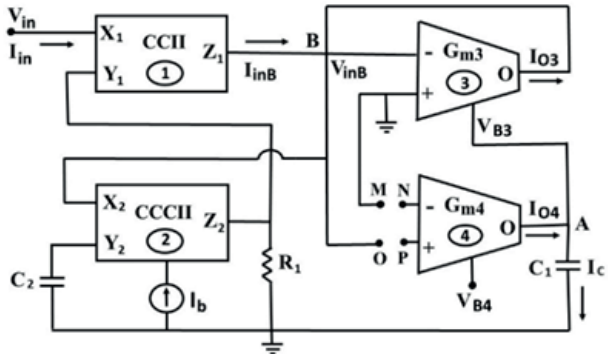


Figure 4: Schematic diagram of grounded meminductor emulator.

The proposed grounded meminductor emulator is shown in Figure. 4. Considering the incremental type of meminductor emulator, i.e., pins M, N and O, P are interconnected, the input current I_{in} is obtained as:

$I_{in}(t) = I_{X1} = I_{Z1}$ (using port relationship of CCII)

Again, $I_{in}(t) = -I_{inB}$ (4a)

Similarly, $V_{Y2} = V_{X2} - I_{X2}R_{X2}$,

(by the port relationship of CCCII)

$$V_{Y2} = V_{inB} = -\frac{I_{X2}}{sC_2} - I_{X2}R_{X2} = -I_{X2}\left(\frac{1}{sC_2} + R_{X2}\right) \quad (4b)$$

Again, $I_{X2} = I_{Z2} = \frac{-V_{Y1}}{R_1} = \frac{-V_{in}}{R_1}$ (4c)

Since ($V_{Y1} = V_{X1} = V_{in}$)

Substituting (4c) in (4b)

$$V_{in} = V_{inB}\left(\frac{sR_1C_2}{1+sC_2R_{X2}}\right) \quad (5)$$

Dividing (5) by (4a)

$$\frac{V_{in}}{I_{in}} = -\frac{V_{inB}}{I_{inB}}\frac{sR_1C_2}{1+sC_2R_{X2}} \quad (6)$$

Bias voltage V_{B3} is given by

$$\begin{aligned} V_{B3} &= \frac{1}{C_1}\int I_C(t)\,dt = \frac{G_{m4}}{C_1}\int V_{inB}(t)\,dt = \\ &= \frac{G_{m4}}{C_1}\left(\frac{1+sC_2R_{X2}}{SR_1C_2}\right)\int V_{in}(t)\,dt = \\ &= \frac{G_{m4}}{C_1}\left(\frac{1+sC_2R_{X2}}{sR_1C_2}\right)\phi_{in} \end{aligned} \quad (7)$$

Where ϕ_{in} is the total flux obtained by the meminductor, and it is expressed as

$$\varphi_{in} = \int V_{in}(t)\,dt = \frac{V_{in}}{s} \quad (8)$$

Substituting (7) into (1), the transconductance G_{m3} is obtained as

$$\begin{aligned} G_{m3} &= \frac{k}{\sqrt{2}}\left(V_{B3} - V_{ss} - 2V_{th}\right) = \\ &= \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\left(1+sC_2R_{X2}\right)\phi_{in}}{sC_1R_1C_2} - V_{ss} - 2V_{th}\right) \end{aligned} \quad (9)$$

Also, $G_{m3} = \frac{-I_{O3}}{V_{inB}} = \frac{I_{inB}}{V_{inB}}$ (10)

Using (10) and (9) results in an expression

$$\frac{I_{inB}}{V_{inB}} = \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\left(1+sC_2R_{X2}\right)\phi_{in}}{sC_1R_1C_2} - V_{ss} - 2V_{th}\right) \quad (11)$$

On substituting (11) in (6) and by incorporating the relation of (8), meminductance (L_M) of the proposed grounded incremental meminductor emulator is obtained as

$$L_M = \frac{\phi_{in}}{I_{in}} = \frac{R_1C_2}{\frac{k}{\sqrt{2}}\left(V_{ss}+2V_{th}\right) - \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\left(1+sC_2R_{X2}\right)\phi_{in}}{sC_1R_1C_2}\right)}\frac{1}{1+sC_2R_{X2}} \quad (12)$$

Similarly, the switching connections to M-P and O-N changes the polarity of the time-variant part of the meminductance of (12), resulting in a decremental type meminductance as

$$L_M = \frac{R_1C_2}{\frac{k}{\sqrt{2}}\left(V_{ss}+2V_{th}\right) + \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\left(1+sC_2R_{X2}\right)\phi_{in}}{sC_1R_1C_2}\right)}\frac{1}{1+sC_2R_{X2}} \quad (13)$$

Equations (12) and (13) can be combined and rewritten as

$$L_M = \frac{R_1 C_2}{\frac{k}{\sqrt{2}}\left(V_{ss}+2V_{th}\right) \mp \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\left(1+sC_2R_{X2}\right)\phi_{in}}{sC_1R_1C_2}\right)} \frac{1}{1+sC_2R_{X2}} \quad (14)$$

If the operating frequency is much lower than $\frac{1}{2\pi C_2 R_{X2}}$ where R_{X2} is the resistance at input port X of CCCII and is usually kept low [40], then we can write $\left(1+sC_2R_{X2}\right) \approx 1$.

Hence, equation (14) can then be simplified in terms of the inverse of L_M as:

$$L_M^{-1} = \frac{\phi_{in}}{I_{in}} \approx \frac{k}{\sqrt{2}R_1C_2}\left(V_{ss}+2V_{th}\right) \pm \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1R_1^2C_2^2}\right) \quad (15)$$

In equation (15), G_{m4} can be controllable by external bias voltage V_{B4}, which makes the proposed circuit electronically tunable. Equation (15) represents incremental and decremental meminductance, where for a fixed operating frequency $\frac{k}{\sqrt{2}R_1C_2}\left(V_{ss}+2V_{th}\right)$ is the constant term and $\frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1R_1^2C_2^2}\right)$ is the time-varying term as φ_{in} is the function of the time-varying input signal. For $\varphi_{in} = 0$ meminductance attains a constant value in both topologies (incremental and decremental), where for the operator ±, the + is for decremental and – is for incremental configuration.

3.2 Floating meminductor emulator

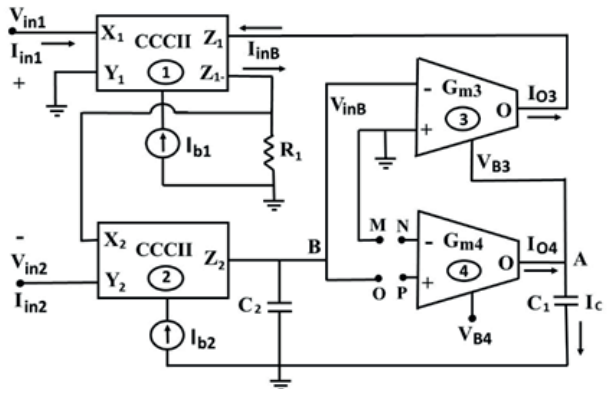


Figure 5: Schematic diagram of floating meminductor emulator.

The floating meminductor emulator is shown in Figure. 5. Considering incremental type meminductor emulators, i.e., pins M, N, and pins O, P are interconnected. The currents from the port relationship are obtained as follows;

$$I_{in1} = I_{in} = I_{X1} = I_{Z1} = -I_{Z1-} \quad (16)$$

And $V_{in1} = V_{X1} = V_{Y1} + I_{X1}R_{X1}$ (17)

Hence, $V_{in1} = I_{in}R_{X1}$ [As V_{in1}=0] (18)

Again, $V_{Z1-} = V_{Y2} = I_{Z1-}R = \frac{V_{in1}}{R_{X1}}R$ (19)

For $R = R_{X1}$, we get from (19),

$$V_{Y2} = V_{in1} \quad (20)$$

Further,

$V_{in2} = V_{X2} = V_{Y2} + I_{X2}R_{X2}$ [from port relation] (21)

Hence from (20) and (21),

$$V_{in2} = V_{in1} + I_{X2}R_{X2} \quad (22)$$

As at node B, $I_{X2} = I_{Z2} = -sC_2V_{inB}$ (23)

Hence from (22),

$$V_{in2} = V_{in1} - sC_2V_{inB}R_{X2} \quad (24)$$

Or, $V_{in1} - V_{in2} = V_{in} = sC_2V_{inB}R_{X2}$ (25)

From (25), $V_{in} = sR_{X2}C_2V_{inB}$

0r, $V_{inB} = V_B = \left(\frac{V_{in}}{sR_{X2}C_2}\right)$ (26)

Also $I_{in} = I_{O3}$ (27)

Dividing (26) by (27), we get;

$$\frac{V_{in}}{I_{in}} = \frac{V_{inB}}{I_{O3}}sR_{X2}C_2 \quad (28)$$

Further, bias voltage V_{B3} using (26) results in;

$$V_{B3} = \frac{1}{C_1}\int I_C(t)\,dt = \frac{G_{m4}}{C_1}\int V_{inB}(t)\,dt = \\ = \frac{G_{m4}}{C_1}\left(\frac{1}{sR_{X2}C_2}\right)\int V_{in}(t)dt = \frac{G_{m4}}{C_1}\left(\frac{1}{sR_{X2}C_2}\right)\phi_{in} \quad (29)$$

Substituting (29) into (1), transconductance G_{m3} is obtained as;

$$G_{m3} = \frac{k}{\sqrt{2}}\left(V_{B3} - V_{ss} - 2V_{th}\right) = \\ = \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1R_{X2}C_2} - V_{ss} - 2V_{th}\right) \quad (30)$$

Further from Fig. 5, $G_{m3} = -\frac{I_{O3}}{V_{inB}}$

So (30) becomes:

$$\frac{I_{O3}}{V_{inB}} = -\frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1R_{X2}C_2} - V_{ss} - 2V_{th}\right) = \\ = \frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th} - \frac{G_{m4}\phi_{in}}{sC_1R_{X2}C_2}\right) \quad (31)$$

Substituting (31) in (28) gives,

$$\frac{V_{in}}{I_{in}} = \frac{sR_{X2}C_2}{\frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) - \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1R_{X2}C_2}\right)}$$

Hence, the meminductance of the proposed grounded incremental meminductor emulator is obtained;

$$L_M = \frac{R_{X2}C_2}{\frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) - \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1R_{X2}C_2}\right)} \quad (32)$$

Similarly, the change of switch connections to M-P and O-N changes the polarity of the time-variant part of meminductance of (24), resulting in a decremental type meminductance;

$$L_M = \frac{R_{X2}C_2}{\frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) + \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1R_{X2}C_2}\right)} \quad (33)$$

So, equations (32) and (33) can be combined and rewritten as;

$$L_M = \frac{\phi_{in}}{I_{in}} = \frac{R_{X2}C_2}{\frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) \pm \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1R_{X2}C_2}\right)}$$

$$L_M^{-1} = \frac{I_{in}}{\phi_{in}} = \quad (34)$$

$$\frac{k}{\sqrt{2}R_{X2}C_2}\left(V_{ss} + 2V_{th}\right) \pm \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1R_{X2}^{\,2}C_2^{\,2}}\right)$$

In equation (34), G_{m4} can be controllable by external bias voltage $V_{B4,}$ and R_{X2} is controlled by external current $I_{b2,}$ which makes the proposed circuit electronically tunable. In the inverse of the meminductance equation, the term $\frac{k}{\sqrt{2}R_{X2}C_2}\left(V_{ss} + 2V_{th}\right)$ is constant, and $\frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{SC_1R_{X2}^{\,2}C_2^{\,2}}\right)$ is the time-varying term as φ_{in} is the function of the time-varying input signal. For φ_{in} = 0, meminductance attains a constant value in both the topologies (incremental and decremental), where for the operator ±, the + is for decremental and – is for incremental configuration.

4 Comparison of meminductor emulators

A comparison of available meminductor emulators is given in Table 2. It is observed that most emulators use many analog building blocks for implementation and have frequency limitations. The emulator designs reported in [8-12, 26, 27] use many active building blocks and a large number of passive components and do not possess electronic tunability. Only the configurations [13, 14, 19] possess both grounded and floating types of meminductors, hence finding flexibility in applications. Moreover, the topologies [8-12, 15-18, 21, 25-27] are only grounded type, and [20, 23, 23, 28] are floating type of meminductors. Further, all these designs [8-14, 26-28] employ a multiplier in the configuration, which is undesirable as it increases circuit complexity. The design in [15] uses a floating inductor in the configuration, resulting only in grounded types of meminductor. Furthermore, the designs [8-13, 15, 21-26] exhibit low frequency of operation (few Hz to few kHz range). Meminductors [8-13, 22, 23, 28] can be operated only in incremental configuration.

The proposed work presents both grounded and floating types of meminductor realizations using simple basic blocks, two CCII/CCCII, and two OTAs with only two capacitors and one resistor. All the passive ele-

ments in both of the proposed meminductor circuits are grounded. Moreover, both the incremental and decremental properties are present in the proposed emulators. Further, the proposed grounded and floating meminductors are valid for frequencies of 1 MHz and 10 MHz, respectively. An important feature of the proposed meminductor emulator is its ability to control the meminductance value by controlling the

Table 2: Comparison of meminductor emulators.

Ref.	Number in count and type(s) of active building blocks used	Tech. used	Passive element (C/R/L)	All grounded passive elements	M /NM based	G/ F meminductor	Electronic tunability	Max. operating frequency shown	Inc/Dec or both	P. C (W)
[8]	3 CCII, 1 Multiplier, 1 Adder	CMOS	2/3/0	Yes	NM	G	No	20 Hz	Inc	NA
[9]	2 Op-Amp, 2 Current Mirrors, 1 Buffer, 1 Multiplier	CMOS	2/2/1	No	NM	G	No	300 Hz	Inc	NA
[10]	4 CFOAs, 1 Buffer, 2 Op-Amp, 1 Multiplier	CMOS	2/6/0	No	NM	G	No	36.9 Hz	Inc	NA
[11]	5 Op-Amp, 1 Multiplier	CMOS	2/10	No	NM	G	No	70 Hz	Inc	NA
[12]	6 Op-Amps, 1 Multiplier	BJT	2/13/0	No	NM	G	No	300 Hz	Inc	NA
[13]	1 OTA, 3 CFOA, 1 Op-Amp, 1 Multiplier	BJT	2/8/0	No	NM	Both (G+F)	Yes	5 kHz for both	Inc	NA
[14]	2 VDTAs, 1 Multiplier	CMOS	2/0/0	Yes	NM	Both (G+F)	Yes	1 MHz for both	Both	200 µ
[15]	1 MO-OTA	CMOS	1/1/1	No	NM	G	Yes	500 Hz	Both	120 µ
[16]	3 OTAs	CMOS	2/0/0	Yes	NM	G	Yes	10 MHz	Both	NA
[17]	2 OTAs,1 DVCC	CMOS	2/1/0	Yes	NM	G	Yes	10 MHz	Both	NA
[18]	1 OTA, 1 VDTA	CMOS	2/0/0	Yes	NM	G	Yes	3 MHz	Both	NA
[19]	2 OTAs, 1 CDBA	CMOS	2/0/0	Yes	NM	Both (G+F)	Yes	2 MHz for both	Both	NA
[20]	2 OTAs, 1 CDTA	CMOS	2/0/0	Yes	NM	F	Yes	1 MHz	Both	NA
[21]	2 CCIIs, 1 OTA	CMOS	2/2/0	Yes	NM	G	Yes	700 kHz	Both	14.3m
[22]	2 VDTAs	CMOS	2/0/0	Yes	NM	F	Yes	700 kHz	Inc	NA
[23]	1 MVDCC, 1OTA	CMOS	2/1/0	Yes	NM	F	Yes	300 kHz	Inc	NA
[25]	1 Microcontroller, 1 ADC, 1 Op Amp	CMOS	1/3/0	No	M	G	No	8 Hz	Both	NA
[26]	1 CCII, 6 Op-Amp, 1 Multiplier	CMOS	2/10/0	No	M	G	No	200 Hz	Both	NA
[27]	7 TOAs, 1 Op-Amp, 1 Multiplier, 3 Buffers	CMOS	2/11/0	No	M	G	No	21.1 Hz	Both	NA
[28]	2 CBTAs, 1 Multiplier	CMOS	2/2/0	No	M	F	Yes	1 MHz	Inc	NA
Our Work	2 OTAs, 1 CCCII, 1 CCII	CMOS	2/1/0	Yes	NM	G	Yes	1 MHz	Both	1.01 m
	2 OTAs, 2 CCCIIs	CMOS	2/1/0	Yes	NM	F	Yes	10 MHz	Both	1.03 m

Note: M: Mutator; NM: Non-mutator; G: grounded; F: Floating; Inc: Incremental; Dec: Decremental; P.C: Power consumption.

transconductance, G_{m4} with the bias voltage, $V_{B4;}$ hence both the emulator circuits are electronically tunable. Power consumption of the proposed circuits is greater than that of [14, 15], however smaller than that of [21] among the available literature.

5 Simulation results and discussion

This section deals with verifying the hysteresis loop between flux and the current, one of the fingerprints of the meminductor. Various simulations with 180 nm CMOS technology have been performed to verify the meminductive nature of proposed emulator circuits. Supply voltages of +1.2V and -1.2 V are used for V_{DD} and $V_{SS,}$ respectively, for grounded and floating meminductors. The aspect ratios of MOS transistors are given in Table 3, and they operate in the saturation region.

5.1 Grounded meminductor simulation result

The grounded meminductor emulator in Figure. 4 is simulated for different frequencies. The results for the pinched hysteresis loop obtained for a sinusoidal signal of amplitude (A_m=140 mV) with frequencies of 100 kHz, 200 kHz, 300 kHz, 400 kHz, and 500 kHz are shown in Figure. 6. Here, the product of the capacitor (C_2) value and frequency (f) is kept constant (75 x 10^{-6} FaradHz) and V_{B4}=450 mV. On increasing the frequency, the pinched hysteresis loop area of Φ-I curves decreases, which satisfies (14), suggesting that the time-varying nature of the loop decreases and ultimately vanishes at a specific frequency. Figure. 7 shows the relationship between charge q(t) and ρ(t), where $\rho(t) = \int \varphi(t)dt$ and $q(t) = \int i(t)dt$. Additionally, the current, $i(t)$ flowing in a meminductor can be expressed as per [6]. The single valued function q(ρ) has been illustrated in detail in [6]. This can also be verified graphically from Figure. 7 as a single valued curve is obtained, implicitly implying that the corresponding device is a meminductor.

Table 3: Design Parameters for analog blocks in grounded meminductor

OTA

MOS Transistors	W(μm)	L(μm)
M_{1-4}	12	0.375
M_{10}	12	0.510
M_{5-9}, M_{11}	12	0.500

CCII/CCCII

MOS Transistors	W(μm)	L(nm)
M_1, M_{3-13}	12	0.500
M_2	2	0.200

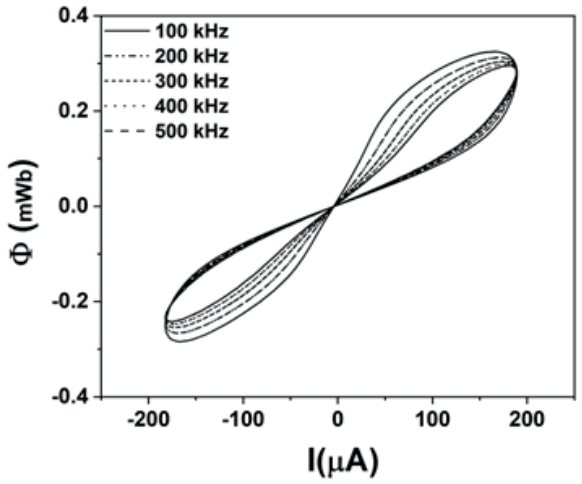


Figure 6: Φ-I characteristic for grounded meminductor circuit at different operating frequencies for A_m = 140 mV, I_b=20 μA, V_{B4}= 0.45 V, C_1= 150 pF, R=10 Ω and constant C_2f =75 x 10^{-6} FaradHz.

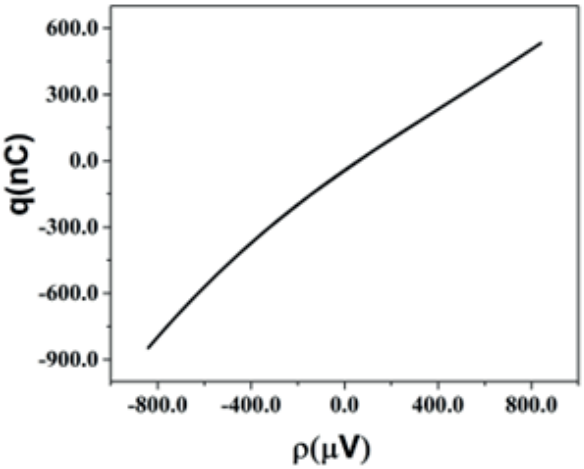


Figure 7: Locus of q(t) and ρ(t) for grounded meminductor.

5.2 Floating meminductor simulation result

The floating emulator's simulation results for the pinched hysteresis loop obtained for frequencies of 1 MHz, 2 MHz, 4 MHz, 6 MHz, and 8 MHz are shown in Figure. 8. Here, the product of capacitor(C_2) value and frequency (f) is kept constant (75 x 10^{-6} FaradHz) with A_m=200 mV, V_{B4}=500 mV. On increasing the frequency, the pinched hysteresis loop area of Φ-I curves decreases; this validates the meminductive behavior of emulators as obtained in (34). Fig. 9 shows the relationship between charge q(t) and integral of flux, ρ(t). It shows that q(t) is a single-valued function of ρ(t). Therefore, the device current goes through a meminductor. On increasing the frequency, the pinched hysteresis loop area of Φ-I curves decreases, which satisfies (14), suggesting that the time-varying nature of the loop de-

creases and ultimately vanishes at a specific frequency. Figure 9 shows the relationship between charge q(t) and ρ(t). As discussed earlier for Figure 7, the curve in Figure 9 is also a single valued. Therefore, the device current flows through a meminductor.

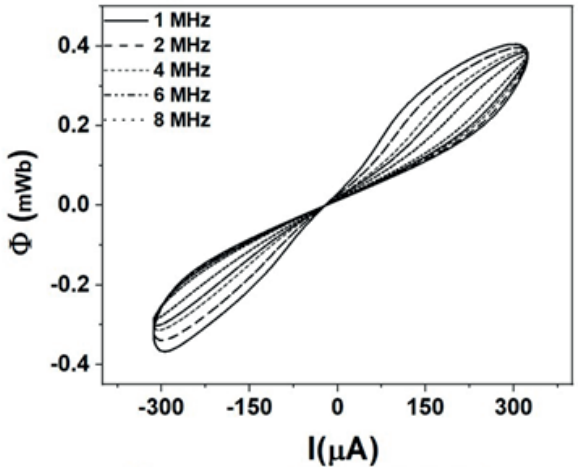


Figure 8: Φ-I characteristic for floating meminductor circuit at different operating frequencies for A_m = 200 mV, I_{b2}=20 μA, V_{B4}= 0.5 V, C_1= 150pF, R=5 Ω and constant C_2f =75 x 10^{-6} FaradHz.

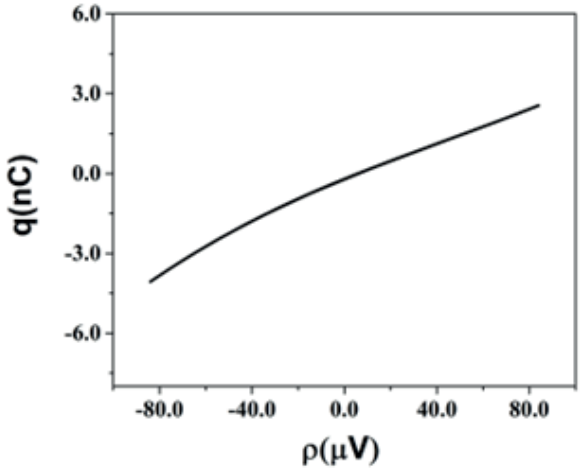
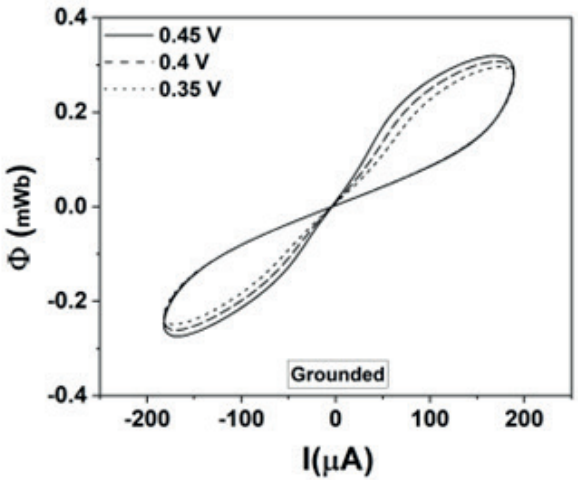


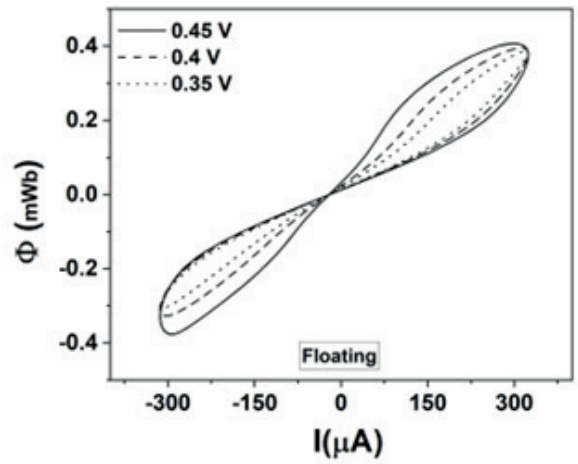
Figure 9: Locus of q(t) and ρ(t) for floating meminductor.

5.3 Effect of variation of bias voltage (VB4) of OTA on the pinched hysteresis loop

It is seen in (15) and (34) that the meminductance of emulators depends on transconductance $G_{m4,}$ which is electronically tunable by the external bias voltage, $V_{B4,}$. Figure. 10(a) shows the grounded meminductor's simulation results for signal frequency of 500 kHz, capacitor value C_1=C_2=150 pF, I_b=20μA, and A_m=140 mV at different values of V_{B4} (0.45 V, 0.4 V, and 0.35 V). Similarly, Figure. 10(b) shows the floating meminductor's simulation results for signal frequency of 500 kHz, capacitor value of C_1=375 pF, C_2 =150 pF, I_{b1} =-48 μA, I_{b2} =-20 μA and A_m=140 mV at different values of V_{B4} (0.45V, 0.4V, and 0.35V). It is observed that the pinched hysteresis loop of Φ-I curves area increases with the increase of V_{B4} as expected as per position of G_{m4} in (15) and (34). It implies that the meminductance can be controlled by $V_{B4.}$



(a) Grounded

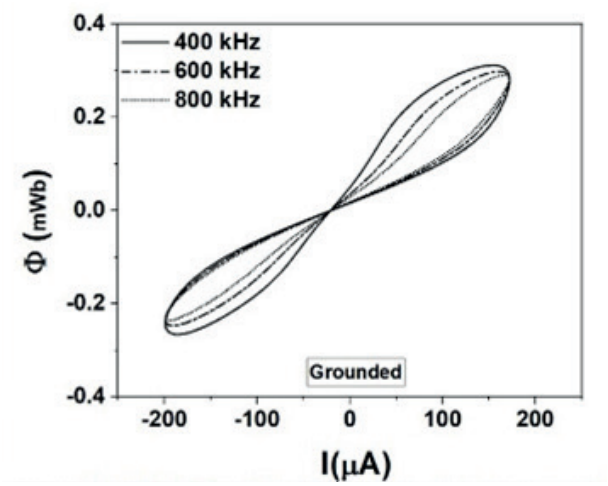


(b) Floating

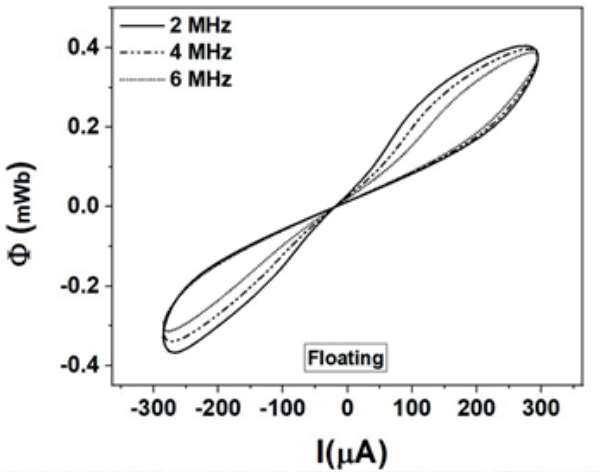
Figure 10: Φ-I characteristic curves obtained with sinusoidal current signal with 500 kHz, A_m=140 mV, C_2=150 pF for (a) grounded meminductor circuit with C_1=150 pF, I_b=20 μA, and different V_{B4}, (b) floating meminductor circuit with C_1=375 pF, I_{b2}=20 μA, and different V_{B4}.

5.4 Effect of varying frequency and capacitances on the pinched hysteresis loop

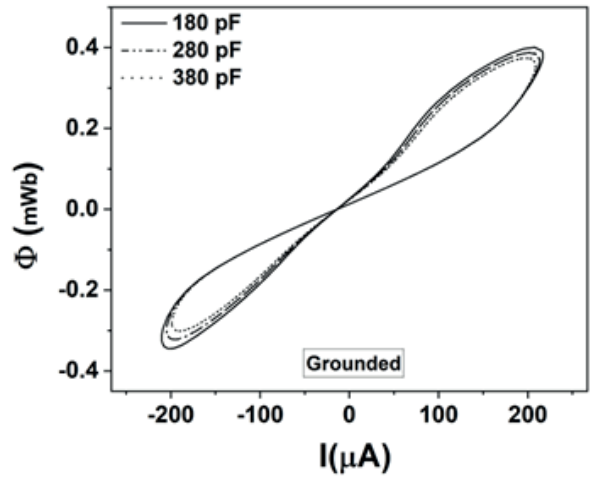
The effect on Φ-I characteristics for variation of applied signal frequency for a fixed capacitance for both grounded and floating meminductor emulators are shown in Figures. 11(a) and 11(b), respectively. Figure. 11(a) shows that as frequency increases from 400 kHz – 800 kHz for a fixed capacitance value, the hysteresis



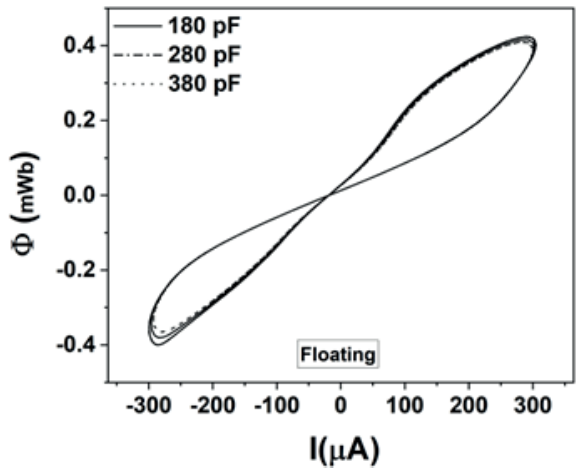
(a) Grounded



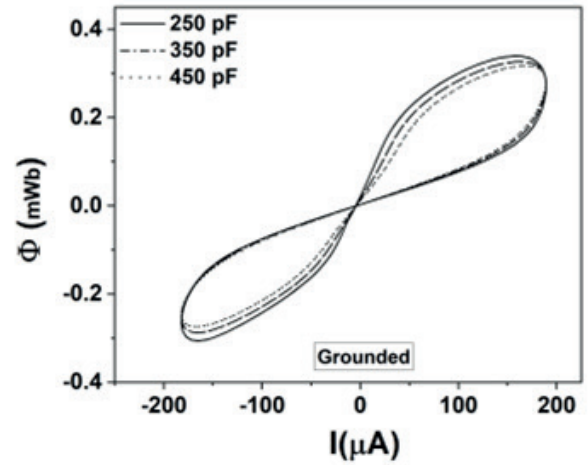
(b) Floating



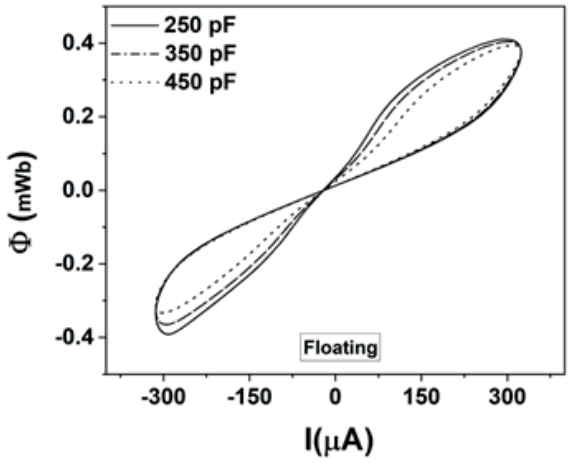
(c) Grounded



(d) Floating



(e) Grounded



(f) Floating

Figure 11: Φ-I characteristic curves for a sinusoidal current signal of A_m=140 mV and V_{B4}=500mV for (a) grounded meminductor for the variable frequency with C_1=180 pF, C_2=150pF, I_b=20 μA, (b) floating meminductor for the variable frequency at C_1=375 pF, C_2=150pF, I_{b2}=20 μA, (c) grounded meminductor for variable C_2 at 500 kHz (d) floating meminductor for variable C_2 at 800 kHz frequency, (e) grounded meminductor for variable C_1 at 500 kHz frequency, (f) floating meminductor for variable C_1 at 800 kHz frequency.

loop becomes more and more linear, which satisfies (15), suggesting the time-varying nature of the loop decreases. Figure. 11(b) shows that as the frequency increases from 800k Hz – 4 MHz for a fixed capacitance value, the area under the hysteresis loop gradually decreases as predicted by (34). Similar to the effect of frequency variation, area of hysteresis loop of meminductance changes for the variation in capacitances (C_1 and C_2) and this can also be verified by observing these parameters in (15) and (34). On varying C_1 and C_2 with a fixed frequency of 500 kHz for grounded topology and 800 kHz for floating topology, the results are obtained as shown in Figure. 11(c-f).

6 Layout, post-layout simulations, and Monte Carlo analysis

Layouts are obtained, and post-layout simulations are carried out for both grounded and floating topologies to check the effect of parasitics on the hysteresis. Further, the simulation results of the Monte Carlo analysis of proposed emulator circuits are also presented.

6.1 Pre and post-layout results for grounded and floating meminductor emulators

Layouts of grounded and floating meminductor emulators are shown in Figure. 12. Layout areas occupied by grounded and floating meminductor emulators are 1845 μm² and 1874 μm², respectively. Figure. 13(a, b) shows the Φ-I characteristic curves for grounded me-

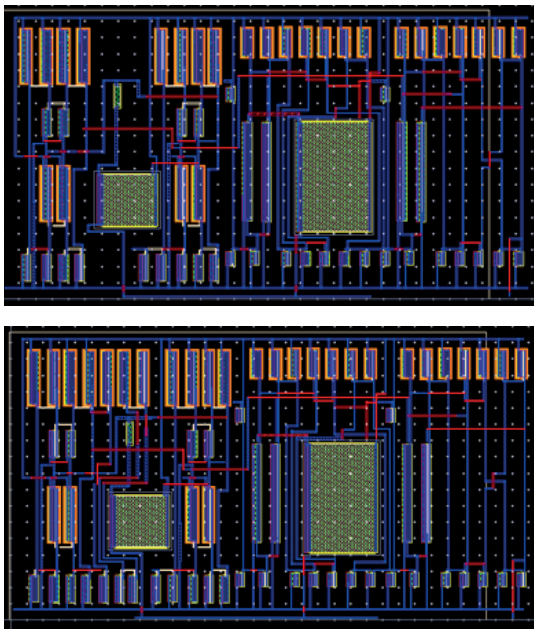


Figure 12: Layout of meminductor emulators (a) grounded (b) floating.

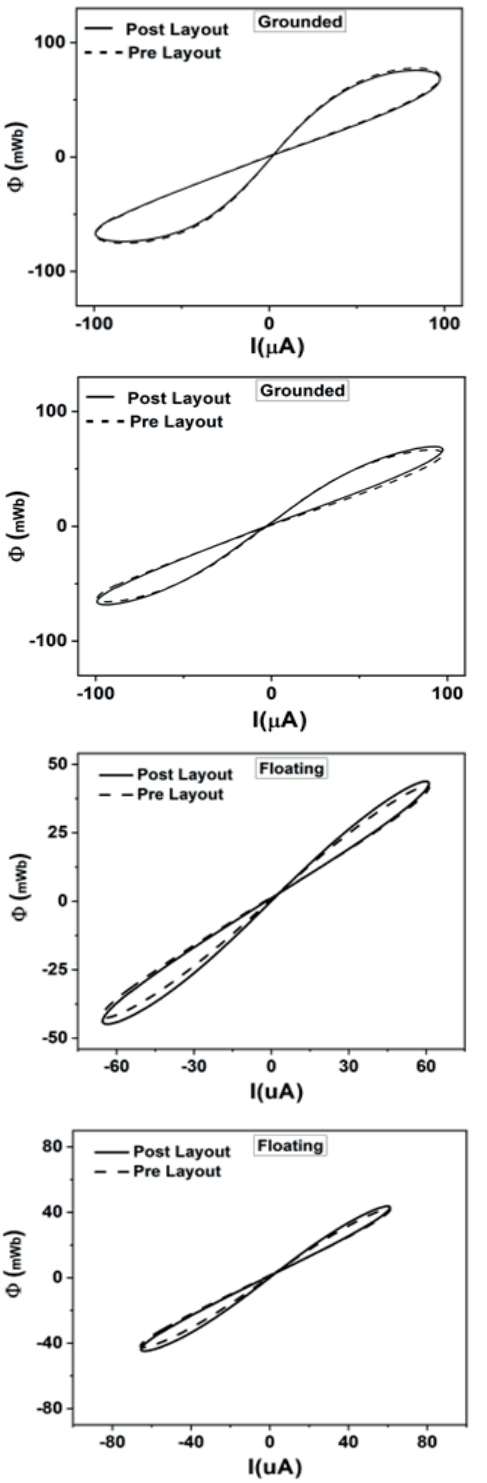


Figure 13: Pre and Post layout simulation results of Φ-I characteristic plot for (a) grounded meminductor emulator at 500 kHz for V_{B4} = 450 mV, A_m= 140 mV, C_1=48 pF, C_2= 80 pF and I_b=20 μA, (b) grounded meminductor emulator at 1 MHz for V_{B4} = 450 mV, A_m= 140 mV, C_1= 8 pF, C_2=13 pF and I_b=20 μA, (c) floating meminductor emulator at 100 kHz for V_{B4} = 500 mV, A_m= 200 mV, C_1=75 pF, C_2=150 pF and I_{b2}=18 μA, (d) floating meminductor emulator at 1 MHz for V_{B4} = 500 mV, A_m= 200 mV, C_1=18 pF, C_2=28 pF, and I_{b2}=18 μA.

minductor emulators at 500 kHz and 1 MHz, respectively. Similarly, Figure. 13(c, d) shows the Φ-I characteristic curves for floating meminductor emulators at 100 kHz and 1 MHz operating frequencies, respectively. It is observed in Figure. 13 that the pre and post-layout results are in close agreement except for slight deviations due to parasitics present in active blocks.

6.2 Monte Carlo analysis

Monte Carlo (MC) simulation for process mismatch at a frequency of 1 MHz for 200 simulation runs is performed for grounded topology. A similar MC analysis is performed for floating topology at a frequency of 200 kHz for 200 simulation runs. MC results for the hysteresis loop in both grounded and floating topology are shown in Figure. 14. Figure. 14 reveals that the proposed circuit is affected by process mismatch; however, the hysteresis loop closely retains the original form.

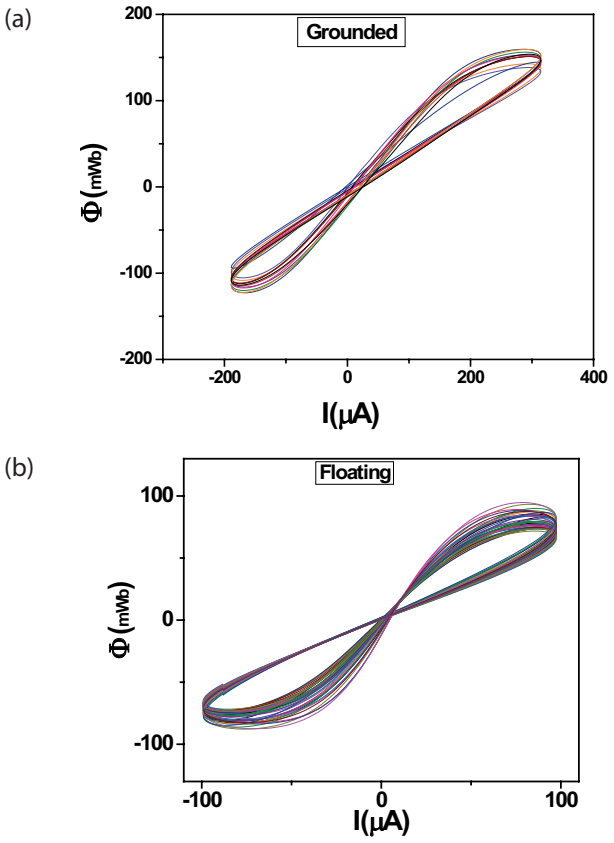


Figure. 14. Hysteresis loop of MC result for 200 simulation runs for (a) grounded topology and (b) floating topology.

7 Nonideality Analysis

Non-ideal transfer gains and parasitics of active building blocks affect the emulator's response. Sections 7.1 discusses the effect due to non-ideal transfer gains, and sections 7.2 and 7.3 discuss the effect due to OTA and CCII/CCCII parasitics.

7.1 Nonideality effect of OTA transconductance gain and CCII/CCCII current and voltage transfer gains

Due to the OTA's non-ideal transfer gain, the port relationship is modified as follows:

$$I_{0\pm} = \pm\gamma G_m \left(V_{in+} - V_{in-}\right) = \pm\gamma G_m V_{in} \tag{35}$$

γ is the non-ideal transconductance gain coefficient from the input terminal to the output terminal of OTA, which is ideally considered unity.

Similarly, the port relationships of CCII and CCCII due to non-ideal transfer gains become:

$$\begin{bmatrix} V_X \\ I_Z \\ I_Y \end{bmatrix} = \begin{bmatrix} \beta_1 & 0 & 0 \\ 0 & \alpha_1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad \text{and} \tag{36}$$

$$\begin{bmatrix} V_X \\ I_Z \\ I_Y \end{bmatrix} = \begin{bmatrix} \beta^{(j)} & R_X & 0 \\ 0 & \alpha^{(j)} & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}, \tag{37}$$

Where j=1 stands for the first CCCII and j=2 for the second CCCII. α and β and are current and voltage transfer gains from X to Z and Y to X terminals for CCII/CCCII, respectively. Ideally, α and β are unity.

The routine analysis of Figure. 4 considering non-ideal port relationships from (35), (36), and (37) for grounded meminductor configuration results in:

$$\frac{\phi_{in}}{I_{in}} = \frac{R_1 C_2 \beta^{(2)} \alpha_1 \alpha^{(2)}}{\frac{k\gamma_1}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) \mp \frac{k\gamma_1\gamma_2}{\sqrt{2}}\left(\frac{G_{m4}\left(1+sC_2R_{X2}\right)\phi_{in}}{\beta^{(2)}\alpha_1\alpha^{(2)}sC_1R_1C_2}\right)} \frac{1}{1+sC_2R_{X2}} \tag{38}$$

Similar analysis for the floating topology of Figure. 5 results in:

$$\frac{\alpha^{(1)}\beta^{(2)}V_{in1}-V_{in2}}{I_{in}}=\frac{sR_{X2}C_2}{\frac{k\gamma_1\alpha^{(2)}}{\sqrt{2}}\left(V_{ss}+2V_{th}\right)\mp\frac{k\alpha^{(2)}\gamma_1\gamma_2}{\sqrt{2}}\left(\frac{G_{m4}\alpha^{(2)}\int\left(\alpha^{(1)}\beta^{(2)}V_{in1}-V_{in2}\right)dt}{sC_1R_{X2}C_2}\right)} \tag{39}$$

[where V_{in1} - V_{in2} = V_{in} and $\int(V_{in1}$ - $V_{in2})dt = \varnothing_{in}$]

γ_1 and γ_2 are the transconductance gains of grounded and floating meminductors' first and second OTAs. It is observed from (38) and (39) that non-ideal transfer gains affect meminductance.

7.2 Nonideality effect due to device parasitics on grounded meminductor emulator

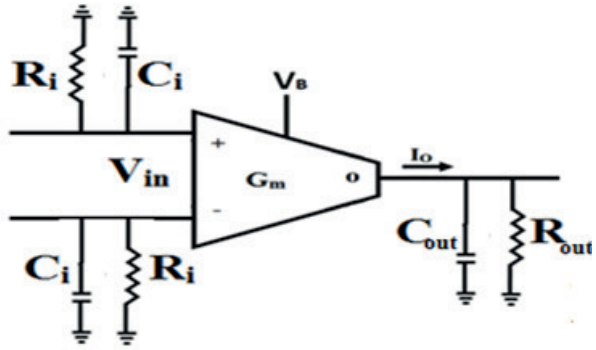


Figure 15: Non-ideal model of OTA [36-37]

Figure. 15 shows the non-ideal model of OTA where (R_i, C_i) and (R_0, C_0) are input and output parasitic capacitances and resistances, respectively. The capacitances across the input ports are assumed to be equal.

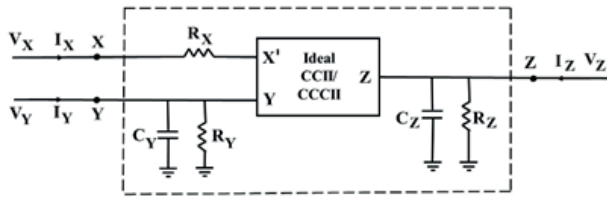


Figure 16: Non-Ideal model of the CCII/CCCII [38].

Figure. 16 shows the non-ideal model of CCII/CCCII. R_X represents a low-value parasitic resistance at the X terminal for CCII., whereas R_X for CCCII is a variable intrinsic resistance. At terminal Y and Z, the parasitic components are in parallel (i.e., R_Y || C_Y and R_Z || C_Z), where R_Y and R_Z are of high value, and C_Y and C_Z are of low value. Fig. 17 shows the non-ideal model with device parasitics of proposed grounded meminductor emulators of Fig.4. Let the impedances be:

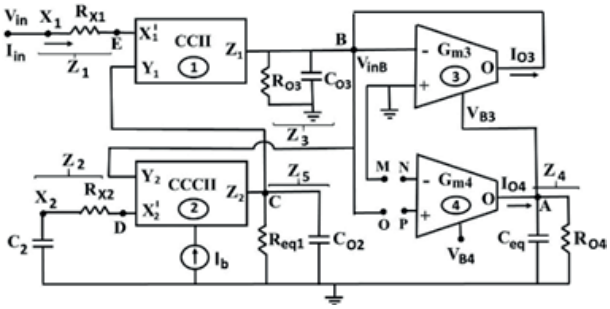


Figure 17: Non-ideal model of grounded meminductor emulator.

$$Z_1=\left(R_{X1}\right),\quad Z_2=\left(R_{X2}+X_{C2}\right),\quad Z_3=\left(R_{03}\,\|\,X_{C03}\right),\quad Z_4=\left(R_{04}\,\|\,X_{Ceq}\right)\text{ and }Z_5=\left(R_{eq1}\,\|\,X_{C02}\right) \tag{40}$$

where

$$\begin{aligned}&C_{eq}=\left(C_1+C_{out4}\right),\\&\mathrm{R}_{03}=\left(R_{i3}\,\|\,R_{i4}\,\|\,R_{Z1}\,\|\,R_{Y2}\,\|\,R_{out3}\right),\\&\mathrm{R}_{\mathrm{eq1}}=\left(R_1\,\|\,R_{Y1}\,\|\,R_{z2}\right),\\&\mathrm{C}_{03}=\left(C_{i3}\,\|\,C_{i4}\,\|\,C_{Z1}\,\|\,C_{Y2}\,\|\,C_{out3}\right),\\&\mathrm{C}_{02}=\left(C_{Z2}\,\|\,C_{Y1}\right)\text{ and }R_{o4}=R_{out4}\end{aligned} \tag{41}$$

Where R_{i3}, C_{i3}, and $R_{i4,}$ C_{i4} are parasitic resistances and capacitances at the inputs of the first OTA (G_{m3}) and second OTA (G_{m4}), respectively. Similarly, R_{out3}, C_{out3}, and $R_{out4,}$ C_{out4} are parasitic resistances and cap acitances at the first OTA (G_{m3}) and second OTA (G_{m4}) output, respectively.

$$\begin{aligned}&V_{Y2}=V_{inB}=V_{X2}-I_{X2}R_{X2}=\\&=-I_{X2}X_{C2}-I_{X2}R_{X2}=-I_{X2}Z_2\ \text{(by port relationship)}\end{aligned} \tag{42}$$

Also, on applying KCL at node C and by port relationship

$$I_{X2}=I_{Z2}=\frac{-V_{Y1}}{Z_5}=\frac{-\left(V_{X1}\right)}{Z_5}=\frac{-\left(V_{in}\right)}{Z_5} \tag{43}$$

Using (43) in (42) results in

$$V_{in} = \psi V_{inB}, \text{ where } \psi = \left(\frac{Z_5}{Z_2}\right) \tag{44}$$

On applying KCL at node B

$$I_{in} = I_{Z1} = I_{O3} - \frac{V_{inB}}{Z_3} \tag{45}$$

Using (44) and (45) results in

$$\frac{I_{in}}{V_{in}} = \left(\frac{1}{\psi}\right)\left(\frac{I_{O3} - \frac{V_B}{Z_3}}{V_B}\right) = \left(\frac{1}{\psi}\right)\left(\frac{I_{O3}}{V_B}\right)\left(1 - \frac{V_{inB}}{I_{O3}Z_3}\right) \tag{46}$$

Further analysis using (1) and $G_{m3} = \frac{-I_{O3}}{V_{inB}}$ results in the following;

$$\frac{I_{O3}}{V_{inB}} = \frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{TH}\right) - \frac{kZ_4 G_{m4} V_{in}}{\sqrt{2}\,\psi} \tag{47}$$

So, the inverse meminductance equation after substituting (47) in (46) becomes for both the incremental and decremental topologies

$$\frac{I_{in}}{V_{in}} = \frac{1}{\psi}\left(\frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) \mp \frac{kZ_4 G_{m4} V_{in}}{\sqrt{2}\,\psi}\right)\left(1 - \frac{V_B}{I_{O3}Z_3}\right) \tag{48}$$

Typical practical values of CMOS OTA parasitic obtained from routine analysis and [38] can be assumed to be approximately, $R_{i3} = R_{i4} = \infty$, $R_o = 1M\Omega$, $C_i = 50$ *fF*, $C_o = 100$ *fF*. Similarly, values of CCII/CCCII obtained from routine analysis and [40] can be assumed to be a few ohms for Rx, a few hundreds of MΩ for R_Y, and few MΩ for R_Z, and the Cy, and Cz are in the range of a few femtofarads. If the operating frequency is within the range of a few MHz, then we may use:

$Z_2 \approx R_{X2} + \frac{1}{sC_2}$, $Z_4 \approx 1/sC_1$, $Z_5 \approx R_1$ =few Ω,

$\psi = \frac{sR_1C_2}{1 + sC_2R_{X2}}$, and $Z_3 \approx \infty$, and

$\left[\frac{V_{inB}}{I_{O3}Z_3}\right] \approx 0$ as $\left(Z_3 \approx \infty\right)$.

The substitution of these values in (48) results in:

$$\frac{V_{in}}{I_{in}} = \frac{sR_1C_2}{\frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) \mp \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\left(1 + sC_2R_{X2}\right)\phi_{in}}{sC_1R_1C_2}\right)} \frac{1}{1 + sC_2R_{X2}} \tag{49}$$

This is similar to (14). Hence, it can be concluded that the effect of parasitics on the proposed grounded circuit in the frequency range of a few MHz is negligible.

7.3 Nonideality effect due to device parasitic on floating meminductor emulator

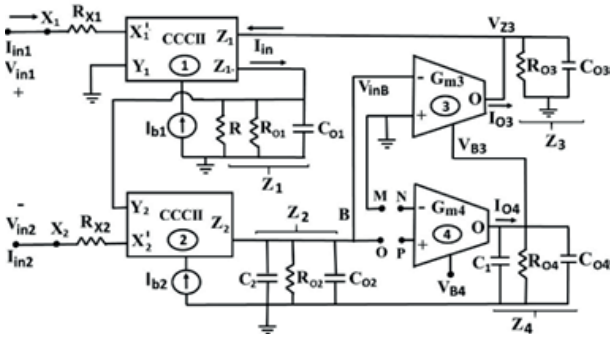


Figure 18: Non-Ideal model of proposed floating meminductor emulator.

In Figure. 18, let the equivalent impedances at nodes be given as,

$$Z_1 = \left(R_{01} \,||\, X_{C01}\right) || \, R, \; Z_2 = \left(R_{02} \,||\, X_{C02}\right) || \, X_{C2}, \; Z_3 = \left(R_{03} \,||\, X_{C03}\right) \text{ and } Z_4 = \left(R_{04} \,||\, X_{C04}\right) || \, X_{C1} \tag{50}$$

and

$$C_{01} = \left(C_{Z1-} + C_{Y2}\right), \quad C_{02} = \left(C_{Z2} + C_{i3} + C_{i4}\right), \quad C_{03} = \left(C_{out3} + C_{Z1}\right), \quad C_{04} = \left(C_{out4}\right), \quad R_{01} = \left(R_{Z1-} \,||\, R_{Y2}\right), \quad R_{02} = \left(R_{Z2} \,||\, R_{i3} \,||\, R_{i4}\right), \quad R_{03} = \left(R_{Z1} \,||\, R_{out3}\right), \; R_{04} = \left(R_{out4}\right) \tag{51}$$

Also, $V_{Y2} = V_{z1-} = \frac{V_{in1}}{R_{X1}} Z_1$ (by port relationship) (52)

By applying the port relationship at the X_2 terminal of CCCII and using (52), we get:

$$V_{X2} = V_{in2} = V_{Y2} + I_{X2}R_{X2} = \frac{V_{in1}}{R_{X1}} Z_1 + I_{X2}R_{X2} \tag{53}$$

Moreover, at node B,

$$-I_{Z2}Z_2 = V_{inB}\text{, or, } I_{Z2} = I_{X2} = \frac{-V_{inB}}{Z_2} \tag{54}$$

Thus, from (53) and (54),

$$\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2} = V_{inB}\frac{R_{X2}}{Z_2} \tag{55}$$

Further as; $I_{in} = I_{Z1} = I_{O3} - \frac{V_{Z3}}{Z_3}$ (56)

Hence, from (55) and (56)

$$\frac{\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}}{I_{in}} = \frac{V_{inB}}{\left(I_{O3} - \frac{V_{Z3}}{Z_3}\right)}\frac{R_{X2}}{Z_2} \tag{57}$$

Or, $$\frac{\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}}{I_{in}} = \frac{V_{inB}}{I_{O3}\left(1 - \frac{V_{Z3}}{I_{O3}Z_3}\right)}\frac{R_{X2}}{Z_2} \tag{58}$$

Further, as $V_{B3} = Z_4 I_{O4} = Z_4 G_{m4} V_{inB}$ (59)

Hence from (55), by putting the value of V_{inB} in (59), V_{B3} becomes;

$$V_{B3} = \left(G_{m4}Z_4\right)\left(\frac{Z_2}{R_{X2}}\right)\left(\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}\right) \tag{60}$$

Also, $G_{m3} = \frac{-I_{O3}}{V_{inB}}$ (61)

Further from (1) and (60),

$$G_{m3} = \frac{k}{\sqrt{2}}\left(V_{B3} - V_{ss} - 2V_{th}\right) =$$

$$= \frac{k}{\sqrt{2}}\left(\left\{\left(G_{m4}Z_4\right)\left(\frac{Z_2}{R_{X2}}\right)\left(\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}\right)\right\} - V_{ss} - 2V_{th}\right)$$

Using (61) results in;

$$\frac{I_{O3}}{V_{inB}} = -\frac{k}{\sqrt{2}}\left(\left\{\left(G_{m4}Z_4\right)\left(\frac{Z_2}{R_{X2}}\right)\left(\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}\right)\right\} - V_{ss} - 2V_{th}\right)$$

$$\frac{I_{O3}}{V_{inB}} = \frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th} - \left\{\left(G_{m4}Z_4\right)\left(\frac{Z_2}{R_{X2}}\right)\left(\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}\right)\right\}\right) \tag{62}$$

On substituting (62) in (58) we obtain (both the incremental and decremental topologies) as;

$$\frac{\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}}{I_{in}} = \frac{\frac{R_{X2}}{Z_2}}{\frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th} \mp \left(G_{m4}Z_4\right)\left(\frac{Z_2}{R_{X2}}\right)\left(\frac{V_{in1}}{R_{X1}}Z_1 - V_{in2}\right)\right)}\left(1 - \frac{V_{Z3}}{I_{O3}Z_3}\right) \tag{63}$$

It is inferred from (63) that meminductance will be affected by parasitics, however, the typical values of CMOS OTA parasitics obtained from routine analysis and [38] are; $R_i = \infty$, $R_o = 1M\Omega$, $C_i = 50$ *fF*, $C_o = 100$ *fF*, while those of CCII/CCCII are as discussed previously in connection to grounded meminductor. If the operating frequency is within the range of a few MHz (say 10 MHz), then we may write: $Z_2 = X_{C2}$, $Z_4 = XC_1$, $Z_1 = R$, $R = R_{X1}$, $Z_3 \approx$ very high, and hence, $\left[\frac{V_{Z3}}{I_{O3}Z_3}\right] \approx 0$. The substitution of these terms in (63) for both incremental and decremental topologies results in:

$$\frac{V_{in}}{I_{in}} = \frac{sR_{X2}C_2}{\frac{k}{\sqrt{2}}\left(V_{ss} + 2V_{th}\right) \mp \frac{k}{\sqrt{2}}\left(\frac{G_{m4}\phi_{in}}{sC_1R_{X2}C_2}\right)} \tag{64}$$

This is similar to (32) and (33). Hence it can be concluded that the effect of parasitics on the proposed floating meminductor in the frequency range of 10 MHz is negligible.

8 Application of meminductor as amplitude modulator (AM)

An AM modulation scheme with a meminductor is carried out as an application of the proposed meminductive device. Schematic of various circuits along with a floating meminductor emulator is shown in Figure. 19. In Figure. 19(a), a multifunction filter [39] using OTA is

given, which can implement both bandpass filter (BPF) and low pass filter (LPF) responses using the components, as given in Table 4, for Y_1, Y_2, Y_3, Y_4, and Y_5. Current mode (CM) BPF and LPF filters are used for modulation and demodulation, respectively. The meminductance of the meminductor shown in Figure. 19(b) is controlled by the low-frequency message signal $V_m(t)$, due to which message gets imposed on the high-frequency carrier signal $V_c(t)$. The output is filtered out by the bandpass filter in Figure. 19(a) centered at the carrier frequency to obtain an amplitude-modulated wave. The circuit in Figure. 19(c) is used to demodulate the AM signal to recover the message signal.

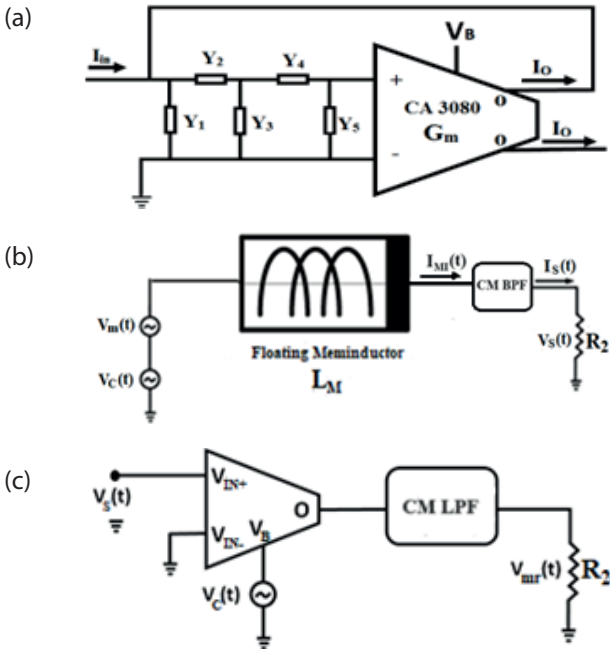


Figure 19: Block diagram of (a) current mode multifunction filter, (b) AM modulator circuit using floating meminductor emulator and filter, (c) coherent demodulator circuit using OTA.

Table 4. Specification for multimode filter components

	Y_1	Y_2	Y_3	Y_4	Y_5
Low pass	C1	R2	C3	∞	0
Band pass	R1	R2	C3	C4	R5

8.1 Analysis of amplitude modulator and demodulator

The voltage message signal $V_m(t)$ and carrier signal $V_c(t)$ are given by

$$V_m(t) = A_m \cos(\omega_m t),\ V_C(t) = A_C \cos(\omega_c t) \quad (65)$$

The flux imposed on the meminductor is given by

$$\varphi_{in} = \int V_{in}(t)\,dt = \int \left(V_m(t) + V_C(t)\right)dt = \\ = \frac{A_m \sin(\omega_m t)}{\omega_m} + \frac{A_C \sin(\omega_C t)}{\omega_C} \quad (66)$$

Also, $V_{in}(t) = A_m \cos(\omega_m t) + A_C \cos(\omega_c t)$ (67)

Thus, the output current of the meminductor, $I_{MI}(t)$, of Figure 19(b) results as:

$$I_{MI}(t) = V_B \frac{k}{\sqrt{2}}\left(\frac{G_{m4}}{C_1}\int V_B(t)\,dt - V_{ss} - 2V_{th}\right) \quad (68)$$

Now using (26), (66), and (67) in (68) and passing it through BPF yields;

$$I_s(t) = M_1 \sin\omega_c t + M_2\left[\sin(\omega_c + \omega_m) + \right. \\ \left. + \sin(\omega_c - \omega_m)\right] + M_3[\sin(\omega_c + \omega_m) - \\ - \sin(\omega_c - \omega_m)] \quad (69)$$

where,

$$M_1 = -\frac{k(V_{SS} + 2V_{th})A_C}{\sqrt{2}R_{X2}C_2\omega_C},$$

$$M_2 = \frac{A_C A_m G_{m4} k}{2\sqrt{2}C_1\omega_C}\left(\frac{1}{sR_{X2}C_2}\right)^2 \text{ and}$$

$$M_3 = \frac{A_C A_m G_{m4} k}{2\sqrt{2}C_1\omega_m}\left(\frac{1}{sR_{X2}C_2}\right)^2$$

It is evident that (69) is in the form of components of the upper sideband, lower sideband, and carrier of standard AM expression. In order to recover the message signal from the modulated signal, a coherent product demodulator is used. The demodulator circuit is realized with OTA as a multiplier cascaded with an OTA-based low pass filter, as shown in Figure. 19(c).

8.2 Simulation of amplitude modulator and demodulator

The parameters used for simulating the amplitude modulator (AM) and demodulator are given in Table 5. Figure. 20(a) shows the carrier signal ($V_C(t)$), modulating signal ($V_m(t)$), and the modulated signal, $V_s(t) = I_s(t)$ R_1 taken at the output of current mode band pass filter in Figure. 19(b). Figure. 20(b) shows the modulated

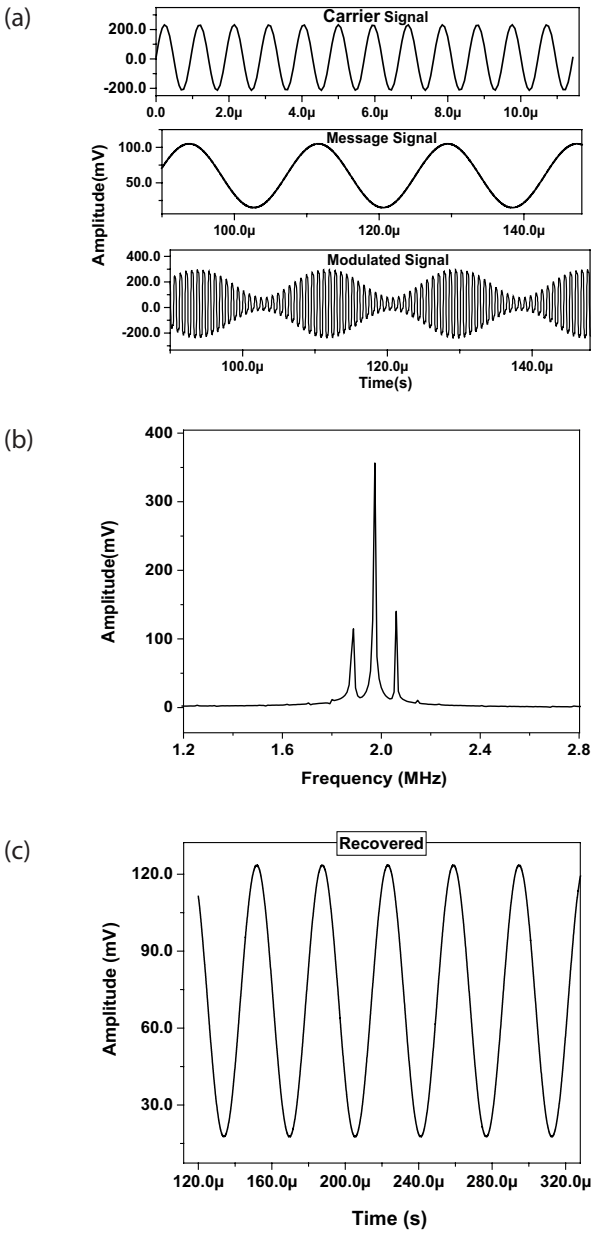
signal spectrum obtained by applying the rectangular window function. Figure. 20(c) shows the recovered message signal, $V_{mr}(t)$, obtained at the output of the coherent demodulator, as shown in Figure. 19(c). It confirms that the scheme of AM proposed in this section using meminductor circuit works as intended. It can further be shown that one can obtain under, over, and critical modulations by varying the amplitude of carrier and message signal. Figures 20(d) and 20(e) show amplitude-modulated waveform and its hysteresis loop for the one-time period, respectively. On analyzing Figure. 20(d) and Figure. 20(e) simultaneously, one can observe that the amplitude of the hysteresis loop formed between charge and voltage increases and decreases according to the increase and decrease in the amplitude of the message signal. So, the hysteresis loop itself changes its shape, size, and amplitude according to the message signal. For the first half cycle of the message signal, i.e., for time interval A-B in Fig. 20(d), the amplitude of the hysteresis loop in Fig. 20(e) decreases from point S to T in the positive half cycle, and point U to V in the negative half cycle of the modulated wave, simultaneously. This results in the mapping of message amplitude on the carrier signal. Similarly, for the second half cycle of the message signal, i.e., for time interval B-C in Figure. 20(d), the hysteresis loop of Figure. 20(e) increases from point T to S for the positive half cycle and point V to U for the negative half cycle of the modulated wave simultaneously leading to the mapping of message amplitude on the carrier signal. Thus, the hysteresis loop, resulted from one time period of AM signal is nothing but a meminductance slope, which is frozen i.e. it does not get affected by the peak amplitude variation of the carrier signal and follows the amplitude variation of the message signal. This means, the increment/decrement in hysteresis loop as visible in Figure 20(e) is corresponding to the variation in amplitude of message signal. From Figure. 20(e), we find that the hysteresis loops overlap each other on each half-cycle.

Table 5: AM circuit simulation parameter

S.No.	Parameter	Value
1	Message signal amplitude Am	120 mV
2	Message signal frequency fm	50 kHz
3	Carrier signal amplitude Ac	240 mV
4	Carrier signal frequency fc	1 MHz
5	Band Pass filter center frequency	1 MHz
6	Band Pass Resistance (R1=R2=R5); these three resistances are being used in BPF as per Fig. 19(a) and Table 4	200 Ω
7	Band Pass Filter Capacitance (C_3=C_4)	150 pF
8	Capacitance C_1	32 pF
9	Capacitance C_2	150 pF
10	Local carrier amplitude	240 mV
11	Local carrier frequency fc	1 MHz
12	Low Pass filter cut-off frequency	50 kHz
13	Low Pass Resistance R_2	200 Ω
14	Low Pass Filter capacitance (C_1=C_3)	10 pF

9 Experimental results

As monolithic implementations of the proposed meminductor are not available, the possible experimental realization of meminductors using commercially available ICs, AD844 and CA3080, is shown in Figure. 21 (a, b), followed by the assembled grounded meminductor



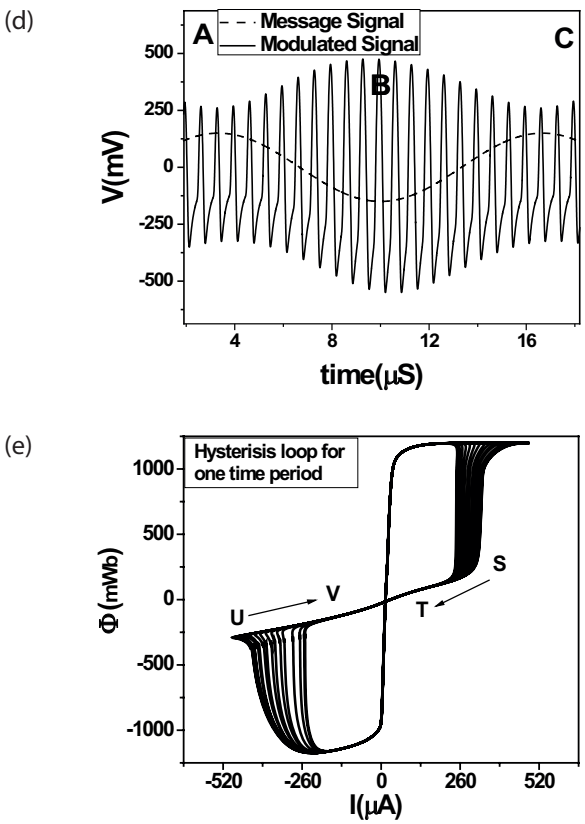


Figure 20: The plot of (a) carrier signal, message signal, and modulated signal, (b) spectrum of the modulated signal, (c) recovered message signal, (d) waveform of message and carrier for one period, (e) hysteresis loop of AM for one period.

emulator on a breadboard given in Figure. 21 (c). This circuit can broadly verify the functionality; however, detailed parameters are comparable with monolithic implementation. To verify experimentally, the proposed meminductor emulator is implemented with capacitance (C_1) as 40nF (in a parallel combination of four 10nF), resistance (R_1) of 100 Ω, and commercially available BJT-based OTA ICs (CA3080), and CFOA ICs (AD844). The pinched hysteresis loops of the emulator are obtained for the operating frequency of 820 kHz for a 4V peak-to-peak input signal, as shown in Figure. 22(a). Figure. 22(b) shows the pinched hysteresis loops for a floating meminductor (hardware implementation not shown) emulator at an operating frequency of 910 kHz for a 4V peak-to-peak input signal. Figure. 22(c) shows the time domain waveform for the grounded meminductor's current and charge (integral of current). Figure. 22(d) shows the time domain waveform for input phi (φ) and rho (ρ) (integral of phi) (using double integration in DSO) for the grounded meminductor. It can further be noted that both charge and rho (ρ) curves tend to increase as time increases which justifies that the proposed circuit is a meminductor. Figure. 22(e) shows the time domain waveform for flux and current for the grounded meminductor. Analysis of Figure. 22(e) reveals that the proposed circuit possesses a nonlinear relationship between flux and current and the relationship is not simultaneously zero all the time, just at one point simultaneously zero, thus verifying passivity.

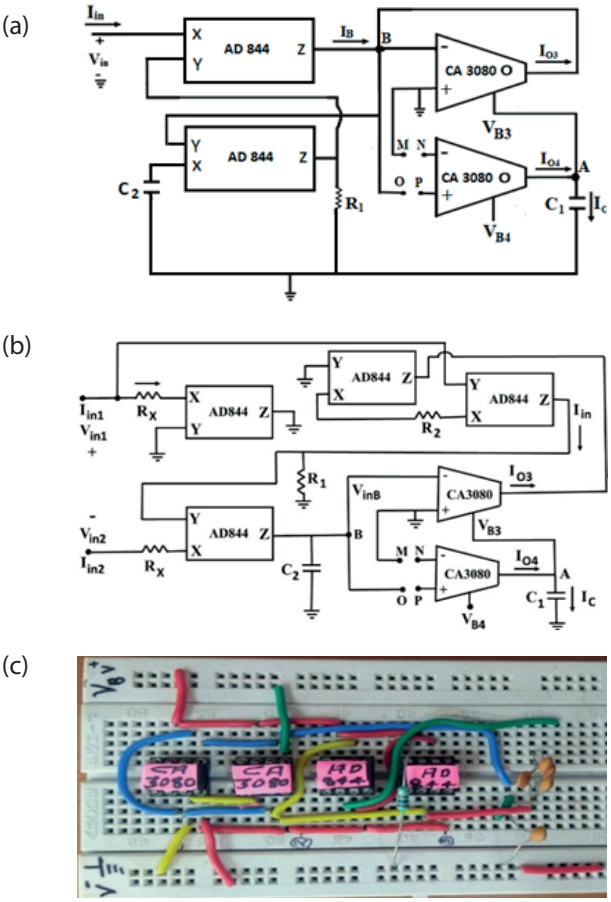


Figure 21: Meminductor emulator (a) Grounded Meminductor experimental circuit, (b) Floating Meminductor experimental circuit, (c) Prototype on a breadboard.

10 Conclusion

The proposed grounded and floating meminductor emulators show a pinched hysteresis loop and meminductive nature similar to an actual memindcutive device. Emulators have simple circuitry built with two OTAs and two CCII/CCCII. Proposed emulators are useful for a frequency of up to 1 MHz for grounded and 10 MHz for floating in both incremental and decremental topologies. The meminductance of the proposed emulators is electronically tunable with the bias voltage of OTA. The controllability of the pinched hysteresis loop and the meminductance nature of proposed emulators

for different frequencies of the input signal, capacitors, and external bias voltage is verified by simulation results. Layout, post-layout simulations, Monte Carlo, and detailed non-ideal analyses have also been carried out. Moreover, an AM modulator has been realized using the proposed meminductor emulator circuit as an application. Finally, a prototype of the proposed circuit is assembled, and experimental results are given and discussed.

(a)

(b)

(c)

(d)

(e)

Figure 22: Experimental Results of meminductor emulator (a) hysteresis loop for grounded meminductor, (b) hysteresis loop for floating meminductor, (c) time domain waveform for Current (Green) and Charge (pink), (d) time domain waveform for phi (yellow) and rho (pink), (e) time domain waveform for phi (nonlinear) and current (sinusoidal).

11 Conflict of interest

The authors declare no conflict of interest.

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Arrived: 19. 06. 2023
Accepted: 01. 12. 2023

Original scientific paper
https://doi.org/10.33180/InfMIDEM2023.304

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 53, No. 3(2023), 167 – 176

Detection of Burst Header Packet Flooding Attacks via Optimization based Deep Learning Framework in Optical Burst Switching Network

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Abstract: Optical Burst Switching (OBS) technique has the greatest potential for securing future Internet connections. In real-time applications, OBS adoption is motivated by the lack of Quality of Service (QoS) in OBS networks. The accuracy of existing methods for detecting the misbehaving nodes that cause Burst Heading Packet (BHP) flooding attacks is typically poor. To overcome these issues, a novel Elephant Herd Algorithm-based Deep Learning (EHA-DL) network has been proposed for detecting BHP flooding attacks. The proposed approach is divided into three phases: pre-processing, feature selection, and classification. The Elephant Herd Algorithm (EHA) is used to select the most crucial features after pre-processing the raw data to increase the effectiveness of the model. To decrease overfitting and increase detection accuracy, a MobileNet is used to construct the model for the classification phase using the select features of BHPs. The performance of the experimental outcomes was assessed using evaluation metrics like accuracy, specificity, recall, and f-measure. The EHA-DL approach method yielded a 99.27% accuracy rate, which was comparatively high when compared to other approaches. In optical burst switching networks, the method effectively and highly efficiently detects flooding assaults and maintains network stability.

Keywords: Optical Bust Switching; Quality of Service; Burst Header Packet (BHP) flooding attack; Deep learning

Detekcija napadov s hitrimi naslovnimi paketi s pomočjo optimizacije na osnovi globokega učenja v omrežju optičnega hitrega prekapljanja

Izvleček: Tehnika optičnega hitrega preklapljanja (Optical Burst Switching - OBS) ima največji potencial za zavarovanje prihodnjih internetnih povezav. Pri aplikacijah v realnem času je razlog za uvedbo OBS pomanjkanje kakovosti storitev (QoS) v omrežjih OBS. Natančnost obstoječih metod za odkrivanje nepravilno delujočih vozlišč, ki povzročajo poplavne napade s paketi BHP (Burst Heading Packet), je običajno slaba. Za odpravo teh težav je bilo predlagano novo omrežje EHA-DL (Elephant Herd Algorithm-based Deep Learning) za odkrivanje poplavnih napadov BHP. Predlagani pristop je razdeljen na tri faze: predobdelava, izbira značilnosti in klasifikacija. Algoritem Elephant Herd Algorithm (EHA) se uporablja za izbiro najpomembnejših značilnosti po predhodni obdelavi neobdelanih podatkov, da se poveča učinkovitost modela. Za zmanjšanje pretiranega prilagajanja in povečanje natančnosti zaznavanja se za izdelavo modela za fazo razvrščanja z izbranimi značilnostmi BHP uporablja mobilna mreža. Uspešnost eksperimentalnih rezultatov je bila ocenjena z ocenjevalnimi metrikami, kot so natančnost, specifičnost, priklic in f-merilo. Metoda pristopa EHA-DL je dala 99,27-odstotno stopnjo natančnosti, ki je bila v primerjavi z drugimi pristopi razmeroma visoka. V optičnih omrežjih s preklapljanjem s prekinitvami metoda uspešno in zelo učinkovito odkriva napade s poplavljanjem in ohranja stabilnost omrežja.

Ključne besede: Optično hitro preklapljanje; kakovost storitev; napad s poplavljanjem paketov BHP (Burst Header Packet); globoko učenje

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How to cite:
R. Vahalingam et al., "Detection of Burst Header Packet Flooding Attacks via Optimization based Deep Learning Framework in Optical Burst Switching Network", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 53, No. 3(2023), pp. 167–176

1Introduction

Optical fiber communication outperformed conventional communication systems and revolutionized communication technology [1]. Over the last few decades, optical networks have expanded quickly in tandem with rising bandwidth demands [2]. Consequently, optical burst switching networks are commonly used as both a backbone and an access network today [3]. The development of Internet backbone infrastructures has been made possible by OBS, which has grown in importance as a method for switching subwavelengths in networks [4]. Three different node categories, referred to as core nodes, ingress nodes, and egress nodes, make up the primary component of the OBS network. Optical data bursts are processed through control data packets with information by intermediate nodes called core nodes, which avoid buffering [5].

In OBS, the client packet is merged into a burst header packet (BHP) and a Data Burst (DB) at the edge nodes (ingress nodes) [6]. OBS networks still face several QoS and security issues as a consequence of BHP flooding attacks, despite all of their network benefits, including resilience, bandwidth/resource efficiency, and overall financial benefits [7]. Preparing the channel for incoming DB is done using OBS's BHP feature. An attacker can use this function to transmit fake BHPs without being acknowledged by the DB. It is important to understand that Denial-of-Service (DoS) attacks are one of the most significant security risks to networks, which can lower network efficiency through reduced bandwidth utilization and increased data loss [8,9].

BHP flooding is a type of assault where a lot of BHPs are sent into a network to control the switches [10]. Malicious nodes flood the network with BHPs during a BHP flooding assault, which reduces network bandwidth usage. Since it takes over the core switch and fills the wavelength division multiplexing channel, regular BHP is unable to transmit [11]. Flood attacks result in serious data loss, network performance degradation, and bandwidth waste when edge nodes send BHP at high speeds to reserve bandwidth for future bursts of data. Another major danger to network security is denial-of-service (DoS) attacks [12,27].

Numerous strategies have been developed in the literature for defending against BHP flooding attacks and DoS against OBS networks, with positive results. However, because OBS core switches have limited capabilities, it is still difficult for developers and researchers to come up with an effective technique that achieves high accuracy with a minimal number of features. This study's main goal is to reduce those risks by analyzing edge node behavior in OBS networks during BHP flood attacks. In this research, a novel Elephant herd algorithm-based Deep learning (EHA-DL) has been proposed for detecting BHP flooding attacks [28]. The major contribution of the proposed technique is;
The primary goal is to develop a novel Elephant herd algorithm-based Deep learning (EHA-DL).
The Elephant Herd Algorithm (EHA) is utilized to select the most crucial features after pre-processing the raw data to increase the effectiveness of the model.
To decrease overfitting and increase detection accuracy, a MobileNet is used to construct the model for the classification phase using the select features of BHP.
Evaluation measures like accuracy, precision, recall, specificity, and f-measure were used to evaluate the performance of the experimental results.

The following examples illustrate the remaining section of this study: the literature survey is explained in Section 2. The proposed approach and its corresponding algorithm are described in Section 3. The findings of the performance analysis are described in Section 4. Section 5 encloses a conclusion and future work.

2 Literature survey

In 2018, Uzel, V.N., and Eşsiz, E.S., et al [13] presented machine learning methods for categorizing BHP Flooding Attacks into four class labels. The following techniques are employed in classification: Multilayer Perceptron (MLP), Logistic, Decision Tree (J48), Reduce Error Pruning (REP) Tree, Naive Bayes (NB), and Random Tree (RT). As a consequence, it has been discovered that J48 and RT produce the best outcomes with greater accuracy.

An approach to lower the likelihood of BHP flooding assaults in OBS networks was proposed by Rajab, A., et al. [14] in 2018. Based on the principles derived by the proposed learning algorithm, the results show that 93% of BHP flooding attacks will be accurately classified into either the Behaving (B) or Mis-behaving (M) classes. Based on comparisons with experts or human network managers, the results of the proposed decision tree model are overwhelmingly positive.

In 2018, Hasan, M.Z., et al [15] introduced a Deep Convolution Neural Network (DCNN) model for autonomously identifying edge nodes. The demonstration demonstrated that the suggested model performs as expected for datasets with a specific collection of features. The results show that the suggested deep model performs better than any other conventional model (SVM, KNN, and Naive Bayes).

Haque, M.M., and Hossain, M.K. [16] proposed the use of K-means in 2019 to detect malicious nodes in an OBS network. In experiments, the model could categorize all nodes as behaving or non-behaving with 90% accuracy after only 20% of the data was used for training. Based on various performance metrics, the proposed model outperforms existing methods.

In 2019, Rajab, A., [17] suggested using machine learning (ML) to detect and block misbehaving ingress nodes at an early stage. More than two ingress nodes, more than 530 runs, and simulation data were used to test a range of machine-learning techniques. The runtime results, expressed in milliseconds, show that decision tree classifiers outperform the other algorithms in terms of efficiency and prediction.

In 2020, Kamrul Hossain and Mokammel Haque [18] suggested using a Gaussian mixture model (GMM) predictor to forecast how traffic will behave in an OBS network. Only 1% of the test data were labelled, and they discovered the highest accuracy of 69.7% using the tied covariance type of the constructed GMM.

in 2020, Almaslukh, B., [19] suggested an effective and efficient ML-based security method for identifying BHP flooding attacks. A phase of feature selection and a phase of categorization make up the suggested methodology. Comparing the efficacy as well as efficiency of the suggested method with related research, it is found to be appropriate for OBS security of networks.

A method for identifying BHP flooding attacks using particle swarm optimization and support vector machines (PSO-SVM) was presented by Liu, S., et al. [20] in 2021. The outcomes of the experiments demonstrate that the PSO-SVM model's detection efficiency is 95.0%. In identifying assaults in OBS networks and preserving the security and stability of the network, the suggested method is efficient and highly effective.

In 2021, EFEOLU, E. and Gürkan, T.U.N.A. [21] introduced K* algorithms and Sequential Minimal Optimization (SMO) for categorizing BHP attacks. Based on standard performance metrics, the suggested SMO and K* algorithms' performances are contrasted. The findings demonstrate that the K* algorithm is more effective at forecasting BHP Flooding attacks than the SMO algorithm.

Panda (2019) introduced the Flower Pollination method (FPA) and subsequently employed a Decision Forest method that penalizes attribute classifiers to detect flooding threats. The efficacy of the suggested approach is evaluated using several performance criteria, such as recall, informedness, specificity, sensitivity, precision, and accuracy.

According to a literature review, BHP flood attacks typically have low detection accuracy for the misbehaving nodes that contribute to BHP attacks, but they can achieve high detection accuracy with a small number of features. To overcome these challenges, a novel Elephant herd algorithm-based Deep learning has been proposed.

3 Proposed methodology

In this research, a novel Elephant herd algorithm-based Deep learning (EHA-DL) has been proposed for detecting BHP flooding attacks. The proposed method is categorized into three phases: pre-processing, feature selection, and classification. The EHA is used to select the most crucial features after pre-processing the raw data to increase the effectiveness of the model. To decrease overfitting and increase detection accuracy, a MobileNet is used to construct the model for the classification phase using the selected features of BHP. The overall block of the proposed method is depicted in Fig 1.

3.1 Pre-processing

It is essential for improving the data's suitability for model analysis and learning. Initial data is typically incomplete in the actual world, also known as "dirty data." Direct learning from these data could result in some mistakes. Data preparation is the process of transforming "dirty data" into a format that machine language can "learn" easily. This phase involves data cleaning, data transformation, and data noise removal.

Data Cleaning: In this process, only a small number of missing values are removed from the data, so it does not affect the analysis. It also removed the Packet Size Byte (D11), which is a constant value and does not provide any useful information.

Data transformation: This procedure involves the not behaving, NB Block, Block, Block, node status behaving, NB, probably not behaving, and No Block Wait are transformed into one-hot encoding, which improves the processing efficiency of the classifier. One-hot encodings, for instance, of the "Node Status," such as " B, NB, PNB," are {0, 1, 0}, {1, 0, 0}, and {0, 0, 1} correspondingly.After transformation, all the data are transformed into numeric values. The features should be normalized to make the various indicators comparable to remove the dimensional impact between data features. Afterward, min-max normalization is used to standardize data, removing the influence of various samples' attributes with varying orders of magnitude as well as improving classification accuracy by searching for the best gradient descent solution.

$$Normal_p = \frac{P - P_{min}}{P_{max} - P_{min}} \quad (1)$$

Where, $Normal_p$ represents the normal value, P_{max} and P_{min} represents the minimum and maximum data before normalization. By using this technique, the data is compressed to a number that is proportionally equal to the original value and falls within the [0, 1] range.

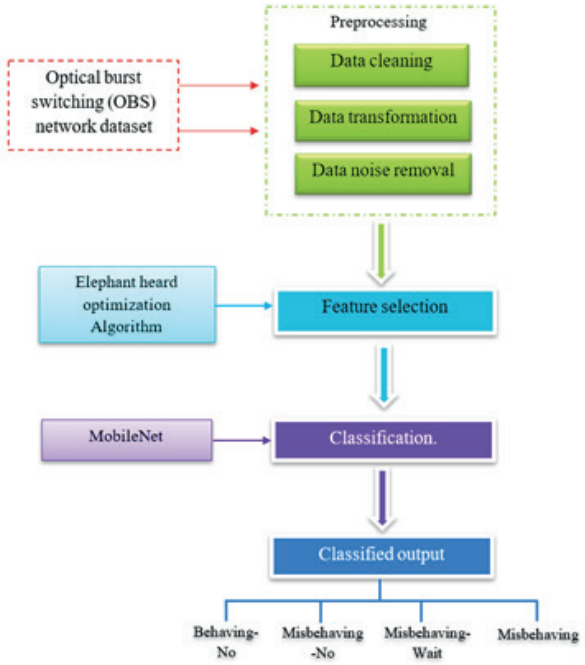

Figure 1: The overall block of the EHA-DL model

Data noise removal: The Gaussian distribution is used to introduce noise into the data to make the variables statistically more significant and to level the values of the variables. Additionally, it serves to avoid overfitting during developing models. A mathematical formula for Normal distribution is given in equation (2)

$$\varphi(q) = \frac{1}{\sqrt{2\pi\tau}} \exp\{-(-(q-\omega)^2 / 2\tau^2 \quad (2)$$

Where, π, τ denotes the variance and expectation of Gaussian distribution.

3.2 Feature selection via elephant herd algorithm (EHA)

Following preprocessing, the feature selection stage removes as much of the pre-processed data as feasible to enhance model training performance. EHA is used to select relevant features [23, 24, 25]. It is based on how elephants behave and live. Elephant intelligence (EHA) is a heuristic intelligence system that draws inspiration from elephants' nomadic lifestyle. Elephants are social animals with a sophisticated structure that consists of a female and young. The EHA selects the most pertinent features from the extracted features. After the matriarch dies, the best female elephant in the clan is designated as the most relevant feature of the data; the irrelevant features represent the male elephants with the lowest fitness value. The number of elephants in this algorithm indicates the features that were extracted from the input layer.

An elephant herd consists of multiple clans, each headed by a matriarch who may be responsible for caring for calves or other related females. The algorithm suggests the following guidelines: Elephants live in clans, with a certain number of elephants belonging to each tribe. In addition, every tribe has a matriarch who serves as the leader (the most physically fit elephant in the clan). Every generation, a predetermined number of elephants (the worst candidates) must leave the clan, and the matriarch is in charge of the entire clan of elephants. The Elephant Herding Optimization algorithm consists of two stages: separation operators and clan update operators. The entire population of elephants is initially split up into 'y' clans. Each elephant m_x a new position is influenced by the matriarch m_x. The clan m_x elephant 'y' can be determined using

At first, all elephants in the population are divided into "y" clans. The matriarch m_x has an impact on every elephant m_x that moves into a new position. It is possible to identify the clan m_x elephant 'y' using

$$P_{n,m_{x,y}} = P_{m_{x,y}} + \alpha \times \left(P_{best,m_x} - \lambda_{m_{x,j}} \right) \times L \quad (3)$$

where $P_{n,m_{x,y}}$ represents the old and new places of elephant "y" in clan x, P_{best,m_x} represents the position with the highest fitness values inside clan "x," and [0,1] is a scaling factor. L is a random number with an average distribution and a value in the interval [0, 1]. The best elephants in each clan are chosen using

$$P_{n,m_{x,y}} = \beta \times P_{ct,m_x} \quad (4)$$

In the following iteration, the position of the clan leader $P_{n,m_{x,y}}$ will vary based on the influence of the clan center P_{ct,m_x}, with $\beta \in [0.1]$ representing the scaling factor. The value of a clan center is calculated using Eq. (5):

$$P_{ct,m_x,k} = \frac{1}{N_{m_x}} \times \sum_{y=1}^{N_{m_x}} P_{ct,m_x,k} \quad where 1 \le k \le K \quad (5)$$

The total number of elephants in the clan, N_{m_x}, is represented by the k[th] dimension of each elephant. The information of every clan member is connected to the updating of the matriarch position in Equation (4).

During the separation process, the worst solution individuals are swapped out for randomly initialized individuals. Elephant populations grow as a result, and their ability to explore is enhanced. Each tribe's least valuable elephants are moved to the location shown by

$$P_{w,m_x} = P_{Min} + \left(P_{Max} - \lambda_{Min} + 1\right) \times L \tag{6}$$

The positions of the elephant with the lowest and highest fitness values in clan "x" are denoted by P_{w,m_x} and; L is a random number with a normal distribution falling between [0, 1].

Selecting a random number slows down convergence by introducing problems like random replacement of the smallest person and lack of exploitation. To address this problem, the LF mode and the EHO are combined. The model for the LF is,

$$LF\left(L\right) = \begin{cases} 1 & L < 1 \\ (L)^{-F} & L \geq 1 \end{cases} \tag{7}$$

The progress of EHA with LF is obtained by combining equations 5 and 6.

$$P_{w,m_x} = P_{Min} + \left(P_{Max} - \lambda_{Min} + 1\right) \times LeF\left(L\right) \tag{8}$$

As a result, the EHA provides the most pertinent features, which are as follows:

$$RF_x = \left\{rf_1, rf_2, rf_3, \ldots\ldots, rf_n\right\} \tag{9}$$

Following the inputs' multiplication by the feature vectors, the features that were randomly selected are then added together. The input layer can be expressed numerically as

$$I_x = \sum_{x=1}^{n} RF_x w_x + B_x \tag{10}$$

In this instance, RF_x represents the input features, w_x indicates the weight values, B_x indicates the bias value, and I_x displays the IL.

3.3 Classification via MobileNet

The selected features are classified by utilizing MobileNet. The convolution used in conventional networks is regular, however in this network, depth-wise separable convolution (DSConv). Requiring fewer modulo parameters than a standard convolution network, a MobileNet [26] network built on DSConv can carry out the same feature extraction function. Hardware resource constraints related to networks can thus be loosened. Pairwise convolution (PWConv) and depth-wise convolution (DWConv) are combined to create a depth-wise separable convolution. Figure 2 illustrates the structure.

DWConv does not support multidimensional convolution kernels; instead, each convolution kernel is limited to handling a single channel. After DWConv, the number of channels cannot be raised. Furthermore, using feature data from several channels at the same spatial position is not feasible due to the sequential nature of each convolution operation between each channel. PWConv must be paired with the feature maps produced by DWConv to produce new feature maps. PWConv is distinct from regular convolution due to its convolution kernel size of 1x1. A combination of sev-

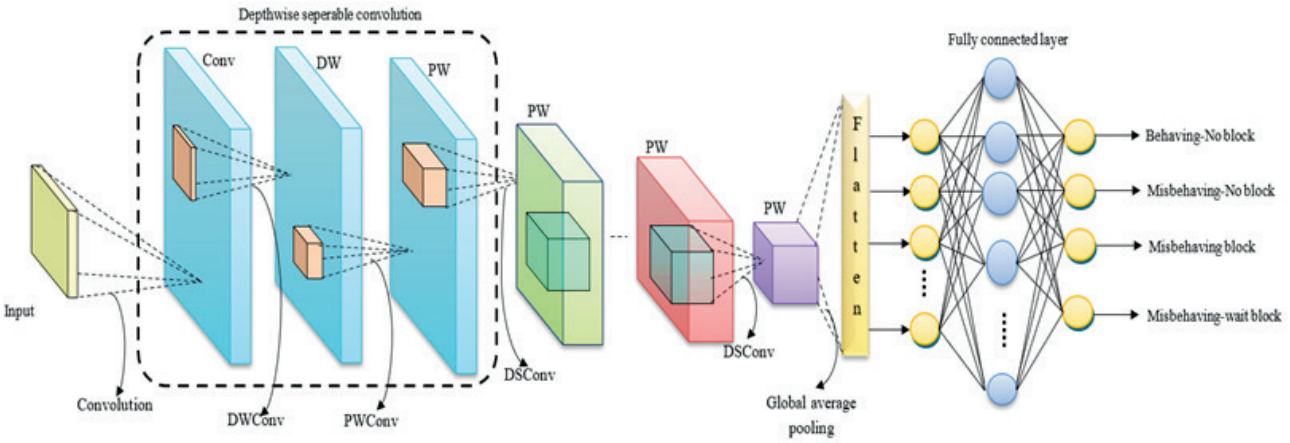

Figure 2: Architecture of proposed MobileNet

eral convolutions with rectified linear units (ReLUs) makes up the fundamental model's degrees of abstraction. employing the resolution multiplier variable ω to reduce the dimensionality and internal depiction of each layer in the input using the same variable. The kernel has dimensions of $k_s * k_s$, while the feature vector map has dimensions of $f_m * f_m$. The variable that is input is called x, while the variable that is output is denoted by y. To assess the total computing efforts C_{eff} for the network's central abstract layers, utilize equation (9) as follows.

$$C_{eff} = k_s * k_s * \omega * \alpha f_m + \omega * \rho * \alpha f_m * \alpha f_m \quad (11)$$

The multiplier value is clear for context, and the range from 1 to n is taken into account for the weed classification breakdown that results. The value of the variable resolution multiplier is expected to be 1, and it is recognized as ω. The variable $cost_{eff}$ is used to identify the computational efforts, and Equation (12) is used to assess it.

$$cost_{eff} = k_s * k_s * \omega * \rho * f_m * f_m \quad (12)$$

The DWConv and MobileNet are integrated, and PW-Conv is restricted in the reduction variable identified by the variable D, which resembles Equation (13),

$$D = \frac{f_s * f_s * \omega * \alpha f_m + \omega * \rho * \alpha f_m * \alpha f_m}{f_s * f_s * \omega * \rho * f_m * f_m} \quad (13)$$

The resolution multiplier and width multiplier both contribute to adjusting the window area for precise prediction in various circumstances.

4 Results and discussion

In this section, the performance analysis and comparative are discussed in detail. The proposed EHA-DL experiments are performed in Anaconda using an Intel Core i7 processor running at 3.40 GHz and 8 GB of RAM. This subsection has been divided into the following: dataset preparation, evaluation metrics, and analyses.

4.1 OBS network dataset description

Numerous BHP DDoS assaults on OBS networks are documented in the OBS Network Dataset [19]. The goal class label has 21 attributes, and there are 1,075 instances.

Table 1: Number of instances for each class in the OBS network dataset.

Class Label	MB-No block	MB-wait block	B Block	M B block	Total
Number of instances	500	300	120	155	1075

Is target label has four different class kinds, including Behaving block (B block), misbehaving no block (MB-No block), Mis behaving block (MB block), and Misbehaving-wait block (MB-wait block). Every feature in the dataset has a numeric value aside from the node state feature. The test dataset makes up 25% of the total data, while the training dataset makes up 75%. Table 1 shows the number of instances for each class in the dataset.

4.2 Evaluation metrics

The effectiveness of the suggested technique was evaluated using various parameters, including specificity, recall, F1 score, accuracy, and precision based on the datasets gathered.

Accuracy is the proportion of the test set that was accurately predicted. The specificity, also known as the true negative rate, is a measure of how many negatives are accurately predicted. A recall also known as true positive rate or sensitivity gauges the percentage of positives that are accurately anticipated. How many of the precision measures that an algorithm predicted to be positive truly. F-measure calculates a suggested method's performance by allowing for both recall and precision.

$$Accuracy(A) = \frac{TP + TN}{all\ samples} \quad (14)$$

$$Specificity(S) = \frac{TN}{TN + FP} \quad (15)$$

$$Precision = \frac{TP}{TP + FP} \quad (16)$$

$$Recall(R) = \frac{TP}{TP + FN} \quad (17)$$

$$F\ measure = \frac{P \times R}{P + R} \quad (18)$$

Where, false positives and negatives of the sample data are denoted by FP and FN instead of true positives and negatives (TP and

TN), respectively. Table 2 and Fig. 3 both provide visual representations of the effectiveness of the suggested approach for categorizing various BHP flooding attack types.

Table 2: Performance analysis of the proposed EHA-DL

Parameters	MB-No block	MB-wait block	B Block	MB block
Accuracy	98	98.32	99.54	99.15
Specificity	97.25	96.25	99.15	98.45
Recall	98.21	98.25	99.47	97.54
Precision	97.42	97.64	98.25	96.18
F measure	98.75	97.56	99.05	97.25

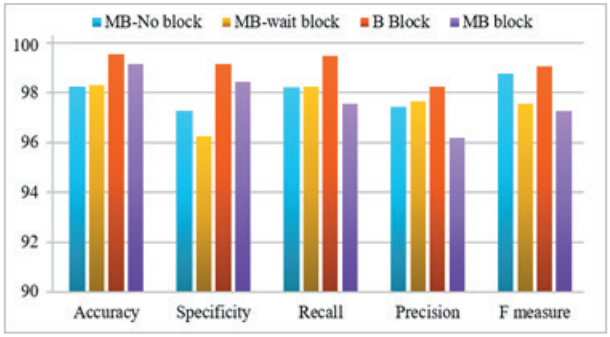

Figure 3: Graphical representation of different BHP flooding attack

Table 1 shows the performance of the proposed EHA-DL for categorizing the various kinds of BHP flooding attacks, including MB-wait block, NB-No block, B block, and MB block. The precision, specificity, recall, accuracy, and f1 score serve as the success metrics. For the OBS dataset, the suggested approach achieves an overall accuracy of 99.24%. The overall performance of the EHA-DL is depicted in fig 3.

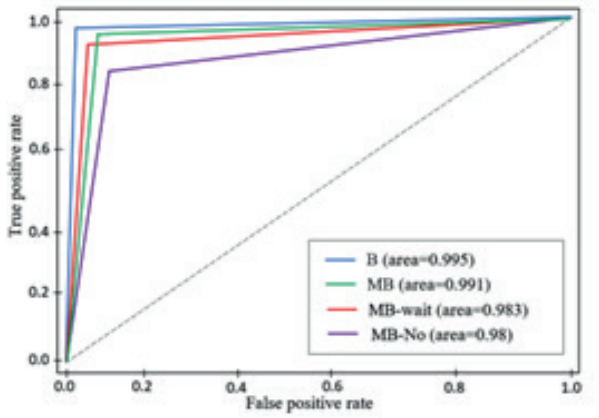

Figure 4: ROC curve of the proposed EHA-DL

Using the collected dataset that yields a higher AUC, the ROC computed for the various classes of HE is shown in Figure 4. AUC values of 0.995 for B, 0.991 for MB, 0.983 for MB-wait, and 0.98 for MB-no blocks were obtained by the proposed EHA-DL network, which can be evaluated using TPR and FPR parameters.

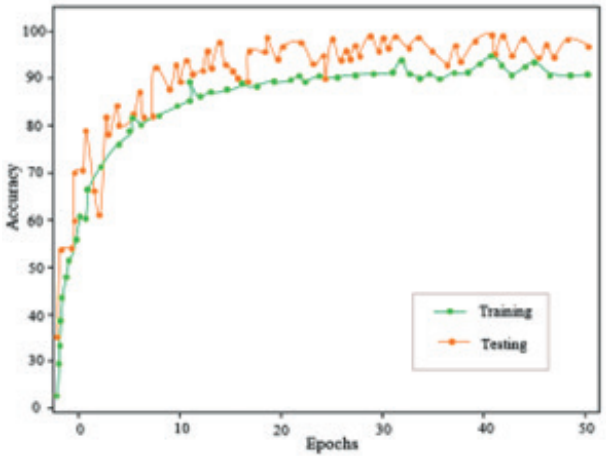

Figure.5: Accuracy curve of the proposed EHA-DL

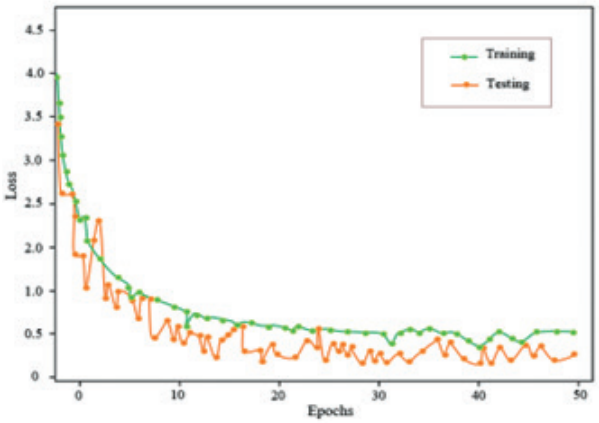

Figure 6: Loss curve of the proposed EHA-DL

The accuracy range is plotted on the vertical axis and the number of epochs on the horizontal axis to depict the accuracy curve in Figure 5. The accuracy of EHA-DL grows with the number of epochs. When the number of epochs is increased, the loss of the EHA-DL is shown in Figure 6. For identifying the various classes of BHP flooding attacks using the dataset, the proposed EHA-DL gets a high accuracy range. To achieve the highest possible testing precision, this study first calculated the number of training epochs required. As a result of achieving a testing accuracy of 99.15% with a small error rate, the findings show that the classification accuracy of EHA-DL was attained after 50 training epochs.

4.3 Comparative analysis

The effectiveness of the proposed EHA-DL achieves high accuracy in its findings. The suggested EHA-DL

was evaluated in comparison to other methods, including the Gaussian Mixture Model (GMM) [18], DCNN [15], K-mean algorithm [16], and PSO-SVM [20].

Table 3: Comparison of the proposed technique with existing techniques

Techniques	Accuracy (%)	Specificity (%)	Recall (%)	Precision (%)	F measure (%)
GMM	83.45	80.32	79.05	85.66	77.58
DCNN	88.25	86.44	90.15	82.42	85.38
K-mean	90.21	92.1	88.54	89.71	86.22
PSO-SVM	95.02	93.42	94.85	92.15	96.69
Proposed EHA-DL	99.27	97.75	98.35	97.37	98.15

The suggested EHA-DL's accuracy of 99.5%, which is better than the existing technique, was evaluated using a variety of metrics, including specificity, precision, recall, F measure, and accuracy of each existing technique. Table 3 shows the comparative analysis of the proposed with state-of-the-art method.

Figure 7 shows the comparative analysis of the proposed novel Elephant herd algorithm based Deep learning network approach (EHA-DL) and Existing methods GMM [18], DCNN [15], K-mean algorithm [16], and PSO-SVM [20] methods. The comparative analysis indicates that the proposed EHA-DL outperforms the current methodologies. While the accuracy of current models such as GMM has 83.45%, DCNN has 87.25%, K-mean is 90.21%, and PSO-SVM is 95.02%, the suggested EHA-DL has a maximum accuracy of 99.27%. It illustrates that the suggested method is efficient and produces a very precise result.

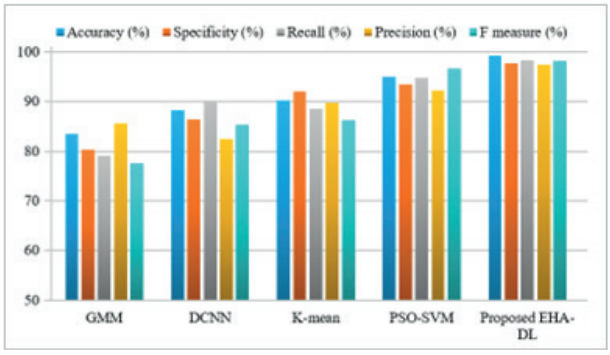

Figure 7: Comparative analysis of the proposed with the existing method

The current GMM, DCNN, K-mean algorithm, and PSO-SVM approaches have raised the precision of the proposed EHA-DL by 10.4%, 8.8%, 6.2%, and 3.6%. The application of extensive classification from a sizable database is what accounts for the improved precision. The suggested EHA-DL has a recall that is 11.4%, 9.6%, 7.2%, and 2.7% higher than the current techniques. When compared to the current approaches, the highest specificity value of 97.75% for the suggested EHA-DL is comparatively high.

5 Conclusion

In this research, a novel Elephant herd algorithm-based Deep learning network has been proposed for detecting BHP flooding attacks. The proposed method is categorized into three phases: pre-processing, feature selection, and classification. The EHA is used to select the most crucial features after pre-processing the raw data to increase the effectiveness of the model. To decrease overfitting and increase detection accuracy, a MobileNet is used to construct the model for the classification phase using the select features of BHPs. Evaluation measures like precision, accuracy, specificity, recall, and f-measure were utilized to calculate the effectiveness of the proposed method. The proposed EHA-DL approach technique acquired a 99.27% accuracy which is relatively high compared to the existing method. In optical burst switching networks, the method effectively and highly efficiently detects flooding assaults and maintains network stability. The suggested framework is being extended, and the thorough design and assessment will be covered in future projects.

6 Acknowledgments

The authors would like to thank the reviewers for all of their careful, constructive and insightful comments in relation to this work.

7 Conflict of Interest Statement

The authors declare that they have no conflict of interest.

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Arrived: 07. 06. 2023
Accepted: 06. 12. 2023

Original scientific paper
https://doi.org/10.33180/InfMIDEM2023.305

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 53, No. 3(2023), 177 – 189

Minimum Component Truly Mixed Mode First Order Universal Filter Employing EXCCTA

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Abstract: A mixed mode first order universal filter (FO-UF) has been proposed in this study. One Extra X Current Conveyor Transconductance Amplifier (EXCCTA), one capacitor and two resistors are used to design the filter. The main attributes of the filter include (i) electronic tunability (ii) ability to work in all four modes of operation (iii) cascadability (iv) availability of low pass (LP), high pass (HP) and all pass (AP) responses simultaneously. By incorporating the filter to design the second order current mode and trans-admittance mode filters, the filter's practicability is investigated. To determine how component spread and frequency-dependent current and voltage transfer gains affect the filter's operation, non-ideal analysis is conducted. The layout of the EXCCTA occupies an area of 51.47*23.33µm2 and it is designed and validated using 180nm GPDK in Cadence software. The FO-UF functions at ±1.25V supply at a frequency of 16.23MHz. Experimental analysis using off the shelf integrated circuits (ICs), the AD844 and CA3080 is also conducted to validate the proposed design.

Keywords: current mode; filter; current conveyor; universal filter; analog

Minimalna komponenta mešanega načina univerzalnega filtra prvega reda z uporabo EXCCTA

Izvleček: V študiji je predlagan univerzalni filter prvega reda (FO-UF) z mešanim načinom delovanja. Za zasnovo filtra so uporabljeni ojačevalnik EXCCTA (Extra X Current Conveyor Transconductance Amplifier), kondenzator in dva upora. Glavne lastnosti filtra so: (i) elektronska nastavljivost (ii) sposobnost delovanja v vseh štirih načinih delovanja (iii) kaskadnost (iv) razpoložljivost odzivov nizke prepustnosti (LP), visoke prepustnosti (HP) in vseh prepustnosti (AP) hkrati. Z vključitvijo filtra v zasnovo tokovnega režima drugega reda in filtrov s prehodno prepustnostjo je raziskana praktična uporabnost filtra. Da bi ugotovili, kako razširjenost komponent in od frekvence odvisni tokovni in napetostni prenosni dobički vplivajo na delovanje filtra, je izvedena neidealna analiza. Postavitev EXCCTA zavzema površino 51,47*23,33 µm2 ter je zasnovana in potrjena z uporabo 180 nm GPDK v programski opremi Cadence. FO-UF deluje pri napajanju ±1,25 V in frekvenci 16,23 MHz. Za potrditev predlagane zasnove je izvedena tudi eksperimentalna analiza z uporabo razpoložljivih integriranih vezij AD844 in CA3080.

Ključne besede: tokovni način; filter; tokovni ojačevalnik; univerzalni filter; analogni

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How to cite:
S. Perumal et al., "Minimum Component Truly Mixed Mode First Order Universal Filter Employing EXCCTA", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 53, No. 3(2023), pp. 177–189

1 Introduction

Any signal processing system must have universal active frequency selective filters as a fundamental component. The analog active filters are employed to carryout multiple signal processing tasks like noise removal, phase correction, avoid aliasing by analog to digital converters (ADCs) or digital to analog converters (DACs). They are also an integral part of audio processing, telecommunications, and instrumentation systems. The analog filters [1-2] are also employed in image processing for removing noise or sharpening edges of the images. Current mode (CM) active components are the most favoured for the construction of multifunction filters because they have higher order linearity, a wider bandwidth, a straightforward design, and better performance in LVLP conditions [3–4]. The all-pass filters are utilised in the construction of multiphase oscillators, high quality factor (Q) bandpass filters, and for phase correction and equalization [5, 6]. Differential voltage current conveyor (DVCC) [15], operational transconductance amplifier (OTA) [6], inverting-current conveyor (ICCII) [8–9], current differencing transconductance amplifiers (CDTA) [18] and second-generation voltage conveyor (VGC) [6] are a few examples of analog active blocks (ABBs) used in the design. Many first order universal or all pass filter topologies can be found in the literature[5-37]. Table 1 presents the comparative analysis of some filters reported in the literature. Mixed-signal processing systems require interaction between current-mode and voltage-mode (VM) circuits. This requirement can be met by employing transadmittance-mode (TAM) and transimpedance-mode (TIM) circuits that not only perform signal processing, but also facilitate distortion-free interfacing between CM and VM units with the advancement of technology mixed-mode systems are being developed which require the interaction between CM and VM circuits by acting as a bridge. The mixed-mode first order universal filter that can provide LP, HP and AP filter functions in CM, VM, TAM and TIM modes of operation is needed for mixed signal system implementation.

It is found during the study that the filters presented in [6-9, 11-12, 16, 23, 31, 36, 37] utilizes more than one active block. The designs in [14, 15, 19, 20, 23, 27, 30-32] require three or more passive components. Floating passive elements are necessary for the filter architectures in [7-10, 12, 13, 15, 20, 23, 30-32]. The filter designs found in [5, 27] involve use of several capacitors. The literature review suggests that the majority of filters have the following flaws (i) large numbers of active analog blocks (ii) operation in a single mode (iii) excessive use of passive elements (iv) use of floating passive components (v) lack of on chip tuning.

In this study, we present a single mixed mode first order universal filter based on the extra X current conveyor transconductance amplifier (EXCCTA) [33] that can generate all three filter responses concurrently. The suggested filter can function in trans-admittance (TAM), trans-impedance (TIM), voltage mode (VM), and current mode (CM).

2 Proposed EXCCTA mixed mode universal filter

The EXCCTA is a versatile active analog block [33] that has inbuilt tunability property. The functional diagram of EXCCTA is presented Figure 1 and the current-voltage relations are given by Equations (1-4).

$$V_{XP} = V_{XN} = V_Y \tag{1}$$

$$I_{XP} = I_{ZP+} = -I_{ZP-} \tag{2}$$

$$I_{XN} = I_{ZN+} = -I_{ZN-} \tag{3}$$

$$I_{O+} = -I_{O-} = g_m\left(V_{ZP+}\right) \tag{4}$$

The designed EXCCTA mixed mode filter is presented in Figure 2. The design requires one EXCCTA, one capacitor and two resistors for implementation. The resistors are implemented using MOSFET based active resistors [34]. The filter operates in all four modes without requiring any change in the topology.

The filter key characteristics are (i) electronic tunability (ii) operation in all four modes (iii) cascadability (iv) usage of a limited number of active blocks and passive components (v) low input impedance in CM and TIM operation (vi) high input impedance in VM and TAM operation (vii) simultaneous availability of LP, HP, and AP responses. Equations (5–17) give the filter transfer function for each of its four operating modes.

The expression for pole frequency is given in Equation 11. It can be concluded for the transfer function analysis for VM, TAM and TIM modes that the filter gain can be adjusted by changing the value of the resistor without disturbing the frequency. The resistors can be implemented using MOSFETS making the frequency and gain electronically tunable.

2.1 Operation in CM and TAM

In CM operation the filter did not require any resistors for implementation. In the TAM mode of operation, the

Table 1: Comparative analysis of first order filters

Reference	Number of Active Block	Passive components count		Low input impedance (CM /TIM) or High input impedance (VM/TAM)	High output impedance (CM/ TAM) or Low output impedance (VM/TIM) for AP response	Tunability	Mode of Operation	Universal Filter	Employment of Floating Passive Components
		R	C						
[5]	DXCCTA-1	0	2	Yes	Yes	Yes	CM	Yes	No
[6]	OTA-2	1	1	Yes	No	Yes	VM	Yes	No
[7]	CCII-2	1	1	Yes	Yes	No	CM	Yes	Yes
[8]	ICCII-2	1	1	No	Yes	No	CM	No	Yes
[9]	ICCII-2	0	1	No	Yes	Yes	CM	Yes	Yes
[10]	DXCCDITA-1 (APF-1)	0	1	Yes	Yes	Yes	VM	No	Yes
[11]	MO-CCII-2	1	1	Yes	Yes	No	CM	Yes	No
[12]	Subtractor-2	1	1	Yes	Yes	No	VM	No	Yes
[13]	ZC-VDCC (Fig.2)-1	1	1	No	Yes	Yes	CM	No	No
[14]	DV-DXCCII-1	3	1	Yes	No	No	VM	No	Yes
[15]	DVCC-1	2	1	Yes	No	No	VM	Yes	Yes
[16]	CCII-2	1	1	Yes	Yes	No	CM	No	No
[17]	DXCCTA-1	0	1	Yes	Yes	Yes	CM	No	No
[18]	CDTA-1	0	1	Yes	Yes	Yes	CM	No	No
[19]	DXCCII-1 (Fig.2)	2	1	Yes	No	No	VM	No	No
[20]	DVCC-1	2	1	No	Yes	No	VM	No	Yes
[21]	VCII-2	3	1	Yes	Yes	No	VM/CM	No	Yes
[27]	DX-MOCCII	2	2	No	Yes	No	CM	Yes	No
[30]	CFOA-2 (Fig.1 a)	3	1	No	Yes	No	VM	No	Yes
[31]	VCII-2	2	1	Yes	Yes	No	VM/CM	Yes	Yes
[32]	LT-1228-1	2	1	No	Yes	Yes	VM	Yes	Yes
[34]	EXCCTA-1	0	1	Yes	Yes	Yes	CM	Yes	No
[35]	VDDDA-1	0	1	Yes	Yes	Yes	VM	Yes	No
[36]	DDTA-2	1	1	Yes	Yes	Yes	VM	Yes	No
[37]	CCCII-2	0	1	Yes	Yes	Yes	CM	Yes	No
Proposed	EXCCTA-1	1	1	Yes	Yes	Yes	CM, VM, TAM, TIM	Yes	No

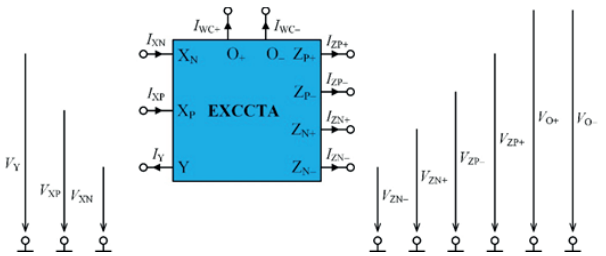


Figure 1: Functional diagram of EXCCTA

filter employs one active resistor (R_1) for voltage to current conversion. In both CM and TAM modes the filter provides all three responses simultaneously. The transfer functions and relation of pole frequency for LP, HP and AP responses are given by Equations (5-11).

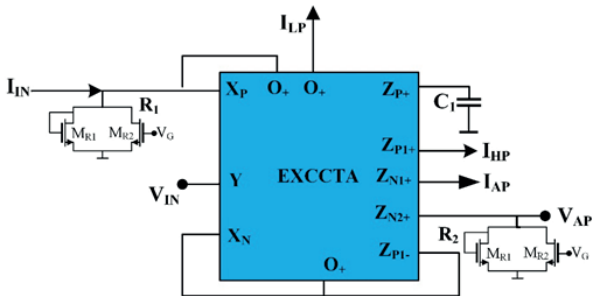


Figure 2: Mixed Mode First Order universal filter

$$I_{HP(CM-Mode)} = \frac{-sC}{sC + g_m} \tag{5}$$

$$I_{LP(CM-Mode)} = \frac{-g_m}{sC + g_m} \quad (6)$$

$$I_{AP(CM-Mode)} = -\left[\frac{sC - g_m}{sC + g_m}\right] \quad (7)$$

$$I_{HP(TAM-Mode)} = \frac{1}{R_1} * \left[\frac{sC}{sC + g_m}\right] \quad (8)$$

$$I_{LP(TAM-Mode)} = \frac{1}{R_1} * \left[\frac{-g_m}{sC + g_m}\right] \quad (9)$$

$$I_{AP(TAM-Mode)} = \frac{1}{R_1} * \left[\frac{sC - g_m}{sC + g_m}\right] \quad (10)$$

$$f_o = \frac{1}{2\pi} * \left[\frac{g_m}{C}\right] \quad (11)$$

It can be seen from Equations (8-10) that the gain of the TAM filter is $(H_o = \frac{1}{R_1})$ that can be tuned by varying the resistance value of the active resistor. In TAM configuration the filter offers dual tunability of frequency and gain.

2.2 Operation in VM and TIM

In the TIM mode of operation, the input will be current, and the output will be voltage. To operate in this mode the filter requires one active resistor at the output for current to voltage conversion. For the sake of simplicity only AP voltage output responses are shown in the Figure 2. The same process will be followed to get LP and HP responses. Since the active MOSFET resistors require less chip area it will have negligible effect on the chip area.

In VM mode operation two resistors are required, one at the input side and other at the output. As is clear from Equations (12-17). The VM and TIM modes offer dual tunability. The filter frequency can be controlled by OTA transconductance (g_m) and gain can be changed by active resistors (R_2/R_1). For VM mode the filter gain $(H_o = \frac{R_2}{R_1})$ and for TIM the gain is ($H_o = R_2$).

$$V_{HP(VM-Mode)} = \frac{R_2}{R_1} * \left[\frac{sC}{sC + g_m}\right] \quad (12)$$

$$V_{LP(VM-Mode)} = \frac{R_2}{R_1} * \left[\frac{-g_m}{sC + g_m}\right] \quad (13)$$

$$V_{AP(VM-Mode)} = \frac{R_2}{R_1} * \left[\frac{sC - g_m}{sC + g_m}\right] \quad (14)$$

$$V_{HP(TIM-Mode)} = -R_2 * \left[\frac{sC}{sC + g_m}\right] \quad (15)$$

$$V_{LP(TIM-Mode)} = -R_2 * \left[\frac{-g_m}{sC + g_m}\right] \quad (16)$$

$$V_{AP(TIM-Mode)} = -R_2 * \left[\frac{sC - g_m}{sC + g_m}\right] \quad (17)$$

3. Non-ideal analysis of the filter

The major contributing factors for the deviation in frequency performance of the EXCCTA are the frequency dependent current and voltage transfer gains, $\boldsymbol{\alpha}_i(s)$ and $\beta_i(s)$ respectively, where $\alpha(s) = \alpha_0/(1 + s/\omega_\alpha)$ and $\beta(s) = \beta_0/(1 + s/\omega_\beta)$. Ideally, $\alpha_0 = \beta_0 = 1$ and $\omega_\alpha = \omega_\beta = \infty$. The γ symbolizes the inaccuracy in the transconductance transfer of the OTA. If the non-ideal gains are considered the V-I relationships of the EXCCTA are transformed to $I_Y = 0$, $V_{XP} = \beta_P(s)V_Y$, $V_{XN} = \beta_N(s)V_Y$, $I_{ZP+} = \alpha_p(s)\, I_{XP}$, $I_{ZP-} = \alpha_p'(s)\, I_{XP}$, $I_{ZN+} = \alpha_N(s)\, I_{XN}$, $I_{ZN-} = \alpha_N'(s)\, I_{XN}$, $I_{0+} = \gamma g_m V_{ZP+}$, $I_{0-} = \gamma' g_m V_{ZP+}$.

The reanalysis of the all-pass filter including the effect of frequency dependent current and voltage transfer gains results in the modified transfer functions and pole frequency expression as presented in Equations (18-20). For the sake of brevity only non-ideal AP responses of all modes are included.

$$I_{AP(CM-Mode)} = -\frac{sC\alpha_N\alpha_P\beta_P - \alpha_P\alpha_N\beta_P\gamma' g_m}{sC + \alpha_P\gamma' g_m} \quad (18)$$

$$I_{AP(TAM-Mode)} = \frac{1}{R_1} * \frac{sC\alpha_N\alpha_P\beta_P - \alpha_P\alpha_N\beta_P\gamma' g_m}{sC + \alpha_P\gamma' g_m} \quad (19)$$

$$V_{AP(VM-Mode)} = \frac{R_2}{R_1} * \left[\frac{sC\alpha_N\alpha_P\beta_P - \alpha_P\alpha_N\beta_P\gamma' g_m}{sC + \alpha_P\gamma' g_m} \right] \quad (20)$$

$$V_{AP(TIM-Mode)} = -R_2 * \left[\frac{sC\alpha_N\alpha_P\beta_P - \alpha_P\alpha_N\beta_P\gamma' g_m}{sC + \alpha_P\gamma' g_m} \right] \quad (21)$$

$$f_o = \frac{1}{2\pi} * \left[\frac{\alpha_P\gamma' g_m}{C} \right] \quad (22)$$

4. Simulation results

The EXCCTA employed in the design of FO-UF is designed in 180nm GPDK in Cadence Virtuoso analog design environment at a supply voltage of ±1.25V. The CMOS implementation of EXCCTA is presented in Figure 3. The width and length of the EXCCTA transistors can be found in [34]. The width to length ratio of MOSFET active resistors are 8.6 µm /1.8µm. The layout of the EXCCTA is designed and verified as presented in Figure 4. It occupies an area of 51.47*23.33µm^2.

4.1 Analysis of the first order universal filter:

By fixing I_{Bias} = 100µA and C_1 = 10pF, the filter is configured for a frequency of 16.23MHz. First, the CM operation is examined. The input is applied at the X_p terminal, while the Y node is connected to ground. Figure 5 presents the ideal and simulated LP and HP responses. Figure 6 shows the AP configuration gain and phase response. The AP gain and phase response for various bias currents are presented in Figure 7 to demonstrate the filter tunability property. Figure 8 depicts the Lissajous curve to further verify the phase relationship between the input and output signals. The illustration shows that there is a 90° phase difference between the input and output signals. The filter transient analysis performance for an input sinusoidal signal of 40µA (p-p) at a frequency of 16.23 MHz is shown in Figure 9. The Monte Carlo mismatch analysis is done by incorporating the models provided in the GPDK for MOSFETs and MIM Capacitor, the statistical analysis is performed for 200 runs to examine the impact of process variables on the performance of the filter. The results presented in Figure 10 show satisfactory performance with little variation. The total harmonic distortion (THD) of the CM AP configuration is measured for different input signal amplitudes. The Figure 11 shows that the THD remains within acceptable range till 80µA input range.

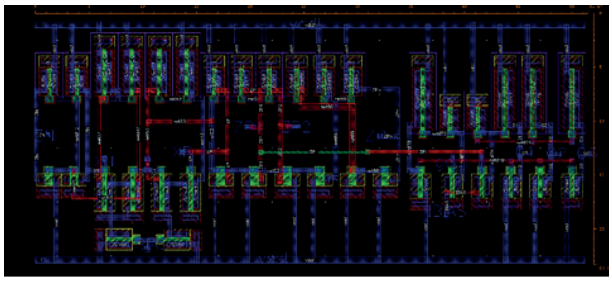


Figure 4: The layout of EXCCTA in 180nm technology

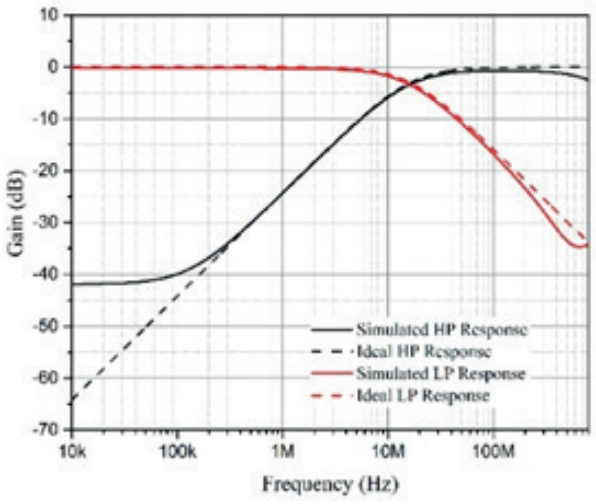


Figure 5: Frequency responses of CM HP and LP configuration

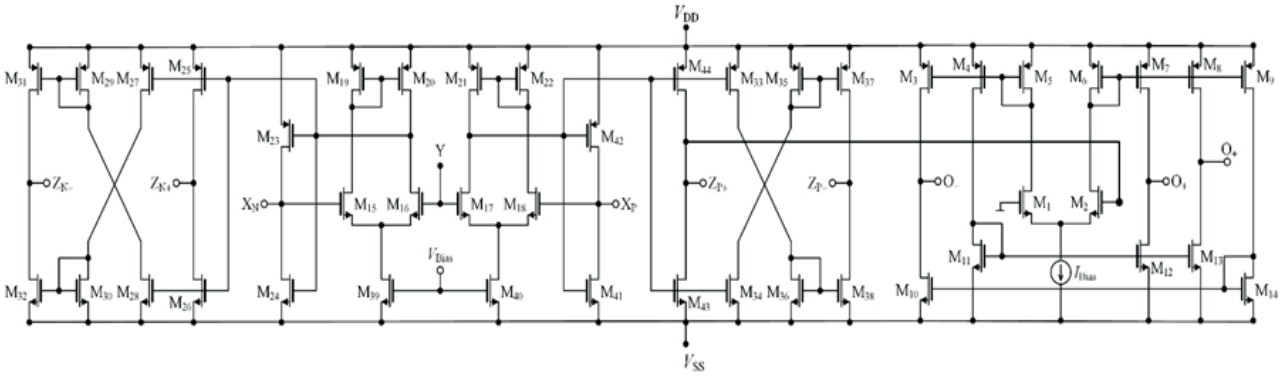


Figure 3: The CMOS implementation of EXCCTA

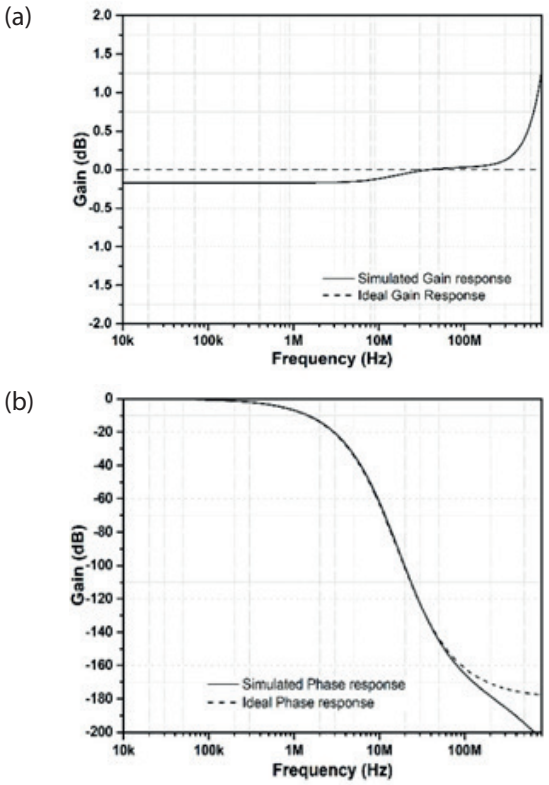


Figure 6: Frequency response of CM AP configuration: (a) Gain (b) Phase

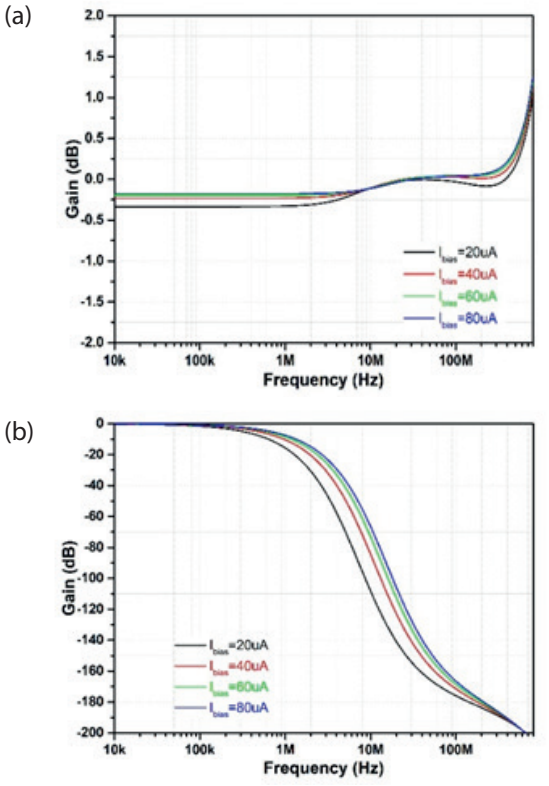


Figure 7: Tunability of CM AP response for different values of bias currents: (a) Gain (b) Phase

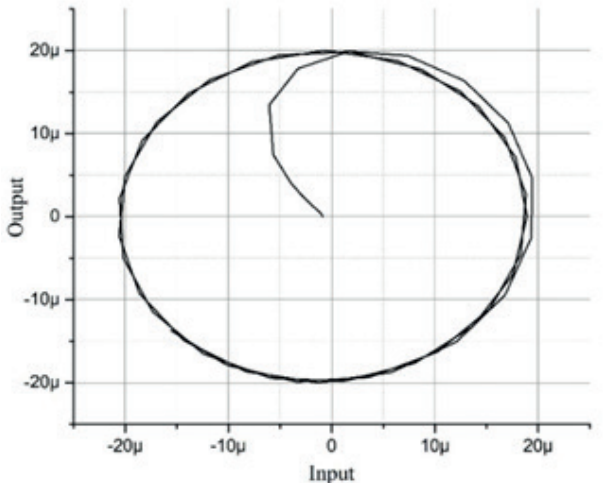


Figure 8: Lissajous patters for CM AP configuration

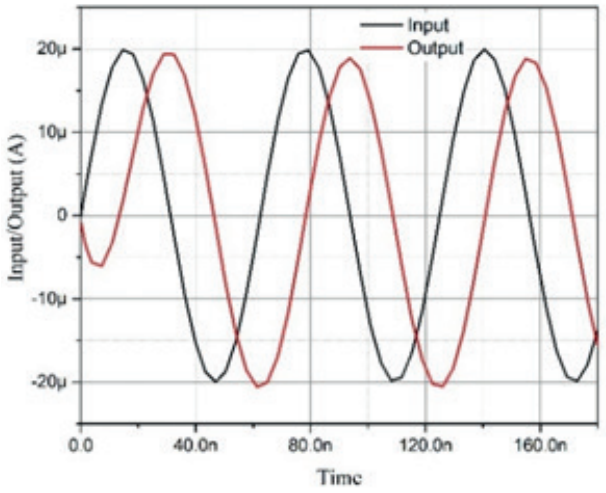


Figure 9: Time domain analysis of CM AP configuration

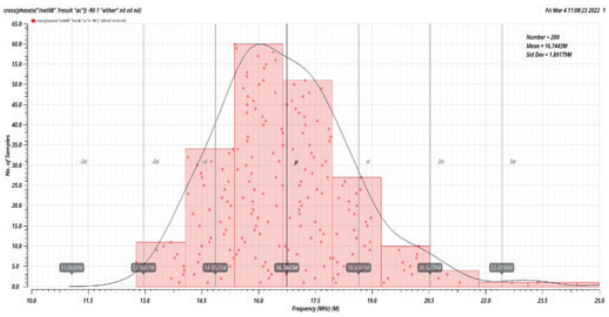


Figure 10: Monte Carlo analysis of CM AP configuration

Next, the VM operation of the filter is examined. The input voltage is applied at Y node. The Figure 12 presents the LP and HP response in VM configuration. To obtain the LP and HP gain responses a 1kΩ active MOSFET resistor is attached to the output terminal of the filter. The value of the active resistor can be controlled by setting the control voltage (V_G). The AP gain and

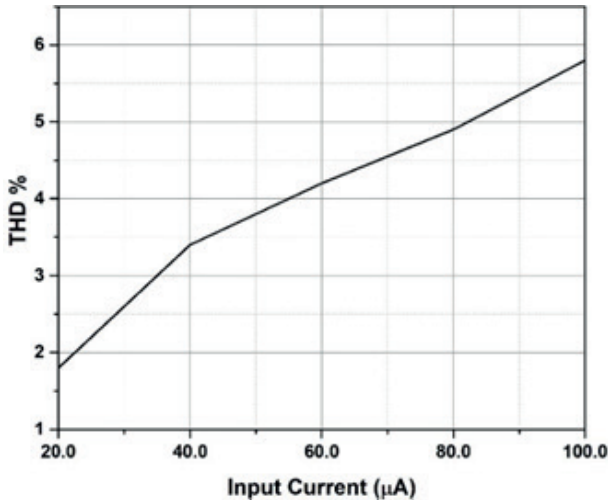


Figure 11: Total harmonic distortion of CM AP configuration

phase responses are presented in Figure 13. The time domain results of an input sinusoidal voltage signal of 400mV(p-p) at 16.23MHz is shown in Figure 14. The Monte Carlo analysis results for 200 runs as presented in Figure 15 indicate negligible effect of process variations on the AP filter response.

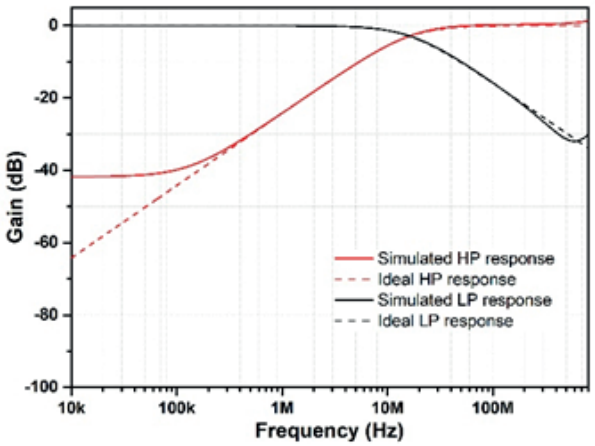


Figure 12: Frequency responses of VM HP and LP configuration

The LP, HP and AP responses for the TAM and TIM configurations are shown in Figures 16-17. The value of the active resistor was set at 1kΩ for the analysis. The analysis of the responses indicates the correct functioning of the designed filter in mixed mode configuration. The THD of the VM AP filter configuration is also measured for different input signal amplitudes. The Figure 18 shows that the THD remains within acceptable range till 160mV input range.

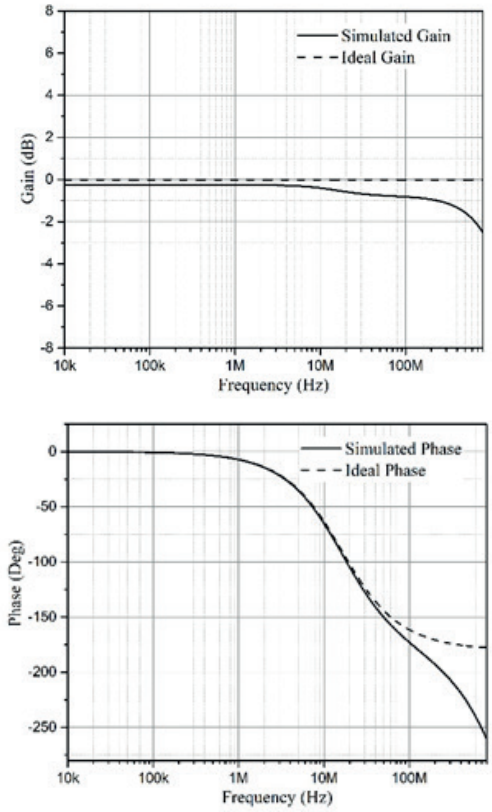


Figure 13: Frequency response of VM AP configuration: (a) Gain (b) Phase

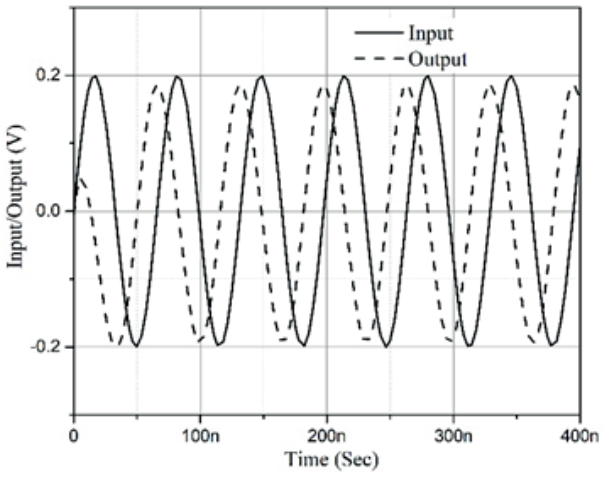


Figure 14: Time domain analysis of CM AP configuration

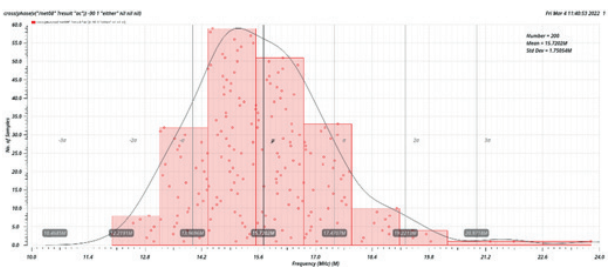
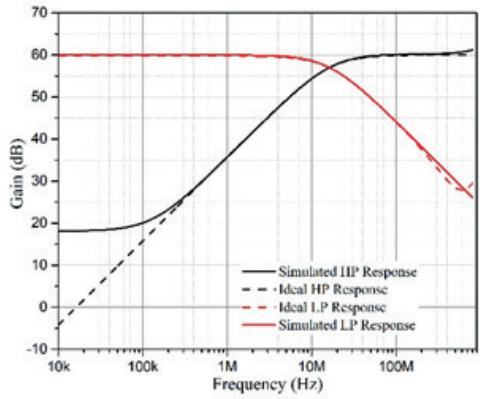


Figure 15: Monte Carlo analysis of VM AP configuration

(a)



(b)

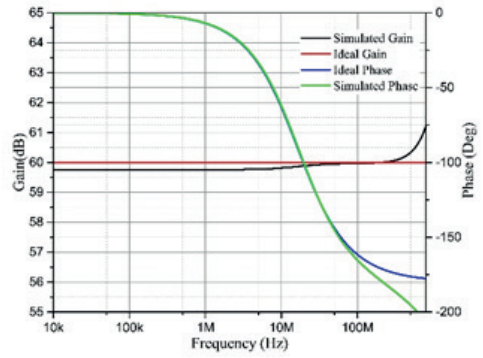
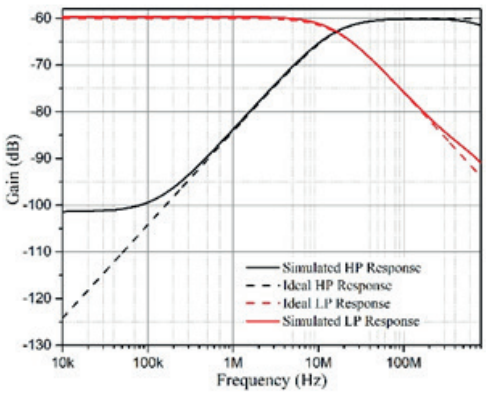


Figure 16: Frequency responses of TIM configuration (a) HP and LP (b) AP

(a)



(b)

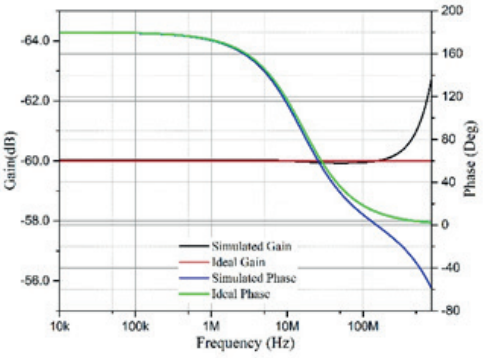


Figure 17: Frequency responses of TAM configuration: (a) HP and LP (b) AP

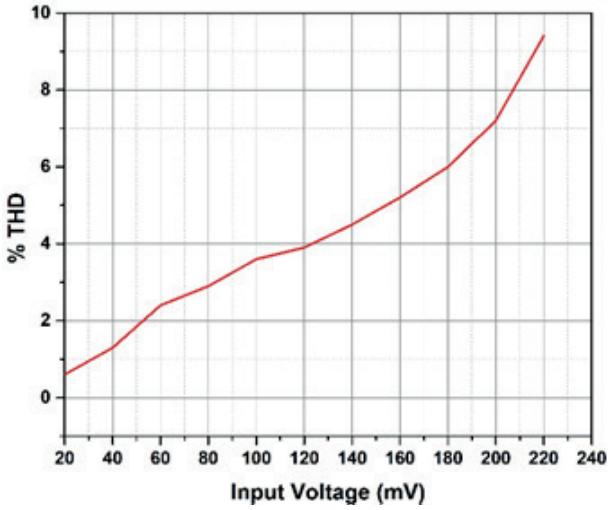


Figure 18: Total harmonic distortion of VM AP configuration

(a)

(b)

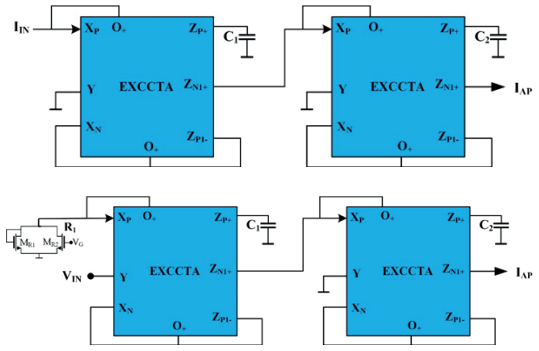


Figure 19: Second order AP filters obtained by direct cascading (a) CM (b) TAM

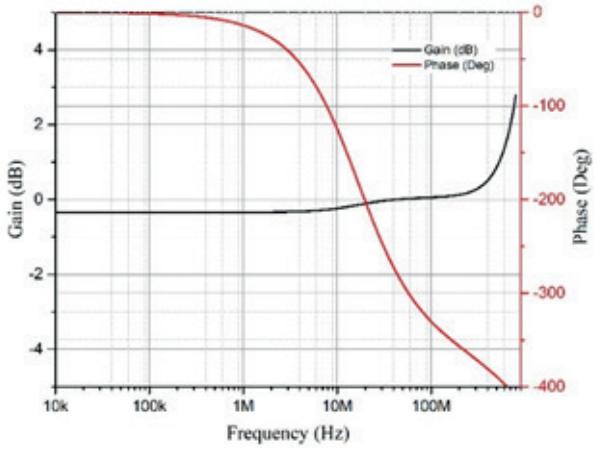


Figure 20: Frequency response of CM Second order AP configuration

4.2 Design of second order CM and TAM Filters

Second order CM and TAM mode filters are designed to verify the cascadeability of the proposed filter. The proposed all pass filter is cascaded together to achieve

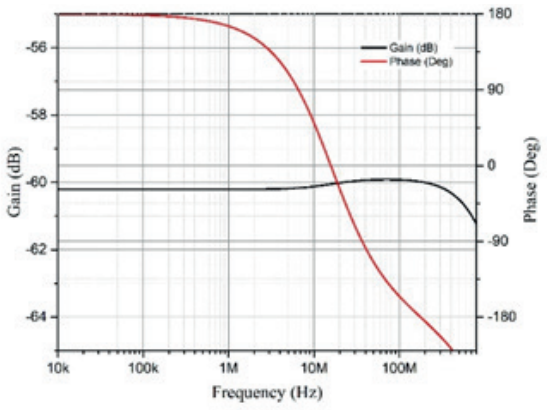


Figure 21: Frequency response of TAM Second order AP configuration

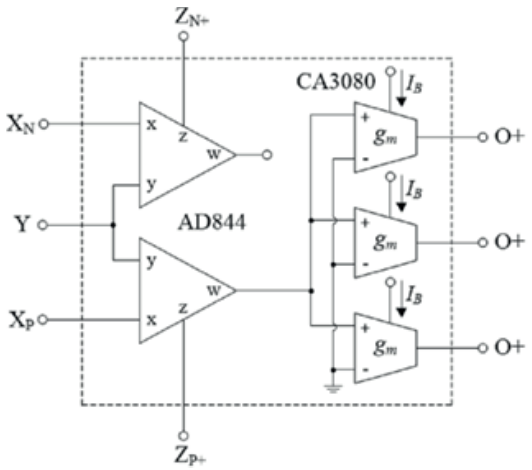


Figure 22: Implementation of EXCCTA using off the shelf ICs

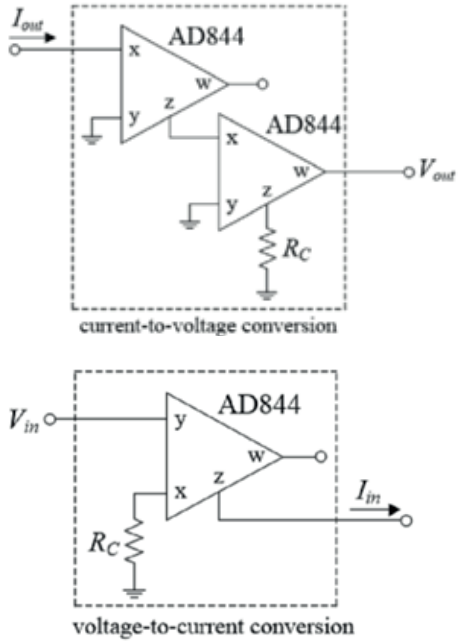


Figure 23: Current to voltage (V-I) and Voltage to current (V-I) converters

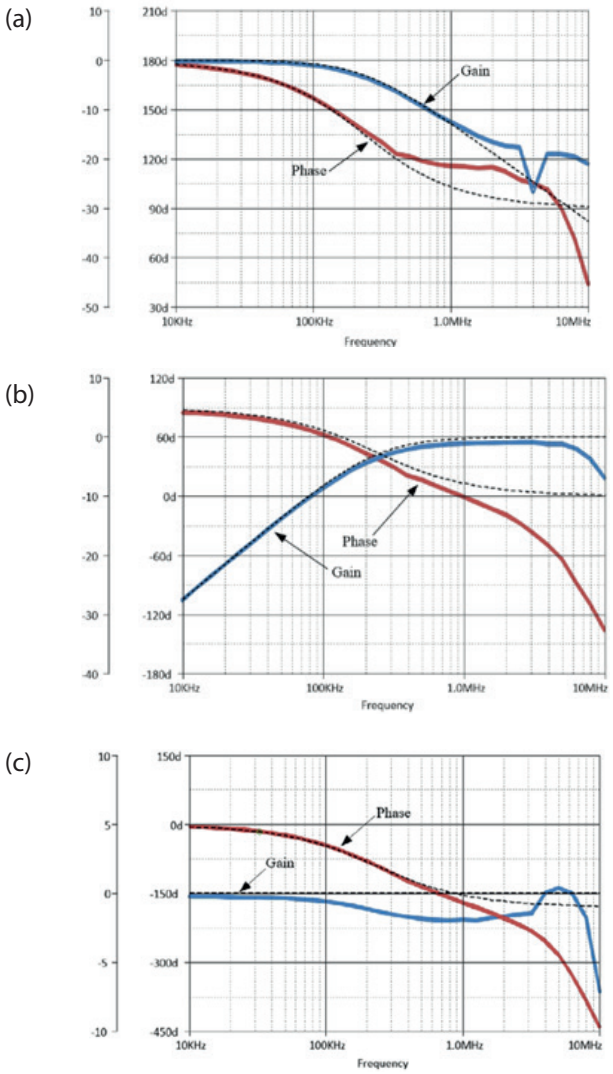


Figure 24: Frequency response of CM configuration: (a) LP (b) HP (c) AP

the second order AP filter as shown in Figure 19(a-b). The second CM and TAM filters are tested at a frequency of 16.23MHz by choosing $C_1 = C_2 = 10$pF and $I_{bias1,2} = 100\mu$A. For $C_1 = C_2 = C$ and $g_{m1} = g_{m2} = g_m$ the pole frequency expression of the filter will be identical to the one given in Equation 11. The Figures 20-21 present the frequency domain results of the designed filters which validates the cascadeability of the filters.

4.3 Experimental analysis

To further establish the practical feasibility of the proposed designs experimental analysis using commercially available integrated circuits AD844 [10] and CA3080 is done. The EXCCTA is realised as presented in Figure 22.

The results are obtained with $g_m = 1$mA/V, $R_1 = 1$kΩ and $C_1 = 680$ pF at supply voltage of ±5V which results in $f_o =$

234.5 kHz. The current to voltage (V-I) and voltage to current (V-I) converters used for obtaining the results are presented in Figure 23. The value of the converting resistance R_C = 1Ω k. A sinusoidal signal of 50mA(p-p) at 234kHz is applied to the filter for testing. The frequency domain results for CM mode LP, HP and AP are presented in Figure 24. The transient analysis results are given in Figure 25. The Fourier transforms results are also shown in Figure 26.

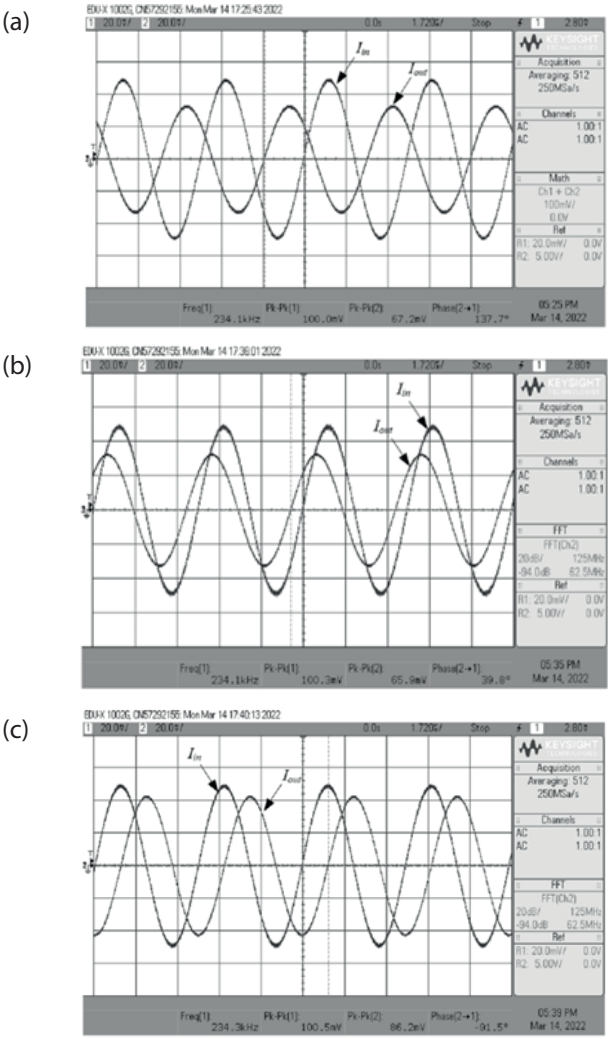
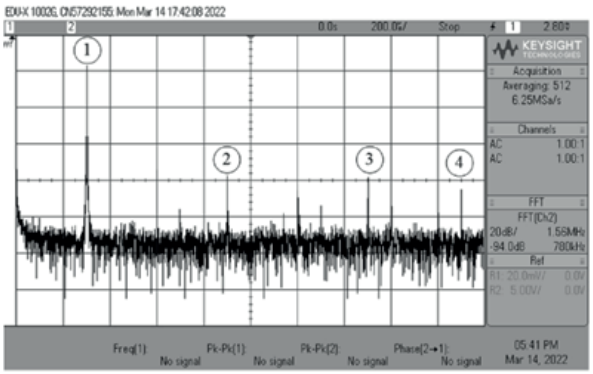


Figure 25: Time domain Analysis of CM configuration: (a) LP (b) HP (c) AP

Similarly, frequency domain results for TAM LP, HP and AP are presented in Figure 27. Analysis of the results reveal that the proposed mixed mode FO-UF works as expected.

5 Conclusion

The manuscript presents a topology of mixed mode first order universal filter using EXCCTA. The filter employs single grounded capacitor and two active MOS-



No.	Frequency (kHz)	Gain (dB)
1	234.05	-33.86
2	704.34	-92.64
3	1173.12	-93.21
4	1486.68	-117.8

Figure 26: Fourier transforms results of CM AP configuration

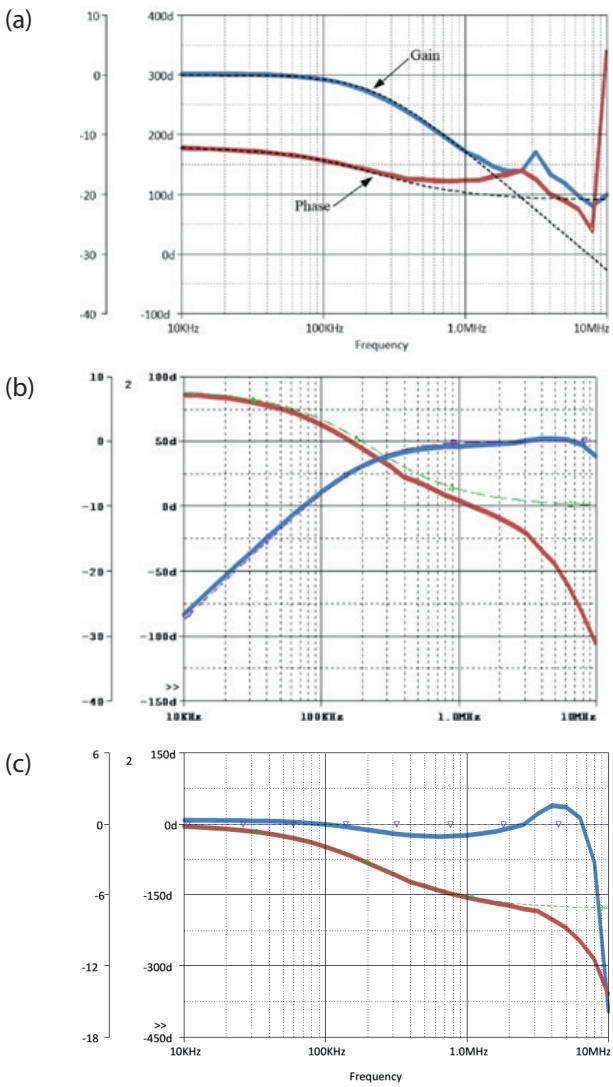


Figure 27: Frequency response of CM configuration: (a) LP (b) HP (c) AP

FET resistors for implementation. The filter can operate in VM, CM, TAM and TIM modes and provide LP, HP and AP responses. The filter is cascadable and did not require any matching condition for passive components. The filter enjoys tunability of filter frequency and gain. The non-ideal gain and sensitivity analysis of the filter is also conducted to gauge their effect on the performance of the filter. The filter is validated at a frequency of 16.23MHz and the layout of the EXCCTA is also designed and verified. The experimental validation using off the shelf ICs is also conducted for the proof of concept.

6 Acknowledgement

This work was financially supported by King Mongkut's Institute of Technology Ladkrabang [2566-02-01-040].

7 Conflicts of Interest

The authors declare no conflict of interest.

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Arrived: 21. 09. 2023
Accepted: 21. 12. 2023

Original scientific paper
https://doi.org/10.33180/InfMIDEM2023.306

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 53, No. 3(2023), 191 – 202

A Comprehensive Strategy for Modelling the Conducted EMI of an Integrated Motor Drive in the Time Domain

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Abstract: The paper introduces a comprehensive strategy for modelling the conducted electromagnetic interference (EMI) of a 48 V 11,2 kW permanent magnet motor drive with an integrated three-phase inverter in the time domain to comply with the CISPR 25 standard. The strategy is based on transient electrical simulations using LTspice® and EMI receiver modelling by signal post-processing in MATLAB®. To extract AC lumped component parameters for electrical simulations of the inverter, the Ansys® Q3D Extractor® environment was employed, while the electrical parameters of the motor side were determined from an impedance analyzer measurement. Two distinct transient simulations were performed and compared, namely a static PWM and a Space Vector Pulse Width Modulation (SVPWM) control strategy, where for the latter the simulation time was chosen to capture one electrical revolution of the motor. For the EMI receiver simulation, a digital Short-Time Fourier Transform (STFT) algorithm, compliant with CISPR 1611, was implemented. The simulation of one electrical revolution of the motor lasted 43 minutes, resulting in the average spectral deviation between the measured and simulated spectrum bandwidth of 3,33 dBµV and 2,58 dBµV for peak and average detectors, respectively. The introduced strategy proposes a straightforward approach for the extraction of parasitic elements. Furthermore, it ensures accurate EMI prediction without compromising simulation time, which is crucial to stay within the timeframe when developing an automotive product.

Keywords: EMI modelling; integrated motor drive; FFT EMI receiver; SVPWM; transient analysis

Celostni pristop k modeliranju prevodnih elektromagnetnih motenj integriranega elektromotorskega pogona v časovni domeni

Izvleček: Članek predstavlja celovito strategijo modeliranja prevodnih elektromagnetnih motenj (EMI) elektromotorskega pogona s trajnimi magneti (48 V, 11,2 kW), ki ima integriran trifazni pretvornik, v skladu s standardom CISPR 25. Strategija temelji na uporabi orodja LTspice® za analizo v časovnem prostoru in na modeliranju EMI sprejemnika s post-obdelavo signalov v okolju MATLAB®. Za pridobivanje parazitnih parametrov, ki so potrebni za električne simulacije pretvornika, je bilo uporabljeno okolje Ansys® Q3D Extractor®, medtem ko so bili električni parametri na strani motorja določeni z impedančnim analizatorjem. Izvedeni in primerjani sta bili dve različni časovni simulaciji. Prva je temeljila na statičnem PWM krmiljenju mostiča, druga pa na pulzno-širinski modulaciji v vektorskem prostoru (SVPWM), pri čemer je bilo za slednjo določeno trajanje simulacije na podlagi zajema enega električnega obrata motorja. Pri simulaciji EMI sprejemnika je bila v skladu s CISPR 16-1-1 implementirana časovno kratka Fourierjeva transformacija (STFT). Simulacija enega električnega obrata motorja je trajala 43 minut. Povprečno odstopanje med merjenim in simuliranim spektrom na frekvenčnem območju zanimanja je za detektor vršne vrednosti znašalo 3,33 dBµV, za detektor povprečne vrednosti pa 2,58 dBµV. Predstavljena strategija predlaga preprost pristop za določanje parazitnih parametrov. Poleg tega zagotavlja zadovoljivo napoved EMI, vendar ne na račun podaljšanja trajanja simulacije, kar je ključno za upoštevanje časovnih omejitev pri razvoju izdelka za avtomobilski trg.

Ključne besede: EMI modeliranje; integriran elektromotorski pogon; FFT EMI sprejemnik; SVPWM; analiza v časovnem prostoru

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How to cite:
K. Saksida et al., "A Comprehensive Strategy for Modelling the Conducted EMI of an Integrated Motor Drive in the Time Domain", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 53, No. 3(2023), pp. 191–202

1 Introduction

During the development phase of an automotive product, strict project timelines and budget limitations must be considered and not taken separately from the technical aspect. Having fewer iteration loops also means using fewer project resources.

Development of an integrated motor drive is a good example, where failing to reach electromagnetic compatibility (EMC) requirements could lead to major correction loops of the entire design. An accurate and fast electromagnetic interference (EMI) prediction is therefore crucial to stay within the project timeline and budget boundaries. To mitigate the simulation time, researchers mainly propose a frequency domain instead of a time domain approach, simply claiming that the time domain simulation takes too long to complete [1]–[3]. However, they do not reveal actual simulation times [4]–[6].

Regardless of the simulation domain, many papers focus on methodologies for the extraction of lumped parameters. Frequently, they focus intensively on a particular component of the system, such as a switching device, PCB, or motor, while oversimplifying other elements. However, they often lack support from a sensitivity study addressing the omitted parameters that influence the EMI spectrum.

In terms of modeling switching devices, authors mainly focus on adequately describing current and voltage transition slopes, recognizing these phenomena as the main source of the EMI [4], [5], [7], [8].

The determination of lumped parameters of a PCB is typically approached in two ways. One method involves analytical techniques, particularly suitable for straightforward geometries. Alternatively, for more intricate structures, such as multilayer configurations, parasitic extraction software is often employed [5].

When modelling a motor, the finite element method (FEM) yields good results; however, managing mechanically complex electrical machine geometries is a time-consuming task [9]. Based on this fact, many researchers propose a method, where a complex motor model is built from different impedance measurements [10]–[15]. Keeping the rotor position in mind, the method is suitable for induction and permanent magnet motors.

Last but not least, in many cases the EMI receiver models are either not implemented or the specifics not documented or referenced, resulting in a questionable comparison of a simulated and measurement results [1]–[6].

This paper proposes a comprehensive strategy for modelling the conducted emissions of an integrated motor drive, ensuring that spectrum accuracy is not compromised by simplifications that lead to simulation time mitigation. The paper indicates the lumped parameters with significant effect to the EMI spectrum and objectively addresses the simulation time duration, aiming to keep it below 1 hour. In conjunction with non-symmetrical parasitic elements, it also evaluates the impact of a motor control strategy implementation on the EMI spectrum. Furthermore, it indicates the minimum simulation time needed to capture all EMI phenomena of an integrated motor drive within the dwell time of the EMI receiver.

The equipment under test (EUT) was MAHLE 48 V 11,2 kW permanent magnet motor drive (see Fig. 1) with an integrated 3phase inverter that must comply with the CISPR 25: 2016 standard for Conducted and Radiated Emissions [16], [17]. The standard prescribes an EUT to operate under typical loading conditions. To simplify the test setup, the EUT was used without a load in a fixed operating point.

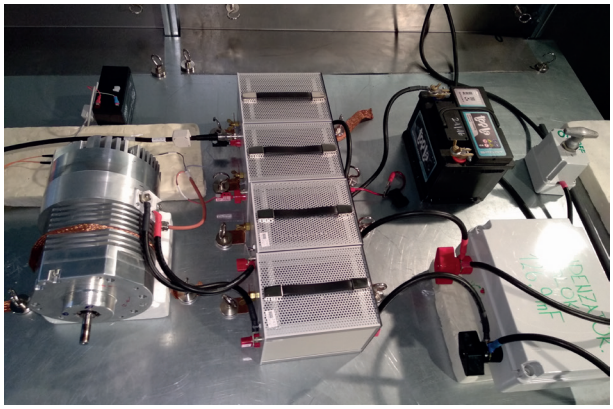

Figure 1: MAHLE 48 V 11.2 kW integrated motor drive with test setup according to CISPR 25.

2 Frequency & time domain approach

SPICE based simulators are commonly used for electronic circuits simulation. Modelling of EMI phenomena consists of modelling the EUT itself as well as the test setup specifics according to an applied standard. Many authors propose to use frequency domain approach which gives almost an instant simulation result, that is spectral density on the measurement node [1]–[3]. This approach usually gives adequate results when simulating low power motor drives where the dimensions and with that all parasitic phenomena are limited to the components themselves.

However, when the dimensions increase and with that nonsymmetrical parasitic elements are introduced, the simplification of the *di/dt* and *du/dt* transients with current and voltage sources respectively, deteriorates simulation accuracy. High power motor drives usually consist of multiple printed circuit board assemblies (PCBAs), where additional parasitic elements are introduced with interfaces between these boards (see Fig. 2).

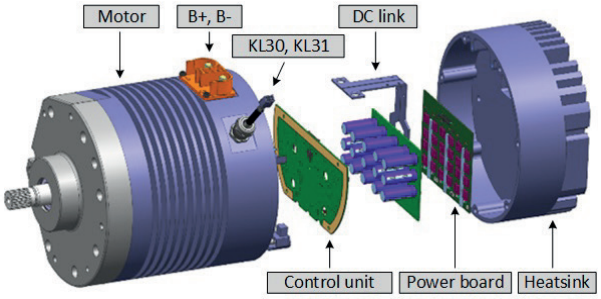

Figure 2: Exploded view of the EUT.

To accurately capture all EMI effects that are influenced by the rotation of the motor itself in the form of different current paths through the non-symmetrical geometry, a transient analysis must be performed, inevitably resulting in longer simulation times. A comparison between both approaches could be seen in the Table 1.

Table 1: Frequency vs. time domain.

Frequency domain	Time domain
(-) EMI receiver functionality (limited implementation)	(+) Complete EMI receiver functionality (IF filter, STFT, detectors, dwell time)
(-) Circuit analysis presumes stationary conditions	(+) Space Vector Pulse Width Modulation
(-) Complex non-linear SPICE models not possible to use	(+) Possibility to use official non-liner SPICE models (e.g., MOSFETs)
(+) Instant simulation results with high convergence	(-) Time consuming simulation with convergence issues

To mitigate long simulation time and convergence issues, a good understanding of the EM spectrum sensitivity to different parasitic components is beneficial. By that, to simplify the model and thus shorten the simulation time, we can exclude those with negligible effect to the spectrum.

3 Modelling

According to the Fig. 3, the LTspice® environment was used to construct an appropriate schematic for transient analysis. Signal post-processing, corresponding to the EMI receiver, was done using MATLAB®.

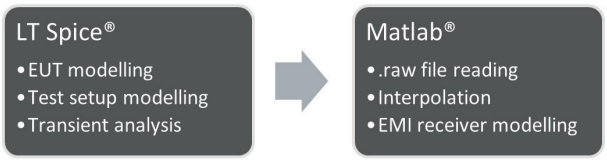

Figure 3: Modelling flow.

The EUT has a dedicated 12 V power supply line for the logic board, which is separate from the main 48 V battery power supply in terms of grounding. This setup enables us to observe and address conductive emissions for each part separately. In this paper, our focus will be solely on the 48 V power stage.

3.1 CISPR 25 test setup

The baseline for the test setup modelling is a reference ground plane with two grounded Artificial Networks (Ans), where the EUT's housing is also grounded with a copper braid (see Fig. 4). This configuration establishes a return path for common-mode (CM) emissions. The power supply lines were 40 cm long, and their inductances are a part of the path for differential mode noise. The mentioned inductances were calculated analytically based on their geometry according to CISPR 16-2-1 [18].

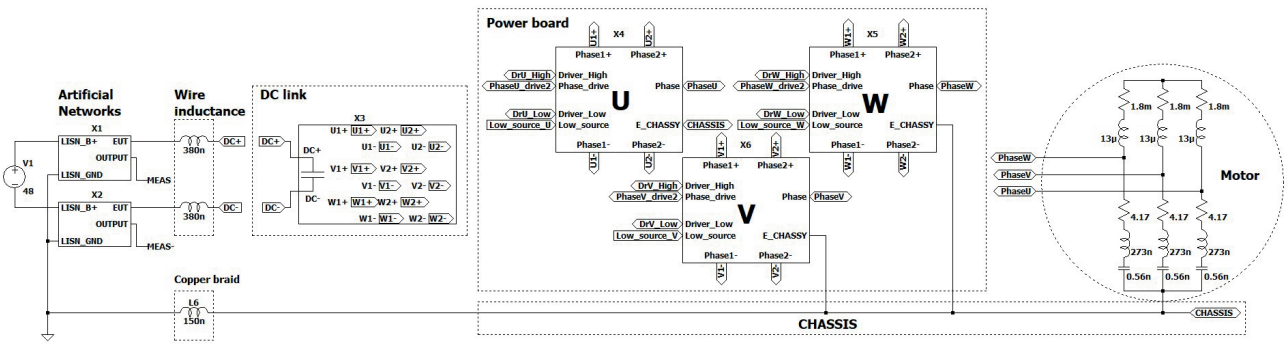

Figure 4: Top level EMI model including inverter (DC link, power board), motor and test setup according to CISPR 25.

$$L = 2l\left(\ln\frac{2l}{b+c}\right) + 0,5 + 0,22\frac{b+c}{l} \quad (1)$$

3.2 DC link

The DC link PCB assembly (PCBA) consists of four copper layers, as shown in the Fig. 5, with the internal two layers serving as DC positive and DC negative power planes. The two external layers contain multiple polygons to ensure a homogeneous load on each capacitor. This configuration forms a matrix of parasitic inductances that was modeled along with electrolytic and ceramic capacitors. Parasitic capacitances between the planes were neglected due to their small values in comparison to the capacitances of the capacitors.

The parasitic inductances, extracted with boundary element method (BEM), were recalculated into an average inductance per unit length (IPL) to establish a foundation for simplifying the matrix. This simplification results in fewer components and nodes for SPICE simulation.

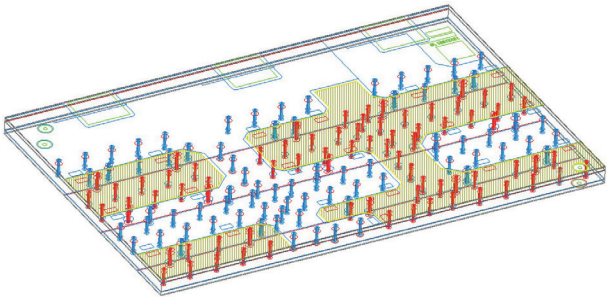

Figure 5: DC link PCB (Ansys® SIwave™).

The DC link matrix was modeled with 5 different horizontal inductances and 2 vertical ones. Each inductance has its own series resistance (see Table 2). The pads connecting the DC link to the power board are not symmetrically distributed, as shown in the Fig. 6.

Table 2: DC link parasitic parameters.

Parameter	Inductance [nH]	Series resistance [mΩ]
Lh1	0,88	0,22
Lh2	1,76	0,44
Lh3	2,4	0,6
Lh4	3,28	0,82
Lh5	1,4	0,35
Lv1	0,44	0,11
Lv2	1,64	0,41

3.3 Power board

The same approach to extract the parasitic elements from the Table 3 was used for the power board (see Fig.

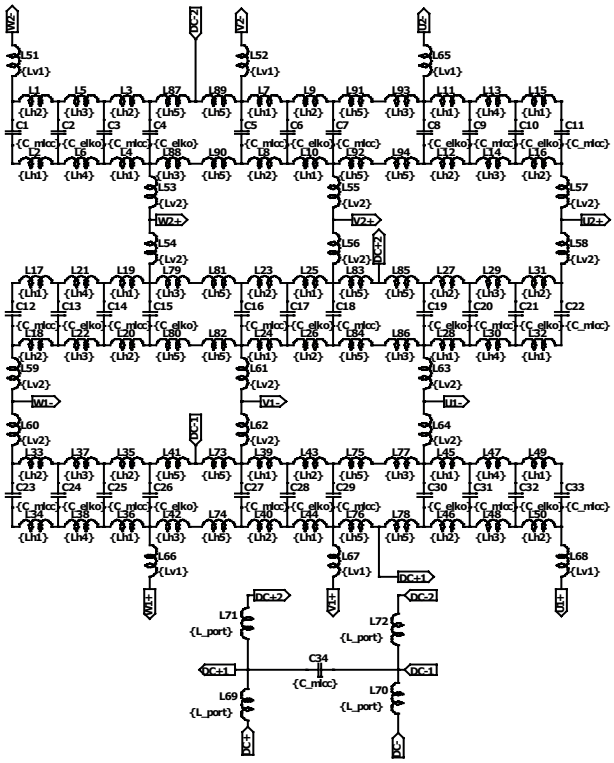

Figure 6: LTspice® model of the DC link.

7), where we sought the values of the parasitic inductances between the MOSFETs soldered onto the copper layer of the insulated metal substrate (IMS) [19].

Table 3: Power board PCB parasitic parameters.

Parameter	Inductance [nH]	Series resistance [mΩ]
L_pwr1	1,75	0,1
L_pwr2	3,5	0,2
L_phase	3,0	0,15

Parasitic capacitances of the polygons towards the substrate were calculated analytically. Capacitances of the B+ and B- polygons towards the substrate did not have an influence on the EMI spectrum due to the much higher capacitance of the Y-capacitors C1 and C2 from the Fig. 8. There was also a negligible influence of the parasitic inductances of the gate traces, whose values vary with the distance from the connector to the most distant MOSFET.

To model the MOSFET used in our experiment (Fig. 8), we applied the official SPICE model provided by the manufacturer. As the accurate switching element simulation is crucial for accurate EMI modelling, we verified the MOSEFET model adequacy by comparing the measured and simulated switching voltage transition shapes on a clamped inductive load according to Vrtovec et. al. [8]. Fig. 9 shows the setup for switching of the high side MOSFETs where the power board model is simplified for figure clarity.

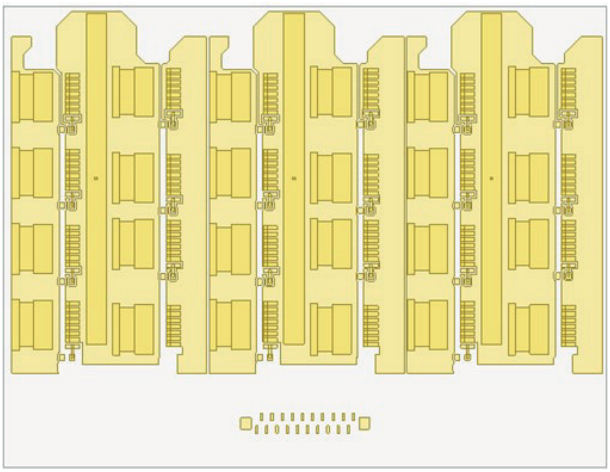

Figure 7: Power board PCB planes (Ansys® SIwave™).

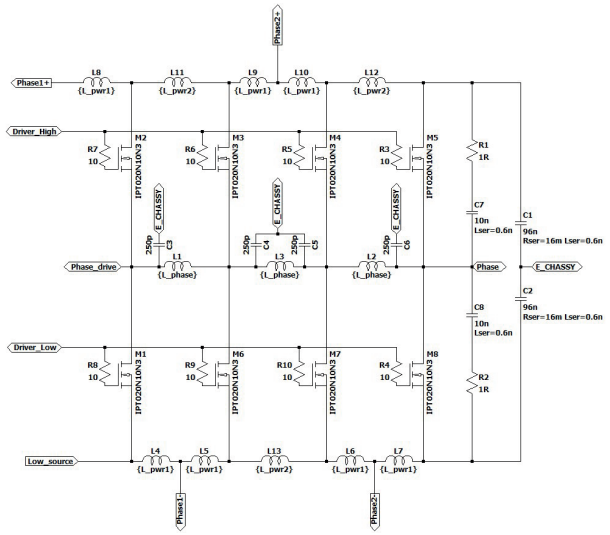

Figure 8: Power board single phase LTspice® model.

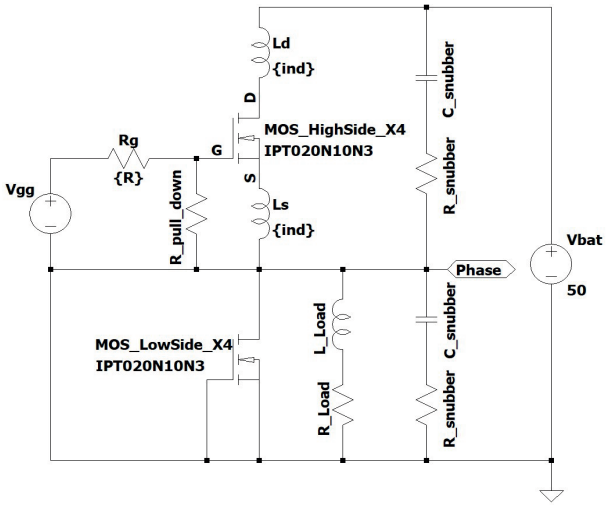

Figure 9: Test configuration featuring the clamped inductive load with V_{gg} controlling the high side MOSFETs. The measurements were taken using an inductive load of 40 µH and 6.66 Ω, achieving a current of 400 A_{DC} with the correct duty cycle, the V_{DC} was 50 V.

In the Fig. 10 we observe a good matching between the measured and simulated switching behavior of the high side MOSFETs (Phase V). It's crucial to note that the voltage-dependent capacitances of a MOSFET consistently influence the switching characteristics, alongside the inductances L_d and L_s originating from the PCB itself [8]. The latter is probably the cause for a slight phase shift between the graphs.

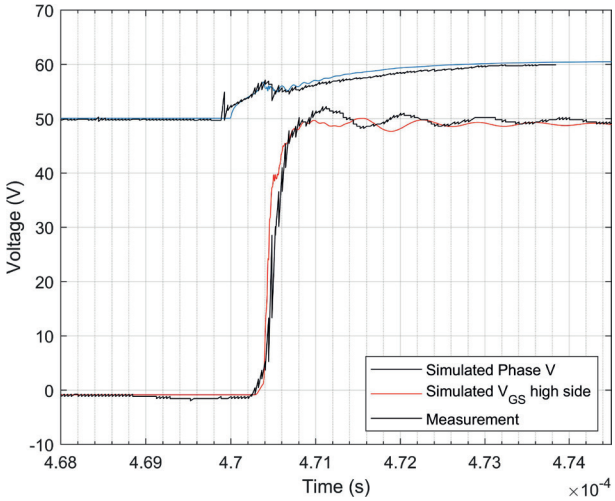

Figure 10: Switching sequence – high side ON. V_{GS} has an offset of +50 V for figure clarity.

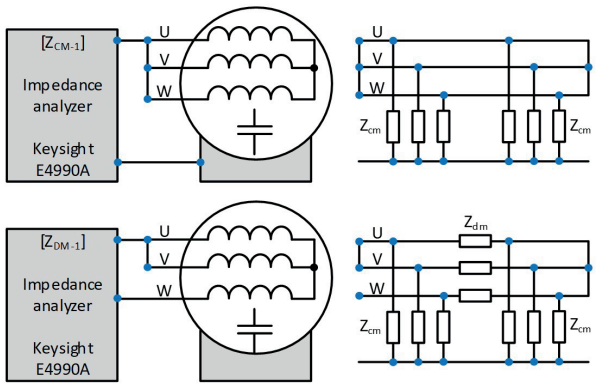

Figure 11: Common mode test configuration with motor equivalent impedance $Z_{CM\text{-}1}$ and differential mode test configuration with $Z_{DM\text{-}1}$ [13].

3.4 Motor

As already stated in the introduction, many researches propose an approach where lumped motor parameters are extracted through motor impedance measurements [10]–[15]. With this technique, a high-frequency model distinguishes common mode (CM) and differential mode (DM) impedances (see Fig. 11).

The $Z_{CM\text{-}1}$ measurement results in the Fig. 12 indicates a capacitive response in the low-frequency range, characterized by a single resonance point where inductance becomes predominant. It turns out that the

angular orientation of the rotor, representing the magnetic field of the permanent magnets with respect to the stator winding, exhibits minimal impact within the capacitive range of the $Z_{CM\text{-}1}$.

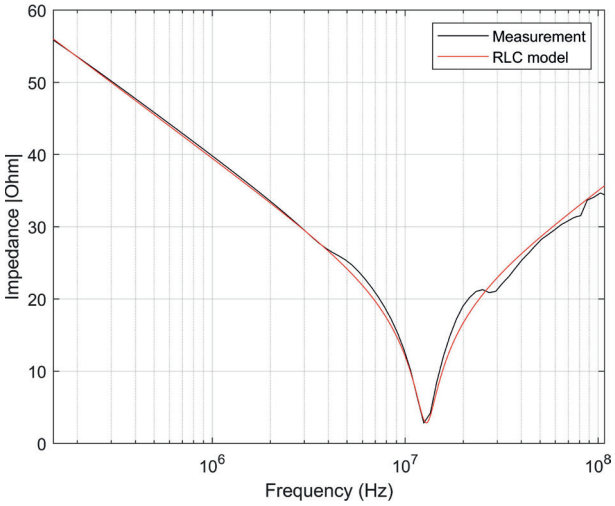

Figure 12: $Z_{CM\text{-}1}$ measurement results and approximation with RLC model.

From the high inductance of the windings, it also follows that the $Z_{DM\text{-}1}$ itself does not have a major influence on the *di/dt* produced during the switching sequence. Proceeding from this claim we can simplify the motor model where the $Z_{CM\text{-}1}$ represents CM propagation path and is independently combined with the winding characteristics.

To model the impedance behavior from the Fig. 12, we employed a simplified $Z_{CM\text{-}1}$ model with three basic RLC circuits, disregarding variations in rotor positions.

$$Z_{CM-1} = \frac{Z_{cm}}{3} \tag{2}$$

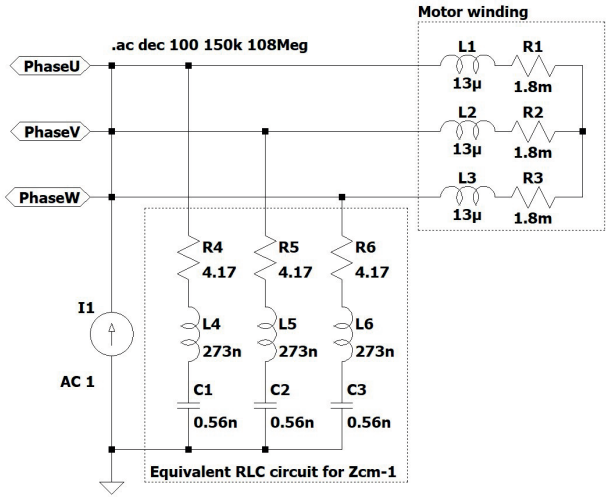

Figure 13: AC analysis model of the RLC circuit together with winding characteristics.

The proposed motor model from the Fig. 4 was evaluated with an AC analysis according to the Fig. 13 resulting in an adequate matching to the measured $Z_{CM\text{-}1}$ behavior (see Fig. 12).

4 EMI receiver

The characteristics of an EMI receiver must also be considered if we want to have an appropriate comparison between measured and simulated results of an EM spectrum. For historical reasons, the instrument characteristics are based on analogue super-heterodyne EMI receivers that sequentially scan frequency range of interest [20]. This approach is time-consuming and has been replaced with new digital Fast Fourier Transform (FFT) based instruments that comply with CISPR 16-1-1 [21], [22]. A basic block diagram of such a digital instrument can be found in the Fig. 14.

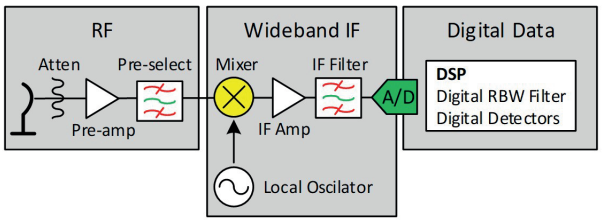

Figure 14: Block diagram of the FFT based EMI receiver [20].

4.1 MATLAB implementation of the EMI receiver

Within the SPICE transient simulation, the time step is varied according to the dynamics of the simulated results, thus an interpolation was performed to obtain a time vector with a constant time step. Generally, interpolation methods can introduce signal artifacts that could result in unrealistic spectral components. Thorough testing, we concluded that for the applied simulation conditions, the only method among the available within the MATLAB® environment that does not produce random overshoots between two simulated points was the Piece-wise Cubic Hermite Interpolating Polynomial (PCHIP) method.

CISPR 16 does not provide normative specifications for the parameters of the FFT. However, emerging from the Table 4, an appropriate windowing function must be used to meet the frequency response of the applied Intermediate Frequency (IF) filter, which originates from the superheterodyne principle [21]. Conventional EMI receivers generally apply a Gaussian window where the standard deviation of the windowing function is defined with the IF bandwidth for each frequency band. The windowing function also prevents spectral leakage caused by the discontinuity of the sampled signal.

Table 4: Bandwidth requirements for measuring receivers according to CISPR 16-1-1.

Frequency range [MHz]	f_{BW} [kHz]
0,15 – 30 (Band B)	9
30 – 1000 (Bands C & D)	120
1000 – 18000 (Band E)	1000

In the time domain, the Gaussian window function is transformed by the Short-Time Fourier Transform (STFT) into a Gaussian measurement bandwidth. This transformation results in discrete, overlapping measurement bandwidths in the frequency range. If a sine-wave carrier is positioned exactly between two measurement bandwidths, referred to as frequency bins, the result is a picket-fence effect (PFE) level error [20].

CISPR 16-1-1 requires accuracy better than ± 2 dB (± 2,5 dB above 1 GHz) for a sine-wave voltage measurement with 50 Ω resistive source impedance [21]. An overlap of more than 75% between the STFTs (see Fig. 15) ensures that the level measurement uncertainty for the pulse amplitude remains less than ± 1,5 dB [23]. In the used R&S ESR EMI test receiver, the STFT's overlap is at least 93%. The maximum level error is ± 0,4 dB, and the average level error just ± 0,1 dB [20].

Higher overlapping means longer computational time. To stay on the theoretical limit for the required error, an overlap of 75% was implemented, where *M* represents the number of applied windows (i.e., the number of STFT computations), including the measures for spectrum corrections [24]:

- dividing by the window length N_{win},
- multiplying by the factor of 2 to calculate single side spectrum,
- dividing by the factor of $\sqrt{2}$ to represent the measured power on 50 Ω input of the EMI receiver since the STFT algorithm returns the peak voltage value,
- dividing by the coherent amplification of the applied window G_C.

$$Gc = \frac{1}{N_{win}} \sum_{n=1}^{N_{win}} \left(w[n] \right) \tag{3}$$

STFT algorithm produces an array of complex numbers $\underline{X}(k,m)$, where the *k* th row corresponds to the amplitudes and phases of the frequency spectrum at frequency $K \cdot f_{res}$.

$$\underline{X}(k,m) = \frac{2}{\sqrt{2} N_{win} Gc} \sum_{n=1}^{N_{win}} \left(x\left[n + (m-1) N_{win} \left(1 - \frac{O_{proc}}{100} \right) \right] w[n] e^{-j 2\pi \frac{n k}{N_{win}}} \right) \tag{4}$$

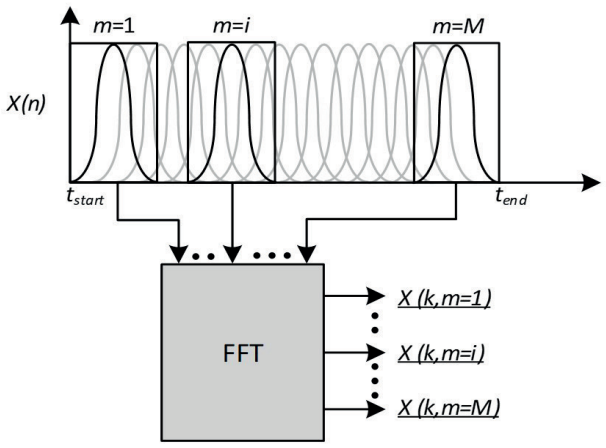

Figure 15: STFT overlapping.

By analyzing each individual row *m* of the complex array $\underline{X}(k,m)$ (see Fig. 16), it is possible to calculate the peak and average values at the observed frequency. The peak value is determined as the maximum value in the respective row.

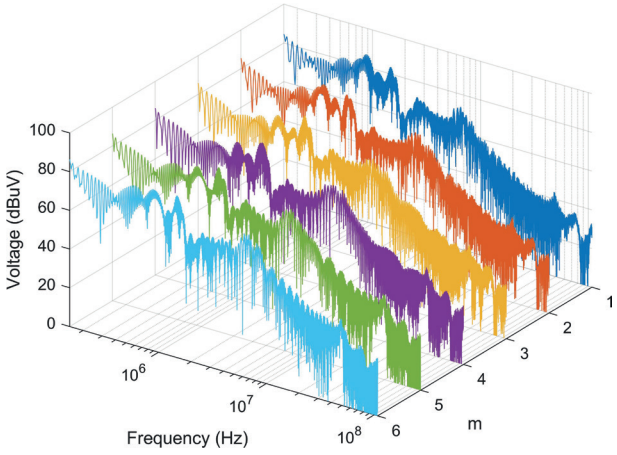

Figure 16: STFT algorithm without envelope detection.

$$X_{PK}(k) = \left| \underline{X}(k,m) \right|, m \in [1, M] \tag{5}$$

The average value for a certain *k* is calculated as the average of all absolute values in a certain row.

$$X_{AV}(k) = \frac{\sum_{m=1}^{M} \left| \underline{X}(k,m) \right|}{M} \tag{6}$$

5 Control strategy and results

The complexity of models, the number of nodes, and simulation parameters, have a direct impact on the duration of transient simulations and spectrum accuracy. The EUT employs the Space Vector Pulse Width Modulation (SVPWM) control strategy. To understand the influences of its implementation in the SPICE environment, we first implemented a simplified strategy where the PWM remains static.

5.1 Static PWM

The circuit from the Fig. 17 simulates a freeze-frame of a switching sequence, including dead-time. We analyzed EMI at 2 arbitrarily chosen static PWM switching sequences according to the Fig. 18, denoted by t_1 and t_2. The first PWM1 switching sequence from the Fig. 19

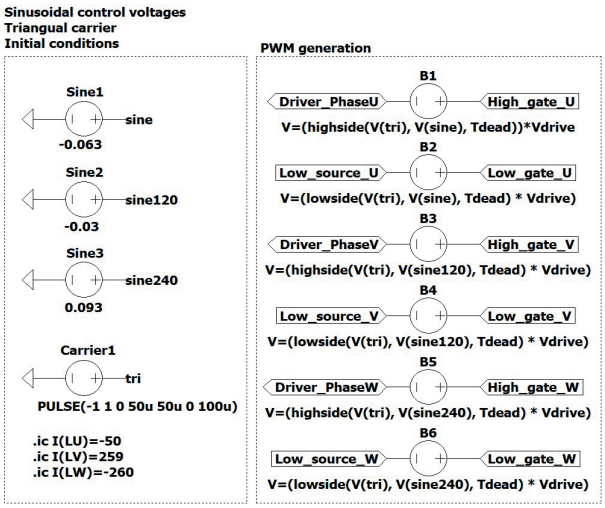

Figure 17: Static PWM1 implementation in LTspice®.

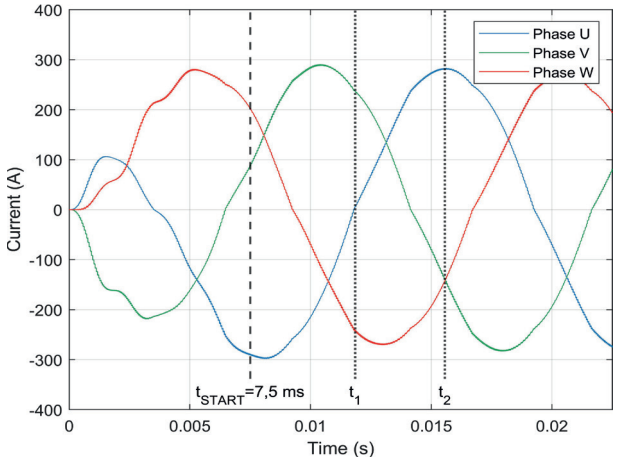

Figure 18: Simulated phase currents based on the SVPWM control strategy (t_{START} is the starting time for post-processing, t_1 and t_2 are times of the arbitrarily chosen static PWM switching sequences).

was set at t_1 when $I_{Phase\ U}$ goes through zero, while the second static PWM2 sequence was set at t_2 when $I_{Phase\ U}$ is at its peak value of 280 A.

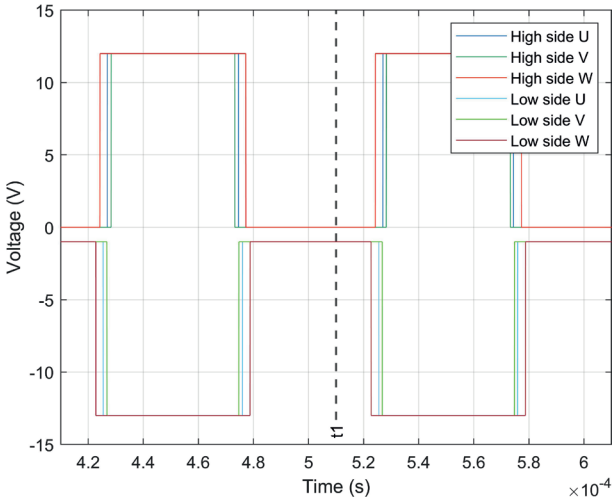

Figure 19: Static PWM1 switching sequence at t_1.

Here we show only the simulation setup at t_1 in detail, similarly was done for t_2. The switching frequency was 10 kHz, and the DC bus voltage was 48 V.

The approximation of this method lies in the inability to completely recreate PWM conditions at any SVPWM operating point. Therefore, it is important to set appropriate initial conditions to match the phase current values.

The input for the STFT algorithm cannot be infinitely short and must encompass at least a few overlapping windows to provide an adequate result. A time range of ± 0,5 ms around t_1 = 0,51 *ms* resulted in the application of six windows M = 6 (see Fig. 20).

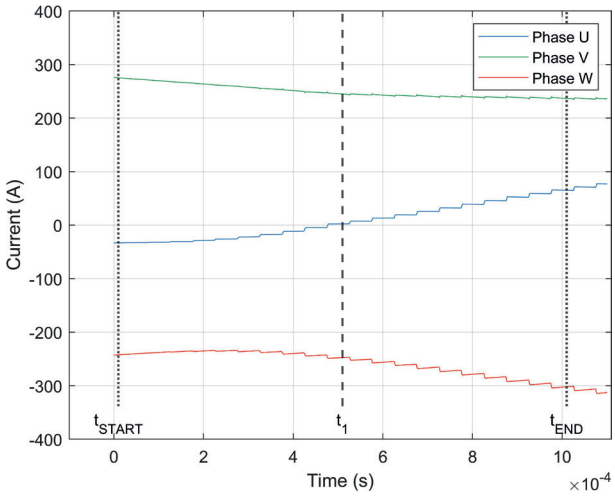

Figure 20: Simulated phase currents based on static PWM1 (± 0,5 ms around t_1 = 0,51 *ms*).

The simulated peak and average spectra for both sequences can be seen in the Fig. 21 and Fig. 22. The average spectral deviation for the switching sequence at t_1 is 7,34 dBµV and 3,79 dBµV, at t_2 is 6,35 dBµV and 3,65 dBµV for peak and average detectors, respectively. The transient analysis took 2 min to apply $M = 6$.

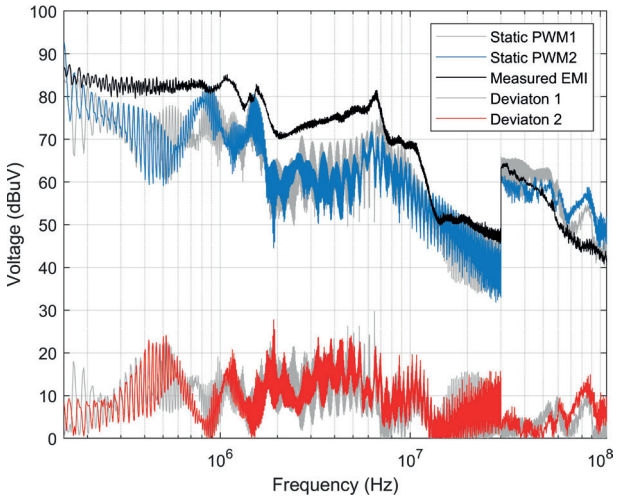

Figure 21: Comparison between measured and predicted peak detector spectrum (static PWM).

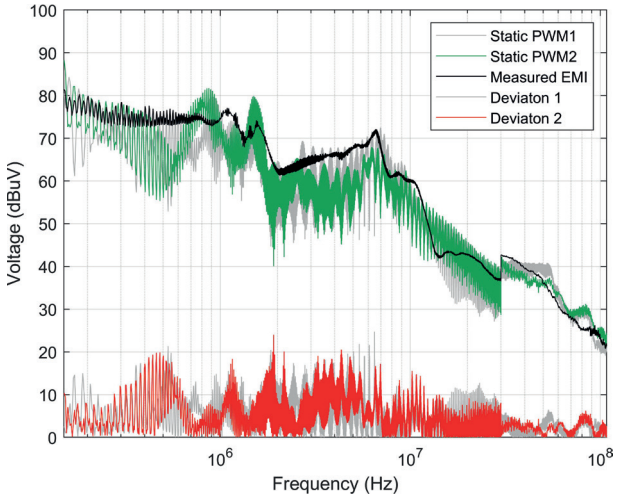

Figure 22: Comparison between measured and predicted average detector spectrum (static PWM).

5.2 Space Vector Pulse Width Modulation

To evaluate the effect of the motor rotation on the overall spectrum accuracy, the complete SVPWM control strategy for the inverter system was implemented in the LTspice® (see Fig. 23). The corresponding control strategy diagram is shown in the Fig. 24.

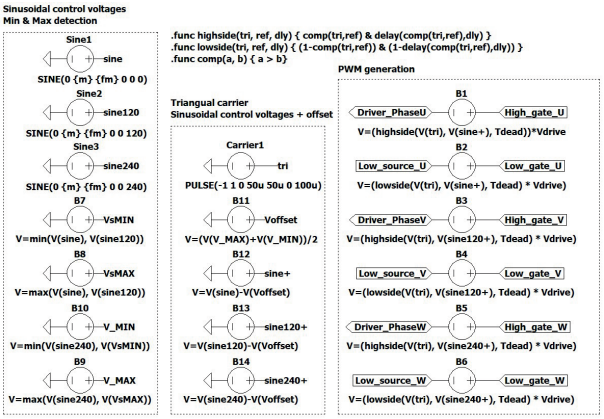

Figure 23: SVPWM implementation in the LTspice®.

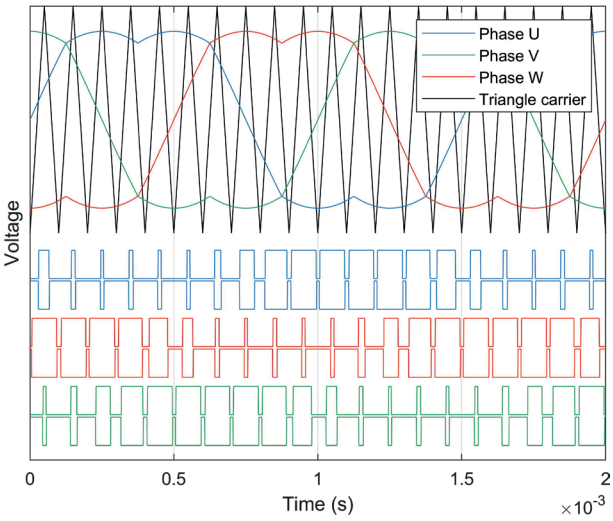

Figure 24: SVPWM control strategy (the chosen sequence is for figure clarity only and does not match the operating point at 1000 RPM).

The simulated peak phase current reached a value of 280 A_{PEAK} (200 A_{RMS}) by adjusting the appropriate modulation factor and other switching parameters according to the Table 5. On the EUT, the crossover distortion effect is mitigated within regulation algorithm.

Table 5: LTspice® switching parameters.

Parameter	Description
.param fm=66.6	Motor frequency
.param m=0.095	Modulation factor
.param Tdead=1.5e-6	Dead time

5.3 Transient analysis

The complexity of models, the number of nodes, and simulation parameters, have a direct impact on the duration of transient simulations. CISPR 25 requires operating the EUT under typical loading and other conditions

like those in a vehicle, ensuring that the maximum emission state occurs. The dwell time was 100 ms for 9 kHz and 10 ms for 120 kHz IF bandwidth, which must be appropriately translated into the simulation environment. To capture the entire spectrum of possible emissions produced by the motor drive, which in our case has 8 poles, we must set the simulation time to observe one electrical revolution of the motor at 1000 RPM.

$$t_{TRAN} > \frac{2\pi}{\frac{p}{2}\omega_m} = 15\,ms \tag{7}$$

As stated in the previous chapter, the LTspice® environment does not have the option to fix the time step due to convergence reasons, but it does have an option to limit its maximum value. In this case, the Nyquist theorem must be considered, with 108 MHz as the max frequency scale of interest.

$$f_{NYQUIST} < 2\,f_S = 2 \cdot 108\,MHz \tag{8}$$

$$t_{stepMAX} < \frac{1}{f_{NYQUIST}} \approx 4,63\,ns \tag{9}$$

In addition to the previously discussed minimum duration of the transient analysis (15 ms), we added 7.5 ms (total 22.5 ms) to ensure that all transient phenomena in LTspice® expired before t_{START}, including all phase currents reaching 280 A_{PEAK}, as it seen in the Fig. 18. The simulation setup was according to the Table 6.

Table 6: Simulation setup.

Parameter	Value
Processor, max. threads	Intel®Core™ i7-12700H, 20
Solver	Normal
Analysis	.tran 0 22.5m 7.5m 4.63n

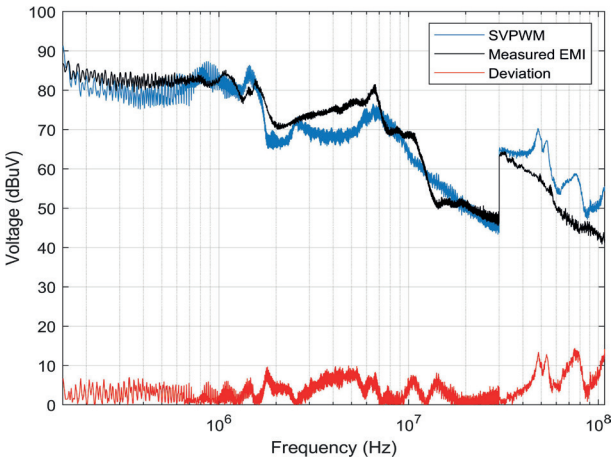

Figure 25: Comparison between measured and predicted peak detector spectrum (SVPWM).

The comparison of the measured and simulated EM spectrum for both detectors is shown in the Fig. 25 and Fig. 26, including the absolute deviation. The results show 3,33 dBµV and 2,58 dBµV of the average spectral deviation for peak and average detectors, respectively. The transient analysis took 43 min to capture one electrical revolution of the motor.

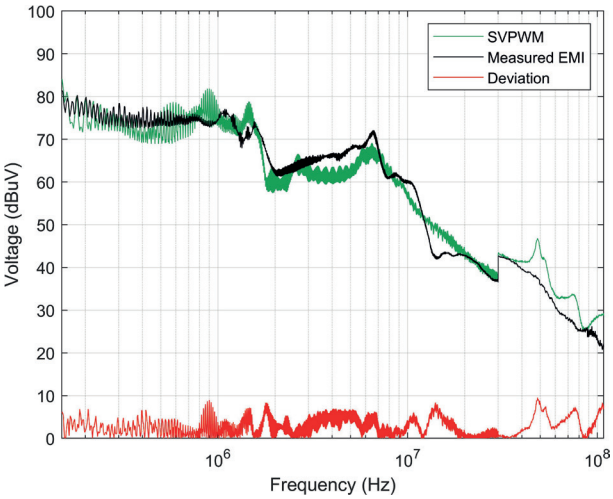

Figure 26: Comparison between measured and predicted average detector spectrum (SVPWM).

6 Conclusions

The proposed comprehensive strategy for modelling the conducted EMI of an integrated motor drive in the time domain was developed with the aim of finding a balance between overall simulation duration and spectrum accuracy.

For modelling the DC link and power board, we employed a direct approach to extract parasitic inductances between points of interest on the circuits, creating simplified matrices. This approach differed from using an automated Ansys® Q3D Extractor® feature, which generates a large matrix of lumped RLGC parameters. When extracting lumped motor parameters, we measured CM impedance through frequency sweep. Other parasitic elements were calculated analytically. This approach allowed us to maintain absolute control over the complexity of the matrices (i.e., to control the number of nodes and parasitic elements), directly addressing convergence issues and simulation duration in the LTspice® environment.

The implementation of the SVPWM control strategy improved the overall spectrum accuracy, considering the design of the EUT, with its large geometry resulting in different current paths during one electrical rotation of the motor. Neglecting this phenomenon leads

to the spectral value of a randomly chosen static PWM sequence deviating from the measured spectrum of a rotating motor. An additional improvement in the simulated spectrum was achieved with a proper EMI receiver implementation. The built-in response of the IF filters significantly impacted the spectrum, especially between multiple frequency ranges of the CISPR 16-1-1 standard.

An overview and comparison of the main factors of the SVPWM and static PWM methods can be seen in the Table 7.

Table 7: Comparison between static PWM and SVPWM simulation results.

Transient analysis	Static PWM1	Static PWM2	SVPWM
Simulation	2 min		43 min
.tran duration	1.01 ms		22.5 ms
Spectrum delta peak @150 kHz- 108 MHz	Average = 7,34 dBµV	Average = 6,35 dBµV	Average = 3,33 dBµV
Spectrum delta avg. @150 kHz- 108 MHz	Average = 3,79 dBµV	Average = 3,65 dBµV	Average = 2,58 dBµV

The proposed method with the SVPWM algorithm took 43 minutes to cover one electrical revolution of the motor, including the duration of the transient phenomena. Based on our experiences with developing multiple integrated motor drives, the resulting simulation time (i.e., < 1 hour) allows multiple iterations of model optimization without introducing bottlenecks in the development process. Simulation loops that take multiple hours or even days have limited repeatability, and their results are usually treated with low confidence since there is not enough time for parameterizing the parasitic elements to observe their impact on the spectrum.

The presented comprehensive strategy has a potential to be extended to other automotive products or even to other fields of interest where the accuracy of EMI prediction is highly dependent on changing current paths during the required dwell time.

7 Conflict of interest

The authors declare no conflict of interest.

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Arrived: 03. 01. 2024
Accepted: 06. 02. 2024

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 53, No. 3(2023), 203 – 203

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Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
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MIDEM Society / Društvo MIDEM
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Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, Ljubljana, Slovenija

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