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A Novel Topology of Variable Gain Distributed Amplifier in 0.13 μm CMOS Technology for UWB Applications

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Abstract: We present a new design of CMOS variable gain distributed amplifier (VGDA) by using a new topology of gain cell and a preamplifier circuit. In order to improve the gain, the proposed gain cell has modified cascade structure with optimized bulk source bias. Variable gain is made in the Preamplifier circuit. This section also increases the gain. Another significant advantage is that the noise level of VGDA has reduced. For this architecture, number of stages calculated in optimum mode and achieved third stages. The main advantage of this circuit is gain control with high range, and best input/output impedance matching in all of range and throughout the entire bandwidth. High flatness gain (in optimum mode) and low noise with best reverse isolation over the entire bandwidth up to 10 GHz are the other features of the proposed VGDA, which makes the VGDA to be more stable. The complete designed circuit was simulated in Taiwan Semiconductor Manufactory Company (TSMC) O.13 μm CMOS technology. The simulated provide a gain control range of 39 dB, from -10 dB to +29 dB, 29.4 dB as flat gain in optimum mode, 2.93 dB as the noise figure average across the bandwidth. Reverse isolation is better than –45.8 dB across the bandwidth, the input/output return loss is better than -10 dB and 61 mW total dc power consumption.

Keywords: CMOS distributed amplifier, variable gain, ultra wide band (UWB), high gain, low noise

Nova topologija porazdeljenega ojačevalnika s spremenljivim ojačenjem v 0.13 μm CMOS tehnologiji za UWB naprave

Izvleček: Predstavljamo nov obliko CMOS porazdeljenega ojačevalnika s spremenljivim ojačenjem (VGDA) z uporabo nove topologije ojačevalne celice in predojačevalnega vezja. Za doseganje višjega ojačenja ima predlagana ojačevalna celica modificirano kaskadno strukturo z optimizirano prednapetostjo substrata. Spremenljivo ojačenje je izvedeno v predojačevalnem vezju. Drugo pomembna novost je znižanje nivoja šuma. Glavna prednost vezja je kontrola ojačenja v visokem obsegu, najboljše ujemanje vhodne in izhodne impedance v celotnem območju in pasovni širini. Celotna struktura je bila simulirana v Taiwan Semiconductor Manufactory Company (TSMC) v 0.13 μm CMOS tehnologiji. Simulacije so pokazale kontrolo ojačenja od -10 dB do +29 dB z 29.4 dB ravnim ojačenjem pri optimalnem delovanju. Šum čez celotno pasovno širino znaša 2.93 dB. Reverzna izolativnost je boljša od -45.8 dB čez celotno pasovno širino; vhodno izhodne povratne izgube boljše od -10 dB in skupna dc moč 61 mW.

Ključne besede: CMOS porazdeljen ojačevalnik, spremenljivo ojačenje, UWB območje, visoko ojačenje, nizek šum

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1. Introduction

Recently, CMOS distributed amplifiers (DAs) have become increasingly popular for ultra-wideband (UWB) systems with 3.1 to 10.6 GHZ bandwidth, because of its wide input-impedance-matching bandwidth, wide gain bandwidth, and excellent linearity, UWB circuits find applications in various fields, such as high-speed

links, high resolution radars, imaging systems, wideband military systems, electronic warfare and broadband commercial radio systems. Among all kinds of high-speed circuits, the wideband amplifier is a key building block at both the transmitting and receiving ends. So far, however, to design the high speed analog systems some contradictory characteristic must be comprehended such as gain, operating frequency, impedance matching, power and noise. Accordingly the design of ultra wide band amplifier is one of the most significant issues in wireless networks. Design of high speed analog circuits requires adapting to contradictory characteristics, including gain, operating frequency, impedance matching, power, and noise, thus the design of ultra wide band amplifier is one of the most important issues in wireless networks. The distributed configuration is used frequently due to its wide bandwidth and high tolerance of process variation. As the semiconductors technology advances, the distributed amplifier (DA) becomes increasingly popular. Although a conventional distributed amplifier (CDA) can achieve a broad bandwidth, due to additive gain mechanism, obtaining a high gain is impracticable [1]. For wideband applications, approximately, the gain of CMOS CDA is restricted to 10dB, even though various circuit techniques have been reported such as the capacitive division technique [2], m - derived technique, loss-compensation technique with negative resistor [1,3] also negative capacitance [4] and nonuniform design approach [5]. Recent developments in the field of CDA, have led to acquiring high gain. These developments include cascaded multi-stage distributed amplifier (CMSDA) [6,7], matrix DA [8], cascaded single-stage distributed amplifiers (CSSDAs) [9], combination of the conventional DA and the cascaded single stage DA [10], and DA with internal feedback [11]. Recently, the DAs with gain control feature are used in various applications. The researches to date, have tend to focus on different methods which have been used for constructing this circuit. Programmable gain distributed amplifier (PGDA) [12] and variable gain distributed amplifier (VGDA) [13-16] are two major topology design methods of this circuit. Input and output impedance matching and stability throughout range, play a key role in designing these circuits and must be investigated attentively. However, a major problem with designing a faultless VGDA, is that there is almost no topology which possesses all the ideal characteristics such as high gain, broad bandwidth, low noise figure (NF), good impedance matching and low dc power consumption. This paper will focus on a new topology for designing VGDA, which relieves more appropriate range control. It has also devalued noise level while higher gain has obtained. Reverse isolation and input and output impedance matching are the other apparent characteristics of this new topology. This paper critically discusses this issue. It has been organized in 5 sections as below: In section 2, theories of distributed circuit and variable gain distributed amplifier have given. In section 3, the proposed VGDA topology has presented. Circuit design and simulation are discussed in section 4 and eventually section 5 presents conclusions.

2 Theory of DA and VGDA

In this section, brief description of distributed circuit has given; then DA has investigated.

2.1 Distributed circuit

A compact circuit is a kind of circuit which dimensions are small compared to the wave length of desired signal. At high frequencies, the device dimension is comparable to the wavelength of the signal and hence could not be called circuit as compression that circuit assumed to distribute. In general, the distributed term can be considered as any system that uses parallel signals from multiple directions [3]. Implementation of this circuit in CMOS technology is more interesting due to low cost and good performance. Distributed circuits in the microwave range are very common and utilizable. Amplifiers, oscillators and mixers are Instances of these circuits. In continue a new topology of DA which obtains high efficiency and low noise are presented.

2.2 Distributed amplifier

The concept of distributed amplification has been around for over Seventy years. Although the term distributed amplifier was coined in a paper by Ginzton et al. in 1948 which used vacuum tubes, the underlying concept can be traced to the patent specification entitled "Improvements in and relating to thermionic valve circuits" filed by Percival in 1935. Traditionally, DA design architectures have been realized using III-V semiconductor technologies, such as GaAs [17] and InP [18], it because of the extraordinary performance of technologies, this performance generate from higher band gaps (higher electron mobility), higher saturated electron velocity, higher breakdown voltages and higher resistivity substrates. The latter contributes to the availability of higher quality-factor (Q-factor or simply Q) integrated passive devices in the III-V semiconductor technologies. Even so, in order to meet the marketplace demands on cost, size, and power consumption of monolithic microwave integrated circuits (MMICs), ongoing research continues in the development of mainstream digital bulk-CMOS processes for such purposes. In 1997, the first implementation of distributed amplifier CMOS technology (0.8 μm) was performed.

Allstot group in Washington University had presented the general solution for DA with CMOS technology in 2000 and 2002 [19,20]. DA had overcome balance between gain and bandwidth.

A schematic of the CMOS conventional distributed amplifier is shown in Figure 1. As it can be seen, CDA consists of two main parts: gain cell, gate and drain transmission lines. These two lines implemented either by artificial transmission lines (in compare with cascade of LC filter sections to form a ladder type structure) or by uniform transmission lines. The internal capacitors of transistor can provide essential capacity. The operation of a DA is based on the fact that the signal from the input travels forward along the gate line and gets amplified by each transistor. The drain line carries these amplified signals both in the forward and reverse direction. The forward traveling waves on the drain line are in phase synchronization with the forward traveling wave of the gate line and with each other, implying that each device adds power in phase to the output signal at each tap point on the drain line. The forward traveling wave on the gate line and the reverse traveling wave on the drain line are absorbed by terminations which are generally matched to the loaded gate and drain lines.

Assuming the transmission lines to be lossless, the propagation constant and characteristic impedance of the transmission lines is given by:

$$\gamma_g = \alpha_g + j\beta_g \approx j\omega\sqrt{L_g\left[C_g + \frac{G_{gs}}{l_g}\right]} \tag{1}$$

$$Z_g = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_g}{C_g + \frac{C_{gs}}{l_g}}} \tag{2}$$

For the gate line and:

$$\gamma_d = \alpha_d + j\beta_d \approx j\omega\sqrt{L_d\left[C_d + \frac{G_{ds}}{l_d}\right]} \tag{3}$$

$$Z_d = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_d}{C_d + \frac{C_{ds}}{l_d}}} \tag{4}$$

Where α is the attenuation constant and $\beta = \frac{2\pi}{\lambda}$ is the wave number, Under perfect matching conditions both the lines are terminated by their characteristic impedances (Z_g, Z_d are gate and drain line characteristic impedances, respectively) [21].

2.2.1 Gain of distributed amplifier

Assuming phase synchronization on each of the lines we have:

$$\beta_g l_g = \beta_d l_d = \beta\, l = \Theta \tag{5}$$

And l_g, l_d are gate and drain line length, respectively. The voltage gain is given by:

$$A_v = -\frac{NgmZ_d}{2} e - jN\Theta \tag{6}$$

Where N is the number of stages or sections in the amplifier. With the increase in the number of sections in a DA the gain increases linearly but so long the conditions of uniform loading are valid. The power gain of the distributed amplifier (assuming lossless transmission lines) can be written as:

$$G = \frac{gm^2 Z_d Z_g N^2}{4} \tag{7}$$

Where Z_g, Z_d are gate and drain line characteristic impedances, respectively. In practical implementation the transmission lines cannot be devoid of losses. Actually, the loaded gate and drain transmission lines will have α_g and α_d as the real part of their propagation constants respectively. Although imaginary components do appear in the propagation constants, their contribution is negligible in the useful frequency range. Under phase synchronization condition of (5), the power gain of the amplifier is [22]:

$$G \approx \frac{gm^2 Z_d Z_g}{4}\left|\frac{e^{-N\gamma_g 1g_{-e}N\gamma_d 1_d}}{\alpha_g l_g - \alpha_d l_d}\right|^2 \tag{8}$$

Thus the gain does not increase monotonically with N and at a particular frequency. The optimum value of N is given by [22]:

$$N_{opt} = \frac{\ln\left(\frac{\alpha_d}{\alpha_g}\right)}{\alpha_d - \alpha_g} \tag{9}$$

Where α_g and α_d are the attenuation constants of gate and drain transmission lines respectively.

2.2.2 Noise in CMOS distributed amplifier

Thermal noise can be considered as induced gate noise and noise from the source/drain termination resistances. If flicker-noise and the noise from the parasitic resistances of the inductors are added to these sources, an expression for the noise figure is [23]:

$$F = 1 + \left(\frac{\sin n\beta}{n \sin \beta}\right)^2 + \frac{4}{n^2 g_m{}^2 R_{og} R_{od}} + \frac{R_{og} w^2 C_{gs}{}^2 \delta \sum_{r=1}^{n} f(r,\beta)}{n^2 g_m} + \\ + \frac{4\rho}{n g_m R_{og}} + \frac{K I_{ds}{}^a}{K T_o n C_{ox} R_{og} L_{eff}{}^2 \left(\frac{w}{2\pi}\right)^{ef} g_m{}^2} + \frac{R_{ig} \sum_{r+1}^{n+1} f(r,\beta)}{n^2 R_{og}} + \\ + \frac{4 r_{id}}{n g_m{}^2 R_{og} R_{od}{}^2} \qquad (10)$$

Where:

$$f(r,\beta) = (n - r + 1)^2 + \left(\frac{\sin(r-1)\beta}{\sin \beta}\right)^2 + \\ + \left(\frac{(2(n-r+1)\sin(r-1)\beta \cos \beta)}{\sin \beta}\right) \qquad (11)$$

$$R_{og} = \sqrt{\frac{L_g}{C_g}} \ , \ R_{od} = \sqrt{\frac{L_d}{C_d}} \qquad (12)$$

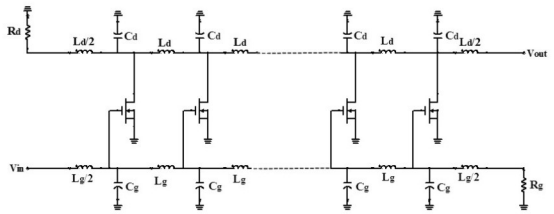

Figure 1: Conventional Distributed Amplifier structure

R_{ig} is the series resistance of the gate line inductors and R_{id} that of drain line inductors, T_o is the standard noise temperature for noise figure calculations (T_o = 290 K). K, a and e are parameters that characterize the flicker-noise, ρ and δ are parameters that characterize the thermal channel noise and the gate-induced noise respectively, and β is the progation constant of the artificial lines.

2.3 Variable gain distributed amplifier

Variable gain is a useful feature for the distributed amplifier, because it can be used along with baseband circuitry in an automatic gain control (AGC) loop. The AGC prevents large input signals from saturating the receiver front-end and amplifies small signals to above the detectable level. One of the important property of DA is possessing high gain and broadband matching simultaneously. A CDA with adjustable termination resistors [14] is the first reported VGDA in CMOS technology; however, the gain is less than 10 dB with a power consumption of 9 mW. a cascaded multi-stage distributed amplifier with variable-resistance metaloxide semiconductor field effect transistors (MOSFETs) [15] in 0.35 µm SiGeBiCMOS has been proposed to take the advantage of the multiplicative gain mechanism in order to reach high gain performance, but the variable gain structure is composed of the variable resistance NMOS using control voltage; hence it is not practical for low voltage and low power systems, to deal with this limitation, the PMOS variable resistor has been used in [16]. In the next section, a new topology of VGDA will be presented which has various advantages.

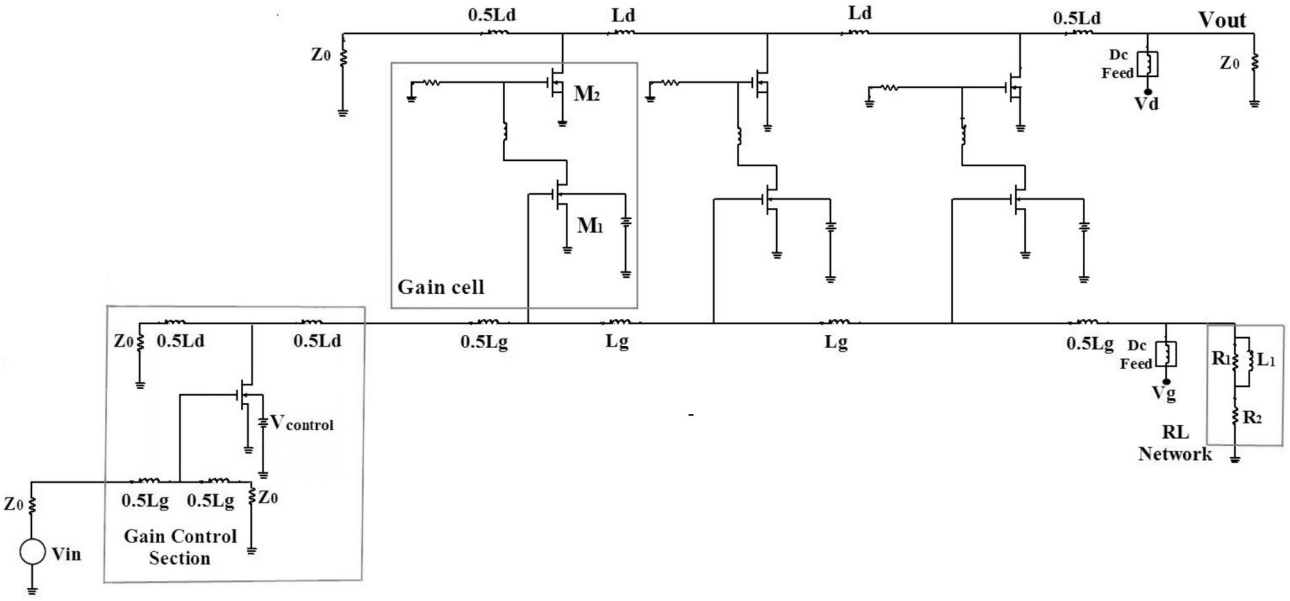

Figure 2: Schematic of proposed 3-stage variable gain distributed amplifier with new topology

3 Proposed variable gain distributed amplifier architecture

Figure 2 illustrates the proposed topology of variable gain distributed amplifier. First, the gain cells with new design will be discussed; then, one of the most effective parts of proposed VGDA circuit will be explained. This section is preamplifier, which is responsible for controlling the gain.

3.1 Gain cell architecture of proposed VGDA

Figure 3 shows the gain cell which is proposed in this paper. As mentioned in the previous sections, one of the influencing parameters on the gain is transconductance (gm). If it increases, the gain also increases. First, the study has focused on reason of optimizing bulk transistor (m_1) and then discusses about using inductor between two transistors in cascade structure, that result is transconductance increases and thereby, increase gain.

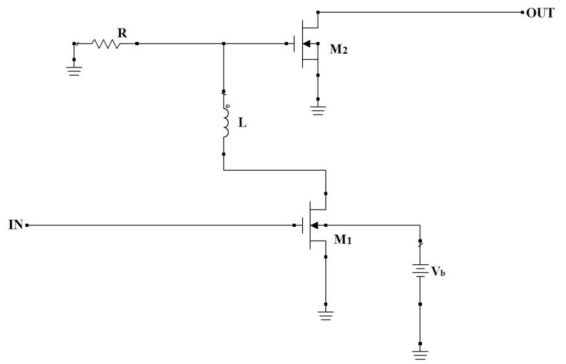

Figure 3: Proposed gain cell

The relation between bulk-source voltage, V_{BS}, and V_T is given as:

$$V_T = V_{To} + \gamma\sqrt{2\left|\varphi_f\right| + \left|V_{BS}\right|} - \gamma\sqrt{2\left|\varphi_f\right|} \tag{13}$$

Where: V_{BS}, V_{To}, γ and φ_f refer to: bulk source voltage, zero bias threshold voltage, bulk threshold parameter strong inversion surface potential, respectively. Equation (13) shows that the value of the threshold conductance voltage of the CMOS depends on the V_{BS} voltage. Figure 4 illustrates the small signal model of the CMOS transistor regarding the bulk effect.

m_1 transistor has two dependent current source. These source are "$g_m V_{gs}$" and "$g_{mb} V_{bs}$". They cause a relevant current with V_{gs} and V_{sb} voltages in drain terminal. In some circuits the source terminal is connected to the bulk in order to reject the effect of $g_{mb} V_{bs}$. The inducted current value toward the drain terminal by CMOS transistor given by:

$$g_m v_{gs} + g_{mb} v_{bs} \tag{14}$$

Where the v_{gs} and v_{bs} are input voltage of the gate source and bulk source capacitor, respectively. The transconductance relation of CMOS transistor given by:

$$g_m = \frac{\delta\, l_d}{\delta\, V_{GS}} = \psi\, v_{DS} \tag{15}$$

$$g_{mb} = \frac{\delta\, l_d}{\delta\, V_{BS}} = \frac{\psi\gamma v_{DS}}{2\left(2\left|\varphi\, f\right| + V_{BS}\right)^2} \tag{16}$$

Where:

$$\psi = \frac{(\mu_0\, c_{OX})W}{L} \tag{17}$$

equation (16) shows the dependency of g_{mb} value on bulk source voltage (V_{BS}) that the result is change in total g_m and thus changed gain by changing the bulk source voltage, this property has been used in this paper with optimal bias point on the bulk for maximum efficiency.

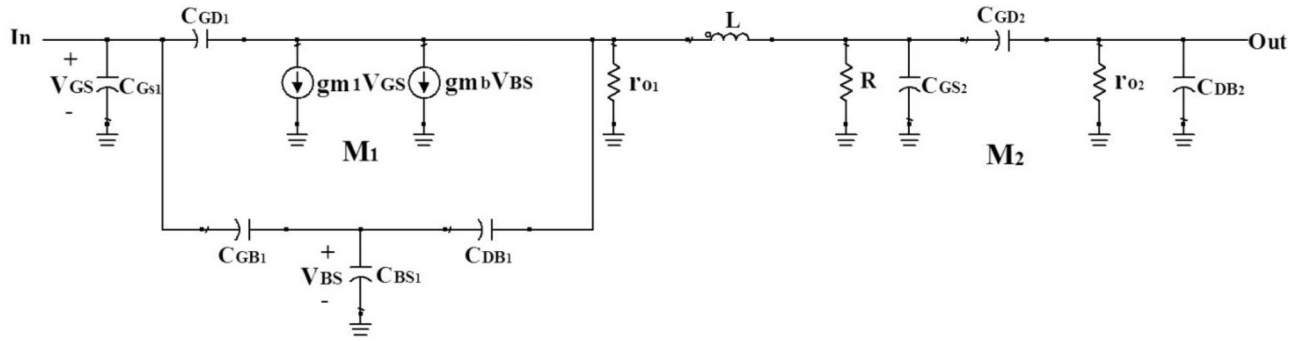

Figure 4: Small-signal equivalent circuit of the proposed VGDA gain cell

As can be seen in Figure 4, in the proposed design, an inductor is utilized between two transistors of cascade structure. According to the small signal equivalent circuit of gain cell (shown in Figure 5), C_{GS}, C_{DB} and C_{GD} are the respective gate to source, drain to bulk, and gate to drain capacitances of transistors, $r_{o(1,2)}$ are the output resistances of the transistors. Typically, $r_{o(1,2)}$ are relatively large and, therefore, can be neglected. Neglecting $r_{o(1,2)}$ and combining C_{GD1} with $C_{GB1,}$ C_{GS1} and C_{GD2} with C_{GB2}, C_{GS2} and also C_{DB1}, C_{DB2} with C_{BS1}, C_{BS2} formed C'_{GS1}, C'_{GS2}, C'_{DB1} and C'_{DB2}, respectively. We can derive the total transconductance of gain cell as:

$$G_m = \frac{\delta I_{out}}{\delta V_{in}} = g_{m1total} g_{m2} \frac{R \,\|\, \frac{1}{sC'_{GS2}} \frac{1}{SC'_{DB1}}}{\frac{1}{sC'_{DB1}} + sL + R \,\|\, \frac{1}{SC'_{GS2}}} =$$

$$= g_{m1total} g_{m2} \frac{R}{LC'_{DB1}C'_{GS2}Rs^3 + LC'_{DB1}s^2 + RC'_{DB1}s + RC'_{GS2}s + 1} \quad (18)$$

The concept of $g_{m1total}$ is related to g_m and g_{mb} of m_1. Usually, $C'_{GS2} >> C'_{DB1}$ and, thus, the total transconductance expression can be further simplified as:

$$G_m \approx g_{m1total} g_{m2} \frac{R}{LC'_{DB1}C'_{GS2}Rs^3 + LC'_{DB1}s^2 + RC'_{GS2}s + 1} =$$

$$= g_{m1total} g_{m2} \frac{R}{(LC'_{DB1}s^2 + 1)(RC'_{GS2}s + 1)} \quad (19)$$

From (19), three poles can be observed. One pole is formed by the input capacitor of the upper transistor. This pole normally dominates the low-frequency response due to the fact that the value of the gate-to-source capacitance of a transistor is usually large. The other two complex conjugate poles are created by the inductance and output capacitance of m_1. In practice, these two poles are located on the left s plane instead of exactly on the complex axis because of the loss incurred in real circuits. The presence of these two poles will boost up the transconductance of this gain cell at (20), which can also be considered as the cutoff frequency of the proposed gain cell transconductance.

$$f_c = \frac{1}{\sqrt{LC'_{DB1}}} \quad (20)$$

Where L and C'_{DB1} are the inductance used in gain cell and the new capacity of drain bulk which is obtained, respectively. In order to use the proposed distributed amplifier in reality, all losses were considered. The proposed gain cell has significantly higher transconductance, which provides a higher gain, as mentioned. Also, given that the gain cell has cascade structure, has better isolation. Another advantage is the input and output impedance matching well preserved, which helped to improve the stability of proposed DA.

3.2 Gain control section

In this VGDA, a preamplifier circuit is used. The main application of this section related to gain controlling. As can be seen in Figure 2, gain controlling is performed by changing bulk source voltage of preamplifier transistor. As discussed in the previous section, by changing the bulk source voltage of transistor, transconductance of transistor will change, that gain will be changed. This circuit has other effects on improving the performance of DAs. The first advantage occurs because signal is amplified before to injecting to the gate line which result in stronger signal arrives to the gain cell across the line, so the gain of DA has sharply increased. Another important advantage of this section is the significant reduction of noise.

Preamplifier is an amplifier which contains a transistor with low noise common source structure, the other section of the circuit is a distributed amplifier.

Therefore, the proposed topology can be assumed as a combined Amplifier as shown in Figure 5, which the first and second blocks are corresponds to the preamplifier and gain cell, respectively.

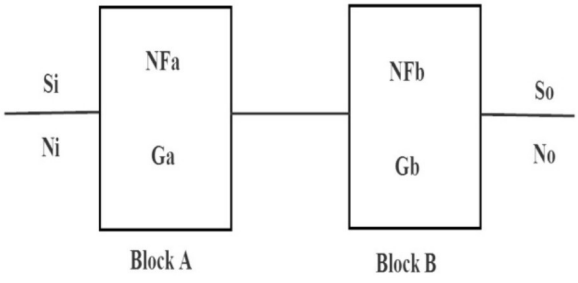

Figure 5: Block of composite amplifier

In this circuit, noise figure is equal to Equation 21:

$$NF = NF_a + \frac{NF_b - 1}{G_a} \quad (21)$$

Where NF_a and NF_b are the noise figure, G_a and G_b and are the gain of block a, and block b, S_i and S_o input and output signal, N_i and N_o input and output noise, respectively.

According to equation, (21) it can be concluded that if block a, which is part of the preamplifier, has high gain

and low noise, it makes total noise of the circuit to reduce. In addition, to further reduce noise, we used the proposed technique in [24], that instead of using single resistor, resistor and other circuit, consisting of resistor and inductor with parallel structure (RL network), have been used in the end of the gate line.

4 Simulation results

The characteristic impedance (Z_o) of both gate and drain lines is set 50Ω. Supply voltage of drain-source and gate-source of each cell is provided by voltage sources at gate and drain transmission lines, respectively. These voltages are considered less than 2V, Which makes the circuit to have low and good power consumption, The power consumption is only 61 mW.

In Figure 6, the flat gain response (S_{2_1}) of approximately 29.4 dB and cut-off frequency of 11.8 GHz in optimum control voltage, is shown. Figure 7 shows the gain control range of 39 dB, from -10 to +29 dB. As it can be seen in Figure 8 and 9, the input return loss (S_{1_1}) and the output return loss (S_{2_2}), respectively, both are better than 10 dB from 3.1 to 10.6 GHz in all of range, Figure 9 shows the reverse isolation (S_{1_2}) which is less than -45.8 dB across the bandwidth. The simulated noise figure (NF) of the variable gain distributed amplifier is shown in Figure 11. The average noise figure for optimum gain (29.4 dB) is around 2.93 dB within the band of interest. The simulations are carried out using "Advanced design system" (ADS) software [25].

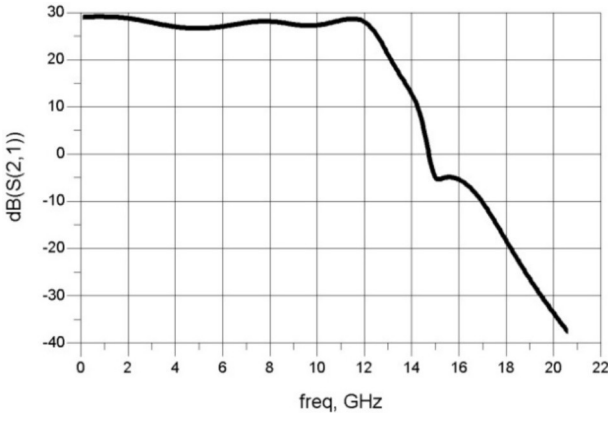

Figure6: Gain (S_{2_1}) of proposed VGDA

As yet, various DA and VGDA design methods are presented. Each of them improves one of the DA or VGDA design parameters. In result, a figure of merit (FOM) is defined to evaluate the power consumption together with the gain and bandwidth [23]:

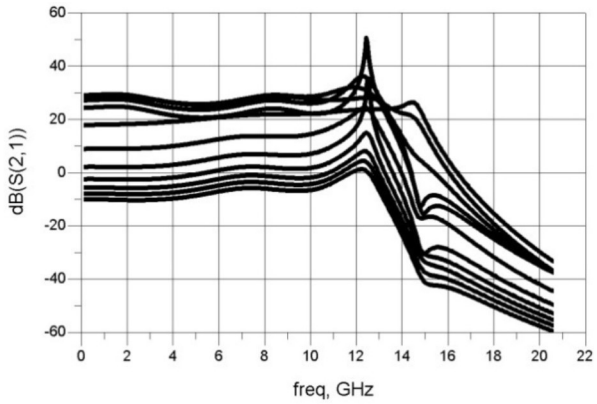

Figure 7: variable gain of proposed VGDA

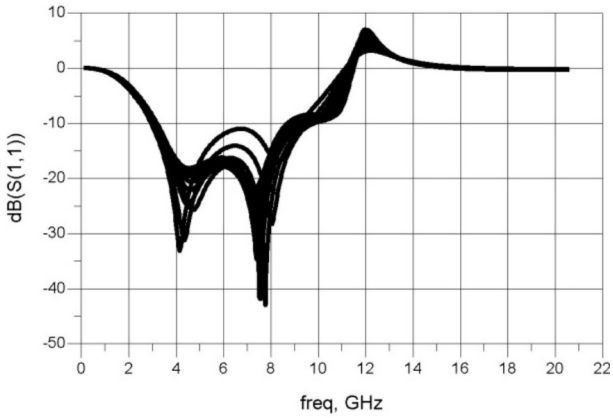

Figure 8: The input return loss

Figure 9: The output return loss

$$FOM\left[\frac{GHz}{mW}\right]=\frac{S_{2_1}[1]BW[GHz]}{(NF-1)[1]P_{DC}[mW]} \quad (22)$$

Where S_{2_2} [1] represents the average power gain in magnitude, BW[GHz] represents the -3dB bandwidth in GHz, (NF-1)[1] Represents the excess noise figure in magnitude, and P_{DC}[mW] represents power dissipation in milliwatts. This FOM includes the most relevant

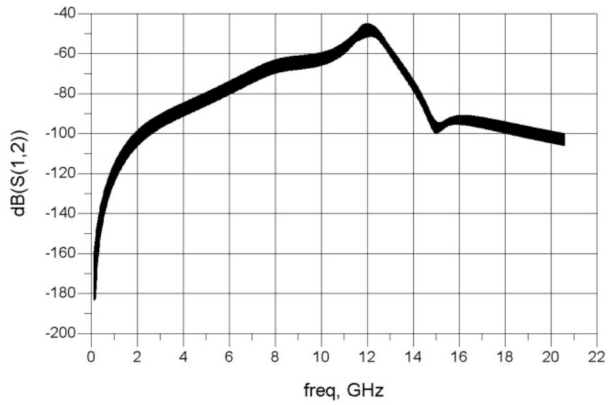

Figure 10: reverse isolation of proposed VGDA

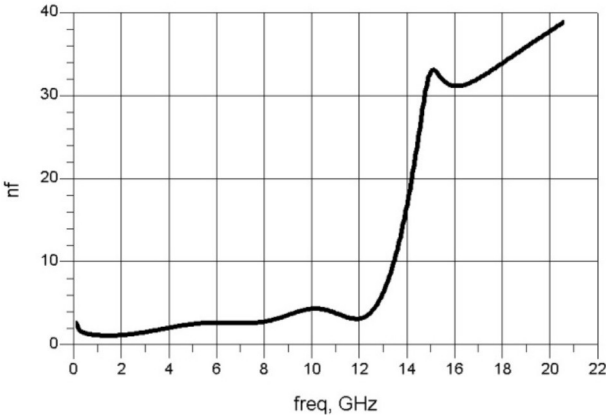

Figure 11: Noise figure for 29 dB gain of proposed VGDA

parameters for evaluating Das or VGDAs, for high gain, low-noise, low-power, and wideband applications.

Table I lists the performance figures of merit of recently published CMOS VGDAs along with those of this work, including bandwidth, gain in optimum mode, gain control range, noise figure, power consumption, and FOM. As shown, the proposed topology of VGDA exhibits the highest reported gain and FOM for CMOS VGDAs with high range of gain control in the UWB frequency.

5 Conclusions

In this paper, a novel topology which combines the preamplifier and new gain cell design with promoted cascade architecture has been proposed. Using this VGDA structure, all of the advantages of Architectures used in the new topology can be maintained. This topology can give considerations to high range gain control in ultra wide bandwidth, good impedance matching, low noise, and with reasonable dc power consumption. To authors' knowledge, this VGDA has the highest gain and FOM in 0.13 μm CMOS, and it has a comparable performance with other VGDAs in advanced processes. Moreover, this paper shows that the preamplifier circuit with new design of gain cell with optimum bias in bulk source can deliver higher gain, lower noise, and better power performance. The concept of proposed topology is demonstrated by VGDA with 3 stage (optimum stage) in a standard 0.13 μm CMOS process, and the simulated results agree with the circuit analysis well.

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Table 1: Performance summary and comparison with the published CMOS VGDA's

FOM	P_{dc} (mW)	AVG NF (dB)	GCR (dB)	Gain (dB)	Bandwidth (GHz)	topology	technology	Reference/ year
0.045	40	8.5	2.5 (0~2.5)	2.5	8.20 (0.8~9)	PGDA	CMOS 0.13 μm	[12] 2011
1.56	25	5.25	38 (-20~18)	18.1	11.4 (2.2~13.6)	VGDA	CMOS 0.18 μm	[16] 2011
2.34	7	5.95		12.5				
0.78	40	6.25	38 (-18~20)	20	10.5 (1.6~12.1)	VGDA	SiGe BiCMOS 0.35 μm	[15] 2006
2.028	6.4			12				
0.90	9	5.2	18 (-10~8)	8.6	6.97 (0.03~7)	VGDA	CMOS 0.18 μm	[13] 2006
3.78	61	2.93	39 (-10~29)	29.4	7.5 (3.1v10.5)	VGDA	CMOS 0.13 μm	This work

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