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A Low-Complexity and Energy-Efficient IR-UWB Pulse Generator in 0.18μm technology

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Abstract: A low-power and low-complexity impulse radio ultra-wideband (IR-UWB) pulse generator is presented in the paper. The tunable architecture is composed of a data and clock synchronization block, a controlled glitch generator, an adjustable two-stage buffer, and a pulse shaping filter. The generator has ability of the power spectral density (PSD) peak and central frequency adjustment. This is accomplished by varying the duration of the very short pulse produced by the glitch generator and changing the slope of the signal edges when passing through the buffer. This allows control in the output signal duration and amplitude (proportional to the slope of the signal at the pulse shaping filter input) determining the PSD value and -10 dB bandwidth. The pulse generator is designed and simulated in low-cost 0.18 μm UMC CMOS technology. The simulation results show 403 mV peak-to-peak amplitude and the pulse width of 0.6 ns. The PSD occupies bandwidth from 3 GHz to 7.8 GHz and fully complies with the corresponding FCC spectral mask. The IR-UWB generator supports OOK modulation with an area of 0.63 mm2. It has low power consumption of 1.3 mW corresponding to energy consumption of 13 pJ per pulse for 100 MHz pulse repetition frequency (PRF).

Keywords: analog RF design, CMOS integrated circuits, impulse radio ultra wideband (IR-UWB), pulse generator, transmitter.

Enostaven in energijsko učinkovit IR-UWB pulzni generator v 0.18μm tehnologiji

Izvleček: Članek predstavlja enostaven impulzni radio ultra širokopasoven pulzni generator (IR-UWB) nizkih moči. Spremenljiva arhitektura je sestavljena iz podatkovnega in časovnega sinhronizacijskega bloka, kontroliranega izvora kratkih pulzov, nastavljivega dvostopenjskega ločilnega ojačevalnika in pulzno oblikovnega filtra. Generator ima možnost spreminjanja spektralne gostote vršne in centralne frekvence. To je izvedeno s spreminjanjem trajanja zelo ozkega pulza generatorja in spreminjanja naklona robov signala pri prehajanju skozi ločilni ojačevalnik, kar omogoča kontroliranje trajanja in amplitude izhodnega signala (sorazmerno s strmino signala pri vhodu filtra oblikovanja pulza) z določitvijo PSD vrednosti in -10 dB pasovne širine. Pulzni generator je načrtovan in simuliran v ceneni 0.18 μm UMC CMOS tehnologiji. Rezultat simulacije je pulz z 403 mW amplitudo vrh-vrh in širino 0.6 ns. PSD zaseda pasovno širino od 3 do 7.8 GHz in polno ustreza pripadajoči FCC spektralni maski. IR-UWB generator podpira OOK modulacijo s površino 0.63 mm2. Ima nizko porabo moči 1.3 mW s pripadajočo porabo energija 13 pJ na pulz pri 100 MHz frekvenci ponavljanja (PRF).

Ključne besede: analogni RF dizajn, CMOS integrirano vezje, impulzni radio ultra širokopasovni (IR-UWB), pulzni generator, oddajnik.

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1 Introduction

Ultra-wideband (UWB), with allocated frequency range from 3.1 GHz to 10.6 GHz, is one of the most promising technologies for wireless communication applications [1] – [3]. There are several approaches within the UWB developed to satisfy very strict market requirements (multiband orthogonal frequency division multiplexing – MB-OFDM [4], direct-sequence – DS [5], the impulse radio ultra wideband – IR-UWB [6]). Besides of high data and wide bandwidth, low power consumption, or in other words high power efficiency becomes increasingly critical in wireless communications because of the popularity of battery-powered wireless devices. The IR-UWB technique has precedence in applications demanding energy efficient, low-cost and modest (without noisy and power-hungry blocks such as mixers and power amplifiers) UWB transmitter realizations allowing simple modulation scheme (e.g. on-off keying – OOK) [6]. These advantages are provided

by not so complicated type of transmission since the technology, as carrier-free approach, uses extremely short pulses (duration less than 1 ns) yielding a few GHz spectrum bandwidth. In addition, the protocol offers a great resistance to multipath fading that usually plagues for narrow-band systems, high time and range resolution (with a potential for centimeter accuracy in indoor environments), multiple access and robustness to interference, and low probability of undesired detection and interception [6]. The IR-UWB transceivers are highly used in very high data rate short-range communication, low data rate communication related to localization or/and positioning systems [6], biomedical applications such as wireless personal area networks [7], inter-chip communications [8], [9], and UWB biotelemetry [10], [11].

A pulse generator is one of the most essential parts of an IR-UWB transceiver as its signal shape determines the spectrum characteristics and effectively dictates specific system requirements. In addition to wideband spectrum satisfying all the FCC demands, it should provide low power and low complexity to enable low-cost UWB systems. Moreover, ability to control and tune the pulse generator spectrum and time domain signals represents very desirable advantage because it provides compensation due to process, voltage and temperature (PVT) variations, regulatory differences, and changes in the channel or antenna characteristics. A special attention must to be paid to this part of an UWB transceiver, as it is highly challenging to design the PG fulfilling all abovementioned demands.

The FCC rules define only allowed frequency bands and radiated power spectral density (PSD) but there are no requirements on the time-domain shapes. Therefore, different PG topologies can be found in the literature. Historically, the first IR-UWB pulse generators have used some specific components such as step recovery diode. They demonstrated limited tunability and very difficult integration in standard CMOS process [12]. Recently reported UWB pulse generators use diverse method to produce appropriately shaped signal, usually 5th derivative of the Gaussian pulse. Authors in [13], create a baseband impulse and then up-convert it to desired frequency using mixer (and local oscillator). These are quite complex and power hungry solutions due to use of continuously operating local oscillators and/or mixers. Although having decreased circuit complexity and power consumption, switched or gated local oscillator-based pulse generators suffer from restricted control over the star-up and turn-off transients and the output pulse shape [14]. PGs using digital-to-analog converter principle offer good resolution and controllability, but require high sampling rates, resulting in high power and system complexity [15]. Distributed waveform generators using transmission lines demand quite large area and complex combination of separately generated pulses [16].

A new energy-efficient, simple pulse generator designed in low cost 0.18 μm UMC CMOS technology is addressed in the paper. The tunable generator based on pulse shaping approach has very simply architecture leading to the power consumption and occupied area savings. Additionally, it provides control of the generated signal duration and amplitude enabling compensation due to the PVT variations and ensuring FCC compliance.

2 Pulse generator architecture and design

The output spectrum central frequency of an oscillator-based pulse generator is defined by the ring oscillator frequency [14]. In our previously published paper, the pulse generator architecture consisting of the ring oscillator uses different approach [17]. Since the maximal ring oscillator frequency obtained in the 0.18 μm UMC CMOS technology is 3.95 GHz (schematic-level simulation result) [18]-[20], the technique of increase in the spectrum frequency by doubling the high-pass filter frequency in comparison with the oscillator frequency was used in the aforesaid paper. To obtain 5th derivative of the Gaussian pulse at the output, only one or two pulses at the ring oscillator output are generated and then shaped by the output filter. The main cause of the frequency restriction is the limited set of transistor sizes available in the used process [18]-[20]. As the full potential of the oscillator-based approach could not be achieved in the 0.18 μm UMC technology, a new method is addressed in this paper. The pulse generator architecture is simplified by leaving the ring oscillator out and shaping a very short pulse produced by an advanced glitch generator topology. This allows UWB mask to be efficiently utilized and at the same time provides decrease in the circuit complexity.

The block diagram and architecture of the proposed pulse generator is shown in Fig. 1. It mainly consists of a Data and clock synchronization block, a glitch generator, a buffer, and a pulse shaping filter.

Buffers (inverter chains composed of transistors M_1–M_8) sharp the rising and falling edge of the clock (*clk*) and data (*Data*) signals. Then, the input signals are synchronized using transmission gate with the *clk* signal as the input, and the *Data* and inverted data (*D*) signal as the control signals. The *clk* signal passes through the transmission gate when the *Data* is high. The inverter stage

(transistors M_{11}–M_{12}) isolates the synchronization block (the transmission gate) from the glitch generator and sharps the rising and falling edge of the forwarded signal.

The tunable glitch generator is based on a three-transistor glitch module with a controlled delay element, implemented by a current starved inverter (transistors M_{16}-M_{18}) [21]. The method can produce Gaussian glitch shorter than techniques the most commonly used in glitch generator design (requiring NAND or NOR gate) due to parasitic reduction. When the *Data* signal is low, the transistor M_{13} is turned on connecting the node *A* to V_{DD}. At rising edge of the *Data*, the transistor M_{14} turns on and toggles the two inverters to charge the output node and the transistor M_{15} gate, turning it on. The M_{15} transistor activation causes the node *A* voltage to decrease sufficiently to toggle the inverters and discharge the output completing the glitch signal. The produced pulse duration is controlled by varying the V_1 voltage. This value determines the current of the M_{16}-M_{17} inverter stage and thus the feedback delay to the gate of M_{15}.

The role of the controlled two-stage buffer (consisting of two current-starved inverters, transistors M_{21}-M_{23} and M_{24}-M_{26}) is multiple. It provides good isolation between the glitch generator and the subsequent transmitter stage. Furthermore, not only does it amplify the glitch signal (G_{out}) but also determines slope of the rising and falling edge of the signal at the filter input. Varying the control voltages V_2 and V_3 changes the buffer stages currents that define the rate of charging and discharging their output parasitic capacitances, and thus allows control of the rising/falling edge of the filter input signal. Since the filter is used as a differentiator in the time domain to form appropriate signal waveform, the amplitude and shape of the generated signal depend on the slope of the filter input signal edges. As a consequence, the amplitude and shape of the output signal are adjusted by varying V_2 and V_3 control voltages.

Since the output spectrum central frequency (depending on the time domain behavior) is determined by the slope/shape of the filter input signal and its characteristics, the pulse shaping filter frequency is set to value approximately equal to the center of the UWB bandwidth by choosing suitable components values: C_1=240 fF, L=1.6 nH and C_2=220 nH.

The ability to tune the output spectrum characteristics in means of the bandwidth and spectrum central frequency by varying the control voltages V_1, V_2 and V_3 enables compensation due to PVT variations and additional spectrum fitting within the FCC spectral mask.

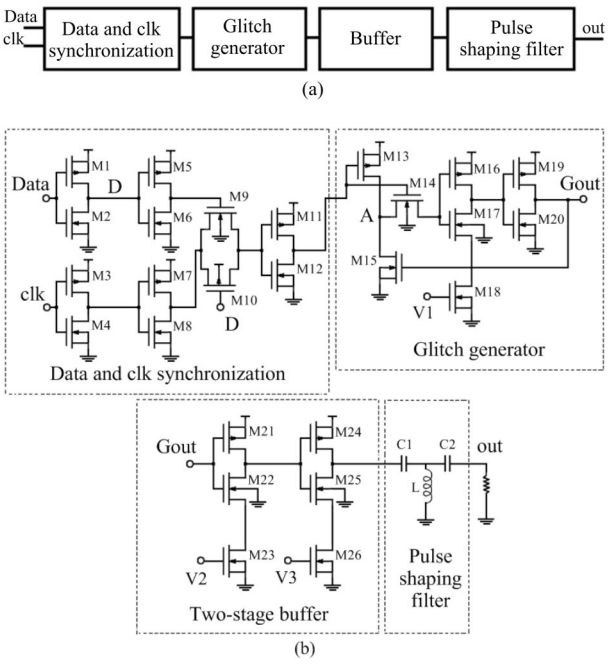

Figure 1: The proposed pulse generator: (a) block diagram and (b) circuit schematic.

3 Post-layout simulation results and comparison

The presented IR-UWB pulse generator is designed in a mixed mode/RF 0.18 µm UMC CMOS process and simulated using SpectreRF Simulator from Cadence Design System. The Assura (Cadence) and Calibre (Mentor Graphics) parasitic extraction tools have been used in post-layout simulations and obtained results were compared with each other. As those tools are the most commonly used in RF IC design, the presented results are very reliable.

The technology has supply voltage of 1.8 V. The generator supports on-off keying (OOK) modulation. This modulation type is adopted due to its simplicity as it allows the simplest transmitter realization, and consequently low power dissipation and the smallest chip area. It is well known that the energy efficiency and low transceiver cost represent the main advantages of the IR-UWB technology.

The proposed pulse generator is supposed to drive a 50 Ω load (the output resistor shown in Fig. 1(b)) representing the antenna characteristic impedance. Even though the UWB antenna impedance is not restricted to 50 Ω, this value is used for most of the models based on miniature commercial antennas. The pulse generator operates in burst mode with low duty cycle and pulse repetition frequency (PRF) of 100 MHz. This value of PRF marks the boundary between the low data

and high data rate applications, and it is considered as the lowest value for high data rate communications. The impulse regime with low duty cycle allows very low power dissipation of PGs. In general, the nature of the IR communication enables saving power between each pulses and consuming power just at the moment when the pulse is produced. The presented topology was optimized with the main goal to cover the lower UWB band with spectrum bandwidth as wider as possible, while still efficiently satisfying the FCC spectrum requirements. Additional aim was to minimize the power consumption and keep acceptable values for remaining Figures of Merits (FOMs). The main reason why the operation range is restricted to the lower UWB bandwidth is availability of measurement equipments. Our institute still has no required instrument but it is in a process of purchasing an oscilloscope that can measure time domain signals till 6 GHz. The proposed design is sent to fabrication and it is expected to be measured by the end of the year.

The pulse generator layout is shown in Fig. 2. The integrated circuit (IC) occupies a die area of 720 x 886 μm^2 including bonding pads, and the active circuit area is only 421 x 508 μm^2. The NMOS and PMOS transistor parameters values are given in Table 1. The transistors are made as multi-finger devices with the fixed channel length of 0.18 μm and variable gate width. The total transistors gate width is calculated by $W = ng \cdot 5$ μm, where 5 μm represents the gate finger width, and parameter *ng* the gate finger number which is in the range from 5 to 21 (the manufacturing process limitation). Additional technology recommendation is to use only odd values for the *ng* parameter. Since the 0.18 μm UMC CMOS is a twin-well process (without additional deep N-well layer), the bulks of all NMOS/PMOS transistors are connected to adequate reference voltages (GND in case of NMOS, and V_{DD} in case of PMOS transistors), shown in Fig 1(b).

The generated waveform and its spectrum are shown in Figs. 3 and 4, respectively. The pulse has peak-to-peak voltage amplitude (V_{pp}) of about 403 mV, and the duration about 0.6 ns. The 10 dB bandwidth of power spectral density (PSD) is from 3 GHz to 7.8 GHz. In fact the spectrum has wider bandwidth because the lower cut-off frequency is below 3 GHz (2.7 GHz). However, this is not taken into account since frequencies lower than 3 GHz are not considered in this kind of application. It can be noticed that the obtained PSD fully meets the FCC spectral mask except in the GPS band.

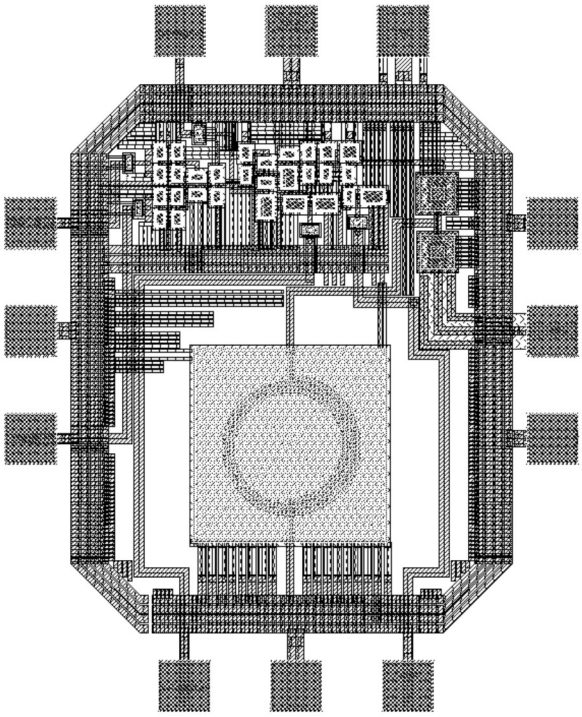

Figure 2: The IR-UWB pulse generator layout.

The PSD has maximum value of-43.78 dBm/MHz at 4.8 GHz, and a quite sharp roll off with more than 25 dB of out-of-band rejection relative to the peak power level. It is worth noticing that the peak value is very close to the maximal value regulated by the FCC alliance. The value could be increased to the FCC limit by choosing the appropriate set of control signals, but the corresponding spectral mask would be violated at frequencies around/below 3.1 GHz.

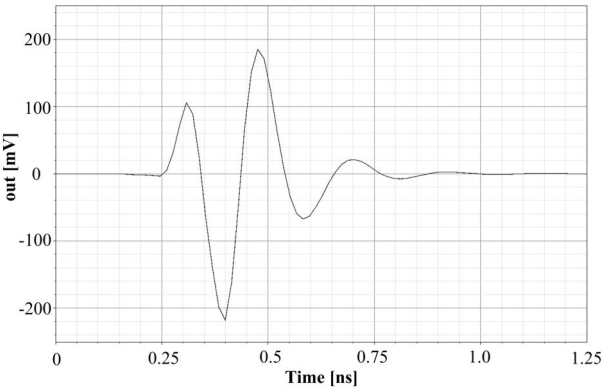

Figure 3: Pulse generator output waveform.

It should be emphasized that PG spectrum characteristics can be tuned in case of difference in post-layout

Table 1: The NMOS and PMOS transistors sizes.

Transistor	M1-12	M13	M14-16	M17	M18-20	M21	M22	M23	M24	M25,26
Width [μm]	25	35	25	105	25	45	25	105	75	25

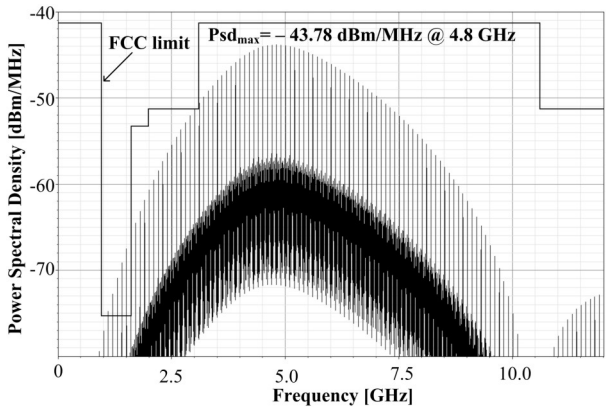

Figure 4: Pulse generator output power spectral density.

and measured results usually caused by the PVT variations. The pulse generator dissipates average power of only 1.3 mW corresponding to 13 pJ energy consumption per pulse for PRF of 100 MHz.

Table 2 summarizes the obtained post-layout simulation results of the proposed IR-UWB pulse generator and comparison to performance of the recently published PG designs. Although, it can be difficult to make fair comparisons when different specifications and technologies are used, it is clear that the proposed circuit has by far the highest peak-to-peak amplitude, the widest 10 dB bandwidth and the lowest power consumption. Moreover, other FOM are comparable to the results presented by the authors. The occupied area in Ref [25] is a little bit smaller comparing to layout dimensions presented here. However, it is expected since the chip is designed in scaled technology. The proposed pulse generator is suitable for ultra-low power wireless communication applications covering the 3 – 7.8 GHz frequency range.

4 Conclusion

A new energy-efficient tunable pulse generator is designed in 0.18 µm CMOS UMC technology for high date rate 3 – 7.8 GHz UWB applications. The time and spectrum domain signal adjustment is provided by varying the control voltage of tunable glitch generator and two-stage buffer composed of current starved inverted topologies. The power spectrum density of the output signal is tunable in order to provide compensation due to PVT variations and satisfies the FCC UWB mask requirements under different transmit conditions. The post-layout simulation results demonstrate that the proposed architecture has significantly lower power consumption and higher peak-to-peak amplitude compared to the previously reported UWB pulse generators covering the approximately the same frequency range.

Acknowledgments

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Table 2: Performance comparison of the IR-UWB pulse generators.

Reference	Power cons. [mW]	BW (-10 dB) [GHz]	Vpp [mV]	Pulse width [ns]	Die area [mm2]	PRF [MHz]	Technology
/24/	4.2	3.5 – 7.5	150	1	N/A	200	0.13 µm CMOS
/25/	3.8	3.0 – 6.0	230	0.5 – 0.9	0.44	910	0.13 µm CMOS
/26/	23.0	N/A	200	0.82	0.50	50	0.18 µm CMOS
This work	1.3	3 – 7.8	403	0.60	0.63	100	0.18 µm CMOS

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