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A MULTILAYER CHIP VARISTOR: THE FUTURE IN THE LOW VOLTAGE TRANSIENT SUPPRESSION
Part I: Fabrication and Characteristics

Z. Živič
KEKO, Žužemberk, Slovenia

Keywords: voltage transients, protective devices, protection components, SMT, surface mount technology, multilayer chip varistors, MLV chip varistors, ZNO varistors, thin sheet laminating technology, ceramic technology, leakage currents, surge currents, response times, nonlinear coefficients, surge absorptions, electrical breakdowns, fabrication processes, electrical properties

Abstract: A low voltage ZnO multilayer chip varistor for surface mounting was developed using tape casting and green sheet laminating ceramic technology. Differently sized chip varistors with breakdown voltage ranging from 4 V to 100 V were realised, featuring low leakage current, high nonlinear coefficient in a wide current range, very high surge current withstand capability (> 2000 A) and response time shorter than 5 ns. Very good stability on repetitive pulse of high amplitude and high energy level was also recorded. All these characteristics make multilayer chip varistor a very promising low voltage protection device.

Večplastni čip varistor: Prihodnost zaščite proti prehodnim pojavom in napetostnim sunkom
I del: Izdelava in lastnosti

Ključne besede: pojavi prehodni napetostni, naprave zaščitne, elementi zaščitni, SMT tehnologija montaže površinske, MLV chip varistorji večslojni, chip varistorji, ZNO varistorji, tehnologija nalivanja plasti tankih, tehnologije obdelave keramike, tokovi uhajavi, tokovi udarni, časi odzivni, koeficienti nelinearni, absorpcije udarov, preboji električni, procesi proizvodni, lastnosti električne

Povzetek: Nizko napetostni ZnO večplastni čip varistor za površinsko montažo je bil razvit s pomočjo keramične tehnologije nalivanja tankih plasti. Narejeni so čip varistorji različnih dimenzij, s prebojnimi napetostmi v obsegu od 4 V do 100 V, z naslednjimi lastnostmi: nizki tok puščanja, visoki nelinerni koeficient v širokem tokovnem področju, sposobnost absorpcije tokovnih sunkov višjih od 2000 A in čas odziva krajši od 5 ns. Zelo dobra stabilnost proti tokovnim sunkom visoke amplitude ter visokih energij je tudi bila ugotovljena. Vse te lastnosti kažejo da je večplastni čip varistor zelo obetavna nizko napetostna zaščitna komponenta.

1. Introduction

Electronic and electrical circuits can be subject to severe and sudden impulse voltage transients generated by lightning, switching and electrostatic discharge accumulated on the human body.

A contemporary development in the field of electronics and especially microelectronics requires miniaturised, highly integrated and low power consumption devices. As a result of this, the requirements for reducing device sizes and operation at low voltages are becoming extremely important for all electronic components including protective or surge absorbing devices.

Namely, lowering of the device geometrical dimensions, or scaling down principle, is widely used to improve CMOS IC's performances as: speed, density, complexity, reliability and cost. The dimension lowering is followed by operating voltage lowering as well. At the same time, internal protection devices built into IC's (typically containing monolithic connected diffused resistor with two or four Zener diodes) have been reduced in size to minimise their impact on speed and circuit area. Therefore, protection efficiency of the internal protection decrease, so CMOS IC's become more sensitive to damage or malfunctions caused by supply voltage transients and electrostatic discharges.

As a solution, electronic designers can either overspecify the circuits or use external protection. Final stability and quality of systems as well as economic balance call for the use external protection, not only of the whole systems or subsystems but of the individual sensitive components as well.

Transient voltage overstress protective devices can be divided into three categories: filters (R-C, R-L-C, etc.), crowbars such as gas discharge tubes or thyristors and low voltage clamps like varistors and Zener diodes. As

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far as low voltage surface mount devices are concerned only multilayer chip varistor (MLV) and Zener diode will be discussed. Both exhibit the necessary voltage - current relationship: at low voltages the current is very small, but when the applied voltage exceeds some predefined value (threshold), the device impedance decreases drastically and dissipates the excess energy which would be absorbed by the active component being protected. A ZnO MLV as well as Zener diode have this property although the operating physical principles and technology are different as shown in Table 1.

Both planar Si processing technology and pn-junction physics as a basis of Zener diode functioning are very well covered in literature[1,2]. Shallow pn- junction depletion region directs the operation of Zener diode. Its breakdown mechanism is tunnelling and avalanche multiplication one. Zener diode breakdown voltage is regulated by the depletion layer width, i.e. by the charge carrier concentration on both sides of pn-junction as well as by its geometry. When the diode is in breakdown, the greatest part of the energy is dissipated exactly in the shallow depletion layer.

In the case of varistor the physical model of its operation is not so 'clear', which will be one of the subjects of the discussion to follow.

Table 1: General differences between Zener diodes and multilayer varistor

General Characteristics	Zener Diode	MLV
Basic material	Si	ZnO
Structure	Monocrystal	Polycrystal
Physical mechanism	Tunneling & avalanche multiplication	Thermoionic emission & hot carrier injection effect
Barrier type	Abrupt junction	Double Shotky barrier
Technology	Planar Si	Ceramic - thin sheet laminating

2. Fundamental Characteristics of ZnO Varistors

2.1. Basic material

While Zener diode is semiconductor component made on monocrystalline Si, varistor is polycrystalline semiconductive electronic component on ZnO. Semiconducting ZnO of wurzite crystallographic structure is basic varistor material amounting to more than 90 % wt. This structure is relatively 'open' allowing easy building-in of dopants and influencing the nature of defects and diffusion mechanism[3]. The most common defect in ZnO is the metal ion in the open interstitial site, leading to a nonstochiometric metal excess N-type semiconductor with band gap of 3.3 eV. Within the band gap there are donor and acceptor levels occupied by thermally induced intrinsic defects as shown in Fig. 1.

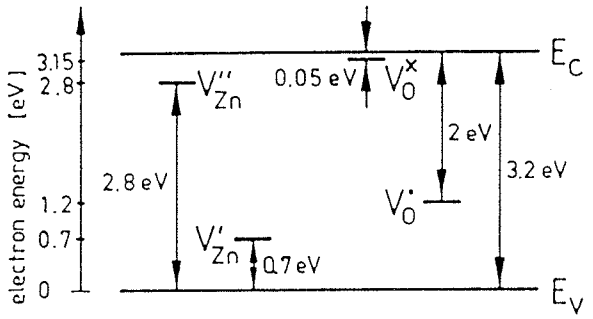

Figure 1: Energy - band diagram of ZnO[3]

2.2. Varistor Microstructure

Varistor is realised by homogenisation of ZnO powder with the oxide additives of Bi, Sb, Mn, Co, Cr, Ni, Al, etc. Forming of such a composite is performed by one of the ceramic procedures (dry pressing for example). After sintering, final polycrystalline ceramic structure, characterised by unique grain boundary properties that contribute to the nonlinear I-V varistor characteristics is obtained. As the flow of the electric current is controlled by electrostatic potential barrier of the grain boundaries, its electrical activity and microstructure can be adapted to provide the desired special properties of the material. For this reason many material scientists have been extensively studied ZnO varistor mictrostructures, especially those of the grain boundaries[4-6]. Their main concern was to investigate various crystalline phases, their

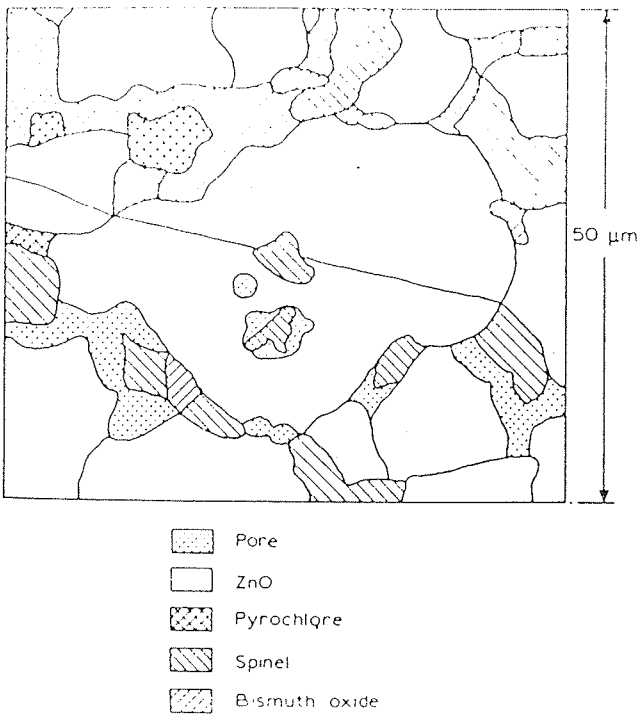

Figure 2: Actual structure of ZnO varistor[7]

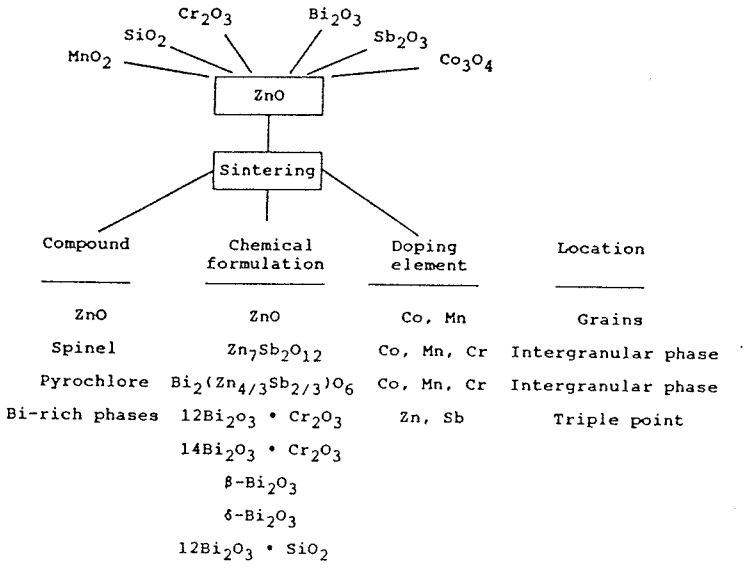

Figure 3: Microstructural components of the ZnO varistor[8]

chemical formulation and dopants in various phases comprised in varistor structure on the one hand, and their influence on electrical characteristics on the other hand. Schematic view of the real ZnO varistor microstructure is shown in Fig. 2., which illustrates ZnO grains surrounded by spinel, pyrochlore and several Bismuth phases including intra- and intergranular porosity. The major findings of the microstructure analyses are summarised in Fig. 3.. When the grain is etched out with acid, intergranular phases appear as a three dimensional network, which is electrically conductive under certain conditions (high field, high temperature, etc.)

Microstructural study resulted in a vary important conclusion. The primitive varistor or basic building block of a ZnO varistor is a boundary between two grains, being formed during sintering. Different chemical elements and ZnO intrinsic defects are being distributed during sintering so that the grain boundary region becomes highly resistive ($R_{gb} \approx 10^{12}$ Ωcm) and the grain interior highly conductive ($R_g \approx$ 1-10 Ωcm). Abrupt conductivity change on the grain boundary suggests the existence of the potential barrier and the depletion layer on both sides of the boundary inside the ZnO grain. It should be pointed out that each grain boundary in doped ZnO shows a nonlinear I-V characteristics, except in the cases, where one of the grains has high symmetry (e.g. basal plane), showing special electrical properties[4]. Several studies have indicated the presence of a thin (<20Å) and homogeneous layer of Bi[3,9] and excess oxygen at the grain boundary[10] as shown in Fig.4.

The role of Bi in grain boundary activation is very interesting. On the one hand, no varistor effect is obtained without Bi doping. On the other hand Bi concentration at the grain boundary stays unchanged in the cases of postsintering annealing or electric loading, when I-V

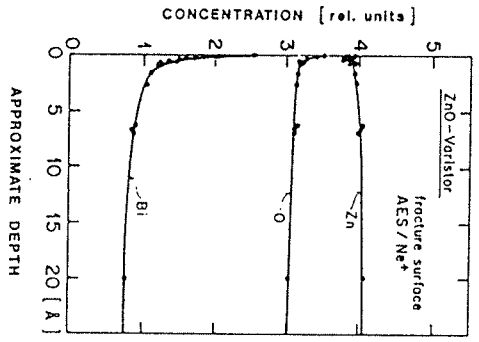

Figure 4: ZnO varistor grain boundaries AES chemical analysis[10]

characteristic in the prebreakdown region changes its shape[10]. Similarly, no correlation has been found between net charge stored at the grain boundary and Bi concentration. That's why it is generally assumed that absorbed Bi ions create some intrinsic interface defects which are capable of capturing an excess electron.

Unlike Bi ions, O ions are completely mobile[10], their concentration on the grain boundary being in the direct correlation to the I-V characteristic change, i.e. to the potential barrier height and the net charge stored at the grain boundary[11].

2.3. Varistor Physics

Several physical models have been proposed in the past to explain conductive mechanism in varistor[12,13]. Their inadequacy was in the fact that they could explain just

some of the experimental results. Advances in microstructural analysis at the atomic level and a wide range of electrical and spectroscopical measurement techniques helped Pike[14] to establish the most comprehensive model, being later refined by Greuter and Blatter[11,15].

The model is based on the fact that a net interface charge at the grain boundary results from the trapping of an excess electron (or hole) by the appropriate interface states. The interface charge Q_i is screened by the ionised bulk defects N_o, associated with intrinsic defects such as Zinc interstitial or Oxygen vacancies, in order to establish the overall charge neutrality. Visualising this process in an energy band diagram corresponds to the formation of a double Schottky potential barrier at the grain boundary as shown in Fig. 5. The current flowing across the grain boundary is controlled by the applied bias and the temperature dependent height of the potential barrier $\varnothing_b$ (V, T). Solving the Poisson equation, several authors[12,13,14] obtained that the potential barrier height is 0.9-1.0 eV. It should be pointed out that an increase in Q_i results in a larger $\varnothing_b$, whereas a higher N_o reduces $\varnothing_b$. Applying thermoionic emission model, current flow through the grain boundary can be described by the equation:

$$J = A T^2 \exp\left(-(e\varnothing_s - \in_n)/kT\right) (1 - \exp(-eV/kT)),$$

where A is a constant containing Richardson's constant, $\in_n = E_c - E_f$ and V is the applied voltage.

The existence of the following four current components on the interface is obvious: the thermally emitted electrons travelling from the left to the right and backwards (being suppressed by the factor exp(-eV/kT)) and small current of the electrons being trapped and remitted from the interface states. The two last currents are responsible for the updating of Q_i, and actually control the main current flowing over the barrier[15].

When a bias is applied to the junction (V< 3 V), $\varnothing_b$ will rapidly decay for a fixed Q_i. However, if through the lowering of $\varnothing_b$ new empty interface states can be filled, Q_i increases and $\varnothing_b$ is efficiently stabilised keeping the leakage current low. This is usually referred to as a pinning of b by the interface states. The strong pinning leads to a concentration of the voltage drop within a 1000Å wide region on the positively biased side of the junction. Near the top of the barrier, electric fields as high as 1 MV/cm can build up. Under this condition some electrons can get enough kinetic energy (became "hot") to create minority carriers by means of the impact ionisation. The holes created in this way, diffuse back to the interface ($\tau_t < 10^{-10}$ s), partly compensate Q_i and abruptly lower $\varnothing_b$ initiating the breakdown. Energy-band diagram of "hot" electron-hole induced varistor breakdown, different trajectories of "hot" electrons and the creation by impact ionisation are shown in Fig. 6.

As the optical-phonon scattering at low energies (0.1-0.4 eV) is the dominant loss mechanism in ZnO, a high starting field near the interface is the most important to overcome this critical energy range. On the basis of the

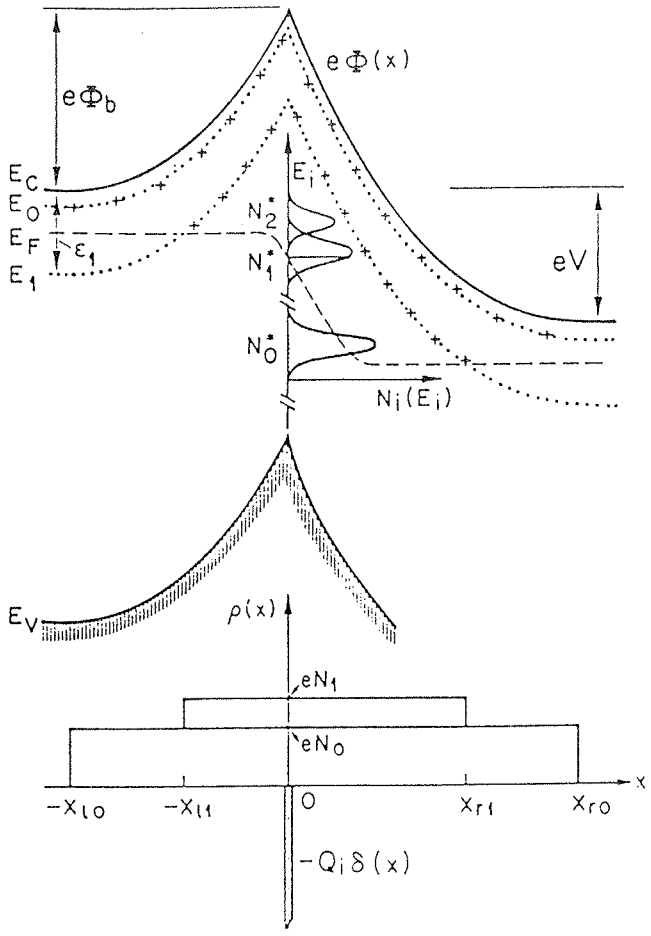

Figure 5: Double Schottky barrier at a negatively charged grain boundary[11]

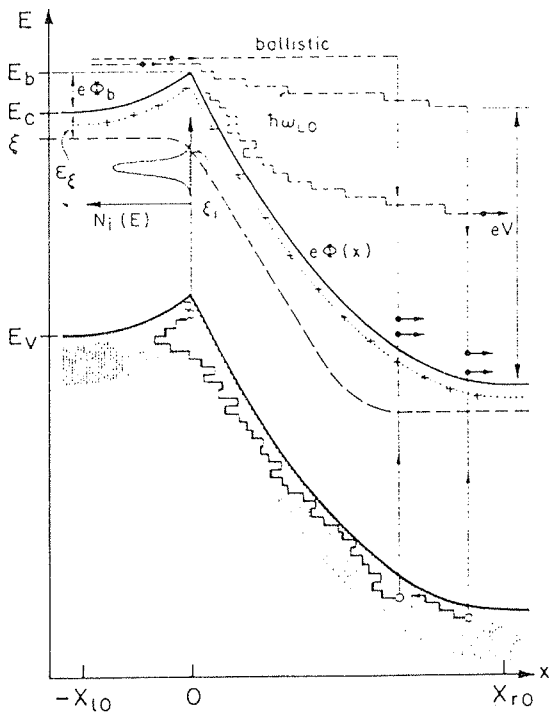

Figure 6: Energy-band diagram of a grain boundary barrier illustrating the hole induced breakdown[14]

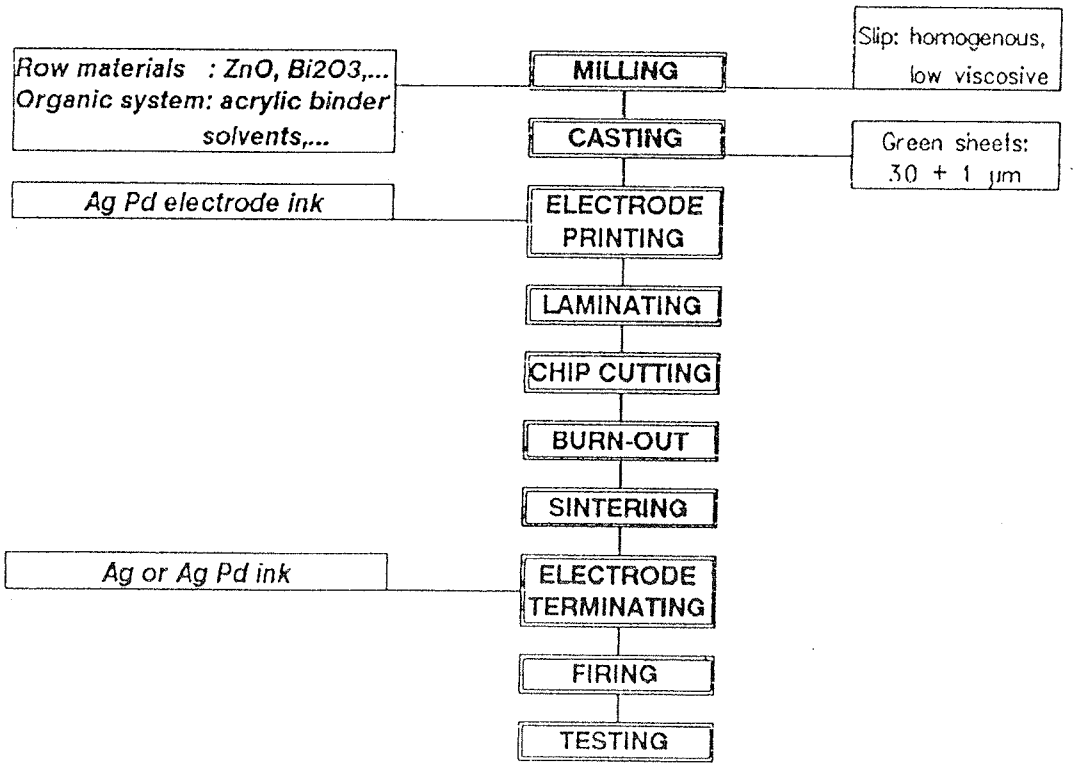

Figure 7: MLV fabrication process steps

data on threshold energy for electron-hole pair creation in ZnO ($E_{th} \approx 3.7$ eV) and the yield of the hole production and using the described model Greuter et. al.[15] estimated single grain boundary junction breakdown to be $V_b = 3.3\text{-}3.8$ V, which is in a very good agreement with the experimental results.

Besides, "hot"-electron-hole induced avalanche breakdown model can explain most basic experimental observations such as: high coefficient of nonlinearity ($\alpha > 40$) and its dependence on doping, small negative signal capacitance at large bias, voltage overshoot effect under the excitation with fast pulses, electroluminescence phenomena observed at grain boundaries and many other[11].

3. Multilayer Chip Varistor

Ceramic tape casting and especially green sheet lamination technology have been very intensively developing during the last twenty years, in the first place owing to the development of the multilayer ceramic capacitor and hybrid integrated circuit substrates. These technologies set the basis for the development of the multilayer chip varistor.

Although the first article was published by Shohata et. al.[16] in 1981 there has been little published about this new protection component, which became commercially available not more than two years ago.

3.1. Technology

3.1.1. Fabrication Process

Green sheet lamination process applied in presented MLV production experience is shown in Fig. 7. Varistor processing was based on fine particle high purity ZnO and other dopants. They were mixed in a nonaqueous system based on an acrylic binder in a ball mill for 15-20 h. The homogeneous low viscosity ceramic slip was tape cast into 30-100 µm thick sheets. Tape cutting was followed by AgPd internal electrode screen printing and their stacking into 10 x 10 cm large green ceramic blocks. Ceramic blocks were then laminated and cut into chips sized 2.5 x 1.5 mm, 3.2 x 2.5 mm and 5.7 x 5.0 mm, which are popular SMD dimensions. After binder burn out, chips were sintered in an air atmosphere furnace at the temperature of 950-1100°C. Finally, external AgPd electrodes were attached and fired to make contact with comb-like inner electrodes as shown in Fig. 8.. Fig. 9 illustrates the outside view and final dimensions of realised chips while Fig. 10 shows optical microscope photographs of the microstructure of the cross sectioned MLV.

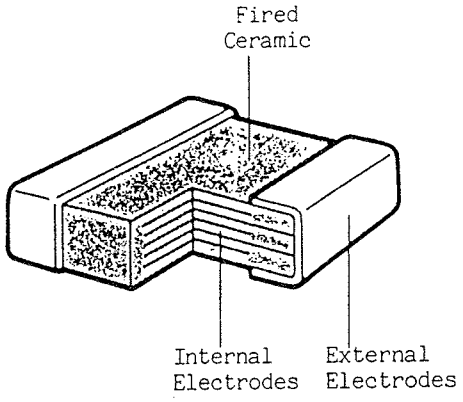

Figure 8: A cross sectional illustration of a MLV

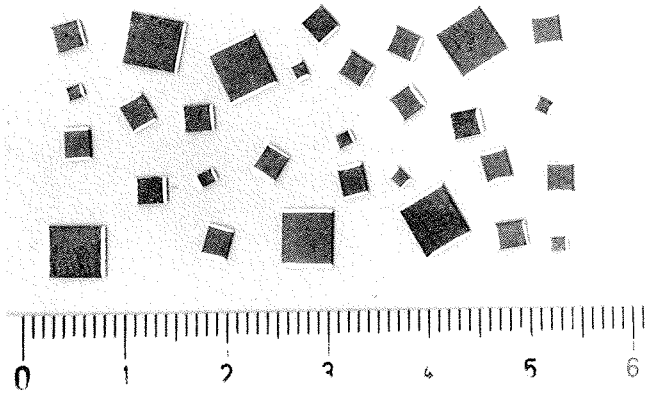

Figure 9: Outside view of differently sized MLVs

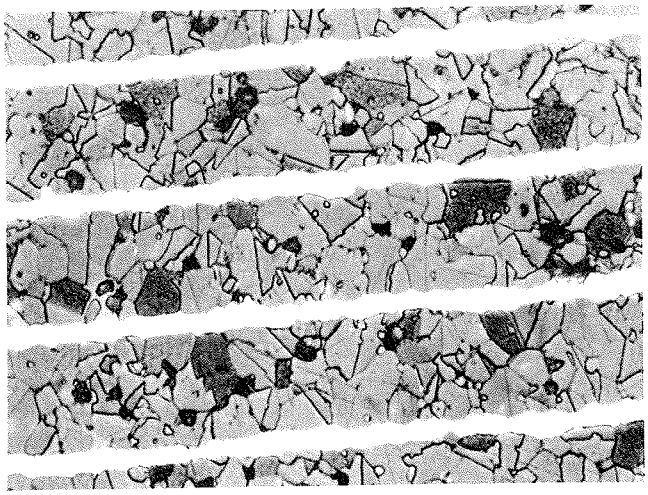

Figure 10: Microstructure photographs of a cross section of an MLV

3.1.2. Varistor Compositions

Shohata et. al.[17] concluded that the utilisation of Bi_2O_3 in MLV ceramic system is not possible because it easily reacts with any metal used for internal electrodes, destroying the multilayer structure. That's why, instead Bi_2O_3, they especially developed and suggested the usage of borosilicate-lead-zinc glass. Microstructural analysis of the ceramic- electrode interface[18] showed increased concentration of Bi in the case of low sintering temperatures (950°C), while at higher temperatures (1100°C) a lamelar reaction product, identified as $PdBi_2O_4$, was observed only in the "pockets" of a melt at the interface. TEM/EDS studies of the interface confirm that the reaction layer is neither continuous nor monophase. Due to that and opposite to the statements in [17], it was shown in [19] and it will be shown in this paper that usage of Bi_2O_3 is possible in varistor system without consequences either to the electrical characteristics or varistor reliability. Having this in mind, special varistor composition was designed[20,21], comprising ZnO (>92 wt %) and oxide additives such as Bi_2O_3, MnO, CoO, Sb_2O_3, etc. As the composition presents one of the design parameters, the care was also taken of the fact, that some differences exist in the case of the bulk varistors and MLV, the final ceramic layer thickness being both small and comparable to the grain size in the later. Two such examples are illustrated in Fig. 11. and Fig. 12.. They show the dependence of nonlinearity coefficient and specific voltage on sintering temperature in the case of MLV (layer thickness ≈ 17 μm) and bulk varistor (d ≈ 1 mm), realised with the same composition.

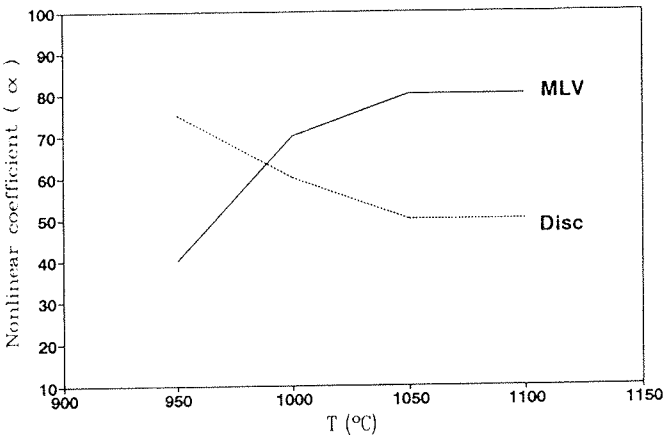

Figure 11: Nonlinear coefficient - α Versus sintering temperature

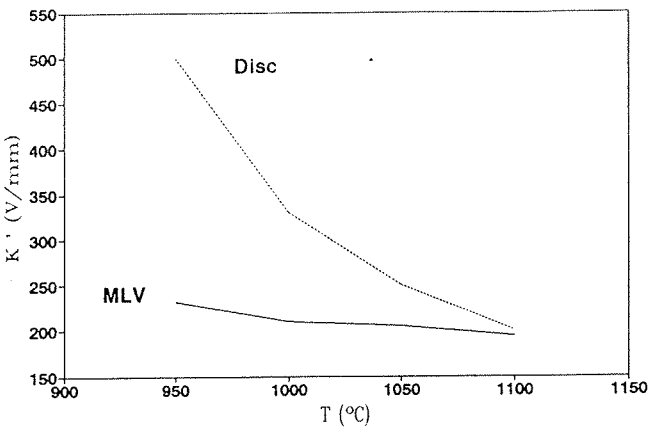

Figure 12: Specific voltage versus sintering temperature

3.1.3. Ceramic Foil

Presently, it is possible to use two processes for thin ceramic foil formation: extrusion & stretching process and doctor-blade tape casting process. We applied both processes to form varistor ceramic foil. The results of the second process will be shown in this paper. Nonaqueous tape casting system, containing acrylic binder, solvents, defloculants, plasticiser and some other additives, was used, enabling formation of homogeneous, stabile, low viscosity slurry, during homogenisation of varistor ceramic system. After homogenisation, the slurry travels on the carrier surface beneath the blade of the knife, that controls the thickness of the out-coming layer. When the solvent evaporates, the fine solid particles coalesce into a relatively dense flexible film that may be stripped from the carrier surface in a continuous sheet. Foils obtained in such a way have good mechanical firmness (enabling simple manipulation) and no pin hole defects. Besides, in the whole range of thicknesses no "skin" effect has been observed as illustrated in Fig.

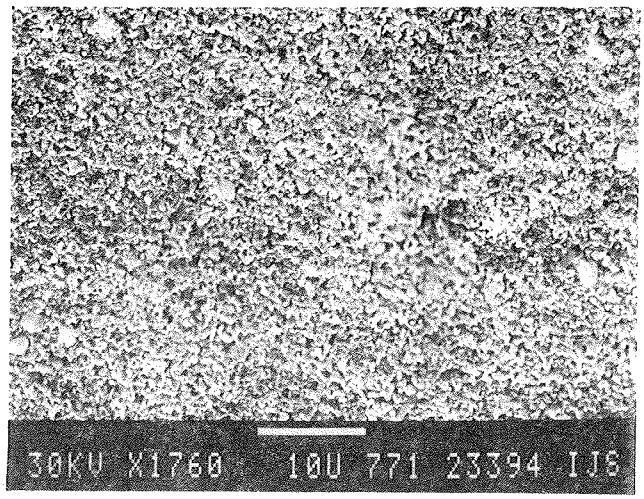

Figure 13: SEM photograph of the tape cast foil surface

13., showing the appearance of the surface of the varistor tape cast foil.

3.2 Chip Design and Structure

Based on considerations in #2.3. the overall varistor breakdown voltages could be calculated as n x 3.6 V, n being the mean number of grain boundaries along the shortest linear path between electrodes. Following this principle a low voltage MLV can be designed combining the ratio of the ceramic foil thickness and ZnO grain size. However, this procedure is limited by the opposing requirements for certain electrical characteristics, processing and surface mount technology.

Fig. 14. shows the breakdown voltages (at 1 mA) dependencies on sintering temperature with green sheet thickness as a parameter, while Fig. 15. shows the photograph of a) 4 V and b) 56 V sectioned MLV at the same magnification.

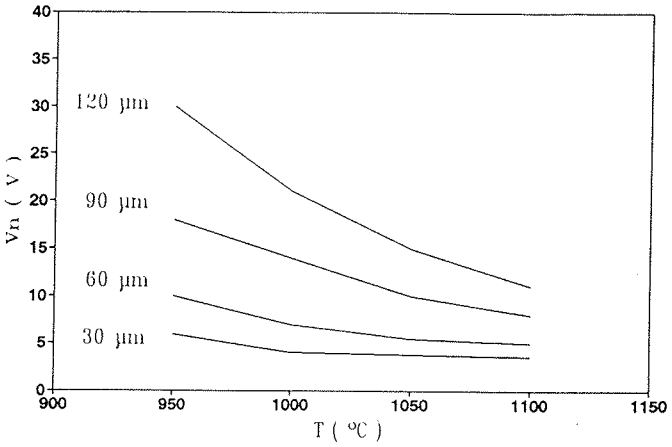

Figure 14: Breakdown voltage versus sintering temperature for different sheet thicknesses

As seen in Fig. 8. inner electrodes are set parallel to each other, where each second electrode is displaced to the same side, so that one group of electrodes is electrically connected to the end termination on one side and the other to the end termination on the other side of the chip. This finger- or comb-like electrode structure enables optimum usage of material volume and shows the whole array of other advantages. Inner electrodes

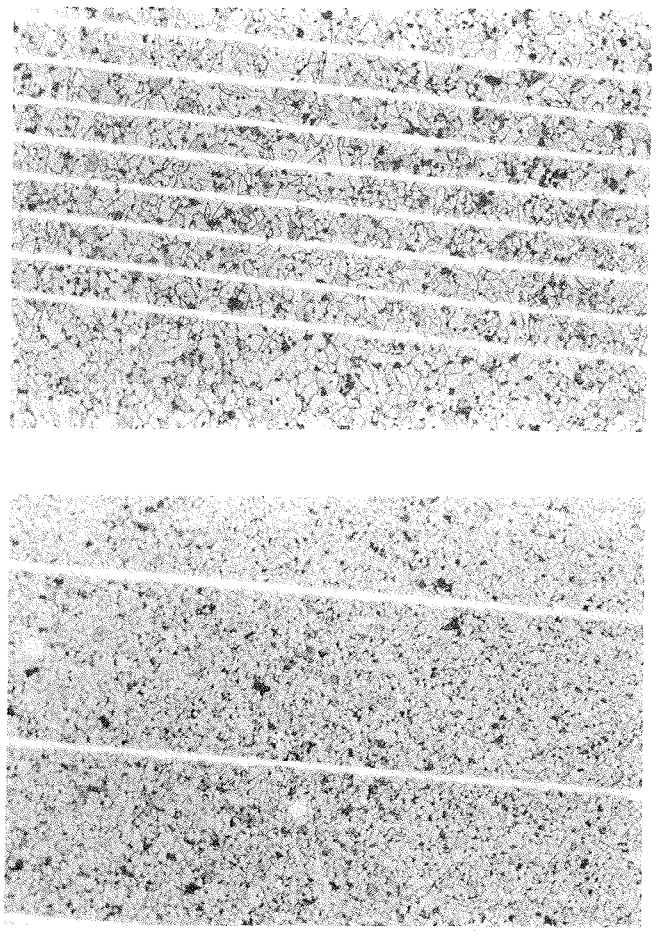

Figure 15: Photograph of cross-sectioned 4 V and 56 V MLV

are encircled with varistor ceramics, so that there are no parasitic structures between adjacent electrodes, meaning that there are no paths causing surface leakage currents or enabling flash-over breakdown. Moreover, this way of electrode design enables their relatively large active surface with respect to chip volume. This is especially evident when compared with the bulk varistor. This electrode disposition enables very uniform current and energy volume distribution, avoiding "hot" spots in the structure, which is of great importance when stability and reliability are concerned.

Beside inner electrode surface, their periphery is important as well. Being very long it facilitates peripheral electrode current injection, similarly as with high current power transistors and acts as an "amortiser" of extremely high current surges.

Being good heat conductors inner electrodes have dual positive role. In the case of ambient heating, they minimise large temperature differences between chip sides, helping uniform microstructure formation and prevent defect diffusion and electrical characteristic degradation. In this case they act as ideal internal heaters. On the other hand, during internal heating due to DC, AC or pulse loading, they conduct heat outwards and act as coolers. This provides fast varistor heat dissipation through the volume, shifting failure mechanism toward higher temperatures. This is one of the reasons that MLV is the only varistor capable of operating at +125°C, whereas the maximum operating temperature of other varistors is +85°C.

3.3. Electrical Properties

3.3.1. Current-Voltage Characteristics

MLVs with breakdown voltage in the range from 4 V to 100 V were realised in the above described way. It should be emphasised, that 4 V breakdown is practically, the lowest theoretically possible breakdown in ZnO varistor (see #2.3.). Achieved result illustrates that, it is possible to realise controllable microstructure, such, that in the cross section between the adjacent large surface electrodes there is only one grain boundary on the average, i.e. the whole structure acts as one large equivalent monobarrier.

Fig. 16 a) and b) shows symmetrical AC I-V characteristics of 4 V and 56 V varistor respectively. The sharp breakdown knee is typical for these high devices with a clearly defined threshold voltage. This is even more evident in Fig. 17, presenting measured I-V relationships. Wide current range measurements were provided using DC technique up to 10 mA and the pulse (8/20 μs) technique above this value. In both cases characteristics show distinct difference between the prebreakdown and breakdown region, which extends over six (for 4 V MLV) to seven (for 56 V MLV) orders of magnitude of current. Typical values of the nonlinear coefficient α measured

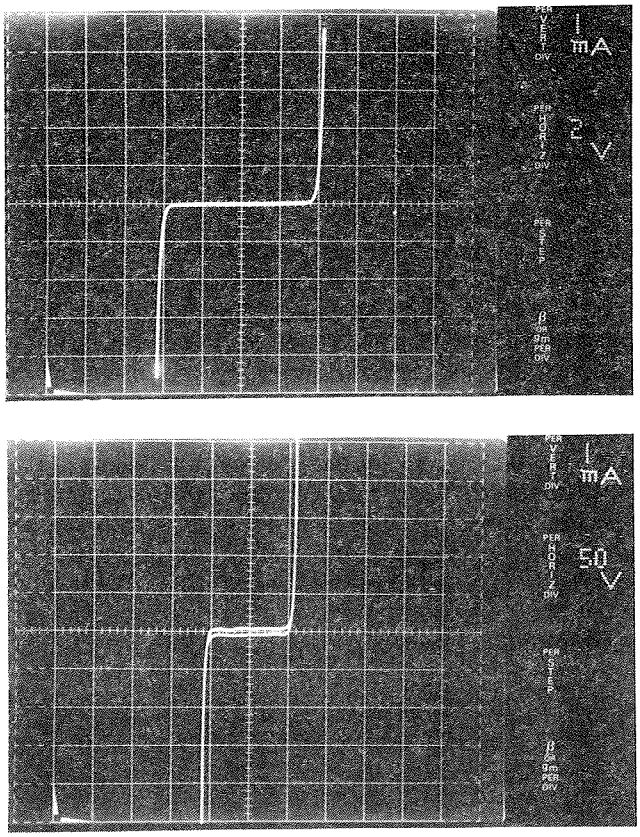

Figure 16: AC current-voltage characteristics of the a) 4 V and b) 56 V MLV

by the ALPHA meter in the current range from 1-10 mA usually exceeds 25 and in some cases reaches values over 50. It is especially important that α has so high value within the whole breakdown region. Fig.18. illustrates the example of 33 V MLV (5.7 x 5.0 mm), where α has the value >15 in the current range up to 1000 A, above which its value decreases and correlates with upturn region on the I-V characteristics. Protection level coefficient, defined as the ratio of clamping voltage for any specified current and the breakdown voltage at 1 mA, has the value < 2.5 up to the current value of 1000 A, increasing for the higher currents. It means that MLV provides very effective protection in the wide current range.

In the prebreakdown region MLV shows very low leakage current (typically < 5 μA), meaning at the same time, a low DC watt loss upon steady state operating voltage, typically set between 75-85 % of the threshold voltage. Although the leakage current increases with temperature, as shown in Fig. 19., for the case of 4 V MLV measured at V_{dc} = 3 V, it holds relatively low value even for the temperatures as high as +125°C, enabling its normal operation in that temperature range as well (see #3.2.). The linear relationship between current and temperature in semilogarithmic scale confirms the thermoionic emission mechanism, i.e. the validity of physical model described in #2.3.. The measured threshold voltage temperature coefficient is much lower than 0.01 %/°C in the temperature range from +25°C to +85°C.

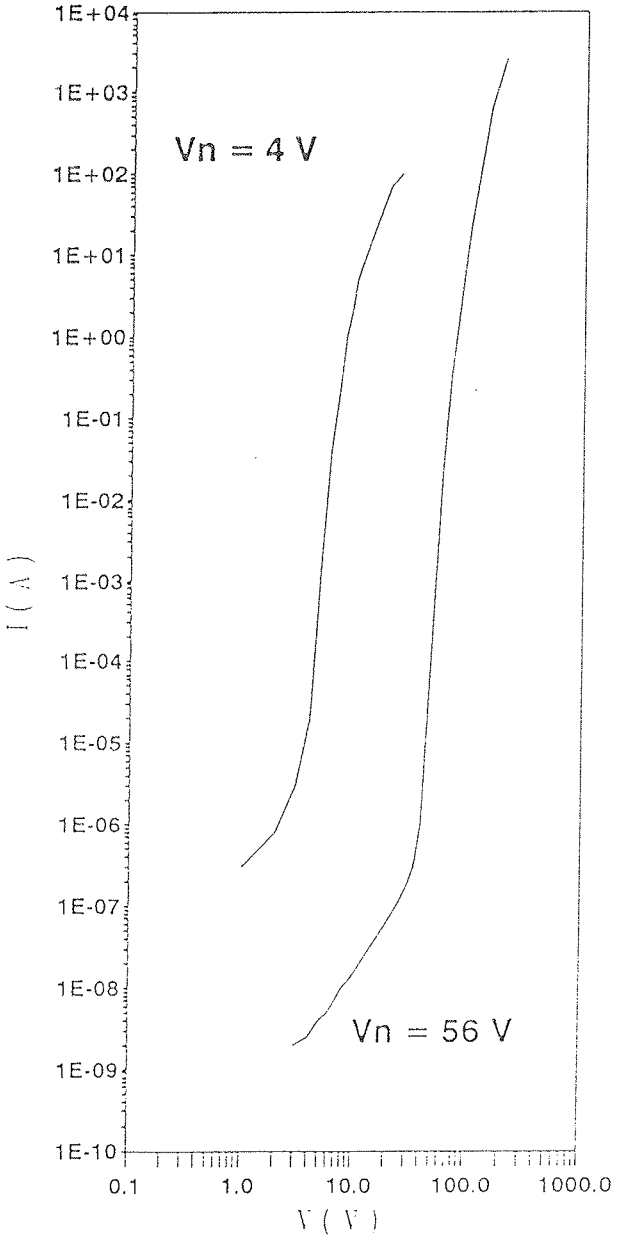

Figure 17: Current-voltage characteristics of 4 V (3.2 x 2.5 mm) and 56 V (5.7 x 5.0 mm) MLV

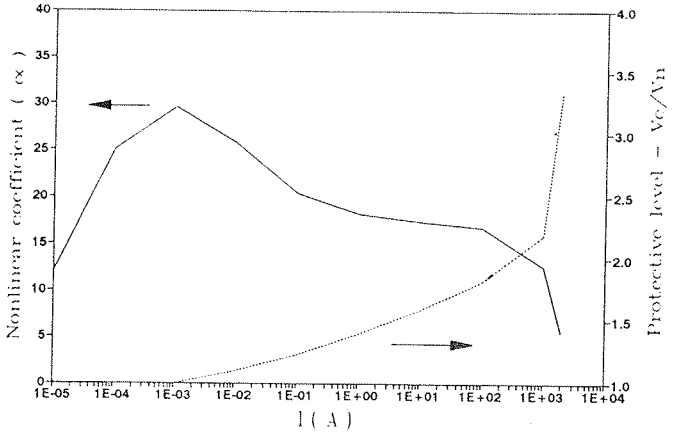

Figure 18: Nonlinear coefficient-α and protective level versus current

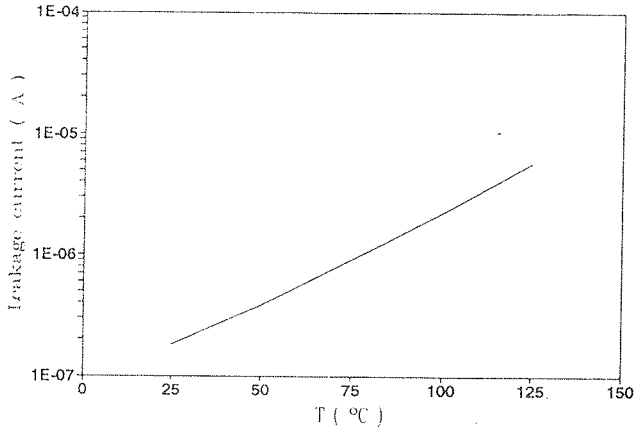

Figure 19: Temperature dependence of DC stand-by current (V_{dc} = 3 V) of the 4 V MLV

3.3.2. Capacitance and Response Time

Dielectric constant of ZnO is relatively small (≈ 10), while the effective dielectric constant of the varistor ceramics is about 100 higher as the consequence of intergranular barriers and their nature (see #2.3.). Capacitance of MLV with different breakdown voltages measured at 1 kHz, ranged from 0.5-40 nF, depending on the chip dimensions, layer thickness and their number. MLV capacitance is relatively stable over a wide frequency range, up to 1 MHz, as shown in Fig. 20.. The same figure shows bell shaped frequency-loss factor characteristics with the minimum value typically at 10 kHz. , The capacitance temperature change, in the temperature range from +25° to +85°C, is < 15 %.

Such a medium MLV capacitance value, which to a certain extent can be designed is especially desirable in specific applications to be discussed in the Part II: Advantages and Applications.

MLV chip has very low inductance, typically < 1.5 nH. The voltage response overshoot effect, being controlled by inherent parasitic lead inductance, is typically not observed in the case of 8/20 μs pulse, as illustrated in Fig. 21.. This figure shows 54 V pulse response charac-

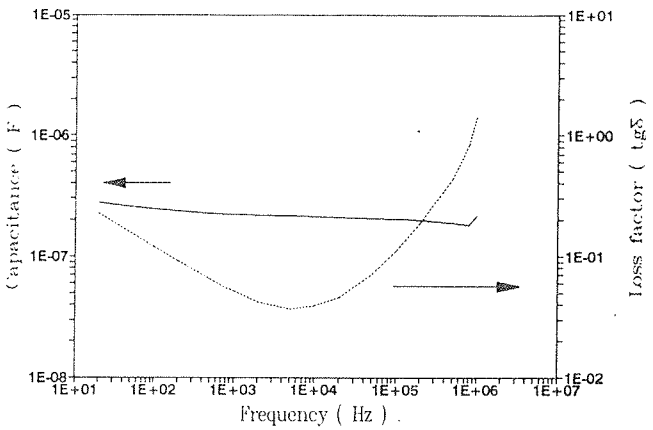

Figure 20: Capacitance and loss factor variation with frequency of the 8 V MLV

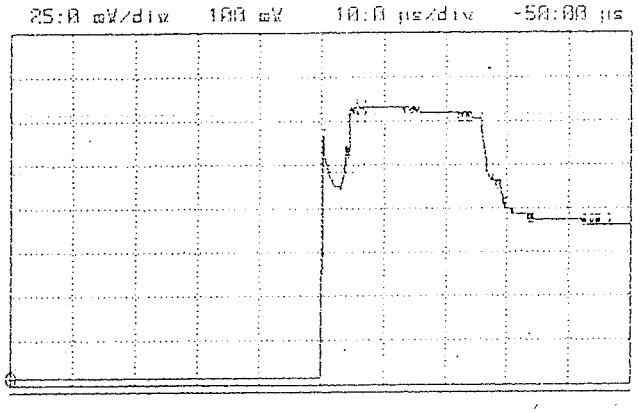

Figure 21: Pulse absorption characteristics of 33 V MLV (8/20 µs, 20 A; Hor. : 10 µs/div, Ver. : 351 x 25 mV/div)

teristics of a 33 V MLV after triggering with 20 A of 8/20 µs pulse. Our present equipment has enabled us to estimate the response time of MLV to be definitely < 5 ns, being adequate for protection in electrostatic discharge environment.

3.3.3.Stability and Reliability

MLV stability and reliability are especially important regarding the fact that it is intended to be protective device. To estimate its stability and reliability a number of tests were performed. The result of high current amplitude and high energy surge withstand capability tests are shown in Fig. 22 and 23.. Standard surge pulse shapes of 8/20 µs and 10/1000 µs were used. The relative threshold voltage change is plotted as a function of the number of surges. It is evident in Fig. 22. that in the case of 8/20 µs pulse threshold voltage increases somewhat faster during the first 10 surges, the change being slower afterwards. The change is lower than 5 %, even after 500 surges. The value of this result can be fully evaluated, having in mind that threshold voltage change of 33 V standard 20 mm disc varistor is higher than 10 % already after 100 to 150 surges. Similar results were obtained in the case of 10/1000 s pulse as shown in Fig. 23. It illustrates excellent stability of MLV

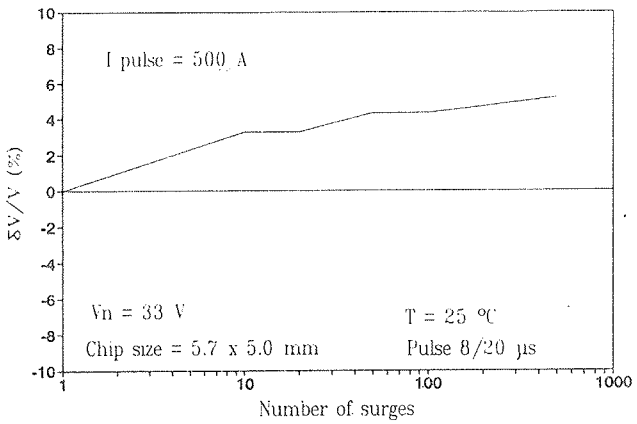

Figure 22: Repetitive pulse capability (30 s between pulses)

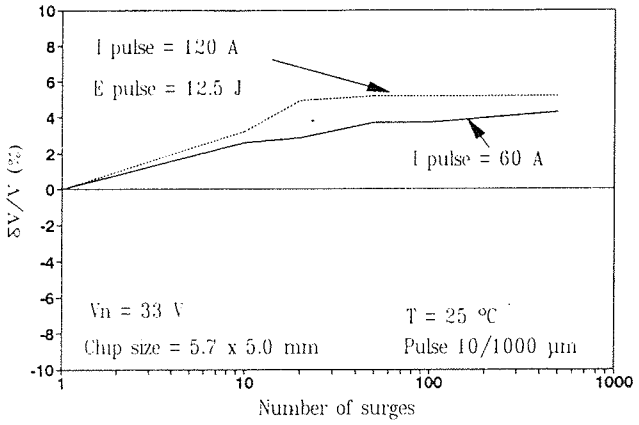

Figure 23: High energy repetitive pulse capability (30 s between pulses)

even in the case of 12.5 J pulses. During this test 33 V MLV was cumulatively absorbing the energy of more than 6 kJ in the period of 4 h, without substantially changing its characteristics. Similar threshold voltage change in the cases of different MLV pulse loading, suggests activation of the same failure mechanism, with no regard to the pulse duration or its shape.

As, varistors are, generally speaking, very sensitive to DC loading in the prebreakdown region, a continuous power dissipation life test was performed on 4 V MLV. The DC applied voltage was higher than the threshold voltage, i.e. the 4 V MLV was subjected to a 10 mA and 30 mA current. A stability that can not be obtained with any low voltage disc varistor is apparent in Fig. 24. Even after 80 min of loading with current of 30 mA, the threshold voltage change was not higher than 15 %. This result, as well as all the others, again confirms the consideration in #3.2. and proves the possibility of realising of a very homogeneous and ordered mictrostructure by means of thin ceramic layer technology.

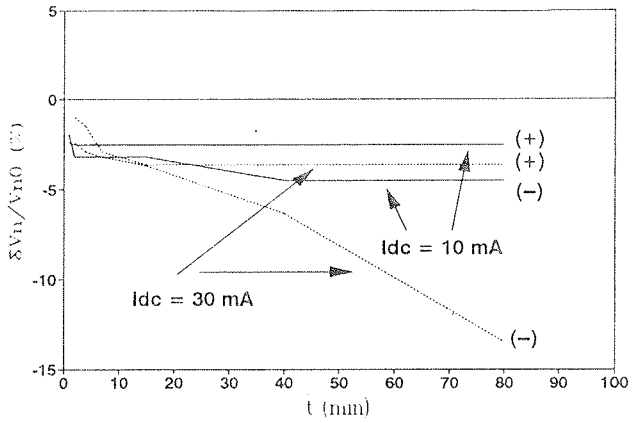

Figure 24: Continuous power dissipation life test of 4 V MLV. The marks (+) and (-) indicate the Vn change in the same and the opposite polarity with DC bias.

4. Conclusion

A low voltage MLV was developed using tape casting and green sheet lamination technology. Obtained electrical characteristics showed that the utilisation of Bi_2O_3 is possible in MLV ceramic system. Namely, MLV has high nonlinearity coefficient in the whole breakdown range, i.e. low clamping level, providing high protection efficiency. It was also shown that with respect to its planar surface MLV can withstand pulse density loading higher than 7000 A/cm^2, being far higher than in any protective device known today. Besides, leakage current in prebreakdown region has relatively small value even in the temperature range around +125°C. Very low inductance of chip MLV enables response time shorter than 5 ns, eliminating to a great extent voltage response overshoot effect.

Life test results, and especially repetitive pulse capability tests show MLV excellent capability to withstand great number of short high voltage surges as well as long high energy surges. Practically all static and dynamic characteristics as well as MLV stability lead to the conclusion that and MLV is favourable low voltage protective device.

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Zoran Živič, M.S.E.E.
KEKO, d.d.
Ceramic Capacitor Factory
Grajski Trg 15
68360 Žužemberk
Slovenia
tel. + 386 68 87 230
fax + 386 68 87 315

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