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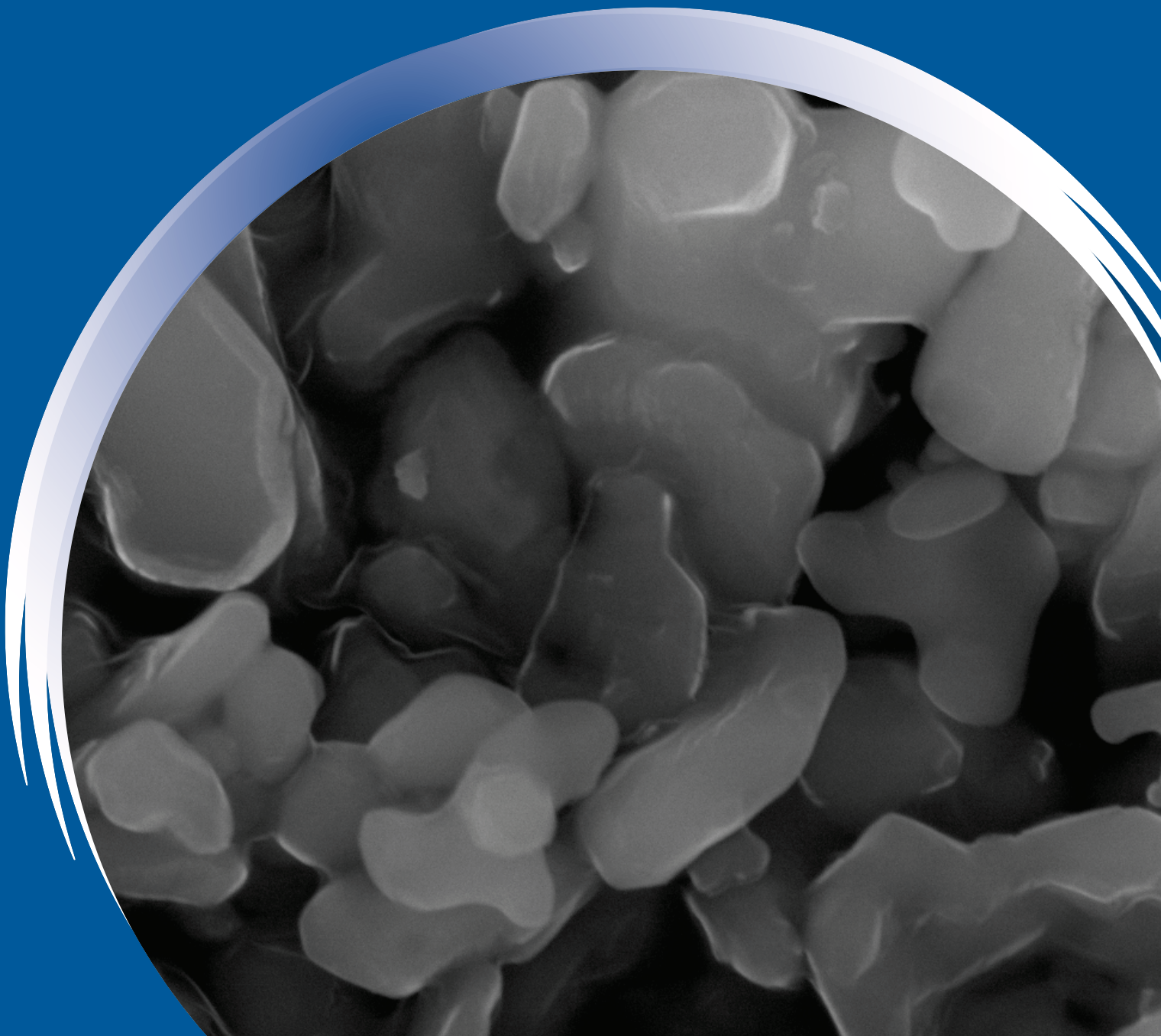

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Memory Efficient High Speed Systolic Array Architecture Design with Multiplexed Distributed Arithmetic for 2D DTCWT Computation on FPGA

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Abstract: This paper presents customized Systolic Array Architecture (SAA) design of Dual Tree Complex Wavelet (DTCWT) sub band computation based on multiplexed Distributed Arithmetic Algorithm (DAA). The proposed architecture is memory efficient and operates at frequencies greater than 300 MHz in decomposing 256 x 256 input image. Three architectures such as reduced order structure, multiplexed DA structure and zero pad structure are designed and evaluated for its performances for DTCWT computation minimizing arithmetic operations with improved latency. The proposed design is modeled in Verilog HDL and is implemented on Spartan-6 and Virtex-5 FPGA considering Xilinx ISE FPGA design flow. The latency of proposed architectures is evaluated to be 15 clock cycles and throughput is estimated to be 4 outputs for every 5 clock cycles. The SAA architecture occupies less than 12% of FPGA resources and consumes less than 10 mW of power on FPGA platform.

Keywords: Memory efficient, high speed, FPGA, Systolic Array, Distributed Arithmetic

Spominsko učinkovita arhitektura sistoličnega polja visokih hitrosti za 2D DTCWT računanja na FPGA

Izvleček: Članek opisuje dizajn arhitekture sistoličnega polja za računanje kompleksne dvoslojne valovnice na osnovi multipleksnega distribuiranega aritmetičnega algoritma. Predlagana struktura je spominsko učinkovito in deluje s frekvenco večjo od 300 MHz pri dekompoziciji slike velikosti 256 x 256. Dizajn je narejen v Verilog HDL okolju in implementiran na Spartan-6 in Virtex-5 FPGA. Latenca arhitekture je 15 časovnih ciklov in propustnost 4 izračuni na 5 časovnih ciklov. Arhitektura zaseda manj kot 12 % FPGA spomin ain porabi 10 mW moči.

Ključne besede: učinkovitost spomina; visoke hitrosti; FPGA; sistolično polje; dinamična aritmetika

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1 Introduction

Wavelets have played an important role in signal and image processing applications supporting both time and frequency localization property. Hardware implementation of Discrete Wavelet Transform (DWT) is achieved by filter bank structures that are flexible and computationally less intensive. Down sampling and up sampling in the analysis and synthesis filter bank structures in DWT introduce aliasing effects leading to shift variance and directionality selectivity limitations. Complex Wavelet Transforms (CWT) and Un-decimated DWT (UDWT) have been reported in literature to overcome limitations of DWT. CWT implementation was presented by Nick Kingsbury [1] with two tree structure

for signal decomposition for image processing applications. Ioana Adam [2] in his PhD thesis presented CWT for image denoising which was performed using separable filters generating high pass sub bands providing directional information in six orientations. Selesnick et al [3] in their work have presented signal and image processing applications using Dual Tree CWT (DTCWT). Olhede and Metikas [4] have presented four different types of complex wavelets for both 1D and 2D signal decomposition. Computing DTCWT output coefficients is twice complex than DWT computation as it generates 2N DWT output coefficients, where N is the input data size. Simplified structures for computing DTCWT are presented in [5-7] that require two real DWT filter bank structures or two critically sampled DWTs that process the input data in parallel. DTCWT is well suited for image analysis such as image de-noising, texture analysis, segmentation, classification, motion estimation, watermarking and compression [6]. With additional directional features in wavelet domain arising in DTCTW sub bands image processing algorithms provide better performances for real time applications [8]. Computation complexity of DTCWT can be addressed by implementing DTCWT on FPGA platform. Several architectures for FPGA implementation of DWT [9-25] is reported in literature based on lifting scheme, distributed arithmetic algorithm, multiplierless scheme, systolic array algorithm, serial architectures, parallel architectures etc. Divakara et al [25] have reported on FPGA implementation of DTCWT for image processing applications based on reorder and symmetric structure. For improving the processing speed and reducing computation complexity of DTCWT computation redundancy among filter coefficients need be eliminated and customized arithmetic operators need to be designed. In this paper, high speed area efficient architectures for DTCWT are presented and the area, timing metrics of three different architectures are compared considering Xilinx Spartan-6 FPGA device. The proposed architectures are implemented on Spartan-6 development kit and co-simulation is performed for validation of architecture functionality. Advanced optimization options are enabled during synthesis process for further improvement in area and timing performances. Section 2 briefly introduces DTCWT algorithm and review of various architectures and methods for DWT is presented. Section 3 presents discussion on improved methods for DTCWT architectures, section 4 presents implementation details and conclusion is presented in section 5.

2 DTCWT

Kingsbury demonstrated the shift invariance property of DTCWT by using both real and imaginary tree [6] structures for signal decomposition. The aliasing effects in DWT are addressed by having two tree (tree a and tree b) structure for decomposition of input data (X) using DTCWT as shown in Figure 1. The four filters required for DTCWT decomposition are represented as La (low pass tree a coefficient), Ha (high pass tree a filter coefficient) and Lb (low pass tree b filter coefficient), Hb (high pass tree b filter coefficient). The filter coefficients defined by Daubechies 10-tap filter are presented in Table 1.

The first stage comprising of two filter pairs processes input image along the rows to generate output samples represented as {y1, y2, y3 and y4}. The second stage comprising of eight filters processes the row processed outputs along the columns to generate eight sub bands denoted as {y11, y12, y21, y22, y31, y32, y41, y42}. The first two outputs represented by y11 and y31 are the low pass sub bands and the remaining are the high pass sub bands. Sum and difference operation with scaling ($1/\sqrt{2}$) is performed on the high pass sub band outputs {y12, y21, y22, y32, y41, y42} to obtain the DTCWT high pass sub bands with six orientations. The complex sub bands of DTCWT after level-1 are represented as {LLR1, LLC1, LHR1, LHC1, HLR1, HLC1, HHR1 and HHC1}. LLR1 and LLC1 are the two low pass

Table 1: Low Pass and High Pass Filter Coefficients

Order	L_a	IL_a	H_a	IH_a	L_b	IL_b	H_b	IH_b
0	0	0	0	0	0.011226979	2	0	0
1	-0.08838834	-22	-0.011226979	-2	0.011226979	2	0	0
2	0.08838834	-22	0.011226979	2	-0.08838834	-22	-0.08838834	-22
3	0.69587998	178	0.08838834	22	0.08838834	22	-0.08838834	-22
4	0.69587998	178	0.08838834	22	0.69587998	178	0.69587998	178
5	0.08838834	22	-0.69587998	-178	0.69587998	178	-0.69587998	-178
6	-0.08838834	-22	0.69587998	178	0.08838834	22	0.08838834	22
7	0.011226979	2	-0.08838834	-22	-0.08838834	-22	0.08838834	22
8	0.011226979	2	-0.08838834	-22	0	0	0.011226979	2
9	0	0	0	0	0	0	-0.011226979	-2

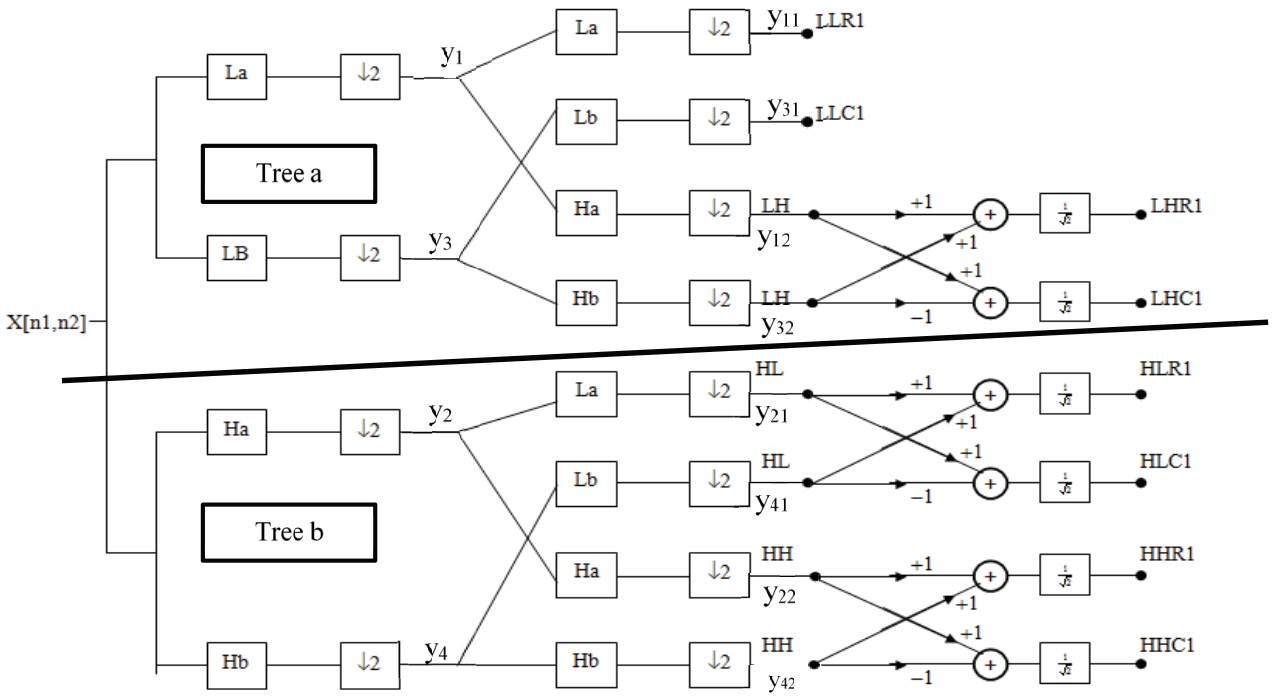

Figure 1: Level-1 2D DTCWT structure

complex sub bands and LHR1, LHC1, HLR1, HLC1, HHR1 and HHC1 are the six high pass complex sub bands. LLR refers to sub band processed by low pass filter in first stage and low pass filter in second stage.

Representing each of the filter coefficients La, Lb, Ha and Hb in binary format requires 16-bit number representation, scaling the filter coefficients by 256 and rounding off to nearest integer is carried out to represent the filter coefficients using 9-bit signed two's complement representations. La represents the low pass tree a filter coefficients and ILa refers to integer low pass tree a filter coefficient obtained after scaling. Similarly by scaling operation the filter coefficients for all other filters are obtained and are presented in Table 1. Computation complexity of DTCWT computation is expressed in terms of number of multipliers and adders required for hardware implementation. Considering single 10-tap filter computing one output coefficient requires 10 multipliers (M) and 9 adders (A). For an image of size N x N for row processing using one filter it requires 10N2 and 9N2 multipliers and adders respectively. For column processing another 10N2 and 9N2 per filter is required. Processing input data using 12 filters (both first stage and second stage), total number of multipliers and adders operations required are 120N2 and 108N2 respectively. In addition to multipliers and adders intermediate registers and memory elements are also required for DTCWT computation. Implementing DTCWT on FPGA platform requires optimizing number of arithmetic operations and memory elements. In literature, several architectures for hardware implementation of DWT optimizing arithmetic operations and memory utilization are reported improvising throughput, latency, operating speed and power dissipation. Few of the most popular methods for DWT implementation improving speed and optimizing area are reviewed in the next section that can provide an insight into the improved methods that are proposed in this work for DTCWT implementation.

2.1 Review of high speed architectures

In order to reduce arithmetic operations and area resources, multipliers are implemented using shift and add logic for computing 1D/2D DWT [10]. Barua et al [11] have presented folded multi-level DWT architecture with 100% hardware utilization requiring 12 multipliers and 16 adders with output latency of 7N. Martina and Masera [12] have presented FPGA implementation of multiplierless architecture based on Distributed Arithmetic (DA) approach considering 9/7 and 5/3 filter with folded structure. Cell based and modified lifting scheme architecture proposed is proposed by Seo and Kim [13] that requires 4 multipliers and 8 adders with Tm (multiplier delay) critical path timing. Pipelined multi-level DWT architecture is designed by Varshney et al [14] that requires 2j multipliers and j adders (j representing number of pixels) with line buffers with 60% hardware utilization and critical path delay

of 2Ta (Ta is adder delay). Distributed arithmetic based DWT architectures for 1D/2D and 3D data processing is presented by Jiang and Crookes [15] with lossy mode configuration. Lifting based 2D DWT architecture that uses non-separable scheme with complex control logic is designed with 10 multipliers and 16 adders that have a critical path Tm [16]. 2D DWT architecture with area efficient schemes and low power logic is designed by Mohanty et al [17], that require 4 multipliers and 8 adders with critical path of Tm + 2Ta. Pipelined multilevel 2D architecture based on 5/3 filter using lifting scheme is implemented on hardware platform considering 4N line buffers with 2 and 4 shifters and subtractors respectively for every stage of decomposition occupying 4N on-chip memory with 2Ta path delay requires 206 slices for every stage and consumes 1220 mW of power operating at 221.44 MHz of frequency [18]. Darji et al [19] have presented design of folded, recursive and pipelined architectures for multi-level decomposition of 2D DWT is designed and implemented on FPGA demonstrating the advantages of dual scanning method operating at speed greater than 200 MHz. Pipelined architecture that processes data in Z-scanning mode is designed by Darji et al [20] based on lifting scheme algorithm replacing multipliers with shift operators and is implemented on FPGA that requires 630 logic elements operating at maximum frequency of 353 MHz. 3D DWT based on parallel lifting algorithm 9/7 wavelet filter is designed by combining two spatial processing and four temporal processing computations [21] which are implemented on FPGA platform that requires 2852 slices and operates ate maximum frequency of 265 MHz. Systolic array based DWT architecture for 2D data with novel data scanning method is designed by Hongda Wang and Chiu-Sing Choy [22] based on lifting scheme algorithm and is implemented on VLSI platform that requires 294579 logic gates and occupies 1508243 micro meters square of area consuming less than 32.78 mW of power. Multiplierless pipelined architecture for 1D and 2D data processing is proposed by Chakraborty et al [23] based on lifting algorithm for DWT computation optimizing area requirement and latency on Spartan 3E FPGA that requires 98 adders with critical path less than T_a. High precision 3D DWT architecture for multi-level decomposition is designed and implemented on FPGA operating at 200 MHz clock consuming less than 329 mW of power for 3D image compression [24]. 2D 3-level DWT architecture is designed to operate at 365 MHz on Virtex-5 platform consuming less than 1261 slices.

Most of the architectures reported in literature focus on reducing arithmetic operations by replacing multipliers by multiplierless logic such as shift and add methods, distributed arithmetic methods and lifting method to reduce computation complexity. Pipelined and parallel processing algorithm and systolic array algorithms have also been used to improve processing speed and throughput in DWT computation. Redundancy in filter coefficients and arithmetic operations in DWT implementations have not been utilized for optimization of are and timing requirement. DTCWT is twice complex than DWT and it is required to reduce the arithmetic operation, memory requirement and processing delay by eliminating redundancy between filter bank pairs. In this work three different types of architectures are designed and implemented on FPGA optimizing area and timing requirements.

3 DTCWT architecture design

As presented in Figure 1 the first stage has four filters and second stage has eight filters. In this section design of three different architectures {reduced order, multiplexed DA and zero pad logic} for DTCWT filter is presented. The filter architecture is designed considering the scaled filter coefficients (ILa) presented in Table 1.

3.1 Reduced order architecture

Expressing the four filter outputs {y_1, y_2, y_3 and y_4} of first stage mathematically considering convolution operation is as in Eq. (1). The filter outputs of all four filters are expressed considering ILa coefficient only. As the input is common to all the four filters and the filter coefficients ILa(0) and ILa(9) are zeros the reduced order structure based on Eq. (1) is designed and is presented in Figure 2.

$$y_1(n)=\begin{pmatrix} x(n)0-[x(n-1)+x(n-2)]ILa(1)+ \\ [x(n-3)+x(n-4)]ILa(3)+[x(n-5)-x(n-6)]ILa(1)+ \\ [x(n-7)-x(n-8)]ILa(7)+x(n-9)0 \end{pmatrix} \quad (1a)$$

$$y_3(n)=\begin{pmatrix} [x(n)+x(n-1)]ILa(7)+[-x(n-2)+x(n-3)]ILa(1)+ \\ [x(n-4)-x(n-5)]ILa(3)+[x(n-6)-x(n-7)]ILa(1)- \\ x(n-8)]ILa(7)+x(n-9)0 \end{pmatrix} \quad (1b)$$

$$y_2(n)=\begin{pmatrix} x(n)0-[-x(n-1)+x(n-2)]ILa(7)+ \\ [x(n-3)+x(n-4)]ILa(1)+[-x(n-5)+x(n-6)]ILa(3)- \\ [x(n-7)+x(n-8)]ILa(1)+x(n-9)0 \end{pmatrix} \quad (1c)$$

$$y_4(n)=\begin{pmatrix} x(n)0+x(n-1)0-[x(n-2)+x(n-3)]ILa(1)+ \\ [x(n-4)-x(n-5)]ILa(3)+[x(n-6)-x(n-7)]ILa(1)+ \\ [x(n-8)-x(n-9)]ILa(7) \end{pmatrix} \quad (1d)$$

In the reduced order structure inputs are loaded into the Serial in Serial out (SISO) register that requires 10 clock cycles. Addition of input samples as per Eq. (1) considering common terms is performed by the first stage adder

structure and the results are stored in the intermediate registers. The intermediate data obtained after first stage addition is correspondingly multiplied by the ILa filter coefficients the multiplied outputs are accumulated in the second stage adder array. The first stage addition, multiplication and second stage addition requires 3 clock cycles. To compute the first output of each filter 13 clock cycles are required (10 clocks for loading data, three clocks for addition, multiplication and addition). After computing the first output at the end of 13th clock cycle every output requires four clock cycles (1 clock for loading new data into SISO, three clocks for addition, multiplication and addition). The latency is 13 clock cycles and throughput is 4 clock cycles. The reduced order structure is advantageous as it computes four filter outputs simultaneously once the data is loaded in the SISO register and hence the throughput is one clock cycle (4 outputs every four clock cycles). The reduced order architecture requires 16 multipliers, 28 adders or subtractors, 16 intermediate registers and one SISO register for implementing first stage DTCWT filter structure or row processing structure.

Implementing the reduced order design on FPGA requires use of DSP block sets for multiplication, as FPGA comprises of LUT logic in large number than the DSP block sets, distributed arithmetic based structure is designed and is presented in next section.

3.2 Multiplexed DA architecture

The second stage or column processing comprises of 8 filters that processes the four row processed outputs $\{y_1, y_2, y_3$ and $y_4\}$ to generate level-1 DTCWT sub bands. In the first stage as the input was common to all four filters, design of reduced order filter structure was an advantage. In the second stage the data samples y_1 or y_2 or y_3 or y_4 is common to two filter modules and requires 32 total numbers of multiplier. In this work, DA Algorithm is used for design of second stage filtering to demonstrate its advantages for DTCWT implementation.

$$y_{11}(n) = \begin{pmatrix} y1'(n)\,ILa(1) + y1'(n-1)\,ILa(3) + \\ y1'(n-2)\,ILa(1) + y1'(n-3)\,ILa(7) \end{pmatrix} \quad (2a)$$

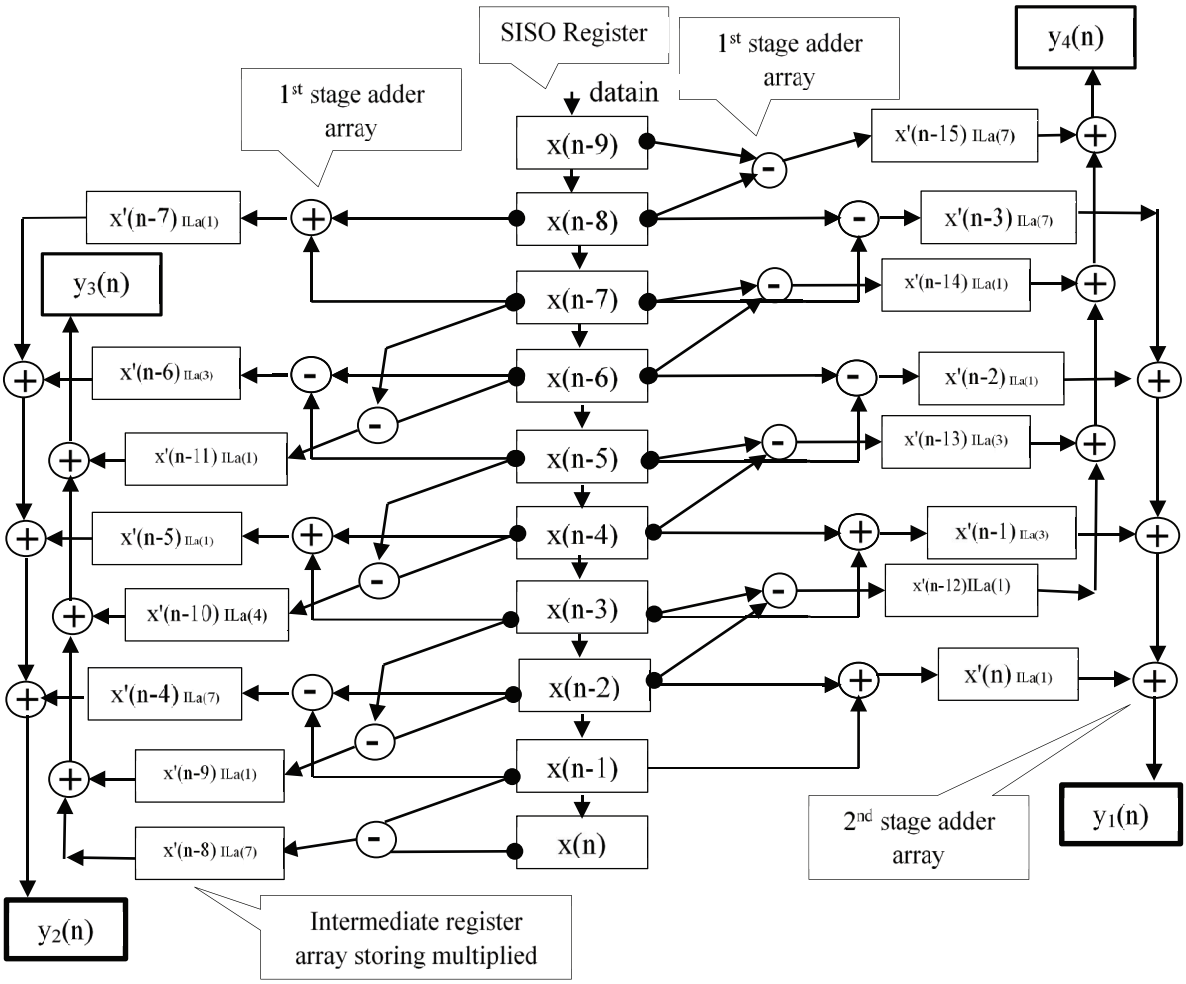

Figure 2: Reduced order DTCWT architecture

$$y_{12}(n) = \begin{pmatrix} yl'(n)\,ILa(7) + yl'(n-1)\,ILa(1) + \\ yl'(n-2)\,ILa(3) + yl'(n-3)\,ILa(1) \end{pmatrix} \quad (2b)$$

$$y_{31}(n) = \begin{pmatrix} y3'(n)ILa(7) + y3'(n-1)\,ILa(1) + \\ y3'(n-2)\,ILa(3) + y3'(n-3)ILa(1) + y3'(n-4)ILa(0) \end{pmatrix} (2c)$$

$$y_{32}(n) = \begin{pmatrix} y3'(n)ILa(0) + y3'(n-1)\,ILa(1) + \\ y3'(n-2)\,ILa(3) + y3'(n-3)ILa(1) + y3'(n-4)ILa(7) \end{pmatrix} (2d)$$

Outputs y_{11} and y_{12} are computed considering y_1 and y_{31} and y_{32} are computed considering y_3. Considering common filter coefficients the reduced expression for $y_{11,}\, y_{12,}\, y_{31}$ and y_{32} are presented in Eq. (2), the term y'(n) is obtained by adding the terms y(n) that have common filter coefficients ILa. Realizing Eq. (2) consists of two stages, the first stage computes the intermediate outputs by addition and subtraction operation and the second stage is the DA logic. Figure 3.1(a) and Figure 3.1(b) presents the two stage structure for computation of $\{y_{11,}\, y_{12}\}$ and $\{y_{31}$ and $y_{32}\}$ respectively.

In the proposed DA architecture two outputs are simultaneously computed from a single LUT that is stored with pre-computed partial products according to DA logic [12][25]. Considering Eq. 2(a) and Eq. 2(b) the order in which the ILa coefficients are multiplied with corresponding data samples y_1' are reversed. Eq. 2(b) is reorganized in accordance to Eq. 2(a) to have the ILa coefficients sequence matching expression $y_{11}(n)$.

$$y12(n) = \left(yl'(n-3)\,ILa(1) + yl'(n-2)\,ILa(3) + \right. \\ \left. + yl'(n-1)\,ILa(1) + yl'(n)\,ILa(7)\right) \quad (3)$$

Considering DA algorithm discussed in detail in [25] the expressions y_{11} (Eq. 2a) and y_{12} (Eq. 3) are expressed as in Eq. (4a) and Eq. (4b) respectively.

$$y_{12}(n) = \begin{pmatrix} \sum_{m=0}^{7} y'1,m(n)\,ILa(1)2^m + \\ \sum_{m=0}^{7} y'1,m(n-1)\,ILa(3)2^m + \\ \sum_{m=0}^{7} y'1,m(n-2)\,ILa(1)2^m + \\ \sum_{m=0}^{7} y'1,m(n-3)\,ILa(7)2^m \end{pmatrix} \quad (4a)$$

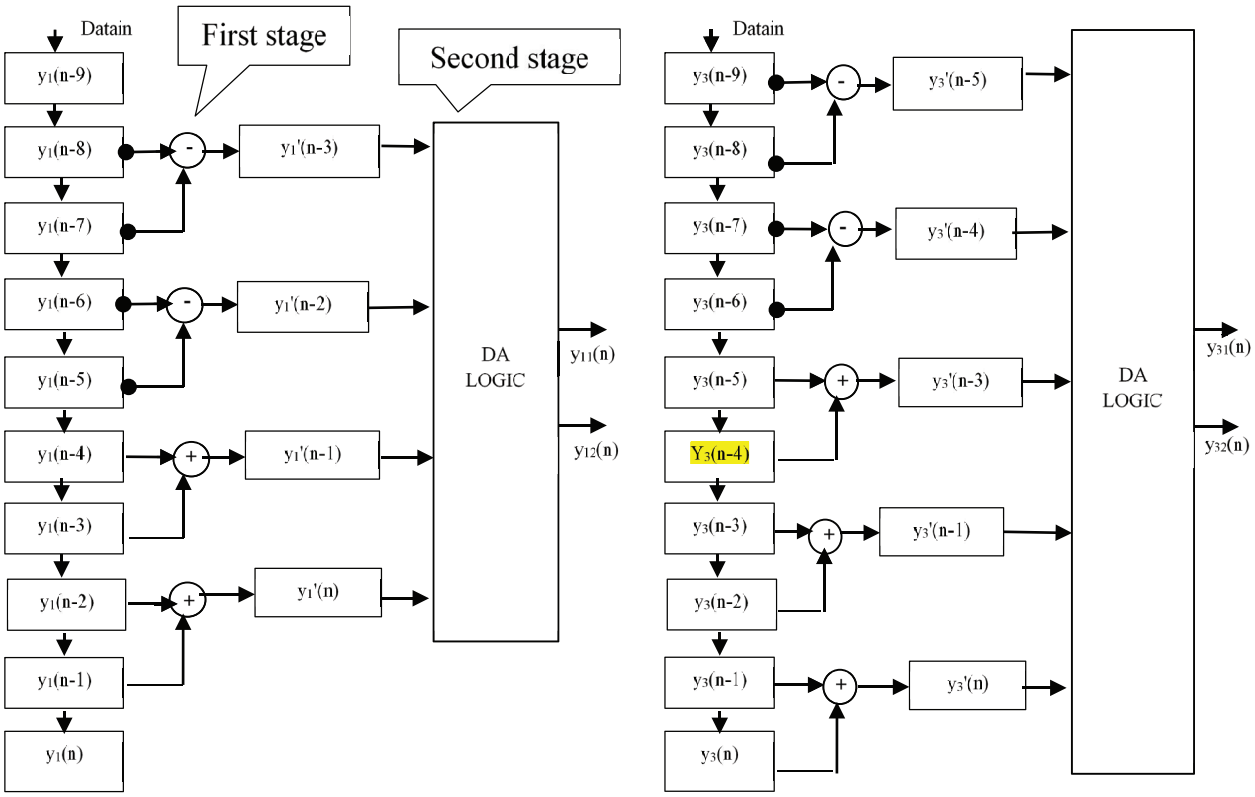

Figure 3: Second stage DTCWT processing (a) y_{11} and y_{12} structure (b) y_{13} and y_{32} structure

$$y_{12}(n) = \begin{pmatrix} \sum_{m=0}^{7} y'1,m(n-3)\,ILa(1)2^m + \\ \sum_{m=0}^{7} y'1,m(n-2)\,ILa(3)2^m + \\ \sum_{m=0}^{7} y'1,m(n-1)\,ILa(1)2^m + \\ \sum_{m=0}^{7} y'1,m(n)\,ILa(7)2^m \end{pmatrix} \quad (4b)$$

As there are four terms {ILa(1), ILa(3), ILa(7), ILa(1)} the contents of LUT for expression Eq. 4(a) is computed that comprises of sixteen terms as shown in Table 2. The address bits {A_0, A_1, A_2, A_3} are used to access the LUT contents. The inputs $y'_{n1,n2}(n)$ is the MSB and $y'_{n1,n2}(n-3)$ is the LSB for the term in Eq. (4a). For the term in Eq. 4(b) $y'_{n1,n2}(n)$ is LSB and $y'_{n1,n2}(n-3)$ is the MSB.

Table 2: LUT contents for DA logic for computing $y_{11\,and}\,y_{12}$

A_3	A_2	A_1	A_0	LUT Contents
0	0	0	0	0
0	0	0	1	ILa (7)]
0	0	1	0	ILa (1)
0	0	1	1	ILa (1) + ILa (7)
0	1	0	0	ILa (3)
0	1	0	1	ILa (3) + ILa (7)
0	1	1	0	ILa (3) + ILa (1)
0	1	1	1	ILa (3) + ILa (1) + ILa (7)
1	0	0	0	ILa (1)
1	0	0	1	ILa (1) + ILa (7)
1	0	1	0	ILa (1) + ILa (1)
1	0	1	1	ILa (1) + ILa (1) + ILa (7)
1	1	0	0	ILa (1) + ILa (3)
1	1	0	1	ILa (1) + ILa (3) + ILa (7)
1	1	1	0	ILa (1) + ILa (3) + ILa (1)
1	1	1	1	ILa (1) + ILa (3)+ ILa (1) + ILa (7)

The multiplexed DA logic that is designed in this work requires single LUT that is used to compute both y_{11} and y_{12} outputs. The contents of LUT are accessed twice in one clock during the positive edge and negative edge. During the positive state of clock the address to LUT is $\{y'_{1,7}(n-3), y'_{1,7}(n-2), y'_{1,7}(n-1), y'_{1,7}(n)\}$ and during negative state of clock the address is $\{y'_{1,7}(n), y'_{1,7}(n-1), y'_{1,7}(n-2), y'_{1,7}(n-3)\}$. Figure 4 presents the multiplexed DA architecture that comprises of input registers, multiplexer, LUT, demultiplexer, accumulator logic and output register. The input data register is of 8 bit width and there are four registers that are serially loaded with the input samples. Loading of four input registers requires 32 clock cycles. The 2:1 multiplexer has two inputs that are connected to the LSBs of four input registers. The multiplexer control signal S_1 is used to select the appropriate LSB to form the address bit for the LUT. If S_1 is '0' $\{y'_{1,7}(n-3), y'_{1,7}(n-2), y'_{1,7}(n-1), y'_{1,7}(n)\}$ form the address {A_0, A_1, A_2, A_3} to the LUT if S_1 is '0', then the address to LUT is $\{y'_{1,7}(n), y'_{1,7}(n-1), y'_{1,7}(n-2), y'_{1,7}(n-3)\}$. S_1 is connected to clock pin and s1 toggles between positive and negative levels ensuring reading of LUT contents twice in one clock cycle. The LUT contents read out are accumulated in the output section comprising of adder and Right Shift (RS) register. The demultiplexer at the output directs the LUT contents to the corresponding accumulator section. The final outputs are stored in the two output registers. Loading data samples into the input register requires 32 clock cycles, and comput-

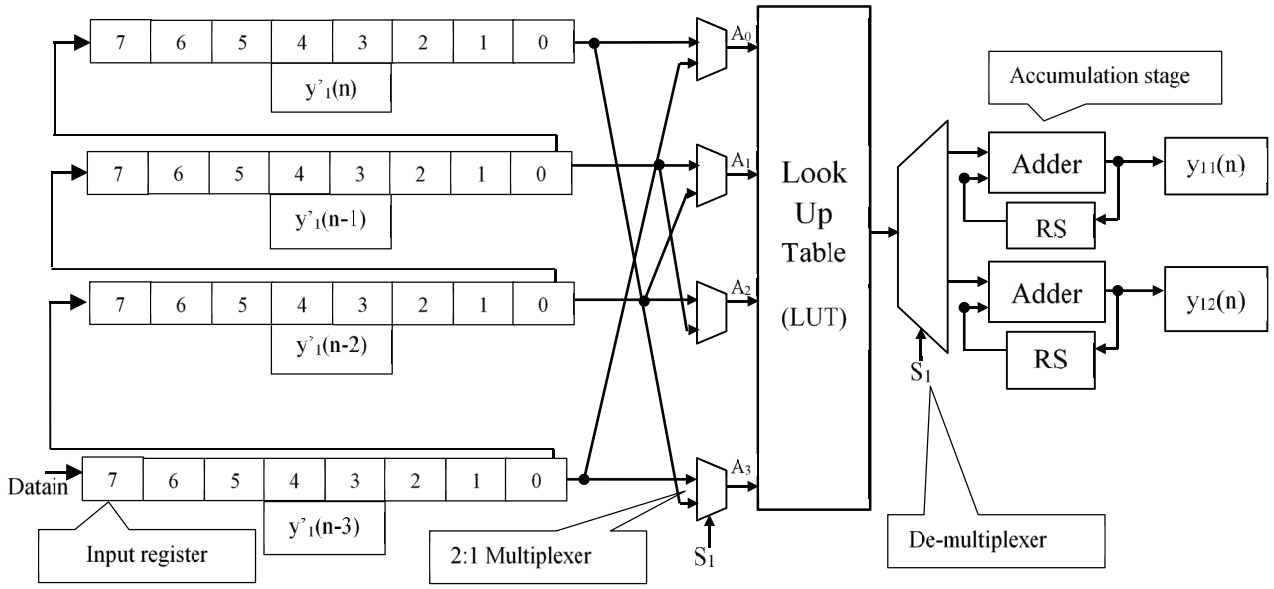

Figure 4: Multiplexed DA logic for y_{11} and y_{12} computation

ing the output samples using DA logic requires 8 clock cycles. After 40 clock cycles the first output of two filters are computed. Computing the consecutive output requires 16 clock cycles (8 clocks for new data sample loading in the input register and 8 clocks for LUT content read and accumulation). Latency for computing y_{11} and y_{12} is 40 clock cycles and throughput is 16 clock cycles for every two outputs.

In the similar way, DA structure for computation of y_{31} and y_{32} is carried out using multiplexed DA logic based on the expressions presented in Eq. (5a) and (5b) respectively.

$$y_{31}(n) = y_3'(n)IL_a(7) + y_3'(n\text{-}1)\,IL_a(1) + \\ + y_3'(n\text{-}2)\,IL_a(3) + y_3'(n\text{-}3)IL_a(1) + y_3'(n\text{-}4)IL_a(0) \quad (5a)$$

$$y_{32}(n) = y_3'(n\text{-}4)IL_a(7) + y_3'(n\text{-}3)\,IL_a(1) + \\ + y_3'(n\text{-}2)\,IL_a(3) + y_3'(n\text{-}1)IL_a(1) + y_3'(n)IL_a(0) \quad (5b)$$

The LUT size for y_{31} and y_{32} is of depth 32 as there are five input registers and five filter coefficients. The latency for computing y_{31} and y_{32} is 48 clock cycles and throughput is 16 clock cycles for every two outputs. Similar structure is designed for computing y_{21} and y_{22} samples and y_{41} and y_{42} of second stage filtering. The advantage of this designed architecture is that the for second stage structure that requires 8 filters are realized using four LUTs. The multiplexed DA logic reduces the LUT resources by 50% as compared with direct DA logic implementation. The multiplexer based DA logic is suitable for FPGA implementation as the number of DSP block sets required for DTCWT computation is reduced and a multiplierless logic is realized. In order to reduce the number of DSP blocks as well as LUT resources for DTCWT computation Zero Pad Logic (ZPL) based structure is also designed and is presented in next section.

3.3 Zero pad architecture

The scaled filter coefficients presented in Table 1 are $\{IL_a(0) = IL_a(9) = 0,\ IL_a(1) = IL_a(2) = IL_a(5) = IL_a(6) = 22,\ IL_a(3) = IL_a(4) = 178,\ IL_a(7) = IL_a(8) = 2\}$. In this design multiplierless structure is designed by using zero padding logic. The filter coefficients are represented in power of 2 as $\{ILa(1) = 22 = 16 + 4,\ IL_a(3) = 178 = 128 + 32 + 16 + 2,\ IL_a(7) = 2\}$. As the filter coefficients are represented in power of 2, multiplying the input data sample by either 2 (2^0), 4(2^2) or 2^N requires to shift left the input data by N. The first stage filter output $y_1(n)$ presented in Eq. 1(a) is rewritten as in Eq. (6), by expanding the filter coefficients in power of 2.

$$\begin{pmatrix} x'(n)[ILa1(1) + ILa2(1)] + \\ x'(n\text{-}1)[ILa1(3) + ILa2(3)] + ILa3(3) + ILa4(3)] + \\ x'(n\text{-}2)[ILa1(1) + ILa2(1)] + x'(n\text{-}3)ILa1(7) \end{pmatrix} \quad (6)$$

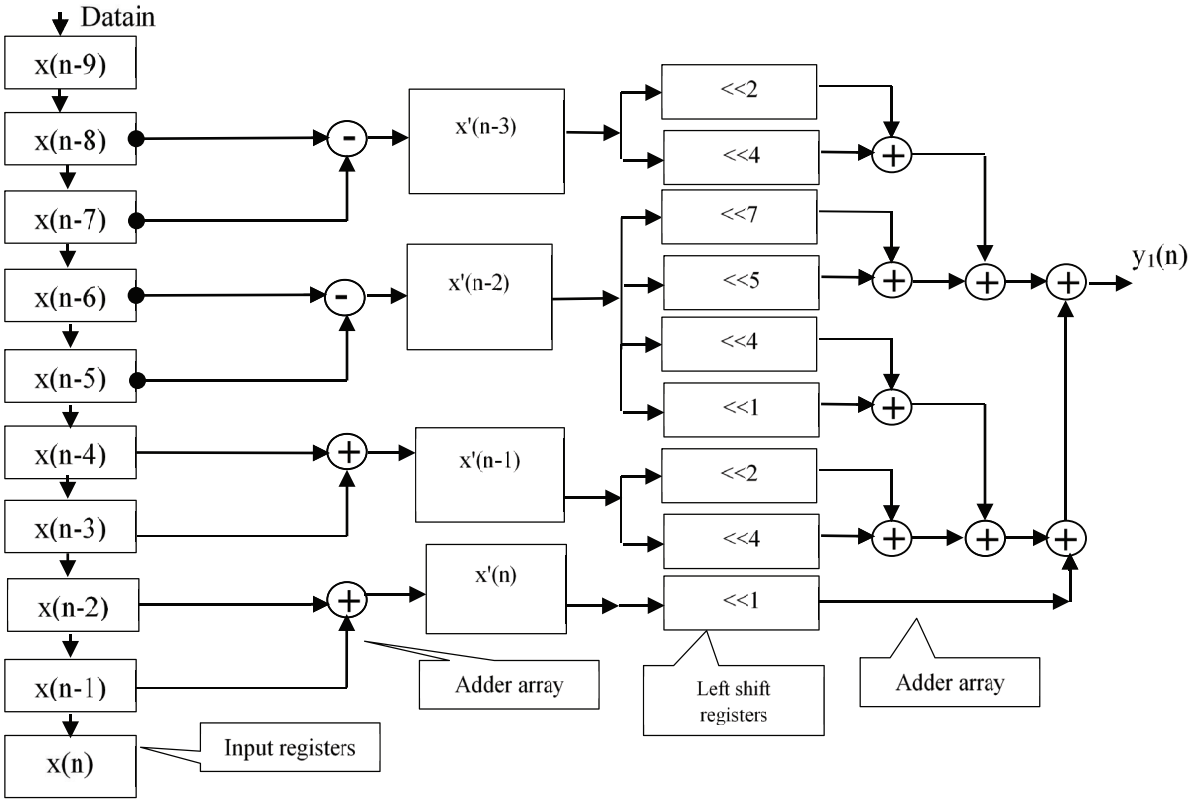

Figure 5: DTCWT filter structure based on zero pad logic

Multiplication of input data sample by 128, or 32, or 16, or 4, or 2 is equivalent of shifting x'(n) by 7, 5, 4, 2 and 1 respectively. This shift operation can also be performed by zero padding 7, 5, 4, 2 and 1 zeros at the LSB of X corresponding to multiplication by 128, or 32, or 16, or 4, or 2 respectively. The expression in Eq. (6) is represented as in Eq. (7) based on zero pad logic.

$$\begin{pmatrix} \{x'(n)ZPL(4)\} + \{x'(n)ZPL(2)\} + \{x'(n-1)ZPL(7)\} + \\ \{x'(n-1)ZPL(5)\} + \{x'(n-1)ZPL(4)\} + \{x'(n-1)ZPL(1)\} + \\ \{x'(n-2)ZPL(4)\} + \{x'(n-2)ZPL(2)\} + \{x'(n-3)ZPL(2)\} \end{pmatrix} \quad (7)$$

ZPL(4) implies shifting or zero padding 4 zeros at the LSB of data sample x'(n). Figure 5 presents the zero pad based architecture for computing y_1 term. The content of intermediate register {x'} is zero padded by 2, 4, 7, 5, 4, 1, 2, 4, 1 of zero bits at the LSBs of each of the intermediate registers. The adder array logic unit is designed to compute the final output and is designed to process data in parallel. The total time requirement from output of intermediate array register to final output is four clock cycles and throughput is 1 clock cycle for every output. Similar structure is designed for computing all 12 filters of 2D DTCWT computation. It is observed that the number of zero padding required is 9 for the architecture shown in Figure 5. Zero padding also requires memory resources on FPGA.

Figure 6 presents improved structure for zero pad logic that reduces the number of zero padding. Eq. (7) is simplified to Eq. (8) by rearranging the terms considering common factors in terms of zero pads. In the rearranged expression, addition operation of intermediate register content is carried out prior to zero padding. From the architecture design the reduced zero pad architecture requires 5 zero pads and eight adders as compared with the structure shown in Figure 5 that requires 9 zero pads and 8 adders.

$$Y_1(n) = \begin{pmatrix} \{[x'(n) + x'(n-1) + x'(n-2)]ZPL(4)\} + \\ \{[x'(n) + x'(n-2) + x'(n-3)]ZPL(2)\} + \\ \{x'(n-1)ZPL(7)\} + \\ \{x'(n-1)ZPL(5) + x'(n-1)ZPL(1)\} \end{pmatrix} \quad (8)$$

The latency In computing filter output is 3 clock cycles and throughput is one clock cycle per filter output.

In this section three different architectures for DTCWT level-1 implementation is presented. The reduced order structure optimizes the number of multipliers and adders required for row processing logic. The multiplexed DA logic reduces the number of LUTs required for computing column processing in DTCWT. The zero padding logic is a multiplierless and LUTless structure that requires adders and storage registers with logic zero contents.

3.4 Systolic array architecture

In order to improve processing speed and throughput for DTCWT computation on an N x N size image systolic array architecture that combines pipelining and parallel processing operations is designed. As every stage of DTCWT processing has four filters, the filter outputs can be generalized as in Eq. (9). Representing the inputs and filter coefficients in 2's complement number representation, subtraction operation is carried out using addition operation.

$$Y1 = Ila(0)(x0+x9) + Ila(1)(x2+x1) + \\ + Ila(3)(x3+x4) + Ila(1)(x5+x6) + Ila(7)(x7+x8) \quad (9a)$$

$$y2 = Ila(0)(x0+x9) + Ila(7)(x2+x1) + \\ +Ila(1)(x3+x4) + Ila(3)(x6+x5) + Ila(1)(x7+x8) \quad (9b)$$

$$y3 = Ila(7)(x0+x1) + Ila(1)(x3+x2) + \\ +Ila(3)(x4+x5) + Ila(1)(x7+x6) + Ila(0)(x8+x9) \quad (9c)$$

$$y4 = Ila(0)(x0+x1) + Ila(1)(x2+x3) + \\ +Ila(3)(x4+x5) + Ila(1)(x7+x6) + Ila(7)(x9+x8) \quad (9d)$$

The data path operation for systolic array structure is designed based on the data flow summarized in Table 3. The filter coefficients for computing outputs of each filter is indicated along with the data input. For computing y1 and y2 as well as y3 and y4 the data input is common, the filter coefficients corresponding to each of the data to be multiplied are indicated in the table.

Figure 7 presents the systolic array structure designed for first stage DTCWT computation based on generic expressions presented in Eq. (9). The SAA architecture consists of four processing elements represented as

Table 3: Data path operation

Clock	y_1 =	y_2 =	y_3=	y_4 =
1	$(x_0 + x_9)$ Ila(0)	$(x_2 + x_1)$ Ila(7)	$(x_0 + x_1)$ Ila(7)	$(x_0 + x_1)$ Ila(0)
2	+ $(x_2 + x_1)$ Ila(1)	+ $(x_3 + x_4)$ Ila(1)	+ $(x_3 + x_2)$ Ila(1)	+ $(x_3 + x_2)$ Ila(1)
3	+ $(x_3 + x_4)$ Ila(3)	+ $(x_6 + x_5)$ Ila(3)	+ $(x_4 + x_5)$Ila(3)	+ $(x_4 + x_5)$Ila(3)
4	+ $(x_6 + x_5)$ Ila(1)	+ $(x_7 + x_8)$ Ila(1)	+ $(x_7 + x_6)$ Ila(1)	+ $(x_7 + x_6)$ Ila(1)
5	+ $(x_7 + x_8)$ Ila(7)	+ $(x_0 + x_9)$ Ila(0)	+ $(x_8 + x_9)$ Ila(0)	+ $(x_8 + x_9)$ Ila(7)

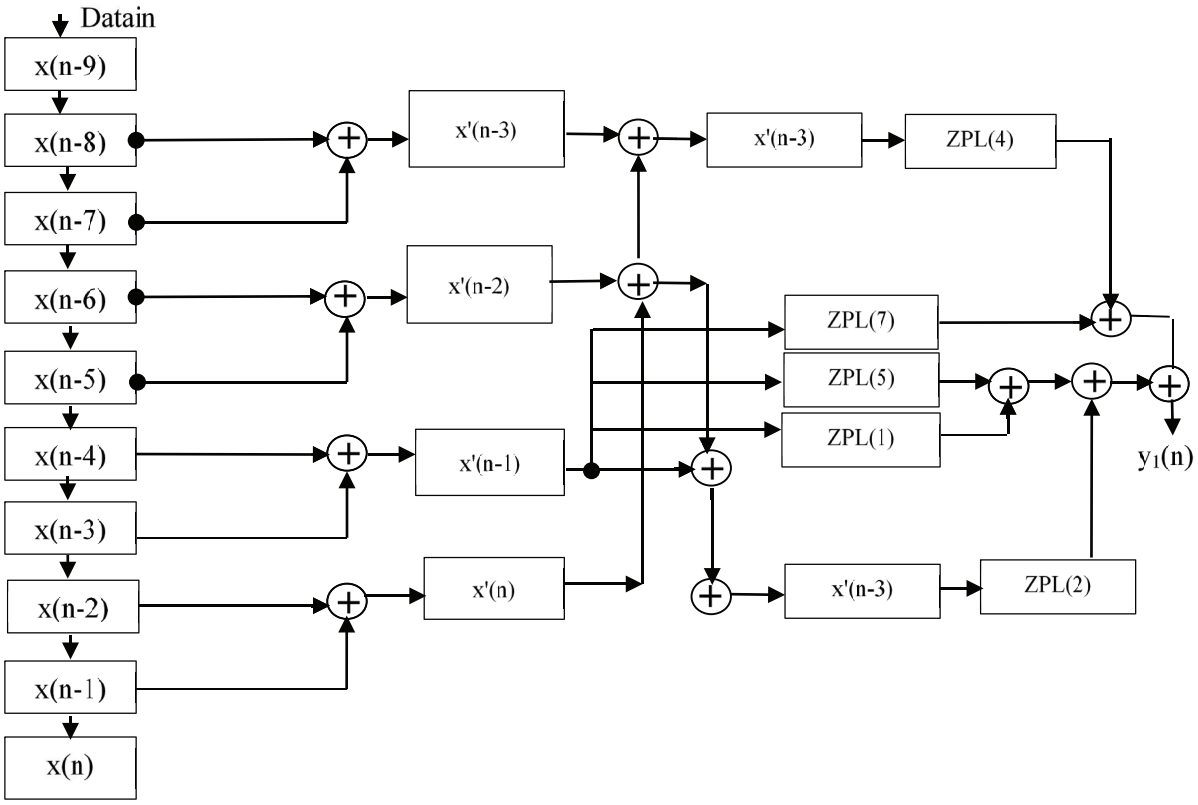

Figure 6: Reduced zero pad logic based DTCWT filter structure

{PE0, PE1, PE2 and PE3}. The data sequence into the SAA structure for filter coefficients is from left to right and for input samples is from bottom to top. From the data sequence listed in table it is found that for computation of y1 happens in PE2 with the two input vectors {c_0, c_1, c_2, c_3, c_4} and {Ila(0), Ila(1), Ila(3), Ila(1), Ila(7)} entering the PE2 from left to right and bottom to top respectively. Similarly computation is performed in PE0, PE1 elements for computing output samples y3 and y1. For computing y2 it is found that the data sequence required is { c_1, c_2, c_3, c_4, c_0} and {Ila(7), Ila(1), Ila(3), Ila(1), Ila(0)}. As the input data and filter coefficients enter PE3

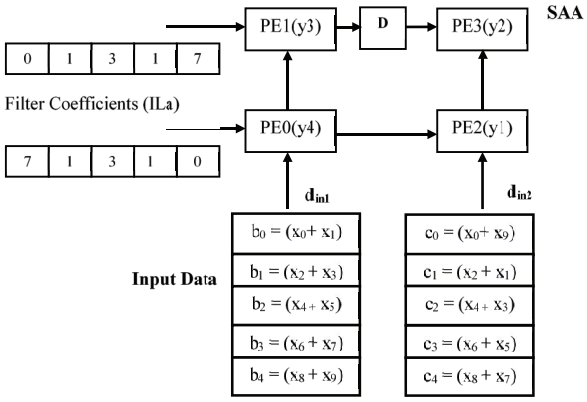

Figure 7: Systolic array structure for stage 1 DTCWT computation

there is a mismatch in data sequence, this is addressed by introducing delay element (D) in the data path between PE1 and PE3 for filter coefficients. This delay ensures that the correct data sequence enters the PE3 element to compute y_2 output.

The intermediate data computation and final output computation of systolic array structure is presented in Table 4. The PE0 generates the first output at 5th clock cycle, PE1 and PE2 generates the y_3 an y_1 outputs respectively at 6ht clock cycle and the PE3 generates y_2 output at 7th clock cycle. New Set of Data (ND2) is processed from 6th clock cycle onwards in PE0 similarly data processing is carried out in all other Pes. The latency of SAA structure is 5 clock cycles and throughput is 1 clock cycle. At every clock multiplication and addition operation is carried out which can be realized using any of the three architectures designed in previous sections.

3.5 Comparison of DTCWT architectures

Table 5 compares the performance metrics of three different architectures (A1, A2 & A3) designed in this paper in terms of arithmetic blocks, latency and throughput. From the comparisons presented, multiplexed DA and zero pad architecture are realized without multipli-

Table 4: Data computation in SAA

Clock	PE0	PE1	PE2	PE3
1	b_0.Ila(0)	0	0	0
2	b_0.Ila(0)+ b_1.Ila(1)	b_0.Ila(7)	c_0. Ila(0)	0
3	b_0.Ila(0)+b_0.Ila(1)+ b_2.Ila(3)	b_0.Ila(7)+ b_1.Ila(1)	c_0.Ila(0)+c_1. Ila(1)	0
4	b_0.Ila(0)+b_1.Ila(1)+ b_2.Ila(3)+ b_3.Ila(1)	b_0.Ila(7)+b_0.Ila(1)+ b_2.Ila(3)	c_0.Ila(0)+c_1.Ila(1)+ c_2. Ila(3)	c_1. Ila(7)
5	b_0.Ila(0)+b_1.Ila(1)+ b_2.Ila(3)+ b_3.Ila(1)+ b_4.Ila(7) = y4	b_0.Ila(7)+b_1.Ila(1)+ b_2.Ila(3)+ b_3.Ila(1)	c_0.Ila(0)+c_1.Ila(1)+ c_2.Ila(3)+ c_3.Ila(1)	c_1.Ila(7)+ c_2.Ila(1)+
6	ND2	b_0.Ila(7)+b_1.Ila(1)+ b_2.Ila(3)+b_3.Ila(1)+ b_4.Ila(0) = y3	c_0.Ila(0)+c_1.Ila(1)+ c_2.Ila(3)+ c_3.Ila(1)+ c_4.Ila(7) = y1	c_1.Ila(7)+ c_2.Ila(1)+ c_3.Ila(3)
7	ND2	ND2	ND2	c_1.Ila(7)+ c_2.Ila(1)+ c_3.Ila(3)+ c_4.Ila(1)=y2
8	ND2	ND2	ND2	0
9	ND2	ND2	ND2	ND2
10	ND2	ND2	ND2	ND2

ers and hence when implemented on FPGA will occupy less area in terms of LUTs available in Configurable Logic Blocks (CLB).

Table 5: Performance metric comparison

Metrics	A1	A2	A2
Type	Reduced order	Multiplexed DA	Zero pad
DTCWT stage	Stage 1	Stage 1	Stage 1
Adders	28	6	16
Multipliers	16	-	-
Shifters	-	-	18
Memory (SISO)	1	2	2
Intermediate Registers	16	9	16
LUTs	-	2	-
Latency	13	40	3
Throughput	4 output/ 4 Clocks	2 output/16 clocks	1 output/ 1 clocks

The number of adders in zero pad architecture is 62.5% higher than multiplexer based DA logic. The CLBs in FPGA comprises of LUTs and multiplexers hence implementing multiplexed DA on FPGA will occupy minimum resources. The latency and throughput of multiplexer based DA is 31.81% and 58% higher respectively than zero pad logic. Considering higher processing speed in terms of throughput and reduced area requirement the zero pad architecture is recommended as compared with direct implementation. For optimized area requirement and implementation of multi stage DTCWT processing multiplexed DA logic is recommended. In this work, the systolic array architecture designed in section 3.4 is implemented considering both multiplexed DA and zero pad logic for computing level-1 DTCWT.

4 FPGA Implementation

In this work, Spartan-6 FPGA development kit and Virtex-5 development kit is selected for implementation of DTCWT architecture. For validation of proposed architecture, two input images of size 256 x 256 have been chosen. Verilog code for DTCWT computation based on systolic array architecture is developed to compute level 1 DTCWT sub bands. The real and imaginary sub bands of both images are fused in the wavelet domain and the inverse transformation is performed to generate the fused image. Two images are stored in the ROM of Spartan-6 device by storing the 256 x 256 gray scale image in *.coe file and loading the file through JTAG mode while programming. The two images are read into the systolic array structure for processing and the fused image is read out through VGA controller into the PC monitor for display. Figure 8 presents the FPGA setup for architecture validations. With the proposed setup validation of DTCWT, inverse DTCWT and complexity in terms of image processing using DTCWT is evaluated. Figure 9 presents the implementation results of processing of two images based on simple fusion algorithm. The first image is a visible image and the second image is IR image that are fused in the wavelet domain by combining the DTCWT sub bands and performing inverse DTCWT operation.

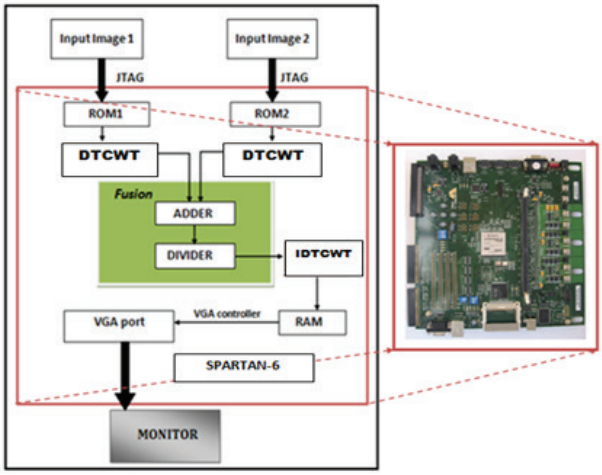

Figure 8: Evaluation of DTCWT on FPGA platform

The DTCWT architecture design is synthesized in the Xilinx tool, post place, map and route simulation also have been carried out. The design is optimized for power, area and timing. RTL synthesized block diagram of DTCWT is obtained using Xilinx ISE and the synthesis report is analyzed for estimation the performances of the proposed design in terms of area, speed and power. Table 6 compares the performances of three different architectures designed in this work. Multiplexed DA logic is found to operate at maximum frequency of 489.896 MHz and occupies LUTs less than reduced order logic. Zero pad architecture requires less than 232 LUTs and the maximum operating frequency is limited to 352.889 MHz.

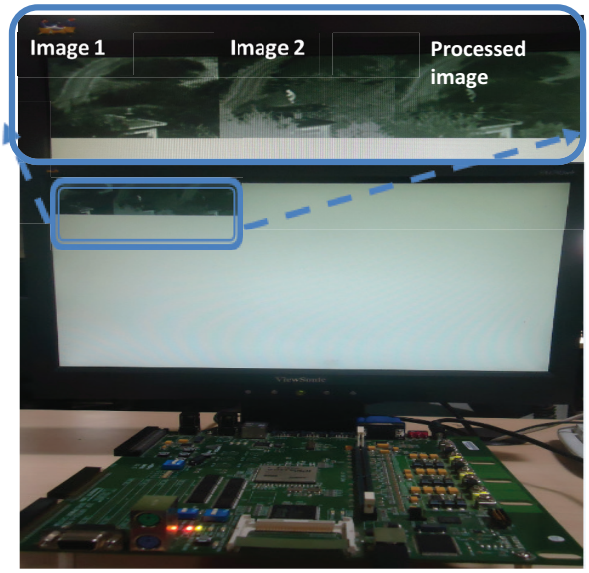

Figure 9: FPGA implementation of DTCWT based Image Fusion

Table 6: FPGA implementation of DTCWT architecture

FPGA parameters	Single filter	Two filter	First stage DTCWT
Multiplexed DA based Logic (data size 256)			
Slice Registers (Total 126800)	87	168	376
Slice LUTs (63400)	88	170	373
IOBs	24	37	68
DSP48A (240)	1	2	4
Max. Frequency (MHz)	498.262	498.262	489.896
Total power (W)	0.037	0.037	0.082
Zero pad logic (data size 256)			
Slice Registers (Total 126800)	54	106	244
Slice LUTs (63400)	52	122	232
IOBs	24	37	68
DSP48A (240)	2	4	8
Max. Frequency (MHz)	348.91	348.91	352.889
Total power (W)	0.036	0.037	0.081
Reduced order logic (data size 256)			
Slice Registers (Total 126800)	127	242	476
Slice LUTs (63400)	124	238	472
IOBs	24	37	68
DSP48A (240)	8	16	32
Max. Frequency (MHz)	332.22	332.22	325.2
Total power (W)	0.044	0.044	0.092

Power dissipation in all three architectures is limited to less than 10 mW and the results obtained are for single stage DTCWT processing. Table 7 compares the performances of SAA based architecture for computation of 256 x 256 image decomposition using DTCWT and the results are compared with direct implementation based on convolution operation.

Table 7: Comparison of hardware requirements

	SAA with Multiplexed DA	DTCWT [25]	Direct DTCWT
Number of Slice Registers	3672	4112	7482
Number of Slice LUTs	3173	4091	7224
Total power (W)	1.5702	1.71111	2.00207
Max. Frequency (MHz)	321.89	289.12	212.67

The hybrid DA architecture discussed in [25] optimizes area utilization on CLBs and DTCWT structure is implemented on Virtex-5 FPGA for four filters. The algorithm

proposed in [25] is modeled and is extended for DTCWT computation of 256 x 256 image and the results are compared with proposed SAA architecture based on multiplexed DA logic. From the results obtained, the SAA architecture consumes less than 11% power compared with existing methods for DTCWT implementation. The operating frequency of processing 256 x 256 on Virtex-5 platform is 9% faster with less than 12% of FPGA resources occupied.

5 Conclusion

In this paper, we have proposed three architectures for DTCWT computation optimizing area and timing requirement. Memory efficient architecture compatible with FPGA architecture is designed based on multiplexed DA logic that computes four filter outputs using two LUT structures. The zero pad algorithm design reduces arithmetic operations and the reduced order architecture reduces arithmetic operations. Systolic array based architecture proposed processes 256 x 256 image computing 2D DTCWT and 2D inverse DTCWT. The proposed architecture is implemented on FPGA and is demonstrated to achieve higher performance metrics in terms of speed and area on Virtex-5 and Spartan-6 FPGA. The proposed architecture for computing DTCWT sub bands operating at 321.89 MHz is suitable for high speed image processing applications such as image registration and image fusion for surveillance and remote sensing. With images acquired having high resolution, the proposed DTCWT architecture could be extended to process images of size greater than 1024 x 1024 and multiple level decomposition can be performed. Systolic array architecture design can be extended to compute multi-level DTCWT decomposition.

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Analysis and Design Consideration of a High Sensitivity Silicon Avalanche Photodiode Receiver for Low Frequency Applications

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Abstract: Silicon avalanche photodiodes (APDs) are designed predominantly for high-speed communication applications, but they can also offer interesting low-light application solutions in lower frequency bands. The design and analysis of a high sensitive silicon avalanche photodiode (APD) receiver for low-light fiber-optical sensor applications is described in this paper. The presented analysis shows relatively significant differences in the overall achievable signal-to-noise and distortion ratio (SINAD) of an optical receiver when using otherwise apparently very similar APDs. Furthermore, to maximize SINAD for the selected APD at a given target total receiver gain, an optimum setting exists between diodes' internal gain (reverse voltage) and transimpedance gain. Unfortunately, these optimum settings are usually not determinable from the typical specification parameters that are given by APD suppliers, but rather need to be determined experimentally. A circuit with low-noise transimpedance amplifier (TIA) followed by post-amplifier and low-pass filter has, thus, been designed for measurement of the fiber-optical sensor signals with optical power less than 100 pW at 20 kHz bandwidth. The overall SINAD of a receiver circuit is highly dependent on APD excess noise and, therefore, several receiver circuits with different APDs have been built and tested. The receiver responsivity 5.5 GV/W and SINAD of more than 20 dB are achieved with the optimally selected APD.

Keywords: Optoelectronics; optical receivers; avalanche photodiode (APD); fiber-optical sensors

Načrtovanje in analiza visoko občutljivega optičnega sprejemnika s silicijevo plazovno fotodiodo za nizkofrekvenčne aplikacije

Izvleček: Silicijeve polprevodniške plazovne fotodiode so pretežno načrtovane za visoke hitrosti v komunikacijah, vendar lahko nudijo tudi pri nižjih frekvencah zanimive aplikacijske rešitve s šibko svetlobo. V tem članku je opisano načrtovanje in analiza visoko občutljivega optičnega sprejemnika s silicijevo plazovno fotodiodo za optične vlakenske senzorske aplikacije s šibkimi optičnimi signali. Predstavljena analiza prikazuje relativno velike razlike v doseženem skupnem razmerju med signalom in šumom ter popačenjem (SINAD) optičnega sprejemnika pri uporabi sicer navidezno zelo podobnih plazovnih fotodiod. Poleg tega obstaja za doseganje maksimalnega razmerja SINAD pri izbrani diodi in danem ciljnem skupnem ojačenju optičnega sprejemnika optimalna nastavitev med notranjim ojačenjem (zaporno napetostjo) plazovne fotodiode in ojačenjem transimpedančnega ojačevalnika. Žal teh optimalnih nastavitev običajno ne moremo določiti iz tipičnih parametrov, ki jih podajajo proizvajalci plazovnih fotodiod, ampak jih je potrebno določiti eksperimentalno. Zatorej je bilo načrtano vezje z nizkošumnim transimpedančnim ojačevalnikom in dodatnim ojačevalnikom ter nizkoprepustnim filtrom za merjenje šibkih signalov iz optičnih vlakenskih senzorjev z optično močjo manjšo kot 100 pW pri 20 kHz pasovni širini. Skupno razmerje SINAD sprejemnika je precej odvisno od presežnega šuma plazovne fotodiode, zato je bilo sestavljenih in testiranih več sprejemniških vezij z različnimi plazovnimi fotodiodami. Z optimalno izbiro plazovne fotodiode je bila dosežena odzivnost sprejemnika 5.5 GV/W in razmerje SINAD več kot 20 dB.

Ključne besede: Optoelektronika; optični sprejemniki; plazovne fotodiode; optični vlakenski senzorji

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1 Introduction

A silicon avalanche photodiode (APD) is often used for low-light detection in the visible and near-infrared regions, due to its bias dependent internal gain and its ability to amplify the photogenerated signal by avalanche multiplication [1-4]. Internal current gain is provided in an APD because the photogenerated charge carriers are accelerated in the electrical field and produce further electron-hole pairs through impact ionization. This internal gain mechanism can improve the signal-to-noise ratio (SNR) of an optical receiver which uses an APD instead of a PIN diode [5]. However, the increased sensitivity is limited by the level of excess noise generated by the avalanche process [6]. This additional noise increases with the multiplication, and the optimum internal gain is achieved when the APD noise is approximately equal to the noise of the receiver circuit. The excess noise generated by the avalanche process also varies between different APDs and affects the noise performance of a receiver circuit significantly.

In this paper we present the design of a highly sensitive silicon avalanche photodiode (APD) receiver for low-light fiber-optical sensor applications. The receiver testing procedure, based on SINAD measure, is described and used for optimization between APD multiplication and amplifier gain. The receivers with several different APDs were compared and evaluated after the gain optimization procedure.

2 Receiver Circuit

The electrical schematic of the receiver circuit is shown in Figure 1. The optical signal is sensed with the APD connected to the input of the optical receiver in reverse-biasing. The transimpedance amplifier (TIA), which is based on a dual low-noise CMOS operational amplifier LTC6241, was used to convert the diode photocurrent into a voltage. The transimpedance gain equal to 10^7 V/A was set with a thin-film 10 MΩ feedback resistor R10. A feedback capacitor C14 provides compensation for the effects of the input capacitance, and stabilizes the circuit [5, 7-9]. The voltage signal from the TIA is then amplified with an AC-coupled post-amplifier, which removes the DC signal component and provides output voltage level adjustment. The gain of the post-amplifier depends on the selected APD, and is in a range between 37 V/V and 109 V/V. The output signal from the post-amplifier is filtered with a linear phase 10th order low-pass filter LTC1569-6 to remove high-frequency noise. The cutoff frequency of the filter is set with a single resistor R15 to 23.7 kHz. The receiver power supply voltage is regulated with a 5 V linear regulator ADM7150, which provides high power supply rejection (>90 dB from 1 kHz to 1 MHz) and ultralow output noise (<1.7 nV/√Hz).

The internal current gain of the APD depends on the applied reverse bias voltage. Typically, reverse bias voltage for silicon APDs is between 80 V and 200 V. Since the APD gain also varies with the temperature, it is necessary to control the bias voltage to keep a sta-

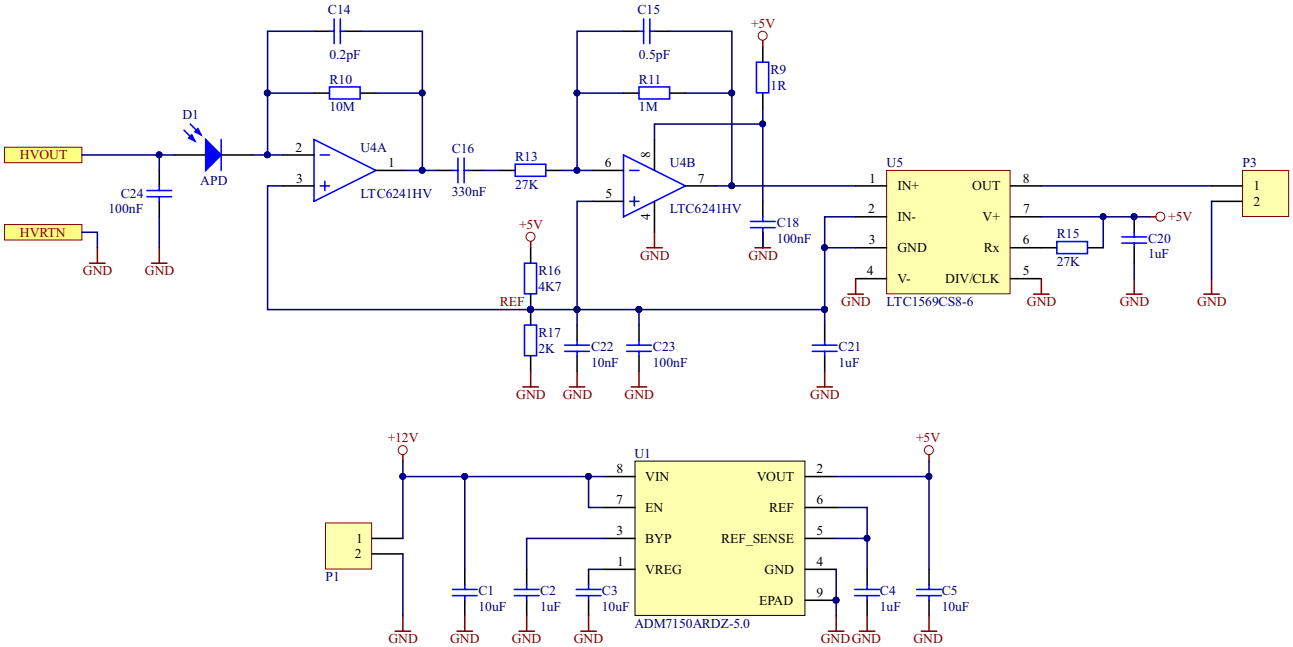

Figure 1: Electrical schematic of the receiver circuit (top) and power supply circuit (bottom).

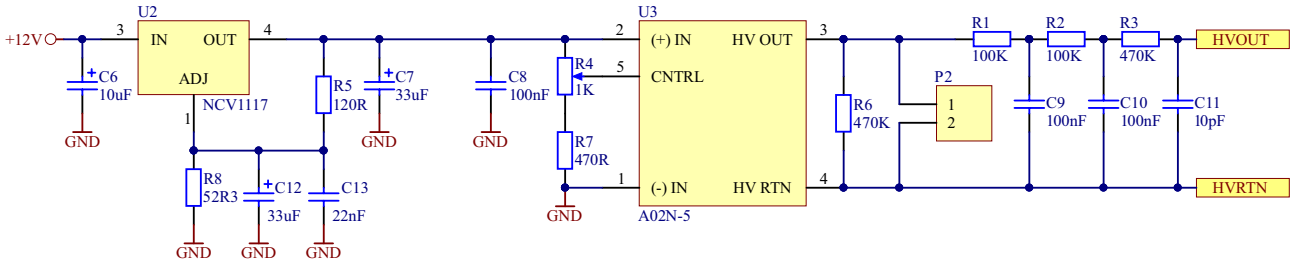

Figure 2: Reverse bias voltage circuit.

ble gain [10]. The reverse bias voltage circuit is shown in Figure 2. The reverse bias high voltage (HV) is provided with an isolated 1 W miniature proportional DC to HV DC converter module A02N-5 from XP Power. The module converts 5 V voltage from voltage regulator U2 into high output voltage with a value up to 200 V. The output voltage is set with control voltage applied to a high impedance control pin (CNTRL). This control pin could also be used in closed loop temperature control for APD gain stabilization. The module is loaded with resistor R6 and low-pass RC filer, which also reduces output ripple and limits the current through the APD.

Receiver circuits with six different silicon APDs were assembled for testing. The low-pass filter and the converter module A02N-5 for reverse bias voltage are not fitted on printed circuit boards (PCB) because they are not necessary during the diode comparison test. The reverse bias voltage is obtained from two in series connected high-voltage linear regulated laboratory power supplies PLH120-P from Aim-TTi. Typical APDs, which are commercially available on the market, were selected for this comparison. The characteristics of the tested APDs are shown in Table 1. They provide high multiplication gain and high responsivity in the wavelength range 800 nm to 950 nm. The APD3 is designed for operation at gains in the range 10 to 20, and can be operated at a fixed bias voltage without the need for temperature compensation. APD5 and APD6 were fiber coupled at manufacture, while the rest have been put into an FC diode housing and filled with black epoxy resin.

3 Results and discussion

The measurement system setup shown in Figure 3 was created for the testing of the presented receiver circuit. The fiber-optical sensor signal is simulated with a 50/125 µm multimode fiber (MM) illuminated with an 850 nm wavelength infrared emitter (IR LED) driven by a function generator. Forward current through the LED is reduced intentionally with an oversized 10 kΩ serial resistor, in order to reduce the radiant intensity of the LED and, consequently, optical power from the multimode fiber (MM). The output of the function generator is set to sinewave voltage with DC voltage offset. The optical power from the multimode fiber (MM) was measured with an Agilent 8153A lightwave multim-

Table 1: Electro-optical characteristics of tested APDs.

Parameter	Unit	APD1	APD2	APD3	APD4	APD5	APD6
Wavelength range	nm	550-1050	400-1100	600-1050	400-1100	400-1100	400-1100
Active area diameter	µm	500	500	500	230	230	230
Responsivity (850 nm, M=100)	A/W	50	62	7.6 (M=15)	50	60	59
Breakdown voltage	V	150-300	150-400	350	120-160	160-240	120-160
Capacitance	pF	2	1.5	1	1.5	1	0.6
Dark current	nA	1	1.5	20	0.05	0.5	0.05
Noise current	pA/√Hz	0.2	0.4	0.1	-	-	-
Manufacturer		Laser Components	Laser Components	Excelitas	Marktech Optoelectronics	Shengshi Optical*	Shenzhen Yigudian
Part number		SAE500NX	SAR500X	C30724PH	MTAPD-06-003	SAP-5001M510	GSAPD9-230
* Using silicon from First Sensor AD230-9 TO52S1							

eter equipped with an optical head interface module HP 81533B and optical head HP 81520A. The analog output of the optical head interface module was connected to a digital oscilloscope for measurement of the instantaneous optical power signal. The sinewave peak-to-peak value and DC offset on the function generator were changed until the same signal was obtained on the oscilloscope as from the real fiber-optical sensor. The average optical power measured with the Agilent 8153A lightwave multimeter was 320 pW, and the peak-to-peak sinewave instant power measured on the analog output was 90 pW. The sinewave frequency was set to 100 Hz during the instant power measurement, because the bandwidth limitation of the power meter's analog output.

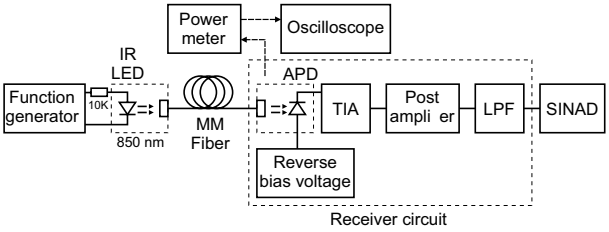

Figure 3: Block diagram of the receiver circuit test system.

The LabVIEW based spectrum analyzer with signal-to-noise and distortion ratio (SINAD) measurement was designed for the noise evaluation. The receiver output signal was digitized with the National Instruments (NI) multifunction DAQ card NI PCI-6251, which has a 16-bit analog to digital converter. The sample rate was set to 1 MS/s, and one million samples were acquired to achieve 1 Hz frequency resolution within a spectral band from DC to 500 kHz. The Spectral Measurements and Distortion Measurements (SINAD) Express VIs were used for signal analysis.

The receiver circuit bandwidth is determined with feedback resistance and capacitance, the junction capacitance of the APD and the operational amplifier gain bandwidth product [9]. The transimpedance gain for each tested receiver circuit was increased with the TIA feedback resistor until the bandwidth of 50 kHz was obtained. The maximum useful gain in APDs is limited by the excess noise generated by the stochastic nature of the avalanche multiplication process. This noise degrades the overall SINAD of the receiver circuit at high gain values, and, therefore, the reverse bias voltage was increased until the optimum multiplication gain had been achieved. After the optimum multiplication gain for a particular APD had been found, the gain of the post-amplifier was fine-tuned until reaching a 250 mV output amplitude. Figure 4 shows spectral measurement results for the receiver circuit with APD1. The top graph shows the spectrum obtained with optimal 140 V reverse bias voltage applied to the APD, but without an optical signal. This spectrum displays the uniform noise contributed mainly by the TIA circuit, and depends on the TIA gain determined with feedback resistance. The middle graph shows the spectrum after applying the simulated fiber-optical sensor signal with 10 kHz sinewave frequency, as described at beginning of the session. For the clarity of the noise floor the magnitude scale of the graph is limited and therefore the fundamental spectral component of the signal and its second harmonic are cut-off at 1.5 mV. The second harmonic is due to nonlinearity of the source and has negligible influence on the results. In addition to uniform noise, the APD noise contribution was evident, and the SINAD obtained with this multiplication gain was 14.9 dB. The further increase of multiplication gain worsened the SINAD, because the excess noise increased faster than the receiver output sinewave amplitude. This is shown in the bottom graph, where the reverse bias voltage is 175 V, the receiver output sinewave amplitude is 0.9 V, but the SINAD drops to 12.8 dB.

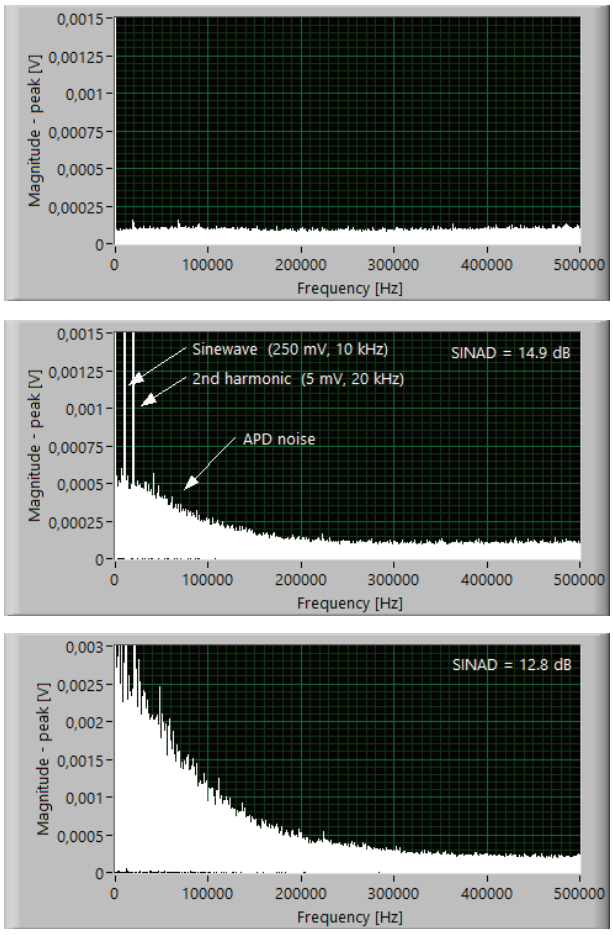

Figure 4: Spectral measurement results for the receiver circuit with APD1. Top - without optical signal, middle - with optimal gain, bottom - with high gain.

The same optimization procedure was applied to all six receiver circuits, and the comparison results are shown in Figure 5. The SINAD rise with the reverse bias voltage to some maximum value, and then began to fall, because the avalanche noise then started to increase faster than the signal. Although the tested APDs have similar electro-optical characteristics, the achieved maximum SINAD depends highly on the APD used. Also, the narrow characteristic with fast SINAD increase and decline around the maximum is inconvenient, since it requires precise reverse bias voltage control. The flattest characteristic was obtained with APD3, which is designed for operation at lower gains, but the obtained maximum SINAD was 3.5 dB lower than the best achieved result. This is because the lower multiplication gain must be compensated with higher post-amplifier's gain. The best result was obtained with APD1, which has moderate flat characteristic and the highest SINAD of 14.9 dB.

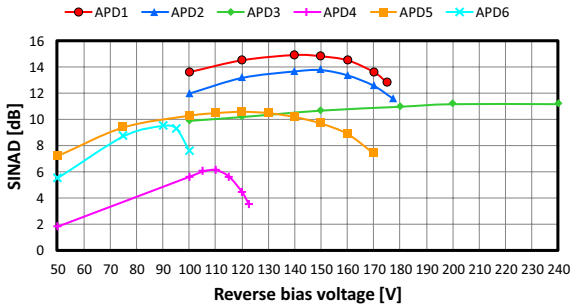

Figure 5: Comparison results for receiver circuits with different APDs.

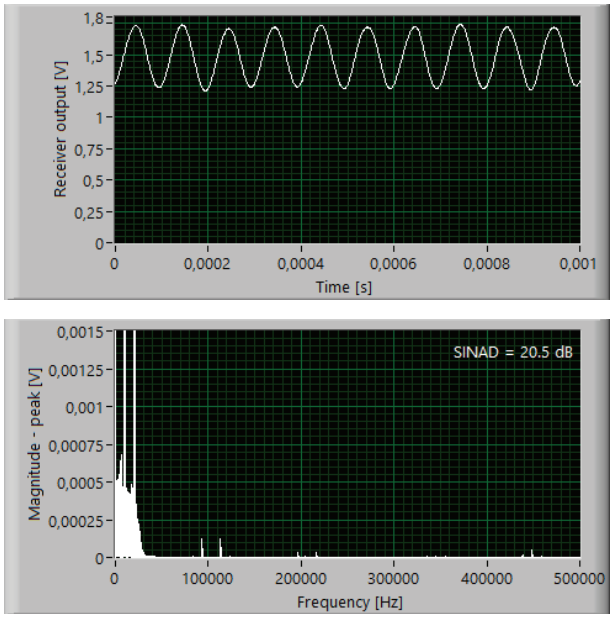

Figure 6: Measurement results for the complete receiver circuit with APD1. Top – receiver output waveform, bottom – frequency spectrum.

The complete receiver circuit with low-pass filter and the converter module A02N-5 was tested after the diode comparison test. The measurement results for APD1 are shown in Figure 6. The top waveform graph displays the receiver output sinewave with frequency 10 kHz, and 500 mV peak-to-peak value obtained from the optical sinewave signal with 90 pW peak-to-peak instant power value, while the bottom graph displays the frequency spectrum. The low-pass filter removes high-frequency noise and the SINAD of the complete receiver circuit is 20.5 dB.

4 Conclusion

The presented receiver circuit is able to amplify low-level fiber optical sensor signals with optical power less than 100 pW to voltage level, which is then suitable for analog to digital conversion and further digital signal processing. The measurement results show that relatively significant differences in SINAD were obtained with apparently very similar APDs. Furthermore, to maximize SINAD for selected APD at a given target total receiver gain, an optimum setting exists between diodes' internal gain and transimpedance gain. Unfortunately, these optimum settings are usually not determinable from the typical specification parameters that are given by APD suppliers, but rather need to be determined experimentally.

With an optimally selected APD, the receiver responsivity 5.5 GV/W was obtained at avalanche multiplication M=18 and amplifier gain 370 MV/A. Higher avalanche multiplication generates too much excess noise compared to the noise due to increased amplifier gain which is then required to get the same output voltage level. After diode selection and gain optimization, the achieved SINAD of receiver circuit with high order low-pass filter was 20.5 dB. Further improvements of SINAD for some low-frequency fiber-optical sensor applications are possible with averaging of multiple sinewave periods, or with single tone extraction.

5 Acknowledgements

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Electronically tunable current-mode multifunction filter using current-controlled current follower transconductance amplifier

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Abstract: A new electronically tunable current-mode multifunction universal filter with three inputs and one output based on current-controlled current follower transconductance amplifier is presented. The proposed filter can implement low-pass, band-pass, high-pass, band-stop and all-pass transfer functions with a single topology. For implementation of these transfer functions, no passive component-matching conditions, no inverted input signal requirements and high-output impedance are required. Also the proposed filter offers electronic control of the natural angular frequency, low active and passive sensitivities and use of grounded capacitors which is ideal for integrated circuit implementation. The proposed universal biquadratic filter has been used for implementing sixth-order filters. PSPICE simulation results confirm the presented theory.

Keywords: Universal filter; current follower transconductance amplifier (CFTA); current-controlled CFTA (CCFTA); current-mode circuit; high-order filter

Elektronsko nastavljiv multifunkcijski filter v tokovnem načinu za uporabo v tokovno krmiljenem transkonduktančnem ojačevalniku

Izvleček: Predstavljen je nov elektronsko nastavljiv multifunkcijski filter v tokovnem načinu s tremi vhodi in enim izhodom na osnovi tokovno krmiljenega transkonduktančnega ojačevalnika. Predlagan filter lahko vsebuje, nizko pasovno, pasovno, visoko pasovno, pasovno blokirno in vse-propustno prenosno funkcijo v enojni topologiji. Za implementacijo propustnih funkcij ne potrebujemo pogoje usklajenosti pasivnih komponent, invertiranih vhodnih signalov ali visokih izhodnih impedanc. Filter prav tako omogoča elektronski nadzor naravne kotne frekvence, nizko aktivno in pasivno občutljivost in ozemljene kondenzatorje, ki so idealni za implementacijo v integrirana vezja. Predlagan filter je bil uporabljen kot filter šestega red in simuliran v okolju PSPICE.

Ključne besede: univerzalni filter; tokovni transkonduktančni ojačevalnik; tokovno krmiljenje; filter visokega reda

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1 Introduction

The universal biquadratic filters are classified as second-order filters that typically implement five filtering functions with a single topology such as low-pass (LP), band-pass (BP), high-pass (HP), band-stop (BS) and all-pass (AP) transfer functions. The biquadratic filters can be used in electronic and communication systems such as phase locked loop (PLL), touch-tone telephone tone decoder, cross-over network for a three-way high-fidelity loudspeaker [1]. It is also well-known that

biquadratic filter can be used for implementing high-order filters [2]. As a result, many universal biquadratic filters are reported; see, for example [3]-[26]. Considering the input and output terminals, these filters can be classified in three categories, that are a single-input multiple-output (SIMO) filter, a multiple-output single-input (MISO) filter and a multiple-input multiple-output (MIMO) filter. When a single signal is applied at the input of a SIMO filter, filtering functions such as LP, BP, HP, BS and AP functions can be obtained at each output terminal. Thus, a SIMO filter can generate the response to several filtering functions without changing the input terminal and without requiring additional circuitry. Unfortunately, a SIMO filter normally requires several active and passive devices, if five standard filtering functions are implemented. Compared with SIMO filter, MISO and MIMO filters require fewer active and passive components, because the filtering function is selected by appropriately applying the input signals and/or selecting the output signals. However, if five filtering functions are required, additional summing and subtraction amplifiers are needed. This requirement is difficult especially for voltage-mode (VM) filters where addition and subtraction voltage amplifiers are required using several passive components. Fortunately, this problem is not present in current-mode (CM) filters, because summing and subtracting currents can be implemented in a straightforward manner. Moreover, multiple copies of an input signal can be easily implemented with multiple-output current mirrors.

Current-mode (CM) signal processing circuits received considerable attention because this technique offers several advantages compared to voltage-mode (VM) signal processing circuits, such as greater signal bandwidth, wider dynamic range and especially simpler circuitry [27], [28]. Considering the universal filters in [3-26], the circuits in [3-12] are VM filters while the circuits in [13-26] are CM filters. This paper is focused on the CM filters which are supposed to use only a single active device and grounded capacitors. Several active devices have been used to realize CM universal filters; see, for example [13-33]. The CM filters in [13-17] use second-generation current conveyor (CCIIs) as the active element. However, these structures suffer from a lack of electronic tuning capability. The CM filters with an electronic tuning capability can be realized using operational transconductance amplifiers (OTAs) [18-20] and second-generation current-controlled current conveyors (CCCIIs) [21-26], but these circuits use a large number of active elements.

Recently, a new current-mode active device with two current inputs and two kinds of current output referred to as a current differencing transconductance amplifier (CDTA), has been proposed [29]. This device is a synthesis of the well-known advantages of the current differencing buffered amplifier (CDBA) [30] and the transconductance amplifier (TA) to facilitate the implementation of current-mode analog signal processing circuits. Some current-mode universal filters using CDTAs as active elements have been reported in technical literature, see, for example [31-34]. However, these reported filters require more than one CDTA. Moreover, some configurations do not exploit the full capability of the CDTA when typically one of two input terminals of the CDTA is floated and not used [31-33]. Unfortunately, this can cause noise injection in a monolithic circuit [35].

More recently, a new active element with one current input and two kinds of current outputs, the so-called "current follower transconductance amplifier (CFTA)", has been introduced [36]. It is obtained by modifying the original CDTA. It is similar to the CDTA except for current input. The current input of CFTA is operated as a current follower. CFTA-based universal filters were already proposed [37-48]. However, the reported circuits in [37-46] require an excessive number of active components while reported circuits in [47], [48] provide only three filtering functions and some output current terminals do not exhibit high output impedance, thus additional current followers are needed for avoiding the loading problem. Active filters employing only a few active components have a lower power consumption and smaller chip area when implemented as an IC. Also the use of grounded capacitors is suitable for IC implementation [49].

Several current-mode universal filters using a single active element have been proposed in the technical literature; see, for example [50-55]. However, the reported filters suffer from one or more of the following disadvantages: (i) lack of electronic tuning capability [50-52], (ii) use of either floating capacitors or floating resistors [50-53], (iii) cannot provide five standard filtering functions [50], [53], [54], (iv) do not exploit the full capability of the active device when the y-terminal of the current conveyor is not used [55].

In this paper, a new electronically tunable current-mode universal filter employing only a modified CFTA and two grounded capacitors, is presented. The proposed circuit can implement LP, BP, HP, BS, and AP filtering functions simultaneously, by appropriately applying the input signals. For realizing these filtering functions, no passive component-matching conditions and no inverted input signal are required. Also the natural angular frequency (ω_o) can be electronically controlled. The proposed universal filter has been used to realize high-order filters as application examples. PSPICE simulation results confirm the characteristics

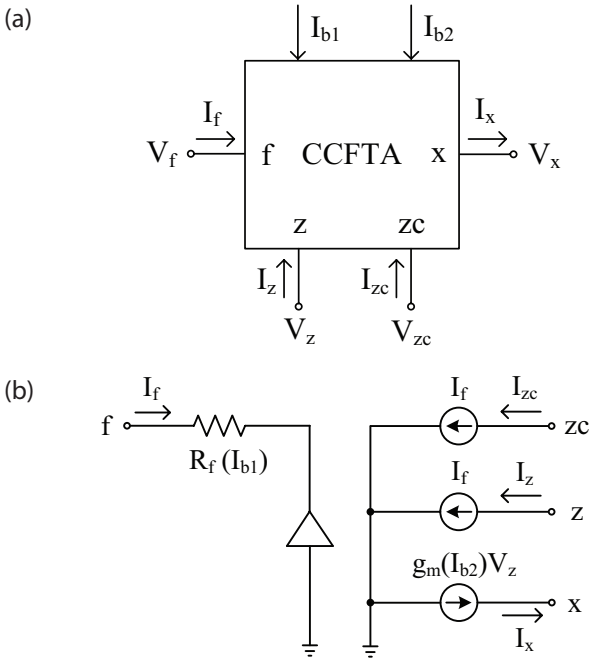

Figure 1: CCFTA: (a) circuit symbol, (b) equivalent circuit.

of the proposed circuit. The comparison between the proposed filter and some previous work is summarized in Table 1. From Table 1 it can be seen that when compared with CCII-based filters in [13-17], the proposed filter provides an electronic tuning capability whereas when compared with filter structures that enjoy an electronic tuning capability in [19-33], the proposed filter uses fewer active elements and when compared with CFTA-based filters in [37-46], the proposed filter uses fewer active and passive elements. Also when compared with the filters using a single active element in [47-55], the proposed filter provides five standard filtering functions, electronic tuning capability, the use of grounded capacitors and high-output impedance.

2 Circuit realization

The circuit symbol and the equivalent circuit of the CCFTA are shown in Fig. 1 (a) and (b). The ideal characteristic of CCFTA can be described as

$$\begin{pmatrix} I_z \\ I_{zc} \\ I_x \\ V_f \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \\ g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & R_f \end{pmatrix} \begin{pmatrix} V_z \\ V_{zc} \\ V_x \\ I_f \end{pmatrix} \quad (1)$$

where R_f and g_m are the internal resistance at the f-terminal and the transconductance gain of the CCFTA, respectively. The properties of this device are similar to those of the CFTA [36], [42] except for the f-terminal of CCFTA has finite input resistance R_f. From Fig. 1(b), the parasitic resistance R_f can be controlled by adjusting the bias current I_{b1}. This property makes it different from conventional CFTA. From Fig. 1(a), the transconductance g_m can also be controlled by adjusting the bias current I_{b2}. The current I_z can be copied to current I_{zc} at the zc-terminal. This terminal may be called the z-copy terminal [36] and it can be realized both as plus- and minus-type zc terminal. Similarly, the plus- and minus-type x-terminals can also be obtained.

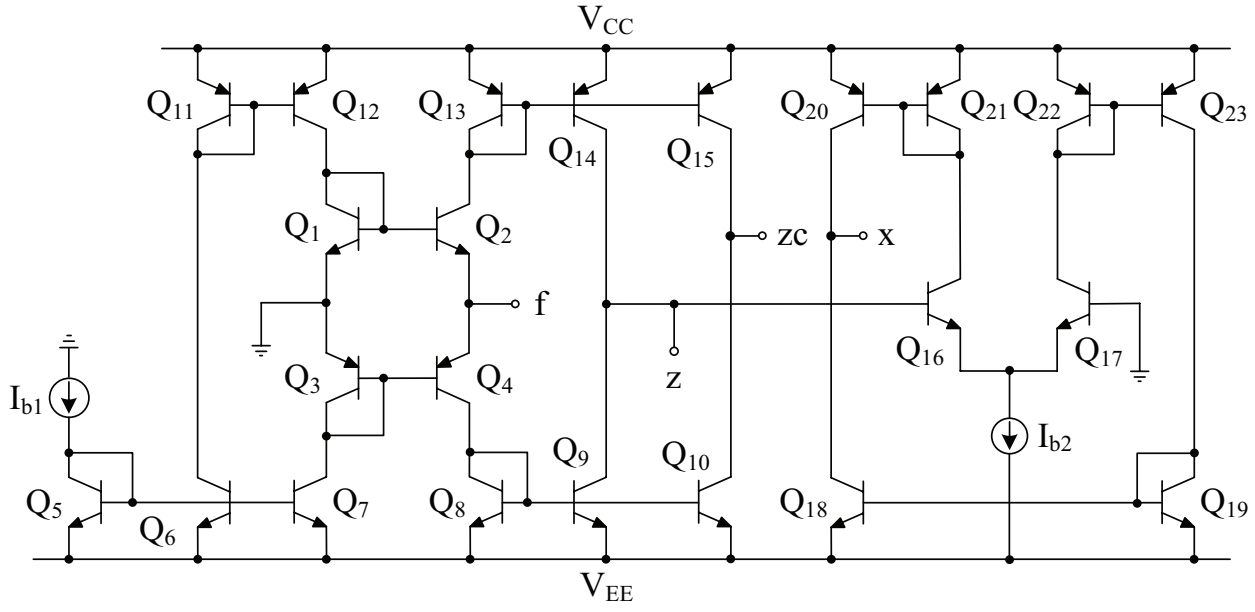

Figure 2: Bipolar implementation of the CCFTA.

Table 1: Comparison of the proposed filter with existing CM filters (*Continued*).

Circuits	Technology or active device used	Number of active elements	Number of resistors (R) & capacitors (C)	Offers five standard filters simulta-neously	Controlling ω_o without affecting Q	All-grounded passive components	High-output impedance	Operational frequency (simulated)
Proposed filters	HFA3096 (BJT)	1-CCFTA	2-C	Yes	Yes	Yes	Yes	>100 MHz
Ref. [13]	AD844N (BJT)	6-CCII	6-R & 2-C	Yes	Yes	Yes	Yes	>1 MHz
Ref. [14] (Fig.8)	LM13600, LF356 (BJT)	10-CCII	8-R & 2-C	Yes	Yes	Yes	Yes	>10 MHz
Ref. [15] (Fig.2)	AD844N (BJT)	4-CCII	2-R & 2-C	Yes	Yes	No	Yes	>1 MHz
Ref. [16] (Fig.3)	Ad844N (BJT)	1-CCII	2-R & 2-C	No	Yes	No	No	>1 MHz
Ref. [17] (Fig.3a)	0.35 µm CMOS	1-FDCCII	2-R & 2-C	Yes	Yes	Yes	Yes	>100 MHz
Ref. [18]	0.5 µm CMOS	4-OTA	2-C	Yes	Yes	No	Yes	>10 MHz
Ref. [19]	0.5 µm CMOS	2-OTA	2-C	Yes	Yes	Yes	Yes	>100 MHz
Ref. [20]	LM13600 (BJT)	2-OTA	2-C	Yes	Yes	Yes	Yes	>10 MHz
Ref. [21]	ALA400 BJT	5-CCCII	2-C	Yes	Yes	Yes	Yes	>10 MHz
Ref. [22]	ALA400 BJT	4-CCCII	2-C	Yes	Yes	Yes	Yes	>2 MHz
Ref. [24]	ALA400 BJT	4-CCCII	2-C	Yes	Yes	Yes	Yes	>10 MHz
Ref. [26]	HFA3096 (BJT)	2-CCCII	2-C	Yes	Yes	Yes	Yes	>100 MHz
Ref. [31]	0.5 µm CMOS	2-CDTA	2-C	No	Yes	Yes	No	>100 MHz
Ref. [32]	0.5 µm CMOS	2-CDTA	2-C	Yes	Yes	Yes	Yes	>10 MHz
Ref. [33]	0.35 µm CMOS	3-CDTA	1-R & 2-C	Yes	No	Yes	No	>10 MHz
Ref. [37]	ALA400 BJT	3-CFTA, 3-PCA	1-R & 2-C	No	Yes	Yes	Yes	>10 MHz
Ref. [38]	AD844N, MAX435	3-CFTA, 3-CMI	3-CFTA, 3-CMI	1-R & 2-C	Yes	Yes	Yes	>10 MHz
Ref. [39]	AD844N, MAX435	3-CFTA	1-R & 2-C	Yes	Yes	Yes	Yes	>10 MHz
Ref. [40]	AD844N, MAX435	3-CFTA	1-R & 2-C	Yes	No	Yes	No	>10 MHz
Ref. [41]	0.5 µm CMOS	3-CCFTA, 1-OTA	2-C	No	Yes	Yes	Yes	>100 MHz
Ref. [42]	0.35 µm CMOS	3-ZC-CFTA	1-R & 2-C	Yes	Yes	No	Yes	>100 MHz
Ref. [43]	AD844N, MAX435	3-CFTA	2-C	Yes	Yes	Yes	Yes	>100 MHz
Ref. [44]	AD844N, MAX435	3-CFTA	1-R & 2-C	Yes	Yes	Yes	Yes	>100 MHz
Ref. [45]	ALA400 BJT	3-CFTA	2-C	Yes	Yes	Yes	Yes	>100 MHz
Ref. [46]	0.35 µm CMOS	3-ZC-CFTA	2-C	Yes	Yes	Yes	Yes	>100 MHz
Ref. [47]	ALA400 BJT	1-CFTA	1-R & 2-C	Yes	Yes	Yes	No	>10 MHz
Ref. [48]	0.5 µm CMOS	1-CCFTA	2-C	No	Yes	Yes	No	>100 MHz
Ref. [50]	CMOS	1-CCII	3-R & 2-C	No	No	No	No	>10 MHz
Ref. [51]	AD844N (BJT)	1-CCII	2-R & 2-C	No	Yes	No	Yes	>10 MHz
Ref. [52]	AD844N (BJT)	1-CFOA	2-R & 2-C	No	Yes	No	Yes	>10 MHz
Ref. [53]	0.35 µm CMOS	1-CDTA	1-R & 2-C	No	No	No	No	>10 MHz
Ref. [54]	0.5 µm CMOS	1-CDTA	2-R & 2-C	No	No	No	No	>100 MHz
Ref. [55]	ALA400 BJT	1-CCCCTA	2-C	Yes	Yes	Yes	Yes	>3 MHz

The bipolar implementation CCFTA that was used in this work is shown in Fig. 2. It should be noted that if CMOS implementation of CCFTA is required, the bipolar junction transistors in Fig. 2 can be replaced by MOS transistors counterparts. Assuming that transistors, Q_1 to Q_4, in Fig. 2 are identical, the resistance at f-terminal (R_f) can be expressed [56] as

$$R_f = \frac{V_T}{2I_{b1}} \tag{2}$$

where V_T is the thermal voltage.

Assuming transistors Q_{16} and Q_{17} are identical, the transconductance gain (g_m) can be expressed as

$$g_m = \frac{I_{b2}}{2V_T} \tag{3}$$

The multiple-output plus/minus CCFTA can be obtained by adding additional current mirrors and cross-coupled current mirrors to obtain plus- and minus-type outputs ±zc and ±x [24]. It should be noted from Fig. 2 that there are two parasitic parameters available for implementing universal filter, meaning that passive de-

vices such as resistors are not required. Therefore the CCFTA-based universal filter can be tuned electronically. If Fig. 2 is implemented using CMOS technology, the values of R_f and g_m in (2) and (3), are proportional to the square root of the bias current. This, however, changes the electronic tunability of the CCFTA-based universal filter in the sense that the tuning range is no longer linear.

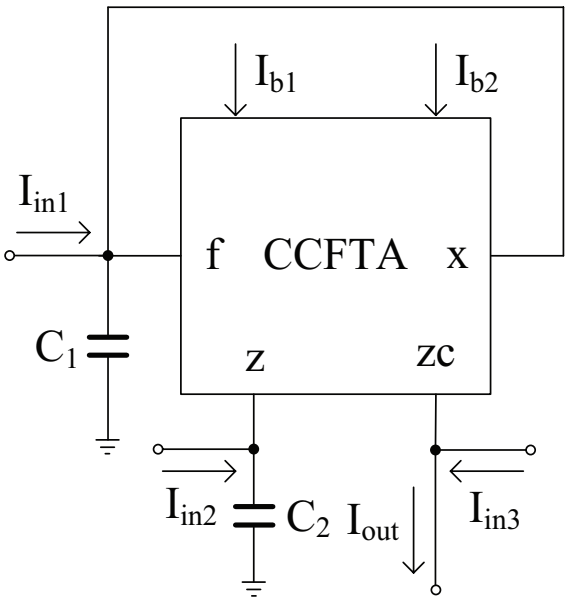

Figure 3: Proposed universal multifunction filter using CCFTA.

The proposed current-mode universal multifunction filter using minimum number of active and passive components is shown in Fig. 3. This filter is developed from a previously reported filter in [57]. The circuit consists of only one CCFTA and two grounded capacitors which is the main advantage of proposed circuit. It should be noted that the proposed circuit uses grounded capacitors which is ideal for IC implementation [49]. Assuming I_{in1}, I_{in2} and I_{in3} are input currents, using nodal analysis and CCFTA characteristic given in (1), current output I_{out} of the proposed filter can be expressed as

$$I_{out} = \frac{D(s)\ I_{in3} - g_m I_{in2} - sC_2 I_{in1}}{D(s)} \tag{4}$$

where $D(s) = s^2 R_f C_1 C_2 + sC_2 + g_m$.

From (4), the LP, BP, HP, BS and AP filters can be obtained as follows:

- The LP response can be obtained if $I_{in2}=I_{in}$ and $I_{in1}=I_{in3}=0$.
- The BP response can be obtained if $I_{in1}=I_{in}$ and $I_{in2}=I_{in3}=0$.
- The HP response can be obtained if $I_{in1}=I_{in2}=I_{in3}=I_{in}$.
- The BS response can be obtained if $I_{in1}=I_{in3}=I_{in}$ and $I_{in2}=0$.
- The AP response can be obtained if $2I_{in1}=I_{in3}=I_{in}$ and $I_{in2}=0$.

Therefore, the proposed filter in Fig. 3 can implement five standard filtering functions with a single topology. It should be noted that the realization requires no passive-matching condition and no inverted input signal. For obtaining HP, BS and AP responses, multiple- and/or double-input signals are required, but which can be easily obtained with a multiple-output current follower circuit. However, compared with LP and BP responses, HP, BS and AP responses may suffer from the input current mismatch because two identical input signals are required. This mismatch can disturb the operation of some responses, especially for obtaining the AP response when the condition of $2I_{in1} = I_{in3} = I_{in}$ is needed. This problem can be minimized by carefully designing the current follower. Also it should be noted that the current gains of the LP, HP and BP responses are equal to unity. If a filtering function with a current gain is required, additional active elements such as current amplifiers [58] are be needed. The use of current amplifier at the input avoids the problem of input impedance dependency on the frequency.

The peak frequency ω_o and quality of BP filter $Q = \omega_o/BW$ is usually related, where BW is the bandwidth. It should be noted that the relation of Q and BW is inverse, thus the higher Q, the narrower BW of BP filter. Meanwhile, the peak frequency ω_o for the LP and HP filters will also increase with increasing the value of Q. The parameters ω_o and Q are calculated, respectively, as

$$\omega_o = \sqrt{\frac{g_m}{C_1 C_2 R_f}} \tag{5}$$

$$Q = \sqrt{R_f g_m \left(\frac{C_1}{C_2}\right)} \tag{6}$$

Using (2) and (3), the parameters ω_o and Q in (5) and (6) can be rewritten as

$$\omega_o = \frac{1}{V_T}\sqrt{\frac{I_{b1} I_{b2}}{C_1 C_2}} \tag{7}$$

$$Q = \frac{1}{2}\sqrt{\frac{I_{b2}}{I_{b1}}\left(\frac{C_1}{C_2}\right)} \tag{8}$$

Letting $I_{b1} = I_{b2} = I_b$, (7) and (8) simplify to

$$\omega_o = \frac{I_b}{V_T}\sqrt{\frac{1}{C_1 C_2}} \tag{9}$$

$$Q = \frac{1}{2}\sqrt{\frac{C_1}{C_2}} \tag{10}$$

From (9) and (10), the parameter ω_o can be tuned by adjusting the value of I_b whereas the parameter Q can be given by adjusting the ratio of C_1/C_2. Therefore, the proposed filter can be controlled orthogonally for parameters ω_o and Q, but it cannot be controlled independently. It should be noted from (9) that if the bipolar implementation of CCFTA is used, parameter ω_o can be controlled linearity. For IC implementation, adjusting the value of capacitor for obtaining desired high Q-value is difficult, but it can be resolved using a capacitor bank formed by parallelly connected capacitors with switches. The value of the capacitor can then be varied by setting the switches.

3 Non-ideal analysis

In this section, the effects of CCFTA non idealities on the proposed filter performances have been analyzed. Taking into account the non-idealities of CCFTA, the CCFTA non-idealities can be obtained from

$$\begin{pmatrix} I_z' \\ I_{zc}' \\ I_x' \\ V_f' \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & \beta_z \\ 0 & 0 & 0 & \beta_{zc} \\ g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & R_f \end{pmatrix} \begin{pmatrix} V_z \\ V_{zc} \\ V_x \\ I_f \end{pmatrix} \tag{11}$$

where β_z and β_{zc} are respectively the non-ideal current transfer gains between f–z and f–zc terminals of the CCFTA.

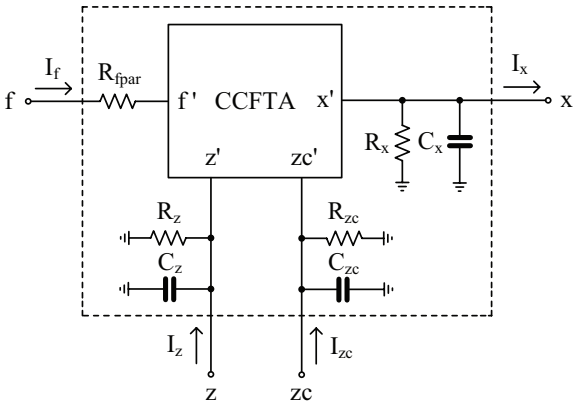

Figure 4: CCFTA with its parasitic components.

The non-ideal CCFTA symbol including various parasitic elements is shown in Fig. 4. The f-terminal exhibits parasitic serial resistance R_{fpar}, the z-terminal exhibits high-value parasitic resistances R_z in parallel with low-value parasitic capacitance C_z, the z_c-terminal exhibits high-value parasitic resistance R_{zc} in parallel with low-value parasitic capacitance C_{zc} and the x-terminal exhibits high-value parasitic resistance R_x in parallel with low-value parasitic capacitance C_x.

The non-ideality of transconductance gain g_{mn} of CCFTA can be expressed as

$$g_{mn} = \frac{g_m \omega_g}{s + \omega_g} \tag{12}$$

where ω_g denotes the first-order pole of the transconductance amplifier. In the frequency range of our interest, g_{mn} is modified to [59]

$$g_{mn} \cong g_m (1 - \mu s) \tag{13}$$

where $\mu = 1/\omega_g$.

Equations (11), (13) now result in Fig. 4, the current I_{out} of Fig. 3 can be given by

$$I_{out} = \frac{D(s)\, I_{in3} - \beta_z R_x g_{mn} I_{in2} - \beta_{zc} R_x \left(sC_2' R_z + 1\right) I_{in1}}{D(s)} \tag{14}$$

$$\begin{aligned} D(s) &= \left(s^2 C_1' C_2' R_x R_z + sC_1' R_x + sC_2' R_z + 1\right) R_f + \\ &\quad + \left(sC_2' R_z + 1\right) R_x + g_{mn} R_x R_z \\ &= s^2 C_1' C_2' R_f R_x R_z + sC_1' R_f R_x + sC_2' R_f R_z + \\ &\quad + R_f + sC_2' R_z R_x + R_x + g_{mn} R_x R_z \\ &= s^2 \left(C_1' C_2' R_f R_x R_z\right) + s\left(C_1' R_f R_x + C_2' R_f R_z + C_2' R_z R_x\right) + \\ &\quad + \left(g_{mn} R_x R_z + R_f + R_x\right) \end{aligned} \tag{15}$$

Letting $R_f << R_x$ and $R_f << R_z$, (15) becomes

$$\left.\begin{aligned} D(s) &= s^2 + s\left(\frac{1}{C_2' R_z} + \frac{1}{C_1' R_x} + \frac{1}{C_1' R_f}\right) + \frac{g_{mn}}{C_1' C_2' R_f} \\ &= s^2 + s\frac{1}{C_1' R_f} + \frac{g_{mn}}{C_1' C_2' R_f} \end{aligned}\right\} \tag{16}$$

where $C_1' = C_1 \| C_x$ and $C_2' = C_2 \| C_z$.

From (16) we can see that CCFTA non-idealities affect the circuit characteristics which depart from ideal values. To prevent significant errors, the value of the capacitors C_1 and C_2 should be selected to meet the con-

ditions C_1 >> C_x and C_2 >> C_z. The non-ideal values of parameters ω_o and Q can be expressed as

$$\omega_o = \sqrt{\frac{g_{mn}}{C_1' C_2' R_f}} \tag{17}$$

$$Q = \sqrt{R_f g_{mn} \left(\frac{C_1'}{C_2} \right)} \tag{18}$$

It should be noted from (17) and (18) that the parameters ω_o and Q are slightly changed by the non-idealities of the CCFTA. However, these effects can be compensated by adjusting the g_m-value. The active and passive sensitivities of the filter parameters are

$$S_{g_{mn}}^{\omega_o} = -S_{C_1}^{\omega_o} = -S_{C_2'}^{\omega_o} = -S_{R_f}^{\omega_o} = 0.5 \tag{19}$$

$$S_{R_f}^{Q} = S_{g_{mn}}^{Q} = S_{R_z}^{Q} = S_{C_1'}^{Q} = -S_{C_2'}^{Q} = 0.5 \tag{20}$$

From (19)-(20) we can see that the incremental sensitivities of the active and passive parameters do not exceed 1 in magnitude. Hence, the proposed filter offers low active and passive sensitivities.

4 Application to sixth-order filters

It is well-known that biquadratic filters can be used to realize high-order filters [2]. To confirm the applicability of the proposed universal biquadratic filter, high-order filters using the proposed biquadratic filter are designed. The structures of high-order filters such as sixth-order Butterworth LP, HP and BP filters have been designed. Sixth-order Butterworth LP filter can be designed by cascading tree second-order LP filters. In case of second-order HP filter, additional multiple-input current follower (CF) is required. Fig. 5(a) shows the block diagram of a second-order HP filter. The bipolar implementation of multiple-output CF is shown in Fig. 5(b). Sixth-order Butterworth BP filter can be obtained by cascading a sixth-order Butterworth HP filter and a sixth-order Butterworth LP filter. The block diagram is depicted in Fig. 6. To obtain a sixth-order Butterworth LP and HP characteristics, the filters have been designed using Tables 2 and 3. From Table 2, HP filter is designed for the cut-off frequency of 1 MHz while the LP filter is designed for the cut-off frequency of 3 MHz. Using the bias currents and capacitor-values as shown in Tables 2 and 3, sixth-order Butterworth BP filter can be obtained with the bandwidth of 2 MHz.

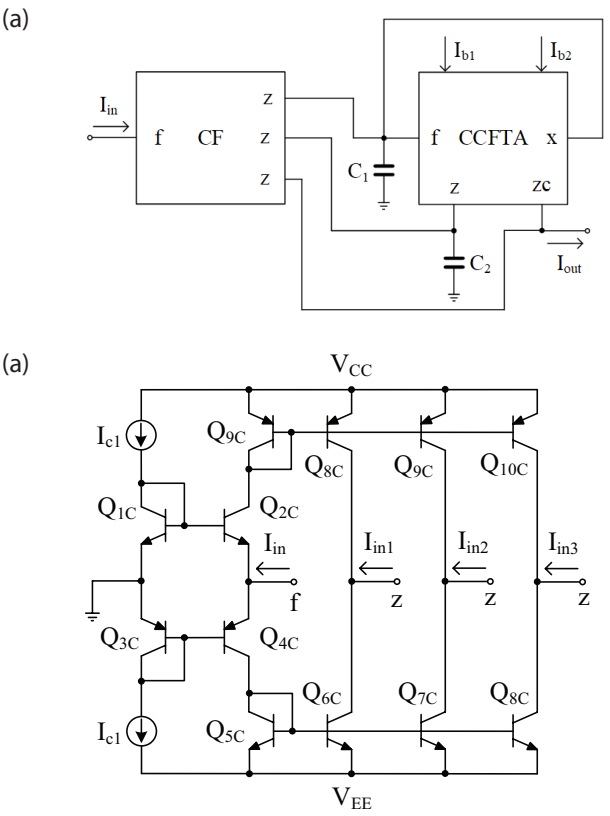

Figure 5: (a) second-order high-pass filter, (b) multiple-output current follower.

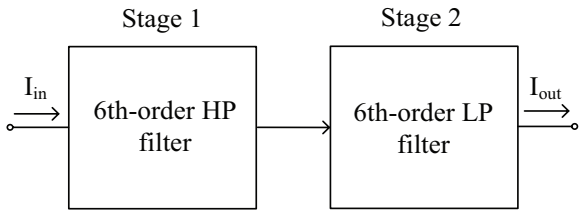

Figure 6: Sixth-order band-pass Butterworth filter.

Table 2: Parameters for sixth-order Butterworth LP filter.

Second-order LP filter	Value (f_o = 3 MHz)
Stage 1 (FSF = 1.000, Q = 0.5177)	$Ib_1 = Ib_2$ = 50.7 µA, C_1 = 107 pF, C_2 = 100 pF
Stage 2 (FSF = 1.000, Q = 0.7071)	$Ib_1 = Ib_2$ = 69.3 µA, C_1 = 200 pF, C_2 = 100 pF
Stage 3 (FSF = 1.000, Q = 1.9320)	$Ib_1 = Ib_2$ = 94.68 µA, C_1 = 746.5 pF, C_2 = 50 pF

Table 3: Parameters for sixth-order Butterworth HP filter.

Second-order HP filter	Value (f_o = 1 MHz)
Stage 1 (FSF = 1.000, Q = 0.5177)	$Ib_1 = Ib_2$ = 33.79 µA, C_1 = 214 pF, C_2 = 200 pF
Stage 2 (FSF = 1.000, Q = 0.7071)	$Ib_1 = Ib_2$ = 46.2 µA, C_1 = 400 pF, C_2 = 200 pF
Stage 3 (FSF = 1.000, Q = 1.9320)	$Ib_1 = Ib_2$ = 126.2 µA, C_1 = 2.98 nF, C_2 = 200 pF

5 Simulation results

The proposed filters are verified with PSPICE simulations. The CCFTA in Fig. 2 was implemented with bipolar transistor array HFA3096 [60]. The supply voltages were V_{CC}= – V_{EE} = 3 V. Simulated performance of CCFTA is given in Table 4.

Fig. 7 depicts simulated frequency responses of LP, BP, HP and BS filters with $I_{b1} = I_{b2}$ = 90 µA, C_1 = 3000 pF and C_2 = 100 pF, resulting in a natural angular frequency $f_o \cong$ 1 MHz and Q ≅ 2.73. Fig. 8 shows simulated frequency responses of the magnitude and phase characteristics of the AP filter at $f_o \cong$ 1 MHz. It is clear from Figs. 7 and 8 that the proposed filter performs five standard filtering functions such as LP, BP, HP BS and AP filters with a single topology. Fig. 9 shows the simulated frequency response of a BP filter when the bias currents I_b (i.e., $I_b = I_{b1} = I_{b2}$) were simultaneously adjusted to 20, 50, 100 and 200 µA, respectively, while keeping C_1 = 3000 pF and C_2 = 100 pF for a constant Q ≅ 2.73. This simulation result confirms (9).

Table 4: Simulated parameters of CCFTA.

Parameters	Value
Technology	Bipolar
Supply voltage	±3 V
R_f (I_{b1} = 1-250 µA)	12k to 52 [Ω]
g_m (I_{b2} = 1-250 µA)	21µ to 51m [A/V]
Current gain (I_z/I_f)	0.991
Current gain (I_{zc}/I_f)	0.991
-3dB bandwidth: I_z/I_f I_{zc}/I_f I_x/I_f ($Ib_1 = Ib_2$ = 100 µA, R_z = 495 Ω)	 191 MHz 191 MHz 66 MHz
R_z//C_z @ I_{b1} = 100 µA R_{zc}//C_{zc} @ I_{b1} = 100 µA R_f//L_f @ I_{b1} = 100 µA R_x//C_x @ I_{b2} = 100 µA	63 kΩ // 0.792 pF 184 kΩ // 0.304 pF 128 Ω // 0.127 nH 363 kΩ // 0.208 pF
Static power dissipation @$I_{b1} = I_{b2}$ = 1 µA @$I_{b1} = I_{b2}$ = 250 µA	 43.5 µW 108 mW

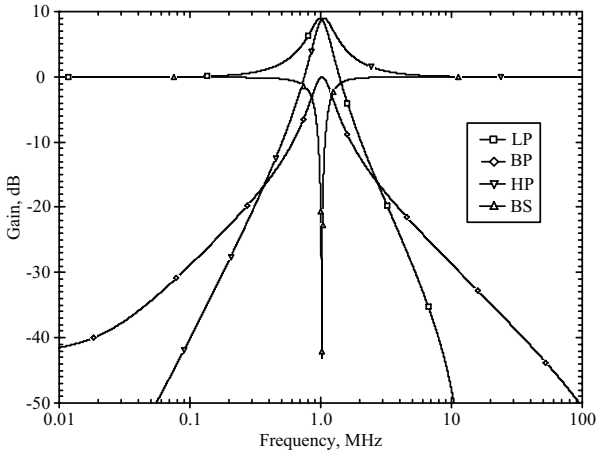

Figure 7: Simulated frequency responses of LP, BP, HP and BS filters.

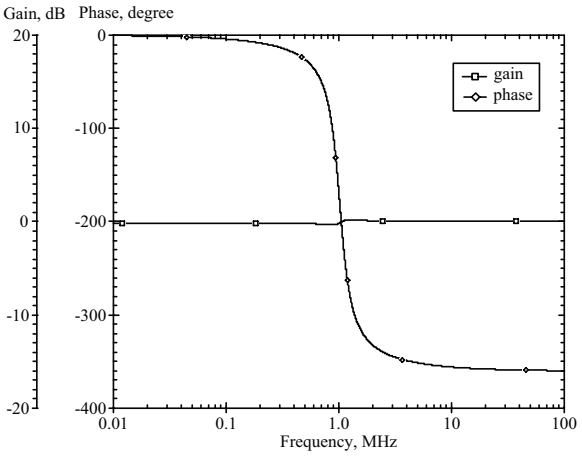

Figure 8: Simulated magnitude and phase response of an AP filter.

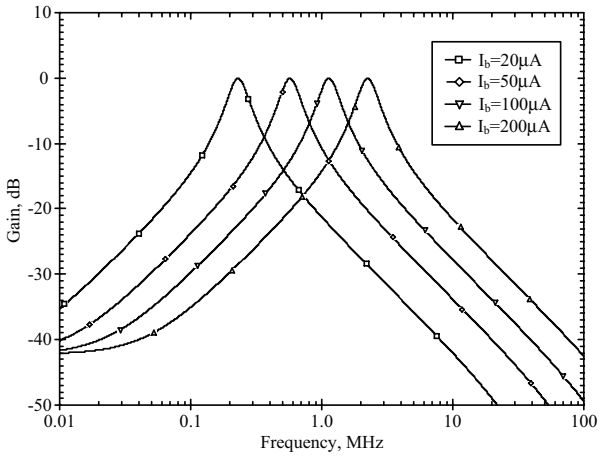

Figure 9: Frequency responses of a BP filter when I_b is varied.

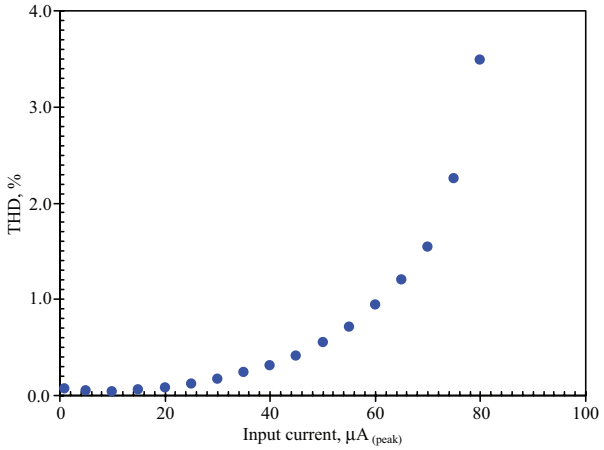

Figure 10: Dependence of the output harmonic distortion of LP filter on the input current amplitude for a 100 kHz input signal.

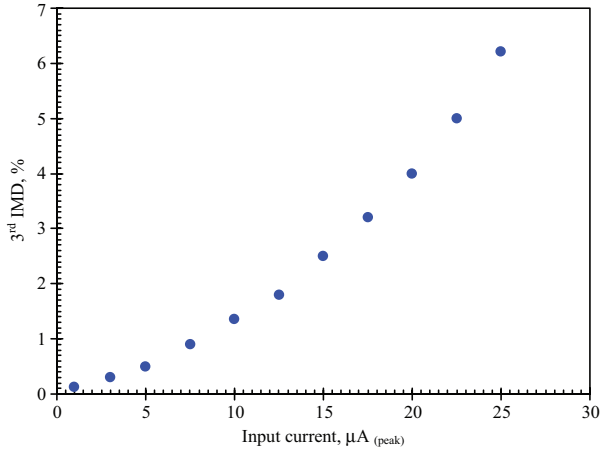

Figure 11: Dependence of the 3rd IMD of BP filter on input current amplitudes.

In order to test the linearity of the proposed filter, two methods were used; single-tone and two-tone tests. A single-tone test was performed by applying a sinusoidal signal of f_o = 100 kHz at the input of a LP filter. The dependence of the output harmonic distortion on the input amplitude is shown in Fig. 10. From this result, the THD was about 1.2 % when the input signal was 65 µA (peak) and it increases to 3.49 % when input signal increases to 80 µA (peak). A two-tone test was performed on the BP filter by applying two closely spaced tones with equal input signal amplitudes simultaneously at the input of BP filter. Fig. 11 shows the dependence of the 3rd IMD (intermodulation distortion) of BP filter on the input signals amplitudes. The two closely space tones with f_1 = 0.8 MHz and f_2 = 1.2 MHz had the same amplitude. It shows that the 3rd IMD is 6.2 % for the input signals amplitude of 25 **µA** (peak). The proposed filter was investigated using a Monte-Carlo analysis. The simulation test was the fluctuation of f_o changes caused by the deviation of the capacitors. In this test, the BP filter was simulated for 5 % tolerances of capacitors C_1 and C_2 at f_o = 1 MHz, Q ≅ 2.73 and 200 Gaussian distribution runs. Fig. 12 shows the derived histogram of f_o. The standard deviation (σ) of f_o was 31.96 kHz and the minimal and maximal values of f_o were 0.928 MHz and 1.1 MHz, respectively.

From (9) we can see that ω_o depends on V_T which in turn depends on the absolute temperature. Thus temperature stability of the proposed filter's ω_o of the proposed filter on parameter ω_o was investigated by varying temperature from 0° to 75°. The simulated frequency responses of the BP filter corresponding to different temperatures are depicted in Fig. 13.

When temperature varied between 0 and 75°, the corresponding f_o varied between 1.1 MHz and 0.879 MHz. This effect is expressed by (7). This problem can be solved by using a bias current source with the current proportional to the absolute temperature [61].

Three sixth-order Butterworth filters were also tested using parameters given in Tables 2 and 3. Simulated frequency responses of sixth-order Butterworth LP and HP filters are depicted in Figs. 14 and 15, respectively. The cut-off frequencies of 3 MHz and 1 MHz were obtained. The sixth-order Butterworth BP filter was simulated and the result is depicted in Fig. 16. The bandwidth (BW) of 2 MHz was expressed. The power consumptions for sixth-order Butterworth LP, HP and BP filters were 9.05 mW, 18.5 mW and 82.4 mW, respectively.

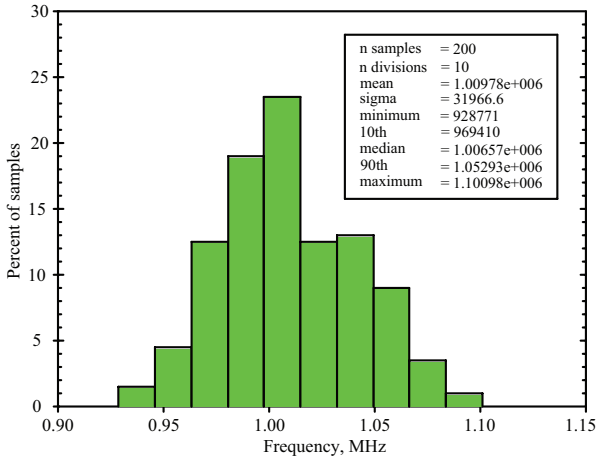

Figure 12: Histogram of Monte-Carlo analysis for BP filter with a 5% variation of capacitors C_1 and C_2.

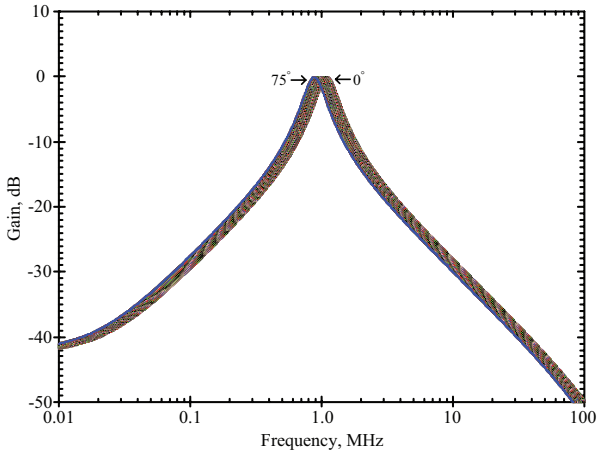

Figure 13: Simulated frequency responses of the BP filter for different temperatures.

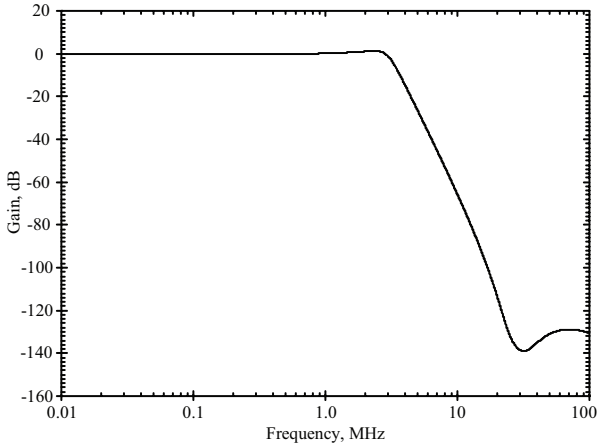

Figure 14: Simulated magnitude response of the sixth-order Butterworth LP filter.

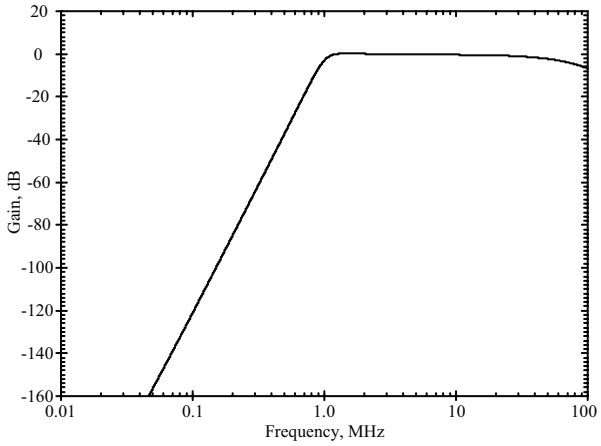

Figure 15: Simulated magnitude response of the sixth-order Butterworth HP filter.

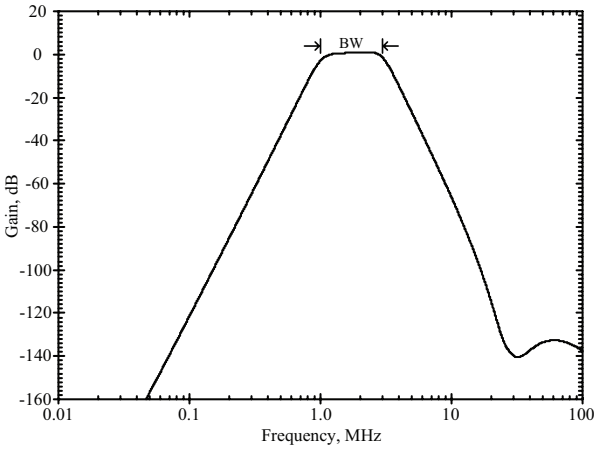

Figure 16: Simulated magnitude response of the sixth-order Butterworth BP filter.

6 Conclusions

In this paper, a new electronically tunable current-mode multifunction biquadratic filter employing one CCFTA and two grounded capacitors is presented. The proposed filter offers the following properties: (i) employment of grounded capacitors which is ideal for IC implementation; (ii) ability to implement LP, BP, HP, BS and AP filter responses without inverted input signals and passive component-matching conditions; (iii) orthogonal control of parameters ω_o and Q; (iv) current-controlled of parameter ω_o; (v) high output impedance output which can be directly connected to next the stage and (vi) low active and passive sensitivities. The proposed biquadratic filter has been used to implement high-order filters such as sixth-order Butterworth LP, HP and BP filters to confirm the applicability of the presented structure. Simulation results confirm the performance of the proposed filters.

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An LTspice simulation model of gamma-radiation effects and annealing in a voltage regulator with a lateral serial PNP transistor with round emitters

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Abstract: The aim of this paper was to determine the reasons for a complex radiation response of the commercial-off-the-shelf LM2940CT5 low-dropout voltage regulator. Examination of this circuit in a gamma-radiation environment disqualified its use when operated with relatively high output currents, while its radiation tolerance was satisfactory when load current was approximately one-tenth (or lower) of the nominal value. In order to obtain a more thorough insight into the radiation response of this integrated circuit, a detailed SPICE model was developed. This model enabled mutual comparison of the influence of serial and driver PNP power transistor parameters: forward emitter current gain, knee current and emitter resistance. The serial lateral PNP power transistor with round emitters was identified as the weakest element that crucially affected the entire circuit radiation tolerance. The effects of gamma-radiation were examined for total doses up to 500 Gy followed by three sequences of annealing. Detailed characteristics of Beta(Ic) were procured for four different kinds of bias and load conditions during irradiation. The emitter resistance increase of the serial power transistor was a primary reason for the low radiation tolerance of the entire voltage regulator; it was much more influential than the perceived decline of the PNP power transistor forward emitter current gain.

Keywords: lateral PNP transistor; radiation effects; annealing; SPICE model; voltage regulator

LTspice simulacijski model vplivov gama žarkov in žganja v napetostnem regulatorju z lateralnim PNP tranzistorjem z okroglimi emitorji

Izvleček: Namen članka je določitev vzrokov kompleksnega sevalnega odziva napetostnega regulatorja LM2940CT5. Regulator je v okolju z gama radiacijo in relativno visokimi izhodnimi tokovi neuporaben, pri izhodnem toku pod desetino nazivnega pa je njegova uporaba zadovoljiva. Za natančno analizo je bil zgrajen natančen SPICE model. Model omogoča medsebojno primerjavo parametrov serijskega in napajalnega tranzistorja. Izkazalo se je, da je serijski lateralni tranzistor najšibkejši člen vezja. Analize so bile opravljene za dozo radiacije gama žarkov do 500 Gy. Izrisane so bile natančne karakteristike za štiri kombinacije napajanja in bremena. Primarni vzrok netolerance na gama žarke je dvig upornosti emitorja.

Ključne besede: lateralni PNP tranzistor; vpliv radiacije; žganje; SPICE model; napetostni regulator.

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1 Introduction

Voltage regulators are widely used for electronic circuit power supply in aerospace, nuclear and military systems [1-4], where a harsh radiation environment heavily affects the electron devices' reliability [5]. Low-dropout voltage regulators are particularly important in battery-powered systems [6].

Usually, low-dropout voltage regulators are bipolar or BiCMOS circuits, which are based on bipolar transistors as the basic components. A considerable part of the voltage regulator chip is occupied by power transistors [3, 4], in both serial and driver element roles. PNP power devices are usually used to achieve a very low dropout voltage on the serial transistor. Due to the large area

of these transistors, high perimeter-to-area ratio and thick isolation oxide, in many cases power transistors are considered to be the most vulnerable elements of power integrated circuits to ionising radiation [7]. Vertical power transistors are generally preferred to lateral ones due to their lower vulnerability to radiation effects that affect the oxide above the base area [8]. Nevertheless, in some cases the use of power integrated circuits with lateral PNP transistors cannot be avoided; further, there are specially designed radiation-tolerant analogue integrated circuits based on these power elements [9-11].

During the previous years, detailed research was conducted in order to define the topologies of cheap, commercial-off-the-shelf (COTS) low-dropout voltage regulators suitable for implementation in radiation environments instead of specially designed "rad-hard" components [12-17]. Among these candidates was a LM2940CT5 voltage regulator, an automotive circuit with lateral PNP power transistors with round emitters. Nevertheless, experimental results clearly indicated that these commercial integrated circuits had low radiation tolerance [12-14, 16]. In the same period, examinations indicated that the specially designed, rad-hard LM2941W circuits exhibited high radiation tolerance [11]. This circuit is, in its basic topology, very similar to the LM2940CT5 circuit, so it would be justified to expect the COTS voltage regulator to demonstrate much higher radiation tolerance than what was recorded. Thus, an effort was made to examine the reasons for the low LM2940CT5 voltage regulator radiation tolerance, and this effort led to the development of a detailed simulation model of this integrated circuit.

2 Theory

Ionising radiation primarily affects bipolar transistors by reducing their forward emitter current gain, namely by a base current (I_B) increase. This excess base current (ΔI_B: difference between base current, created by the influence of radiation, and its pre-irradiation value, I_{B0} [7]) is a direct consequence of charge trapping in the isolation oxide above the base area as well as the charge trapped in the interface between the silicon and silicon dioxide. Excess base current may be approximated by the following equation [18, 19]:

$$\Delta I_B \approx \frac{qV_T n_i P_E \Delta s(D)}{2E_M} e^{\left(\frac{V_{EB}}{2V_T}\right)} \quad (1)$$

where: q – elementary electron charge ($1.6 \cdot 10^{-19}$ C), n_i – intrinsic carrier concentration in silicon, P_E – length of the emitter perimeter, $\Delta s(D) = s(D) - s(0)$ – change of the surface recombination velocity, a function of the absorbed total dose of ionising radiation D, V_{EB} – emitter-base voltage, E_M – electric field at the point of the maximum recombination of the space charge region and V_T – thermal voltage (25.9 mV at 20°C).

General expression regarding a concentration of the oxide-trapped charge, N_{ot}, is [20]:

$$N_{ot} = \sqrt{\frac{2\varepsilon_{Si} n_S}{q}\left(V_T \ln\left(\frac{n_S}{n_i}\right) - \frac{V_{tr}}{2}\right)} \quad (2)$$

where: ε_{Si} – permitivity of silicon ($1.04 \cdot 10^{-12}$ F/cm), n_S – surface electron concentration in the base area, V_{tr} – emitter – base transition voltage from the ideality factor $m < 2$ to $m = 2$. Transition voltage is defined for the surface potential in the base area ψ_s, being $\psi_s = V_{EB}/2$.

Using relation (2), a simplified model for a maximum electric field in the space-charge region was developed [18]:

$$E_M = \sqrt{\frac{2qn_S}{\varepsilon_{Si}}\left(V_T \ln\left(\frac{n_S}{n_i}\right) - \frac{V_{EB}}{2}\right)} \quad (3)$$

Therefore, in model, basically found on equations (1) and (3), excess base current is directly related to the surface recombination velocity and, consequently, to the interface traps concentration [18]:

$$\Delta N_{it} \approx \Delta I_B \frac{2E_M}{q\sigma v_{th} V_T n_i \pi P_E} e^{\left(\frac{V_{EB}}{2V_T}\right)} \quad (4)$$

where: σ – carrier capture cross section, v_{th} – carrier thermal velocity.

Nonetheless, limitation of the model described by equation (4) is taking into account only the surface recombination effects, thus neglecting the effects of the oxide trapped charge above the base area, as well as the effects of interface traps on the semiconductor surface potential. In order to take into account also some other effects, improved model for the excess base current was recently introduced [21], emphasizing the effects of interface traps on the N-type base area surface potential, ψ_S [21]:

$$\Delta I_B = \Delta I_{R-SCR} + \Delta I_{R-NBS} = \frac{qV_T \pi n_i P_E \Delta s(D)}{2E_M} e^{\left(\frac{V_{EB}-R_S I_E}{2V_T}\right)} + \\ + \frac{qn_i^2 P_E W_B \Delta s(D)}{2n_S(\psi_S)} \left[e^{\left(\frac{V_{EB}-R_S I_E}{2V_T}\right)} - 1 \right] \quad (5)$$

where: $\Delta I_{R\text{-}SCR}$ – surface recombination base current, $\Delta I_{R\text{-}NBS}$ - neutral-base-surface recombination current, R_s – the series resistance between the base and emitter, I_E – emitter current, W_B – base width.

As may be seen from equation (5), even this sophisticated model primarily takes into account interface traps [21]. Thus, its authors frequently neglected the influence of the oxide-trapped charge on the excess base current, since a positive charge trapped in the oxide layer opposes the electrostatic impact of the interface traps on the surface carriers recombination [21].

The next cause of transistor parameter degradation is charge trapping in oxide and at interfaces above emitter areas, yet the influence of these effects is not as well defined as charge trapping above the base area [19]. In PNP transistors, oxide trapped charge (during the initial period of irradiation) suppresses the negative effects of interface traps, primarily due to the accumulation of N-type base [9]. On the other hand, oxide trapped charge and interface traps have additive negative effects on the P-type emitter area [8]. Unbiased bipolar PNP transistors are the most sensitive to ionising radiation [8]. Further, high load current, which can significantly increase the chip temperature, leads to the tremendous recovery of the trapped charge and, therefore, may prevent irradiated circuit failure [4]. These effects are even more prominent in lateral PNP transistors, where both base and emitter areas are situated directly below the oxide.

After ionising radiation exposure, post-irradiation effects commence in bipolar transistors and related integrated circuits [22]. At room temperature, trapped charge tunneling is a dominant effect, while at approximately 100°C a more pronounced oxide trapped charge recovery commences [7]. Interface traps are more stable defects, so their annealing happens at 150-250°C and higher temperatures [7]. In some bipolar integrated circuits it is possible to roughly exclude the oxide trapped charge influence, where oxide trap annealing occurs at approximately 100°C. Applying even higher temperatures therefore leads to partial recovery of the interface traps [22]. The bipolar integrated circuit degree of recovery (or further degradation) after irradiation also depends on bias conditions (both during the irradiation and the following annealing), absorbed total dose, dose rate (particularly due to enhanced low-dose-rate sensitivity (ELDRS) effect), a quality of the implemented oxides, technological processes, concentration of impurities, et cetera [7].

3 Materials and methods

3.1 Experiment

A COTS LM2940CT5 circuit was used as a representative of a low-dropout voltage regulator with lateral PNP power transistors. This circuit, made by *National Semiconductor*®, has two power transistors, comprised of a multitude of parallel connected elementary lateral PNP transistors with round emitters: the serial and driver transistor [23]. The serial transistor is comprised of 350 elementary transistors, while the driver transistor is made by parallel connection of 70 PNP transistors of the same type [23, 24]. Each elementary transistor has a structure with a round emitter (13 μm in diameter) and may provide an output current of nearly 3 mA [24].

Voltage regulators were exposed to ionising radiation in the Vinča Institute of Nuclear Sciences, Belgrade, Serbia. Samples were irradiated in the vicinity of a ^{60}Co gamma-radiation source, at a dose rate of 40 mGy(SiO_2)/s. After absorption of the predefined total doses, irradiation was temporarily interrupted, and electrical characteristics of samples were examined. Then, irradiation was continued and this procedure was repeated until samples absorbed a total dose of 500 Gy(SiO_2). Integrated circuits were irradiated with various bias and load conditions: without bias during irradiation (V_{IN} = 0 V, I_{OUT} = 0 A), then with input bias voltage and negligible load (V_{IN} = 8 V, I_{OUT} = 1 mA), moderate load (V_{IN} = 8 V, I_{OUT} = 100 mA) as well as with input bias voltage and high load current (V_{IN} = 8 V, I_{OUT} = 500 mA).

Following absorption of the specified total dose, irradiated integrated circuits were kept in an office locker at room temperature for nearly ten years. After 85,000 hours, samples were again tested with the same laboratory setup in order to examine the influence of the long-term room-temperature annealing. Then, a seven-day annealing in a thermal chamber was performed at 100°C. After another round of experiments, a final annealing sequence in a thermal chamber was performed for 168 hours at 150°C.

Electrical characteristics of LM2940CT5 voltage regulators were obtained through examination of maximum output current and minimum dropout voltage (at two operating points: output currents of 100 and 400 mA). The maximum output current was detected for an in-

put voltage of 8 V DC, when output voltage declined to 4.7 V DC [12, 13]. Minimum dropout voltage (for I_{OUT} = 100 mA) was determined for a constant output current and the output voltage of 4.9 V [12, 15]. For the second operation point, when I_{OUT} was 400 mA, most of the performed measurement output voltages did not reach 4.9 V. Accordingly, results were recorded for the maximum available output voltage [16].

More details about the experimental procedures, dosimetry and radiation sources may be found in the literature [12-17, 25, 26].

3.2 Computer simulation

Previous research demonstrated myriad possibilities for the use of the open-source SPICE simulation tools for examination of radiation effects in bipolar integrated circuits [27-29]. Thus, a detailed computer simulation model was created with *LTspice IV* software [30], according to the schematic circuit diagram published in the manufacturer's data sheet [23]. The focus in the simulation model was on analysis of radiation and post-irradiation power transistor responses, i.e., serial and driver transistors. For every predefined absorbed ionising dose and period of annealing, forward emitter current gain, knee current and emitter ballasting resistance were changed for both serial and driver transistors.

Since the filter capacitor of the power source had a low value (nominally 330 µF [14, 17]), there was a large AC component of the input voltage. Due to the influence of parasitic capacitances and inductances of the power supply cables (10 m long), as well as the inevitable difference between the simulation model and the real integrated circuit, it was not sufficient to simply transfer measured filter capacitance to the *LTspice* model. Thus, in order to establish a faithful simulation model, the filter capacitor value was adjusted until the AC component of the input voltage measured during the experiment and the voltage obtained by simulation matched exactly for all the examined cases (this value was 440 µF for all the tested LM2940CT5 circuits).

Simulation of the maximum output current proceeded when the adequate filter capacitor was determined. Output current, as well as input and output voltages in the simulation model had to be approximately the same as in every particular point of the experiment. Serial and driver transistors had the same values for the forward emitter current gain, but different values for knee current and emitter resistance. Since the serial transistor had five times more elementary PNP transistors than the driver transistor, the driver transistor knee current was five times lower, whilst its emitter resistance was five times greater than for the serial transistor. In order to obtain an exact match between experimental and simulation results on the maximum output current (approximately V_{IN} = 8 V DC, V_{OUT} = 4.7 V DC), the values of the emitter resistance were precisely determined, with the accuracy in the range of 0.1 mΩ.

When these three parameters were successfully selected (forward emitter current gain (β_F), knee current (I_{KF}) and emitter resistance (R_{E12})) and simulation of the maximum output current experiment was evaluated as acceptable, simulations then determined the minimum dropout voltage. The same schematic circuit diagram had been used for two further simulations, regarding the dropout voltage with constant output currents, being 400 mA and 100 mA. If there were unacceptable disagreement in these two models with experimental results, simulation of the maximum output current was repeated, and β_{F12}, I_{KF12} and R_{E12} were determined again. Only when simulations of all three types of experiments were estimated to be satisfactory, parameters of the serial and driver transistors were accepted as true values that enabled successful modelling of γ-radiation and post-irradiation effects at all the measurement points, for all absorbed total doses and types of annealing. The above procedure was performed for all predefined control points for both irradiation and post-irradiation periods. Thus, according to the implemented simulation models, $\beta(I_c)$ characteristics were generated for all four bias and load conditions for the serial power transistor.

4 Results

The results that unify examination of the maximum output current and minimum dropout voltage, recorded in LM2940CT5 voltage regulators, are summarised in Table 1. Previously published results were complemented by the new experimental results on post-irradiation effects. Since the internal consumption currents, i.e., the voltage regulator no-load quiescent currents (I_{Q0}), were in all cases approximately the same, only the values, procured during examination of the maximum output current, are presented in Table 1. In order to obtain a complete review of the LM2940CT5 voltage regulators, the basic parameters of the serial and driver transistors, obtained by computer simulations, are included in Table 1.

As seen in Table 1, dropout voltage varied modestly, both during the irradiation and annealing. On the other hand, maximum output current variations were more substantial. Nevertheless, output voltage values decreased below the minimum acceptable value of 4.9 V while operating with a load current of 400 mA. There-

Table 1: Absolute values of input voltage (V_{IN}) and output voltage (V_{OUT}), procured during the experiment for determination of the serial transistor's minimum dropout voltage (V_{EC12}; tests with load current of 100 mA and 400 mA), as well as output current (I_{OUT}) and no-load quiescent current (I_{Q0}), procured during maximum output current (I_{MAX}) examination. Also the accompanying data on the serial transistor's excess base current (ΔI_{B12}) in the LM2940CT5 *National Semiconductor*® voltage regulator were enclosed, being a consequence of the exposure to the ionising radiation. Experimental results were extended with parameters of the serial and driver transistors (maximum forward emitter current gain (β_{Fmax}), knee current (I_{KF}) and emitter resistance (R_E)), defined in the *LTspice* simulation models. Successive periods of annealing are marked as follows: Ann.1: the first period of annealing (Θ_a = 20°C, t = 85,000 hours); Ann.2: the second period of annealing (Θ_a = 100°C, t = 168 hours); Ann.3: the third period of annealing (Θ_a = 150°C, t = 168 hours). Experimental values of I_{MAX}, V_{IN}, V_{OUT} and I_{Q0}, procured during the irradiation of LM2940CT5 voltage regulators, for total doses up to 500 Gy(SiO_2), were used from references [13], [15] and [16].

National Semiconductor® LM2940CT5		Type of experiment								Computer simulation				
Operation during irradiation and annealing		V_{EC12} (100 mA), V_{OUT} = 4.9 V		V_{EC12} (400 mA)			I_{MAX}			Parameters of PNP power transistors, Q_{12} and Q_2				
										β_{Fmax}	Parameters of the serial transistor, Q_{12}		Parameters of the driver transistor, Q_2	
Bias and load during irradiation	Dose, D [Gy]	V_{IN} [V]	ΔI_{B12} [mA]	V_{IN} [V]	ΔI_{B12} [mA]	V_{OUT} [V]	I_{OUT} [mA]	I_{Q0} [mA]	ΔI_{B12} [mA]		I_{KF12} [A]	R_{E12} [Ω]	I_{KF2} [A]	R_{E2} [Ω]
0 V,0 A	0	5.505	0	7.316	0	4.903	744.2	9.82	0	175	0.135	0.085	0.027	0.425
	50	5.501	0.06	7.485	0.11	4.782	424	9.73	-11.62	136	0.145	0.365	0.029	1.825
	100	5.439	0.24	7.921	0.08	4.785	439.4	9.61	-10.31	126	0.16	0.3457	0.032	1.7285
	200	5.471	0.45	7.39	1.47	4.721	391.5	9.37	-11.96	110	0.15	0.395	0.03	1.975
	300	5.465	0.7	7.169	2.41	4.72	392	9.13	-11.17	98	0.155	0.3798	0.031	1.899
	400	5.436	1.06	7.191	3.40	4.718	390.1	8.87	-10.33	78	0.17	0.35	0.034	1.75
	500	5.449	1.28	7.266	4.11	4.691	351.6	8.6	-11.76	66	0.17	0.3903	0.034	1.9515
	Ann.1	5.55	0.97	8.247	1.21	4.835	503.9	9.02	-4.91	84	0.22	0.238	0.044	1.19
	Ann.2	5.55	0.84	7.914	1.28	4.757	432.7	9.3	-9.37	96	0.195	0.3405	0.039	1.7025
	Ann.3	5.515	0.58	7.874	0.64	4.765	453.7	9.53	-9.1	107	0.185	0.319	0.037	1.595
8 V, 1 mA	0	5.569	0	7.468	0.00	4.904	702	9.43	0	170	0.14	0.112	0.028	0.56
	50	5.535	-0.06	7.902	-0.02	4.859	490	9.49	-7.76	165	0.13	0.29	0.026	1.45
	100	5.549	0.03	7.944	0.37	4.850	474.1	9.35	-7.96	157	0.13	0.304	0.026	1.52
	200	5.484	0.24	7.935	1.17	4.840	480.7	9.19	-6.76	143	0.13	0.284	0.026	1.42
	300	5.52	0.51	7.902	1.81	4.814	457.8	8.96	-6.86	114	0.16	0.306	0.032	1.53
	400	5.528	0.72	7.901	2.40	4.817	473.9	8.79	-5.35	93	0.2	0.28	0.04	1.4
	500	5.502	0.89	7.712	3.68	4.796	444.6	8.56	-5.94	78	0.22	0.3	0.044	1.5
	Ann.1	5.611	0.89	7.684	3.47	4.697	440.1	8.78	-6.34	78	0.235	0.316	0.047	1.58
	Ann.2	5.581	1.02	7.721	2.55	4.741	416.3	9	-8.37	72	0.26	0.35	0.052	1.75
	Ann.3	5.547	0.45	7.704	1.64	4.75	446.4	9.33	-8.07	116	0.175	0.3344	0.035	1.672
8 V, 100 mA	0	5.596	0	7.516	0	4.9	833.8	9.778	0	205	0.15	0.0415	0.03	0.2075
	50	5.578	0.27	8.007	-0.12	4.898	524.2	9.5	-8.26	160	0.145	0.263	0.029	1.315
	100	5.571	0.44	8.177	0.17	4.871	500.7	9.34	-8.56	151	0.145	0.2816	0.029	1.408
	200	5.536	0.82	8.077	1.68	4.863	495.2	9.08	-7.49	143	0.13	0.265	0.026	1.325
	300	5.519	1.08	7.903	2.66	4.845	488.9	8.81	-6.65	131	0.135	0.2648	0.027	1.324
	400	5.491	1.40	8.010	3.23	4.847	484.9	8.57	-5.80	105	0.16	0.2552	0.032	1.276
	500	5.496	1.64	7.871	4.14	4.847	495.8	8.37	-4.35	90	0.18	0.2269	0.036	1.1345
	Ann.1	5.705	1.37	7.695	4.61	4.681	433.8	8.55	-7.45	95	0.185	0.3263	0.037	1.6315
	Ann.2	5.632	1.32	7.847	3.27	4.692	401.1	8.86	-10.36	100	0.18	0.3877	0.036	1.9385
	Ann.3	5.624	1	7.905	2.11	4.724	428.3	9.2	-10.03	114	0.16	0.3473	0.032	1.7365

8 V, 500 mA	0	5.557	0	7.768	0	4.9	524	9.6	0	168	0.14	0.2638	0.028	1.319
	50	5.558	0.32	7.409	1.18	4.899	572.9	9.51	2.69	143	0.15	0.203	0.03	1.015
	100	5.56	0.49	7.602	1.45	4.9	575.9	9.34	4.01	136	0.145	0.187	0.029	0.935
	200	5.517	0.93	7.676	2.48	4.9	562.8	8.95	5.08	116	0.155	0.1821	0.031	0.9105
	300	5.556	1.02	7.867	2.98	4.87	518.1	8.63	4.22	92	0.185	0.208	0.037	1.04
	400	5.530	1.53	7.611	4.60	4.9	578.4	8.35	9.34	76	0.21	0.065	0.042	0.325
	500	5.508	1.81	7.704	4.96	4.9	569.1	8.17	9.56	66	0.25	0.03	0.05	0.15
	Ann.1	5.575	1.75	8.055	4.39	4.773	466.5	8.25	3.78	61	0.29	0.2438	0.058	1.219
	Ann.2	5.602	1.48	7.715	4.70	4.734	400.4	8.55	-0.57	66	0.22	0.332	0.044	1.66
	Ann.3	5.54	0.91	7.837	2.65	4.732	439	9.11	-0.48	89	0.22	0.3322	0.044	1.661

fore, these results highlight that, if the LM2940CT5 voltage regulator operated with only 10 % of the load current, it would be acceptable for implementation in a moderate radiation environment.

Taking into account data on the circuits, biased and heavily loaded during irradiation, the LM2940CT5 voltage regulator was acceptably radiation tolerant; its output voltage was maintained near the threshold of 4.9 V, while its characteristics sharply degraded only after removal from the radiation environment! There was also an unusual response of the excess base current (ΔI_B) during examination of the maximum output current. Excluding the heavily loaded circuits during irradiation, all other samples demonstrated negative values for the excess base current! Usually, in the radiation environment, base current increases as a consequence of ionising radiation exposure and then decreases during annealing. Such a response was indeed recorded during minimum dropout voltage examination (see Table 1), but the completely opposite response was recorded when voltage regulators were examined with the maximum output current.

In order to provide answers to these, seemingly contradictory results, a detailed computer simulation model was developed.

5 Discussion

5.1 Computer simulation

Detailed schematic circuit diagram that unified the experimental setup and LM2940CT5 voltage regulator internal structure is presented in Fig. 1, while a simplified version of the same test circuit was presented in Fig. 2. As a basis for development of the *LTspice* model of power transistors, the model of the discrete D45H11 PNP power transistor was used [31, 32]. This component is a 10 A power transistor with the following electrical characteristics: forward emitter current gain β_F = 40–60, emitter-collector breakdown voltage BV_{EC0} = 80 V and transition frequency (or gain-bandwidth product) f_T = 40 MHz [32]. Basic D45H11 transistor *SPICE* model was modified in order to meet the requirements

Table 2: SPICE parameters for serial (Q_{12}) and driver (Q_2) PNP power transistors based on the D45H11 transistor model [31]. Since the values of the forward emitter current gain (BF) and the forward knee current (IKF) were changed for every predetermined dose, their values are not included in the table.

SPICE parameters of PNP transistors Q_{12} and Q_2											
Parameter	Value	Unit	Parameter	Value	Unit	Parameter	Value	Unit	Parameter	Value	Unit
IS	7.8998e-11	A	Eg	1.1222	eV	TF	3.8976e-09	s	Cje	1.0308e-09	F
NF	0.851		BR	1.962		ITF	0.99999	A	Vje	0.6517	V
VAF	10.7084	V	Rb	4.7117	Ω	XTB	0.1376		Mje	0.3531	
Ise	4.797e-14	A	Rbm	0.2039	Ω	XTI	1.0316		Cjc	5e-10	
Ne	4		Irb	0.1086	A	XTF	1.3572		Vjc	0.4265	V
Nc	3.5938		Re	0.0001	Ω	VTF	0.9957	V	Mjc	0.2428	
Nr	1.295		Rc	0.1223	Ω	TR	4.9098e-07	s	Xcjc	0.8031	
VAR	23.2874	V	Vceo	80	V	PTF	0		Cjs	0	F
IKR	9.9963	A	Icrating	10	A	KF	0		Vjs	0.75	V
Isc	4.797e-14	A	FC	0.5335		AF	1		Mjs	0.5	

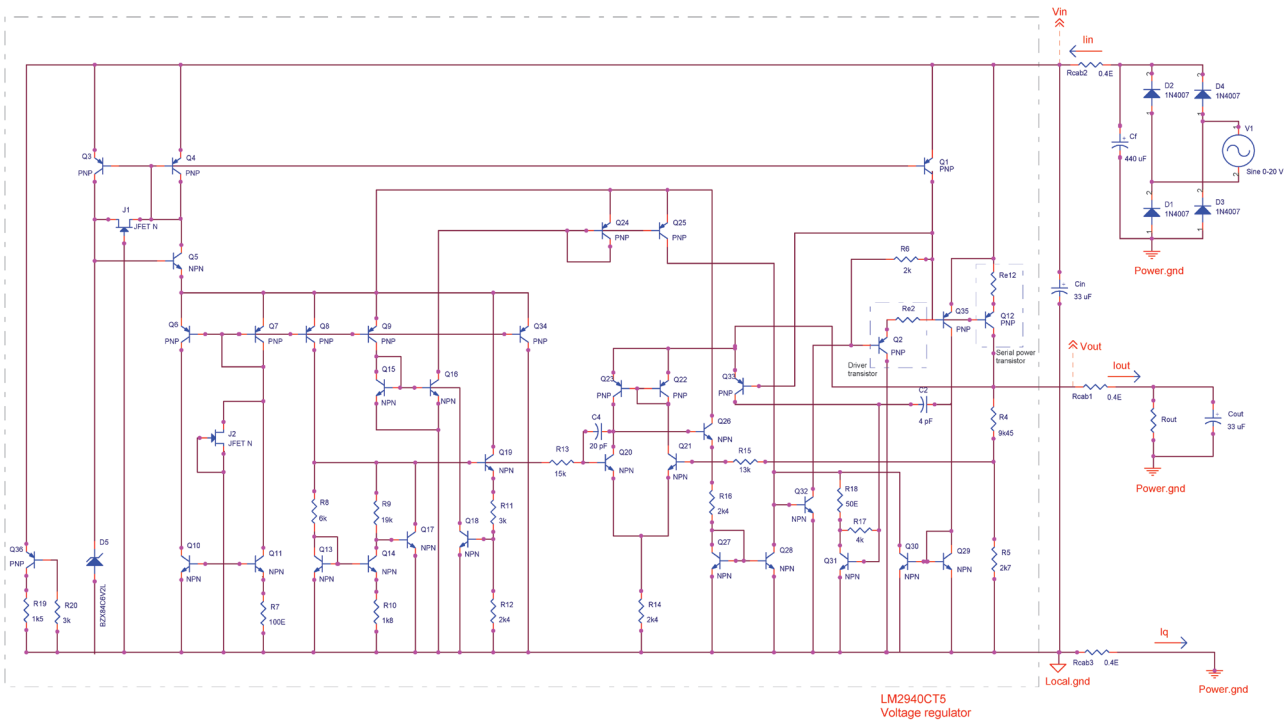

Figure 1: Detailed schematic circuit diagram of the simulation model, which was generated for examination of radiation and post-irradiation effects in the LM2940CT5 voltage regulator

for successful simulation and its harmonisation with the procured experimental results.

In order to obtain a faithful model of the implemented LM2940CT5 circuit PNP power transistor, additional resistors, R_{E12} and R_{E2} (see figures 1 and 2), were added to the serial and driver PNP power transistor emitters. The emitter resistance value of the power transistor in its *LTspice* model was kept at a constant value, while only external emitter resistance was changed, a feature that simulated radiation and post-irradiation effects in the emitter area of power transistors. *SPICE* parameters of the power transistors, the serial, Q_{12} and the driver one, Q_2 (see Fig. 1), are presented in Table 2. Most of the parameters from the original D45H11 model were not changed, but parameters related to the base resistance (Rb and Rbm) were increased twofold in order to obtain a faithful simulation of the Q_{12} power transistor response. Meaning of parameters, specified in Table 2, is given in the SPICE manual [33].

At first, a possibility was considered for significant influence of the operational amplifier output stage, supplying the driver transistor, as previously described in the literature [28]. Thus, possible influence of the output stage transistor (Q32 in Fig. 1) was evaluated on the perceived reduction of the maximum output current in LM2940CT5 voltage regulator. As in the case of all the other NPN transistors in the voltage regulator control circuit, transistor Q32 was selected as a basic model, having forward emitter current gain β_{F32} = 100. Influence of γ-radiation on the output stage transistor, Q32, was simulated by reduction of its current gain. None-

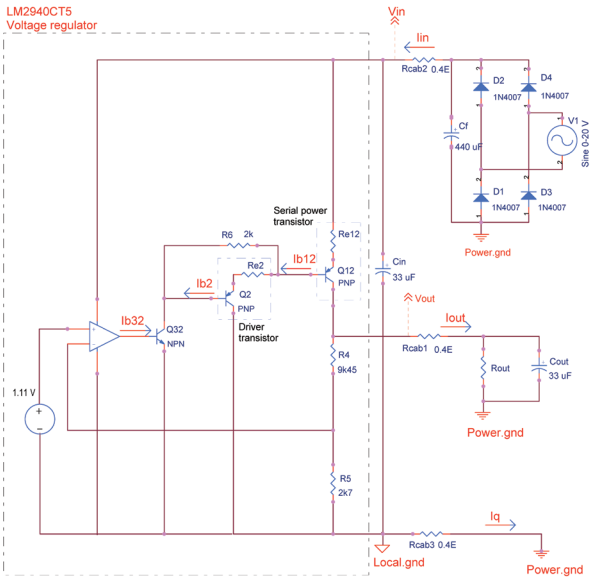

Figure 2: Simplified schematic circuit diagram of the simulation model presented in Fig. 1. The most important elements and nodes used for the analysis of the LM2940CT5 voltage regulator, presented in Table 1, are emphasized in the plot

theless, procured results led to the conclusion that the parameters of the transistor Q32 had negligible effect on the serial transistor's base current and the voltage regulator maximum output current. Even a fivefold reduction of its current gain (down to β_{F32} = 20) led to only 0.5 % reduction of the serial transistor base current, whilst keeping the voltage regulator maximum output current almost unchanged.

Therefore, according to the previous analysis, as well as the published data [12-16], it was assumed that the elements of the control circuit would have constant values, while the values of two power transistors (serial and driver PNP transistors) were changed for every control point. Comparison of the experimental and simulation data for the base current of the serial PNP power transistor, I_{B12}, are presented in figures 3 - 6. Used parameters of the serial and driver transistors, for every predetermined irradiation and annealing point, are presented in Table 1. Successive periods of annealing are marked in the same way as in the capture of Table 1.

Thus, the data presented in Table 1 and figures 3 - 6 indicate the relatively small influence of radiation and post-irradiation effects on the serial power transistor knee current, a much greater effect on its forward emitter current gain and, finally, a substantial influence on emitter resistance. This last parameter crucially affected the radiation hardness of the serial power transistor and, consequently, the radiation response of the LM2940CT5 voltage regulator.

In general, for increased total ionising dose, the current gain of power transistor declined, knee current increased and, usually, emitter resistance increased.

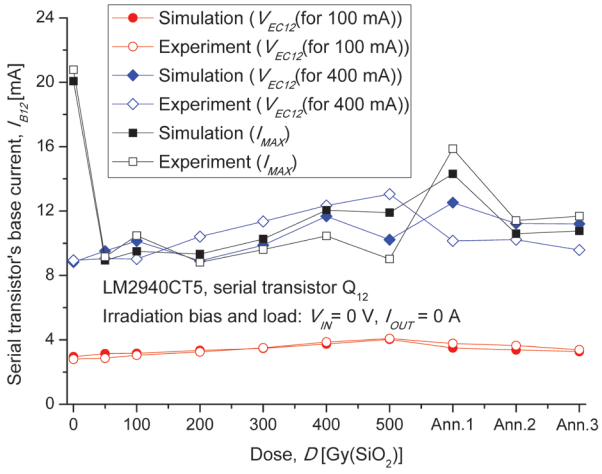

Figure 3: Variations of the serial transistor's base current as a function of the total ionising dose and type of annealing: comparison between simulation and experimental results. Bias conditions during irradiation: V_{IN} = 0 V, I_{OUT} = 0 A.

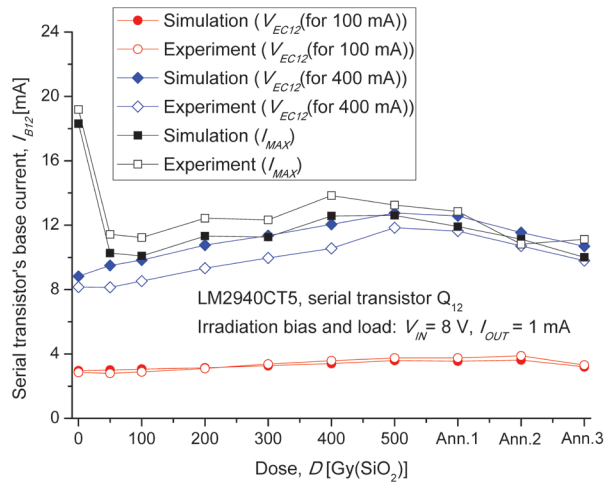

Figure 4: Variations of the serial transistor's base current as a function of the total ionising dose and type of annealing: comparison between simulation and experimental results. Bias conditions during irradiation: V_{IN} = 8 V, I_{OUT} = 1 mA.

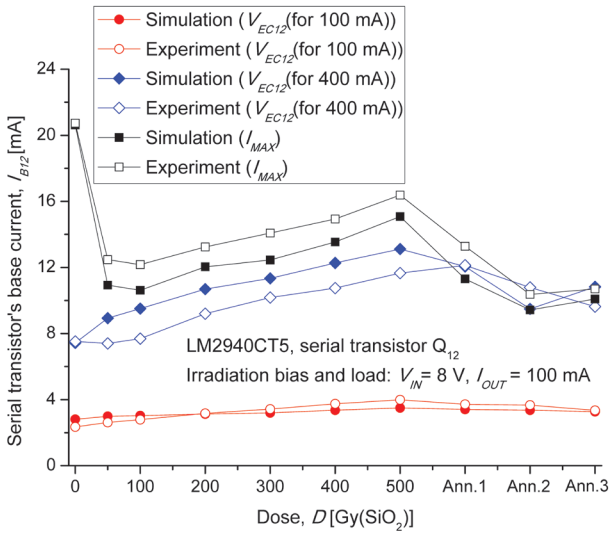

Figure 5: Variations of the serial transistor's base current as a function of the total ionising dose and type of annealing: comparison between simulation and experimental results. Bias conditions during irradiation: V_{IN} = 8 V, I_{OUT} = 100 mA.

When knee current was too low, for simulation of the maximum output current, base current of the serial transistor was too large. If a current gain would be too high, a base current (for minimum dropout voltage with output current of 100 mA) would be too low, in comparison with experimental values. If emitter resistance would not match exactly with the filter capacitor, the input (≈ 8 V DC) and output voltage (≈ 4.7 V DC), obtained experimentally, could not match the simulation results when the maximum output current was ex-

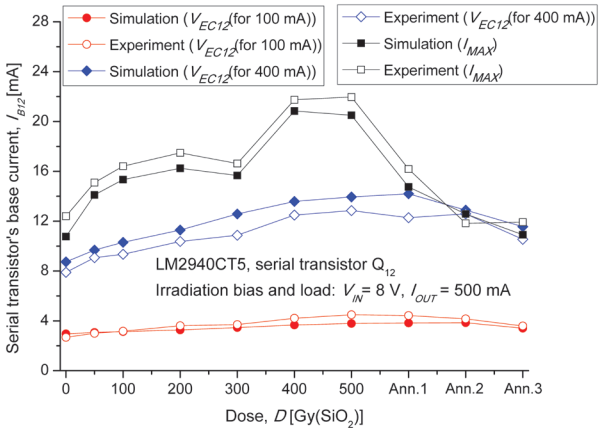

Figure 6: Variations of the serial transistor's base current as a function of the total ionising dose and type of annealing: comparison between simulation and experimental results. Bias conditions during irradiation: V_{IN} = 8 V, I_{OUT} = 500 mA.

amined. Therefore, using a procedure of trial and errors, acceptably good combination of the serial power transistor parameters β_{F12}, I_{KF12} and R_{E12} have been achieved.

Criterium for the acceptable deviation of simulation results from the experimental ones was mainly defined as a compromise between overshoot of the simulated base current, obtained during examination of the minimum dropout voltage (for I_{OUT} = 400 mA), and undershoot of the same simulated value, procured whilst maximum output current was determined. Thus, the parameters of the serial lateral PNP transistor were changed until a balance was achieved between deviation of base currents (I_{B12}), procured during an experiment and simulation. An effort was made to keep the deviation between experimental and simulation results of base currents up to 10 – 15 %. Only in several extreme points (see, for instance, Fig. 3: D = 500 Gy (SiO$_2$)) this range was exceeded, when the deviation reached, at most, 30 %.

At last, when simulations of all the experiments were finished, for all the total doses and annealing sequences, new simulations had been made. These characteristics, presented in Fig. 7, were produced for serial transistor collector currents, which ranged from 1 - 400 mA, and for a constant emitter-collector voltage of 3.3 V. Since the maximum output current for samples of unbiased voltage regulators in many cases declined below 400 mA, simulation results for 300 mA were also included.

5.2 Radiation effects

Bias conditions implemented during irradiation primarily affected variations of the serial transistor's emitter resistance, R_{E12}. On the other hand, bias condition influences were less apparent on variations of the forward emitter current gain and knee current, since these measures were primarily affected by the absorbed total ionising radiation dose. Deposition of the total 500 Gy dose in all cases decreased forward emitter current gain by 54 - 62 %. The knee current was more sensitive to the bias conditions, since it increased by 20 - 80 %. Nevertheless, emitter resistance variations exhibited a wide range of behaviour; they sharply increased when the circuit did not operate with high load current during the irradiation and steadily decreased when integrated circuits were biased and heavily loaded during gamma-radiation exposure. $\beta_F(I_{C12})$ characteristics were generated for I_{C12} collector currents between 1 – 400 mA (Fig. 7). Simulation results revealed that, simultaneously, collector current of Q_2 driver transistor changed only from 1.6 mA up to 12 mA. For the specified range of collector currents of the serial power transistor, and taking into account all the control points, the computer simulation provided emitter-base voltage values (V_{EB12}) between 355 and 691 mV.

The marked differences between the emitter resistance variations, recorded for various bias conditions, demonstrate different dominant mechanisms of the charge buildup in oxides and interfaces of irradiated integrated circuits. Based on the data presented in Table 1 and figures 3 - 6, one can conclude that the serial power PNP transistor emitter area was, for the first three cases, primarily affected by the initial buildup of the oxide trapped charge following the absorption of 50 Gy radiation. This initial absorbed dose significantly decreased the maximum output current and, consequently, the entire voltage regulator radiation tolerance. Nevertheless, this phenomenon did not occur for the samples that were heavily loaded during irradiation. In these circuits, emitter resistance steadily decreased as the absorbed dose increased, and declined nearly ninefold after 500 Gy radiation absorption. At the same time, the serial transistor forward emitter current gain decreased by 60 %. Data on the maximum output current and minimum dropout voltage (for total ionising dose of 500 Gy) revealed that the overall performance of heavily loaded voltage regulators slightly improved (see Table 1). This result suggests that the voltage regulator radiation tolerance was more affected by the positive influence of the serial transistor emitter resistance decline than by the negative influence of the serial transistor current gain reduction.

It is important to define the reason for the maximum current improvement of the samples heavily loaded during irradiation. As previously mentioned, high load current may significantly increase chip temperature and thus lead to oxide-trapped charge annealing. Nev-

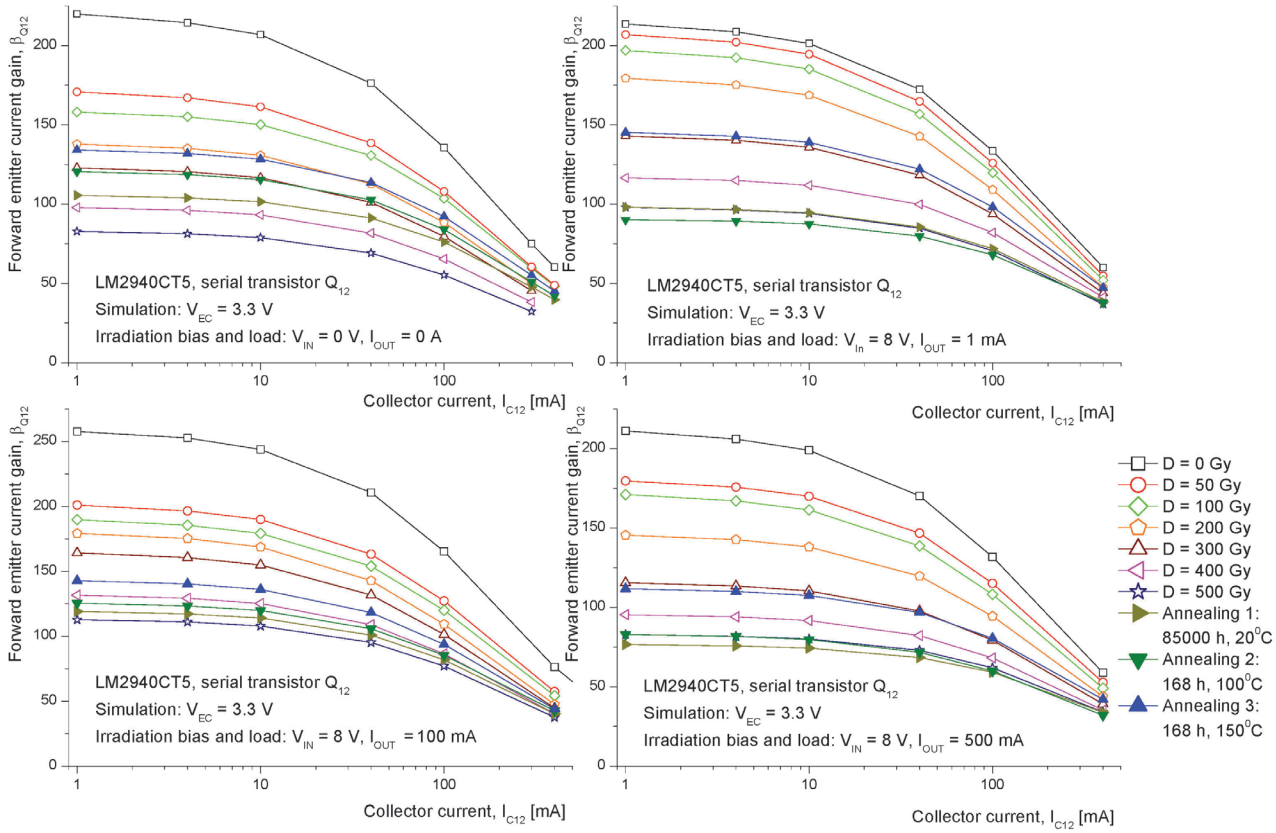

Figure 7: Variations of the current gain of the serial power transistor Q_{12} in the LM2940CT5 voltage regulator, presented as a function of the collector current in: a) unbiased circuits (V_{IN} = 0 V, V_{OUT} = 0 A); b) biased and negligibly loaded (V_{IN} = 8 V, V_{OUT} = 1 mA); c) biased and moderately loaded (V_{IN} = 8 V, V_{OUT} = 100 mA); d) biased and heavily loaded circuits during irradiation (V_{IN} = 8 V, V_{OUT} = 500 mA). Diagrams were created for a constant emitter-collector voltage, V_{EC} = 3.3 V. Data were obtained from computer simulation models of the irradiated and annealed voltage regulators, which demonstrated high agreement with the experimental results presented in Table 1 and figures 3 - 6.

ertheless, this factor is connected with the total power dissipation and, consequently, to the emitter-collector dropout voltage. Since the input voltage was 8 V during irradiation, the dropout voltage was nearly 3 V. Taking into account an output current of 0.5 A, power dissipation was 1.5 W. The total thermal resistivity of the LM2940CT5 voltage regulator is approximately 18 K/W (thermal resistivities of the implemented heatsink and junction-case structure of the TO-220 package were, respectively, 14 K/W [14] and 4 K/W [23]), as well as an ambient temperature of 20°C, there could be a theoretical chip temperature rise of up to 47°C. Nevertheless, this value is low for any expressed annealing of the oxide-trapped charge, since the oxide-trapped charge significantly anneals only when temperatures exceed 75–100°C [34], and interface traps at even higher temperatures, up to 250°C [7].

In previous research, a detailed discussion was dedicated to analysis of the influence of the trapped charge type on the LM2940CT5 voltage regulator radiation response [16]. Taking into account that, above the base and emitter areas of the lateral power PNP transistor was highly contaminated isolation oxide, with an approximate thickness d_{ox} = 500 nm [12], it was assumed that the oxide trapped charge would primarily affect this integrated circuit radiation response, while the interface trap concentrations would have secondary importance [16]. The primary reason for this supposition was the expectation that the concentration of the charge trapped in the oxide would be very high, with a proportion of $N_{ot} \sim d_{ox}^{\ 2}$ [34, 35] or even $N_{ot} \sim d_{ox}^{\ 3}$ [34]. Nevertheless, a more recent publication revealed that in thick oxides, at room temperature and at low electric fields, charge yield would be relatively low, since most of the oxide bulk would not influence the total concentration of the oxide trapped charge [36]. Accordingly, in most real applications, in thick isolation oxides of bipolar integrated circuits, the concentration of the oxide trapped charge would not be proportional to the square of the oxide thickness, but rather much weaker dependence than $N_{ot} \sim d_{ox}^{\ 2}$, primarily observed in thin

gate oxides of metal-oxide-semiconductor (MOS) devices [35]. Thus, in most practical cases, the influence of the interface trap concentrations (N_{it}) would be of primary importance to bipolar integrated circuit radiation response.

Therefore, it may be assumed that high current flow in the LM2940CT5 voltage regulator primarily passivated switching states, i.e., traps at the interface silicon–oxide and at the accompanying border oxide region, which lead to voltage regulator recovery from gamma-radiation influence. This proposition is much more plausible than the influence of high current on the oxide-trapped charge itself, either due to chip temperature increase or the high-current-density effect on the oxide below the wide emitter's metal contacts [16]. Large emitter resistivity variations in virgin, unirradiated devices indicate a defect build-up even in the fabrication phase of integrated circuits that would consequently decrease the voltage regulator's maximum output current (as have been seen in [12]).

The developed *LTspice* simulation model and obtained electrical characteristics $\beta(I_{C12})$, as well as the previously presented line regulation characteristics [16], mutually show the primary cause of the LM2940CT5 voltage regulator low radiation tolerance was primarily related with high emitter resistance of the serial PNP power transistor Q_{12}.

5.3 Post-irradiation effects

As mentioned earlier, three annealing sequences were selected to analyse the dominant influence of various kinds of trapped charge on the radiation response of the LM2940CT5 voltage regulator. It would be expected that long-term, room temperature annealing should allow partial recovery of the oxide-trapped charge with further build-up of interface traps [25, 37]. Then, one-week 100°C annealing should allow recovery of most of the remaining oxide-trapped charge without seriously affecting the interface traps [17, 23]. Finally, 168-hour, 150°C annealing should remove most residual interface traps while simultaneously eliminating all remaining oxide trapped charge [17, 22]. Thus, such an approach enables a rough estimation of the influence of bias and load conditions on charge trapping in the LM2940CT5 voltage regulator.

Data from Table 1 and Fig. 7 indicate great variation in the post-irradiation response of the various voltage regulator samples. Current-gain characteristics of the serial power transistor, $\beta(I_{C12})$, are good foundations for analysis of these circuit responses. The first conclusion is that post-irradiation effects related to the serial transistor's forward emitter current gain and knee current, on the one hand, and the emitter resistance, on the other, showed no correlation; both demonstrated variations in separate ways. Heavily loaded voltage regulators demonstrated slight degradation of the serial transistor current gain during the ten-year room-temperature annealing, while moderately loaded circuits showed slight recovery. However, in both mentioned cases emitter resistance increased (sevenfold for the heavily loaded circuits). At the same time, negligibly loaded circuits (I_{OUT} = 1 mA) seemingly remained unaffected by the room-temperature annealing sequence, both from the perspective of current gain and emitter resistance. Finally, unbiased samples demonstrated great recovery of the serial transistor's current gain, followed by significant reduction in emitter resistance. Thus, a conclusion may be drawn that during radiation exposure the unloaded circuits were heavily affected by the oxide-trapped charge. Biased and negligibly loaded samples were seemingly unaffected by the oxide trapped charge, and, consequently, ten-year build-up of the interface traps. Room-temperature annealing apparently caused more substantial degradation to the voltage regulator operated with higher load current during radiation exposure. In this case, it may be assumed that the interface states buildup resulted in the marked emitter resistance increase.

The next step was one-week, 100°C annealing. Except in the case of unloaded voltage regulators, this test marginally affected the serial transistor's forward emitter current gain, while, for all biased samples, emitter resistance increased (most prominently in the heavily loaded devices). This test was intended primarily to remove the oxide-trapped charge. Thus, the obtained results (Table 1 and Fig. 7) supported the previous conclusion that, in all the voltage regulators, biased during irradiation, serial transistors were, in comparison with the influence of interface traps, marginally affected by the influence of the oxide trapped charge.

Finally, the third annealing procedure was 168-hour, 150°C exposure of irradiated samples in a thermal chamber. Such an annealing procedure, designed for the removal of most interface traps, led to the recovery of the serial transistor current gain in all of the examined circuits. The most prominent was the forward emitter current gain recovery in biased, negligibly loaded voltage regulators. Further, emitter resistance declined or remained the same in all cases. Nevertheless, all the examined circuits were far from complete recovery from the ionising radiation influence, since the serial transistor current gain remained approximately 60 % of its pre-irradiation value. Yet, there was a very interesting result regarding the serial transistor emitter resistance, R_{E12}. Despite great initial variations obtained by simulations from the experimental results (see Table 1), at the end

of the third annealing sequence, emitter resistances for all serial transistors, regardless of the bias conditions of irradiated voltage regulators, were nearly the same! The maximum values of the output voltage, obtained during the examination of the minimum dropout voltage (with a constant output current of 400 mA) were also nearly the same (V_{OUT} = 4.724 – 4.765 V; Table 1). Thus, at the end of the high-temperature annealing process, it may be assumed that only interface traps remained in the LM2940CT5 voltage regulator, and they heavily affected the serial transistor emitter resistance and forward emitter current gain.

6 Conclusion

The COTS LM2940CT5 voltage regulator was examined in a gamma-radiation environment, where it was exposed to up to 500 Gy radiation, followed by analysis of its performance in various annealing procedures. In order to analyse these radiation and post-irradiation effects, a detailed *LTspice* simulation model of this integrated circuit was developed.

Implementation of the simulation model clearly identified the serial power transistor, comprised of 350 elementary lateral PNP transistors, as the weakest part of the entire integrated circuit. Radiation effects in small signal transistors, as well as in the driver PNP power transistor, did not significantly affect the LM2940CT5 voltage regulator's radiation tolerance. On the other hand, primarily the increase of the serial transistor emitter resistance, followed by the decrease of its forward emitter current gain, disqualifies this circuit for use in a radiation environment.

This integrated circuit demonstrated great influence from bias and load conditions on its radiation tolerance. With the exception of samples that operated with a high load current during irradiation, all the other circuits demonstrated a significantly increased serial PNP power transistor emitter resistance even after initial irradiation (50 Gy total dose). On the other hand, operation with high load current during irradiation led to a multifold reduction in emitter resistance concomitant with an increase in the voltage regulator's maximum output current, regardless of the simultaneous significant reduction of the forward emitter current gain. As expected, serial transistors of unbiased and unloaded voltage regulators exhibited the greatest degradation in the ionising radiation environment; both forward emitter current gain and emitter resistance were affected.

In most of the examined cases, three annealing sequences further degraded emitter resistance. There was significant recovery of forward emitter current gain observed in all the irradiated LM2940CT5 voltage regulators. Serial transistors of unbiased and unloaded circuits demonstrated the most prominent recovery during the 10-year room-temperature annealing. One-week, 100°C annealing led to significant recovery only of the unbiased circuits. Finally, one week, 150°C annealing sequence led to significant recovery of the forward emitter current gain of serial lateral PNP power transistors in all the examined integrated circuits. This final annealing procedure unified emitter resistance in all of the analysed circuits, regardless of their initial values or bias conditions during operation in a gamma-radiation environment.

7 Acknowledgement

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Novel Dual Mode Multifunction Filter Employing Highly Versatile VD-DXCC

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Abstract: In this research a new highly versatile analog building block (ABB), the voltage differencing dual X current conveyor (VD-DXCC), is proposed. It is employed to synthesize a versatile dual mode biquadratic filter. The proposed filter uses canonical number of passive elements and has inbuilt tunability feature. In addition, the proposed filter can work as multi input single output (MISO) and single input multi output (SIMO) filter in current mode (CM) of operation. Furthermore, the quality factor and pole frequency of the filter can be set independently. The non-ideal gain analysis and sensitivity analysis of the filters is also carried out to study the effect of process variations and process spread on the filter response. The proposed designs are validated using 0.18um Silterra Malaysia process design kit (PDK) in Cadence Virtuoso design software. The parasitic extraction is carried out using Calibre tool from Mentor Graphics. The complete layout of the VD-DXCC is made and post layout simulation results are given for each design. The post layout results are in close agreement with the theoretical analysis.

Keywords: biomedical signal processing, current mode; current conveyor; filter; voltage mode

Nov multifunkcijski filter z dvojnim delovanjem v visoko prilagodljivem VD-DXCC

Izvleček: V članku je predstavljen nov visoko prilagodljiv analogni blokovni napetostno diferenčni tokovni ojačevalnik (VD-DXCC), ki vsebuje prilagodljiv bi-kvadratni filter. Filter vsebuje kanonično število pasivnih komponent in ima sposobnost nastavljanja. Filter lahko deluje v več-vhodnem eno-izhodnem ali eno-vhodnem več-izhodnem načinu. Model je preverjen v 0.18 um Silterra Malaysia načrtovalskem kitu in programskem paketu Cadence Virtuoso. Rezultati izdelave se ujemajo s teoretično analizo.

Ključne besede: biomedicinsko procesiranje signalov; tokovni način; tokovni ojačevalnik; filter; napetostni način

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1 Introduction

Analog circuits play a vital role in all electronic systems. The analog circuits are used for interfacing analog world with the digital systems or as standalone high speed signal conditioning systems. The analog signal processing (ASP) offers tremendous benefits over digital signal processing (DSP), especially in terms of chip area, power consumption and speed [1]. All naturally occurring signals are analog in nature, in order to process them digitally the signals need to be converted from analog domain to digital domain and back to analog domain after processing. The digital signal processors require the extra analog to digital converter (ADC) and digital to analog converter (DAC) together with interfacing circuits this increases the power and area requirement of digital signal processing. Recently, the current mode analog active blocks are widely utilized by the researchers in designing analog filters due their advantages over voltage mode circuits [2-3]. The most utilized current mode active blocks are the second generation current conveyor (CCII) [1], differential difference current conveyor (DDCC) [2], fully differential current conveyor (FDCCII) [11], current feedback operational amplifier (CFOA) [1], current backward transconductance amplifier (CBTA) [8], current conveyor transconductance amplifier (CCTA) [22], differ-

ential voltage current conveyor (DVCCII) [10], voltage differencing current conveyor (VDCCII) [11], differential voltage current conveyor transconductance amplifier (DVCCTA) [15] etc. Each block carries its own advantages in context to the same the authors in this paper propose another versatile ABB namely the voltage differencing dual X current conveyor (VD-DXCC).

Filters are a critical part of any electronics system. They are employed in data acquisition systems, communication equipment, phase shifters, oscillator designs and bio-medical devices etc. [1, 19]. Portable and network connected medical devices for real time monitoring and diagnosis of diseases will be vital in detecting diseases for future medical observation system. To develop such a system low power and low noise analog circuits such as amplifiers and filters are required for physiological signal acquisition and signal processing. The filters are also vital parts in bio-medical data acquisition systems like sensors for artificial kidney for blood flow and filtration rate detection etc. The universal filters are most versatile as they can provide low pass (LP), high pass (HP), notch pass (NP), band pass (BP) and all pass (AP) responses from a single configuration. The main attributes that are desirable in any filter structure are (i) tunability (ii) use of minimum number of passive elements (iii) no requirement of matching between passive components (iv) provision of independent tunability of pole frequency and quality factor (v) use of minimum number of active blocks. The Table 1 provides a detailed literature survey of some exemplary MISO filters from the literature. The study points out that most of the designs suffer from one of the following issues (i) excessive use of active blocks and passive components (ii) lack of tunability (iii) requirement of passive component matching (iv) need of inverting input signal for the realization of filter function.

In this research a highly versatile ABB the VD-DXCC is developed and utilized in design of a MISO dual mode universal filter and SIMO CM filter. The proposed circuits utilized one ABB and minimum passive components. The designed circuits are electronically tunable via bias current of the OTA. The proposed circuits are

Table 1: Comparison of MISO filters available in the literature with the proposed filter

S. No.	Mode of Operation	Active Block Used(No.)	No. of R+C	No. of grounded C+R	Matching Condition	Electronic Tunability	Inverting Input Needed	Low output Impedance	Power Dissipation
[20]	MISO (VM)	CCII+ (3)	2+2	0+0	No	No	No (Except for AP)	No	-
[21]	MISO (VM)	DVCC (3)	4+2	2+3	No (Except for AP)	No	No	No	4.266 mW
[22]	MISO (VM)	CCTA (1)	2+2	0+0	No	Yes	No	No	-
[23]	MIMO (VM)	DVCC (1)	2+2	0+0	Yes	No	No	No	-
[24]	MISO (VM)	DOCCCII (2)	0+2	0+0	No	Yes	No (Except for AP)	No	-
[25]	MISO (VM)	VD-DIBA	1+2	0+0	No	Yes	No	No	-
[26]	MISO (VM)	CDBA (2)	4+2	0+0	Yes	No	No	Yes	-
[27]	MISO (VM)	DDCC (2)	2+2	2+1	No	No	No	No	-
[28]	MIMO (VM)	FDCCII (1)	3+2	1+1	No	No	No (Except for AP)	No	-
[29]	MISO (VM)	DDCC (3)	2+2	2+2	No	No	No	Yes	-
[30]	MISO (VM)	CCII (2)	3+2	0+0	Yes	No	Yes	Yes	3.65 mW
Proposed	MISO(VM & CM)/ SIMO CM	VD-DXCC (1)	2+2	1+0	No (except in MISO CM)	Yes	No	Yes	2.237 Mw (for VM Mode)

validated using 0.18µm PDK from Silterra Malaysia in Cadence to verify the theoretical predictions.

2 Voltage differencing dual X current conveyor

The block diagram of VD-DXCC is shown in Figure 1 and the current voltage equations are presented in matrix Equation 1. The VD-DXCC is a two stage ABB. The first stage consists of operational transconductance amplifier (OTA) and second stage is dual X current conveyor (DXCC).

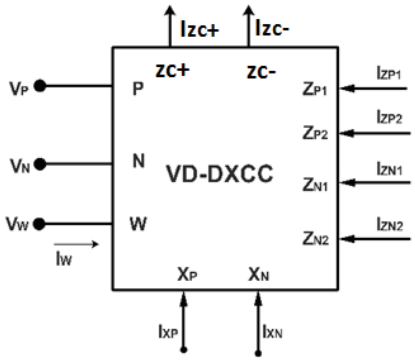

Figure 1: Block diagram of VD-DXCC

$$\begin{bmatrix} I_N \\ I_P \\ I_{zc\pm/I_W} \\ V_{XP} \\ V_{XN} \\ I_{ZP1} \\ I_{ZP2} \\ I_{ZN1} \\ I_{ZN2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_W \\ I_{XP} \\ I_{XN} \\ V_{ZP1} \\ V_{ZP2} \\ V_{ZN1} \\ V_{ZN2} \end{bmatrix} \quad (1)$$

The CMOS implementation of VD-DXCC is presented in Figure 2. The transistors (M25-M36) form the OTA which is the first stage of the VD-DXCC. The output current of the OTA depends on the voltage difference between voltages at terminals *P* and *N*. Assuming saturation region operation for all transistors and equal W/L ratio for transistors M25 and M26 the output current $I_{ZC^{\pm}} = I_W$ of the OTA is given by Equation 2. The $ZC\pm$ terminals are high impedance current output terminals.

$$I_{ZC^{\pm}} = I_W = g_m\left(V_P - V_N\right) = \left(\sqrt{2I_{Bias}k_i}\right)\left(V_P - V_N\right) \quad (2)$$

Where, $K_i = \mu C_{ox} W/2L$ (i=25, 26), W is the effective channel width, L is the effective length of the channel, C_{ox} is the gate oxide capacitance per unit area and µ is the carrier mobility.

The second stage consists of transistors (M1-24). The W terminal is high impedance voltage input terminal, the X_p and X_N terminals are low impedance current input terminals and the $Z_{P1\text{-}2}$, $Z_{N1\text{-}2}$, terminals are high impedance current output terminals.

3 Layout design

The complete layout of the VD-DXCC is designed using Silterra Malaysia 0.18µm PDK in cadence design suit. The high performance nhp and php MOS transistors are used for the design. To minimize the effect of parasitics the transistors are put as close as possible. Three level of metal layers are used for the interconnections. The complete layout is presented in Figure 3. The layout occupies an area of (55*25.73µm^2).

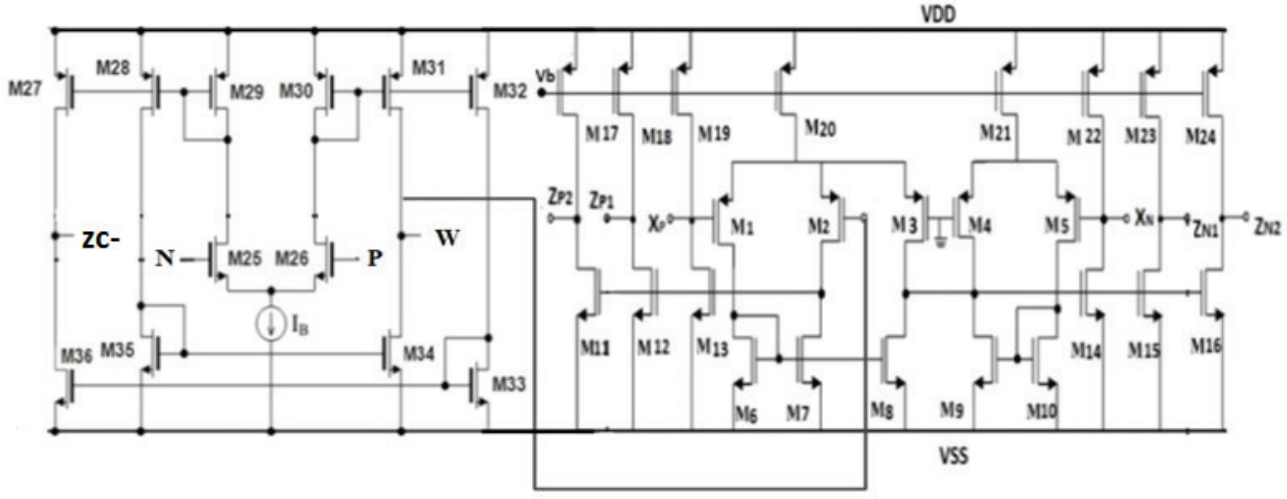

Figure 2: CMOS Implementation of VD-DXCC

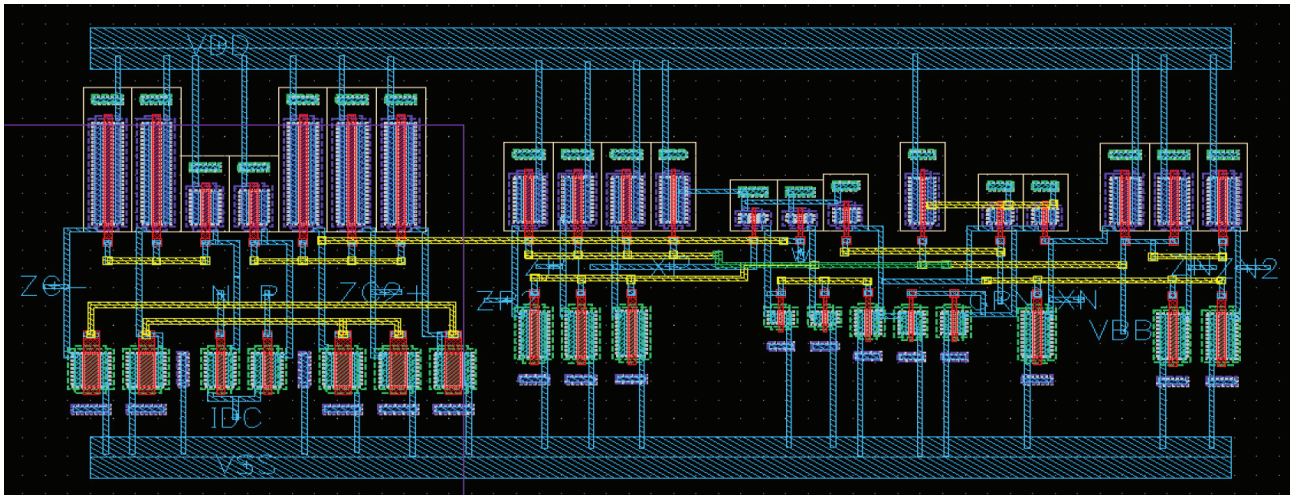

Figure 3: Layout of the VD-DXCC

4 Proposed dual mode universal filter

The proposed dual mode MISO filter is presented in Figure 4. The filter consists of four passive elements and can work in VM and CM without requiring any changes in its topology. Furthermore, the proposed filter with addition of some extra output terminals can function as CM SIMO filter as well. The features of the filter include ability to work in dual modes, no requirement of negative inputs for realization of filter functions, orthogonal control of frequency and quality factor, simultaneous availability of inverting and non-inverting outputs in the VM configuration, availability of current output at high impedance node, no matching between passive elements is required (except in CM MISO configuration) and tunability. The operation of filter in MISO and SIMO configurations is discussed below:

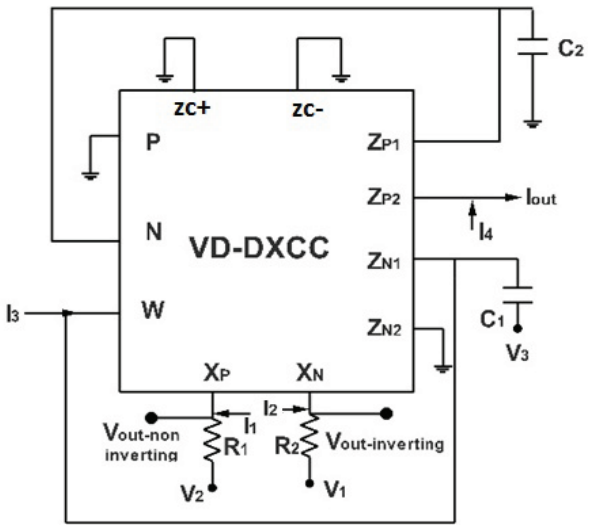

Figure 4: Dual mode MISO universal filter

4.1 Voltage Mode Operation in MISO Configuration

In this mode of operation, the input currents I_1 to I_4 are set to zero. The input voltage V_1 to V_3 are applied according to Table 2 to realize a given filter response. In the design capacitor C_2 is always grounded which is beneficial for integrated circuit implementation. Structures using grounded capacitors are advantageous with respect to reducing parasitic effects and the chip area, as the floating capacitor has bigger parasitic capacitances and requires larger chip area [31-32]. The output of the filter can be obtained from low impedance X_p and X_N nodes. This filter provides both inverting and non-inverting output signals which is another striking feature of the design. The filter transfer function and expression for frequency are given in Equations (3-5).

$$V_{out} = \frac{S^2 V_3 C_1 C_2 R_1 R_2 - sR_1 C_2 V_1 + g_m R_2 V_2}{S^2 C_1 C_2 R_1 R_2 + sC_2 R_1 + R_2 g_m} \tag{3}$$

$$\omega_o = \sqrt{\frac{g_m}{C_1 C_2 R_1}} \tag{4}$$

$$Q = R_2 \sqrt{\frac{g_m C_1}{C_2 R_1}} \tag{5}$$

Table 2: Input Excitation Sequence for VM

Response	Inputs			Matching Required
	V_1	V_2	V_3	No
LP	0	0	1	No
HP	1	0	0	No
BP	0	1	0	No
NP	1	0	1	No
AP	1	1	1	No

4.2 Current Mode Operation in MISO Configuration

In CM operation the input voltages V_1 to V_3 are reduced to zero grounding all the passive elements. The input current I_1 to I_4 are applied according to Table 3 to realize a given filter response. As can be deduced from the filter structure the output current is obtained from high output impedance terminal which is necessary for cascading. The filter requires a simple resistive matching condition for realizing HP, NP and AP responses. The slight drawback is the requirement of double input to realize AP response but given the capability of the filter to work in dual mode this can be accommodated. The transfer function and expression for frequency are given Equation (6-8).

$$I_{out} = \frac{(S^2C_1C_2R_1R_2 + sR_1C_2 + g_mR_2)I_4 - ((S^2C_1C_2R_1R_2 + sR_1C_2)I_1 \\ -sR_2C_2I_2 + sR_2C_2I_3}{S^2C_1C_2R_1R_2 + sC_2R_1 + R_2g_m} \quad (6)$$

$$\omega_o = \sqrt{\frac{g_m}{C_1C_2R_1}} \quad (7)$$

$$Q = R_2\sqrt{\frac{g_mC_1}{C_2R_1}} \quad (8)$$

Table 3: Input Excitation Sequence for CM

Response	Inputs				Matching Required
	I_1	I_2	I_3	I_4	
LP	1	0	0	1	No
HP	1	1	0	0	$R_1 = R_2$
BP	0	0	1	0	No
NP	0	1	0	1	$R_1 = R_2$
AP	0	2	0	1	$R_1 = R_2$

4.3 Current Mode Operation in SIMO Configuration

The SIMO filter structure is shown in Figure 5. As can be seen from the figure the filter has same topology as the previously discussed dual mode MISO filter presented in Figure 4. This topology has additional output terminals to provide explicit current output from high impedance nodes. The filter transfer function and expression for pole frequency and quality factor are summarized in Equations 9-13.

$$\frac{I_{HP}}{I_{IN}} = -\frac{S^2C_1C_2R_1R_2}{S^2C_1C_2R_1R_2 + sC_2R_1 + R_2g_m} \quad (9)$$

$$\frac{I_{LP}}{I_{IN}} = -\frac{g_mR_2}{S^2C_1C_2R_1R_2 + sC_2R_1 + R_2g_m} \quad (10)$$

$$\frac{I_{BP}}{I_{IN}} = -\frac{sC_2R_1}{S^2C_1C_2R_1R_2 + sC_2R_1 + R_2g_m} \quad (11)$$

$$\omega_o = \sqrt{\frac{g_m}{C_1C_2R_1}} \quad (12)$$

$$Q = R_2\sqrt{\frac{g_mC_2}{C_1R_1}} \quad (13)$$

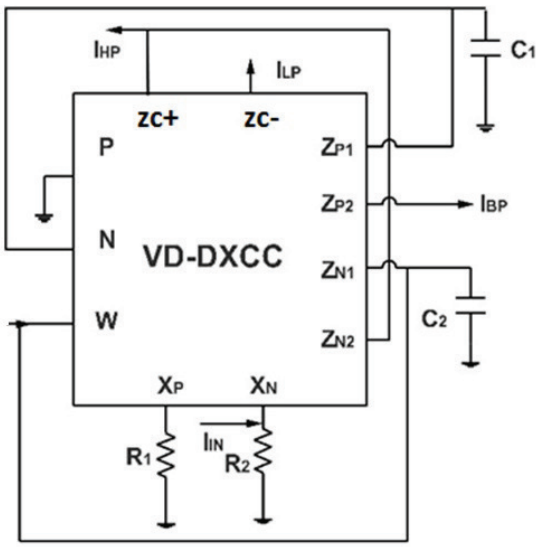

Figure 5: SIMO filter structure

5 Non-ideal gain and sensitivity analysis

In this section the non-idealities of the VD-DXCC are considered and their influence on the proposed filter circuits is analyzed. The frequency dependent non-ideal voltage (β), current (α) and transconductance transfer (γ/γ′) gains cause a slight change in the current and voltage signals during transfer leading to undesired response. Considering the effect of frequency dependent current and voltage transfer gains the V-I characteristics of VD-DXCC are modified as given below.

$$I_{ZP1} = I_{ZP2} = \alpha_P I_{XP} \quad (14)$$

$$I_{ZN1} = I_{ZN2} = \alpha_N I_{NP} \quad (15)$$

$$V_{XN} = -\beta_N V_W \quad (16)$$

$$V_{XP} = \beta_P V_W \quad (17)$$

$$\boldsymbol{I_{ZC+} = I_W = \gamma' g_1 (V_P - V_N)} \quad (18)$$

$$\boldsymbol{I_{ZC-} = -\gamma g_1 (V_P - V_N)} \quad (19)$$

Where α is the current transfer gain, β stands for voltage transfer gain and γ denotes the transconductance transfer gain. Ideally their values should be unity.

The transfer function, pole frequency and quality factor of the MISO filter considering the effect of non-ideal current and voltage gains are given in Equations (20-23).

$$V_{out} = \frac{S^2 C_1 C_2 R_1 R_2 V_3 - \alpha_N S C_2 R_1 V_1 + \gamma' \alpha_P g_1 R_2 V_2}{S^2 C_1 C_2 R_1 R_2 + \alpha_N \beta_N S C_2 R_1 + \gamma' \alpha_P \beta_P g_1 R_2} \quad (20)$$

$$I_{out} = \frac{(S^2 C_1 C_2 R_1 R_2 + \alpha_N \beta_N S C_2 R_1 + \gamma' \alpha_P \beta_P g_1 R_2) I_4 - \alpha_P \alpha_N \beta_P S C_2 R_2 I_2 + \alpha_P \beta_P S C_2 R_2 I_3 - \alpha_P (S^2 C_1 C_2 R_1 R_2 + \alpha_N \beta_N S C_2 R_1) I_1}{S^2 C_1 C_2 R_1 R_2 + \alpha_N \beta_N S C_2 R_1 + \gamma' \alpha_P \beta_P g_1 R_2} \quad (21)$$

$$\omega_o = \sqrt{\frac{\gamma' \alpha_P \beta_P g_1}{C_1 C_2 R_1}} \quad (22)$$

$$Q = R_2 \sqrt{\frac{\gamma' \alpha_P \beta_P g_1 C_1}{C_2 R_1}} \quad (23)$$

The non-ideal expressions for pole frequency and quality factor of the SIMO filter are presented in Equations (24-25).

$$\omega_o = \sqrt{\frac{\alpha_P \beta_P \gamma' g_m}{C_1 C_2 R_1}} \quad (24)$$

$$Q = R_2 \sqrt{\frac{\alpha_P \beta_P \gamma' g_m C_1}{C_2 R_1}} \quad (25)$$

The sensitivities of ω_o and Q with respect to the non-ideal gain and passive elements are given below. The Equations (26-28) give sensitivities of MISO filter and Equations (29-31) give sensitivities of SIMO filter. The sensitivities are not more than one which is desired.

$$-S_{C_1}^{\omega} = -S_{C_2}^{\omega} = -S_{R_1}^{\omega} = S_{\gamma'}^{\omega} = S_{g_1}^{\omega} = S_{\alpha_P}^{\omega} = S_{\beta_P}^{\omega} = \frac{1}{2} \quad (26)$$

$$-S_{C_1}^{Q} = -S_{R_1}^{\omega} = S_{C_2}^{Q} = -S_{R_2}^{Q} = S_{g_1}^{Q} = S_{\alpha_P}^{Q} = S_{\beta_P}^{Q} = S_{\gamma'}^{Q} = \frac{1}{2} \quad (27)$$

$$S_{R_2}^{Q} = 1 \quad (28)$$

$$-S_{C_1}^{\omega} = -S_{C_2}^{\omega} = -S_{R_1}^{\omega} = S_{\gamma'}^{\omega} = S_{\beta_P}^{\omega} = S_{g_1}^{\omega} = S_{\alpha_P}^{\omega} = \frac{1}{2} \quad (29)$$

$$S_{C_2}^{Q} = -S_{C_1}^{Q} = S_{\alpha_P}^{Q} = -S_{R_1}^{\omega} = S_{\gamma'}^{Q} = S_{\beta_P}^{Q} = S_{g_1}^{\omega} = \frac{1}{2} \quad (30)$$

$$S_{R_2}^{Q} = 1 \quad (31)$$

6 Simulation results

To validate the proposed designs the VD-DXCC is designed in 0.18µm PDK from Silterra Malaysia. The complete layout of the VD-DXCC is designed and the post layout results are discussed. The transistors width and length used are presented in Table 4. The circuits are simulated at a supply voltage of V_{DD} = -V_{SS} = 1.25V. The transconductance of OTA is fixed at g_m = 903.92µS by selecting bias current of OTA, I_B = 100µA. The current and voltage transfer gains are found to be (α=0.976 and β=0.982).

Table 4: Width and length of the transistors

Transistor	Width (W µm)	Length(L µm)
M1- M2	1.4	0.7
M3- M5	2.8	0.7
M6- M7	2.4	0.7
M8- M10	4.8	0.7
M11-M24	9.6	0.7
M25-M36	2	1

The dual mode filter is validated by designing it for a frequency of 2.704 MHz in voltage mode of operation. The passive elements are selected as R_1 = 4kΩ, R_2 = 4kΩ, C_1 = 20pF, C_2 = 20pF and I_{Bias} = 20uA. The ideal and post

layout response of the filter is shown in Figures 6-7. The simulated pole frequency of the filter is found to be 2.7959 MHz which translates into 3.4% error. To examine the signal processing capability of the filter transient analysis is performed for band pass configuration. A sinusoidal signal of 100mV amplitude and 2.704 MHz frequency is given at the input and the output is noted. It can be deduced from Figure 8 that the filter functions well.

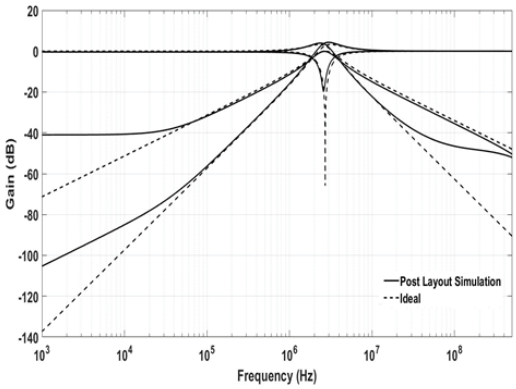

Figure 6: Frequency response of VM Filter

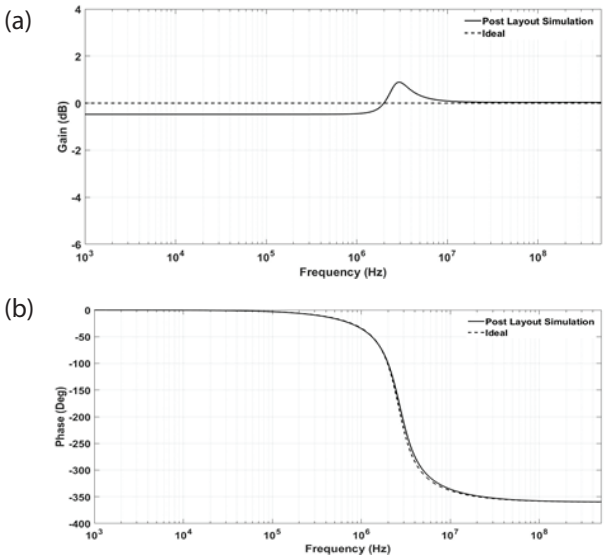

Figure 7: Frequency response of VM AP Filter

The tunability feature of the filter is verified. First, the filtering frequency is varied by changing the bias current of the VD-DXCC as shown in Figure 9. Second, the quality factor is varied by changing the value of the resistor R_2 as presented in Figure 10. It can be seen that the frequency and quality factor of the filter can be independently controlled. The power dissipation of the filter for VM is found to be 2.237mW.

To study the effect of process variation on the proposed filter Monte Carlo analysis is carried out for 10% variation in capacitors (C_1&C_2) values for the AP response.

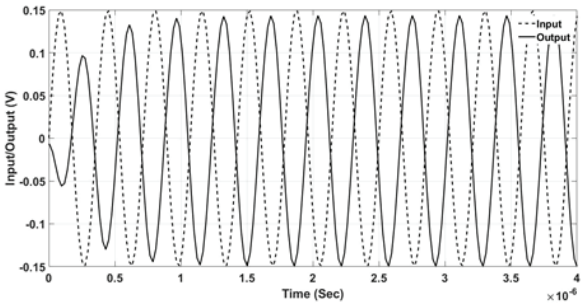

Figure 8: Transient analysis of BP filter

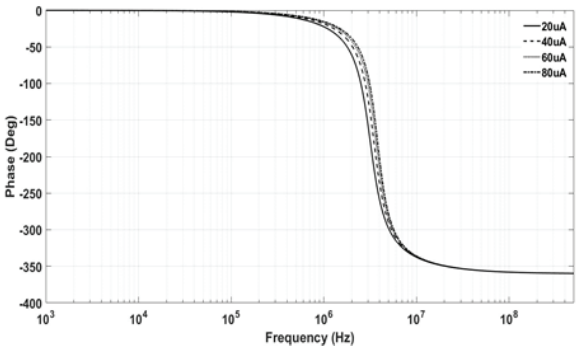

Figure 9: Frequency response tunability of VM Filter

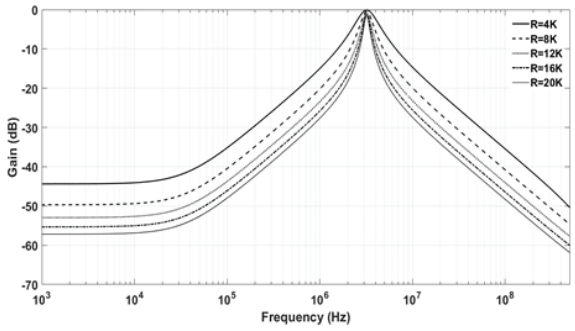

Figure 10: Quality factor tunability of VM Filter

The analysis is done for 200 runs and the results are presented in Figures 11-12. To further examine the filter the Monte Carlo analysis is done for 10% variation in capacitor (C_1&C_2) and resistors (R_1&R_2) values for 200 runs for HP response. The results are presented in Figures 13-14. The analysis results indicate that the filter performs well and requires no matching of passive elements.

Now the CM mode operation in MISO configuration is investigated. The filter is designed for a frequency of 5.408 MHz. The passive elements are selected as R_1 = 4kΩ, R_2 = 4kΩ, C_1 = 10pF, C_2 = 10pF and I_{Bias} = 20uA. The response of the filter is shown in Figures 15. The quality factor tunability is also tested for different values of the resistor *R2* as presented in Figure 16. It can be inferred

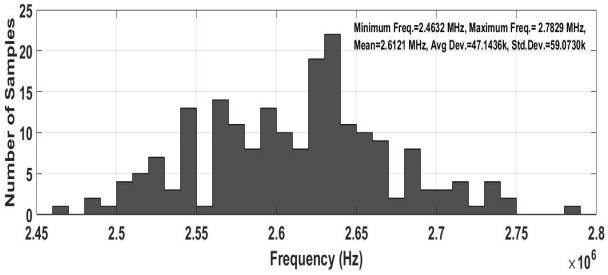

Figure 11: The Monte Carlo analysis results for AP response

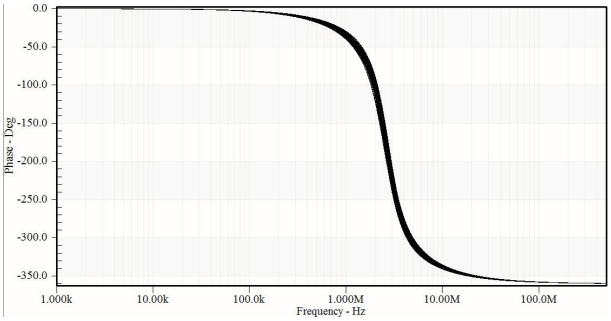

Figure 12: The Monte Carlo analysis results for AP phase

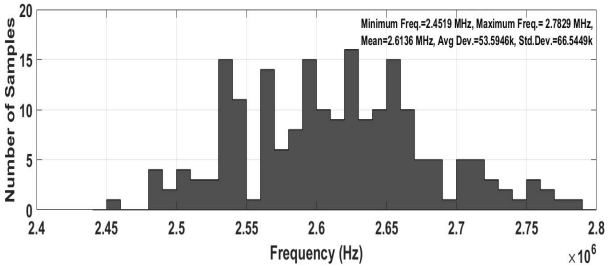

Figure 13: The Monte Carlo analysis results for HP response

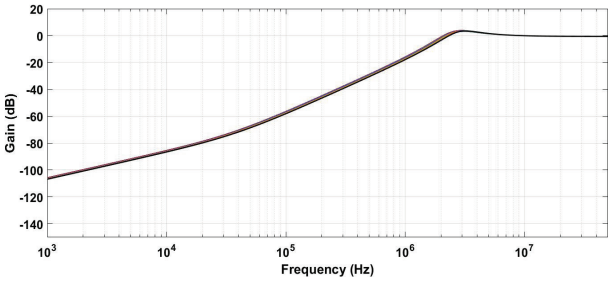

Figure 14: The Monte Carlo analysis results for HP response

from the figure that the quality factor can be tuned independent of the frequency. The transient analysis result for BP configuration are also presented in Figure 17 which further testifies the accurate signal processing capability of the filter structure.

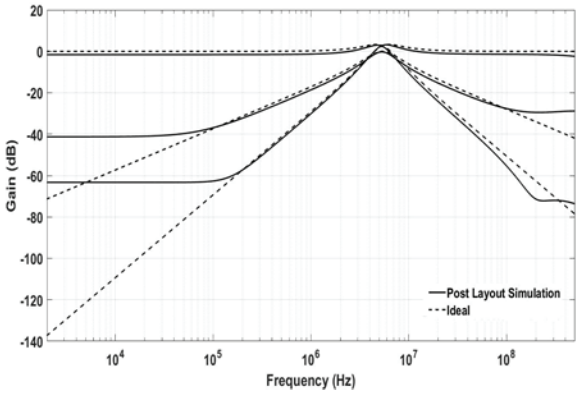

Figure 15: Frequency response of CM SIMO Filter

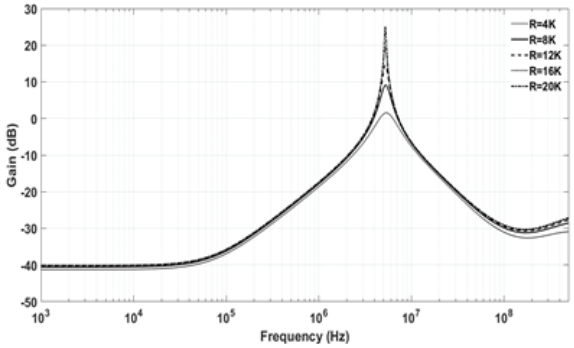

Figure 16: Quality factor tunability of CM SIMO Filter

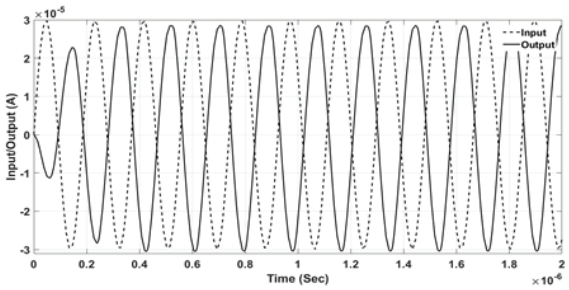

Figure 17: Transient analysis of BP SIMO filter configuration

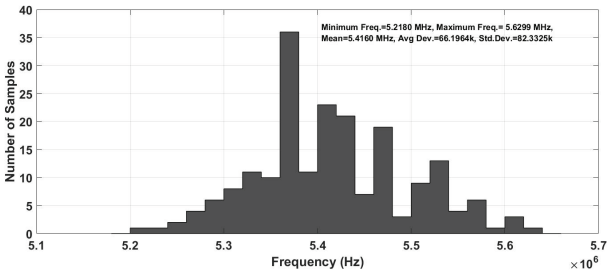

Figure 18: The Monte Carlo analysis results for BP response

The Monte Carlo analysis is carried out for the CM SIMO filter for 10% variation in resistors (R_1&R_2) values

for BP response. The analysis is done for 200 runs and the results are presented in Figures 18-19. Additionally, Monte Carlo analysis is also done for 10% variation in capacitors (C_1&C_2) values. The results are given in Figure 20. It can be inferred from the analysis results that the filter does not require an passive components matching constraints.

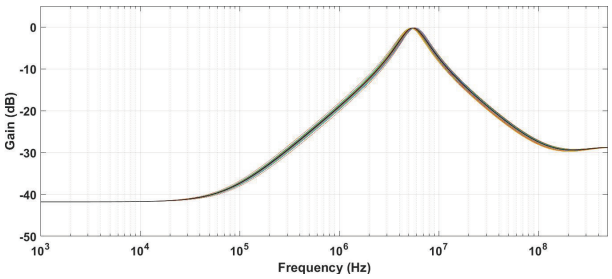

Figure 19: The Monte Carlo analysis results BP response

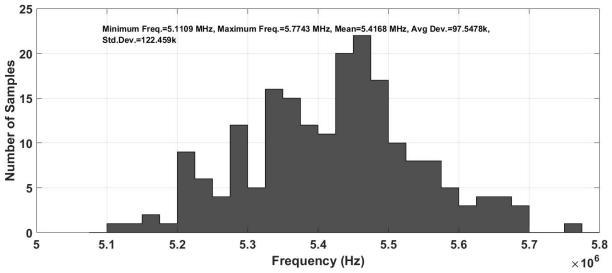

Figure 20: The Monte Carlo analysis results for BP filter response

7 Acknowledgement

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8 Conclusion

In this research, a newly proposed ABB the VD-DXCC is employed in designing a novel dual mode filter capable of working in MISO (VM, CM) and SIMO (CM) configurations. The developed filter did not require any passive components matching condition (except in SIMO CM configuration) for realizing filter responses. The pole frequency and quality factor of the proposed filter can be tuned independently. The non-ideal and sensitivity analysis are also carried out for the filter circuit to study the effect of the process variations. The post layout simulations are in close agreement with the theoretical analysis.

9 Reference

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Protective Alumina Coatings Prepared by Aerosol Deposition on Magnetocaloric Gadolinium Elements

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Abstract: In this work the preparation of a protective insulating alumina coating on magnetocaloric gadolinium elements was investigated. In order to prepare a dense ceramic coating at room temperature the aerosol deposition technique was used. The study reveals that the powder morphology and particle size are important parameters that influence the deposition efficiency, powder packing and consequently also the density and functional properties of the alumina coating. The optimal powder pre-deposition treatment includes heating the powder to 1150 °C, followed by milling. The deposition of this powder resulted in the preparation of dense alumina coatings with a low specific electrical conductivity of $6.4 \cdot 10^{-14}\ \Omega^{-1}m^{-1}$.

Keywords: protective alumina coating, aerosol deposition, magnetocaloric gadolinium

Korundna zaščita magnetokaloričnih hladilnih elementov pripravljena z metodo nanašanja delcev v curku aerosola

Izvleček: V članku smo preučevali pripravo zaščitnih korundnih prevlek za magnetokalorične hladilne elemente iz gadolinija. Prevleke smo pripravili z metodo za nanašanje delcev v curku aerosola, ki omogoča pripravo gostih prevlek že pri sobni temperaturi. Ugotovili smo, da morfologija prahu in velikost delcev pomembno vplivata na učinkovitost nanosa in pakiranje prahu ter posledično tudi na gostoto in funkcionalne lastnosti prevlek. Optimalni postopek obdelave prahu pred nanašanjem vključuje termično obdelavo prahu pri 1150 °C ter mletje v planetarnem mlinu. Iz predhodno obdelanega prahu je mogoče pripraviti goste korundne prevleke z nizko specifično električno prevodnostjo, ki znaša $6.4 \cdot 10^{-14}\ \Omega^{-1}m^{-1}$.

Ključne besede: korundne zaščitne prevleke, nanašanje delcev v curku aerosola, magnetokalorični gadolinij

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1 Introduction

Magnetocaloric (MC) refrigeration technology is gaining importance as it represents an alternative to conventional vapor-compression technology for specific applications [1,2]. One of the best candidates for a MC material operating at around room temperature is gadolinium, with an adiabatic temperature change of ΔT_{ad} ~ 12 K for a magnetic field change of 5 T at a temperature of 294 K [3].

Many of the MC refrigeration prototypes are based on the principle of active magnetic regeneration. This principle is suitable for implementing in large refrigeration devices, where also an efficient heat-exchange system is needed [2]. The heat-exchange media are typically water or water-based fluids, which can cause the gadolinium working elements to corrode [4].

Caloric research is also developing towards the use of MC cooling technology in electronics. In this case, for the

efficient transfer of heat, more sophisticated heat-management systems are needed, such as thermal switches or thermal diodes [5,6]. One way to activate these thermal switches is by using an electric field, which can be detrimental for the working elements. In addition to problems with the oxidation of gadolinium, new challenges appear regarding the protection of the gadolinium elements against possible electrical breakdown. These problems can be solved by the deposition of a protective layer on the top of the gadolinium element.

Polycrystalline aluminum oxide (Al_2O_3), more often referred as alumina, is an abundant and one of the most widely used ceramic materials. Alumina is used in versatile applications due to its excellent properties, e.g., high electrical insulation, heat resistance, chemical inertness and high mechanical hardness. Those properties make alumina one of the best materials for protecting materials against harsh environments [7–10]. In order to deposit a protective alumina layer on gadolinium metal an aerosol deposition (AD) method can be used.

AD is a spray-coating process for producing dense thick films, where the deposition mechanism is based on the collision of fine particles with the substrate's surface. A powder is mixed with a carrier gas to form an aerosol, which is then ejected through a nozzle and deposited onto the substrate under vacuum [11,12]. The AD process occurs at room temperature; thus this method makes it possible to combine materials that are normally not stable or compatible at high temperatures. Aerosol-deposited alumina thick films exhibit excellent corrosion resistance [13] and electrical insulation [14]. For example, they have a high electrical breakdown strength, exceeding 600 $kV \cdot cm^{-1}$ [14,15]. These films can also be used as anti-scratch and anti-smudge coatings due to their promising mechanical properties [12]. The high hardness of AD alumina films (between 1100 HV and 1800 HV [13,16–18]), which is comparable with the hardness of bulk alumina, and a good adhesive strength of 64 MPa [19] were reported.

In this work the AD of a protective alumina coating on gadolinium cooling elements was investigated. The properties of the alumina powder are of high importance for efficient deposition and good particle packing. Therefore, special attention was given to the pre-deposition treatment of the starting powder in order to prepare a dense insulating protection layer.

2 Materials and Methods

For AD a raw Al_2O_3 commercial powder AL-160SG3, Showa Denko, Japan (further denoted as the R powder) and its two modifications; heated (H) powder as well as heated and milled (HM) powder were used. The H and HM powders were thermally treated in a chamber furnace (Custom-made, Terna, Slovenia) at 1150 °C for 1 h (with 5 $K \cdot min^{-1}$ heating and cooling rates). These annealing conditions were chosen based on the sintering curve of pressed Al_2O_3 pellets at the point where the densification starts (1150 °C). The HM powder was after annealing milled in a planetary mill (PM400, Retsch, Germany) at 200 min^{-1} for 1 h using yttria-stabilized-zirconia milling balls in iso-propanol as a liquid medium. The particle size distribution of the powders was determined by using a light-scattering granulometer (S3500, Microtrac, USA).

The aerosol deposition equipment was provided by Invertech, Germany. The commercial gadolinium substrates (Metall Rare Earth Limited, Hong Kong) were used. A scheme of the AD apparatus is shown in Figure 1. The process parameters during the AD were kept the same for the deposition of all three powders (shown in Table 1).

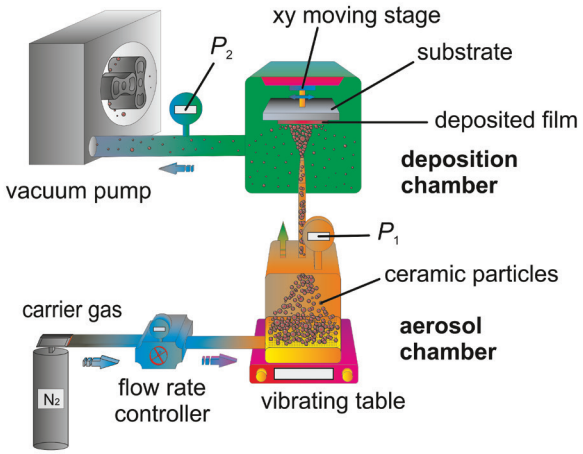

Figure 1: Scheme of the AD apparatus.

Table 1: Process parameters used during the AD.

Process parameters	
P_1	150–250 mbar
P_2	0.2–0.5 mbar
Nozzle geometry (slit size)	(0.5 · 10) mm^2
Carrier gas species	N_2
Gas flow rate	4 $L \cdot min^{-1}$
Distance between nozzle and substrate	5 mm
Sweep speed	5 $mm \cdot s^{-1}$

The thickness and root-mean-square roughness (R_q) of the prepared layers were evaluated from line profiles

measured with a contact profilometer (DektakXT, Bruker, USA) by using the software Vision64 (Bruker, USA). The thickness was evaluated from the step height of the film after curvature removal using a quartic polynomial. R_q was evaluated from the roughness profile obtained after filtering the total profile using Gaussian regression (cut off 0.08 mm).

The alumina powders and thick films were microstructurally analyzed using a field-emission scanning electron microscope (FE-SEM, JSM 7600F, Jeol, Japan). The microstructural analyses of the thick films were made on polished cross-sections.

Prior to the electrical characterization, gold electrodes with a diameter of 1.5 mm were deposited on the top of the film's surface by magneton sputtering (Cinquepascal SRL, Italy). The current density–electric field (*J–E*) measurements were made using a Keithley 237 high-voltage-source measurement unit (Keithley Instruments, USA). Each sample was exposed to step-like voltages from negative to positive polarity in the range up to 150 kV·cm^{-1}. The whole measurement consisted of seven equal field steps. The specific direct current (DC) conductivity (σ_{DC}) was obtained at 150 kV·cm^{-1}, assuming Ohm's law.

3 Results

In order to evaluate the characteristics of all three powders used for the deposition experiment we first examined the particle size distribution. Figure 2 shows the particle size distributions (solid line) and the corresponding cumulative curves (dashed line). In the inset the d_{10}, d_{50} and d_{90} values for each powder are collected. According to the literature, the optimal particle size for the aerosol deposition of ceramic powders ranges between 0.2 µm and 2 µm [11,12]. In the R and HM powders, 90 vol% of the particles fit well in this range, while in the H powder the percentage of such particles is smaller (i.e., ~75 vol%). This indicates that the R and HM powders could exhibit better deposition characteristics in comparison to the H powder.

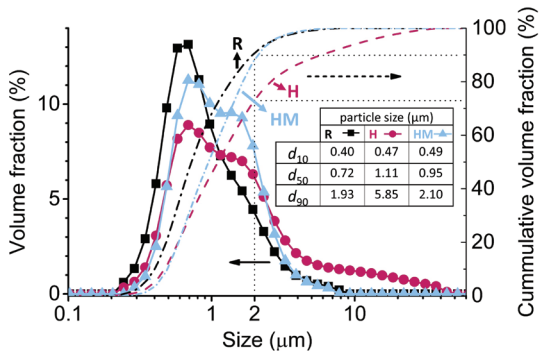

Figure 2: Particle size distributions (solid line) and the corresponding cumulative curves (dashed line) of R, H and HM powders. The d_{10}, d_{50} and d_{90} values of all three powders are presented in the inset table.

The FE-SEM micrographs of the powders are shown in Figure 3. By comparing the R and H powders, it is clear that in the R powder the particles are sharper and more irregularly shaped. The heat treatment causes particle coarsening in terms of merging the small agglomerated particles together and creating necks between them. After heating the particle surface appears smoother.

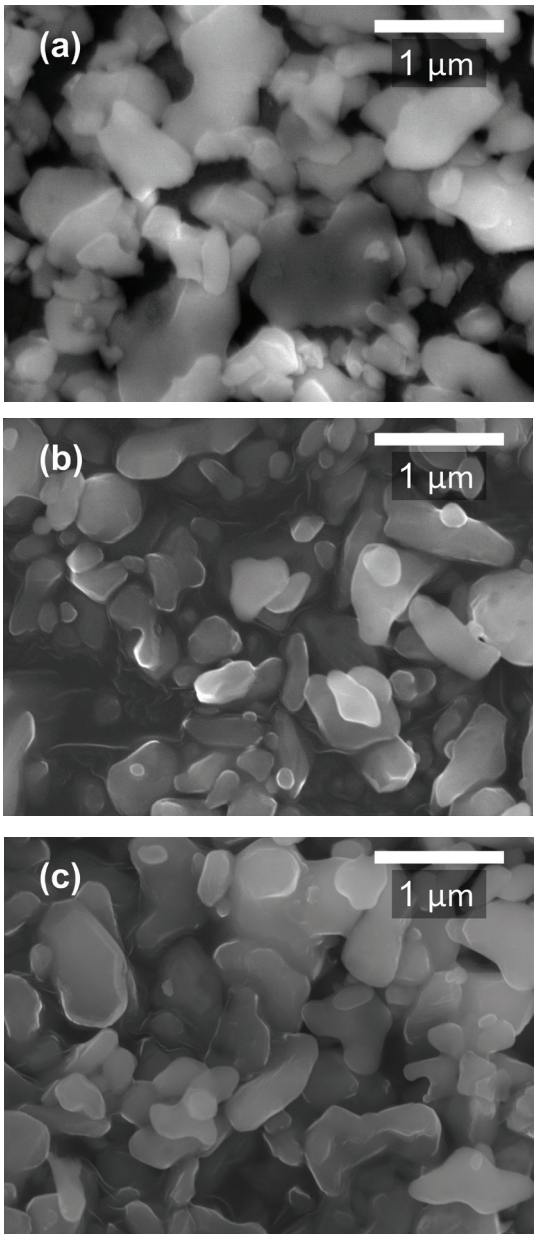

Figure 3: Secondary-electron FE-SEM images of (a) R, (b) H and (c) HM powders.

The additional milling treatment reduces the average particle size (HM powder). However, compared to the particles of R powder, the surface of the HM powder remains smooth and more uniform in size.

After the examination of the powder, all three types of powders were deposited on polished gadolinium elements. The line profiles of the films deposited on the substrates are shown in Figure 4. The H powder has the lowest deposition rate, which is reflected in the very small film thickness (~0.9 µm) and the high surface roughness (R_q ~0.2 µm). On the other hand, the R and HM powders were much more effectively deposited on the gadolinium element, resulting in films with thicknesses of 10.9 µm and 6.4 µm, respectively. Also, the roughness of both films was smaller (R_q ~0.1 µm) compared to the roughness of the film prepared from the H powder.

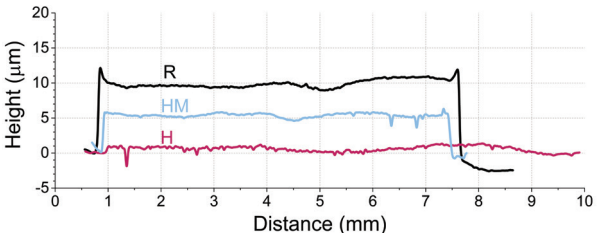

Figure 4: Line profiles of deposited alumina layers on gadolinium elements.

To investigate the electrical conductivity of alumina coatings, *J–E* measurements were performed at room temperature (Figure 5). The films prepared from the H powder (thickness <1 µm) were electrically conductive, and the leakage current was too high to perform the measurements. This enhanced conductivity is most probably the consequence of the non-uniform deposition of the H powder onto the gadolinium substrate

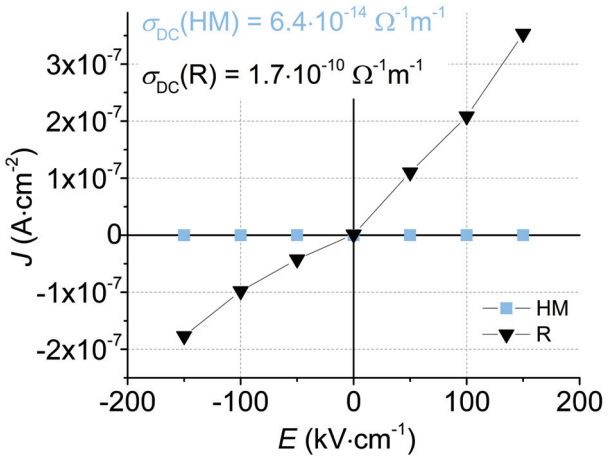

Figure 5: *J-E* curves and calculated σ_{DC} values of thick films prepared from R and HM powders.

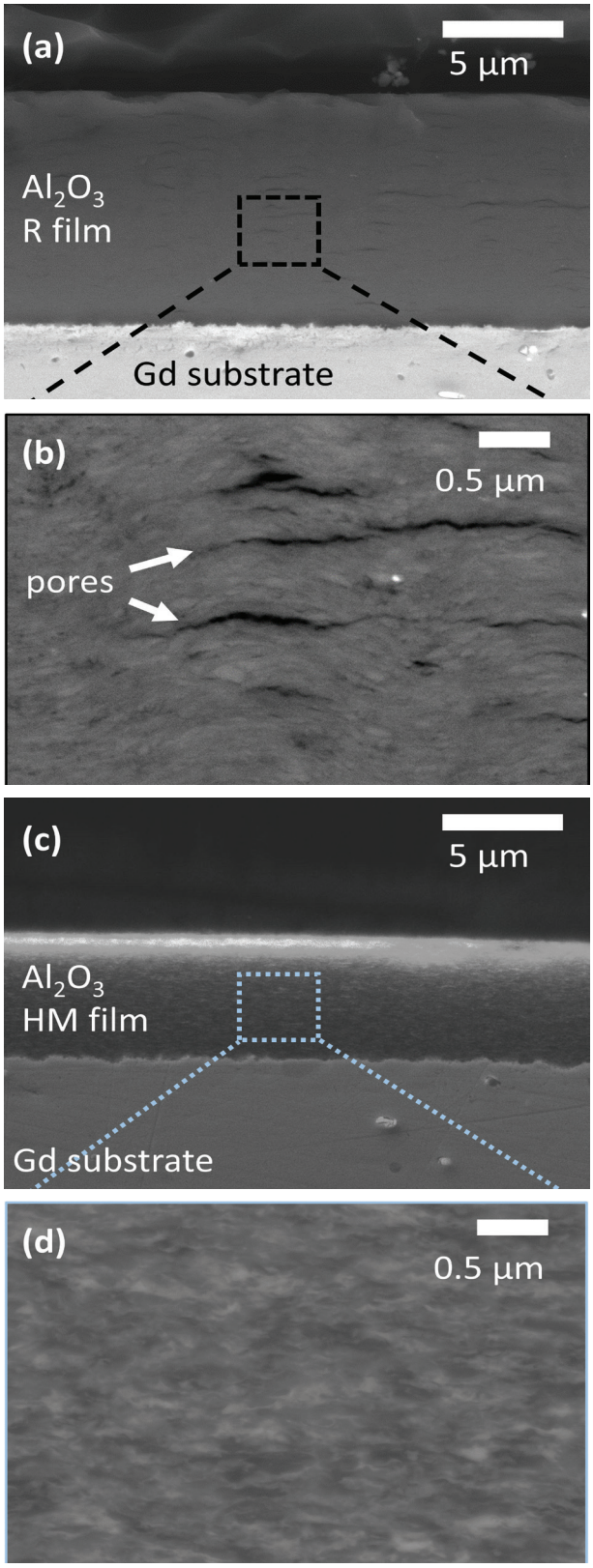

Figure 6: FE-SEM cross-sectional images of thick films prepared from (a,b) R and (c,d) HM powders. The micrographs in Figures (a,c) and (b,d) were taken with a secondary-electron and backscattered-electron detector, respectively.

(Figure 4). The lowest σ_{DC} was obtained in the films prepared from the HM powder, i.e., $6.4 \cdot 10^{-14}\ \Omega^{-1}m^{-1}$, which is comparable to the conductivity of the sintered bulk alumina [20]. The films prepared from the R powder possess a significantly (4 orders of magnitude) higher σ_{DC}, i.e., $1.7 \cdot 10^{-10}\ \Omega^{-1}m^{-1}$.

In order to understand why alumina coatings prepared from R powder are more conductive than those prepared from HM powder, the FE-SEM microstructural analyses of those films in cross-section were performed. The images of the R and HM films are shown in Figures 6 (a,b) and (c,d), respectively. Both the R and HM films exhibit good adhesion to the gadolinium substrate. In Figure 6 (a, c) a larger thickness of the R film in comparison to the HM film (in agreement with line profiles in Figure 4) is revealed, indicating better deposition rate of the R powder. Larger thickness of the layer can also lead to higher probability for defects in microstructures, which could lead to higher conductivity of the sample. Furthermore, a closer look of R film (Figure 6 (b)) reveals micro-sized pores elongated in the horizontal direction. Similar elongated pores were already reported in aerosol deposited alumina films [13]. Such microstructure is most probably the main reason for the high electrical conductivity of these films. On the other hand, the films prepared from the HM powder (Figure 6 (d)) are very dense and pore-free. This indicates better packing of the HM powder during the deposition, in comparison to the R powder, which could be related to the more smooth and uniform size of HM powder. The films prepared from the HM powder possess the lowest electrical conductivity and are therefore the most promising for the protection and electrical insulation of the magnetocaloric elements.

4 Summary and Conclusions

To summarize, the processing of alumina protective layers on magnetocaloric gadolinium elements was studied. The protective coating was prepared by the aerosol deposition technique, which enables the preparation of dense films at room temperature. In order to study the influence of powder size and morphology on the deposition rate, different pre-deposition treatments of the powders were used. The optimal powder treatment includes heating the powder to 1150 °C for 1 h and subsequent milling in a planetary mill. The deposition of such thermally treated and milled powder yielded a dense, few-micrometers-thick alumina protective layer with promising electrical insulation properties (a specific DC conductivity below $10^{-13}\ \Omega^{-1}m^{-1}$).

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6 Conflicts of Interest

The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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Modelling Supported Design of Light Management Structures in Ultra-Thin Cigs Photovoltaic Devices

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Abstract: Chalcopyrite solar cells exhibit one of the highest conversion efficiencies among thin-film solar cell technologies (> 23.3%), however a considerably thick absorber ≥1.8 µm is required for an efficient absorption of the long-wavelength light and collection of charge carriers. In order to minimize the material consumption and to accelerate the fabrication process, further thinning down of the absorber layer is important. Using a thin absorber layer results in a highly reduced photocurrent density and to compensate for it an effective light management needs to be introduced. Experimentally supported, advanced optical simulations in a PV module configuration, i.e. solar cell structure including the encapsulation and front glass are employed to design solutions to increase the short current density of devices with ultra-thin (500 nm) absorbers. In particular (i) highly reflective metal back reflector (BR), (ii) internal nano-textures and (iii) external textures by applying a light management (LM) foil are investigated by simulations. Experimental verification of simulation results is presented for the external texture case. In the scope of this contribution we show that any individual aforementioned approach is not sufficient to compensate for the short circuit current drop of the thin CIGS, but only a combination of highly reflective back contact and introduction of textures (internal or external) is able to compensate and also to exceed (by more than 5 % for internal texture) photocurrent density of a thick (1800 nm) CIGS absorber.

Keywords: ultra-thin CIGS solar cells, light management, textured interfaces, optical modelling

Načrtovanje struktur za upravljanje svetlobe v izredno tankih CIGS fotonapetostnih strukturah z uporabo modeliranja

Izvleček: Sončne celice na osnovi Cu(In, Ga)Se2 dosegajo relativno visoke učinkovitosti pretvorbe (> 23,3%) v primerjavi z drugimi tankoplastnimi tehnologijami sončnih celic. Za učinkovito absorpcijo dolgovalovne svetlobe potrebujemo ≥ 1800 nm debelo absorpcijsko plast Cu(In, Ga)Se2. Z namenom zmanjšanja porabe materiala (predvsem In) in pohitritve nanosa absorpcijske plasti poskušamo najti rešitve, ki bi omogočile uporabo tanjših plasti, hkrati pa zagotovile primerljive učinkovitosti pretvorbe, ki jih dosežemo s standardnimi debelinami. Stanjšanje absorpcijske plasti samo po sebi vodi k zmanjšanju fototoka (zaradi nepopolne absorpcije dolgovalovne svetlobe), kar narekuje uporabo posebnih tehnik upravljanja svetlobe znotraj sončne celice. V tem prispevku z uporabo optičnih simulacij raziščemo potencial izbranih tehnik izboljšanja ujetja svetlobe in s tem povečanja absorpcije v strukturi s 500 nm debelo absorpcijsko plastjo. S simulacijami raziščemo učinke (i) visokoodbojnih zadnjih kovinskih odbojnikov, (ii) nanotekstur, prenešenih v celico preko hrapave površine substrata in (iii) zunanjih mikrotekstur, izdelanih na folijah na sprednjem steklu. Slednje ovrednotimo tudi na osnovi eksperimentalnih rezultatov. Rezultati simulacij pokažejo, da za ohranjanje fototoka prvotne celice z debelo plastjo, v tanki celici potrebujemo visokoodbojni zadnji odbojnik (na primer srebro), v kombinaciji z notranjimi ali zunanjimi teksturami. Z delno optimizacijo struktur lahko na celici s 500 nm debelo absorpcijsko plastjo celo presežemo fototok celice s 1800 nm debelo plastjo.

Ključne besede: zelo tanke sončne celice CIGS, upravljanje svetlobe, hrapavi spoji, optično modeliranje

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1 Introduction

Among thin film solar cell technologies, one of the highest efficiencies are achieved by a direct bandgap semiconductor Cu(In, Ga)Se_2 (CIGS), with a current record of 23.35% on the cell level [1]. CIGS exhibits high absorption but a fairly thick absorber (~2-3 µm) needs to be used. As CIGS alloys consist of scarce materials, especially indium and gallium [2, 3] the minimization of material consumption by reducing the thickness of the CIGS absorber layer is of high interest [4, 5]. Besides reduced material usage faster throughput in CIGS deposition process is achieved. By thinning down the CIGS absorber from 1800 nm to 500 nm we expect the reduction of corresponding bill of material (BOM) costs from 31 USD/module to 27 USD/module, including an increased cost of the back contact (reflector) to maintain the conversion efficiency at the same level.

The usage of ultra-thin CIGS absorber layers ($d_{CIGS} \leq 500$ nm) comes with two main drawbacks. First is reduced short-circuit current density (Jsc) due to insufficiently absorbed long-wavelength light in the thin absorber. Second, open circuit voltage (Voc) and fill factor (FF) are affected. This is because in thinner CIGS cells, absorption of light takes place closer to the back contact, increasing the concentration of majority (holes) and minority (electron) carriers, thus, more carriers are exposed to surface defects at the back contact interface. Threreby recombination of charge carriers is increased compared to cells with thick CIGS absorber layers. Additionally, if texturing is introduced to improve light trapping, the surface area becomes larger and may lead to additional recombination.

Thin passivation layers (e.g. Al_2O_3) have already been successfully used at the rear Mo/CIGS interface to reduce surface recombination [6–9]. On the other hand, to compensate for reduced photocurrent density due to reduced thickness, an additional treatment to increase light absorption in the thin absorber needs to be introduced. Proposed solutions are well summarized in a review paper by Schmidt [10], and include improving front transparent contacts, using alternative window layers, implementing anti-reflecting structures, inclusion of efficient back reflectors, introduction of textures and nano-particles to induce light scattering and other.

In this contribution we focus on improving light absorption in ultra-thin ($d_{CIGS} \leq 500$ nm) CIGS absorbers by means of numerical simulations. The optimization is carried out on simplified photovoltaic (PV) module structures where front glass and encapsulation foil (Ethyl Vinyl Acetate - EVA) are considered to form one incoherent thick layer on top of the solar cell in simulations. This simplification is based on low difference in refractive indices of EVA and glass.

Using simulations, we deduce that the main optical losses in the thin film structure are reduced absorption at longer wavelengths in CIGS layer and high absorption losses in the Mo back reflector. To improve the photocurrent density, we introduce (i) a highly reflective metal material - Ag as an alternative back reflector (BR), (ii) texturization on back (nano-textured BR) and front (micro-textures on top of encapsulation) side of the cell and (iii) a combination of both approaches. An additional thin Al_2O_3 layer on top of the metal BR is used both as a passivation of the CIGS rear surface and as a diffusion barrier for metals, preventing their diffusion into the CIGS layer during the evaporation process.

We show that only an alternative BR or only texturization is not sufficient to compensate for reduced photocurrent density when thinning down the absorber thickness from standard 1800 nm to 500 nm. Combination of both, thus texturization (at front or back) and alternative BR needs to be employed in thin absorber devices to reach and even surpass standard thick devices.

2 Modelling and Simulations

Structures with flat and nanotextured interfaces were simulated with three-dimensional simulator Comsol Multiphysics [11], which uses Finite Element Method (FEM) to solve the Maxwell equations. FEM enables modelling of the exact morphology of (periodic) nanotextured interfaces in three dimensional structures. Such rigorous analysis in combination with realistic complex refractive indices of materials [12] enables to include various effects in simulation, such as light scattering and anti-reflection due to nanotexturing, as well as plasmonic absorption that can occur at textured metallic surfaces. However, it only considers coherent propagation of light in thin layers. Therefore, for the thick protection glass and encapsulation foil, we use a previously developed method that extends the applicability of the FEM method also to treatment of thick low absorbing incoherent layers [13]. By adding more incoherent layers, however, the computation time increases, since FEM simulation has to be carried out more times.

A combined wave optics / ray tracing simulator CROWM [14] was used when larger textures with features from several µm to mm, like the texture of the light management (LM) foil, are modeled. Using CROWM an entire PV module with included LM foil is modelled. Here, adding more incoherent layers is not a problem, however, due to the reason of comparison we kept the

encapsulation stack as one layer as in the case of FEM simulations. In CROWM thin coherent layers of the solar cell are simulated using a transfer matrix method and are combined with full three-dimensional ray tracing in micro-textured incoherent layers.

Presented models are used to simulate wavelength-dependent reflectance and absorptance of individual layers. As lateral dimensions of the structures are expected to be much larger than vertical ones, edge effects in simulations are neglected (but are possible to be included). All models were calibrated according to the literature [12] and measurement results – see Section 5.

Main external solar cell parameters, like *EQE* and J_{sc}, which are directly linked to optical behavior of solar cells, are determined by considering an ideal extraction of charge carriers from the CIGS absorber by assuming low level of bulk and surface recombination. Bulk recombination can be minimized by high quality CIGS material obtained by a co-evaporation process and surface recombination can be minimized by using an efficient surface passivation layer [6], like Al_2O_3. In the simulations, contributions of generated carriers from the CdS layer were neglected [15]. Thus, external quantum efficiency (*EQE*) is matched with wavelength dependent absorptance in the CIGS layer (EQE_{opt}). The short circuit density (J_{sc}) is then calculated by integrating the product of the AM1.5g solar spectrum and the EQE_{opt} across all wavelengths of the solar spectrum.

3 Device structure and textures

A schematic cross-section of a CIGS solar cell with included front encapsulation and rear Al_2O_3 passivation layer is presented in Figure 1(a). Solar cell layers are deposited on a soda lime glass (SLG) substrate in the following order: an opaque Mo layer (~ 400 nm) serving as an electrical contact and a BR in the basic case. This is followed by an optional alternative BR and an Al_2O_3 passivation layer. Next, we have an absorbing CIGS layer followed by a CdS, ZnO and ZnO:Al. In the case of a Mo back contact, a thin (5 nm) interfacial layer ($MoSe_2$) is formed during deposition of the CIGS [16], resulting in a decreased reflectance of an ideal CIGS/Mo interface by about 20-25% [17]. Passivation Al_2O_3 layers also serve as protective layers to prevent diffusion of metals into CIGS during deposition. As Al_2O_3 is a non-conducting material, electrical contact is provided by an array of holes – point contacts in the Al_2O_3 layer [6–9]. Dimensions of these holes are sufficiently small (diameter 100~200 nm, with pitch of 1~2 μm), as compared to the wavelength of light and thus do not contribute any significant amount to the optical effects and can thus be neglected in our optical simulations. Small dimensions and low density of the holes is also important from the point of view of the BR (Ag) material diffusion through the holes into CIGS, which can deteriorate the cell electrical performance. To minimize this effect thin Ag layer under these openings can be etched away and Mo takes the role of the local contact point. An alternative to prevent Ag diffusion into CIGS is to use TCO layer as Ag cover [18]. TCO layers (e.g. indium tin oxide) can bring some additional parasitic losses, but works as a diffusion barrier. Anyway, in this work we check optical benefits of the concept with a patterned thin Al_2O_3 layer, assuming to provide high quality passivation and sufficient diffusion barrier for Ag.

Finally, the cell is finished with an encapsulation consisting of two optically thick layers - EVA and glass (both are in mm range). In simulations both layers, EVA and glass, are considered as a single layer, due to good matching in refractive indices of both materials. Presented structure serves as a base model for all further simulations, with thicknesses and basic structure kept constant for all simulations.

To improve optical performance of thin CIGS, in addition to alternative highly reflective BR, we also introduce internal nano-textures and external micro-textures (LM foil) in simulations. The position of the internal and external textures can be seen in Figure 1(a), while its shape and size can be seen in Figure 1(b) and (c), respectively.

In our previous work, a detailed optical analysis of different internal textures introduced at the rear side of the device was performed [12], thus here we only use an optimal texture in our analysis. We selected a periodic two-dimensional, sine-like nano-texture with P = 800 nm and h = 300 nm (see inset of Figure 1(b)), that can be fabricated on silicon or glass master by e-beam or etching techniques [19]. Applicability, with UV nanoimprint lithography makes these textures viable for low-cost, industrial scale production. Sine-like shape of nano-texture is also beneficial as it exhibits a smooth surface without any abrupt changes, reducing the risk of creating defects in the structure. Moreover, sine-like textures showed good results also in other solar cell technologies, like thin c-Si [20] and perovskite-silicon tandems [21]. Deposition of thin film layers on top of the nano-textures transfers the textured shape of the BR to the front side of the thin-film stack. As the layer growth is non-conformal, with a combination of isotropic and conformal growth, in our specific case the ratio of 0.3 (for details on layer growth see [22, 23], this results in changes in interface morphology as can be observed in Figure 1(b).

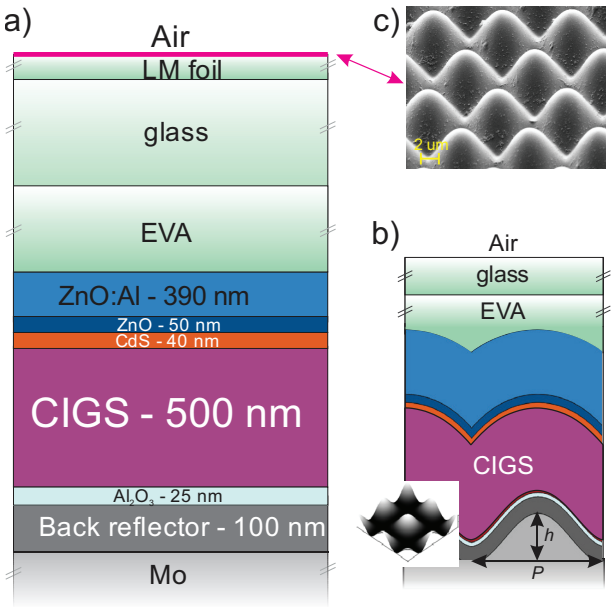

Figure 1: (a) A schematic cross-section of the CIGS PV module structure, (b) Cross-section of the structure with internal texture and non-conformal layer growth considered, (c) A Scanning electron microscopy image of hexagonal array of dome shaped micro-texture applied to the LM foil on top of front glass.

Alternative to texturing the BR, we can also apply texture on the front interface. We introduce a LM foil (lacquer or PDMS material) on top of the cell (at the air / encapsulation interface) on which the texture is realized (e.g. via embossing); by this we keep all other interfaces flat. In this work we focused on a standard commercially available hexagonal array of O shaped domes, with period $P = 7.38$ µm and height $h = 5.5$ µm see Figure 1(c). These structures already show potential for increasing J_{sc} in other solar cell technologies [24–27]. The LM foil is implemented on top of the encapsulation and is in simulations considered as a part of the encapsulation. This is reasonable, as refractive indices of the foil and the glass (also EVA) are sufficiently close together (n = 1.35 – 1.5), thus can be treated as a single layer. This was confirmed by additional simulations where all three incoherent layers were treated separately as a three layer stack. In simulations of the structure with the LM foil with micro-sized texture ray optics in combination with thin-film optics (CROWM simulator) was used.

4 Results and discussion

To identify main optical losses when thinning down the CIGS absorber layer, we simulate a module with a thin (d_{CIGS} = 500 nm) and a standard thick (d_{CIGS} = 1800 nm) CIGS absorber. Comparison of EQE_{opt} and parasitic absorptions in BR (see Figure 2) reveals two main loss mechanisms occurring when thinning down the absorber layer. Due to thinner absorber layer, highly reduced absorption of long-wavelength light, starting already at 550 nm can be observed. Secondly, as more light reaches the BR (less light is absorbed in the absorber) we can notice highly increased absorption losses in the Mo + $MoSe_2$ BR – see Figure 2. On the other hand, reflection and parasitic absorption losses in other layers remain almost unaffected between thin and thick absorbers. Optical losses altogether result in a highly reduced short circuit current of 28.31 mA/cm^2 of the thin module, compared to the 33.04 mA/cm^2 of the standard thick one, which is more than a 14 % decrease.

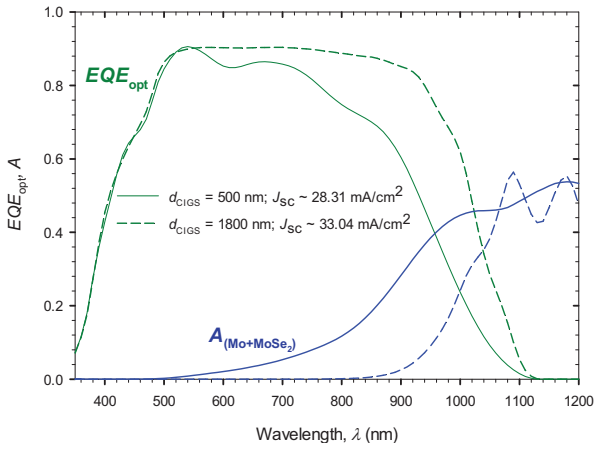

Figure 2: EQE_{opt} (A_{CIGS}) and BR absorption in standard thin (d_{CIGS} = 500 nm) and thick (d_{CIGS} = 1800 nm) CIGS module.

Both main loss mechanisms of thin devices are addressed in this contribution. First, we propose to replace the highly absorbing, poorly reflecting BR ($MoSe_2$/Mo) with alternative highly reflective metal BR, reducing absorption losses. To enhance absorption of long wavelength light, we propose texturization either on front or back side of the device, by which we can induce light scattering, light trapping and also anti-reflection properties, which if properly designed elongate the light path through the absorber, enabling also the long wavelength light to be absorbed.

4.1 Alternative BR

As a reference point, we simulate a thin device with a standard Mo BR, which results in a low J_{sc} = 28.17 mA/cm^2. When introducing an alternative metal-based BR, an additional Al_2O_3 passivation layer is also added to prevent diffusion of metals into the absorber during high temperature CIGS deposition. Adding Al_2O_3 to the existing Mo already increases the J_{sc} to 28.86 mA/cm^2, although not due to the increased reflection, but

due to reduced parasitic absorption losses enabled by the absence of the interfacial $MoSe_2$ layer. Using a highly reflective metal BR results in higher J_{sc}, due to highly reduced absorption losses in the BR. Using an Ag BR resulted in J_{sc} = 30.85 mA/cm^2 - see Figure 3. Data show that for a more reflecting BR, a higher gain in J_{sc} is achievable. However, although a high J_{sc} of 30.85 mA/cm^2 was achieved, it is still lower than the one of the standard thick device. An additional optical treatment is necessary to reach the J_{sc} of the thick device.

4.2 Internal textures

To additionally improve the J_{sc} of the thin CIGS solar cells, we introduce texturization of the BR in simulations. Nanotextures in general induce scattering of light which may improve light trapping inside the CIGS absorber and due to transfer of texture from the textured substrate to the front side (see Figure 1(b)) may also act as an antireflection structure at the front interfaces. The textures can be introduced in the structure of CIGS device e.g. by applying textured substrate. Using 3D FEM simulations, we simulated a PV module device with presented periodic internal sine-like nanotexture (see Figure 1(b)).

Simulations have been performed for the structures with different BR, namely $MoSe_2$/Mo – as a base example, Al_2O_3/Mo and Al_2O_3/Ag. The general observation is that texturizing helps to improve J_{sc} towards the device without the texturization in all cases – see Figure 3. Additionally, we can notice that high J_{sc} is achieved with a highly reflecting Ag BR. The main gain this time is due to the enhanced CIGS absorption in the long wavelength regime. By introducing optimized texturing, the optical path through the absorber is elongated, due to scattering and light trapping, thus additional light with longer wavelengths can be absorbed, contributing to higher J_{sc}. Here the highest J_{sc} of 34.75 mA/cm^2 is achieved with the Ag BR surpassed the J_{sc} of thick CIGS absorber by 5.1 %.

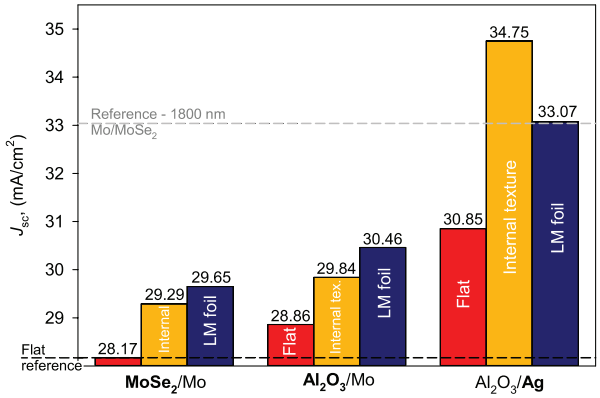

Figure 3: Comparison of simulated J_{sc} for CIGS PV modules without textures - flat (red bars), with internal textures (yellow bars) and with external textures (blue bars) on different BR.

On the other hand, using a Mo BR, the increase in J_{sc} is much lower, and with a J_{sc} of 31.16 mA/cm^2 we are more than 5.7 % below J_{sc} of the thick absorber. Additionally, results show that contribution of a textured Mo BR is lower compared to only replacing Mo with a highly reflective Ag BR in a flat device.

4.3 External textures

Alternative to the internal textures introduced previously are external textures that offer the advantage of an easy integration while at the same time not directly influencing the electrical properties of the device, as they are not in contact with any of the active layers. We introduce LM foil on top of the PV-module – at the air / encapsulation interface, while keeping all other interfaces flat – see Figure 1(a, c).

Feature sizes of the presented textures are in the range of several micrometers, which requires geometrical optics to be used in this case. Textures importantly affect redirection of reflected and transmitted light, resulting in possible multiple entering events as well as redirection of rays propagating inside the structure. Similar as with internal textures, external textures were also tested with different BR. In general, results indicate an increase in Jsc for all BR. With better reflecting Ag BR, higher gains in Jsc are achievable, similarly as with internal textures. Slightly higher improvements compared to internal textures are noticeable for poorly reflecting Mo BR.

Simulation results reveal that a LM foil with an Ag BR increases the J_{sc} up to 33.07 mA/cm^2. For Mo and Mo/Al_2O_3 BR, J_{sc} is also increased compared to the structure without the LM foil to 29.65 mA/cm^2 and 30.46 mA/cm^2, respectively. Although values are much higher than with textured Mo BR, these are still well below standard 1800 nm CIGS cell. Comparing EQE_{opt} and R (not shown here) of a standard cell with a cell with LM foil reveals that the LM foil improves R over the entire wavelength range, minimizing reflection losses and as a result higher A_{CIGS} can be observed over the entire spectrum, not only at longer wavelengths as with textured BR. Again, we can notice that external textures without improved BR, similarly to internal textures, do not enhance the J_{sc} enough to match or exceed standard the 1800 nm cell (see Figure 3). On the other hand, the usage of external textures in combination with a good BR (Ag), compensates for the reduced CIGS absorber layer thickness (1800 -> 500 nm) and similar to internal textures, although only slightly, exceeds the

standard thick CIGS cell. By optimization of the LM foil texture (e.g. aspect ratio) or by using different textures, even higher J_{sc} could be achieved [12].

4.4 Experimental results on external texture

To check the improvements related to the external LM foil and validate the predictions of optical simulations ultra-thin CIGS solar cells (d_{CIGS} = 330 nm in this case) were fabricated on a flat substrate. Details on solar cell fabrication can be found in [28]. Mo was used as a rear contact material. An *EQE* of individual cells is measured in three different configurations: i) a bare cell, ii) a cell with added glass layer and iii) a cell with added glass layer and a LM foil. Both, glass and LM foils are attached to the solar cell using BK-7 matching liquid (Cargille laboratories, n (589.3 nm) = 1.5167 @ 25 °C). This enables us to measure the same cell in three different configurations, eliminating possible deviations between different cells and, thus, contributing measured differences entirely on changed optical properties due to added glass and external texture. In simulations, ideal extraction of charge carriers is assumed as in previous cases, while in the experimental case, due to the use of an ultra-thin absorber, charge carrier recombination losses at the back contact may start to affect carrier collection and extraction. To compensate for this non-ideal extraction all simulated *EQE*s are corrected by the same constant factor of 0.85. This enables us to compare simulation and measurement results in absolute scale.

In Figure 4(b), a selected case of *EQE* measurements of a cell in (i), (ii) and (iii) configurations are presented, while in Figure 4(a) simulation results are given. First, we can notice the same trends in measured and simulated cases for all tree configurations. Next, adding a non-absorbing glass already increases the *EQE* resulting in an average of 3 % (simulated 2.8 %) J_{sc} improvement. Moreover, adding LM foil on top of the glass additionally increases the *EQE* over the entire spectrum, improving J_{sc} in average by additionally 5 % (simulated 6.2 %).

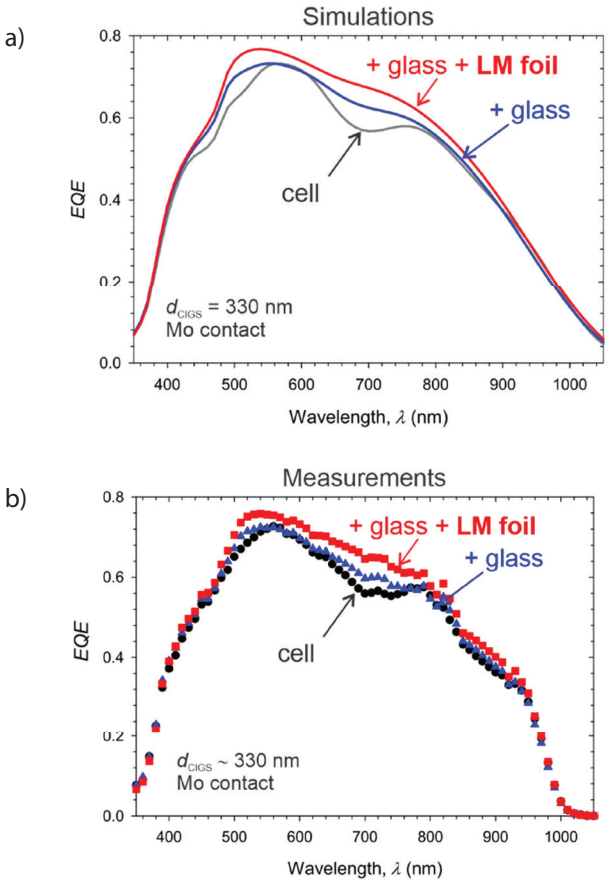

Figure 4: (a) Simulated and (b) measured *EQE* of an ultra-thin CIGS cell (d_{CIGS} = 330 nm) in three configurations: bare cell (i) – black lines&symbols, with added front glass (ii) – blue lines&symbols and with added glass and LM foil (iii) – red lines&symbols. Differences in long wavelength range can be contributed to different bandgap of fabricated and simulated CIGS absorber.

5 Conclusion

Using optical modelling we first analyzed the main J_{sc} loss factors of a CIGS module when thinning down the absorber layer. Comparison between modules with a thick and thin absorber reveals highly reduced long-wavelength absorption in CIGS and mainly enhanced parasitic absorption at the poorly reflecting Mo back contact of the thin module. To increase the J_{sc} of the thin module we first introduce, in simulations, a highly reflective Ag BR, that effectively reduces absorption losses at the back contact, but still an improved J_{sc} of 30.85 mA/cm^2 does not match the J_{sc} of the device with the thick absorber. To further improve the J_{sc}, an additional texturing of the BR in combination with realistic layer growth was introduced in the simulations. Highly increased J_{sc}, surpassing the one of the thick device was observed for the Ag BR, with best result of J_{sc} = 34.75 mA/cm^2. Besides internal nanotextures, external microtextures were investigated by adding textured LM foil with O dome shaped texture on the front side of the flat device. A high J_{sc}, slightly surpassing a thick standard module, was observed when using the LM foil in combination with the flat Ag BR. For external textures, an experimental verification on ultra-thin (d_{CIGS} = 330 nm) cells with Mo BR was carried out. Predicted improvements related to the LM foil were confirmed.

The usage of textures (internal and external) was also simulated with standard Mo BR, but in this case only marginal improvements to the J_{sc} were observed, much lower than with the use of alternative highly reflective BR (flat or with textures). Higher improvements in J_{sc} for thin CIGS absorbers can be achieved using an alternative highly reflective BR, compared to introducing textures in combination with a standard Mo BR. Although to compensate for the J_{sc} drop of thin CIGS, a combination of highly reflective back contact and introduction of textures (internal or external) is needed.

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